OFDM synchronization scheme for Power Line Telecommunications (PLT)

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Abstract

This paper presents a new scheme for OFDM time and frequency synchronization with application in Power Line Telecommunications (PLT).
Simulation results show an excellent behavior, even for the low values of SNR in the synchronizer input inherent to PLT.
The synchronizer has been prototyped on an FPGA prior to be integrated in the single-chip PLT system.
Keywords: OFDM time and frequency synchronization, Power line communication, PLT, FPGA.

1. Introduction

The basic idea of multicarrier modulation (MCM) is to divide the available spectrum in several sub channels. In a classical FDM (Frequency Division Multiplexing) system, narrow-band signals are generated independently, assigned to various frequency bands, parallel transmitted, and separated by filters at the receiver [1].
In an OFDM (Orthogonal Frequency Division Multiplexing) system, the information is parallel mapped into *N*-QAM (Quadrature Amplitude Modulation) signals and multiplexed using a FFT (Fast Fourier Transform) [2].
This technique has been considered for broadband applications including both wired and wireless applications. In the case of radio transmissions, OFDM is used in normalized Digital Terrestrial Video Broadcasting (DTVB) and Digital Audio Broadcasting (DAB), both standards from ETSI. In addition, ETSI-BRAN family of recommendations (Broadband Radio Access Networks technical body) has selected this transmission technique for HIPERLAN/2 (High Performance Local Area Network) [3].
Wired applications, such as ADSL (Asymmetric Digital Subscriber Line) or HDSL (High-bit-rate DSL), employ OFDM techniques (also called DMT: Discrete Modulation Technique) to deliver high bit rates to the end user. [4].
Recently OFDM has been suggested for Power Line Telecommunications (ETSI-PLT Technical Body and [5]). This technology will be able to provide a new local broadband access as well as indoor data networking using ordinary power lines installed in every home and office.
This paper presents an algorithm to provide both, coarse and fine synchronization, for an OFDM system in Power Line Telecommunications (PLT). The outline of this paper is as follows:
Section 2 describes the principles of classical OFDM systems. It will summary the key aspects of the OFDM modulation, as well as its advantages and drawbacks. Section 3 illustrates the effects of synchronization errors in OFDM. Section 4 presents a synchronization scheme to provide time and frequency synchronization in a PLT transceiver, and some simulation results. Section 5 shows a hardware implementation on an FPGA and, finally, in Section 6 some conclusions are drawn.

2. OFDM description

The first OFDM system was proposed in 1971 by Weinstein and Ebert [6]. Since powerful silicon technology was not available at this time, the development of OFDM based systems was certainly delayed until nowadays.
In an OFDM system (see figure 1), the incoming information signal *S* is parallel mapped using an ordinary constellation to obtain complex samples. *N* of these complex samples $X_{k,p}$ ($k = 0,..,\ N\text{-}1$) are transformed by an iFFT to constitute the *p*-th OFDM symbol (see equation 1). As a result, $x_{n,p}$ is a discrete base band sequence of *N*-QAM carriers.

$$x_{n,p} = \sum_{k=0}^{N-1} X_{k,p} e^{\frac{-2\pi kn}{N} j} \qquad n = 0,1,..,N\text{-}1 \qquad (1)$$

A guard interval, called Cyclic Prefix (CP), with *M* samples, is added to the output of the iFFT in order to avoid possible ISI (Inter Symbol Interference).

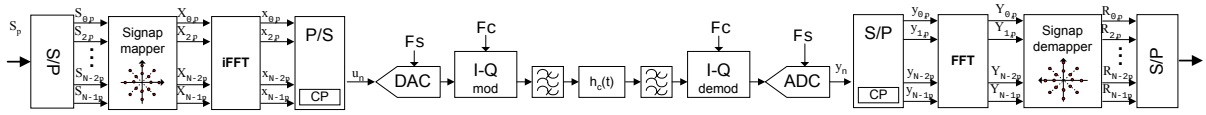

Fig. 1. OFDM system overview

This cyclic prefix is a copy of the last *M* samples of the OFDM symbol that is pretended to be transmitted and it is a pure system overhead that reduce the base band bandwidth required by a factor $\eta=N/(M+N)$.

The discrete base band signal is analogue converted (DAC-Fs) and up mixed to the channel frequency F_c. The resulting signal is expressed in equation 2, where *t* is the absolute time, *T* is the OFDM symbol duration, *N* is the number of sub carriers and $X_{k,p}$ is the constellation point carried by the *k*-th sub carrier of the *p*-th OFDM symbol. The individual spectra are now orthogonal *sinc* functions and the total bandwidth *B* is divided into *N* equidistant narrow band sub channels.

$$z(t) = \sum_{p=-\infty}^{+\infty} \left[\sum_{k=-N/2}^{N/2-1} X_{k,p} e^{j\left(2\pi(t-pT)\frac{\eta}{T}+2\pi F_c t\right)} \right] \qquad (2)$$

The most important advantage of OFDM systems when compared to single carrier systems is obtained in broadband applications over frequency selective channels (radio channels, power line channels, etc). Equalization in OFDM is reduced to a simple multiplication of each sub carrier by a complex factor, whereas equalization in single carrier transmission may not be feasible or introduces large delays.

OFDM produces much grater immunity to impulse noise and fast fades due to its long symbol time. In addition, the cyclic prefix inclusion reduces ISI, even when using an Analogue Front End (AFE) with large order FIR filters.

Difficulties regarding OFDM are: peak-to-mean-power ratio that requires an extremely high linear amplifier to reduce OOB (Out-Of-Band) Interference, and the requirement of accurate time and frequency synchronization.

3. Synchronization errors in OFDM

Time and frequency synchronization between transmitter and receiver are of crucial importance in terms of system performance [3].

A frequency mismatch between transmitter and receiver causes a lost of orthogonality that will reduce the useful signal amplitude and will lead to Inter Carrier Interference (ICI). Both impairments cause an important BER degradation. OFDM systems are orders of magnitude more sensitive to frequency offset and phase noise than single carrier systems [7].

A time offset in the FFT time window estimation causes phase rotation in frequency domain. The output symbol within the OFDM symbol is rotated by a different angle. From subcarrier to subcarrier, the angle increases proportionally to the frequency offset. In OFDM systems with coherent detection this rotation has to be properly corrected. However, under non-coherent detection, this incremental offset does not decrease system performances since the information is carried in phase offsets between consecutive symbols.

If the estimated start position of the FFT window locates within the data interval, the sampled OFDM symbol will contain some samples that belong to other OFDM symbol. The phase rotation imposed by OFDM symbol synchronization error can thus be corrected by appropriately rotating the received signal, but the dispersion of signal constellation caused by ISI forms a bit error BER floor due to the presence of unrecoverable samples.

In conclusion, the use of a synchronization scheme which avoids OFDM symbol estimation error, will lead to an effective decrease in the length of the cyclic prefix, reducing its overhead. In this case, the cyclic prefix length can be reduced until the floor level imposed by the multi-path and fading channel feature.

The most important synchronization methods in OFDM are presented in [8]-[15].

Fig. 2. Burst structure

4. Synchronization algorithm

A time frequency synchronization scheme for burst based transmissions is proposed here. It will be integrated into a PLT system.

As other burst based transmission systems, the OFDM frame is structured as shown in figure 2. The preamble is depicted in figure 3 and consists of three different sections (A, B and C).

Section A is considered for preamble detection, gain adjustment (normally performed by an external Programmable Gain Controller), and coarse timing

estimation. Fine frequency and time tuning are done in the B section. The C-Field is reserved for channel estimation.

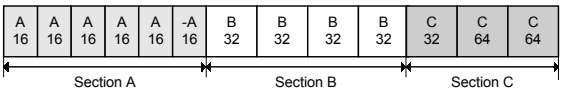

Fig. 3. Header detail description

An auto-correlation scheme has been selected for preamble detection and coarse timing synchronization (figure 4). The received signal is delayed by the correlation delay *D* (16 samples). Conjugate complex samples of the delayed version are multiplied by the received samples. Resulting products are feed into the moving average block, whose window size is *W=64* samples, and then they are post-processed for threshold detection and maximum search in order to find the correct timing.

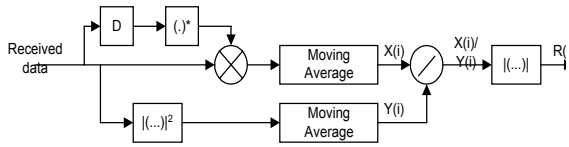

Fig. 4. Autocorrelation scheme

Figure 5 shows the auto-correlator output for section A in presence of AWGN input noise. Note that a threshold value is required a) to minimize the probability of false preamble detection within the data field of a MAC (Medium Access Layer) frame, and b) to filter out small peaks in the auto-correlator output due to input noise. However, a large threshold value decreases the probability of correct preamble detection within the preamble field of a MAC frame. After exhaustive simulation, it has been found that a threshold value of 0.55 represents a good compromise.

Noise and multi-path signal propagation over power-line channels produces broader peaks at the auto-correlator output, reducing the accuracy of the timing recovery process. This coarse synchronization can reduces the burden of the fine timing process. Simulations results show that the maximum error introduced by the coarse timing proces, when the peak of the *R(i)* signal is above the threshold value, is only +/-4 samples.

Fine timing is achieved by using matched filters. Since the maximum error is +/-4 samples, a bank of nine matched filters is required, one for each possible sample delay. It has to be noted that with the four B-fields of the preamble only three complex multiplication and three additions per sample are needed, a much lower load than the 32 complex multiplications and the 32 additions needed if a cross correlation is done over all the incoming samples. Figure 6 shows the filters outputs in the case of AWGN input noise.

Due to frequency deviation between transmitter and receiver oscillators, the received base band signal has a time varying phase component which deteriorates the OFDM demodulation.

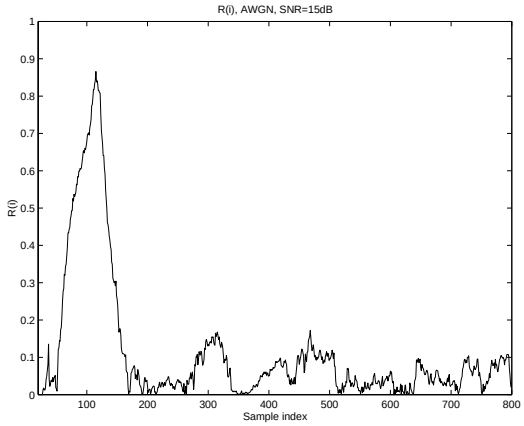

Fig. 5. Auto-correlator output. A section

The process for the estimation of frequency deviation is depicted in figure 7 and it is done in parallel with the fine timing process. Starting with the first sample of the first B-field, the incoming signal is delayed by the delay *D* (32 samples). The conjugate complex samples of the delayed signal are multiplied by the received samples. The output is then averaged over 96 products (until the end of the B-field). Straightforward analysis shows that the angle of the result *Y* is proportional to frequency deviation.

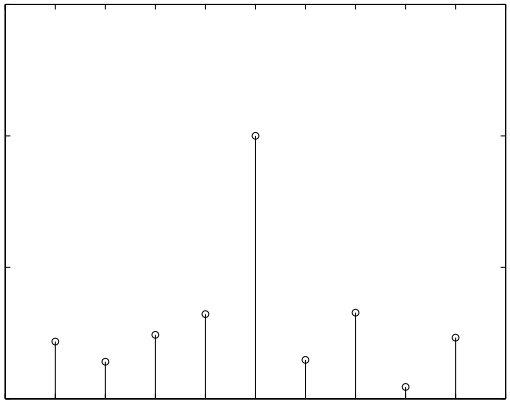

Fig. 6. Matched filters output. B section.

Frequency correction can be easily performed by complex multiplication of the in-phase and quadrature *n*-th input sample with $e^{j\,\Delta\omega\,n}$, where $\Delta\omega$ is the estimated frequency deviation.

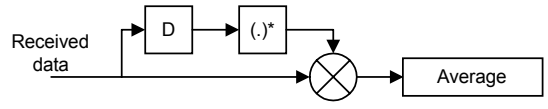

Fig. 7

5. Hardware implementation

Previous sections described a new scheme for time and frequency synchronization with application to PLT. A hardware implementation of this scheme, called Hypersynch Module (HSM), has been done using VHDL. HSM has been implemented trying to save as much silicon area as possible while fitting it into the system clock requirements.

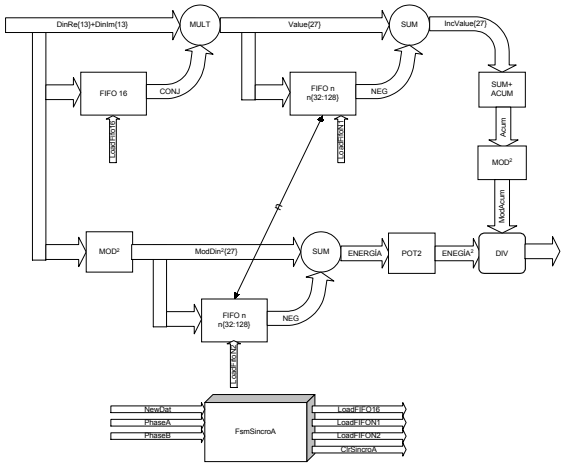

Fig. 8 Section A architecture

First of all, regarding possible time-sharing of hardware resources, coarse and fine synchronization with sections A and B of the preamble are made in different time intervals, sharing hardware resources such as memories, adders and multipliers. Second, those arithmetic operations which are too slow or which consume large silicon area, such as square root and divisions, are avoided, by using power-of-two coding of the internal signals. Finally, pipeline techniques has been introduced in order to reduce delay chain and optimize critical paths. Figures 8 and 9 shows a brief description of the solution adopted for both blocks and hardware resources consumed. They show their own memory blocks, but in the final system the module is shared. For avoiding square roots all the quantities are squared. Before being integrated on the final chip, HMS has been prototyped on an Xilinx Virtex-XV300 FPGA (form HADES-1 System [16]) using Foundation 3.3i The complete system required no more than 50.000 system gates excluding memories, and working at 33 MHz.

The whole system (Base Band Processor) has been also introduced using the same environment and has been rated to 80.000 system gates at 33MHz. The prototype has been run using a XSV-800 board and the on-chip memory for stimuli injection. The results has been compared with Matlab high level simulations, and all the quantization errors and other effects has been validated the FPGA emulation approach.

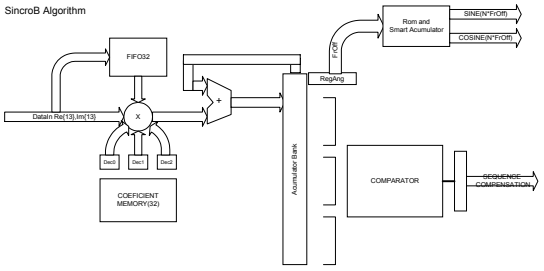

Fig. 9 Section B architecture

6. Conclusions

Power line communication is now possible with significant advantages over conventional cable industry because it uses the existing electric power infrastructure. However, the physical medium is hard, requiring innovative solutions. In this paper, a new scheme for time and frequency synchronization for OFDM burst transmission is presented as well as its hardware implementation on an FPGA. Simulation results are provided and show the effectiveness of the proposed solution, and an implementation has been made using moderate hardware resources.

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References

[1] H. Rohling, T. May, K. Brüninghaus and R. Grünheid. " Broad band OFDM radio transmission for multimedia applications". Proc. Of the IEEE vol. 87, no. 10, october 1999.

[2] John .A.C. Bingham: "Mullticarrier modulation for data transmission: an idea whose time has come". IEEE Communication Magazine, vol 28, no. 5, pp 5-14, May 1990.

[3] T. Keller and L. Hanzo. "Adaptative multicarrier modulation: a convenient frame work for time-frequency processing in wireless communications". Proc. Of the IEEE, vol. 88, no.5, May-2000.

[4] J.S. Cho, J.C. Tu and J.M. Cioffi, "A discrete multitone transceiver system for HDSL applications". IEEE J. Selected areas Comm., vol.9, pp 895-908., Aug. 91.

[5] A. G. Burr, P.A. Brown. "Application of OFDM to Powerline Telecomunications". Proceedings of 3rd ISPLC, Landcaster. 1999.

[6] S.B. Weinstein and P.M. Ebert, "Data tramsmission by frequency división multiplexing using the Fourier

transform". IEEE Trans. Comm. Tech. Vol com-19, pp 628-634, Oct-1971.
[7] T. Pollet, M. Van Bladel and M. Moeneclaey. " BER Sensibility of OFDM systems to carrier frequency offset and Wiener phase noise". IEEE Tran. On Comm. , vol. 43, no 2-3-4, Feb-Mar-Apr 1995.
[8] P. H. Moose. "A technique for orthogonal frequency division multiplexinfg frequency offset correction". IEEE Trans. Commun., vol. 42, pp. 1590-1598, Oct. 1994.
[9] G. Santella. "A frequency and symbol synchronization system for OFDM signals: architecture and simulation results". IEEE Tran. On Veh. Tech., vol 49, no 1, Jan-2000.
[10] T.M. Schmidl and D.C. Cox. "Robust Frequency and Timing Synchronization for OFDM". IEEE Tran. On Comm., vol 45, no. 12, December 1997.
[11] F. Claβen and H. Meyr, "Frequency synchronization algorithms for OFDM systems suitable for communications over frequency delectiva channels". Proc. VCT-94, pp1655-1659.
[12] M. Speth, F. Claβen and H. Meyr. "Frame synchronization of OFDM systems in frequency selective fading channels". Proc. VTC-97. Phoenix. May 1997.
[13] M. Sandell, J-J van de Beek and P. Borjesson, "Timing and frequency synchronization in OFDM systems using the cyclic prefix". Proc. Int. Symp. Synchronization, Essen, Germany. 1995. pp 16-19.
[14] D. Landström. "Synchronization in OFDM systems". Licentiate in Engineering Thesis. March 1999. Department of Applied Electronics. Lund University (Sweden).
[15] P. J. Langfeld, K. Doster. "OFDM System sychronization for Powerline Communications". Proc. of tne 2000 International Symposium on Power Line Communications and its applicatins. ISPLC'00 pp 15-22.Limerick. Ireland
[16] M.A. Aguirre, J.N. Tombs, A. Torralba and L.G. Franquelo "HADES-1: A Rapid Prototyping Environment based on Advanced FPGA's". Accepted for DCIS'01. Oporto 2001.