Implementation of a closed loop SHMPWM Technique for Three Level Converters

J. Napoles, R. Portillo, J. I. Leon, M. A. Aguirre, L. G. Franquelo
University of Seville
jnl@gte.esi.us.es

***Abstract*- High power converters are built using high-voltage and high-current rated semiconductors. The commutation of these devices imply large amounts of energy per cycle leading to very low switching frequency in order to avoid a high rise on the semiconductors temperature. The consequence is high harmonic distortion generated by the converter. Grid Codes requirements specify the maximum admitted harmonic distortion. The well known Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) technique has proved to be useful in eliminating some of the undesired harmonics without increasing the switching frequency, leaving the rest of them free. The solution to the rest of harmonics is to add bulky and expensive filters. Recently, the method named Selective Harmonic Mitigation Pulse Width Modulation (SHMPWM) has been introduced. The aim of this technique is to mitigate the amplitude of the undesirable harmonics, to acceptable values to meet the grid code, considering a larger number of harmonics. In this paper a practical implementation of this technique in a closed loop scheme is presented. The experimental results using a 150kW three-level Diode-Champed converter show that the output signals meet the EN 50160 and CIGRE WG 36-05 grid codes. Comparisons between SHMPWM and SHEPWM are included in the experiments, showing the superior performances of the SHMPWM technique.**

I. INTRODUCTION

Nowadays grid codes are restricting the harmonic content to guarantee the quality of the power supply. Power conversion is one of the most important topics related to solid state multilevel converters [1][2]. Many papers can be found in the literature related to new control approaches focused on improving the quality of the output signals of the converter [3]-[7].

This paper describes the implementation details of a full operative inverter that is controlled using the Selective Harmonic Mitigation Pulse Width Modulation (SHMPWM) technique using a three level 150KVA diode-clamped prototype acting as an Uninterrupted Power Supply (UPS). SHMPWM [8] deals with keeping all the harmonics of interest under a safe value instead of forcing them to become zero, as in the Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) method [9], in order to be able to meet the grid code (harmonic contents and THD limits) with the minimum number of switching angles per period. The experimental results are compared with those obtained using the same test bench with the well known Selective Harmonic Elimination technique SHEPWM and, as it will be shown, the SHMPWM technique produces a higher performance than SHEPWM. Many papers present works where the SHEPWM technique has been used in multilevel converters [10][11]. The SHMPWM technique was previously introduced in [8] and is able to meet several grid codes with a low switching frequency.

The paper is organized as follows; in section II the principle of the SHMPWM technique is summarized, in section III the implementation details are explained, next section is devoted to the experimental results obtained with the prototype and finally the conclusions of the work are detailed.

II. SHMPWM PRINCIPLE

The SHMPWM technique is based on the fact that it is not necessary to make zero some specific harmonics to meet a certain grid code. The goal is to keep the harmonic content under a safe level below the limit specified by the code. This technique was originally presented in [8] and is able to fulfill the EN 50160 [12] and CIGRE WG 36-05 [13] grid codes with a lower switching frequency than any other modulation technique.

Fig. 1 shows the typical three-level PWM pattern. The Fourier analysis of this kind of signal yields the equations detailed in (1) with n=5.

$$\begin{aligned} H_1 &= \frac{4}{\pi}\left[\sin\alpha_0 - \sin\alpha_1 + \sin\alpha_2 - \ldots + (-1)^n \sin\alpha_n\right] \\ H_2 &= \frac{4}{2\pi}\left[\sin 2\alpha_0 - \sin 2\alpha_1 + \sin 2\alpha_2 - \ldots + (-1)^n \sin 2\alpha_n\right] \\ &\vdots \\ H_k &= \frac{4}{k\pi}\left[\sin k\alpha_0 - \sin k\alpha_1 + \sin k\alpha_2 - \ldots + (-1)^n \sin k\alpha_n\right] \end{aligned} \quad (1)$$

The Selective Harmonic Elimination technique (SHEPWM) originally presented in [9] generates the values of the switching angles to fix H_1 and eliminate certain harmonics. In that case, equations (1) change to (2) where q belongs to the set: (5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49) because the harmonics of interest are only the odd ones non multiple of 3. In this case, only the first 50 harmonics are considered.

$$\begin{aligned} M_a &= \frac{4}{\pi}\left[\sin\alpha_0 - \sin\alpha_1 + \sin\alpha_2 - \ldots + (-1)^n \sin\alpha_n\right] \\ 0 &= \frac{4}{5\pi}\left[\sin(5\alpha_0) - \sin(5\alpha_1) + \sin(5\alpha_2) - \ldots + (-1)^n \sin(5\alpha_n)\right] \\ &\vdots \\ 0 &= \frac{4}{q\pi}\left[\sin(q\alpha_0) - \sin(q\alpha_1) + \sin(q\alpha_2) - \ldots + (-1)^n \sin(q\alpha_n)\right] \end{aligned} \quad (2)$$

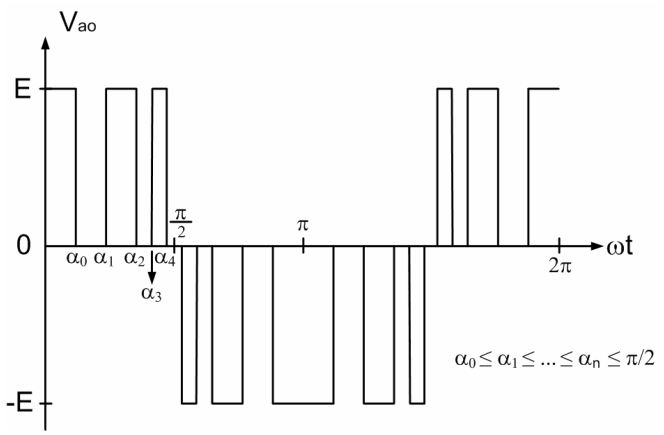

Fig. 1. Three-level Selective Harmonic PWM switching pattern with five switching angles.

The SHMPWM technique, instead of making zero some specific harmonics as in SHEPWM, keeps them below a safe level to meet the grid codes. As a consequence, it is possible to fulfill the grid codes with a lower switching frequency.

The equations are transformed in inequalities as in (3) where E_i are the variables considered in the computing process and L_i are the maximum allowed values. $L_5 \ldots L_{49}$ corresponds to 80% of the limit specified in the grid code. An optimization method can be used to solve the system.

$$\begin{aligned} H_1 &= \frac{4}{\pi}\left[\sin\alpha_0 - \sin\alpha_1 + \sin\alpha_2 - \ldots + (-1)^n \sin\alpha_n\right] \\ E_1 &= M_a - |H_1| \le L_1 \\ E_5 &= \frac{1}{|H_1|}\frac{4}{5\pi}\left[\sin(5\alpha_0) - \sin(5\alpha_1) + \sin(5\alpha_2) - \ldots + (-1)^n \sin(5\alpha_n)\right] \le L_5 \\ E_7 &= \frac{1}{|H_1|}\frac{4}{7\pi}\left[\sin(7\alpha_0) - \sin(7\alpha_1) + \sin(7\alpha_2) - \ldots + (-1)^n \sin(7\alpha_n)\right] \le L_7 \\ &\vdots \\ E_{49} &= \frac{1}{|H_1|}\frac{4}{49\pi}\left[\sin(49\alpha_0) - \sin(49\alpha_1) + \sin(49\alpha_2) - \ldots + (-1)^n \sin(49\alpha_n)\right] \le L_{49} \end{aligned} \tag{3}$$

Inequalities shown in (3) can be collapsed in an Objective Function as in (4).

$$OF(\alpha_0,\ldots,\alpha_n) = \sum_{i=1,5,7,\ldots,49} c_i(E_i)\cdot E_i^2 + c_{THD}(THD)\cdot THD \tag{4}$$

In the present work the Simulated Annealing optimization method has been used [14][15]. The system could be solved using any other optimization method like Tabu Search, Genetic Algorithms [16], Stochastic Evolution, etc due to the fact that all the computation process will be executed offline.

The SHMPWM modulation technique was presented in [8] and studied in deep using an open loop modulation scheme. In the previously published study, the output signal was simply generated switching at the appropriate angle but without any control of the actual output voltage obtained. In this work, a closed loop control system has been designed to maintain the output voltage of the inverter at a desired value even on DC-Link voltage or load changes. This is the scheme typically used in applications such as UPS.

III. Implementation Details

All the experiments have been carried out on the inverter side of a three-level three-phase 150kVA IGBT-based diode-clamped back to back converter (Fig. 2). The rectifier is controlled using the Space Vector Modulation technique to establish the desired DC-link voltage value. The inverter is used to feed a passive RL load with R=120Ω and L=15mH. Both SHMPWM and SHEPWM modulation techniques have been used in order to compare their obtained performance. The main component of the control hardware is a Digital Signal Processor (DSP) that performs the control law as well as the driving of the switches gate signals. Fig. 3 shows the implemented control scheme where the output voltages measurements are compared with the reference one to provide the closed loop input error signal to a Proportional-Integral controller. The same control system has been used with both SHEPWM and SHMPWM.

The switching angles are stored in a memory as the number of clock cycles to wait between two consecutive changes in a 50Hz sine waveform. The memory is being read cyclically and is organized as a two dimensional table where the numbers of waiting cycles of a specific modulation index are stored in the same row. A wide range of Modulation Indexes (Ma) from 0.75 to 1.16 has been used.

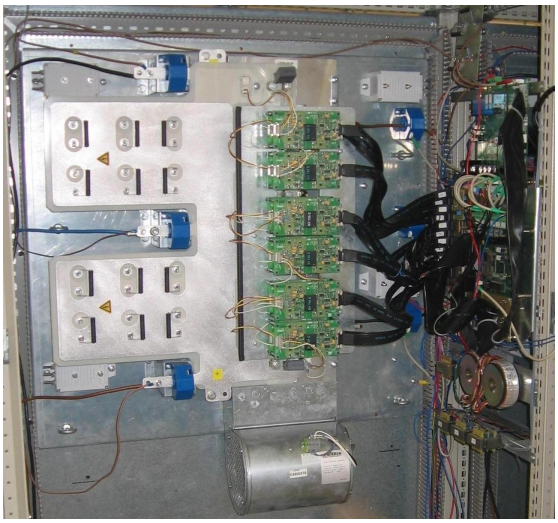

Fig. 2. 150 kVA IGBT-based three-level diode-clamped inverter prototype.

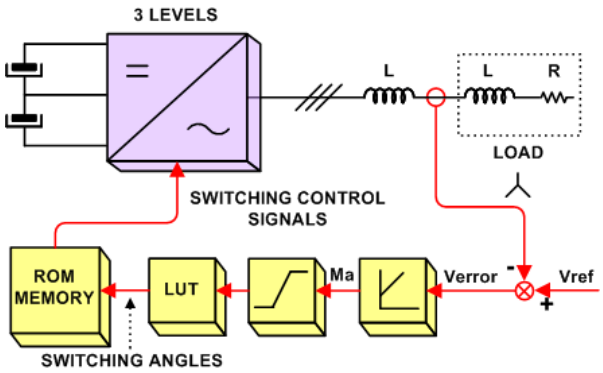

Fig. 3. Power converter schematic and detailed control system implemented.

All the data stored in the memory have been computed off line so for the present implementation the specific algorithm used to solve the inequalities shown in (3) is not relevant. When the converter is running, the memory needs only to be read as in other precomputed PWM techniques like SHEPWM.

The fundamental frequency of the inverter output voltage is 50Hz; the switching frequency that results is 750Hz.

The converter schematic shown in Fig.3 is equivalent to that used in an UPS application replacing the DC-Link capacitors by batteries.

IV. Experimental Results

Several experiments have been carried out in order to check the correct behavior of the system. The results show that the system works properly and complies with all the requirements specified in the related grid codes when the SHMPWM technique is adopted comparing with the classical SHEPWM technique which is not able to meet those codes in the same conditions (f_s=750Hz). Fig. 4 shows one phase output voltage as an example of the waveforms used in the experiments. It can be seen that the switching frequency is very low (15 switching angles per quarter of a period due to symmetry) as it is required in high power applications.

Firstly, an experiment to check all the precomputed data has been made (experiment I). In this experiment, the inverter works in an open loop scheme moving along all the precomputed data for both SHMPWM and SHEPWM techniques testing modulation indexes between 0.75 and 1.16. The worst case results are included in Table I and Fig. 6 and will be analyzed later.

Once the data have been checked, a new experiment closing the control loop is made. This experiment consist of making the rectifier of the back-to-back converter to control the DC-Link total voltage to follow up a ramp varying from 750V to 850V as it is shown in Fig. 5. In addition, on the inverter side, a constant output voltage reference is set so the controller has to act changing the modulation index in order to maintain that reference voltage in the load. This experiment is named experiment II.

Table I shows a comparison between the maximum experimental harmonic values (worst case) obtained with both the SHEPWM and SHMPWM techniques in both experiments. From left to right, for each harmonic order, is represented the maximum value specified by the grid codes and the maximum values obtained using SHEPWM and SHMPWM techniques in both experiments. Next to each column is detailed if the maximum value obtained using that modulation technique is lower than the limit specified by the grid codes. The two final rows represent the THD obtained considering up to both 40^{th} and 50^{th} harmonic orders respectively. The same results are shown in Fig. 6.

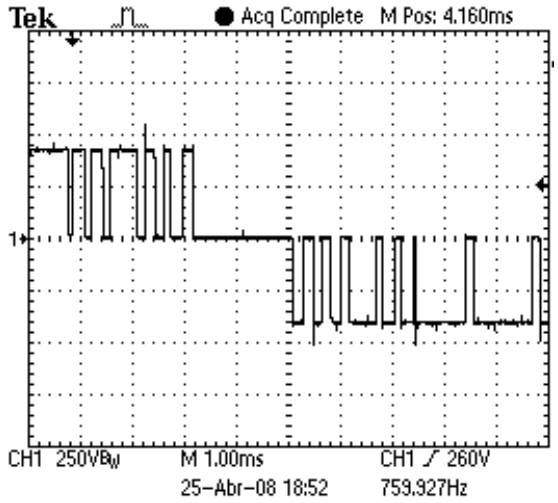

Fig. 4. Half period (1ms) of the measured output voltage pattern using 15 switching angles.

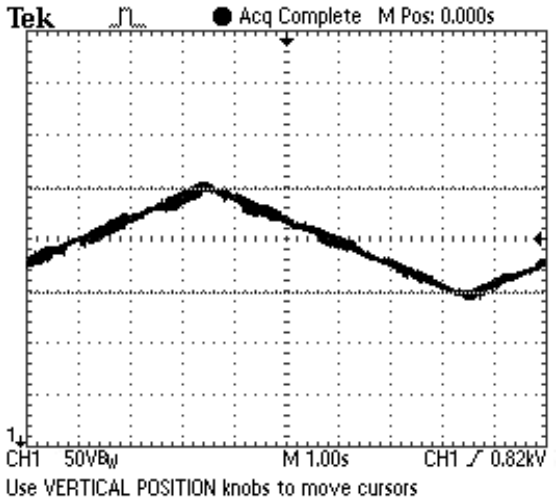

Fig. 5. Ramp in the DC-Link voltage level used to test the closed loop control system.

TABLE I
COMPARISON BETWEEN SHEPWM AND SHMPWM

HARM. ORDER	EN 50160 HARM. LIMITS (%)	SHMPWM				SHEPWM			
		Exp. I (%)		Exp. II (%)		Exp. I (%)		Exp. II (%)	
5	6	3.77	✓	4.88	✓	0.43	✓	0.64	✓
7	5	2.89	✓	3.73	✓	0.34	✓	0.36	✓
11	3.5	2.62	✓	2.62	✓	0.25	✓	0.23	✓
13	3	1.89	✓	2.28	✓	0.18	✓	0.22	✓
17	2	1.39	✓	1.58	✓	0.11	✓	0.13	✓
19	1.5	1.12	✓	1.13	✓	0.06	✓	0.07	✓
23	1.5	0.99	✓	0.9	✓	0.05	✓	0.09	✓
25	1.5	1.04	✓	1.07	✓	0.06	✓	0.1	✓
29	1.32	0.39	✓	0.44	✓	0.06	✓	0.08	✓
31	1.25	0.41	✓	0.44	✓	0.07	✓	0.1	✓
35	1.13	0.37	✓	0.38	✓	0.08	✓	0.11	✓
37	1.08	0.36	✓	0.4	✓	0.18	✓	0.16	✓
41	0.99	0.33	✓	0.32	✓	0.18	✓	0.22	✓
43	0.96	0.38	✓	0.36	✓	0.28	✓	0.39	✓
47	0.89	0.38	✓	0.35	✓	19.95	X	23.81	X
49	0.86	0.36	✓	0.4	✓	9.39	X	17.42	X
THD_{40}	8	6.47	✓	6.68	✓	0.63	✓	0.80	✓
THD_{50}	-	6.47	✓	6.68	✓	20.4	X	24.6	X

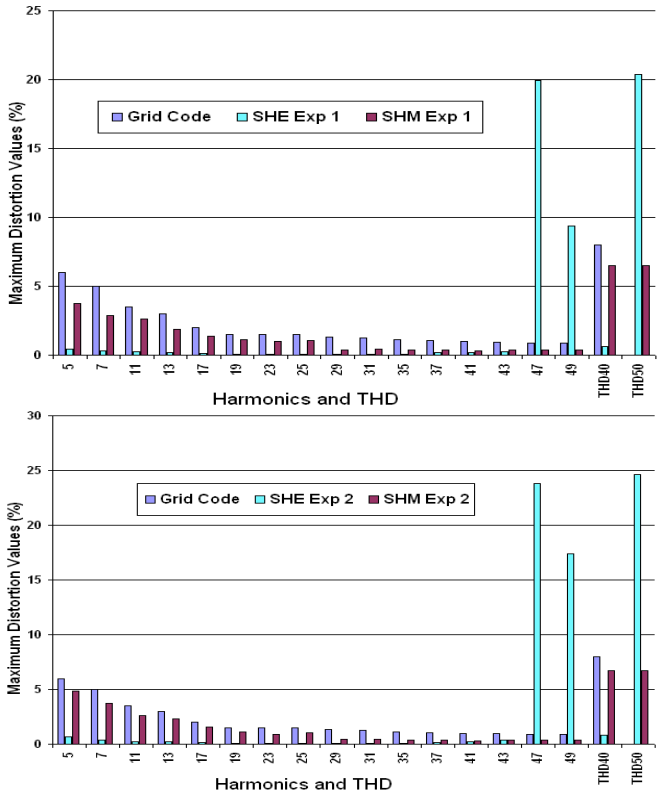

Fig. 6. Maximum harmonic contents obtained in the experimental results in the modulation index range between 0.75 and 1.16.

The results of experiment I show that, using SHMPWM technique, every harmonic into consideration remains under the grid code specific limit and the same happens with the total harmonic distortion, even considering harmonics up to 49th. However, with SHEPWM technique, the precomputed data make almost zero all the harmonics except for harmonics 47th to 49th which are left completely uncontrolled which generates values far over the grid code limits.

The results obtained in experiment II are shown in Fig. 7 to Fig. 12. Fig. 7 to Fig. 11 corresponds to SHMPWM technique whereas Fig. 12 has been obtained using SHEPWM technique. From top to bottom, Fig. 7 shows one phase output voltage, the total harmonic distortion considering harmonics up to 40th (THD_{40}) and the total harmonic distortion considering harmonics up to 50th (THD_{50}). The output voltage average is 280V_{RMS} which corresponds to the imposed reference voltage and exhibits a small oscillation of about 5V_{PP} which is less than 2% of the reference value so it has been considered that the controller adjustment is right. The THD trends limits has been chosen to meet the grid code ones so it can be easily seen that both THD_{40} and THD_{50} meet that specification during the whole experiment.

Fig. 8 to Fig. 11 show the trends for all harmonics under consideration, that is to say, the sixteen shown in Table I, being the lower order harmonic shown upper in the figures. The upper limits of the figures are the limits imposed by the grid codes so it can be easily seen that every harmonic order is under the limit specified in the grid code (with some degree/margin of confidence). The maximum values has been stored in Table 1 as the worst case where can be directly compared with the grid code numeric limits.

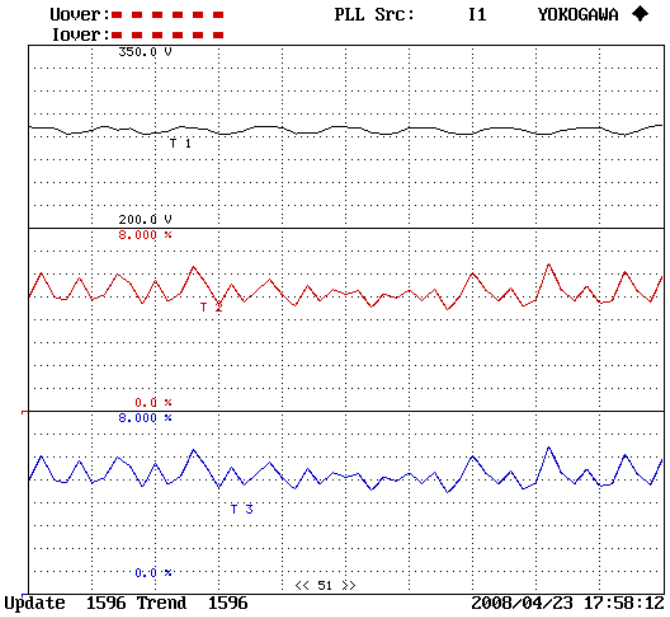

Fig. 7. Results obtained in the second experiment using the SHMPWM technique changing the V_{DC} voltage when V_{REF} = 280V_{RMS}. From top to bottom: output phase voltage, THD_{40} and THD_{50}.

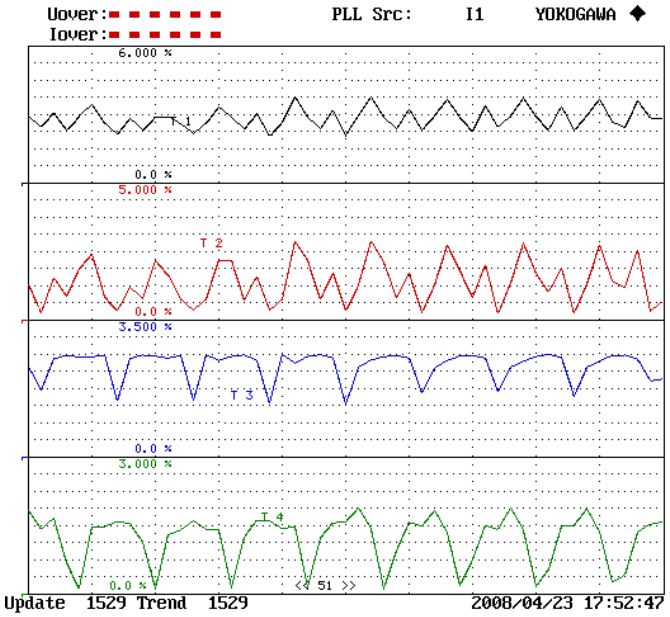

Fig. 8. Results obtained in the second experiment using the SHMPWM technique changing the V_{DC} voltage when V_{REF} = 280V_{RMS}. From top to bottom, harmonics: 5TH, 7TH, 11TH and 13TH.

Fig. 12 shows the results obtained using the SHEPWM modulation technique in the same experiment. In this case, only harmonics 41st, 43rd, 47th and 49th have been represented due to the fact that in this technique all the harmonics from 5th to 43rd are zero (for this switching frequency). The limits of the two upper trends have been adjusted again to meet the

grid codes requirements while in the two lower trends, the limits have been adjusted to keep the whole trace into the plot. This experimental result shows that both 41st and 43rd harmonics are very close to zero whereas the rest that are not zeroed are completely uncontrolled. Both 47th and 49th harmonics reach very high levels far over the limits specified in the grid codes.

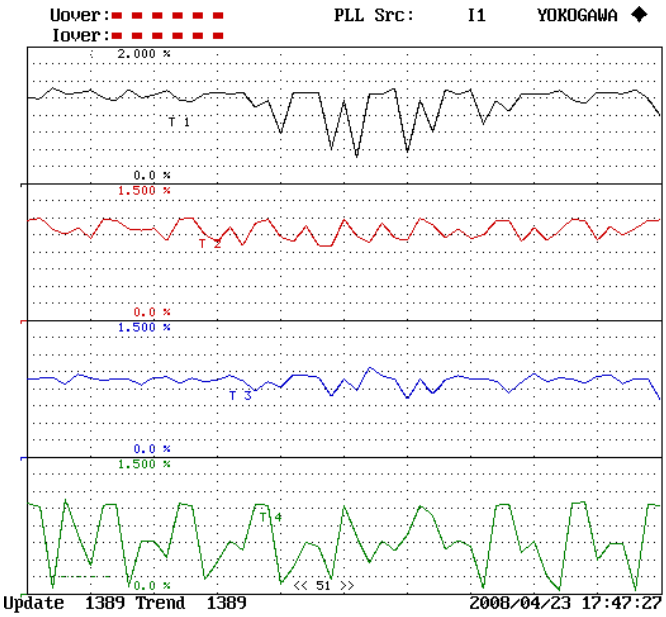

Fig. 9. Results obtained in the second experiment using the SHMPWM technique changing the V_{DC} voltage when V_{REF} = 280V_{RMS}. From top to bottom, harmonics: 17TH, 19TH, 23RD and 25TH.

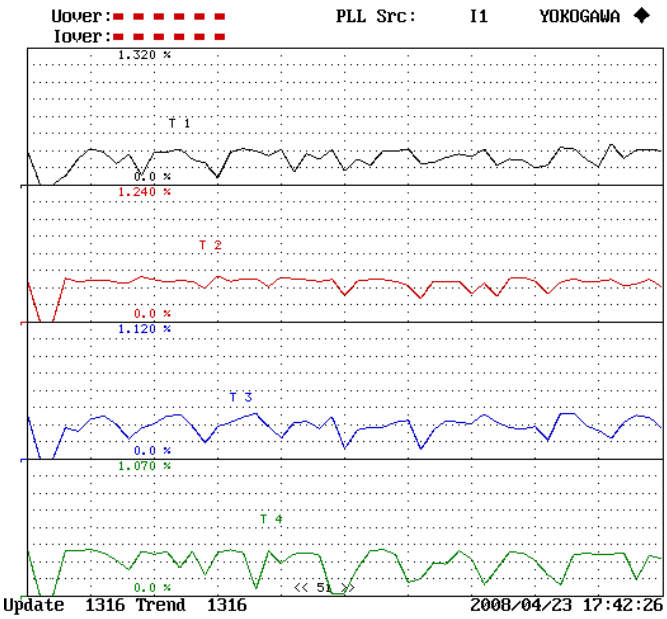

Fig. 10. Results obtained in the second experiment using the SHMPWM technique changing the V_{DC} voltage when V_{REF} = 280V_{RMS}. From top to bottom, harmonics: 29TH, 31ST, 35TH and 37TH.

It must be noticed that the maximum THD_{40} obtained using the SHEPWM is very low and under the limit specified in the grid codes. The reason is that using 15 switching angles, using this technique, harmonics up to 43rd can be reduced to zero. When the THD is obtained considering up to harmonic 50th, the value is much higher than the THD_{40} and above the limit specified in the grid codes. Using the SHMPWM both THD_{40} and THD_{50} are very similar because all the harmonics are considered in the computing process.

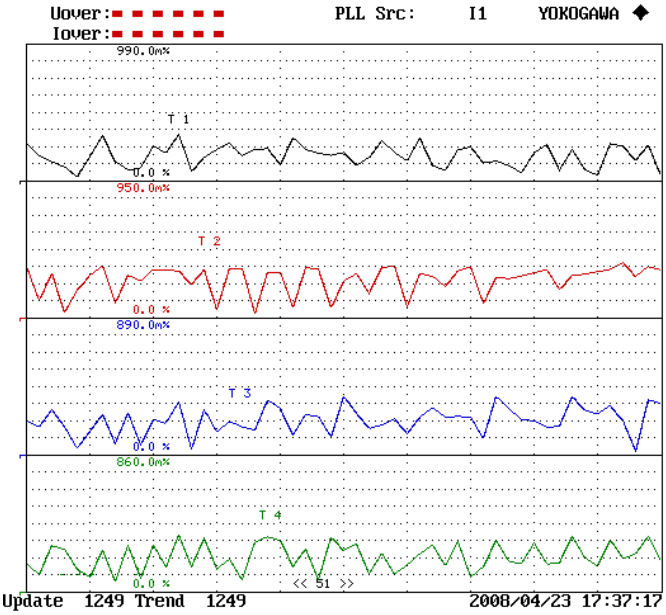

Fig. 11. Results obtained in the second experiment using the SHMPWM technique changing the V_{DC} voltage when V_{REF} = 280V_{RMS}. From top to bottom, harmonics: 41ST, 43RD, 47TH and 49TH.

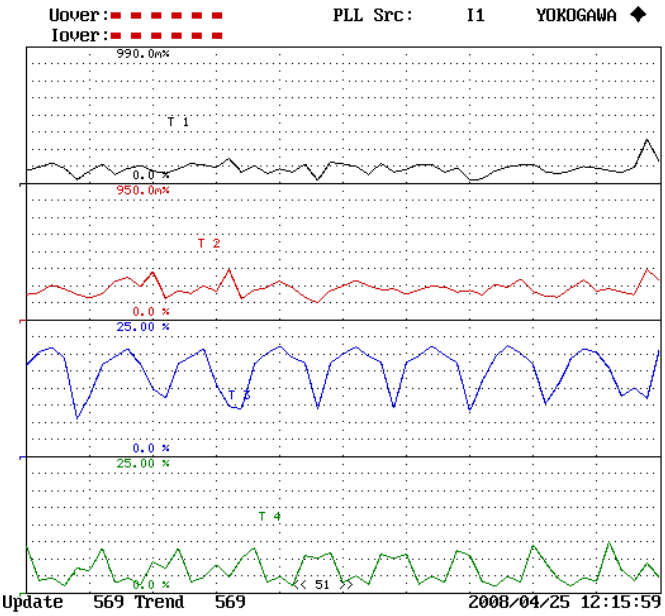

Fig. 12. Results obtained in the second experiment using the SHEPWM technique changing the V_{DC} voltage when V_{REF} = 280V_{RMS}. From top to bottom, harmonics: 41ST, 43RD, 47TH and 49TH.

The limit specified in the grid codes for the 47^{th} and 49^{th} harmonics are very low so, when the final value obtained using SHMPWM are under that limit, their contribution to the THD_{50} is not very significant.

As a conclusion of the experimental results, the table shows that the SHMPWM is able to meet the grid codes in all the range of Ma and when the converter is following in a closed loop a specific output phase voltage reference established by the user. In contrast, the SHEPWM technique is not able to fulfil the codes in the same conditions (with the same switching frequency). The reason is that it generates output signals with low order harmonics close to zero but leaves completely uncontrolled all the non considered harmonics. In this case (750Hz due to it is a three levels converter), the 47^{th} and 49^{th} harmonics maximum output values are far over the limits specified in the grid codes.

V. CONCLUSIONS

The work presented in this paper validates the SHMPWM modulation technique in closed loop applications such as UPS, and fulfilling the EN 50160 and CIGRE WG 36-05 grid codes with a very low switching frequency.

All the experiments have been carried out in the inverter side of a three-level three-phase 150kVA IGBT-based diode-clamped back-to-back converter using both SHMPWM and SHEPWM techniques in order to compare the results.

The experimental results show that the performance obtained using the SHMPWM technique is much better than using the SHEPWM technique due to the fact that as the grid codes are completely fulfilled, any extra filtering system is not required. This is very interesting because, in high power applications, the reactive elements are very bulky and expensive. The SHEPWM is not able to meet the codes unless the switching frequency is increased from 750Hz to 850Hz with the additional power losses and heating generation associated.

The SHMPWM technique can be used in any other multilevel converter topology simply repeating the computing process adapting to the new topology (if necessary) and changing the switching rules.

Is interesting to detail that all the experiments have been carried out focusing on applications such as UPS but the SHMPWM technique is suitable to be used in any other application.

Bearing all this in mind, the SHMPWM modulation technique is a very good alternative in high power applications where a very low switching frequency is required and the reactive elements used to filter the undesired harmonics are very bulk and expensive.

REFERENCES

[1] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng; "Multilevel inverters: a survey of topologies, controls, and applications", on IEEE Transactions on Industrial Electronics, Volume 49, Issue 4, Aug. 2002, pp. 724 – 738.

[2] J. M.Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. Portillo, M. M. Prats, J. I. Leon and N. Moreno-Alfonso, "Power-Electronic Systems for the Grid Integration of Renewable Energy Sources: A Survey", on IEEE Transactions on Industrial Electronics, Volume 53, Issue 4, June 2006 Page(s):1002 – 1016.

[3] M. Prodanovic and T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection", IEEE Transactions on Power Electronics, Volume 18, Issue 1, Part 2, Jan. 2003, pp. 373 – 380.

[4] R. Teichmann, M. Malinowski, S. Bernet, "Evaluation of three-level rectifiers for low-voltage utility applications," Trans. on Industrial Electronics, vol. 52, no. 2, pp. 471- 481, Apr 2005.

[5] M. Marchesoni, P. Segarich and E. Soressi, "A new control strategy for neutral-point-clamped active rectifiers", Trans. on Industrial Electronics, vol. 52, no. 2, pp. 462- 470, Apr 2005.

[6] A. Dell'Aquila, M. Liserre, V.G. Monopoli and P. Rotondo, "An energy-based control for an n-H-bridges multilevel active rectifier," Trans. on Industrial Electronics, vol. 52, no. 3, pp. 670- 678, Jun 2005.

[7] J.E. Espinoza, J.R. Espinoza, L.A. Moran, "A systematic controller-design approach for neutral-point-clamped three-level inverters," Trans. on Industrial Electronics, vol. 52, no. 6, pp. 1589- 1599, Dec 2005.

[8] L. Garcia Franquelo, J. Nápoles, R. C. Portillo Guisado, J. Ignacio León and Miguel A. Aguirre, "A Flexible Selective Harmonic Mitigation Technique to Meet Grid Codes in Three-Level PWM Converters," Trans. Industrial Electronics, Volume 54, Issue 6 Dec. 2007 p.p. 3022-3029.

[9] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters—Part 1: Harmonic elimination," IEEE Transactions on Industry Applications, vol. IA-9, May/June 1973, pp. 310–317.

[10] J. N. Chiasson, L. M. Tolbert, Keith J. McKenzie and Zhong Du, "A Complete Solution to the Harmonic Elimination Problem", IEEE Trans. On Power Electronics, Volume 19, Issue 2, March 2004 p.p. 491-499.

[11] Zhong Du, L. M. Tolbert, J. N. Chiasson and B. Ozpineci, "Reduced Switching-Frequency Active Harmonic Elimination for Multilevel Converters", IEEE Trans. On Industrial Electronics, Volume 55, Issue 4, April 2008 p.p. 1761-1770.

[12] CENELEC EN 50160, "Voltage characteristics of electricity supplied by public distribution systems", 2001.

[13] CIGRE WG 36-05: "Harmonics, characteristic parameters, methods of study, estimates of existing values in the network", Electra No.77, 1981, S.35-54.

[14] S. Kirkpatrick, C. D. Gelatt Jr. and M. P. Vecchi, "Optimization by Simulated Annealing", Science, Vol. 220, Nº 4598, 1983, pp. 671-680.

[15] M. Huang, F. Romeo, and A. Sangiovanni-Vincentelli, "An efficient general cooling schedule for simulated annealing", in IEEE International Conference on Computer-Aided Design,1986, pp. 381-384.

[16] K.L. Shi, Hui Li, "Optimized PWM strategy based on genetic algorithms," Trans. on Industrial Electronics, vol. 52, no. 5, pp. 1458-1461, Oct 2005.