Controller Design for a Single-Phase Two-Cell Multilevel Cascade H-Bridge Converter

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***Abstract*- In this paper is studied the single-phase two-cell multilevel cascade H-bridge power converter connected to the grid, acting as a synchronous rectifier. The power exchange process between the cells of the converter and the grid is analyzed. Based on this analysis and on the power converter model the stages of the controller design process are shown. A new controller for the cascade power converter is proposed, achieving the regulation of each DC-Link capacitor voltage towards its reference. The proposed controller includes a repetitive scheme in the current tracking loop, providing low current harmonic content and almost unity power factor. Simulation results have been carried out in a 10 kVA single-phase two-cell multilevel cascade H-bridge power converter model to illustrate the good performance of the proposed controller.**

***Index Terms*— Multilevel converter, power quality, non-linear control.**

I. INTRODUCTION

Multilevel cascade converters, also named cascaded H-bridge converters, were first presented in 1988 [1]. Since then they have been a focus of researchers because they present several advantages compared with other multilevel converter topologies in terms of modularity, simplicity and number of levels with minimum number of power semiconductors [2]-[4].

Different applications have been developed using the multilevel cascade converter: Synchronous rectifiers [5], renewable energy integration systems [6], inverters [7], Statcoms [8] and active filters [9]. For each application, specific control strategies have been designed, being the DC-Link voltages control the most important challenge in this power converter topology.

The DC-Link voltages control problem is not a trivial issue in the cascaded multilevel topology. As in other multilevel converters, the voltages control task can be approached through modulation or as a part of the system controller. When the modulation is used to control the output voltages, the redundant output states of the converter are used. In [10] this fact is used to regulate the outputs voltages to the same reference value. When the control approach is used, a specific control has to be designed to carry out the voltages control task. Due to this multiple signals are needed, one for each H-bridge, making the controller design more complex. However the advantage is that the output voltage references can be set independently. Several strategies to achieve the voltage balance can be found in the literature such as a passivity control strategy [11], non-linear control strategy [12], and strategies based on PI controllers [13].

In this paper the controller approach will be considered. To develop the controller design the power exchange process between the cells of the cascade converter and the grid is analyzed. From this analysis, the power flow limits as a function of the output voltage values will be pointed out, and finally the controller expression is derived.

II. SYSTEM DESCRIPTION

A single-phase two-cell multilevel cascade H-bridge power converter (CHB) is depicted in Fig. 1. The system is connected to the grid through a smoothing inductor L, and it is assumed that pure resistive loads R_1 and R_2 are connected to each DC-Link capacitor C_1 and C_2 respectively. The system parameters and variables are described in TABLE I, where the continuous control signals δ_1 and δ_2, which represent the switching functions have been defined.

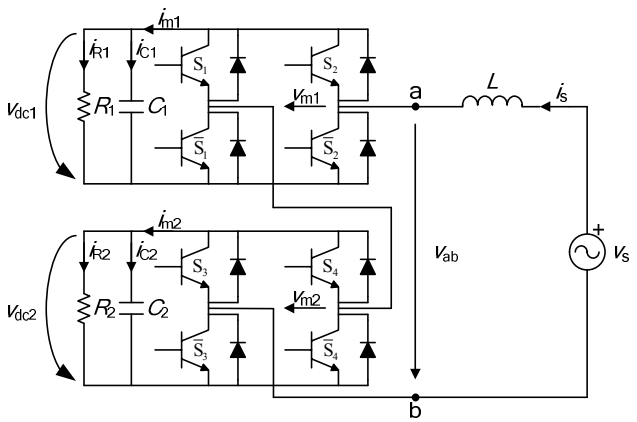

Fig. 1 Single-phase two cell multilevel cascade H-Bridge converter

TABLE I

SYSTEM PARAMETERS

Parameter	Description
L	Inductance
C_1; C_2	Capacitances
R_1; R_2	Resistive loads
$i_s(t)$	Grid current
$v_s(t)$	Grid voltage
i_{R1}; i_{R2}	Load currents
V_{dc1}; V_{dc2}	Capacitor voltages
δ_1;$\delta_2 \in [-1, 1]$	Control signals

The equations that describe the CHB behavior are well known and they have been reported in several previous works [14], these equations are

$$v_{m1} = \delta_1 V_{dc1} \quad (1)$$

$$v_{m2} = \delta_2 V_{dc2} \quad (2)$$

$$v_s = L\frac{di_s}{dt} + v_{m1} + v_{m2} \quad (3)$$

$$v_{m1} i_s = C_1 \frac{d}{dt}\left(\frac{V_{dc1}^2}{2}\right) + \frac{V_{dc1}^2}{R_1} \quad (4)$$

$$v_{m2} i_s = C_1 \frac{d}{dt}\left(\frac{V_{dc2}^2}{2}\right) + \frac{V_{dc2}^2}{R_2} \quad (5)$$

In these equations the control signals v_{m1} and v_{m2} defined in (1) and (2) have been introduced. These signals represent the voltages that are modulated in each cell. The equation that represents the input current dynamic is (3) and the output capacitor DC voltages dynamics are (4) and (5).

To analyze the controller design stages, the power exchange between the cells of a cascade converter and the grid has to be studied. For this purpose the power converter representation of Fig. 2 is used. In this representation the cells have been replaced by voltage sources with values equal to the instantaneous voltages modulated by the cells, v_{m1} and v_{m2} respectively. The active and reactive power consumed or injected by each cell depend on the shift angle between the current i_s, and the modulated voltage in the cell (v_{mi}). This can be analyzed using the phasorial diagram of the cascade power converter represented in Fig. 3.

Now the following assumptions are made:

(i) The voltages v_{dc1} and v_{dc2} are lower than the peak value of v_s

(ii) Cell 1 and cell 2 consume active power, and no reactive power is drawn from the grid.

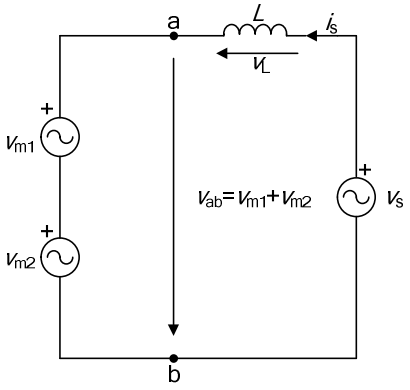

Fig. 2 CHB representation through voltage sources

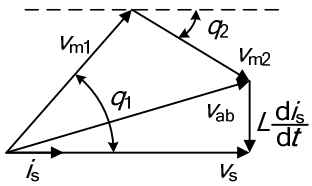

Fig. 3 CHB phasorial diagram of voltages and current

For a given power consumption p_1 and p_2 in each DC-Link, the theoretical reference voltages for each H-bridge can be determined. The total amount of active power that has to be drawn from the grid is

$$p_T = p_1 + p_2;\ p_1 > 0;\ p_2 > 0 \quad (6)$$

The necessary grid current and the associated inductor drop (v_L) can be then calculated and therefore the voltage that should be modulated between the points ab of the converter can be determined.

$$i_s = \frac{p_T}{v_s^2\big|_{RMS}} v_s \quad (7)$$

$$v_L = L\frac{di_s}{dt} \quad (8)$$

$$v_{ab} = v_s - v_L \quad (9)$$

The voltage v_{ab} is composed by the sum of the output voltage of the cells, v_{m1} and v_{m2}. For this reason, the DC-Link capacitor voltage values are constraints that should be considered when the load is applied, because only certain phasors compositions are allowed. Fig. 4 shows the phasors of all voltages involved. The set of points that can be reached for a given DC-Link capacitor voltage values is represented using a market region. An example of valid point is shown in Fig. 4a. Any point outside of this region would make the system unstable because the reference voltage of one cell or both can not be modulated with the actual values of the DC-Link capacitor voltages as is shown in Fig. 4b.

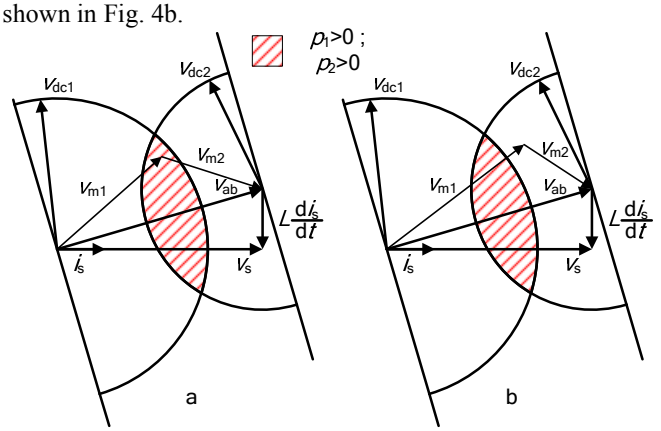

Fig. 4 Reference voltage between points ab. a) Solution inside the reachable region b) Solution outside the reachable region

For a given total amount of power p_T, the values of power that can be consumed in each cell can not be chosen freely. Fig. 5a and Fig. 5b show the minimum value of active power that should be consumed in cell 1 and cell 2 respectively, to maintain the system stability.

Among the possible solutions, only those points where the active power consumed by each cell corresponds with p_1 and p_2 respectively are valid solutions for the system. For instance, from p_1 it is possible to calculate the projection of v_{m1} over i_s as

$$v_{m1p} = \frac{p_1}{i_s\big|_{RMS}} \quad (10)$$

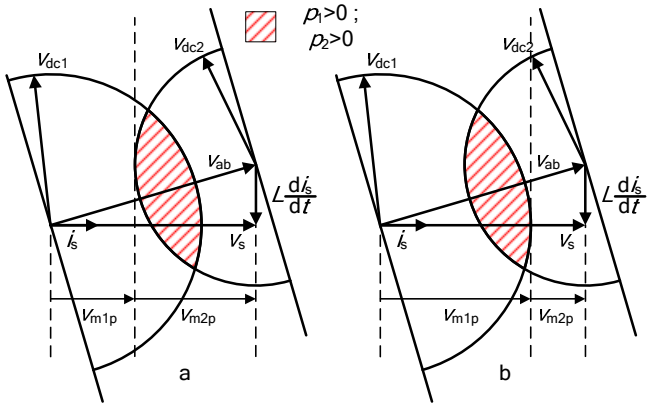

Fig. 5 Minimum values of active power must be consumed by the cells for a consumed total amount of active power p_T. a) Minimum value of p_1. b) Minimum value of p_2

This fact leads to calculate the value of the projection of v_{m2} over i_s, and to determine the possible points to obtain a valid solution. These points are located over the line orthogonal to v_s placed a distance v_{m1p} from the origin. The valid solutions are the points which simultaneously belong to that line and are inside the set of points that can be reached with the DC voltage values in cell 1 and 2. Fig. 6 shows the set of possible solutions for power consumption p_1 and p_2, which are located between the points MN.

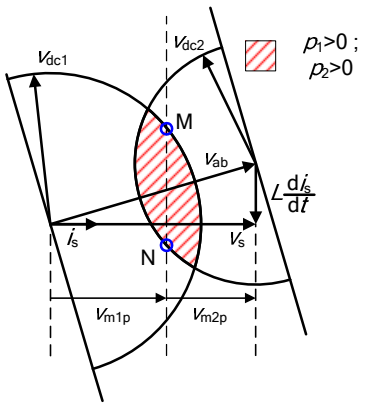

Fig. 6 Set of possible solutions for p_1 and p_2

It is worth pointing out that there is not a single solution for the system. The only restriction is that the solution has to be located between points MN, and therefore there is one degree of freedom which can be used to optimize the converter behavior and design. Fig. 7 shows two possible solutions for the system. Both solutions lead to the same result drawing active power p_1 and p_2. The only difference is the reactive power value delivered or consumed by each cell.

III. Controller Design

To design the controller two facts must be considered, the total voltage regulation and the voltages ratio. The total voltage regulation is related with the sum of the DC-link capacitor voltages, and the voltages ratio is defined as the ratio between the DC-link capacitor voltages of the cells of the converter, meaning for instance that if DC voltage ratio is *k:1* in a two-cell CHB, then $v_{dc1}=k\cdot v_{dc2}$.

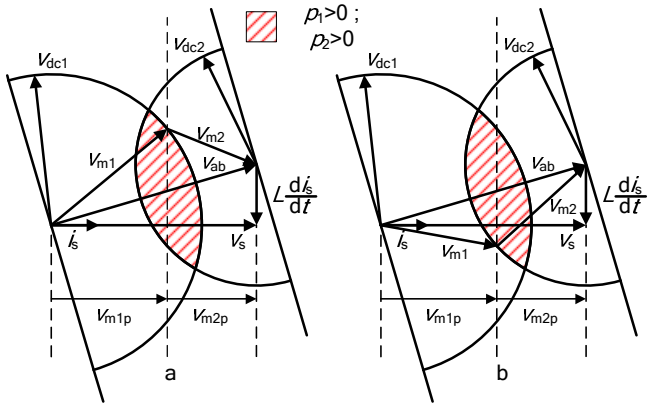

Fig. 7 Two possible solutions to achieve the same active power consumption p_1 and p_2 in each cell respectively.

For the control law design, it is assumed that the switching frequency is high enough to consider the control signal as a continuous signal. Due to this fact the averaged model of the system can be used to develop the controller. Also it is assumed that the current dynamic is faster than the voltage regulation and ratio dynamics of a CHB converter. Finally the control design is split in three stages:

(i) Voltage regulation control loop, which ensures capacitor voltage regulation towards its reference. The output of this loop is the current reference.

(ii) Current control loop, which ensures inductor current tracking towards its reference. The output of this controller is the control signal $u=v_{m1}+v_{m2}$.

(iii) Voltage ratio control loop, which ensures capacitor voltage ratio towards its reference. The output of this controller are the control signals v_{m1} and v_{m2}.

The control objectives are:

(i) Regulate the capacitor voltages to the desire values V_{dc1}^* and V_{dc2}^*

(ii) Achieve inductor current with high quality harmonic content and maintain the power factor as close to unity as possible.

A. *Voltage regulation control loop*

The averaged part of equations (4) and (5) can be used to obtain the necessary input active power to regulate the DC-Link voltages.

$$z_1 = \frac{V_{dc1}^2}{2} \qquad z_2 = \frac{V_{dc2}^2}{2} \qquad (11)$$

Introducing the variables z_1 and z_2, equations (4) and (5) are transformed in

$$p_1 = C_1 \frac{dz_1}{dt} + \frac{2z_1}{R_1} \qquad (12)$$

$$p_2 = C_2 \frac{dz_2}{dt} + \frac{2z_2}{R_2} \qquad (13)$$

Equations (12) and (13) are well-known LTI systems, thus the values of p_1 and p_2 can be calculated through a PI controller as in [15], yielding to the following expressions

$$p_1 = \frac{k_{p1}}{s+\tau_{s1}}\tilde{z}_1 + \frac{k_{i1}}{s}\tilde{z}_1 \qquad (14)$$

$$p_2 = \frac{k_{p2}}{s+\tau_{s2}}\tilde{z}_2 + \frac{k_{i2}}{s}\tilde{z}_2 \qquad (15)$$

Controllers (14) and (15) include a low pass filter in the proportional term to reduce the high frequency noise, the parameters k_{p1}, τ_1, k_{i1}, k_{p2}, τ_2 and k_{i2} are design positive non-zero constants and the error and the references values are calculated as

$$\begin{aligned} \tilde{z}_1 &= z_1^* - z_1 \\ \tilde{z}_2 &= z_2^* - z_2 \\ z_1^* &= \frac{\left(V_{dc1}^*\right)^2}{2} \\ z_2^* &= \frac{\left(V_{dc2}^*\right)^2}{2} \end{aligned} \qquad (16)$$

The total amount of active power that the voltage source should provide is the sum of p_1 and p_2, and then the current reference can be calculated as

$$\begin{aligned} i_{RMS}^* &= \frac{(p_1+p_2)}{v_{RMS}} \\ i^* &= i_{RMS}^* \frac{v_s}{v_{RMS}} \end{aligned} \qquad (17)$$

B. Current control loop

Equation (3) represents the inductor current dynamic, to simplify the control design process the control signal u is defined as

$$u = v_{m1} + v_{m2} \qquad (18)$$

Thus the inductor current dynamic is transformed in

$$v_s = L\frac{di_s}{dt} + u \qquad (19)$$

Equation (19) is equal than the current dynamic equation for the single-phase H-Bridge converter and the three-phase two-level power converter. Several linear and non-linear controllers have been proposed to achieve the current tracking in those power converters, in [16]-[17] a repetitive control scheme is proposed for the current tracking process, and in this work the same solution is adopted.

$$u = v_s + k_{pc}\cdot\tilde{i}_s + k_r\left(\frac{1-K\cdot e^{-\frac{s\pi}{\omega}}}{1+K\cdot e^{-\frac{s\pi}{\omega}}}\right)\tilde{i}_s \qquad (20)$$

$$\tilde{i}_s = i_s - i_s^* \qquad (21)$$

The parameters k_{pc}, k_r and K are positive non-zero design constants. Equation (20) is the expression for the control signal u and (21) is the current error definition. In (20) the proportional term adds damping to the controller to ensure stability and the repetitive term represents an estimation of v_L^*.

$$v_L^* = L\frac{di_s^*}{dt} \qquad (22)$$

C. Voltage ratio control loop

As it is shown in section II, the voltage modulated by each cell (v_{mi}) together with the grid current must provide the active power and the reactive power demanded by the cell. The active power demand is satisfied when the projection of v_{m1} and v_{m2} over i_s are defined respectively as

$$v_{m1p} = \frac{p_1}{i_{RMS}^*}\cdot\frac{v_s}{v_{RMS}} \qquad (23)$$

$$v_{m2p} = \frac{p_2}{i_{RMS}^*}\cdot\frac{v_s}{v_{RMS}} \qquad (24)$$

Besides, to achieve unity power factor the reactive power delivered by the cells must be equal to the reactive power demanded by the smoothing inductor. In addition, to ensure current tracking (20) must be satisfied. To carry out all these constraints the reference voltages in each cell are defined as

$$v_{m1} = v_{m1p} + k_{pc1}\cdot\tilde{i}_s + k_1 k_r\left(\frac{1-K\cdot e^{-\frac{s\pi}{\omega}}}{1+K\cdot e^{-\frac{s\pi}{\omega}}}\right)\tilde{i}_s \qquad (25)$$

$$v_{m2} = v_{m2p} + k_{pc2}\cdot\tilde{i}_s + k_2 k_r\left(\frac{1-K\cdot e^{-\frac{s\pi}{\omega}}}{1+K\cdot e^{-\frac{s\pi}{\omega}}}\right)\tilde{i}_s \qquad (26)$$

where the following restriction must be satisfied

$$k_1 + k_2 = 1 \qquad (27)$$

$$k_{pc1} + k_{pc2} = k_{pc} \qquad (28)$$

where the parameters k_{pc1}, k_{pc2}, k_1 and k_2 are positive non-zero design constants. The constans k_1 and k_2 represent how the reactive power is shared between the cells.

IV. Simulation Results

In this section simulation results are shown in order to test the proposed controller using a prototype. For this purpose the single-phase two-cell multilevel cascade H-bridge power converter has been considered. The experiment consists of a load step from no-load to full load, including different capacitor voltages reference. To modulate the reference voltage a phase-shifted PWM strategy has been used. To assess the controller performance, measurements of DC-Link capacitor voltages, grid voltage and currents are represented. TABLE II shows the electrical parameters of the power converter, switching and sampling frequencies that have been used in the model.

Fig. 8 shows the obtained results for the complete experiment period. The experiment has three steps. In the first step, the DC-Link capacitor voltage references are set to 200V in both cells. Once the reference is achieved, a load step is introduced connecting a 20Ω resistor in each DC-Link.

TABLE II

ELECTRICAL PARAMETERS OF THE SYSTEM

Grid Voltage	230 V
Grid frequency	50 Hz
Smoothing inductance	1 mH
DC-Link capacitor C_1	4700 µF
DC-Link capacitor C_2	4700 µF
Switching frequency	10 KHz
Sampling frequency f_m	10 kHz

The second step is carried out when the steady state is reached, and then the DC-Link capacitor voltage reference of the cell 1 is set to 300V. Finally, the third step is introduced when cell 1 achieves its reference, in this moment the DC-Link capacitor voltage reference of cell 2 is set to 100V. As it can be seen in Fig. 8 the proposed control strategy is capable to regulate each DC-Link capacitor voltages to the desired values, and to control the grid current.

From Fig. 9 and Fig. 10 it is demonstrated that the proposed controller has good performance in transient and steady state conditions when a load step is applied. When a reference DC voltage step is applied in any cell the same good behavior is obtained as is shown in Fig. 11 and Fig. 12.

Fig. 9a shows the DC-Link capacitor voltages transient response when the loads are connected and the voltage references are 200V. Fig. 9b shows the corresponding grid current and voltage. Fig. 10a shows the DC-Link capacitor voltages in steady state. It can be noticed that the references are achieved, the 100 Hz ripple in the voltages is due to the active power consumption. Fig. 10b shows the grid voltage and current in steady state. It can be observed that the grid current has high quality and is almost in phase with the grid voltage.

Fig. 11a shows the DC-Link capacitor voltages transient response when the reference for cell 1 is changed from 200V to 300V and the reference for cell 2 is maintained in 200V. It can be noticed that in a few grid cycles the reference is achieved, and the voltage in cell 2 is almost not affected by the reference change in cell 1. In Fig. 11b it can be observed that the grid current increases until the DC-Link capacitor voltage is stabilized in the new reference value.

Fig. 12 shows similar result compared with Fig. 11 when the reference for the cell 2 is changed from 200V to 100V and the reference for the cell 1 is maintained in 300V.

V. CONCLUSIONS

In this paper a single-phase two-cell multilevel cascade H-bridge power converter connected to the grid, acting as a synchronous rectifier is studied. From the analysis of the power exchange process between the cells of the converter and the grid, it is demonstrated that for a given total active power consumption the active power sharing between the cells can not be chosen freely. The controller design stages are shown, and following these stages a controller is proposed, using in the current tracking loop a repetitive control scheme. Simulation results have been developed and it has been verified that the proposed controller provides DC-Link capacitor voltages regulation and ratio control. Besides the proposed repetitive scheme provides current with low harmonic content and also it is capable to achieve almost unity power factor, providing a very good performance of the overall system.

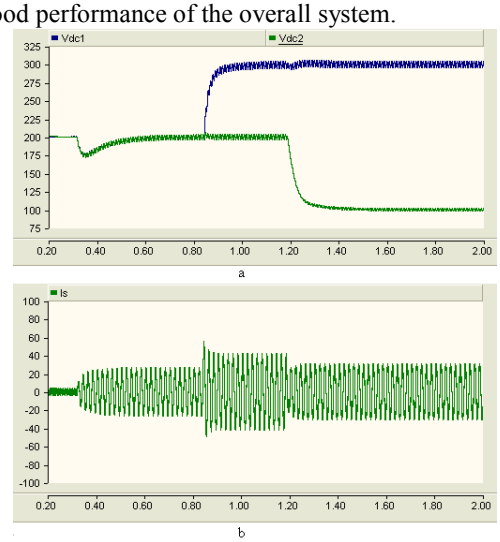

Fig. 8 Curves for the complete experiment period. a) v_{dc1} and v_{dc2} b) i_s

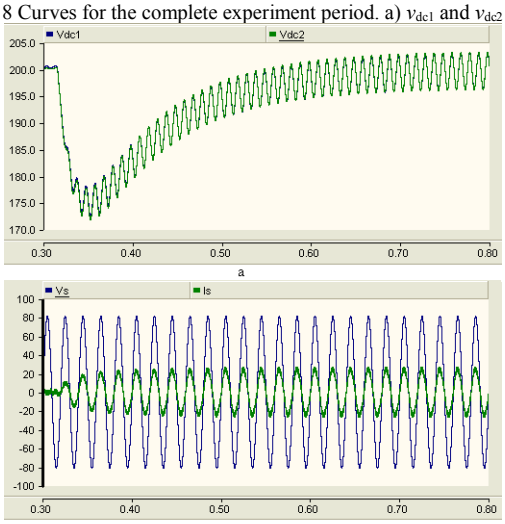

Fig. 9 Capacitor voltages and grid current transients with DC voltage references equal to 200V for both cells. a) v_{dc1} and v_{dc2} b) v_s, and i_s

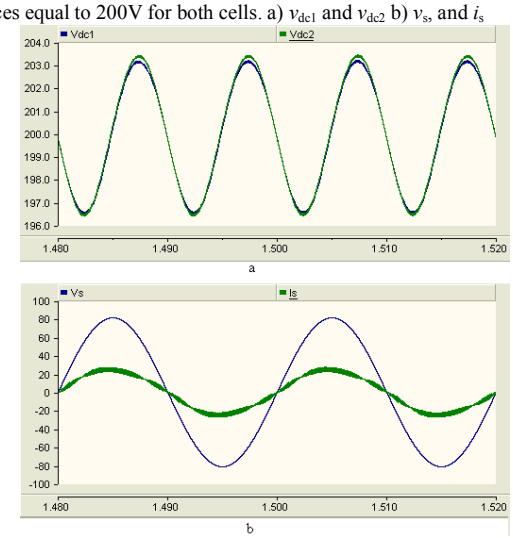

Fig. 10 Capacitor voltages and grid current details in steady state, with DC voltage references equal to 200 V for both cells. a) v_{dc1} and v_{dc2} b) v_s, and i_s

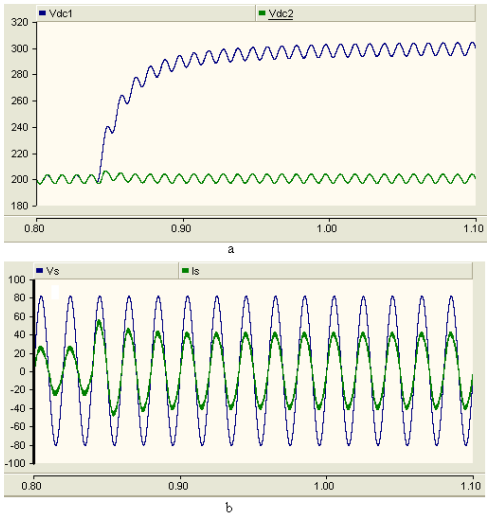

Fig. 11 Capacitor voltages and grid current transients with DC voltage references equal to 300V for cell 1 and 200 V for cell 2. a) v_{dc1} and v_{dc2} b) v_s, and i_s

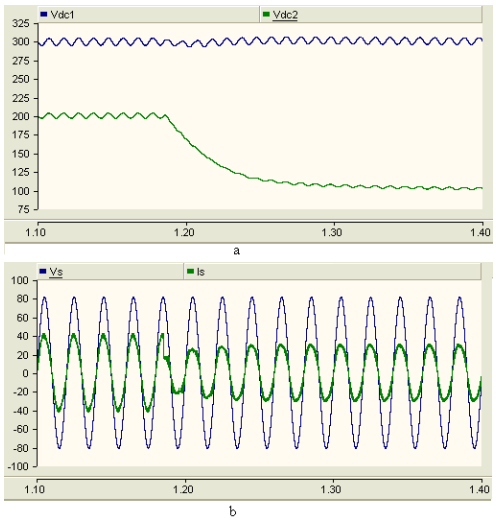

Fig. 12 Capacitor voltages and grid current transients with DC voltage references equal to 300V for cell 1 and 100 V for cell 2. a) v_{dc1} and v_{dc2} b) v_s, and i_s

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