Continuous Time Filter Design Using Stochastic Logic

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***Abstract*—Stochastic logic is based on digital processing of random pulse stream. In this paper we propose a stochastic approach to the digital implementation of continuous time filters. The similarity between probability and Boolean algebras is exploited to obtain simple realizations. A design of a fourth order filter is presented.**

I. Introduction

Stochastic systems make pseudo analog operations using stochastically coded pulse sequences [1], [2]. Information is represented by the statistical mean value of a pulse sequence. In a binary logic, it is codified as the probability of taking a "high" level. Such a sequence can be generated by comparing a register to a random number generator (Fig. 1). Equation 1 give us the probability of an output high level.

$$P(Output =" 1") = \frac{Digital\ Value}{2^n} \qquad (1)$$

A probability can not be exactly measured but only estimated as the relative frequency of "high" levels in a long enough sequence. As a consequence, the stochastic computing technique introduces errors in the form of variance when we attempt to estimate the number from the sequence.

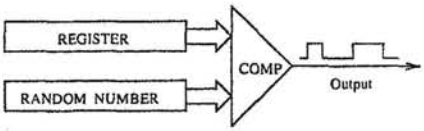


Fig. 1. Digital to stochastic conversion (DSC).

The two most common arithmetic operations on stochastic signals are multiplication and summation, shown in Fig. 2. Assuming that two stochastic signals are stochastically uncorrelated, the product of both of them can be computed by a single AND gate. Summation is a more difficult operation to perform. The simplest way is to use wired OR summation [3], but it is a non linear scheme: as the probability of "high" levels increase, pulse overlap also increases, and the summation saturates gradually (Fig. 2b). Nevertheless, for low pulse densities is an accuracy enough approach. Other techniques to perform summation are described in [4]–[6]. A low pass RC filter that integrates stochastic pulses is well suited to obtain its analog mean value.

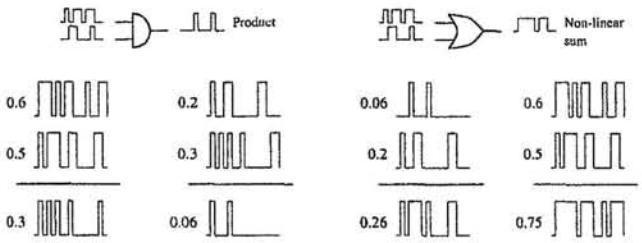


Fig. 2. Stochastic multiplication and summation.

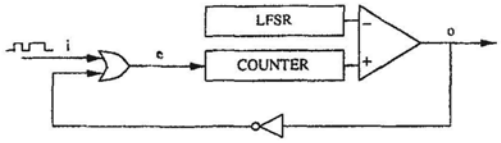
In this paper, we introduce a new approach to digital signal processing using stochastic logic. The information carried out by a random pulse stream is dynamically processed with the elemental operations described before. The only premise is that the stochastic computation must be several order of magnitude faster than input signal dynamics.

II. Low pass filter

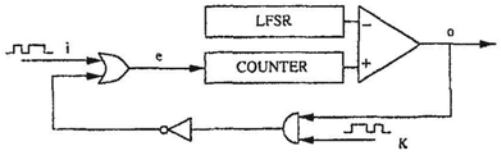
Fig. 3a illustrates the basic scheme of a first order system. The input signal is stochastic pulse stream representing a sinusoidal waveform. This analog information may be recovered with an analog low pass filter [7]. The input signal is compared with the output one with the block ADDER. Basically, this block is developing a wired OR summation, but taking into account a positive and a negative sign. It is a combinational module that implements the following equations:

$$\begin{aligned} add(x_k, y_k) &= x_k \oplus y_k + x_k\overline{(sig(x_k) \oplus sig(y_k)} \\ sig[add(x_k, y_k)] &= x_k sig(x_k)(\bar{y}_k + sig(y_k)) + \\ &\quad y_k sig(y_k)(\bar{x}_k + sig(x_k)) \end{aligned} \qquad (2)$$

The OR summation technique is justified because the output of the ADDER block is an error signal. So, it is a low density pulse stream. The error is time integrated with an up/down counter and then stochastically converted with a digital random number generator, following the scheme of figure 1. The most typical random number generator



(a) First order system with unity gain factor



(b) First order system with 1/k gain factor

Fig. 3. Low pass filter scheme.

for stochastic computing is a linear feedback shift register (LFSR) [8] that allows a very simple and low area cost implementation of a random number generator.

The output signal is a stochastic pulse sequence that follows the input pulse stream, but with a dynamic that depends on the counter size and the clock frequency [9]. Particularly, the time constant and the cutoff frequency of the system described is:

$$\tau = \frac{2^n}{F_{clk}} \qquad f_c = \frac{1}{2\pi\tau} = \frac{F_{clk}}{2\pi 2^n} \tag{3}$$

where n is the counter size and F_{clk} the system clock frequency. The system transfer function is then given by:

$$G(s) = \frac{1}{1+s\tau} \tag{4}$$

The output is digitally available, from the counter, or analogically available, through an external low pass filter.

It can be noticed that our first order system has an infinite input impedance and a zero output impedance. So, it can be serialized to obtain higher order systems, but without loosing a unity gain. An equivalent analog systems appears in Fig. 4. In fact, a gain factor can

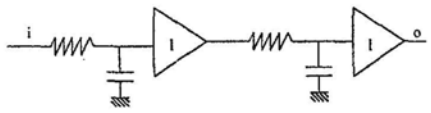


Fig. 4. Equivalent analog systems with impedance isolation.

be easily introduced (Fig. 3b). A k factor is introduced in the feed-back loop to achieve a $1/k$ gain. The only restriction is that stochastic representation of information is ranged from 0 to 1. As a consequence, the input signal multiplied by the gain factor $1/k$ must not exceed a unity value, because there is a saturation effect. Nevertheless, it is not a heavy restriction if we scale the whole problem to the required range. With a gain factor, the system transfer function is:

$$G(s) = \frac{1/k}{1+s(\tau/k)} \tag{5}$$

From this equation it can be observed that a gain factor produces a proportional increment in the time constant.

III. High pass filter

The high pass filter can be obtained from the low pass one. The output pulse stream in Fig. 5 is obtained sub-

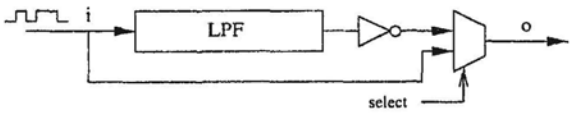


Fig. 5. High pass filter scheme.

tracting the input pulse stream with the low pass filter output. In this case, a sign summation can not be performed using the OR technique, because we are not working with low pulse densities. An alternative solution is a multiplexed scheme. Using a multiplexor, we avoid pulse overlap, but the information is divided by two. To eliminate correlations, a stochastic bit sequence of the LFSR with probability 0.5 is utilized as the select input if the multiplexor [10].

The high pass filter transfer function is given by:

$$G(s) = \frac{s\tau}{1+s\tau} \tag{6}$$

With the gain factor k, the new transfer function is:

$$G(s) = \frac{(k-1)+s\tau}{k+s\tau} \tag{7}$$

IV. Analog to stochastic conversion

A digital to stochastic and a stochastic to digital converter is well known in the literature and has been extensively used from the beginning of stochastic computation [11]–[13]. An analog to digital and digital to analog converter based on stochastic logic has been also developed in [14]. But there is not a clear structure to implement an analog to stochastic conversion. An analog random signal generator [15] may be used, but we propose a mixed analog/digital approach to this conversion, using a generalization of the first order system described before. In Fig. 6 there is a basic scheme for this conversion. The analog input signal $v_i(t)$ is compared with the stochastic pulse sequence integrated with simple RC integrating circuit. and the resulting error signal is integrated with the up/down counter. This structure is similar to the

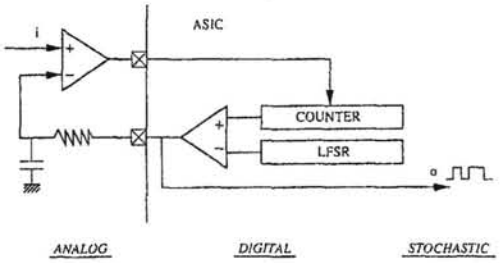


Fig. 6. Analog to stochastic conversion.

stochastic first order system, but with an external analog comparator that leads to a PWM representation of information, instead of an error signal proportional to the input difference.

RC integrating circuit dynamic must be higher than the input signal $v_i(t)$ dynamic. Again, we have a first order system with a transfer function determined by the counter size and frequency clock. Cutoff frequency is given by equation 3.

V. Practical realization

As an example, we have composed the previous circuits to obtain a fourth order low pass filter and a first order high pass filter. The block diagram of the 4^{th} order one is shown in Fig. 7. The analog signal is stochastically con-

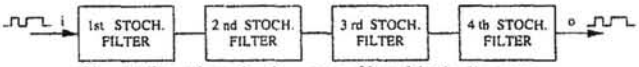


Fig. 7. Fourth order low pass filter block diagram.

verted through the analog to stochastic converter. Four stochastic first order filters are then concatenated. All the digital processing has been implemented in a Xilinx programmable device (FPGA, 4010XL). Analogically we have only a signal adaptation and the RC integrating circuit plus the comparator for the analog to stochastic conversion. In the FPGA is include the rest of the converter and the fourth order low pass filter. The design has been implemented with 8 bits for the analog to stochastic conversion and 14 bits for the low pass filters. Frequency clock is 36 MHz. Mapping, placement and routing has been done with XACT M1.3 Foundation Series. In figure 8a we have the experimental frequency response for each stage of the filter, which has a cutoff frequency of 350 Hz according to equation 3. Figure 9 is the experimental frequency response of the first order high pass filter.

Figure 10 shows the waveforms directly captured from the oscilloscope display. They correspond to a 1^{st} and 4^{th} order low pass filter for a 50 Hz and 350 Hz sinusoidal input waveform.

VI. Conclusions

The use of stochastic logic for implementing systems dynamic provides a set of very simple circuits that can be

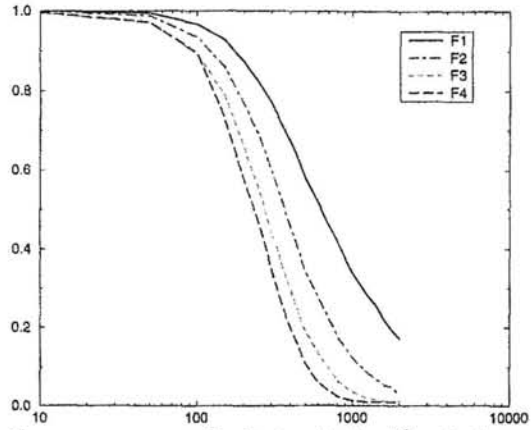


Fig. 8. Frequency response of each stage in the 4^{th} order low-pass filter

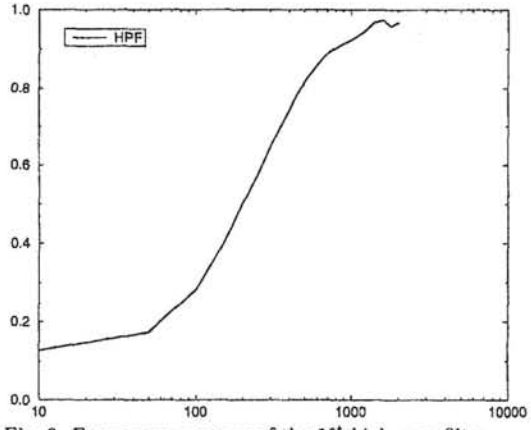


Fig. 9. Frequency response of the 1^{st} high-pass filter

digitally implemented. As a result, the implementation of a continuous time system using digital circuits is achieved. The analog to stochastic conversion solves the problem of the stochastic pulse stream generation. This approach to filter designs allows a low area cost implementation in programmable devices and can be applied to develop embedded systems [16] that process digitally an analog information.

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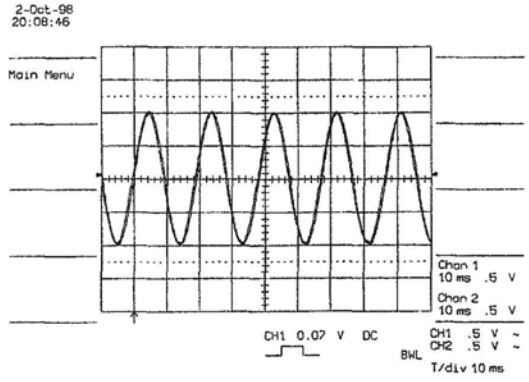
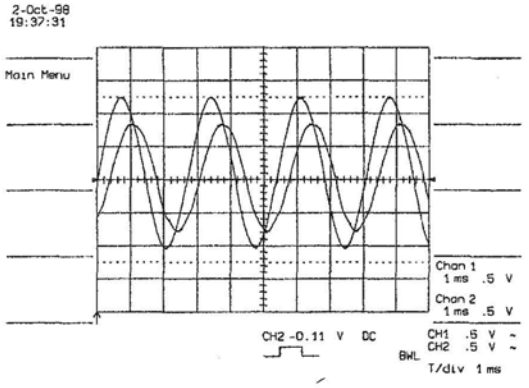
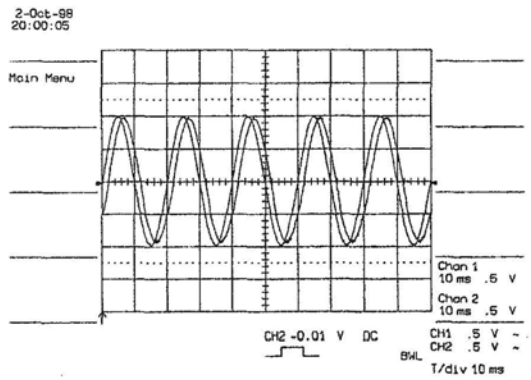


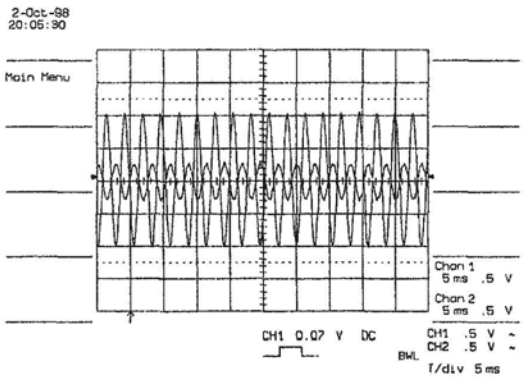
(a) 1^{st} order low-pass filter response to a 50 Hz sinusoidal waveform



(b) 1^{st} order low-pass filter response to a 350 Hz sinusoidal waveform



(c) 4^{th} order low-pass filter response to a 50 Hz sinusoidal waveform



(d) 4^{th} order low-pass filter response to a 350 Hz sinusoidal waveform

Fig. 10. Experimental response of stochastic filters.

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