

ASIC-BASED TACHOMETER WITHOUT MECHANICAL TRANSDUCER FOR INDUCTION MACHINES

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Abstract: A classical method for angular position and speed estimation in adjustable speed drives uses an incremental shaft encoder and an electronic circuit. This paper presents SLESS, a tachometer without mechanical transducer implemented on an ASIC using sensorless speed estimation techniques. The ASIC is intended to serve as part of an integrated solution developed for fuzzy speed regulation and vector control of induction motors.

I. INTRODUCTION

Electrical drives play an important role as electromechanical energy converters in transportation and most production processes. In monitoring and control systems of rotary machines it is essential that rotor position and velocity measurements are available. Also, the knowledge of these variables is indispensable to parameter estimation, electric or thermal modelling and in vector control techniques. Different methods for velocity measurement can be found in the literature. DC tachometers have been used for a long time due to their excellent dynamic performances. However, the following four reasons have encouraged the use of digital tachometers:

- Better accuracy.
- A/D conversion is not required when digital controllers are applied.
- No maintenance required (digital tachometers are brushless machines).
- Noise immunity (no analogue filtering is

required).

Digital tachometers determine speed measurement by calculating the frequency of a pulse train coming from the shaft encoder. Speed measurement methods are thoroughly reviewed in references [1]-[3]. Nevertheless, the incremental shaft encoder presents some problems, especially in hostile environments. In addition, the encoder is an important cost factor since special motor-shaft extensions and encoder mounting surfaces are obligatory.

Hence, a field-oriented speed control scheme not requiring any mechanical shaft transducer constitutes a particularly desirable control solution.

In the last years several methods for sensorless speed estimation have been proposed ([4] and [9]). Between them, those based in model reference adaptative system (MRAS) techniques have shown good performances in the low speed range and robustness against machine parameters variations.

In the elevator industry, ac motors are used in a particular way. The motor is operated from zero speed to nominal, positive or negative, speed and then put back to zero, while positive or negative torque loads are applied. So the ac-machine is operated either as a motor or as a generator. So the sensorless algorithm used in the elevator industry should estimate speed not only in motor zone but also in generator one and in full speed range.

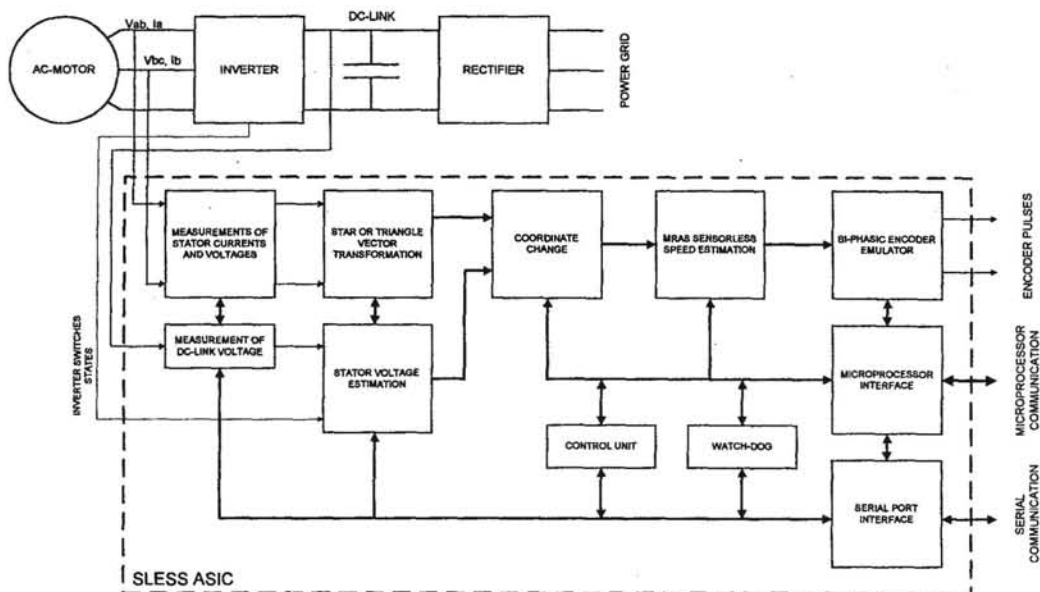


Figure 1. General Schematic of the ASIC (including analog inputs).

This paper presents SLESS, an integrated approach to a digital tachometer without mechanical transducer. SLESS integrates, on a chip, the sensorless speed algorithm based on MRAS techniques. It is based on stator current and voltage measurements and has been designed to work together with ASITRON ([7] and [8]), an ASIC for vectorial control of ac-motors using fuzzy logic. ASITRON and SLESS are the core of a compact, non expensive, industrial control system for elevators. However, SLESS has been designed as a tachometer without mechanical transducer requirements so it generates a encoder emulator biphasic-pulses that allows a direct connection to any induction machine speed controller.

II. SLESS INTEGRATED CIRCUIT

Figure 1 depicts a block diagram of SLESS. The basic tasks implemented are:

1. Stator Current/Voltage measures of two motor phases and dc-link voltage measurement.
2. Stator voltages estimation using dc-link voltage and inverter switches states.
3. Programmable, star or triangle, stator voltages and currents conversion.
4. Coordinate transform in stationary axes.
5. MRAS sensorless speed estimation and biphasic encoder emulator.

6. Watch-dog timer circuitry.
7. Serial port interface (synchronous SPI channel).
8. Parallel microprocessor interface.

To estimate motor speed is necessary to know the stator voltages and current phases values. Four 10-bit A/D converters have been integrated on the chip to measure stator variables.

The stator voltages can be obtained in two ways, measured directly or estimated using the dc-link voltage (which can be measured or externally programmed) and inverter switching states.

The ac-machine can be connected in two ways (star or triangle) so to obtain stator phases voltages and currents values is necessary to transform measured values. Then, the stator phases voltages and currents are transformed into d-q stationary axes to apply on MRAS sensorless speed estimation technique. Speed estimation is based on counterelectromotive force (EMF) vector, as described in [6] where hiperstability of the estimation method is proved (Figure 2). This method compare the output generated by a reference model, speed independent, with the one obtained from an adjustable model which is speed dependent. The reference model and the adjustable model are described by equations (1) and (2) respectively:

$$e_m = v_s - \left(R_s i_s + L_\sigma \frac{di_s}{dt} \right) \quad (1)$$

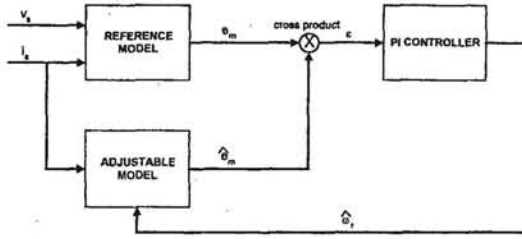


Figure 2. MRAS structure based on EMF vector for speed estimation.

$$\hat{e}_m = L'_m \left(\hat{\omega}_r \otimes \hat{i}_m + \frac{1}{\tau_r} (i_s - \hat{i}_m) \right) \quad (2)$$

Being \hat{i}_m :

$$\hat{e}_m = L'_m \frac{d\hat{i}_m}{dt} \quad (3)$$

The adaptation mechanism is derived from e_m and \hat{e}_m cross product as follows:

$$\hat{\omega}_r = \left(K_p + \frac{K_I}{s} \right) (\hat{e}_m \otimes e_m) \quad (4)$$

The algorithm is implemented using a datapath structure with a 10x14 bits multiplier and a 22x22 bits adder. All the operations are made in integer mode and machine parameters needed for MRAS speed estimation are programmable.

In the SLESS ASIC the estimated speed is used as input to the biphasic encoder emulator block and can be read using a parallel microprocessor interface or a SPI channel. The biphasic encoder emulator block generates two biphasic encoder pulses, simulating the response obtained from a digital tachometer of m pulses per revolution, being m user definable. This feature allows a direct connection between SLESS and any ac-motor speed controller ready to receive encoder pulses from an conventional encoder. The scheme of the incremental encoder emulator block is depicted in Figure 3 and an example of the generated incremental pulses is depicted in Figure 4.

Digital tachometers determine speed measurement by calculating the frequency of a pulse train coming from the shaft encoder. In one method commonly applied the speed is achieved from the elapsed time between successive encoder pulses [17]. In this method the speed is:

$$\omega = \frac{f_{clk}}{m \cdot C_b} \quad (5)$$

Being f_{clk} the clock frequency in Hz of the ASIC, C_b the number of clock pulses counted in one period of encoder pulse and m the number of pulses per revolution of the emulated encoder. The circuit of Figure 3 performs the inverse of (5) counting the number of clock pulses in $1/4$ of the whole period of the encoder pulses (C_{b4} value) as:

$$C_{b4} = \frac{f_{clk}}{4 \cdot m \cdot \omega} = \frac{100 f_{clk} \cdot 16}{64m \cdot (100\omega)} = \frac{NPPR \cdot 16}{\omega_1} \quad (6)$$

Being ω_1 the estimated speed in Hz/100 determined in the sensorless algorithm and $NPPR$ the value programmed for the number of pulses per revolution as $100 f_{clk} / 64m$. Then a state machine generates the encoder pulses $ENC0$ and $ENC1$ using a down counter with the value of C_{b4} . A successive approximation divider performs the division implicit in (6) previous multiplication of $NPPR$ by 16.

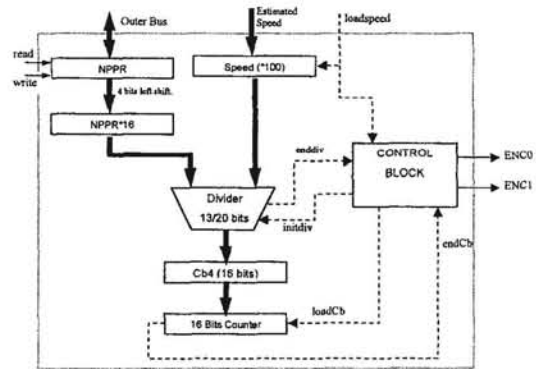


Figure 3. Incremental encoder emulator block diagram.

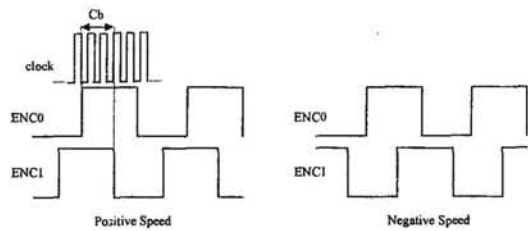


Figure 4. Incremental train pulses and speed signs.

Finally, the ASIC has two ways to communicate with an external microprocessor. SLESS includes a parallel 8 bits bus conventional interface and a synchronous four wire SPI channel for serial communications. This SPI channel would even allow the ASIC to be programmed by an external EPROM

(Figure 5), not requiring an additional microprocessor.

Figure 6 shows the different ways in which SLESS can be programmed.

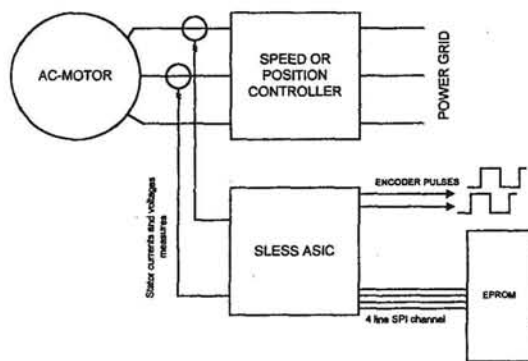


Figure 5. SLESS as a digital tachometer.

III. SIMULATION AND EXPERIMENTAL RESULTS

In order to prove the sensorless algorithm implemented in SLESS many simulations, with several motors in the range between 2HP and 100HP have been made. The sensorless algorithm previously described has been implemented using 'C', codifying variables in integer. The code design matches exactly all the operations performed in the ASIC, including overflows and saturations. To prove this, the simulation results (stator voltages and currents) were used as inputs to the hard level description of the ASIC (in VHDL) and then, the results were

compared. The speed loop has been closed with a vector control algorithm that uses the estimated speed. Figure 7 depicts the results obtained with a 10HP ac-motor. Load torque is maintained constant (about 5Nm) and reference speed tries to emulate a work cycle of an elevator. The control during low speed range is good and the whole system is stable in generator operation zone. Induction machine electrical torque waveforms (triangular shape) show good adaptation of the vector control algorithm.

A prototype version of SLESS is being now fabricated and it will be ready for testing in July 1999. In order to test the code implemented in the ASIC, it has been transferred to a DSP-based ac-motor test-rig. The preliminary results show excellent agreement with expected behaviour.

IV. CONCLUSIONS

In this paper an ASIC that implements a digital tachometer without a mechanical transducer has been presented. The ASIC, named SLESS, implements speed estimation based on the counterelectromotive force MRAS method. A block that emulates an incremental encoder is also included. It generates the biphasic pulse train allowing SLESS to function as a traditional mechanical tachometer. SLESS is being fabricated using a 0.8 μm CMOS digital technology. The final layout is shown in Figure 8. SLESS will be an essential part of a non-expensive high-performance ac-drive for elevators.

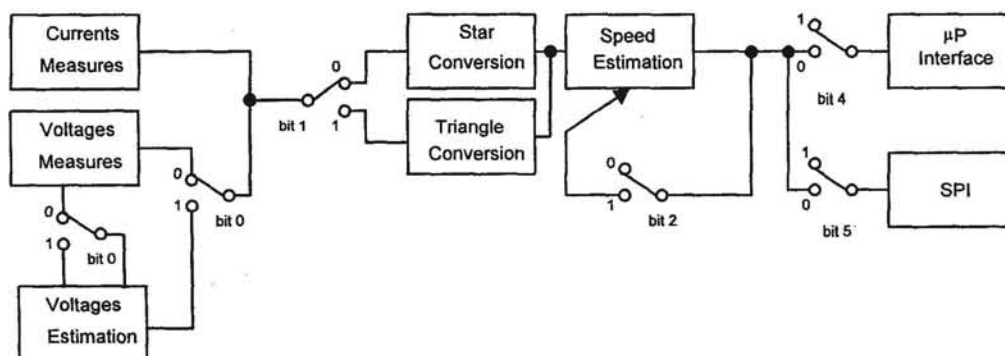


Figure 6. Programmability of SLESS.

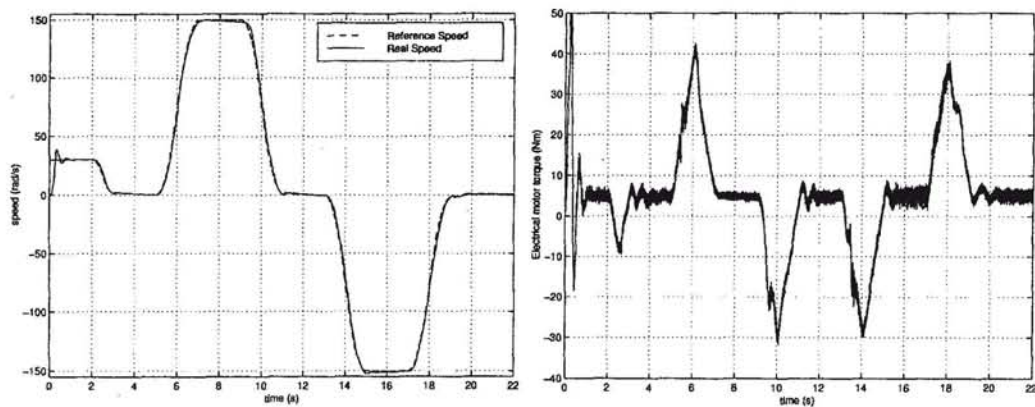


Figure 7. Speed control showing speed and motor torque.

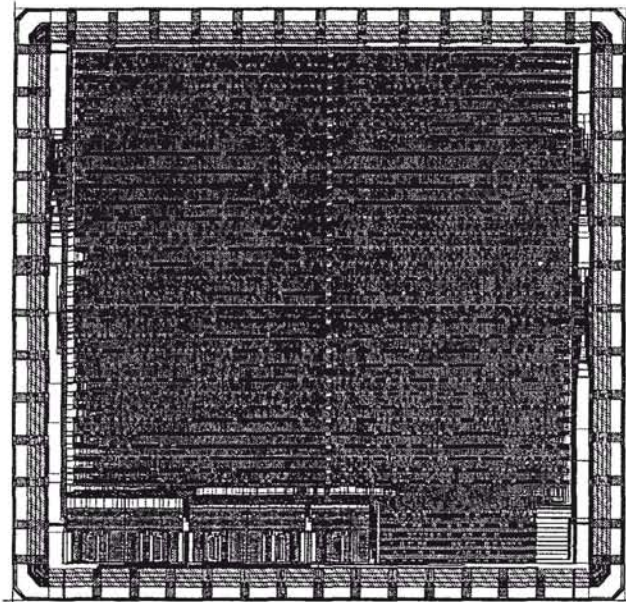


Figure 8. Final layout of SLESS ASIC.

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