Analog Controllers using Digital Stochastic Logic

J.M. Quero, Member IEEE, S.L. Toral, J.G. Ortega and L.G. Franquelo, Senior Member, IEEE
Dpto. de Ingeniería Electrónica, Escuela Superior de Ingenieros,
Avda. Camino de los Descubrimientos s/n, Sevilla–41092 (SPAIN)
e–mail: quero@esi.us.es

Abstract— **Stochastic logic is based on digital processing of a random pulse stream, where the information is codified as the probability of a high level in a finite sequence. The probability of the pulse stream codifies a continuous time variable. Subsequently, this pulse stream can be digitally processed to perform analog operations. In this paper we propose a stochastic approach to the digital implementation of complex controllers. This is approach allows for the realization of the controllers and A/D and D/A converters within a digital programmable device, leading to simple circuit implementations. A practical realization of a classical PID and nonlinear dissipative controllers for the series swithching power resonant converter is presented.**

I. Introduction

Modern control theories is improving the dynamical behavior of our industrial systems. However, in many cases they lack of a simple physical realization. Thus, in practice, the benefits of new controllers are not applied as classical controllers are cheaper to implement. Only in a very limited number of practical applications, the use of a complex electronic control circuit is justified.

Stochastic systems make pseudo analog operations using stochastically coded pulse sequences [1], [2]. Information is represented by the statistical mean value of a pulse sequence. In binary logic, it is codified as the probability of taking a "high" level. The easiest method of generating such sequence is through a random number generator. The value stored in a register is compared with a random number generator. If the random number generator is less or equal than the register value, the output of the comparator is set to a high level. Otherwise, a low level is set. In Fig. 1, the digital to stochastic conversion scheme is shown. Equation (1) give us the probability of an output high level.

$$P(Output = "1") = \frac{Digital\ Value}{2^n} \qquad (1)$$

A probability can not be exactly measured but only estimated as the relative frequency of "high" levels in a long enough sequence. As a consequence, the stochastic computing technique introduces errors in the form of variance when we attempt to estimate the number from the sequence.

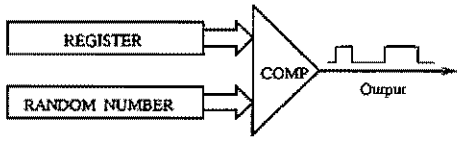

Fig. 1. Digital to stochastic conversion.

This kind of representation leads to very simple computational circuits, as it will be shown in the next section. All this circuits features that they are digitally implemented. The basis of the stochastic signal processing theory that it is included in this work has been formulated some decades ago [1], although some improvements are included in our work. The reason why they are now becoming a practical solution to industry implementation of analog circuits is the appearance of high density digital programmable devices, that allows the realization of large digital circuits and their interfaces within the same integrated circuit [3]. In this paper a set of basic stochastic circuits are introduced together with a design procedure of this kind of circuits. Finally, the stochastic realization of a nonlinear dissipative controllers for the series resonant converter is included as an example to illustrate this novel approach.

II. Stochastic Logic

A. Arithmetic Operations

The two most common arithmetic operations on stochastic signals are multiplication and summation, showed in Fig. 2. Assuming that two stochastic signals are stochastically uncorrelated, the product of both of them can be computed by a single AND gate. Summation is a more difficult operation to perform. The simplest way is to use wired OR summation [4], but it is a non linear scheme: as the probability

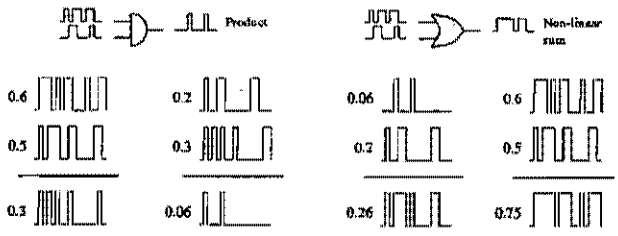

Fig. 2. Stochastic multiplication and summation.

of "high" levels increase, pulse overlap also increases, and the summation saturates gradually (figure 2b). Nevertheless, for low pulse densities, this approach is enough accurate. Another way to realize an exact summation is aggregating pulses in a counter. Other techniques to perform summation are described in [5], [6], [7].

Digitally, integration is performed by a counter. It has been proved [8] that a n bit counter working at a clock frequency f_s is equivalent to a pure analog integrator with time constant $2^n/f_s$

B. *Digital to Stochastic and Stochastic to digital Conversions*

To recover the value of the probability, the stochastic pulse stream must be integrated to obtain its mean value. Digitally, integration is performed by a counter. A low pass RC filter is well suited to recover the analog value of this probability, that is, to perform the stochastic to analog conversion [9].

A digital to stochastic converter is well known in the literature and has been extensively used from the beginning of stochastic computation [10],[11],[12]. An analog to digital based on stochastic logic has been also developed in [13]. Also an analog random signal generator [14] may be used, but we propose a mixed analog/digital approach to this conversion, using a generalization of the first order system described before. In Fig. 3 there is a basic scheme for this conversion. The analog input signal $v_i(t)$

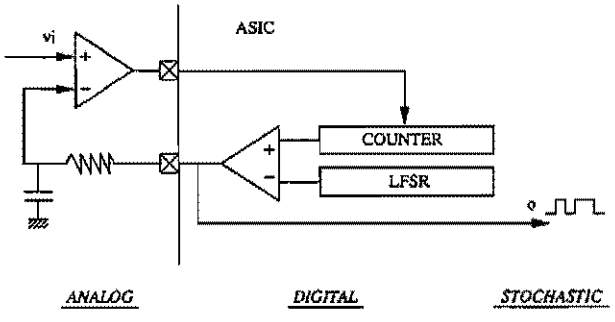

Fig. 3. Analog to stochastic conversion.

is compared with the stochastic pulse sequence integrated with simple RC integrating circuit. The output of the comparator is a PWM representation of the input signal, that is time integrated with the up/down counter. This structure is similar to the stochastic first order system, but with an external analog comparator that leads to a PWM representation of information, instead of an error signal proportional to the input difference.

III. Stochastic Circuit Design Procedure

Once the basic stochastic building blocks are characterized, more complex circuits can be developed, following the next steps:

1. *Determination of Scaling Factors.* The main design constraint that stochastic variables must agree is that the should take values within $[0, 1]$. Therefore, appropriate scaling factors should be determined for any variable. Notice that, on the other hand, all variables are inherently bounded, even under exceptional functional conditions, thus ensuring a secure response of the stochastic circuit.
2. *Determination of integration circuits clock frequency.* The location of constants and additions/substractions previous to the integrators can be done algebraically manipulating the mathematical equations. Placing constants previous to the integrators is appropriate because constant larger than unity can be implemented using integrator's constant. Besides, despite of existing substration stochastic logic circuits [15], it is preferable to aggregate positive values in the incremental input signals of counters, while negative signals are aggregated in the decremental one.
3. *Selection of LFSRs.* The determination of a set of LFSRs (linear feedback shift register) as the random number generator to perform digital to stochastic conversion should be done to generate stochastic pulse streams as uncorrelated as possible. Otherwise, the stochastic signal processing would loose accuracy. This can be done using a set of LFSRs with the same feedback, but using seeds corresponding to pseudo random numbers generated with a sufficiently large number of clock cycles.

IV. Series Resonant Converter Model

Considering the Series Resonant Converter (SRC) circuit shown in Fig. 4. This circuit is fed by a bipolar square signal whose amplitude is in most of the cases constant, remaining the commuting frequency as the only accessible control input. The system is a cascade connection of two subsystems. The first one, the tank circuit, is fed

with a modulated signal and whose states are not available for measurement. The second subsystem acts as a detector of the inductor current amplitude, which is the only useful information coming from the first subsystem. Using harmonics approximation, the discontinuous system can be simplified to a static nonlinearity in cascade with an output passive filter.

A state space model of the system can be obtained from Kirchoff's voltage and current laws [18]

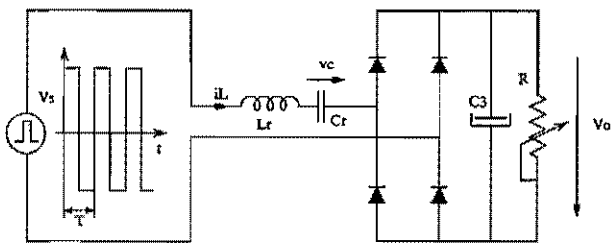

Fig. 4. Circuit schematic of a series resonant converter

$$L\frac{di_L}{dt} = -v_C - v_0 \text{sign}(i_L) + v_i(t)$$
$$C\frac{dv_C}{dt} = i_L \quad (2)$$
$$C_0\frac{dv_0}{dt} = \text{abs}(i_L) - \frac{v_0}{R} - I_0 \quad (3)$$

where i_L is the input inductor current, v_C is the series capacitor voltage and v_0 is the output voltage supplying the load. L and C are the inductance and capacitance in the resonant tank, respectively. C_0 is the capacitance of the output filter and R is the output load. It has been assumed that $v_i(t)$ signal has been implemented as $v_i(t) = V_s\, sign(sin(u\,t))$, with V_s a constant value that represents the source amplitude and u the switching frequency generated by the control system. In our study, the following converter parameters has been chosen: $L = 0.9059mH$, $C = 130\mu F$ and $C_0 = 2400\mu F$.

V. Stochastic PID Controller for Resonant Converter

A classical PID controller for the previous SRC has been designed, and its parameters have been adjusted by simulation. In Fig. 5 the digital realization of the stochastic circuit is shown. It is composed by to blocks: (a) in Fig. 5 represents the integral of the difference between $Vref$ and Vo. Both input signals are normalized using a maximum value $V_m = 80V$. The digital value $Vref$ is transformed in a stochastic pulse stream, indicated by a number in circle. Vo is feedback using a sigma-delta stochastic A/D converter. The integrator's constant is implemented simply dividing the clock frequency of the counter. (b) in Fig. 5 generates the switching signal from the semiperiod $T/2$ calculated in the previous block. The main digital clock frequency is 18MHz.

A. Simulation results

Fig. 6 shows the start-up and a 5Ω to 10Ω load change response, including the output voltage of the resonant converter when using the theoretical and the PID stochastic controllers. Also other test were performed, an theoretical and stochastic circuits behaviour were very similar in all cases.

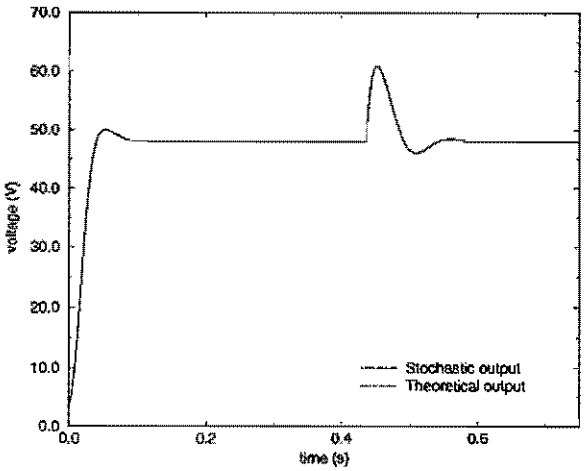

Fig. 6. Response of the resonant converter for the theoretical and PID stochastic controllers

VI. Stochastic Passivity-based Controller for Resonant Converter

Passivity-based control techniques have been shown to be rather useful in several unrelated electrical and mechanical engineering control problems, such as synchronous and asynchronous induction motor, robotic manipulator systems and dc-to-dc power converters (see Ortega *et al* [16] for a complete revision of all this topics).

A new control technique for a SRC was proposed in [17]. The control was obtained by incorporating the passivity based controller design methodology embedded with an adaptive law to estimate the unknown resistive load showing an excellent performance. This control technique is summarized in the following set of differential equations:

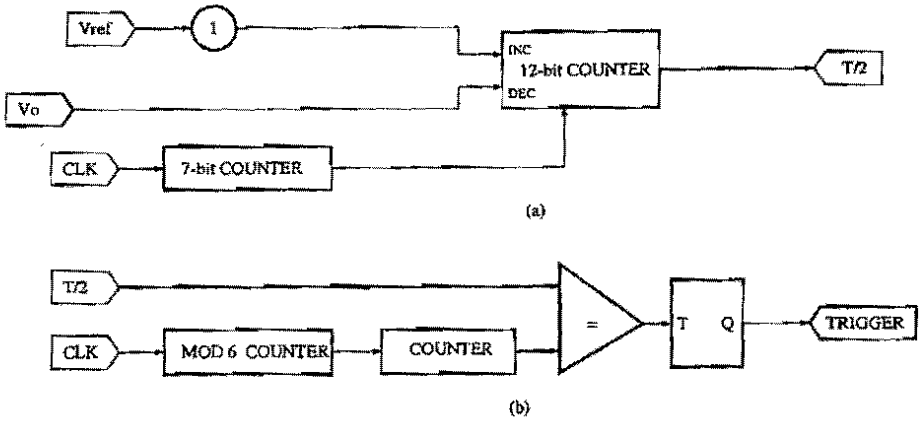

Fig. 5. Digital realization of the PID controller using stochastic logic

Variable	scaling factor	value
$V_s, V_o, V_{ref}, V_{od}$	V_m	80v
$gest$	G_m	0.25 Ω^{-1}
I_{Lest}	I_m	10A
Div	D_m	10e8 $(rad/s)^2$
u	U_m	20000 rad/s

TABLE I

SCALING FACTORS FOR CONTROLLER'S VARIABLES

LFSR #	value
0	1
1	458
2	756
3	703
4	843
5	575

TABLE II

INITIAL VALUES OF LFSRS

$$I_{Lest} = \frac{\pi V_{ref}\, gest}{4} \quad (4)$$

$$C_0 \dot{V}_{od} = \frac{4}{\pi} I_{Lest} - gest V_{od} \quad (5)$$

$$\dot{gest} = -\gamma V_{od}(V_o - V_{od}) \quad (6)$$

$$Div = \frac{V_s^2 - V_{od}^2}{\pi I_{Lest}} \quad (7)$$

$$u = 2\sqrt{Div} \quad (8)$$

$$\dot{gest} = -\gamma V_{od}(V_o - V_{od}) \quad (9)$$

where $gest$ is the estimate for $1/R$, V_{ref} is the output voltage reference, R_1 is a damping constant in the error $V_0 - V_{od}$ and γ is a control constant.

A. Stochastic Controller Design

The set of equations 4–9 should be implemented by applying the procedure described in section III.

According to definitions and simulations, the maximum values of variables given in Table I have been chosen as scaling factors. The application of this scaling factors lead to the following set of normalized equations:

$$\overline{I}_{Lest} = \frac{\pi V_m G_m}{4 I_m} \overline{V}_{0ref}\, \overline{gest}$$

$$\overline{V}_{od} = \frac{1}{C_0 V_m} \int \left(\frac{4 I_m}{\pi V_m} \overline{I}_{Lest} - \overline{gest}\,\overline{V}_{od} G_m\right) dt$$

$$\overline{\dot{gest}} = -\frac{\gamma V_m^2}{G_m} \int \overline{V}_{od}(\overline{V}_o - \overline{V}_{od})dt \quad (10)$$

$$\overline{Div} = \frac{V_m^2}{\pi^2 L^2 D_m I_m^2} \frac{\overline{V}_s^2 - \overline{V}_{od}^2}{\overline{I}_{Lest}}$$

$$\overline{u} = \frac{\sqrt{2 D_m}}{u_m} \sqrt{\overline{Div}}$$

where $\overline{(\cdot)}$ represents per unit variable.

As a digital clock frequency of 18MHz, and a 10-bit resolution has arbitrary been chosen, it can be determined the integrator's clock frequency ratios. In our case, instead of dividing digital clock frequency, it has been increased the number of bits in the counters. More precisely, the integrator counters $\overline{gest}$ and $\overline{V}_{od}$ have 18 and 19 bits respectively, but only the 10 MSBs are considered in the digital to stochastic conversion. As a result, the digital circuit depicted in Fig. 7 is achieved. Finally, it has been defined a set of LFSRs, all with the feedback polynomial given by equation 11, where $\wedge$ represents an XOR logic function, and seeds of Table II.

$$Q_{10} = Q_1 \wedge Q_2 \wedge Q_3 \wedge Q_4 \wedge Q_6 \wedge Q_7 \quad (11)$$

A number X in circle represents a digital to stochastic conversion using LFSR number X and a comparator, as it is depicted in Fig. 1. It should be remarked that blocks (d) and (e)

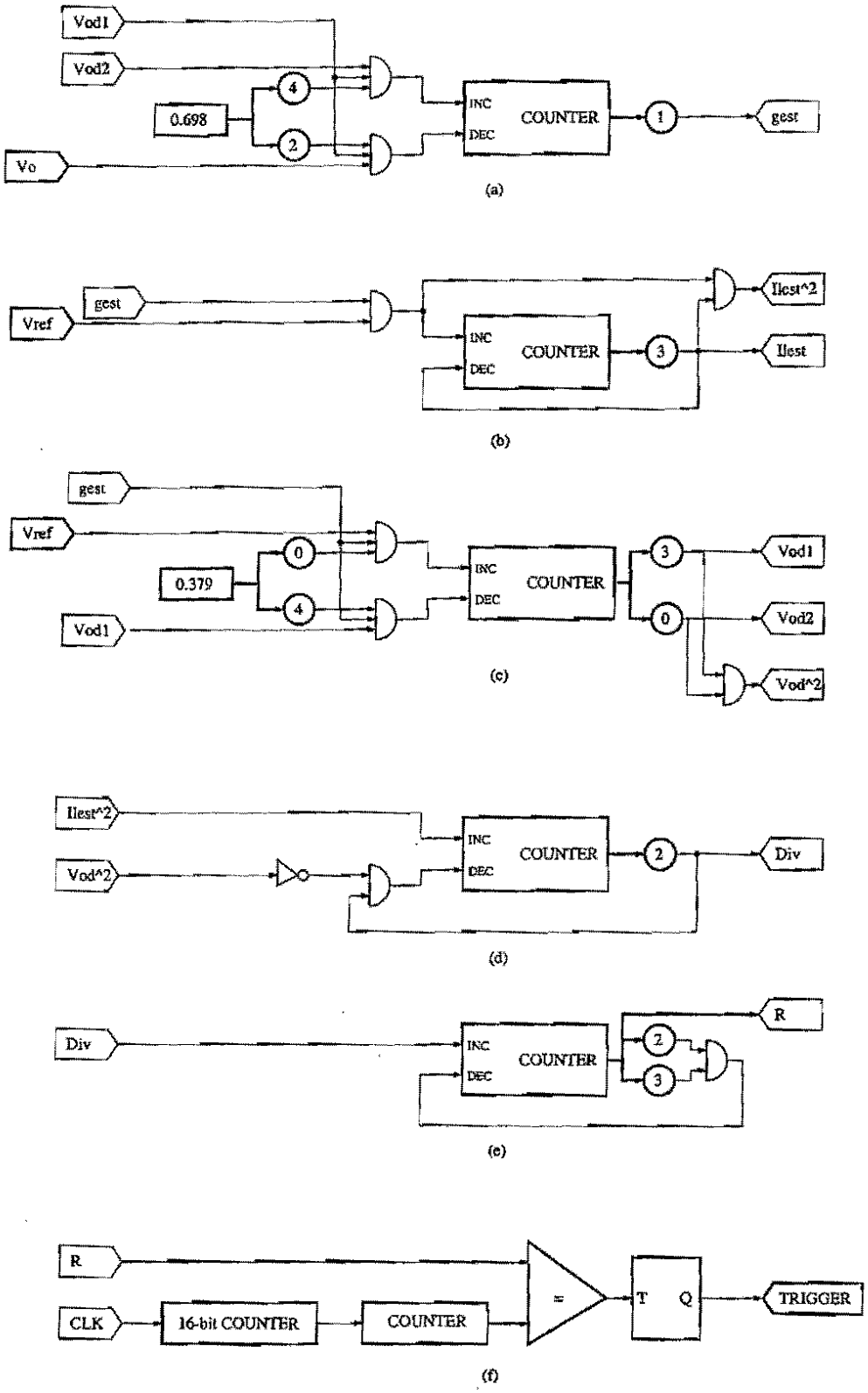

Fig. 7. Digital realization of the passivation controller using stochastic logic

in Fig. 7 correspond to the division and square root functions respectively. It can be easily verified that it is accomplished by using the negative feedback of their inverse functions (multiplication and square). Circuit (f) generates the switching signal of $v_i(t)$ by converting the digitally codified value of the frequency to one half of the period, thus generating the frequency-variable squared switching signal named TRIGGER. It is remarkable than only some counters, digital comparators and auxiliary logic is needed to implement the controller.

B. Simulation results

In order to verify the previous design, both controllers, the stochastic one and its theoretical formulation, have been compared using a passivation model of the series resonant converter. Again, Fig. 8 shows the start-up response, including the output voltage of the resonant converter when using the theoretical and the stochastic controllers and a load change of the same values than in the PID controller simulation. The converter response is faster and presents a lower over-voltage than the response obtained with the PID controller.

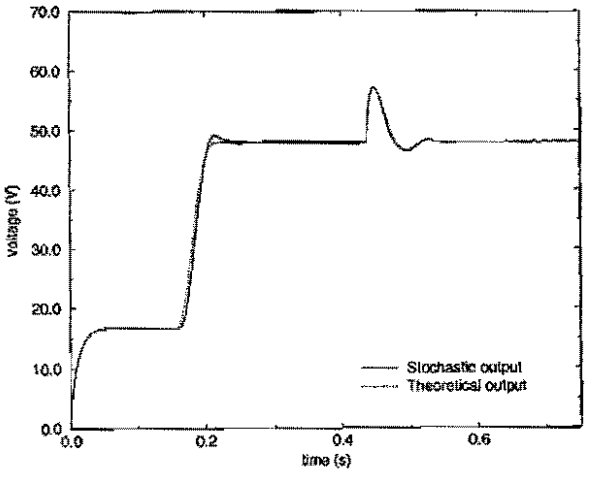

Fig. 8. Start-up response of the resonant converter for the theoretical and stochastic passivity-based controllers

VII. Conclusions

The use of stochastic logic to implement analog controllers provides a set of very simple circuits that can be digitally implemented. As a result, the implementation of a continuous time system using digital circuits and their interfaces is achieved. As an examples, the stochastic implementation of a classical PID and a passivity-based controllers are included. This approach to complex controller designs allows a low area cost implementation in programmable devices and can be applied to develop embedded systems [19] that process digitally an analog information. This approach also simplifies the programmability of the controllers in a networked environment using dynamic device programming.

References

[1] B.R. Gaines, *Stochastic computing systems*, Advances Inform. Syst. Sci., vol. 2, pp. 37-172, 1969.

[2] C.L. Janer, J.M. Quero, J.G. Ortega and L.G. Franquelo, *Fully Parallel Stochastic Computation Architecture*, IEEE Trans. Signal Processing, vol. 44, no. 8, Au. 1996, pp. 2110- 2117, Aug. 1996.

[3] J. Logue, *Virtex Digital to Analog Converter*. Advanced Application Note. Xilinx. Feb. 1999.

[4] A.F. Murray, D. del Corso and L. Tarassenko, *"Pulse-Stream VLSI Neural Networks Mixing Analog and Digital Techniques"*, IEEE Transaction on Neural Networks, vol. 2, no. 2, pp. 193-204, 1991.

[5] D.E. Van den Bout and T.K. Miller, *"A Digital Architecture Employing Stochasticism for the Simulation of Hopfield"*, IEEE Transactions on Circuits and Systems, vol. 36, no. 5, pp. 732-738, May 1989.

[6] C.L. Janer, J.M. Quero and L.G. Franquelo, *"Fully Parallel Summation in a New Stochastic Neural Network Architecture"*, IEEE Intl. Conf. on Neural Net., pp. 1498-1503, San Francisco 1993.

[7] M. van Daalen, J. Shawe-Taylor and J. Zhao, *"Real Time Output Derivatives for on Chip Learning Using Digital Stochastic Bit Stream Neurons"*, IEEE Electronic Letters, vol. 30, pp. 1775-1777, 1994.

[8] J.M. Quero and L.G. Franquelo, *"Controladores Digitales Estocásticos"* DCIS'95, pp. 272-276, Zaragoza, Nov. 1995.

[9] J.G. Ortega, C.L. Janer, J.M. Quero and L.G. Franquelo, J. Pinilla and J. Serrano, *"Analog to Digital and Digital to Analog Conversion Based on Stochastic Logic"*, IEEE Intl. Conf. on Ind. Electr. IECON'95, Orlando, Nov. 1995.

[10] B.R. Gaines, *"Stochastic Computer Thrives on noise"* Electronics, pp. 72-79, July 1967.

[11] S. Ribeiro, *"Random-pulse machines"*, IEEE Transactions on Electronic Computers, vol. EC-16, no. 3, pp. 261-276, June 1967.

[12] A.J. Miller, A.W. Brown and P. Mars, *"Moving-average Output Interface for Digital Stochastic Computers"* Electron. Lett., vol. 10, no. 20, pp. 419-420, Oct. 1974.

[13] J.M. Quero, C.L. Janer, J.G. Ortega, L.G. Franquelo, *"D/A Converter ASIC Uses Stochastic Logic"*, EDN, pp. 86-88, Oct. 1996.

[14] E. Petriu, K. Watanabe and T. Yeap, *"Applications of Random-Pulse Machine Concept to Neural Network Design*, IEEE Trans. Instrum Meas., vol. 45, no. 2, pp. 665-669, 1996.

[15] S.L. Toral, J.M. Quero and L.G. Franquelo, *"Reactive Power and Energy Meter based on Random Signal Processing"* Design of Circuits and Integrated Systems Conference (DCIS98), Madrid, November 1998.

[16] R. Ortega and A. Loria and P. J. Nicklasson and H. Sira-Ramirez, "Passivity-based control of Euler-Lagrange systems", Springer-Verlag, Berlin, 1998.

[17] G. Escobar, *"On the non-linear Control of Switching Power Electronic Systems"*. PhD Dissertation developed in LSS-Supelec, France, 1999

[18] A.M. Stankovic, D. J. Perreault and K. Sato, "Analysis and Experimentation with Dissipative Nonlinear Controllers for Series Resonant DC/DC Converters", *Proceedings of the 28th Annual IEEE Power Electronics Specialist Conference* (PESC97), Vol. 1, pp. 679-685, St. Louis, Missouri. May 1997.

[19] S.L. Toral, J.M. Quero and L.G. Franquelo, *"Power Energy Metering based on Random Signal Processing (ECRPS)"* ISCAS'98. Monterrey, California, May-June 1998.