A Three-Level Common-Mode Voltage Eliminated Inverter With Single DC Supply Using Flying Capacitor Inverter and Cascaded H-Bridge

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***Abstract*—A three-level common-mode voltage eliminated inverter with single dc supply using flying capacitor inverter and cascaded H-bridge has been proposed in this paper. The three phase space vector polygon formed by this configuration and the polygon formed by the common-mode eliminated states have been discussed. The entire system is simulated in Simulink and the results are experimentally verified. This system has an advantage that if one of devices in the H-bridge fails, the system can still be operated as a normal three-level inverter at full power. This inverter has many other advantages like use of single dc supply, making it possible for a back-to-back grid-tied converter application, improved reliability, etc.**

***Index Terms*—Common-mode voltage elimination, hybrid multilevel inverter, multilevel inverter, three-level inverter.**

I. Introduction

MULTILEVEL inverters have improved the performance of medium- and high-voltage drives [1], [2]. The flyin capacitor inverter proposed in [3], the cascaded-H-bridge inverter proposed in [4], and the neutral-point-clamped inverter proposed in [5] are the three basic topologies of a multilevel inverter. The cascaded H-bridge inverter with capacitor-cell and voltage balancing has been proposed in [6] and [7]. In recent times, many hybrid topologies, which are modification to these basic topologies, have been proposed and have their own advantages and disadvantages [8]–[12].

The outputs of these dc–ac converters contain common-mode voltage switched at high frequencies with voltage magnitudes that are comparable to the inverter pole voltages. High frequency switching of the common-mode voltage in the induction motor causes several issues like leakage currents through the stray capacitance between the winding and the body of the motor and create shaft voltages causing bearing currents resulting in bearing failures of the motors [13]–[16].

The effects of common-mode voltage are much more adverse in the case of medium- and high-voltage drives due to high frequency switching of common-mode voltage in the order of few kilovolts. High dV/dt switching in common-mode voltage causes breakdown of bearing lubricant insulation and causes pitting in the bearing surfaces. This leads to quick failure of bearings as discussed in [17].

Many inverter topologies have been proposed to eliminate the effects of common-mode voltage in induction motor drives. The work presented in [18] gives an idea to eliminate the common-mode voltage by connecting two 2-level inverters to the induction motor which is connected in an open-end winding config uration and switching them appropriately so as to remove the common-mode voltage.

A three-level inverter with common-mode voltage elimination for open-end connected induction motor was presented in [19]. Using a fi e level-inverter to eliminate common-mode voltage wherein the motor is connected in an open-end winding configuratio has been presented in [20]. This configuratio requires more number of isolated power supplies and diode bridge rectifiers The work presented in [21] gives an interesting idea of using a single dc power supply for a three-level common mode voltage eliminated inverter. Many topologies have been presented for removing the common-mode voltage in inverter output when fed to an induction motor drive. However, these configuration need motor to be connected in open-end winding configuratio or need multiple isolated power supplies.

In this study, we propose a new three-level common-mode voltage eliminated inverter configuration In the proposed configuration the motor will be connected in Y configuratio as opposed to open-ended configuration Also, the proposed configuratio uses single dc supply. This use of single link dc power supply enables the inverter to be connected in back-to-back configuratio with a front end converter so that the power can be drawn from the grid during motoring operation and put back to grid during regeneration (all four quadrant operation) with specifie power factor (unity power factor in most cases).

II. Topology

Each phase of the proposed topology consists of a floatin capacitor H-bridge with voltage maintained at (0.25 V_{dc}). This H-bridge is cascaded to a three-level flyin capacitor inverter which can generate voltage levels of (0.5 V_{dc}), 0, (-0.5 V_{dc}). The three-phase power circuit for the proposed configuratio is

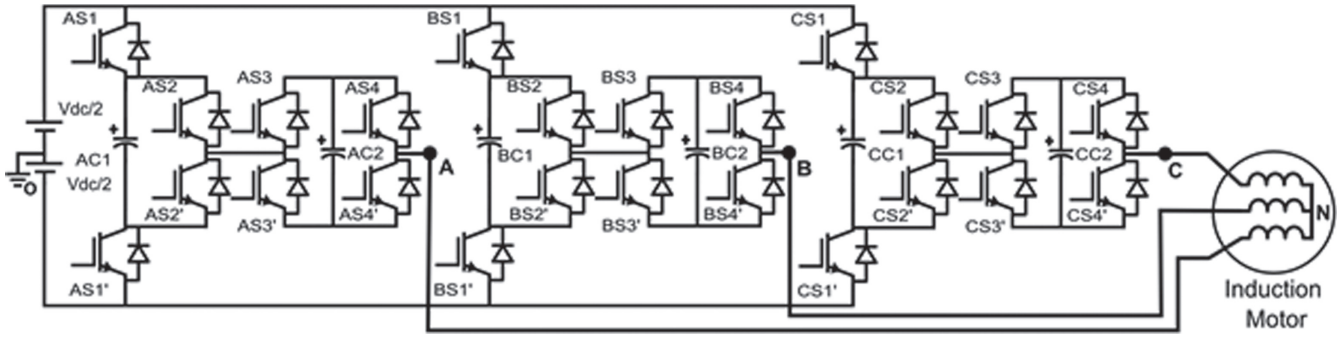
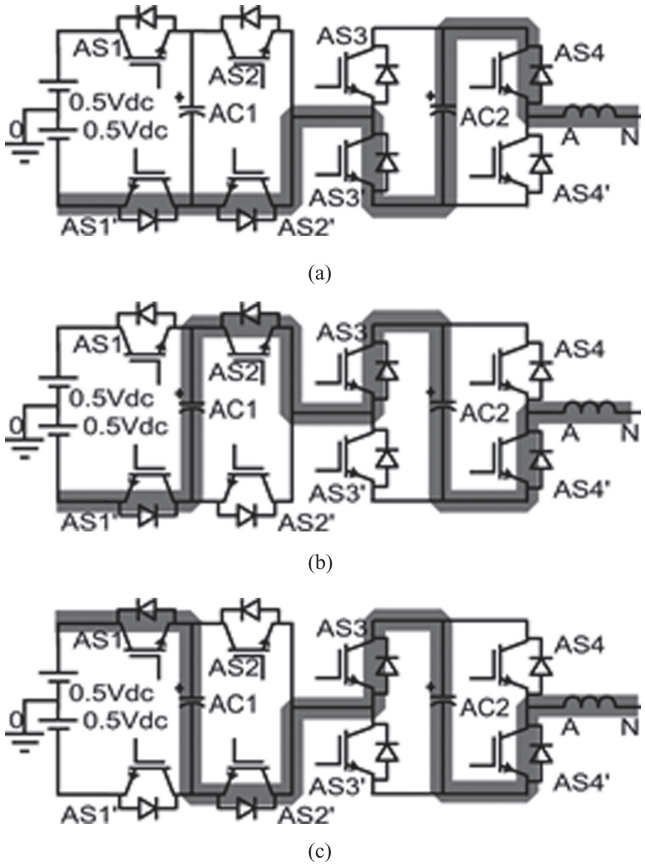


Fig. 1. Power circuit for the proposed three-level common mode voltage eliminated inverter.

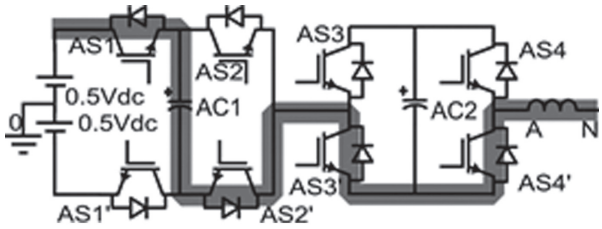


(a)

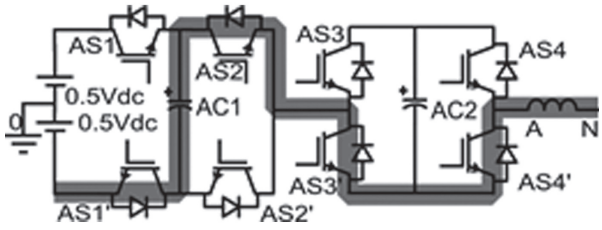
(b)

(c)

Fig. 2. Switching redundancies for pole voltage of $-0.25\ V_{dc}$. (a) Path of current fl w for switching state (0,0,0,1). (b) Path of current fl w for switching state (0,1,1,0). (c) Path of current fl w for switching state (1,0,1,0).



(a)



(b)

Fig. 3. Redundancies voltages of $0.25\ V_{dc}$. (a) Path of current fl w for switching state (1,0,0,0). (b) Path of current fl w for switching state (0,1,0,0).

shown in Fig. 1. The voltage levels of capacitors AC1, BC1, and CC1 are maintained at ($0.5\ V_{dc}$) and that of AC2, BC2, and CC2 are maintained at ($0.25\ V_{dc}$). Each pole of the inverter can generate voltage levels which are arithmetic combinations of the two cascaded structures. In the present power circuit, pole voltage levels of ($-0.5\ V_{dc}$), ($-0.25\ V_{dc}$), 0, ($0.25\ V_{dc}$), and ($0.5\ V_{dc}$) can be generated with respect to dc-bus ground (node O in Fig. 1). The top and bottom devices are switched complementarily. Here, switching state of "1" represents the top device is switched ON and the bottom device is switched OFF and vice versa.

Fig. 2 depicts the redundant combinations for generating a pole voltage of $-0.25\ V_{dc}$ through various switching combinations. When the switching state of (0,0,0,1) is applied as shown in Fig. 2(a) and for positive direction of current, i.e., when the pole is sourcing current, capacitor AC2 gets discharged while applying the pole voltage of $-0.25\ V_{dc}$. To charge capacitor AC2, redundant states of (0,1,1,0) and (1,0,1,0) are applied as shown in Fig. 2(b) and (c). In this process, capacitor AC1 gets discharged and charged when states shown in Fig. 2(b) and (c) are applied, respectively. Based on state of charge of capacitors and the direction of current, one of the switching states is applied for generating pole voltage of -0.25. By switching through all the three redundant states shown in Fig. 2, the voltages of the two capacitors can be maintained at their respective levels. The redundant switching states for pole voltage of 0 V are depicted in Fig. 3. For positive direction of current, switching state (1,0,0,0) [see Fig. 3(a)] is applied to charge capacitor AC1 and state (0,1,0,0) [Fig. 3(b)] is applied to discharge the same, while voltage of AC2 is left unaffected, thereby maintaining the two capacitor voltages at their prescribed values. To generate the pole voltage of $0.25\ V_{dc}$, switching state of (1,1,1,0) is applied which charges capacitor AC2 as shown in Fig. 4(a). To discharge the same, switching states of (0,1,0,1) and (1,0,0,1) are

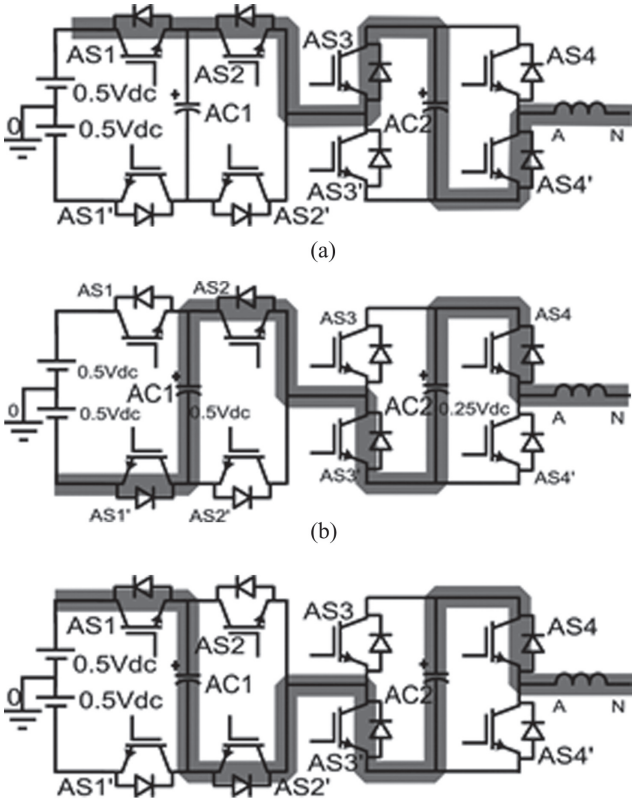


Fig. 4. Redundancies voltages of 0.25 V_{dc}. (a) Path of current fl w for switching state (1,1,1,0). (b) Path of current fl w for switching state (0,1,0,1). (c) Path of current fl w for switching state (1,0,0,1).

applied which discharges and charges capacitor AC1 as shown in Fig. 4(b) and (c), respectively. This helps in maintaining the two capacitor voltages at prescribed values. To generate pole voltage of 0.5 V_{dc}, a switching state of (1,1,1,1) is applied and to generate -0.5 V_{dc}, a switching state of (0,0,0,0) is applied while the capacitor voltages are unaffected.

A detailed list of pole voltage redundancies and their effect on capacitor voltage for the positive direction of current has been presented in Table I. For the negative direction of current, the capacitor effects shown in the table are complemented. For any pole voltage, based on the state of charge of capacitor and the direction of current, a switching state is applied every switching cycle so as to maintain the capacitor voltage ripple within the prescribed values.

III. Common-Mode Voltage Eliminated States

There are total of 125 ($5 \times 5 \times 5$) three-phase pole voltage combinations for the proposed inverter. The space vector structure for the voltage levels that are generated from the proposed circuit is as shown in Fig. 5 where the 125 voltage combinations are mapped to 61 locations of the space vector polygon. In-depth analysis of the algorithm for balancing the capacitor voltage at various voltage levels and other aspects of the configuratio have been presented in [22]. The common-mode voltage of a Y-connected induction motor is given by (1) where

TABLE I
Capacitor States for Different Pole Voltage Redundancies for Positive Current

Pole Voltage	Switching redundancy[+]	Cap AC1 (0.5Vdc)*	Cap AC2 (0.25Vdc)*
-0.5Vdc	(0,0,0,0)	No effect	No effect
-0.25Vdc	(0,0,0,1)	No effect	Discharge
-0.25Vdc	(0,1,1,0)	Discharge	Charge
-0.25Vdc	(1,0,1,0)	Charge	Charge
0	(0,1,0,0)	Discharge	No effect
0	(1,0,0,0)	Charge	No effect
0.25Vdc	(1,1,1,0)	No effect	Charge
0.25Vdc	(1,0,0,1)	Charge	Discharge
0.25Vdc	(0,1,0,1)	Discharge	Discharge
0.5Vdc	(1,1,1,1)	No effect	No effect

[+]1 indicates top device is ON and 0 indicates bottom device is ON.
[*]The capacitor states are complemented for the negative direction of current.

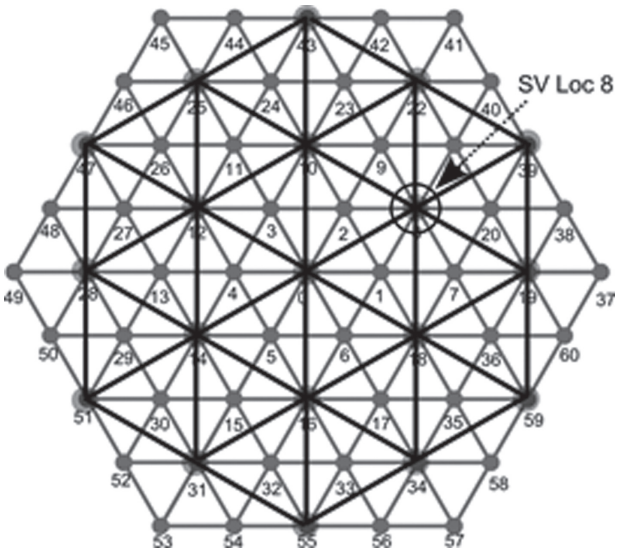


Fig. 5. SV-polygon of the f ve-level inverter and the locations with zero common-mode voltage locations.

V_{AO}, V_{BO}, and V_{CO} are the pole voltages of the inverter. Of all the 125 pole-voltage combinations formed by the proposed inverter configuration there are 19 combinations for which the common-mode voltage is zero

$$V_{CM} = (V_{AO} + V_{BO} + V_{CO})/3. \quad (1)$$

All the 19 space-vector locations and their pole-voltage combinations for zero common mode have been presented in Table II. The locations with zero common-mode voltage have been highlighted on the f ve-level space-vector diagram formed

TABLE II
STATES WITH ZERO COMMON-MODE VOLTAGE

Space Vector Location	Combination of three phase Pole voltages [a]	Pole voltage Combination with zero common mode voltage[a]
0	(-2,-2,-2) (-1,-1,-1) (0,0,0)(1,1,1,)(2,2,2)	(0,0,0)
8	*(0,-1,-2)(1,0,-1)(2,1,0)*	*(1,0,-1)*
10	(-1,0,-2) (0,1,-1) (1,2,0)	(0,1,-1)
12	(-2,0,-1) (-1,1,0) (0,2,1)	(-1,1,0)
14	(-2,-1,0) (-1,0,1) (0,1,2)	(-1,0,1)
16	(-1,-2,0) (0,-1,1) (1,0,2)	(0,-1,1)
18	(0,-2,-1) (1,-1,0) (2,0,1)	(1,-1,0)
19	(1,-2,-2) (2,-1,-1)	(2,-1,-1)
22	(1,1,-2) (2,2,-1)	(1,1,-2)
25	(-1,2,-1) (-2,1,-2)	(-1,2,-1)
28	(-2,1,1) (-1,2,2)	(-2,1,1)
31	(-1,-1,2) (-2,-2,1)	(-1,-1,2)
34	(1,-2,1) (2,-1,2)	(1,-2,1)
39	(2,0,-2)	(2,0,-2)
43	(0,2,-2)	(0,2,-2)
47	(-2,2,0)	(-2,2,0)
51	(-2,0,2)	(-2,0,2)
55	(0,-2,2)	(0,-2,2)
59	(2,-2,0)	(2,-2,0)

[a] 2, 1, 0, −1, −2 represents pole voltages of $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$.

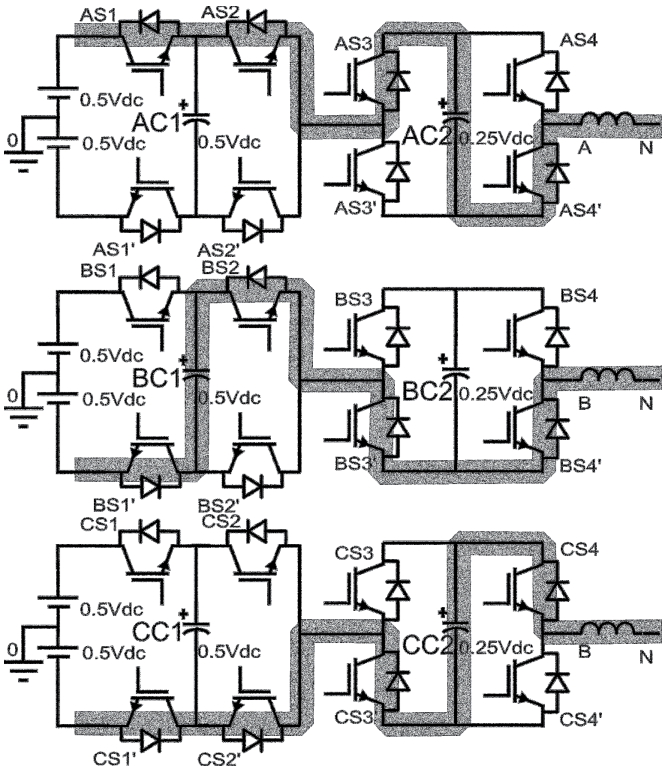


Fig. 6. Three-phase pole voltage combination for SV-location 8.

by the proposed inverter topology in Fig. 5. A three-level space-vector polygon rotated by 30° will be formed with all the zero common-mode voltage combinations for the proposed inverter structure.

Consider a case wherein the controller demands the inverter to generate SV-location 8. The pole voltages are (0.25 V_{dc}), 0 and (−0.25 V_{dc}) for phases A, B, and C, respectively. One switching combination where poles A and B are sourcing current to the motor and pole C is sinking current is presented in

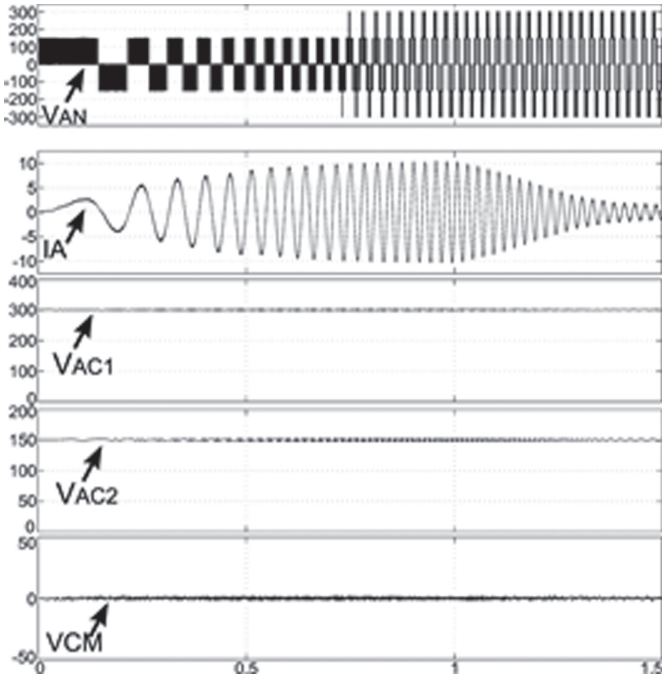


Fig. 7. Simulation result for accelerating the motor throughout the entire modulation range. V_{AO} : pole voltage (100 V/div), I_A : pole current (5 A/div), V_{AC1} : cap1-voltage (100 V/div), V_{AC2}: cap2-voltage (50 V/div), V_{CM} : common-mode voltage (50 V/div), time: 500 ms/div.

Fig. 6. Here, the capacitors AC2, CC2 charge, BC1 discharge, while the other capacitor voltages remain unchanged. To balance the capacitors, other redundant states can be applied for the same set of pole voltages as discussed in the previous section in detail.

IV. SIMULATION

For simulation, the proposed converter is used with a 3-kW, 400-V, 50-Hz Y-connected induction motor. The converter is run with open-loop V/f control algorithm at various modulation indices and frequencies. The switching frequency of the inverter is set at 1 kHz. The capacitors are sized so that the voltage ripple is 2 V at full load current. A level-shifted carrier-based space vector pulse width modulation (PWM) generation technique, which was presented in [23], was used to generate the gating signals for the switches. The performance of the capacitor-balancing algorithm was tested by accelerating the motor from zero to full speed at no load. The pole voltage, the pole current, the two capacitor voltages, and the common-mode voltage waveforms for the simulation are plotted in Fig. 7. To test the ruggedness of the capacitor balancing algorithm, the algorithm was disabled and re-enabled. The simulation results are presented in Fig. 8. It can be observed that the capacitor voltages deviate from their intended values and the common-mode voltage starts rising when the controller is disabled. Also, it can be observed that on re-enabling the controller, the capacitors are balanced back to their intended values bringing the common-mode voltage back to zero.

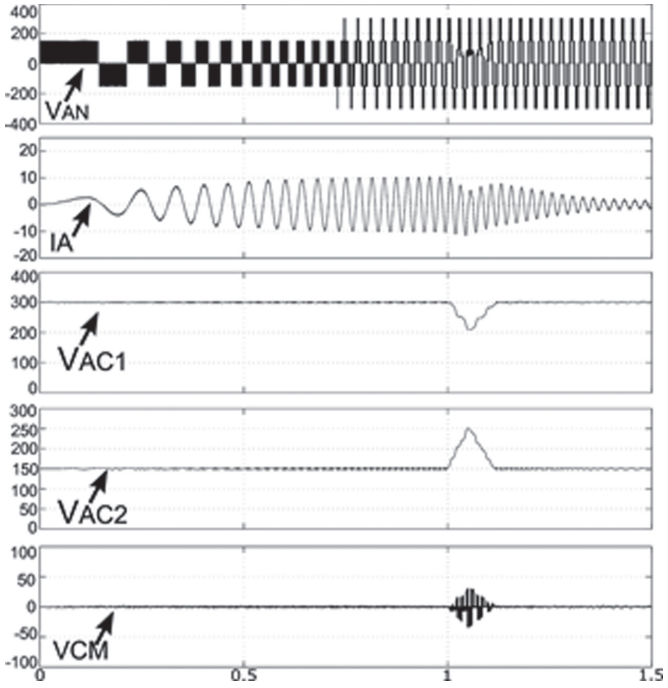


Fig. 8. Simulation result for testing the capacitor balancing algorithm. V_{AO}: pole voltage (100 V/div), I_{A}: pole current (5 A/div) V_{C1}: cap1-voltage (100 V/div), V_{C2}: cap2 voltage (50 V/div), V_{CM}: common-mode voltage (50 V/div), time: 500 ms/div.

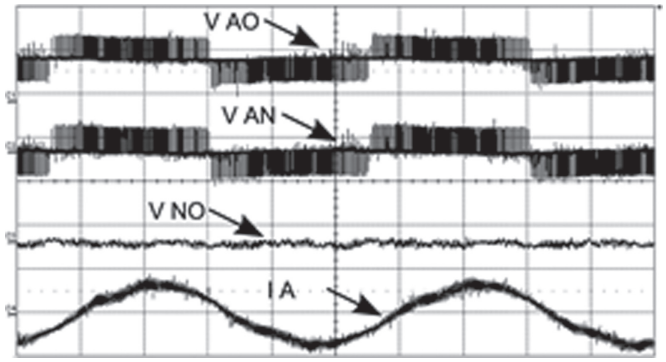


Fig. 9. Steady-state performance at 10 Hz. V_{AO}: pole voltage (100 V/div), V_{AN}: phase voltage (100 V/div), V_{NO}: neutral point voltage (20 V/div), I_{A}: phase current (2 A/div), time: 20 ms/div.

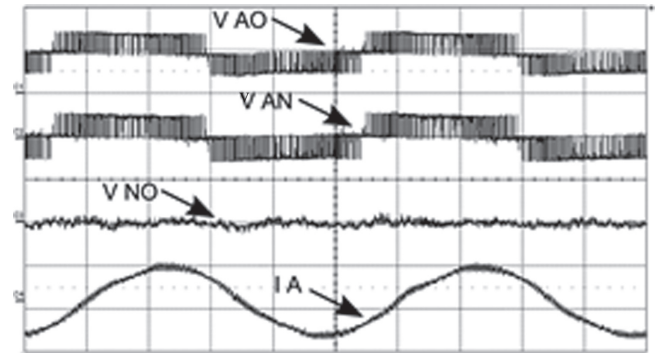


Fig. 10. Steady-state performance at 20 Hz. V_{AO}: pole voltage (100 V/div), V_{AN}: phase voltage (100 V/div), V_{NO}: neutral point voltage (20 V/div), I_{A}: phase current (2 A/div), time: 10 ms/div.

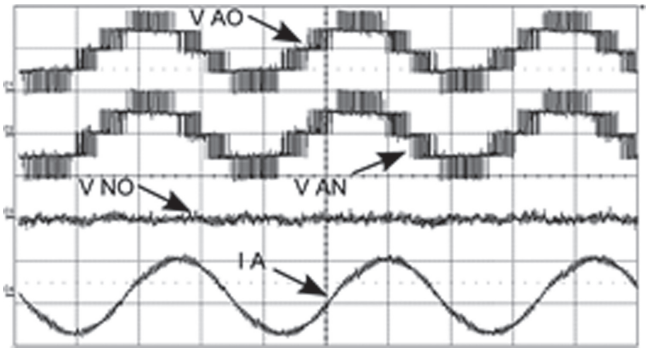


Fig. 11. Steady-state performance at 30 Hz. V_{AO}: pole voltage (100 V/div), V_{AN}: phase voltage (100 V/div), V_{NO}: neutral point voltage (20 V/div), I_{A}: phase current (2 A/div), time: 10 ms/div.

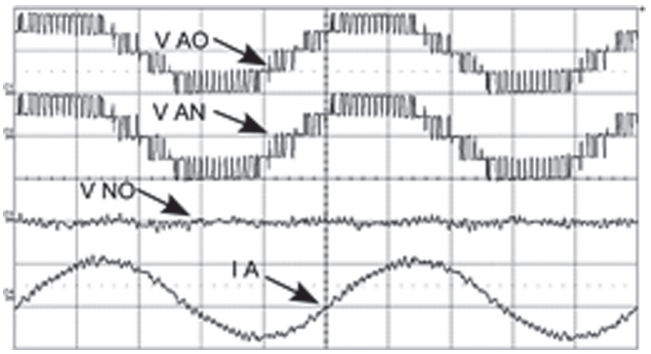


Fig. 12. Steady-state performance at 40 Hz. V_{AO}: pole voltage (100 V/div), V_{AN}: phase voltage (100 V/div), V_{NO}: neutral point voltage (20 V/div), I_{A}: phase current (2 A/div).

V. Implementation

The proposed three-level inverter with common-mode voltage elimination was tested on a 50-Hz, three-phase, Y-connected, 3-kW induction motor. The controller is realized using a TMS320F2812 DSP platform and a Xilinx Spartan-3 XC3200 field-programmabl gate array (FPGA) kit. The inverter was constructed using Semikron SK80GM123D insulated gate bipolar transistor (IGBT) modules driven by M56972L hybrid drivers. The capacitor voltages for all the three phases were sampled every switching cycle and are compared with reference value of ($\mathrm{V_{dc}}$/2) for $C1$ and ($\mathrm{V_{dc}}$/4) for $C2$. These comparator outputs are fed to the FPGA along with the level data and PWM signals of all three phases from DSP. Based on the comparator output, direction of current, level data, and the PWM signals, one of the redundant pole voltage states is applied to balance the capacitors back to their intended values by changing the direction of current fl wing through them. The total dc-bus voltage was chosen as 200 V (+/− 100 V) for verifying the overall system.

The motor was run at frequencies of 10, 20, 30, 40, and 50 Hz, at modulation indices of 0.2, 0.4, 0.6, 0.8, and 0.9 (overmodulation), respectively, at no load. The pole voltage, phase voltage, common-mode voltage, and phase current for 10, 20, 30, 40, and 50 Hz for one of phases are shown in Figs. 9–13, respectively. The pole voltage along with the two capacitor voltages and the phase current for one phase are plotted in Figs. 14–18.

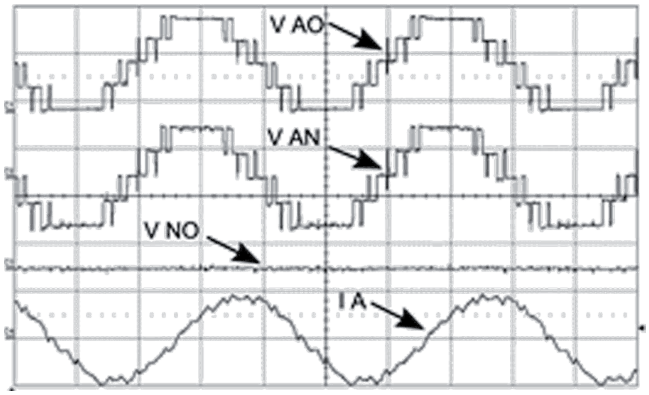


Fig. 13. Steady-state performance at 50 Hz. V_{AO}: pole voltage (100 V/div), V_{AN}: phase voltage (100 V/div), V_{NO}: neutral point voltage (200 V/div), I_{A}: phase current (2 A/div), time: 5 ms/div.

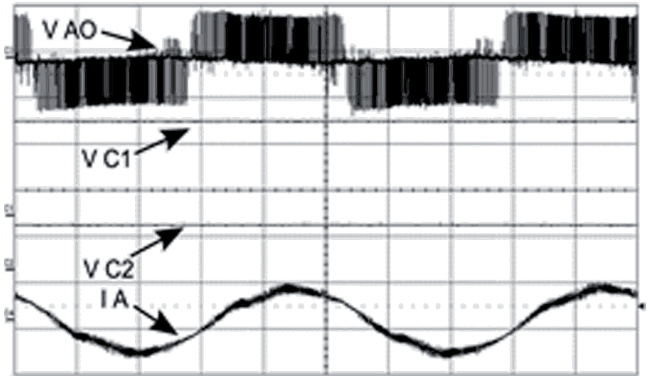


Fig. 14. Steady-state performance at 10 Hz. V_{AO}: pole voltage (50 V/div), V_{C1}: $C1$ ($\mathrm{V_{dc}}/2$) cap voltage (50 V/div), V_{C2}: $C2$ cap voltage (50 V/div), I_{A}: phase current (2 A/div), time: 10 ms/div.

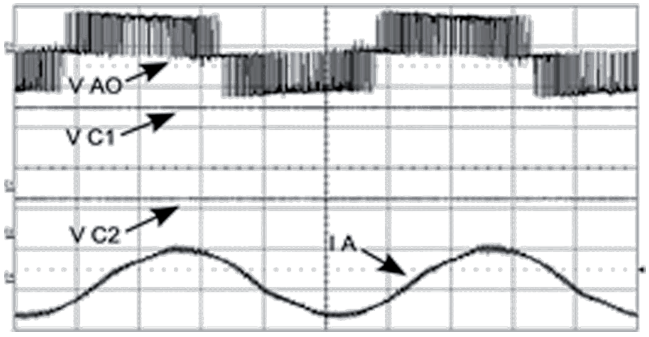


Fig. 15. Steady-state performance at 20 Hz. V_{AO}: pole voltage (50 V/div), V_{C1}: $C1$ cap voltage (50 V/div), V_{C2}: $C2$ cap voltage (50 V/div), I_{A}: phase current (2 A/div), time:10 ms/div.

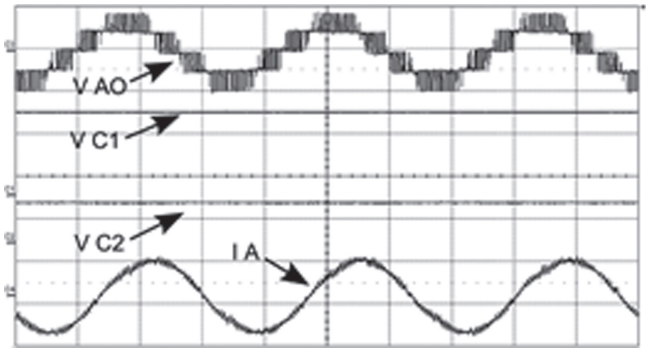


Fig. 16. Steady-state performance at 30 Hz. V_{AO}: pole voltage (100 V/div), V_{C1}: $C1$ cap voltage (50 V/div), V_{C2}: $C2$ cap voltage (50 V/div), I_{A}: phase current (2 A/div), time: 10 ms/div.

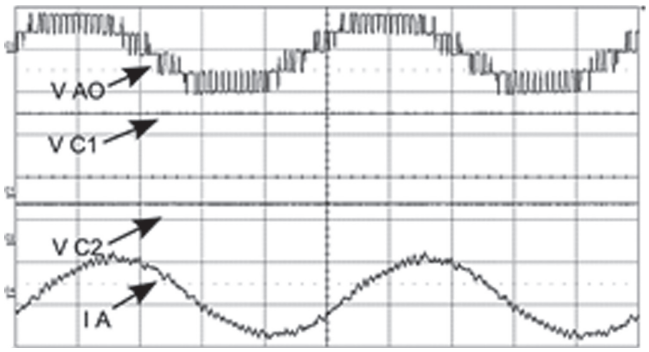


Fig. 17. Steady-state performance at 40 Hz. V_{AO}: pole voltage (100 V/div), V_{C1}: $C1$ cap voltage (50 V/div), V_{C2}: $C2$ cap voltage (50 V/div), I_{A}: phase current (2 A/div).

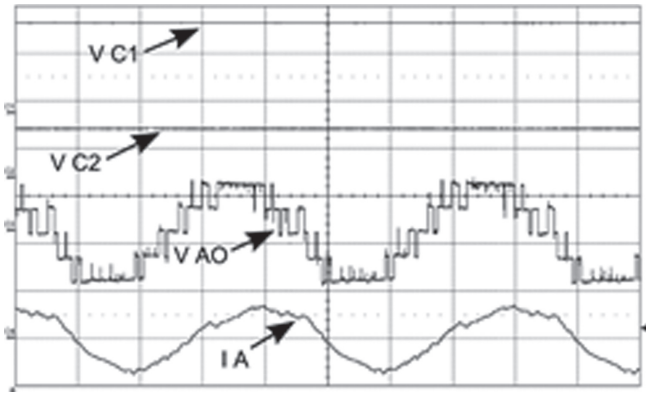


Fig. 18. Steady-state performance at 50 Hz. V_{AO}: pole voltage (100 V/div), V_{C1}: $C1$ cap voltage (50 V/div), V_{C2}: $C2$ cap voltage (50 V/div), I_{A}: phase current (2 A/div), time: 10 ms/div.

It may be observed from the aforementioned results that the common-mode voltage ripple is negligible compared to the dc-bus voltage at all modulation indices and frequencies. Thus, effects of common-mode voltage that lead to mechanical failure of the machines are mitigated.

The motor was suddenly accelerated at no load, during which the stability of the capacitor balancing algorithm was proven and zero common mode was observed throughout the entire range of modulation indices. The phase voltage, capacitor voltage ripple, and the common-mode voltage waveforms along with the phase current during the sudden acceleration process are presented in Fig. 19. It can be observed that the capacitor voltage ripple is less than 2 V even when the motor is drawing huge current during the acceleration period.

The stability of the capacitor balancing algorithm was also tested by disabling and re-enabling the same, as shown in Fig. 20. It may be observed that within few cycles after the controller was enabled, the capacitor voltages were restored back to their intended values and the common-mode voltage was brought back to zero. This feature helps in performing the

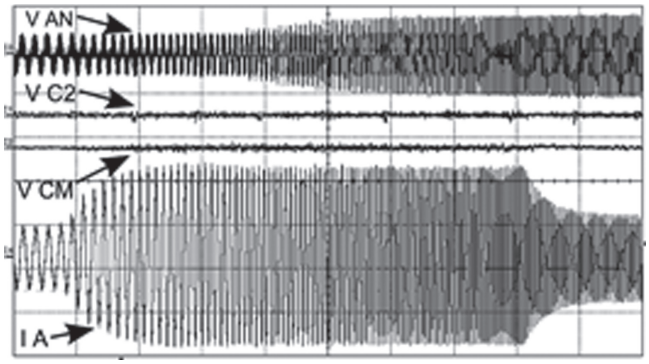


Fig. 19. Acceleration performance. V_{AN}: phase voltage (100 V/div), V_{C2}: $C2$ cap voltage ripple (2 V/div), V_{CM}: neutral point voltage (10 V/div), I_{A}: phase current (2 A/div), time: 500 ms/div.

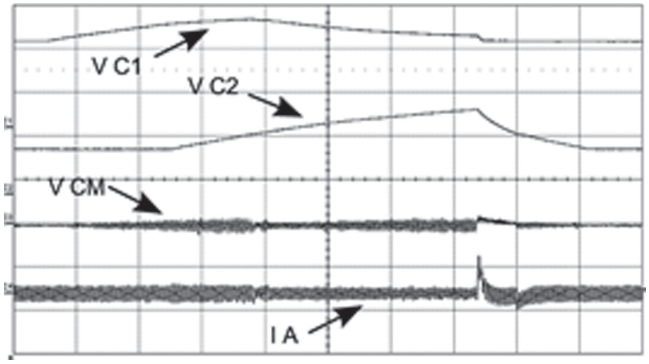


Fig. 20. Capacitor balancing algorithm test, V_{C1}: $C1$ ($V_{\mathrm{dc}}/2$) cap voltage, V_{C2}: $C2$ ($V_{\mathrm{dc}}/4$) cap voltage, V_{CM}: common-mode voltage (10 V/div), I_{A}: phase current (10 A/div), time: 500 ms/div.

"start-on-the-fly operation when the capacitor voltages are not at their intended values. Also, if the capacitor voltages were to momentarily deviate from the desired values, the controller would ensure that the voltages are brought back to their designed values within few fundamental cycles.

VI. Conclusion

In this paper, a three-level common-mode voltage eliminated inverter with single dc supply using flyin capacitor inverter and cascaded H-bridge was proposed and studied. The operation and performance of the proposed inverter is simulated in Simulink with induction motor load. Various aspects of the inverter configuration such as the transients and the performance of the capacitor balancing algorithm, have been studied. The proposed inverter is implemented in hardware using IGBT-based inverters. A three-phase Y-connected induction motor is run with the proposed inverter and the performance of the drive is analyzed for both steady-state operation and transient operation during sudden acceleration. In all the cases, the inverter was able to give faithful reproduction of intended voltage levels with negligible capacitor voltage ripple and common mode, thereby improving the life of bearings. This configuratio has various advantages like motor being connected in single-ended configuration use of reduced number of switches, use of single dc supply, etc. Also, this configuratio has improved reliability. In case of failure of one of the devices in the H-bridge, the inverter can still be operated as a normal three-level inverter at full power or a two-level common-mode voltage eliminated inverter at full power rating by bypassing the H-bridges, thereby improving the overall reliability of the system greatly.

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