

CMOS Operational Amplifiers with Continuous-time Capacitive Common Mode Feedback

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Abstract—A simple and power efficient approach for the implementation of continuous-time common mode feedback networks using a capacitive averaging network is introduced. It is shown that low voltage, continuous-time, fully differential rail to rail operation can be achieved using the proposed technique. This at the expense of very small additional hardware and no additional power dissipation. One stage, two stage, telescopic and folded cascode op-amps are discussed as application examples.

I. INTRODUCTION

Signal processing in modern analog and digital VLSI systems is performed mostly in fully differential fashion. This is due to the well known advantages of increased signal to noise ratio with signal swing scaled by a factor two and to common mode noise rejection in fully differential circuits. These two aspects are critical in fine line CMOS technology that operates from very low supply voltages approaching now $V_{DD} \sim 1V$. Operation with this low supply voltages severely limits signal swing or is not possible at all with most conventional circuits that have been in use for many years.

Fully differential operational amplifiers (Fig. 1a) require a common mode feedback network (CMFBN) to set the common mode output voltage to a reference value V_{refCM} . (Fig. 1a). Traditionally they have been based on continuous time CMFBNs (Fig. 1b and 1c) [1]-[6] or on discrete time switched capacitor CMFBNs (Fig. 1d) [6]-[7]. The later have a very simple architecture and use switched capacitor averaging networks to sense the output common mode voltage. Their main advantage is that they do not load resistively the output nodes. They can be used in one stage op-amps where the open loop gain is strongly dependent on

the load resistance at the output nodes. Their main disadvantage is the inherent speed limitation of sample data systems where signal frequencies must be kept typically a 10-50 below the switching frequency that usually corresponds to the gain bandwidth product (GB) of the op-amp. Switched capacitor CMFBNs are also subject to clock feed through and charge injection errors. Continuous-time CMFBNs can operate at much higher speeds (close to the GB of the op-amp) but they require a relatively large headroom $HR^{MIN} = V_{GS} + V_{Dssat}$ (a transistor's gate-source voltage plus a drain-source saturation voltage) which severely limits the output swing. This headroom is required in order to keep the input circuitry in the CMFBN functional (usually a differential pair as in Figs. 1b and 1c or transistors operating in triode mode [1] are used as active devices to sense common mode output voltage variations). One example is the differential difference amplifier shown in Fig. 1b used commonly as CMFBN [3]-[4]. This circuit finds frequently application in one stage op-amps due to the fact that it does not load resistively the output nodes. The simpler continuous time CMFBN of Fig. 1c [2] can operate with larger output signal swing but requires a minimum headroom $HR^{MIN} = V_{GS} + V_{Dssat}$. This circuit has also the disadvantage that it loads resistively the op-amp's output nodes. For this reason this circuit can be used only in two stage (Miller) or multistage fully differential op-amps and requires relatively large resistors R to prevent open loop gain degradation. Another disadvantage of continuous time CMFBNs (like those of Figs. 1b and 1c) is that they usually add significant power dissipation and Silicon area since the CMFBN must have a gain bandwidth product (GB_{CM}) comparable to the gain bandwidth product (GB) of the main op-amp [6]. This requires bias currents and transistor sizes in the CMFBN which are similar to those used in the main op-amp

In this paper we introduce a very compact continuous-time capacitive common mode feedback network. The proposed

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circuit can be considered the CT counterpart of the discrete time capacitive CMFBN of Fig. 1d. It can operate at similar speed as the main op-amp without clock feed-through or charge injection problems. It does not load resistively the op-amp output nodes and only adds a very small capacitive load. It does not have headroom requirements, so that rail to rail op-amp output swing is possible. It is inherently stable since it is compensated with the op-amp load capacitance and for this reason it does not require additional compensation elements. Its implementation requires very small additional hardware (three small capacitors) and no extra power dissipation. Section II describes the proposed approach. Section III shows its application to some common op-amp architectures and discusses simulations that validate the approach. Section IV provides conclusions

II. CAPACITIVE COMMON MODE FEEDBACK

Fig. 2 shows a telescopic fully differential op-amp used to illustrate the proposed continuous-time capacitive common mode feedback network. The elements of the CMFBN are highlighted and include three capacitors: two of these have equal values C and are connected to the op-amp output nodes. The third capacitor has a value $2C_{CM}$ and is connected to node V_B . The voltage at this node is constant. All capacitors are connected to a common node V_x , at the gates of M4 and M4P. The circuit also includes a DC replica bias circuit formed by transistors M4R and M3R. This is used to generate the DC voltage V_B . Based on charge conservation and assuming, zero net charge on V_x and V_y (a condition easily achievable using the layout technique described in [8]) the voltage V_x at the common gate of M4, M4P is given by:

$$V_x = [(V_{o+} + V_{o-})C + V_b 2C_{CM}] / 2(C + C_{CM} + C_{gs4}) \quad (1)$$

where C_{gs4} is the gate-source capacitance of M4, M4P.

The voltage V_y in the replica bias circuit is given by

$$V_y = (V_b C_{CM} + V_{refCM} C) / (C_{CM} + C + C_{gs4}) \quad (2)$$

Given that transistor M4R has the same current I_B as transistor M4 then assuming both transistors operate in saturation $V_{GS4} = V_{GS4R}$. This leads to

$$V_x = V_y \quad (3)$$

From (1) - (3) we arrive to

$$V_{refCM} = (V_{o+} + V_{o-}) / 2 \dots \dots \dots \quad (4)$$

From (4) it can be seen that the output common mode voltage takes the value V_{refCM}

Remarks:

1) The actual CMFBN of the op-amp consist only of capacitors C and C_{CM} connected to V_x , and does not require additional power dissipation. The replica bias circuit and its associated power dissipation is not considered integral part of the common mode feedback network since it is used only to generate the DC voltage V_B , and can serve several (or all) op-amps in a chip. In the last case it can be buffered.

2) The CT capacitive CMFBN can operate on rail to rail output signals

3) The open loop gains of the differential and common mode feedback loops have similar values and are given by:

$$A_{ol} = g_{m1} R_{out}; \quad A_{olCM} = a g_{m4} R_{out} \quad (5)$$

where "a" is an attenuation factor is given by:

$$a = C / (C + C_{CM} + C_{GS4}) \quad (6)$$

and the output resistance at V_{o+} , V_{o-} is given by

$$R_{out} = (r_{o1} g_{m2} r_{o2}) || (r_{o3} g_{m4} r_{o4}) \quad (7)$$

where $g_{m1}, g_{m2}, g_{m3}, g_{m4}, r_{o1}, r_{o2}, r_{o3}$ and r_{o4} are the transconductance gains and output resistances of M1-M4 respectively. The dominant poles of the open loop gain of the differential and common mode feedback loops are given by

$$f_{pDOM} = 1 / (2\pi R_{out} C_L) \quad (8)$$

where C_L is the load capacitance at V_{o+} , V_{o-} . The gain bandwidth product (GB) for differential and common mode networks is given by

$$GB = g_{m1} / (2\pi C_L); \quad GB_{CM} = a g_{m4} / (2\pi C_L) \quad (9)$$

It can be seen that, as it is commonly required in fully differential op-amps, GB and GB_{CM} can have similar values. In practice attenuation values $a \sim 0.5$ can be used. In this case the selection $g_{m4} = 2g_{m1}$ satisfies the condition $GB = GB_{CM}$. Capacitors C increase the effective capacitive output load and can cause GB (or phase margin) degradation. In practice they can have very small values $C \ll C_L$. In order to prevent a large attenuation factor "a" with the associated reduction in GB_{CM} capacitors C and C_{CM} can be a factor 5 to 10 larger than C_{GS4} . Values $C = C_{CM} = 1.5pF$ were used in all examples. They increased the silicon area of the op-amp by less than 20%.

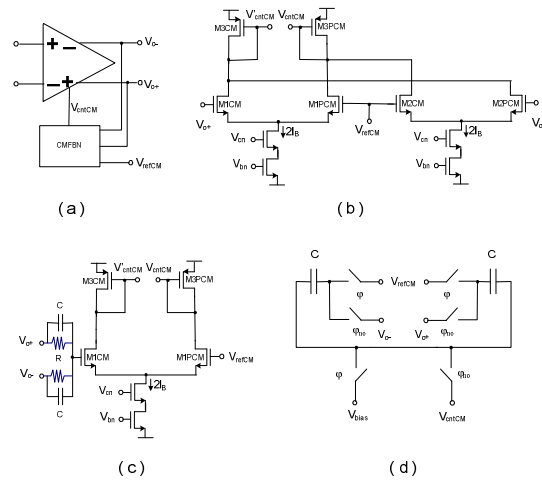


Fig. 1 (a) Generic scheme of fully differential op-amp with common mode feedback network (CMFBN) (b) Continuous-time CMFBN with high input impedance (c) Continuous-time CMFBN with resistor averaging network (d) Discrete time switched capacitor implementation of CMFBN.

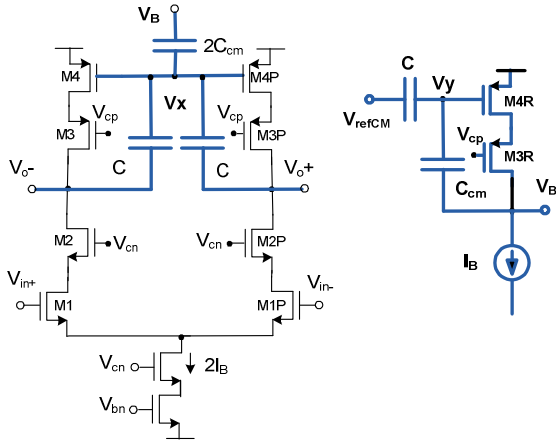
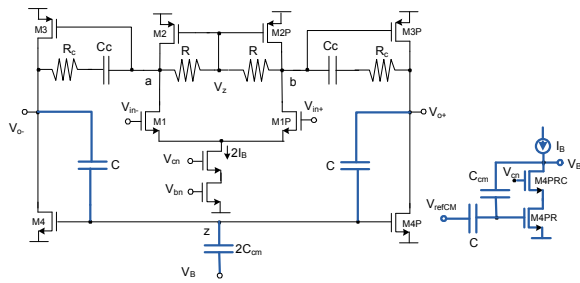
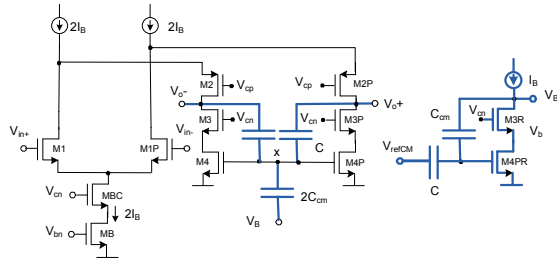


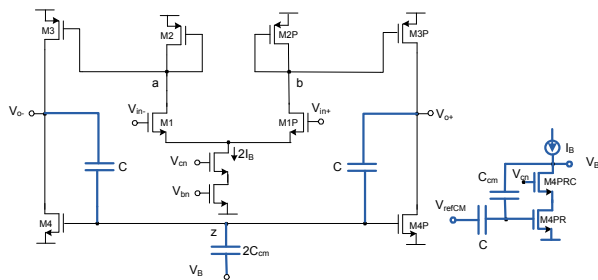
Fig. 2 Fully differential CMOS telescopic op-amp using continuous-time capacitive common mode feedback network



(a)



(b)



(c)

Fig. 3 Fully differential CMOS Operational amplifiers using continuous time capacitive common mode feedback networks (highlighted) (a)Two stage (Miller) op-amp with resistive local common mode feedback in first stage (b)Folded cascade op-amp (c)One stage (current mirror) op-amp

A continuous time capacitive Local CMFBN was reported in [9] that uses charge injection devices. These require generation of high voltages on chip. Additionally the circuit lacks a replica bias circuit and with this the possibility to set the common mode output voltage to a value V_{refCM} .

III. APPLICATION EXAMPLES

Fig. 3a, 3b and 3c shows examples of a Miller op-amp, folded cascade and one stage (current mirror) op-amps with continuous time capacitive CMFBNs. The GB_{CM} analysis and comments of previous section also apply to these circuits. The two stage op-amp of Fig. 3a uses conventional Miller compensation and resistive local common mode feedback (LCMFBN) [10] with resistors R connected between nodes “a” (“b”) to node V_z of the input stage. In this case the gain of the first and second stages is given by $A_{I1}=g_{m1}(R||r_{o1}||r_{o2})$ $A_{I2}=g_{m3}r_{o3}||r_{o4}$. Given that under quiescent conditions no current flows in the LCMFBN resistors R , then voltages $V_z=V_a=V_b$ and $V_{SGQ3}=V_{SGQ2}$. Therefore, the DC current in the output stage is well controlled since it mirrors the DC current in the input stage. The GB of this op-amp is given in this case by the conventional expression $GB=g_{m1}/(2\pi C)$.

The circuits in Fig. 2 and Fig. 3 have been implemented in $0.5\mu m$ CMOS (MOSIS) technology. Post-layout simulations with Spectre-BSIM3v3.2 level 53 transistor models were performed using supply voltages $V_{DD}=0.6V$, $V_{SS}=-0.9V$, $I_B=50\mu A$, $(W/L)_{NMOS}=50/1$, $(W/L)_{PMOS}=120/1$, $V_{inCM}=0V$, $C_L=10pF$, $C_C=10pF$, $R_c=2.5k\Omega$, $C=C_{CM}=1.5pF$, $V_{refCM}=0V$, $C_I=3pF$, $C_F=0.6pF$, $C_B=1pF$, $R=40k$.

Fig. 4 shows the magnitude and phase response of the open loop gain of the op-amps of Figs. 2 and 3 and Table I summarizes some of their performance characteristics. Fig. 6 shows the scheme used to implement a low voltage amplifier with gain $G=C_I/C_F$. This uses op-amps with floating gate transistors in the input differential stage. Capacitors C_I, C_F are used to set the gain and capacitors C_B is used, according to the technique reported in [12], to shift the DC voltage of the op-amp input terminals to a higher value $V_{i+}=V_{i-}=V_{DD}C_B/(C_I+C_B+C_F)$. This increases the HR for the input differential stage and allows operation with very low supply voltages. Fig. 6 shows the transient responses (V_{o+} , V_{o-} , V_o , V_{in}) of the two stage amplifier of Fig. 3a using the scheme of Fig. 5. The amplifier has a nominal gain $G=5$. It uses capacitors $C_I=3pF$, $C_F=0.6pF$, $C_B=1pF$. The input was a $500kHz$ $0.25V_p$ sinusoidal signal.

Table I. Simulated characteristics of op-amps of Figs 2 and 3

Op-amp	GB(MHz)	Aol(dB)	Phase Margin (deg)
2-stage	11.4	59.5	89
1-stage	8.7	62.15	84
Folded-Cascade	7.6	69.1	81.4
Telescopic	8.7	67.15	87.7

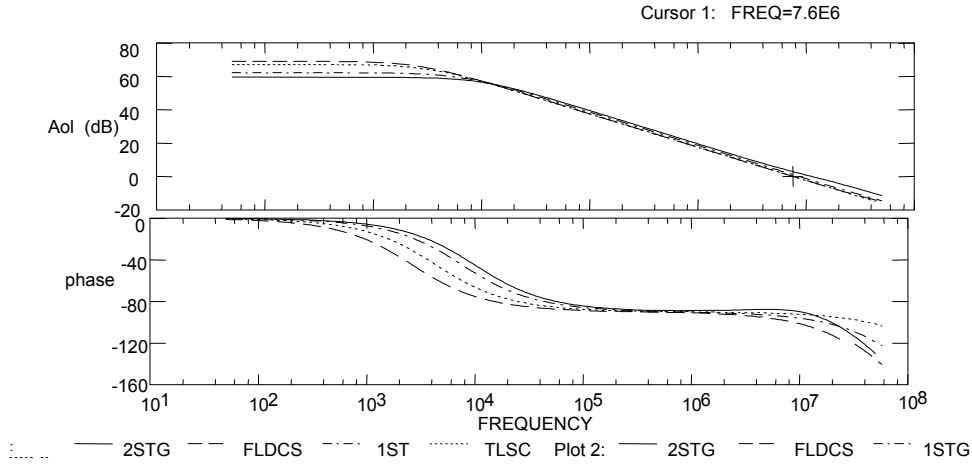


Fig. 4 Open loop and phase response of op-amps of Figs. 2 and 3

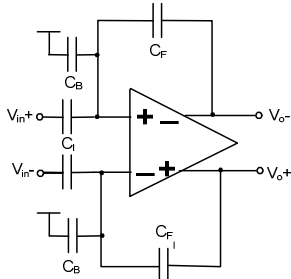


Fig. 5 Implementation of low voltage amplifier with gain $G = -C_F/C_B$

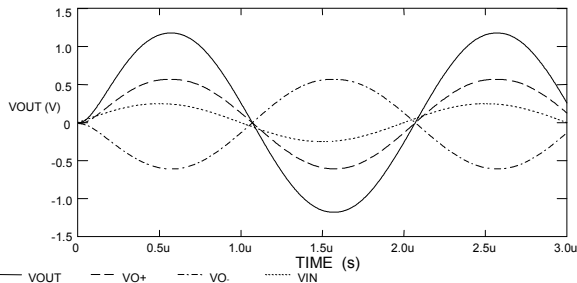


Fig. 6 Output waveforms V_{o+} , V_{o-} , V_{in} and V_o for low voltage amplifier with gain 5 according to Fig. 5 .

IV. CONCLUSIONS

A continuous-time common mode feedback network using capacitors was introduced. It is very compact and allows rail to rail output signal swing. It does not load resistively the output terminals of the op-amp and increases only slightly the output capacitive load. It requires minimal hardware and no additional power dissipation. Its application in one, two stage, folded cascode and telescopic op-amps was discussed. The proposed circuits can operate with very low supply voltages as required in modern fine line technology. All op-amps were validated with simulations in $0.5\mu\text{m}$ CMOS technology.

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