A Novel Switched Capacitor Frequency Tuning Technique For Continuous-Time Gm-C Filters

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***Abstract*— A novel approach for the automatic frequency tuning of Continuous Time Filters is presented. This approach is based on a switched capacitor circuit and only needs three capacitors, some switches and a replica transconductor to adjust the pole frequency of the filter. Despite the simplicity of the scheme, the accuracy of the proposed system is under 1% of frequency error. To evaluate the idea a version of the circuit has been designed in a 0.5 µm CMOS technology with a 3.3 V power supply and simulation results are provided.**

***Keywords*— Frequency Tuning, Gm-C Filters, Switched Capacitor, Transconductor, Low Power.**

I. INTRODUCTION

One of the main problems of the continuous-time Gm-C filters is the need of a tuning circuit. Process variations and temperature changes are the major causes of deviation at the pole frequencies and the quality factor of the filters.

Several techniques, most of them based on master-slave schemes, have been used for tuning. The most popular are:

- PLL based techniques [1][2].
- Adaptive algorithms [3].
- Gm/C tuning techniques [4]-[5].

In master-slave techniques, a replica (master) of the main filter (slave) is inserted in a feedback loop. If a good matching between the two filters is achieved, the same control signal that adjusts the master filter is used to tune the slave one. Although the reference signal is usually quite accurate, the main inconvenience of this technique is the large matching required between the master and the slave filters leads sometimes to quite complex and high power consumption schemes.

In the phase locked loop (PLL) techniques a phase detector, a master filter and a voltage controlled oscillator are placed in a loop. Once the circuit is powered up, the negative feedback of the PLL causes the VCO frequency and phase to lock to an external reference clock. After that, the Gm/C ratio of the VCO is set to a desired value and the tuning voltage can be used to tune the slave filter [6]. The main drawback of these methods is the difficulty of choosing the external clock frequency to achieve a good accuracy avoiding the tuning signal leaks into the main filter.

Adaptive algorithms are based on the same ideas as the other techniques previously mentioned, although with these methods the zeros of the filter are also tuned and therefore a closer matching to the desired transfer function is expected. The main drawback of this method is the complexity of the schemes and the large silicon area needed.

The circuit proposed in this paper uses the Gm/C tuning technique. This method is basically based on designing an extra transconductor in the tuning circuit to generate the control signal for all the transconductors of the filter. Although the use of this technique requires a good matching between the extra transconductor and the filter transconductors, its simplicity allows very low power consumption and small silicon area [4]-[5].

A good example of this kind of tuning circuits is proposed in [4] and it is shown in Fig.1.

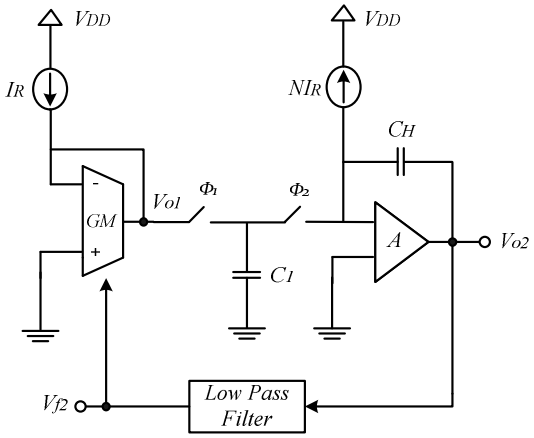

Fig.1. Frequency tuning scheme proposed in [4]

In this circuit, during clock phase Φ_1, capacitor C_1 is charged to I_R/GM. In the clock phase Φ_2, current NI_R discharges the capacitor $C_1$to zero and the charge is transferred to the holding capacitor C_H. In quiescent conditions, the charge introduced in the first phase must be equal to the charge taken away in the second phase. The charge balance is achieved by the integrator. As a result:

$$\frac{GM}{C_1} = \frac{1}{N \cdot T} = \frac{f_{clock}}{N}$$

Despite the simplicity of this tuning circuit, the voltage signal at the SC integrator output exhibits a large variation in every clock period, which prevents it from being directly applied to control the GM value of the transconductors. In practice, the integrator output has to be low-pass filtered both, to provide a stable control signal, and to stabilize the control loop. Although this low-pass filter has no stringent requirements, it consumes a non-negligible area and power.

In this paper, a new version of the circuit in Fig. 1 is proposed where, in the steady state, the SC integrator output is maintained constant so that the low-pass filter can be removed.

The main advantage of the proposed scheme is its simplicity, because it only needs two matched DC current sources and an operational amplifier. Compared with the circuit presented in [4], some advantages can be found:

- The operational amplifier has more relaxed specifications referring to bandwidth.
- It does not need any extra filter at the output of the frequency tuning circuit.

II. Frequency Tuning Circuit Implementation

The proposed frequency tuning circuit is shown in Fig. 2 and it is based on a switched capacitor circuit controlled by three non-overlaping clock signals (Φ_1, Φ_2 and Φ_3).

During the clock phase Φ_1, capacitors C_1 and C_2 are charged to the following values:

$$V_{C1} = \frac{T_1 \cdot I_{b2}}{C_1} \qquad (1)$$

$$V_{C2} = V_{prog} - (V_{cm} - V_{ref}) \qquad (2)$$

where T_1 is the period of time in which Φ_1 is active, Vcm is the input common mode value of the transconductor, Vref is a reference voltage and Vprog is the theoretical control voltage of the tranconductor.

In phase Φ_2, capacitors C_1 and C_2 are connected in series and both in parallel with capacitor C_3, so a charge transfer happens between these three capacitors.

Finally, the only purpose of clock phase Φ_3 is to reset the capacitor C_1 in order to start in a correct value the next clock phase.

In quiescent conditions:

$$V_{out} - V_A = \frac{T_1 \cdot I_{b2}}{C_1} + (V_{cm} - V_{ref}) - V_{prog} \qquad (3)$$

$$I_{b1} = GM \cdot \left[V_{out} - (V_{cm} - V_{ref}) \right] \qquad (4)$$

$$V_{tune} = A \cdot (V_A - V_{prog}) \qquad (5)$$

Using the expressions shown above:

$$GM = \frac{I_{b1}}{\frac{I_{b2} \cdot T_1}{C_1} + \frac{V_{tune}}{A}} \approx \frac{I_{b1}}{I_{b2}} \frac{C_1}{T_1} \qquad (7)$$

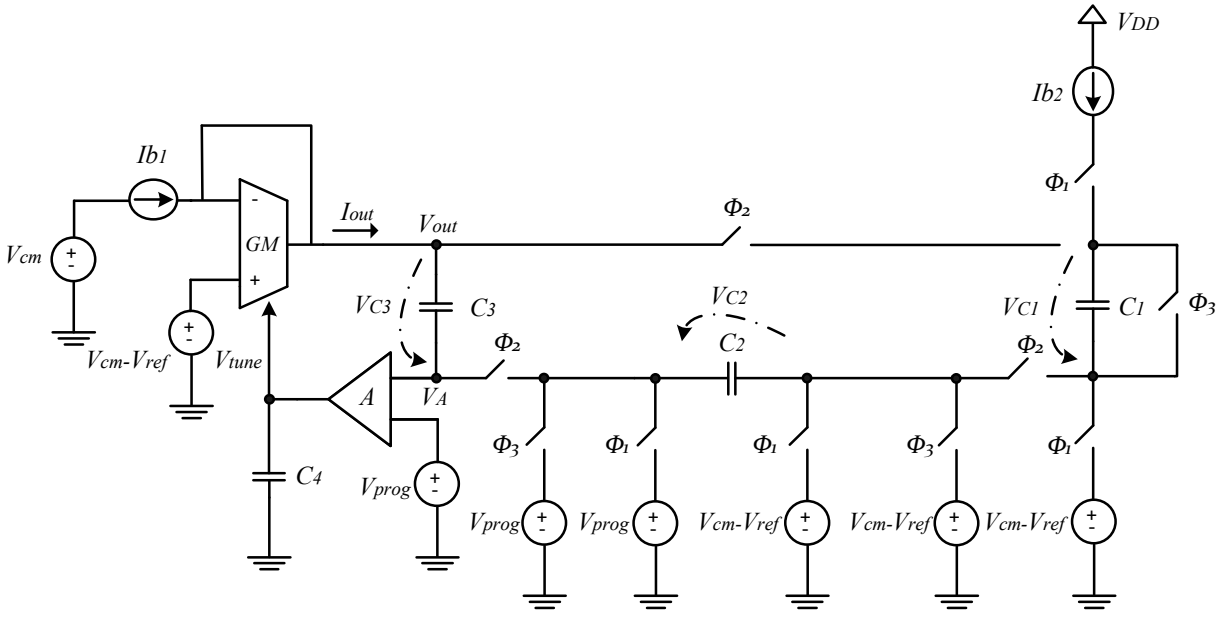

Fig.2. Proposed frequency tuning scheme

As it can be noticed from expression (7) the transconductance value is proportional to the value of capacitor C_1 that will be affected by process variations in the same way the capacitors of the filter.

The term given by $\frac{V_{tune}}{A}$ is just an error that can be negligible if the amplifier gain is high enough.

In our case the amplifier gain needed is 20 dB, so a very simple architecture has been used as shown in Fig.3.

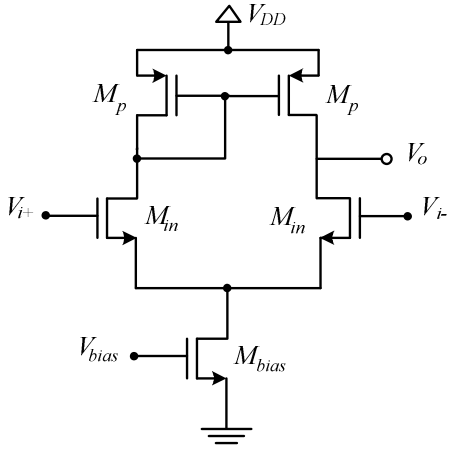

Fig.3. Differential pair

To demonstrate the operation of the proposed frequency tuning circuit, the single-ended version of the transconductor presented in [7] has been used.

It is a programmable source degenerated telescopic cascode OTA improved by a very linear programmable degeneration resistor implemented with four QFG transistors connected in series.

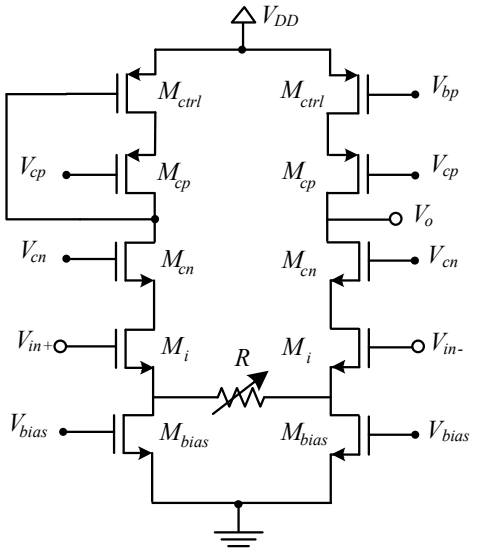

Fig.4. Transconductor

III. Simulation Results

The frequency tuning circuit presented in this paper (Fig.2) has been implemented using a 0.5 µm CMOS technology with a threshold voltage of V_{THP}=-0.96 V and V_{THN}=0.67 V for the P and N MOS transistors respectively. The supply voltage used is 3.3 V.

Table I summarizes the devices values and bias conditions for the circuit proposed.

TABLE I
Device Values And Bias Conditions

Parameter	Value
C_1	8.33 pF
C_2	9 pF
C_3	9 pF
I_{b1}	20 µA
I_{b2}	2.5 µA
Vcm	2.2 V
Vref	0.1 V
Vprog	2.39 V

In order to show the feasibility of the proposed circuit, some simulations have been performed.

Figure 5 shows the voltage in capacitor C_1 in every clock phase. As it is expected during clock phase Φ_1, the capacitor charge from zero to 200 mV according with equation 1. Moreover, when the feedback loop has reached to quiescent conditions, the charge of C_1 does not change during phase Φ_2. And finally, the charge of the capacitor is completely removed during phase Φ_3.

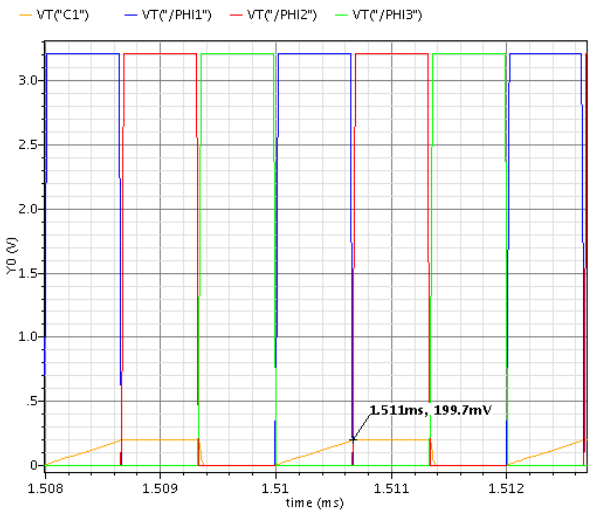

Fig.5. Voltage in capacitor C_1 and clock phases

In the next figure the voltage in capacitor C_2 can be seen. The value in phase Φ_2 can be easily calculated with the values given in table I. In our case:

$$V(C_2) = V_{prog} - (V_{cm} - V_{ref}) = 0.29mV$$

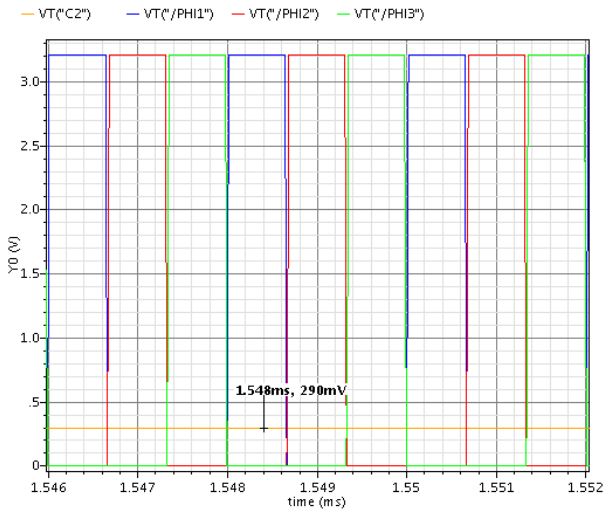

Fig.6. Voltage in capacitor C_2 and clock phases

Finally, voltage in capacitor C_3 is shown in figure 7. Expression 3 gives its value in quiescent conditions.

$$V(C_3) = \frac{T_1 \cdot I_{b2}}{C_1} + (V_{cm} - V_{ref}) - V_{prog} = -0.09V$$

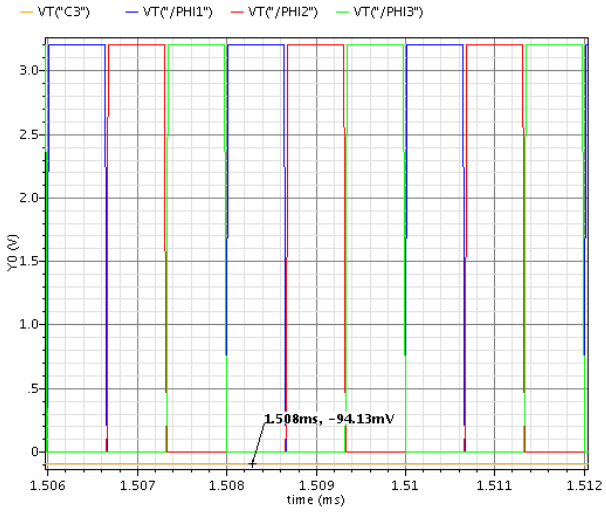

Fig.7. Voltage in capacitor C_3 and clock phases

The next figure shows the transconductor input voltage when a nominal transconductance of 100 µA/V is expected. In this simulation, the effect of the amplifier offset and finite gain as well as the non idealities of the cascode current sources have been taken into account.

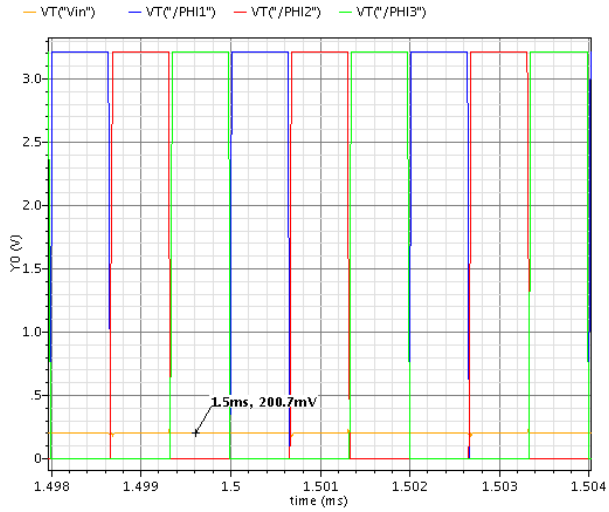

Fig.8. Transconductor input voltage

According to equation 4, to obtain the desired transconductance value, the input voltage at the transconductor should be:

$$G_M = \frac{I_{B1}}{V_{in}} \leftrightarrow V_{in} = \frac{I_{B1}}{G_M} = 200mV$$

As it can be noticed from the simulation above, with an amplifier gain of 20 dB, a 200.7 mV input voltage is obtained at the transconductor input, with corresponds to a 99.65 µA/V transconductance. A 0.35% of error is committed in the transconductance value according with the expected value given by equation (7).

Moreover, with the aim of showing the accuracy of the proposed circuit, some simulations varying capacitance of C_1 have been performed. It can be noted that, despite the variation of the capacitor is high, the gm/C maintains its value with less than 1% of variation.

TABLE II
GM/C RATIOS

C_1 (pF)	I_{b1} (µA)	V_{in} (mV)	GM (µA/V)	GM/C_1
7	20	237.3	84.28	12.04e6
8	20	208.7	95.83	11.98e6
8.33	20	200.7	99.65	11.96e6
9	20	186.3	107.35	11.93e6
10	20	168.4	118.76	11.88e6

IV. CONCLUSIONS

A new frequency tuning circuit based on a switched capacitor circuit has been presented. The purpose is to generate the tuning voltage needed to adjust the transconductance of the extra transconductor designed to tune the supposed filter under design. The main advantage of the proposed circuit is its simplicity, because only a replica of the transconductor and a low gain operational amplifier is needed.

Simulations results show the features of the proposed technique and its good accuracy without the need of an extra low pass filter.

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