Rail-to-Rail Class AB CMOS Tunable Transconductor with -52dB IM3 at 1MHz

Lucia Acosta [#], Antonio J. Lopez-Martin [*], Ramon G. Carvajal [#], Jaime Ramirez-Angulo [$]

[#] *Dpto. de Ing. Electronica, Escuela Superior de Ingenieros, Universidad de Sevilla, Sevilla (Spain)*

[*] *Dept. of Electrical and Electronic Engineering, Public University of Navarra, Pamplona (Spain)*

[$] *Klipsch School of Electrical and Comp. Eng., New Mexico State University, Las Cruces, NM (USA)*

***Abstract*— A novel CMOS tunable transconductor is presented. The circuit operates in classAB hence featuring power efficiency. The internal feedback employed and the use of a linearized triode transistor for voltage-to-current conversion allows achieving high linearity. Rail-to-rail input range is obtained by using floating-gate transistors. Measurement results for a test chip prototype in a 0.5µm standard CMOS process show an IM3 of -52.13dB at 1MHz for a 2Vpp input and a power consumption of 2.2mW.**

***Keywords*— Transconductor, linear OTA, class AB circuits, analog CMOS circuits, analog integrated circuits.**

I. Introduction

Transconductors are widely employed in several analog and mixed-signal applications, such as continuous-time filtering, variable-gain amplifiers, voltage-to-current conversion, etc. Technology scaling as well as current trends of modern wireless transceivers [1]-[2] demand solutions featuring power efficiency and maximum dynamic range, favoring rail-to-rail operation. It is difficult to conciliate these requirements with the need for high linearity, which is critical in several applications today like channel selection filters in COFDM receivers. Achieving transconductors combining high power efficiency, tunability and high linearity is a difficult task.

Due to their open-loop operation transconductor usually feature limited linearity [3]. To solve this shortcoming several proposals to increase linearity of transconductors have been reported. Many of them are based on nonlinearity cancellation, so they require accurate matching of MOS transistors to achieve it, and they are very sensitive to second-order effects affecting these transistors. Due to process variations and geometric mismatch, linearity usually is worse than -50 dB following this approach. The preferred choice for highly linear transconductors is the use of passive resistors for voltage-to-current conversion. Unfortunately passive resistors are not tunable so that continuous tuning is difficult to achieve.

Another drawback of most conventional transconductors is that they usually operate in class A, i.e., the maximum current they can provide is limited by the bias current. Hence to achieve large dynamic range large bias currents are required, increasing static power consumption.

In this paper we propose a novel transconductor that overcomes these drawbacks, which makes it a good candidate for applications like channel filtering in low-power wireless receivers. It combines high linearity, rail-to-rail input range, continuous transconductance tuning, and class AB operation. Linearity is achieved by using Quasi-Floating-Gate (QFG) techniques [4] to linearize a MOS transistor operating in the triode region, which performs voltage-to-current conversion. The voltage followers that translate the input voltage to the triode transistor employ negative local feedback, thus increasing accuracy and therefore further improving linearity. Rail-to-rail input range is obtained by the use of floating-gate techniques [5]. Class AB operation is also achieved using QFG techniques. The transconductor has been designed and implemented in a 0.5µm CMOS technology, and measurement results demonstrating the advantages mentioned are presented.

The paper is organized as follows: Section II describes the principle of operation of floating-gate transistors, and Section III reviews QFG techniques. The transconductor designed is described in Section IV, and measurement results of a test chip prototype containing the transconductor are presented in Section V. Finally, some conclusions are drawn in Section VI.

II. Floating-Gate MOS Transistors

The proposed transconductor is based on the use of the two-input Floating Gate MOS (FGMOS) transistor shown in Fig. 1 to allow rail-to-rail input signals. The polysilicon floating gate is capacitively coupled to both inputs using a second polysilicon layer [5]. Since the total charge at the floating gate must be conserved, the floating-gate voltage will be [5]:

$$V_{FG} = \left(C_1 V_1 + C_2 V_2 + C_{GS} V_S + C_{GD} V_D + C_{GB} V_B + Q_0\right) / C_T \quad (1)$$

where $C_T = C_1 + C_2 + C_{GS} + C_{GD} + C_{GB}$, and Q_0 represents the initial charge trapped in the floating gate during fabrication. This charge can lead to large dc offsets if it is not removed after fabrication (e.g., using UV lighting). This factor has precluded the wide industrial acceptance of FGMOS circuits for analog design in the past. The method proposed in [6] has been employed in this work to avoid this issue. A dummy stacked contact including all the metal layers has been created on the floating gate. Therefore, during deposition of each metal layer and before selective etching, all the nodes sharing this layer are connected to the floating gates, offering a low-impedance path that discharges them. The final metal etching

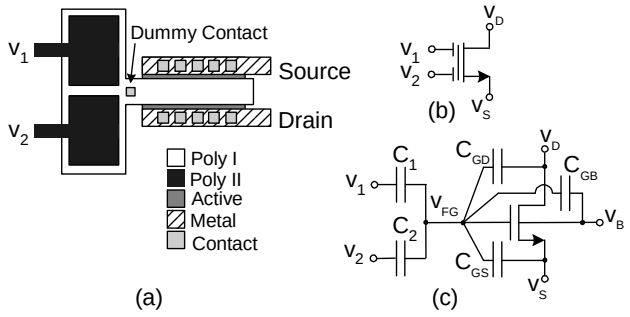

Fig. 1. Two-input FGMOS transistor
(a) Layout (b) Symbol (c) Equivalent circuit

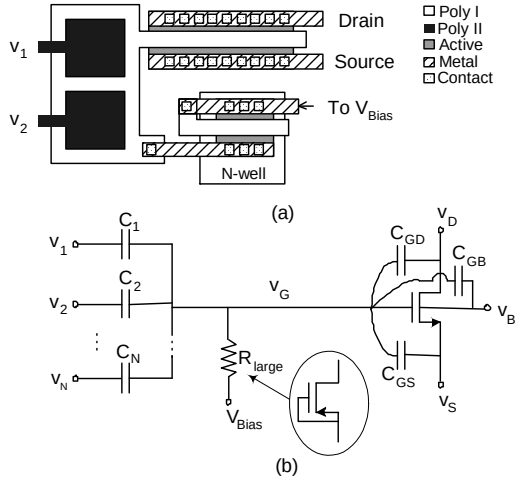

Fig. 2. N-input QFG MOS transistor (a) Layout (b) Equivalent circuit

restores the floating condition to these gates. Therefore, gate charge is removed in fabrication, and Q_0 becomes negligible.

To achieve a rail-to-rail input swing in the transconductor, the PMOS input transistors are two-input FGMOS transistors [7]. This way the gate of the input transistors is capacitively coupled to the differential input voltage V_{id} by a capacitor C_1 and to V_{SS} by another capacitor C_2. Assuming that the intrinsic capacitance at the gate terminal is much smaller than C_1+C_2, the differential voltage at the input gates becomes:

$$V_{FGd} = \frac{C_1}{C_1 + C_2} V_{id} + \frac{C_2}{C_1 + C_2} V_{SS} \qquad (2)$$

yielding a gate voltage which corresponds to the input voltage attenuated by a factor $k= C_1/(C_1+C_2)$ and level-shifted by a dc voltage $V_{SS}C_2/(C_1+C_2)$. By properly choosing C_1 and C_2 a rail-to-rail input swing can be adjusted to the voltage headroom available at the gate of the input transistors.

III. Quasi-Floating-Gate MOS Transistors

An alternative to FGMOS transistors is weakly connecting the floating gate to a proper dc bias voltage using a large-valued resistor R_{large}. The equivalent circuit of the resulting N-input Quasi-Floating Gate (QFG) transistor is shown in Figure 2b, and the resulting layout for a 2-input QFG device is shown in Figure 2a. The input terminals are capacitively coupled to

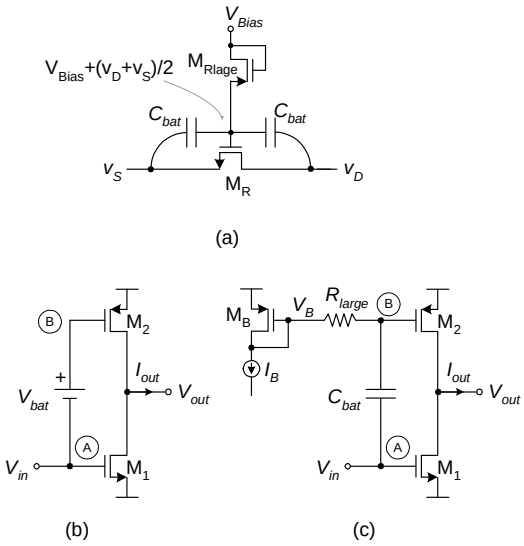

Fig. 3. (a) Linearization of NMOS triode transistor by QFG technique
(b) Basic class AB stage using floating battery (c) Implementation of battery using QFG transistor

the quasi-floating gate, just like in the FGMOS transistor, but in this case the dc gate voltage is set to V_{bias} without requiring another capacitor as in FGMOS transistors. This large resistor can be implemented in practice by the large (and nonlinear) leakage resistance of reverse-biased *pn* junctions of an NMOS transistor operating in cutoff region, as shown in Figure 2. This fact leads to significant savings in terms of area compared to the FGMOS device when the gate voltage requires a dc voltage near a supply rail.

The ac voltage at the quasi-floating gate is given by

$$v_G \approx \frac{sR_{large}}{1 + sR_{large} C_T} \left(\sum_{k=1}^{N} C_k v_k + C_{GS} v_S + C_{GD} v_D + C_{GB} v_B \right) \qquad (3)$$

where lowercase v denotes ac voltage and C_T is

$$C_T = \sum_{k=1}^{N} C_k + C_{GS} + C_{GD} + C_{GB} + C'_{GD} \qquad (4)$$

Note from (3) that inputs are high-pass filtered with a cutoff frequency $1/(2\pi R_{large} C_T)$, which can be made very low (< 1Hz). Therefore, even for very low frequencies, (3) becomes a weighted averaging of the ac input voltages determined by capacitance ratios, plus some parasitic terms. Note also that the exact value of R_{large} or its temperature and voltage dependence are unimportant, if R_{large} remains large enough in order not to influence the circuit operation at the lowest frequency required. This allows the efficient implementation of R_{large} in Fig. 2. The exact value of C_T is also unimportant.

The QFG technique can be employed to perform a weighted voltage averaging at a node of the circuit and simultaneously to independently set the dc bias voltage at this node. Using this idea linearity of a MOS transistor in triode region can be improved. It is well known that the linearity of a MOS transistor in the triode region can be increased if the common-mode of the drain and source voltages is applied to the gate voltage [8]. This can be easily done using QFG techniques, as

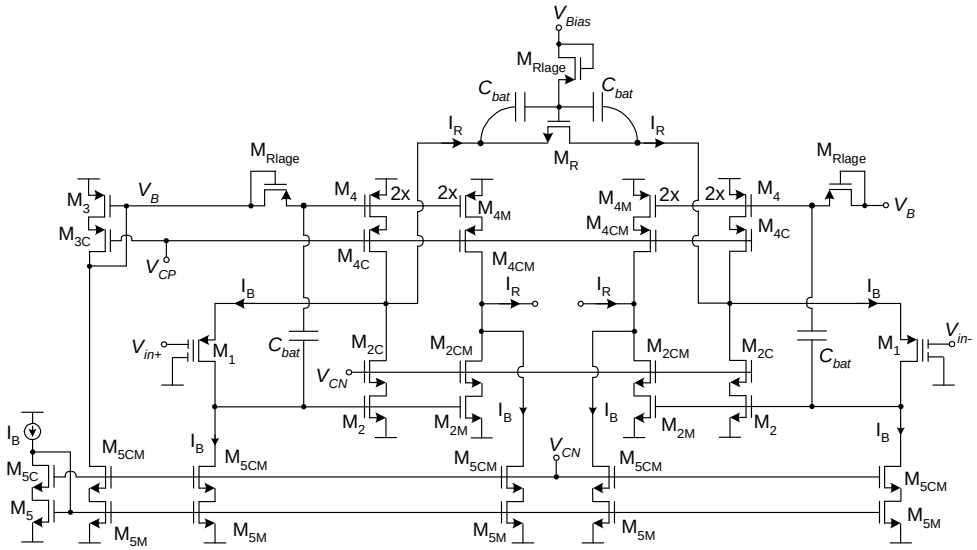

Fig. 4. Detailed schematic of the proposed class AB transconductor

shown in Fig. 3a. The dc gate voltage is accurately set to V_{Bias}, and can be modified to achieve different resistance values. Simultaneously, the ac gate voltage is set to the voltage $(v_D+v_S)/2$ by the capacitive divider, thus improving linearity.

The QFG technique can also be employed to achieve class AB operation [9]. Figure 3b shows a typical scheme of a class AB output stage. It is based on the use of a floating battery that allows node B to track voltage variations at node A with a dc level shift V_{bat}. Under quiescent conditions, the quiescent current is set by voltage at node A and the dc level shift V_{bat}. Under dynamic conditions, signal variations at node A are transferred to node B allowing to provide output currents not limited by the quiescent current. The dc level shift has been implemented in several ways in the technical literature, e.g. using diode-connected transistors or resistors biased by dc currents. The disadvantages of these approaches are that the implementation of the battery requires extra quiescent power consumption. Besides the quiescent current is often not accurately set, it is often dependent on process and temperature variations, and the parasitics added by this extra circuitry may limit speed.

Figure 3c shows how QFG techniques can be employed to efficiently implement the floating battery of Fig. 3b. The quiescent current is accurately set to the bias current I_B, regardless of supply voltage, thermal, and process variations as it is set by a current mirror. Under dynamic conditions, voltage at node A is transferred to node B after being high-pass filtered with a cutoff frequency $1/(2\pi R_{large}C_{bat})$. Due to the large resistance employed (in the order of GigaOhms) this cutoff frequency is typically below 1 Hz, so in practice only the dc component of voltage at node A is not transferred to node B. Note that the implementation of the dc level shifter in Fig. 3c does not require additional quiescent power consumption. The increase in silicon area is modest as R_{large} is made by a minimum-size MOS transistor and C_{bat} can be relatively small (with the minimum value imposed by the parasitic capacitance at node B).

IV. Implementation of the Transconductor

Fig. 4 shows the circuit schematic of the class AB transconductor proposed. Input transistors M_1 are two-input FGMOS transistors that allow rail-to-rail input signals according to (2). The input voltage thus scaled is translated to the triode resistor M_R by a differential voltage follower formed by the source follower M_1 and the negative feedback loop provided by M_2-M_{2C} which improves accuracy of the follower. Class AB operation in this differential source follower is achieved by the floating capacitor C_{bat} and the minimum-size transistor M_{Rlarge} implementing R_{large}, according to Fig. 3c.

The input voltage translated to the terminals of transistor M_R, is converted into current I_R by this transistor, according to the scheme of Fig. 3a. The dc voltage V_{Bias} is applied to the gate of M_R via a minimum-size transistor as large resistive element, and thus sets the transconductance value. This current is translated to a high-impedance output by replicating the output branch of the voltage followers employed, as shown in Fig. 4. Conventional common-mode feedback (not shown for brevity) can be employed.

V. Measurement Results

The proposed tunable transconductor was fabricated in a 0.5μm CMOS n-well process with nominal nMOS and pMOS threshold voltages of 0.67 V and –0.96 V, respectively. Figure 5 shows a microphotograph of the circuit. The silicon area employed is 0.07 mm^2. Capacitor C_{bat} was implemented with two polysilicon layers and has a nominal value of 1 pF. Transistor dimensions W/L (in μm/μm) were 100/1 (M_1, M_{5C}, M_{5CM}), 60/1 (M_2, M_{2M}), 60/0.6 (M_{2C}, M_{2CM}), 100/0.6 (M_3, M_4, M_{4M}, M_6), 200/0.6 (M_{3C}, M_{4C}, M_{4CM}, M_{6C}), 100/3 (M_5, M_{5M}).

Aspect ratio of transistor M_R is 3/1, and poly-poly input capacitors were C_1= 1 pF and C_2= 2 pF. To allow for a wide tuning range of the triode transistor in the technology employed, which features large threshold voltages, a single supply voltage of 5V was employed.

Figure 6 shows the measured dc transfer characteristics for different values of the tuning voltage V_{Bias}, which were measured using a very low frequency periodic input ramp. Note the good linearity obtained for rail-to-rail input voltages. The measured output spectrum for two input tones of 950 kHz and 1050 kHz and 0.5V_{pp} is shown in Fig. 7, showing an IM3 of -74.66 dB. When the input amplitude increases to 2V_{pp}, IM3 is -52.13 dB. Table I summarizes the main performance parameters of the transconductor.

VI. Conclusion

A novel class AB tunable transconductor has been presented and verified experimentally. The circuit features good dynamic performance with low distortion and at the same time low quiescent power consumption. The circuit can be applied to Gm-C channel filters in wireless receivers requiring very low power consumption.

Acknowledgment

This work has been supported in part by the Spanish Dirección General de Investigación and FEDER under grant TEC2007-67460-C03/MIC

Fig. 5. Micrograph of the class AB transconductor

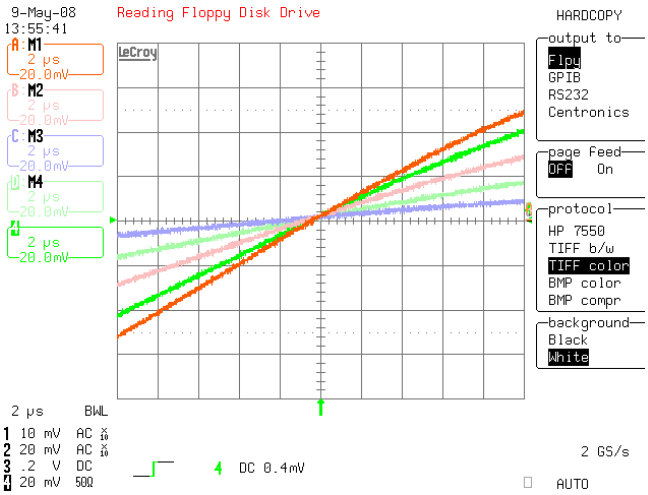

Fig. 6. Measured dc response for different values of voltage V_{Bias}.

References

[1] P. Quinlan, P. Crowley, M. Chanca, S. Hudson, B. Hunt, K. Mulvaney, G. Retz, C.E. O'Sullivan, and P. Walsh, "A multimode 0.3-200-kb/s transceiver for the 433/868/915-MHz bands in 0.25-um CMOS," *IEEE J. Solid-State Cir.*, vol. 39, no. 12, pp. 2297-2310, Dec. 2004.

[2] B. Guthrie, J. Hughes, T. Sayers, and A. Spencer, "A CMOS gyrator low-IF filter for a dual-mode Bluetooth/ZigBee transceiver," *IEEE J. Solid-State Cir.*, vol. 40, no. 7, pp. 1872-1879, Sep. 2005.

[3] A. Lewinski and J. Silva-Martinez, "A 30-MHz fifth-order elliptic low-pass CMOS filter with 65-dB Spurious-Free Dynamic Range," *IEEE Trans. Circ. Syst. I*, vol. 54, no. 3, pp. 469-480, Mar. 2007.

[4] J. Ramirez-Angulo, A.J. Lopez-Martin, R.G. Carvajal, and F. Muñoz-Chavero, "Very low voltage analog signal processing based on Quasi Floating Gate transistors," *IEEE J. Solid State Cir.*, vol. 39, no. 3, pp. 434-442, Mar. 2003.

[5] J. Ramírez-Angulo and A. Lopez, "MITE circuits: The continuous-time counterpart to switched-capacitor circuits," *IEEE Trans. Circuits Syst. II,* vol. 48, pp. 45-55, Jan. 2001

[6] E. O. Rodríguez-Villegas and H. Barnes, "Solution to trapped charge in FGMOS transistors," *Electron. Lett.,* vol. 39, pp. 1416-1417, Sep. 2003.

[7] J. Ramirez-Angulo, S.C. Choi, G. Gonzalez-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors," *IEEE Trans. Circ. Syst. I*, vol. 42, no. 11, pp. 971-974, Nov. 1995.

[8] A. Torralba, C. Lujan-Martinez, R.G. Carvajal, J. Galan, M. Pennisi, J. Ramirez-Angulo, A.J. Lopez-Martin, "Tunable linear MOS resistors using Quasi-Floating-Gate techniques," *IEEE Trans. Circ. Syst. II*, vol. 56, no. 1, pp. 41-45, Jan. 2009.

[9] A.J. Lopez-Martin, J. Ramirez-Angulo, R.G. Carvajal, and L. Acosta, "Power-efficient class AB CMOS buffer," *Electron. Lett.,* vol. 45, no. 2, pp. 89-90, Jan. 2009.

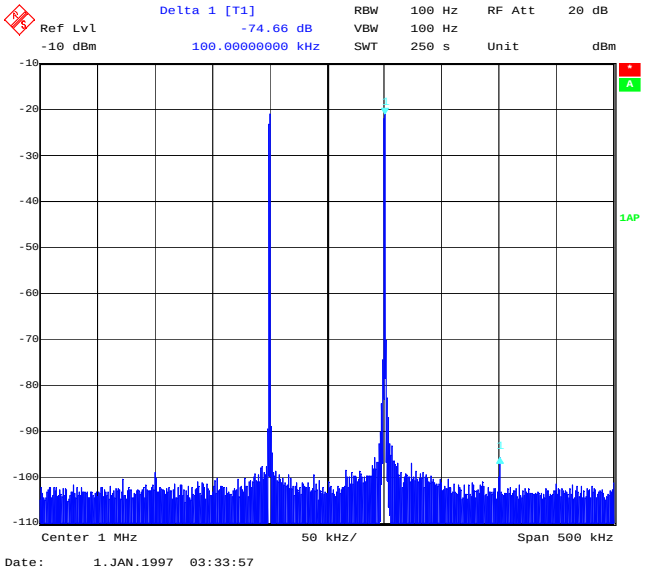

Fig. 7. Measured output amplitude spectrum for two input tones at 950 kHz and 1050 kHz.

TABLE I
MAIN MEASURED PERFORMANCE PARAMETERS

Parameter	Value
Technology	0.5µm CMOS
Supply Voltage	5V
IM3 @1MHz, 2Vpp	-52.13dB
Quiescent power consumption	2.2 mW
Silicon area	0.07 mm^2