New High Performance Second Generation CMOS Current Conveyor

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Abstract— **A new high performance second-generation CMOS current conveyor architecture is presented. It is built using a differential flipped voltage follower as its input buffer stage and a cascode current mirror as output stage. It is characterized by very low output impedance. It provides gain independent high bandwidth when used to implement a programmable gain voltage amplifier. Simulation and experimental results in AMI 0.5µm CMOS technology are provided to validate the characteristics of the design.**

***Keywords*— Analog integrated circuits, current mode signal processing, current conveyor.**

I. Introduction

Current mode signal processing is suitable for the implementation of low voltage, low power, and high bandwidth analog circuits [1]. The second generation current conveyor (CCII) is used as a basic building block in many current mode analog circuits. It is a three-terminal (X, Y and Z) device as shown in the Fig. 1. It consists of a voltage buffer having input terminal Y and output terminal X, and a current mirror that copies the buffer's output current and conveys it to the high-impedance output terminal Z [2].

The performance of the CCII is strongly dependent on the characteristics of the voltage buffer and the current transfer accuracy between the X and Z terminals [2]. An ideal CCII has the following characteristics:

- Infinite input impedance at terminal Y ($R_Y = \infty$ and $I_Y = 0$)
- Zero input impedance at terminal X ($R_X = 0$)
- Accurate voltage copy from terminal Y to X ($V_X = V_Y$)
- Accurate current copy from terminal X to Z with infinite output impedance at Z ($I_Z = I_X$ and $R_Z = \infty$)

One important shortcoming of CMOS CCII's with a one stage buffer reported in literature [3] is that their input impedance R_X is relatively high ($R_X = 1/g_m \sim k\Omega$). This can introduce significant errors in CCII based circuits (like amplifiers) since the external resistance R connected to terminal X must satisfy the condition $R >> R_X$. This paper presents a new CCII architecture that provides very low input impedance at terminal X (in the range of few tens of Ω) with a one stage buffer. It also provides very high output impedance at terminal Z (in the range of M Ω) and accurate current copy from terminal X to Z.

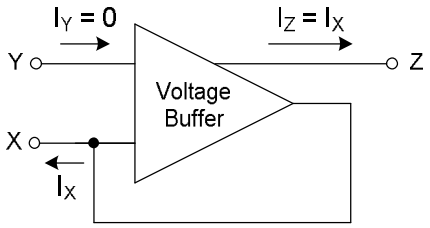

Fig. 1 Simplified Diagram of CCII

II. Proposed Second-Generation CMOS Current Conveyor

A. Differential Flipped Voltage Follower

The proposed CCII is based on a circuit denoted differential flipped voltage follower (DFVF). Fig. 2(a) shows the circuit of the DFVF proposed in [4], [5]. It is characterized by very low output impedance, wide signal range and higher gain accuracy. The DFVF output impedance at node X is given by,

$$R_{,} \cong \frac{\qquad}{\cdot(\quad)} \qquad (1)$$

which is in the range of few tens of ohms in CMOS technology, (g_m is the small signal transconductance and r_o is the output impedance of the transistors) while the output impedance of the conventional voltage follower (CVF) (Fig. 2(b)) is $R_{X,CVF} = 1/g_m$ which is relatively high (few kΩ).

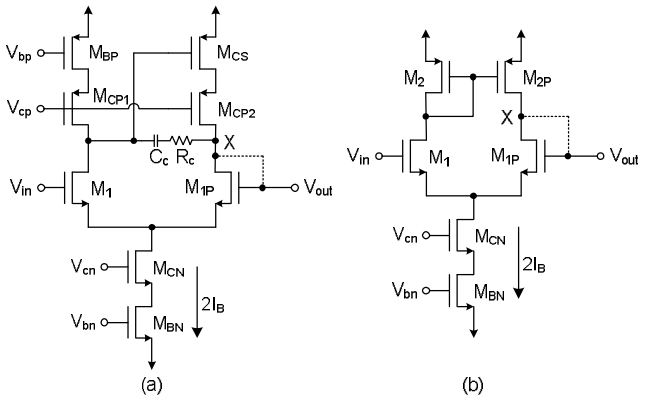

Fig. 2 (a) Differential Flipped Voltage Follower, (b) Conventional Voltage Follower

B. CCII based on DFVF

Fig. 3 shows the proposed CMOS CCII circuit. It uses the DFVF as its input buffer stage as it provides much lower output impedance compared to a CVF and an accurate voltage copy from terminal Y to X is obtained (as discussed in section IIA). A cascode current mirror is used as the output stage to ensure accurate current copy from terminal X to Z. For this reason the DFVF is more appropriate than the CVF for the implementation of CCII's. Some authors use a two stage op-amp to achieve low output impedance but this approach is less power efficient and requires Miller compensation [3], [6].

C. CCII Performance Characteristics

Straightforward AC analysis is used to derive the following characteristics of the circuit in Fig. 3.

1) Output Impedance: The output impedance at node Z is very large and it is given by,

$$R \cong \frac{\quad}{\quad} \tag{2}$$

2) *Input Impedance at node X:* The input impedance at node X is very low due the DFVF implementation of the buffer and it is given by,

$$R \cong \frac{\quad}{\cdot(\quad)} \tag{3}$$

3) Gain: The open loop voltage gain from terminal Y to Z is very high and it is given by,

$$A = \frac{\quad}{\quad} = \frac{(\quad)}{\quad} \tag{4}$$

4) Bandwidth: The pole at terminal Z acts like the dominant low frequency pole due the large impedance at Z and assuming the bandwidth of the input buffer is high, then the bandwidth is given by,

$$f = \frac{\quad}{\quad} \tag{5}$$

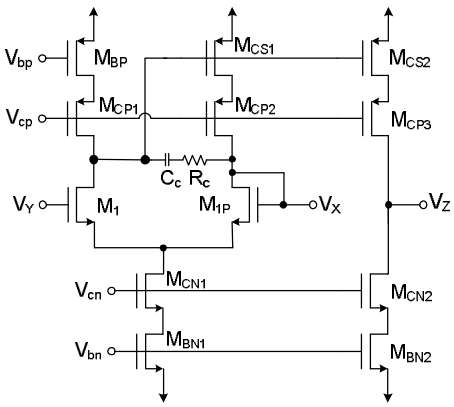

Fig. 3 Second Generation Current Conveyor

where C_Z is the capacitance at the node Z.

5) Slew Rate: The CCII has a class-A topology and therefore exhibits slew-rate limitation in negative direction. The negative slew rate is given by,

$$SR = \frac{\quad}{\quad} \tag{6}$$

where I_B is the bias current and C_L is the load capacitance. It is possible to modify the DFVF and output stage for class AB operation of the current conveyor of Fig. 3 using quasi floating gate techniques as reported in [4] and [8].

6) Input/output Range: The input voltage swing is given by,

$$V \quad = V \quad - 2V \quad + V \tag{7}$$

$$V \quad = V \quad + 3V \quad + V \tag{8}$$

The output voltage swing is given by,

$$V \quad = V \quad - 2V \tag{9}$$

$$V \quad = V \quad + 3V \quad + V \tag{10}$$

III. Application: Programmable Gain Voltage Amplifier

Fig. 4 shows the implementation of a constant bandwidth programmable gain voltage amplifier based on a CCII in feed forward approach. It consists of a resistor R_1 connected at the low impedance terminal X and a resistor R_2 connected at the high impedance terminal Z. The main advantage of this circuit is that if the gain is varied with R_1 by keeping R_2 constant, then gain and bandwidth of the resulting amplifier are independent of each other because of the absence of feedback.

A. Gain:

The voltage gain at DC of the amplifier is given by,

$$A = \frac{\quad}{\quad} = \frac{\quad}{\quad} \tag{11}$$

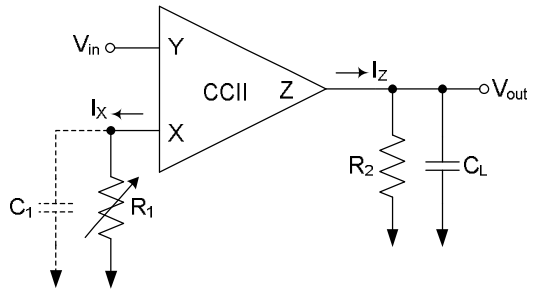

Fig. 4 Programmable Gain Voltage Amplifier using CCII

The input V_{in} can also be applied to R_1 with terminal Y grounded which results in an inverting amplifier whose gain is $-R_2/R_1$. This does not require common mode input signal swing at terminals X and Y.

B. Bandwidth:

If the bandwidth of the input buffer is high, then the bandwidth of the voltage amplifier is determined by the pole at the output node Z and given by,

$$f = \frac{}{(\ \|\ )} \cong \frac{}{} \qquad (12)$$

From the above equation, it can be seen that the bandwidth depends on the load resistance R_2 and thus, constant bandwidth can be obtained for different voltage gains by keeping R_2 constant and varying R_1. Therefore, the CCII circuit shows no gain-bandwidth trade-off.

A well known technique to enhance bandwidth consists of introducing a zero that cancels the output pole. This can be done easily in the circuit of Fig. 4 by connecting a capacitor with value $C_1 = C_L/A$ in parallel with R_1 [7].

IV. Simulation and Experimental Results

To validate the proposed new CMOS CCII design, the circuits in Fig. 2(a), 2(b) and 3 were designed and fabricated in AMI 0.5µm CMOS technology provided by MOSIS. The micrographic view of the fabricated test chip prototype is shown in Fig. 5.

A. Design Parameters

The circuits were designed for supply voltages $V_{DD} = 2.5$ V, $V_{SS} = -2.5$ V, bias current $I_B = 100$ µA and a load capacitance $C_L = 130$ pF (breadboard, scope and probes) at node Z. The transistor sizes (in micrometers), NMOS: $(W/L)_n = 50/1.2$, PMOS: $(W/L)_p = 100/1.2$, were designed for $V_{GS}-V_{thn} \sim 0.2$V in order to obtain high input/output voltage swing. The voltage applied to NMOS and PMOS transistor cascodes are $V_{cn} = -1.1$ V and $V_{cp} = 0.9$ V respectively. The value of the compensation capacitor used is $C_C = 7$ pF and the compensation resistor is $R_C = 4$ kΩ.

B. DFVF and CVF Output Impedance R_X

The simulated output impedance R_X of DFVF and CVF obtained by applying a 1A AC current source to the output terminal with input terminal grounded is shown in Fig. 6. The

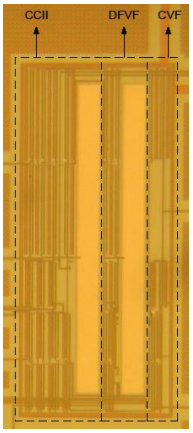

Fig. 5 Micrographic view of the fabricated chip

output voltage in this case directly corresponds to the output impedance. It can be seen that the DFVF provides very small output impedance of 14.54 Ω compared to the CVF whose output impedance is 1.08 kΩ. Experimentally, the output impedance was measured by placing a load resistance R_L at the output. The output voltages with the load (V_L) and without the load (V) are measured and the output impedance is calculated using the voltage divider equation given by $R_{out} = (V/V_L - 1)R_L$. The experimental results obtained are shown in Fig. 7. As expected, the output impedance of DFVF is 31.52 Ω while that of CVF is 1.15 kΩ.

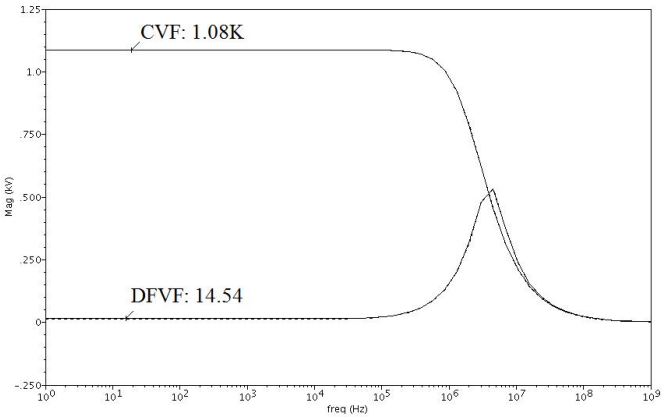

Fig. 6 Simulated output impedance R_X of DFVF and CVF

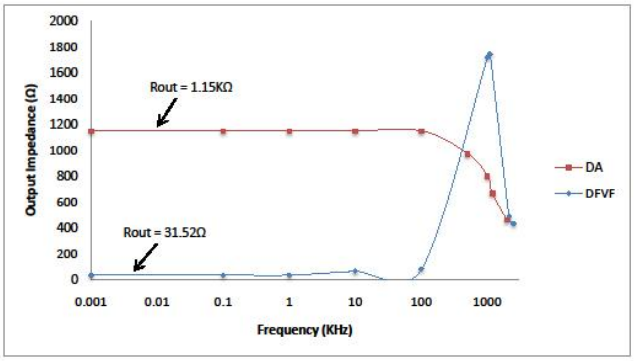

Fig. 7 Experimental output impedance of R_X of DFVF and CVF

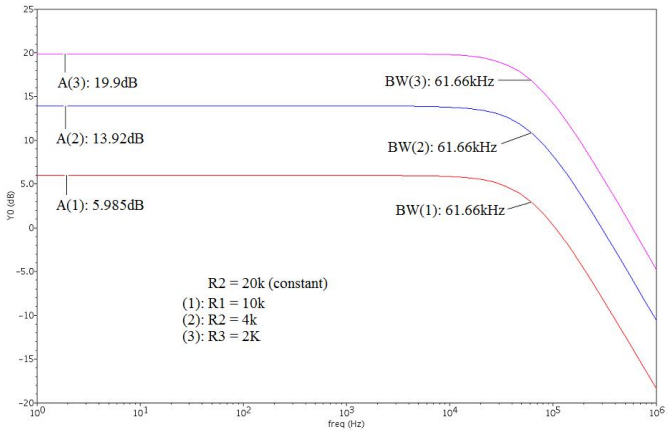

Fig. 8 Simulated AC response of CCII in inverting configuration

C. *AC Response of CCII as Programmable Gain Voltage Amplifier*

The simulated AC response of the voltage amplifier (Fig. 4) in inverting configuration with R_2 (20 kΩ) constant and for R_1 taking values of 10 kΩ, 4 kΩ and 2 kΩ is shown in Fig. 8. It can be seen that the gain varies with R_1 and the bandwidth, 61.66 kHz, remains constant independent of the gain. The AC response obtained experimentally is shown in Fig. 9. As expected, a constant bandwidth of 60 kHz is observed for all the three cases.

V. Conclusions

A new high performance CMOS CCII, built using DFVF as its input buffer stage, was introduced. It is characterized by very low input impedance and high output impedance. It provided gain independent constant bandwidth when used to implement a programmable gain voltage amplifier. Simulation and experimental results from a test chip prototype are provided to validate the design characteristics.

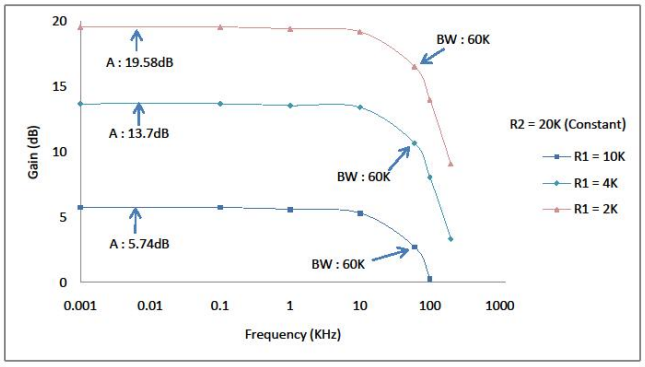

Fig. 9 Experimental AC response of CCII in inverting configuration

References

[1] C. Toumazou, F. J. Lidgey, and D. Haigh, *Analgue IC Design: The Current-Mode Approach*, Peter Peregrinus, 1990.

[2] A. J. Lopez-Martin, J. Ramirez-Angulo, and R. G. Carvajal, "Low-Voltage Low-Power Wideband CMOS Current Conveyors based on the Flipped Voltage Follower," *Proc. ISCAS*, vol. 1, pp. I-801–I-804, May 2003.

[3] G. Di Cataldo, A. D. Grasso, and S. Pennisi, "Two CMOS Current Feedback Operational Amplifiers," *IEEE Trans. on Circuits and Systems–II*, vol. 54, no. 11, pp. 944–948, Nov. 2007.

[4] J. Ramirez-Angulo, S. Gupta, A. J. Lopez-Martin, and R. G. Carvajal, "New Improved CMOS Class AB Buffers based on Differential Flipped Voltage Follower," *Proc. ISCAS*, pp. 3914–3917, May 2006.

[5] G. Palmisano, G. Palumbo, and S. Pennisi, "High-Performance and Simple CMOS Unity-Gain Amplifier," *IEEE Trans. on Circuits and Systems–I*, vol. 47, no. 3, pp. 406–410, Mar. 2000.

[6] B. J. Maundy, A. R. Sarkar, and S. J. Gift, "New Design Topology for Low-Voltage CMOS Current Feedback Amplifiers," *IEEE Trans. on Circuits and Systems–II*, vol. 53, no. 1, pp. 34–38, Jan. 2006.

[7] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed., Cambridge, 2006, pp. 276–278.

[8] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. Lopez-Martin, "A Free But Efficient Low-Voltage Class-AB Two-Stage Operational Amplifier," *IEEE Trans. on Circuits and Systems–II*, vol. 53, no. 7, pp. 568-571, July 2006.