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Accurate Dynamic-Feedback CMOS Cross-Quad suitable for Low-Voltage operation

Belen Calvo
Group of Electronic Design (I3A)
University of Zaragoza
50009 Zaragoza, Spain
becalvo@unizar.es

Jaime Ramirez-Angulo
Klipsch School of Electrical and Computer Engineering
New Mexico State University
Las Cruces, NM 88003-0001, USA
jramirez@nmsu.edu

Antonio Lopez-Martin
Dpto. Ing. Eléctrica y Electrónica
Univ. Pública de Navarra
31006 Pamplona, Spain
antonio.lopez@unavarra.es

Ramon G. Carvajal
Escuela Superior de Ingenieros
University of Seville
41092 Sevilla, Spain
carvajal@gte.esi.us.es

Abstract— **This paper presents the implementation of a cross-quad circuit suitable for low-voltage operation. The proposed cell exploits a dynamic positive feedback g_m boosting technique to achieve linear voltage-to-current conversion, while it manages to work with low-voltage with no extra bias current and minimal additional hardware. Results for a 0.5 µm CMOS implementation supplied at 3 V show a 0.972 % voltage-to-current accuracy, improving the 0.867 % accuracy of a previously reported cross-quad topology also suitable for low-voltage operation which is based on folded transistors.**

Keywords: cross-quad, linear V-I converter, low-voltage CMOS design, dynamic positive feedback

I. INTRODUCTION

CMOS voltage-to-current converters are key building blocks in many analog and mixed signal processing systems, such as continuous-time filters, variable gain amplifiers, data converters and other interface circuits.

One of the most widely used CMOS V-I converter is the source degenerated differential pair, shown in Fig. 1. Although it posses several appealing properties, the effect of the finite input pair transistors small signal transconductance g_m involves a trade-off between linearity and power efficiency that restricts the operating range showing a linear V-I relationship inversely proportional to the source degeneration resistance [1]. To obtain high linearity without increasing the power consumption, one simple technique is based on the boost of the transconductance g_m by means of positive feedback. The straightforward topology exploiting this approach is the well known cross-quad cell [2], shown in Fig. 2(a). This structure, however, has a main drawback that makes it unsuitable for present day applications: since the feedback path consists of stacked devices, it requires a noteworthy power supply voltage that can be larger than the maximum supply available in a modern CMOS process (typically $V_{DDmax}<3V_{TH}$).

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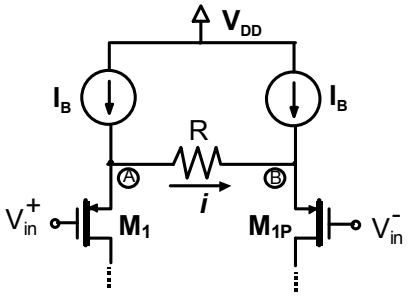

Figure 1. Conventional source degenerated pair

This paper presents a cross-quad implementation which, thanks to the use of dynamic feedback, achieves low-voltage operation while keeping a linear V-I relationship, without the need of increasing the total bias current. Section II reviews the conventional cross-quad cell and a previous low-voltage cross-quad implementation, the folded-cross-quad, highlighting its advantages and drawbacks, and the new approach is described. Section III summarizes the obtained simulation results comparing the different topologies, implemented in a 0.5 µm CMOS process. Some preliminary conclusions are finally presented in Section IV.

II. CROSS-QUAD

In this Section we discuss the conventional cross-quad circuit, an existing low-voltage folded version of the cross-quad and finally, the proposed low-voltage solution. In the following analysis we assume that the technology is P-substrate, as this will be our integrating technology.

A. Classical Cross-Quad

Fig. 2(a) shows the conventional MOS cross-quad [2]. In this circuit, positive feedback is used to compensate for

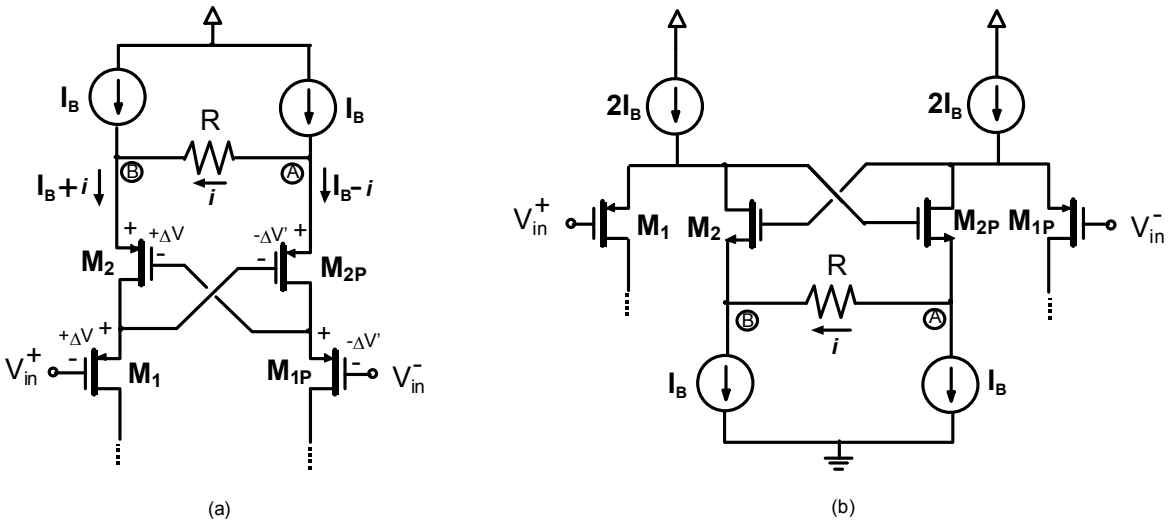

Figure 2. (a) Conventional cross-quad and (b) folded cross-quad

nonlinear variations in the gate source voltage of M_1, M_{1P}, M_2, M_{2P} so that the differential voltage (V_A–V_B) through the degeneration resistor R follows accurately the differential input voltage (V_{in}^+–V_{in}^-), independently of R.

This circuit, as well as other differential followers using positive feedback (e.g. [3]-[8]), operate on the principle that load current variations *i* lead to unequal positive and negative gate-source voltage changes (ΔV) in transistors M_1–M_2, and (–ΔV') in transistors M_{1P}–M_{2P}, respectively (see Fig. 2(a)). The cross connection from the source of M_1 to the gate of M_{2P} (and from the source of M_{1P} to the gate of M_2) implements a positive feedback path which leads to a cancellation of these variations in the differential voltage (V_A–V_B): the individual voltages V_A and V_B are given by $V_A = V_{in}^+ + 2V_{GS}^Q + \Delta V - \Delta V'$ and $V_B = V_{in}^- + 2V_{GS}^Q + \Delta V - \Delta V'$, where V_{GS}^Q is the quiescent gate source voltage of all transistors. If no body effect is present, as occurs considering the PMOS cross-quad version of Fig. 2(a) for our integrating P-substrate technology, then (V_A–V_B) = (V_{in}^+–V_{in}^-), thus resulting in an accurate transference of the differential input voltage V_{in} to the terminals of resistor R.

Therefore, ideally the cross-quad cell completely neutralizes the effect of the finite g_m of the input pair transistors through the use of positive feedback, providing an accurate linear voltage-to-current conversion inversely proportional to the degeneration resistance

$$g_{meff} = \frac{i}{v_{in}} = \frac{1}{R} \tag{1}$$

However, as mentioned in the introduction, this structure does not meet the nowadays low voltage requirement demanded in modern CMOS processes. As a result, the use of this simple and effective structure is restricted in present mixed signal applications.

B. Folded Cross-Quad

Fig. 2(b) shows a low-voltage version of the cross-quad in Fig. 2(a) obtained by folding transistors M_2–M_{2P} [8]. In this case, it is also achieved a g_m neutralization in the V–I conversion by imposing as a design condition that the transconductance of the input PMOS transistors M_1–M_{1P} equals that of the folded NMOS transistors M_2–M_{2P}. The resulting voltage-to-current conversion is given by the following expression

$$g_{meff} = \frac{i}{v_{in}} = \frac{1}{R + (2/g_{mb})} \tag{2}$$

where g_{mb} is the small signal body transconductance of the folded NMOS transistors.

However, the inherent mismatching derived from the use of complementary transistors, as well as the remaining body effect in one of the transistor types in single well CMOS technology, degrade the linearity performance of the voltage-to-current conversion. In addition, although this folded topology enables a significant reduction of the required power supply, note that the use of this cell also implies to double the total current consumption with respect to the conventional cross-quad which has only two branches.

C. Proposed Low-Voltage Cross-Quad

The proposed cross-quad version suitable for low-voltage operation is shown in Fig. 3(a). It consists, as in the conventional cross-quad, of stacked PMOS transistors, in order to eliminate the body effect from the V-I response. However, the cross connection from the source of M_1 to the gate of M_{2P} (and from the source of M_{1P} to the gate of M_2) implementing the positive feedback path to achieve g_m cancellation is now performed by using a Quasi Floating Gate (QFG) scheme.

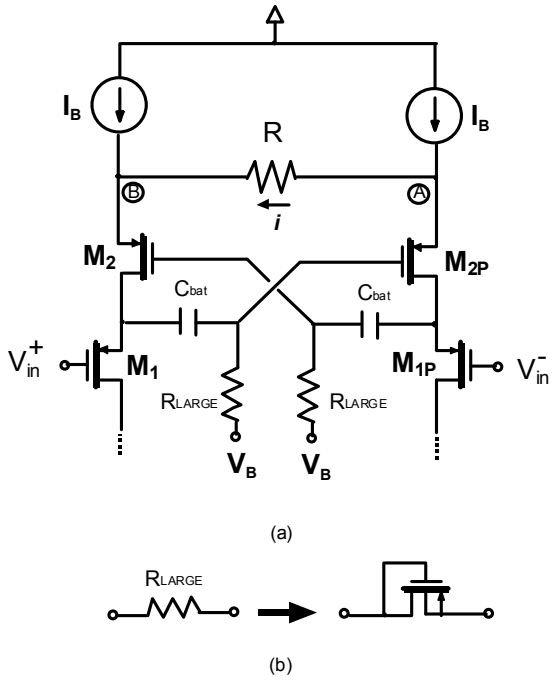

Figure 3. (a) Proposed low-volatge cross-quad based on a QFG dynamic feedback scheme and (b) Implementation of R_{LARGE}

The QFG technique was introduced in [9]. It uses MOS transistors weakly connected to a DC biasing voltage by means of a large resistive element R_{LARGE}, which can be realized using a reverse biased PN junction, a diode connected transistor or a transistor working in subthreshold region. This allows accurately set the quiescent operating point at the gate of the QFG transistor, which performs as a floating gate from the dynamic point of view. One of its applications is the compact implementation of class AB circuits with essentially enhanced slew rate, accurate control of the quiescent current, zero extra static power dissipation and the same supply requirements as their class A counterparts [10]-[11].

In the QFG cross-quad of Fig. 3(a), the gates of transistors M_2–M_{2P} are connected to: (i) a DC biasing voltage V_B through large resistive elements R_{LARGE}, which are implemented using minimum size PMOS diode–connected transistors as shown in Fig. 3(b); and (ii) to the sources of M_1–M_{1P} through small valued capacitors C_{bat} (~pF). In this way, under quiescent conditions the voltage at the gates of M_2–M_{2P} takes a value V_B, which is selected to have a value lower than that taken in the conventional cross-quad circuit, i.e. the quiescent gate source voltage of the input transistors $V_{GS}{}^Q$, while simultaneously keeping M_2–M_{2P} properly biased in saturation with the same $V_{GS}{}^Q$ as M_1–M_{1P}. Therefore, the supply requirements of the circuit can be reduced, allowing low-voltage operation.

Meanwhile, under dynamic conditions, capacitors C_{bat} –given that they can not charge or discharge rapidly through R_{LARGE}– operate as floating batteries and transfer variations in the sources of M_1 and M_{1P} to the gates of M_2 and M_{2P} respectively. Therefore, a dynamic positive feedback path is established, thus achieving as in the case of the conventional cross-quad a g_m neutralization which keeps a linear voltage to current conversion $(i/v_{in}) = (1/R)$, with the advantages that it manages to work with reduced power supply, no additional bias current and minimal additional circuitry. Note that this takes place for signal frequencies higher than $f_o=1/[2\pi R_{LARGE}C_{bat}]$; in practice, with typical values of R_{LARGE} in the range of 100 GΩ, $f_o < 1$ Hz.

III. Simulation Results

To validate the proposed low-voltage cross-quad and compare its performance to the characteristics of the conventional and folded topologies, this three structures have been designed in a 0.5 µm P-substrate (Nwell) CMOS technology, with input PMOS transistors ($V_{TH,PMOS}$= −0.95 V) to eliminate body effect (M_1, M_{1P}, M_2, M_{2P} had their source and substrate terminals connected), and simulated using Spectre with a level 53 transistor model.

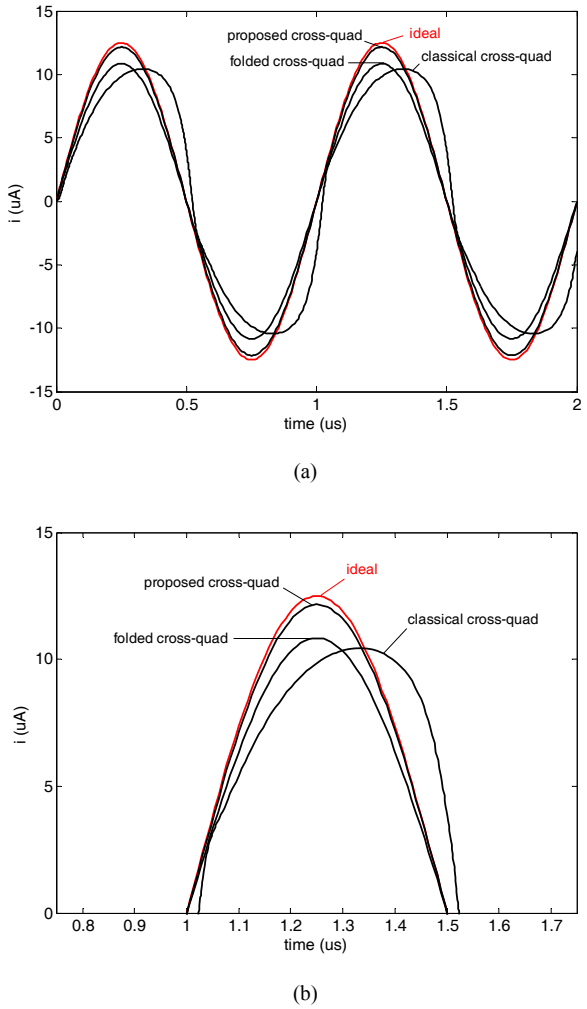

Figure 4. Output current *i* transient response for the classical cross-quad, the folded cross-quad and the proposed low-voltage cross-quad compared to the ideal case, input signal: 1 MHz, 0.5 $V_{p\text{-}p,diff}$ and (b) detailed view

TABLE I. COMPARISON OF CROSS-QUAD (CQ) PERFORMANCES
I_B=50 µA, R=20 KΩ, R_L=20 KΩ, C_L=0.25 pF

Parameter	Fig. 2a – Cross-quad	Fig. 2a – Folded CQ	Fig. 3a – Proposed cell
Technology	0.5 µm CMOS	0.5 µm CMOS	0.5 µm CMOS
Supply voltage	3.0 V	3.0 V	3.0 V
Total current consumption	100 µA	200 µA	100 µA
V-I conversion accuracy	-	0.867 %	0.972 %
Bandwidth	-	46.3 MHz	45.4 MHz
Dynamic range @ THD=-60 dB, 1 MHz	-	56 dB	57 dB

According to the notation of Fig. 2(a), 2(b) and 3(a) we have selected for all circuits a single supply V_{supply} = 3 V, a bias current I_B=50 µA, a source degeneration linear resistance R=20 kΩ and pair transistor sizes $(W/L)_P$=(120/1) and $(W/L)_N$=(50/1) in (µm/µm). Output current nodes were loaded with R_L=20 kΩ, in order to keep the common mode voltage V_{CMin}=V_{CMout}=1 V constant, and C_L=0.25 pF, value that emulates the input capacitance of a V-I converter also based on the cross-quad configuration.

Figure 4 shows the transient response of the current output signal *i* for the ideal case *i*=(V_{in}/R) compared to the obtained waveform for the conventional cross-quad, the folded cross-quad and the proposed low-voltage cross-quad of Figs. 2(a), 2(b) and 3(a) when applying a 1 MHz sinusoidal input signal with 0.5 $V_{p\text{-}p,diff}$. As it can be seen in this figure, the proposed cross-quad structure overcomes the limitations that noticeably reveal the classical cross-quad under low voltage operation, while it exhibits a 0.972 % accuracy in the V-I conversion, figure essentially better than the 0.867 % accuracy shown by the low-voltage cross-quad based on folded transistors and with the advantage that no additional current consumption is required.

Finally, the main characteristics of the three implemented cross quad topologies are summarized in Table I. Therefore, for low-voltage power supply, the new circuit presents very competitive performances in terms of accuracy, bandwidth and dynamic range, improving the features of the previous low-voltage cross-quad using folded transistors.

Thus, it can be a preferential choice for applications requiring high precision, such as instrumentation amplifiers where utilization of a load resistance R_L implemented with the same layer as R results in an accurate gain Av=R_L/R. Digitally programmable accurate gain tuning can be achieved by diverting the output current *i* to the load resistor through current mirrors with digitally programmable gain k. Note that also the linear degeneration resistor (and R_L) can be replaced by an array of programmable MOS resistors, so that tuning of the transconductance is possible for PGA and AGC amplifier applications.

IV. CONCLUSIONS

A new cross-quad version which overcomes the power supply constraint of the classical cross-quad has been presented. The solution makes use of a quasi floating gate scheme to implement a dynamic positive feedback g_m boosting technique, which keeps a linear voltage to current conversion and manages to work with low-voltage with no extra bias current and minimal additional hardware, while simultaneously presents a good trade-off between its main performance values. The proposed cell is thus an appealing choice in present-day mixed signal applications.

Additionally, the use of a positive feedback approach reduces the effect of the mobility degradation -usually modelled by a resistor in series with the source terminal- making suitable the implementation of the proposed structure in the modern deep submicron CMOS technologies.

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