

# Low-Voltage Tunable Pseudo-Differential Transconductor with High Linearity

Juan Antonio Gómez Galán, Manuel Pedro Carrasco, Melita Pennisi, Antonio Lopez Martin, Ramon González Carvajal, and Jaime Ramírez-Angulo

**A novel tunable transconductor is presented. Input transistors operate in the triode region to achieve programmable voltage-to-current conversion. These transistors are kept in the triode region by a novel negative feedback loop which features simplicity, low voltage requirements, and high output resistance. A linearity analysis is carried out which demonstrates how the proposed transconductance tuning scheme leads to high linearity in a wide transconductance range. Measurement results for a 0.5  $\mu\text{m}$  CMOS implementation of the transconductor show a transconductance tuning range of more than a decade (15  $\mu\text{A/V}$  to 165  $\mu\text{A/V}$ ) and a total harmonic distortion of  $-67$  dB at 1 MHz for an input of 1  $V_{pp}$  and a supply voltage of 1.8 V.**

**Keywords:** Analog CMOS circuit, linear resistor, operational transconductance amplifier (OTA), low-power and low-voltage circuit.

## I. Introduction

The design of transconductors is a challenging task in emerging applications which demand high linearity and high dynamic range. Both requirements are difficult to achieve since the designer must preserve or even increase the circuit performance at reduced supply voltages, facing increased nonidealities of small geometry devices and the low power dissipation which is mandatory in modern designs, especially in wireless transceivers. The transconductor is a basic building block of many analog circuits. Due to process tolerances, some degree of programmability is required to control the main parameters of filters, variable gain amplifiers, or voltage-controlled oscillators.

Several studies have addressed the design of low-distortion transconductors, applying different techniques that linearize the voltage-to-current (V-I) conversion in the input stage. These methods mainly include source degeneration, signal attenuation, adaptive biasing, and cross-coupling [1]-[7]. The conventional source degeneration using passive resistors or MOS transistors is the preferred operational transconductance amplifier (OTA) linearization technique. The use of passive resistors precludes continuous tuning, while the use of MOS transistors precludes programmability of transconductance in a wide range. Besides these techniques, new OTA topologies and operation modes, such as weak and moderate inversion, have been exploited [8], [9]. Transconductors using active resistors based on transistors operating in the triode region is a straightforward way to achieve a programmable linear V-I conversion. However, these circuits are typically not well suited to operate in low-voltage environments. We propose a novel and simple scheme to adjust the transconductance. It increases the output resistance and ensures linearity in a wide

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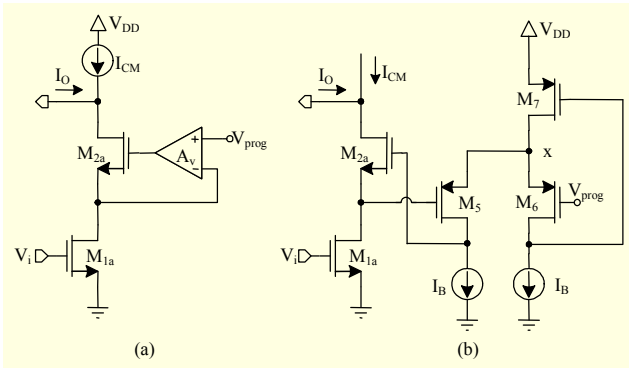


Fig. 1. (a) Conventional regulated-cascode triode structure and (b) proposed implementation.

range of transconductance tuning, requiring a low supply voltage for this kind of transconductor. The principle of operation of the circuit and the proposed control scheme is described in section II. Section III presents simulated and measured performance for a 0.5  $\mu\text{m}$  CMOS implementation. Some conclusions are given in section IV. Finally, an appendix describes in detail the programmability-dependent harmonic distortion degradation.

## II. Proposed Transconductor

### 1. Principle of Operation

Figure 1(a) illustrates the known regulated cascode technique to maintain constant the drain-source voltage of a triode transistor by using a feedback loop formed by a gain stage. This gain stage has been implemented in various ways [10], [11]. Figure 1(b) shows the proposed implementation of the scheme of Fig. 1(a) used in our transconductor. Linear V-I conversion is achieved by applying the input voltage to the gate of the triode-operated transistor  $M_{1a}$ , and the remaining transistors are in saturation. The input transistor is kept in the triode region by means of a regulated cascode topology whose feedback loop is made by a flipped voltage follower (FVF) [12] formed by transistors  $M_6$  and  $M_7$  and the right-hand side bias current  $I_B$ .

Transistors  $M_6$  and  $M_7$  implement a very low impedance node at the common source of  $M_5$  and  $M_6$  which sets the DC voltage at the drain of input transistor  $M_{1a}$  to a value equal to the tuning voltage  $V_{\text{prog}}$ . Voltage at node X can be considered constant due to the very low resistance at node X provided by the FVF, which is given by  $r_x = 1/(g_{m6}g_{m7}r_6)$ , where  $g_{m6}$  and  $g_{m7}$  are the small-signal transconductance gains of  $M_6$  and  $M_7$ , respectively; and  $r_6$  is the small-signal output resistance of  $M_6$ . This circuit solution based on the FVF scheme leads to a compact implementation.

The feedback loop formed by transistors  $M_5$  and  $M_{2a}$  boosts

the transconductor output impedance and maintains the output nodes isolated from the low impedance drain of the input transistor. The boosted output resistance at the drain of  $M_{2a}$  is approximately

$$r_{\text{out}} = (g_{m2} \cdot r_{o2} (A_v + 1) + 1) \cdot r_{o1} + r_{o2} \quad (1)$$

$$\cong g_{m2} \cdot g_{m5} \cdot r_{o1} \cdot r_{o2} \cdot r_{o5},$$

where  $A_v = g_{m5}r_{o5}$  is the small-signal voltage gain provided by the common-source transistor  $M_5$ . Note that the tuning voltage  $V_{\text{prog}}$  of the circuit can be set to near 0 V. This allows a large tuning range to be achieved while a low level of distortion in the output current is maintained for a given input voltage range.

The circuit of Fig. 1(a) contains two independent negative feedback loops. The first one is formed by the FVF ( $M_6$  and  $M_7$ ). It is a two-pole feedback loop, so proper design is required to enforce stability. The dominant pole corresponds to the high-impedance internal node (the drain of  $M_6$ ), and the non-dominant pole corresponds to node X. A stability analysis of the FVF is available in [12], which shows that if the capacitance at node X is not very large (as in this study) stability can be readily enforced by choosing proper dimensions for transistors  $M_6$  and  $M_7$ . The situation is similar for the feedback loop formed by  $M_5$  and  $M_{2a}$ . It is a two-pole feedback loop, where the dominant pole is set by the high-impedance node at the drain of  $M_5$ , and the non-dominant pole is set by the low-impedance node at the source of  $M_{2a}$ . Again, choosing proper dimensions for  $M_{2a}$  and  $M_5$  can enforce stability.

The complete scheme for the proposed pseudo-differential transconductor is shown in Fig. 2. This figure includes the common-mode feedforward (CMFF) circuit required to set the common-mode current  $I_{\text{CM}}$  and a conventional common-mode feedback (CMFB) circuit to fix the common-mode output voltage. The active load formed by transistors  $M_{3a}$  and  $M_{4a}$  is a voltage-controlled current source which ensures high output impedance.

To enforce that  $M_1$  is kept in the triode region, the following condition must be satisfied for the entire input signal range:

$$V_{\text{prog}} < V_{i,\text{CM}} - \frac{V_{\text{id}}}{2} - V_{\text{TN}}, \quad (2)$$

where  $V_{i,\text{CM}}$  and  $V_{\text{id}}$  are the common-mode and differential input voltages, respectively, and  $V_{\text{TN}}$  is the threshold voltage of the NMOS transistor. It is necessary that  $M_5$  remains in the saturation region for the complete input range and the maximum value of  $V_{\text{prog}}$ . To fulfill that  $V_{\text{SD5}} > V_{\text{SG5}} - V_{\text{TP}}$ , the size of  $M_2$ ,  $M_5$  ( $M_6$ ), and the bias current  $I_B$  must be carefully adjusted. A DC level shifter placed between the gate of  $M_2$  and the drain of  $M_5$  could be used to increase the dynamic range and relax the design requirements (mainly, avoiding too large an aspect ratio for  $M_2$ ).

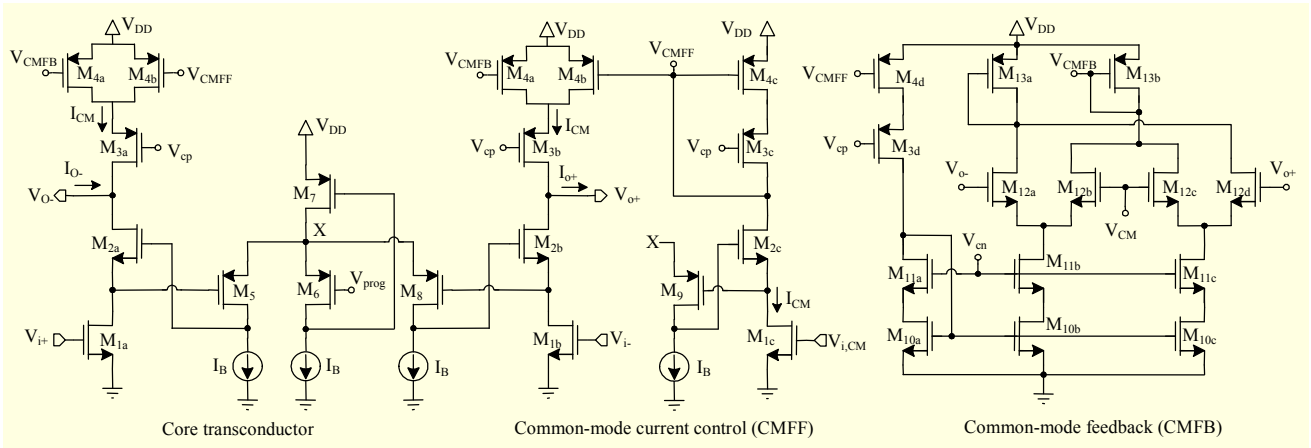


Fig. 2. Differential version of the proposed transconductor.

The tunability of the transconductor requires a feedforward circuit to control the input common-mode current [13]. A current proportional to the common-mode input signal  $V_{i,CM}$  and the control signal  $V_{prog}$  denoted as  $I_{CM}$  is generated and subtracted at the output nodes. This adaptive-bias circuit together with the CMFB circuit stabilizes the common-mode output voltage over the tuning range, which is mandatory for low voltage applications and high linearity levels. The combination of both CMFF and CMFB increases the CMRR of the proposed pseudo-differential topology. The practical cancellation of common-mode components requires good matching between transistors in the CMFF, CMFB, and the main transconductor, which can be achieved using conventional layout techniques.

An approximate expression for the large-signal drain current of the MOSFET input transistors operating in strong inversion and the ohmic region is given by

$$I_{D,1} = \beta_1 \left[ (V_{GS,1} - V_{TN}) \cdot V_{DS,1} - \frac{V_{DS,1}^2}{2} \right] \\ = \beta_1 \left[ (V_{GS,1} - V_{TN}) \cdot V_{prog} - \frac{V_{prog}^2}{2} \right], \quad (3)$$

where  $\beta_1 = \mu_n C_{ox} (W/L)_{M1}$  is the transconductance factor of transistor  $M_1$ ,  $V_{prog}$  is the control voltage, and  $V_{GS,1}$  is the input voltage  $V_i$  formed by the applied AC signal  $v_{in}$  superimposed on the common-mode voltage  $V_{i,CM}$ . The common-mode voltage-controlled current  $I_{CM}$  is expressed as

$$I_{CM} = \beta_1 \left[ (V_{i,CM} - V_{TN}) \cdot V_{prog} - \frac{V_{prog}^2}{2} \right]. \quad (4)$$

Then, the differential output current is

$$I_{out} = I_{D,1a} - I_{D,1b} = \beta_1 (V_{i+} - V_{i-}) \cdot V_{prog} = \beta_1 \cdot V_{id} \cdot V_{prog}, \quad (5)$$

and the linear dependence of the transconductance on  $V_{prog}$  is

$$G_m = I_{out} / V_{id} = \beta_1 \cdot V_{prog}. \quad (6)$$

This expression reveals an ideal dependence of the transconductance on  $V_{prog}$ .

According to the previous equations, the pseudo-differential transconductor achieves the ideal of perfect linearity. For a fixed  $V_{DS1} = V_{prog}$ , (3) shows that the current in a transistor biased in the triode region is linearly proportional to the gate-source voltage. For modern small geometry transistors, this ideal linearity is not achieved, mainly due to short-channel effects, such as mobility reduction, and because the expression of drain current versus gate-source voltage has nonlinear terms. To reduce this effect, large-channel input transistors have been used.

## 2. Distortion Analysis

Harmonic distortion in the output current of the transconductor is mainly due to the variation of the  $M_1$  drain-to-source voltage. Indeed, assuming that the input differential voltage (that is, the gate-to-source voltage) is a pure sinusoid, if the drain-to-source voltage remains constant and equal to  $V_{prog}$ , as in the ideal case, no distortion will arise at the output because  $M_1$  is a triode-operated transistor. Hence, an AC  $v_{ds1a}$  component superimposed on  $V_{prog}$  must be considered to evaluate harmonic distortion. Under this condition, the gate-to-source and drain-to-source voltages of  $M_1$  are given by  $V_{CM} + v_{i+}$  and  $V_{prog} + v_{ds1a}$ , respectively, thus leading to an AC component of the  $M_1$  drain current equal to

$$i_{d1a} = \beta_1 \left[ \left( V_{CM} - V_{TN} - V_{prog} + v_{i+} - \frac{1}{2} v_{ds1a} \right) v_{ds1a} + V_{prog} v_{i+} \right]. \quad (7)$$

Voltage  $v_{ds1a}$  (which is due to the second order effects as explained in the Appendix) may be expressed by the sum of various tones at frequency multiples of the fundamental. In particular, considering the high linearity of the overall

transconductor, harmonics higher than the third harmonic can be ignored because their levels are significantly lower than the first two harmonics. Moreover, in adopting a power series approach in the frequency domain for the nonlinear elements, it is always possible to express  $v_{ds1a}$  as a polynomial of the input voltage, through proper coefficients  $a_i$  [14], [15], such as

$$v_{ds1a} = a_1 V_{i+} e^{j\omega t} + a_2 V_{i+}^2 e^{j2\omega t} + a_3 V_{i+}^3 e^{j3\omega t}, \quad (8)$$

where  $V_{i+}$  is the amplitude of the input voltage. Substituting (8) into (7), disregarding all components at frequencies higher than  $3\omega$ , and evaluating the terms at frequency  $\omega$ ,  $2\omega$ , and  $3\omega$ , harmonic distortion factors  $HD_2$  and  $HD_3$  are obtained as follows:

$$HD_2 \cong \frac{1}{2} \frac{\left[ (V_{CM} - V_{TN} - V_{prog}) a_2 + \frac{1}{2} a_1 - \frac{1}{2} a_1^2 \right]}{\left[ (V_{CM} - V_{TN} - V_{prog}) a_1 + \frac{1}{2} V_{prog} \right]} V_{i+}, \quad (9a)$$

$$HD_3 \cong \frac{1}{4} \frac{\left[ (V_{CM} - V_{TN} - V_{prog}) a_3 + \frac{1}{2} a_2 - a_1 a_2 \right]}{\left[ (V_{CM} - V_{TN} - V_{prog}) a_1 + \frac{1}{2} V_{prog} \right]} V_{i+}^2, \quad (9b)$$

where coefficients  $a_i$  depend on biasing and transistors size. Their analytical expressions are derived in the appendix and shown in (A6)-(A8). The relationships given in (9) are useful since they allow evaluation of how biasing affects distortion, as is demonstrated in the next section, where simulated and experimental results are given.

### 3. Noise Analysis

Due to the relatively large transistor lengths employed and the high bandwidth of the transconductor, the contribution of thermal noise is dominant as compared to Flicker noise. The approximate expression for the thermal output current noise density can be written as

$$\frac{\overline{i_{N,out}^2}}{\Delta f} \approx \frac{16}{3} k_B T \left[ \frac{3}{2r_1} + g_{m4a} + g_{m4b} + \frac{1 + g_{mB}/g_{m5}}{g_{m5} r_1^2} \right], \quad (10)$$

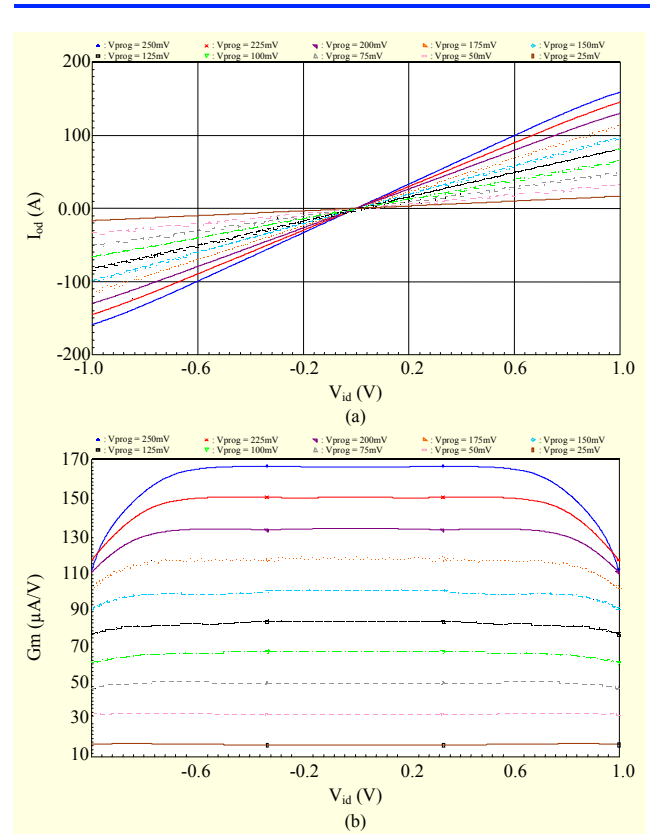
where  $k_B$  is the Boltzmann's constant,  $T$  is the absolute temperature,  $g_{mi}$  is the small-signal transconductance of transistor  $M_i$ ,  $g_{mB}$  is the transconductance of the current source  $I_B$  at the drain of  $M_5$ , and  $r_1$  is the resistance of the triode transistor  $M_1$ . Note that, for large  $r_1$ , the contribution of the current source  $M_4$  dominates the output noise current, but for low  $r_1$  output noise current is dominated by  $M_1$ ,  $M_5$ , and  $I_B$ .

## III. Simulation and Experimental Results

The transconductor shown in Fig. 2 was designed and

**Table 1.** Transistor dimensions of OTA (bias condition:  $V_{DD}=1.8$  V,  $I_B=10$   $\mu$ A,  $V_{CP}=0.6$  V,  $V_{cn}=1.1$  V,  $V_{i,CM}=1.3$ V).

Transistor	W ( $\mu$ m)	L ( $\mu$ m)
M <sub>1a</sub> , M <sub>1b</sub> , M <sub>1c</sub>	20	3
M <sub>2a</sub> , M <sub>2b</sub> , M <sub>2c</sub>	100	0.6
M <sub>3a</sub> , M <sub>3b</sub> , M <sub>3c</sub>	50	1.2
M <sub>3d</sub>	12.5	1.2
M <sub>4a</sub> , M <sub>4d</sub>	30	1.2
M <sub>4b</sub>	90	1.2
M <sub>4c</sub>	120	1.2
M <sub>5</sub> , M <sub>6</sub> , M <sub>8</sub> , M <sub>9</sub>	10	1.2
M <sub>7</sub>	30	1.2
M <sub>10a</sub> , M <sub>10b</sub> , M <sub>10c</sub>	10	1.2
M <sub>11a</sub> , M <sub>11b</sub> , M <sub>11c</sub>	7.5	0.6
M <sub>12a</sub> , M <sub>12b</sub> , M <sub>12c</sub> , M <sub>12d</sub>	5	0.6
M <sub>13a</sub> , M <sub>13b</sub>	30	1.2



**Fig. 3.** Programmability range for the proposed OTA: (a) differential output current and (b) transconductance.

fabricated in a 0.5  $\mu$ m CMOS technology. This non-silicided CMOS process has 3 metal layers, 2 poly layers, and a high resistance layer. The process is for 5 V applications, and the nominal threshold voltages for the PMOS and NMOS

transistors are  $V_{TP} = -0.96$  V and  $V_{TN} = 0.67$  V, respectively. The transconductor was tested with a single supply voltage of 1.8 V and a biasing current  $I_B$  of 10  $\mu$ A. The transistor dimensions and component values employed are shown in Table 1. The common-mode input (output) voltage  $V_{iCM}$  ( $V_{oCM}$ ) was set to 1.3 V.

The linear performance of a transconductor is given by the input voltage range for which the transconductance is constant. The simulated DC transfer characteristics are shown in Fig. 3. The differential output current for the tuning interval from  $V_{prog} = 25$  mV to 250 mV is shown in Fig. 3(a), and the corresponding transconductance ( $dI_o/dV_{id}$ ) is shown in Fig. 3(b) for values between 15  $\mu$ A/V and 165  $\mu$ A/V. Note the excellent linearity obtained in a large tuning range. This interval allows Gm-C filters based on this transconductor to operate in a wide frequency range.

For the nominal transconductance corresponding to  $V_{prog} = 125$  mV, the common-mode input current  $I_{CM} = 43$   $\mu$ A; therefore, the power consumption of the core transconductor together with the CMFF circuit is 170  $\mu$ A. The CMFB circuit adds an extra current of 30  $\mu$ A. Thus, the total quiescent power dissipation is approximately 360  $\mu$ W.

Figure 4 shows a microphotograph of the fabricated chip with 0.054 mm<sup>2</sup> of silicon area. Figure 5 shows the measured total harmonic distortion (THD) results for a differential input signal of 1 MHz and variable voltage amplitude. The transconductor was loaded with a load resistance  $R_L = 1/G_m$  to convert the output current into voltage. The bandwidth for the proposed transconductor is 22 MHz. Figure 6 shows the measured output spectrum for a 1 MHz input signal of peak-to-peak amplitude of 1 V, featuring -67 dB of THD for the nominal transconductance at  $V_{prog} = 125$  mV. Note that this result is in agreement with the theoretical analysis developed in subsection II.2.

In particular, due to the balanced structure of the transconductor, THD is mainly affected by the  $HD_3$ , expressed

by (9b) which is plotted in Fig. 7. Note also that there is a wide range for  $V_{prog}$  where the transconductor operates with very high linearity. However, for values of  $V_{prog}$  higher than 150 mV, distortion significantly increases.

The high-frequency performance of the transconductor was

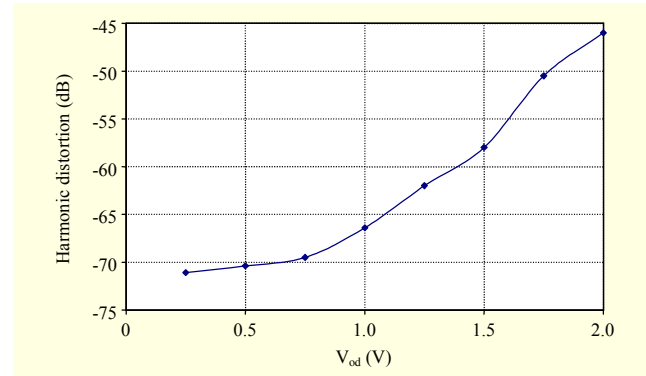


Fig. 5. Measured total harmonic distortion factors versus differential output voltage at 1 MHz.

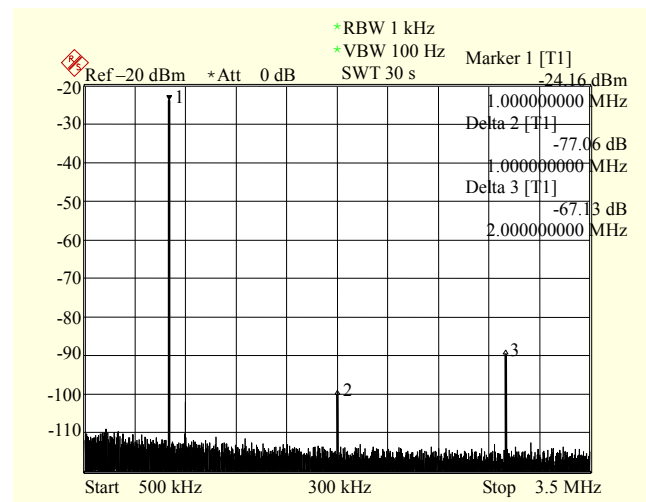


Fig. 6. Measured THD at 1 MHz, 1 V<sub>pp</sub> input (output) signal.

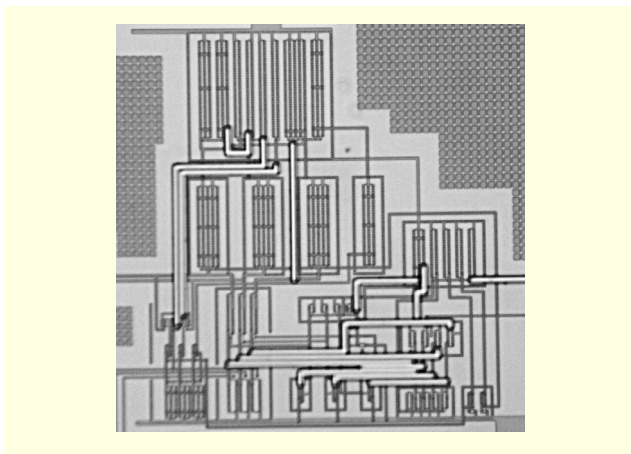


Fig. 4. OTA microphotograph.

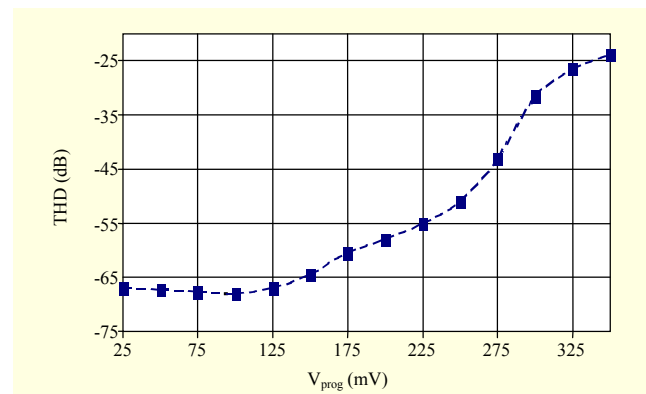


Fig. 7. Theoretical THD expressed by (9b) as function of  $V_{prog}$ .

evaluated by applying a two-tone input signal at 9.95 MHz and 10.05 MHz, respectively, with 1 V peak to peak for each input tone. The circuit maintains a moderate linearity with a measured IM3 of  $-55$  dB as shown in Fig. 8. Table 2 summarizes the main performance parameters of the transconductor, and Table 3 compares various OTA parameters of the proposed transconductor with those presented in recent works. Note that

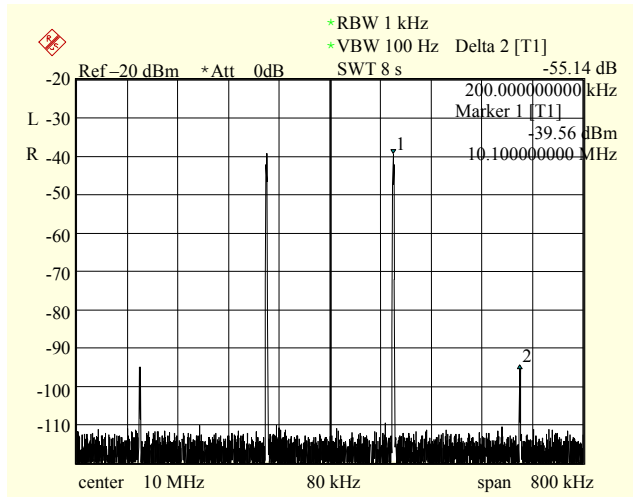


Fig. 8. Measured IM3 at 10 MHz, 1 V<sub>pp</sub> input signals.

Table 2. Nominal parameters for the proposed transconductor.

Parameter	Value
Technology	0.5 $\mu\text{m}$ CMOS
Threshold voltage	$V_{TP} = -0.96$ V, $V_{TN} = 0.67$ V
Supply voltage	1.8 V
G <sub>m</sub> range	15 – 165 $\mu\text{A/V}$
Bandwidth	22 MHz
THD @ 1 MHz, 1 V <sub>pp</sub>	$-67$ dB
IM3 @ 10 MHz, 1 V <sub>pp</sub>	$-55$ dB
Power consumption	360 $\mu\text{W}$
Silicon area	0.054 mm <sup>2</sup>

the results of our proposed transconductor are comparable to recent high linearity transconductors featuring a high input level/power supply ratio. The proposed transconductor can be used in continuous-time filters with high linearity requirements without increasing the complexity. This is due to the control branch shown in Fig. 2 which gives the common-mode current, which can be generated only once and is mirrored to all the transconductors. Furthermore, when various transconductors in the filter have common output nodes, they can share a CMFB circuit, which leads to more compact filter topologies.

## IV. Conclusion

A novel control scheme for a CMOS triode transconductor was presented. A theoretical distortion analysis demonstrated that linearity is preserved for a large transconductance range.

The circuit achieves high linearity with a compact topology. Experimental results confirmed the favorable features of the circuit. The transconductor achieved a THD of  $-67$  dB for a 1 MHz, 1 V<sub>pp</sub> input voltage at a 1.8 V supply voltage and only dissipated 360  $\mu\text{W}$ .

## Appendix

In this appendix, the expression of coefficients  $a_i$  appearing in the polynomial (8) is analytically derived. Let us consider the feedback structure between M<sub>1a</sub>, M<sub>2a</sub> and M<sub>5</sub> shown in Fig. 2. The drain current of M<sub>5</sub> in saturation is given by

$$i_{D5} = \frac{1}{2} \beta_5 \left( V_X - V_{\text{prog}} - v_{g5} - |V_{tp}| \right)^2 \left[ 1 + \lambda_5 (V_X - V_{D5} - v_{d5}) \right], \quad (\text{A1})$$

where the channel length modulation expressed by coefficient  $\lambda_5$  has been considered, and both the AC and DC voltage components have been included.

Since  $i_{D5}$  is always equal to  $I_B$ , which is a constant current, the AC components  $v_{d5}$  and  $v_{g5}$  appearing in (A1) (the source voltage at node X is kept constant by the FVF) must cancel

Table 3. Transconductor comparison of recent works.

Reference	CMOS technology	Power supply	Power consumption	G <sub>m</sub> range	HD3	IM3
[2]	0.35 $\mu\text{m}$	1.8 V	1.1 mW	630-1310 $\mu\text{A/V}$	$-58$ dB (0.3 V <sub>pp</sub> @ 10 MHz)	–
[5]	0.35 $\mu\text{m}$	3.3 V	6.6 mW	160-340 $\mu\text{A/V}$	–	$-70$ dB (1.4 V <sub>pp</sub> @ 26 MHz)
[9]	0.5 $\mu\text{m}$	3.3 V	1.25 mW	50-200 $\mu\text{A/V}$	$-83$ dB (1 V <sub>pp</sub> @ 1 MHz)	$-71$ dB (1 V <sub>pp</sub> @ 1 MHz)
This work	0.5 $\mu\text{m}$	1.8 V	0.36 mW	15-165 $\mu\text{A/V}$	$-67$ dB (1 V <sub>pp</sub> @ 1 MHz)	$-55$ dB (1 V <sub>pp</sub> @ 10 MHz)

each other out. Thus, by performing the calculations in (A1), deriving the AC component for the drain current of  $M_5$ , and setting it to zero, the relationship which  $v_{d5}$  and  $v_{g5}$  have to satisfy may be found. In particular, observing that  $v_{d5}=v_{g2a}$  and  $v_{g5}=v_{ds1a}$ , this relationship is

$$v_{g2a} \cong k \cdot v_{ds1a}, \quad (\text{A2})$$

where  $[-2/(V_X - V_{\text{prog}} - |V_{\text{tp}}|)] \cdot [(1 + \lambda_5 (V_X - V_{G2}) / \lambda_5)]$  depends on the biasing, and the approximation holds for  $v_{ds1a} \ll \sqrt{2I_B / \beta_5}$ . The AC component of the drain current of  $M_{1a}$  has been derived in the main text in (7), and its result is equal to

$$i_{d1a} = \beta_1 \left[ \left( V_{\text{CM}} - V_{\text{TN}} - V_{\text{prog}} + v_{i+} - \frac{1}{2} v_{ds1a} \right) v_{ds1a} + V_{\text{prog}} v_{i+} \right]. \quad (\text{A3})$$

However, it can be also obtained as the current of transistor  $M_{2a}$  in saturation by

$$i_{d1a} = \frac{1}{2} \beta_2 (v_{g2a} - v_{ds1a})^2 + \beta_2 (V_{G2a} - V_{\text{prog}} - V_{\text{TN}}) (v_{g2a} - v_{ds1a}). \quad (\text{A4})$$

Equating (A3) with (A4) and substituting (A2) for  $v_{g2a}$  in the resulting expression, a relationship containing only  $v_{ds1a}$  and  $v_{i+}$  is found:

$$\frac{1}{2} \left[ \beta_1 + \beta_2 (k-1)^2 \right] v_{ds1a}^2 - \beta_1 v_{ds1a} v_{i+} - \left[ \beta_1 (V_{\text{CM}} - V_{\text{TN}} - V_{\text{prog}}) - \beta_2 (V_{G2} - V_{\text{prog}} - V_{\text{TN}}) (k-1) \right] v_{ds1a} - \beta_1 V_{\text{prog}} v_{i+} = 0. \quad (\text{A5})$$

Finally, substituting (8) into (A5) and equating the terms with the same exponential, coefficients  $a_i$  are found, and the result is equal to

$$a_1 = - \frac{V_{\text{prog}}}{(V_{\text{CM}} - V_{\text{TN}} - V_{\text{prog}}) - \frac{\beta_2}{\beta_1} (V_{G2} - V_{\text{prog}} - V_{\text{TN}}) (k-1)}, \quad (\text{A6})$$

$$a_2 = - \frac{\left\{ 1 - \frac{1}{2} \left[ 1 + \frac{\beta_2}{\beta_1} (k-1)^2 \right] \cdot a_1 \right\} \cdot a_1}{(V_{\text{CM}} - V_{\text{TN}} - V_{\text{prog}}) - \frac{\beta_2}{\beta_1} (V_{G2} - V_{\text{prog}} - V_{\text{TN}}) (k-1)}, \quad (\text{A7})$$

$$a_3 = - \frac{\left\{ 1 - \left[ 1 + \frac{\beta_2}{\beta_1} (k-1)^2 \right] \cdot a_1 \right\} \cdot a_2}{(V_{\text{CM}} - V_{\text{TN}} - V_{\text{prog}}) - \frac{\beta_2}{\beta_1} (V_{G2} - V_{\text{prog}} - V_{\text{TN}}) (k-1)}. \quad (\text{A8})$$

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