A Comparison of the Performance and Stability of ZnO-TFTs With Silicon Dioxide and Nitride as Gate Insulators

R. B. M. Cross, Maria Merlyne De Souza, Steve C. Deane, and Nigel D. Young

***Abstract*—The performance and stability of thin-film transistors with zinc oxide as the channel layer are investigated using gate bias stress. It is found that the effective channel mobility, ON/OFF ratio, and subthreshold slope of the devices that incorporate SiN are superior to those with SiO_2 as the dielectric. The application of positive and negative stress results in the device transfer characteristics shifting in positive and negative directions, respectively. The devices also demonstrate a logarithmic time-dependent threshold voltage shift suggestive of charge trapping within the band gap and the band tails responsible for the deterioration of device parameters. It is postulated that this device instability is partly a consequence of the lattice mismatch at the channel/insulator interface. All stressed devices recover to near-original characteristics after a short period at room temperature without the need for any thermal or bias annealing.**

***Index Terms*—Charge trapping, stability, thin-film transistors (TFTs), zinc oxide (ZnO).**

I. Introduction

METAL–OXIDE–semiconductors have recently been subject to intense investigation for optoelectronic applications such as light-emitting diodes and display technologies, e.g., thin-film transistors (TFTs). Major benefits of these materials include the potential for simple low-cost deposition at temperatures compatible with polymer substrates, good stability in air, and high electron mobilities [1], [2]. There is also the possibility of exploiting the wideband gaps of these materials for transparent electronics.

A number of groups have developed TFTs based on multicomponent amorphous oxides such as indium gallium zinc oxide, zinc tin oxide, and zinc indium oxide [3], [4]. Some of these devices demonstrate field effect mobilities as high as 50 $\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$, which bear a favorable comparison to polycrystalline silicon devices and which could be useful for large liquid crystal displays (LCDs), where an increase in mobility would be of benefit when compared to a-Si:H ($\sim$1 $\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$). A similar material that has shown a great deal of promise is zinc oxide (ZnO) [5]–[7]. ZnO can be deposited over large areas and at relatively low temperatures, suggesting a good compatibility with flexible substrates. Although the potential advantages of transparent oxide TFTs are manifold, an issue that has yet to be extensively explored is that of stability. The stability of TFTs is fundamental to the performance and reliability of an application (e.g., an active-matrix LCD). A significant amount of work has been reported on the shift in the threshold voltage V_T of a-Si:H TFTs under bias stress, as correction circuitry is required for adjustment of threshold shifts [8], [9]. Recently, we have shown that ZnO-TFTs with a silicon dioxide gate insulator also suffer from shifts in the threshold voltage [10].

In this paper, we present results on the comparison of the performance of ZnO-TFTs with two different gate insulator materials, together with the effect of extended periods of bias stress on device characteristics.

II. Experiment

The characterization of the devices was performed on inverted-staggered structures, where a silicon wafer (doping concentration $\sim 10^{18}$ cm^{-3}) acted as both the gate contact and the substrate. The two insulating materials incorporated into the test structures were thermally grown silicon dioxide (SiO_2) (100 nm) and a double film stack of thermally grown SiO_2 (50 nm) and silicon nitride (SiN) (50 nm, $\varepsilon_r = 7.5$) deposited by low-pressure chemical vapor deposition (100 nm) and subsequently annealed at 1000 °C. The insulators were grown in a commercial foundry to ensure high quality. Hereafter, the different devices will have the nomenclature of oxide or nitride, respectively. Following this, 100 nm of ZnO was deposited at room temperature using radio-frequency (RF) magnetron sputtering. The sputter deposition took place in an argon atmosphere at a pressure of 3 mtorr using a ceramic ZnO target (99.9%, Kurt J. Lesker). The RF power density was 30 $\mathrm{mW} \cdot \mathrm{cm}^{-2}$, and the substrate–target distance was $\sim$7 cm. Indium tin oxide was then thermally evaporated to form the source–drain contacts. The channel length and width-to-length ratio of the completed devices were 250 μm and 20 : 1, respectively. The channel and source–drain contacts were patterned using shadow masks. All steps of the device manufacture were carried out without any intentional heating or postfabrication annealing.

The device characterization and stress measurements were carried out at room temperature in the dark using an Agilent Technologies B1500A semiconductor parameter analyzer. The

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R. B. M. Cross is with the Emerging Technologies Research Centre, De Montfort University, Leicester LE1 9BH, U.K.

M. M. De Souza is with the Department Electronic and Electrical Engineering, University of Sheffield, S10 2TN Sheffield, U.K. (e-mail: m.desouza@sheffield.ac.uk).

S. C. Deane and N. D. Young are with Philips Research Laboratories, RH1 5HA Surrey, U.K.

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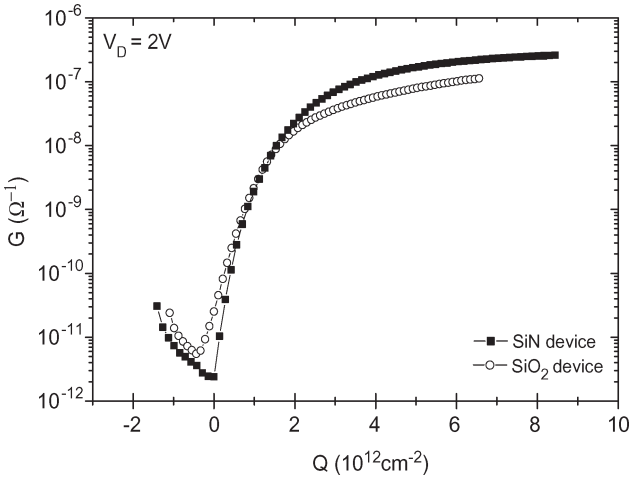

Fig. 1. Typical example of normalized gate transfer characteristics for a ZnO-TFT with SiN (solid squares) and SiO_2 (open circles) as the gate insulator materials.

stress voltages applied to the gate contact ranged from -30 to 80 V, and during the stressing period, the source–drain contacts were connected to ground. Stress was applied for various periods of time up to 10^4 s. To investigate how V_T changed over time, the stress was interrupted, and a transfer characteristic was taken before the reapplication of the stress bias.

Atomic force microscopy (AFM) measurements were performed using a PSIA XE-100 series scanning probe microscope at room temperature.

III. Results and Discussion

A. TFT Performance

Fig. 1 shows a comparison of the gate transfer characteristics of the TFTs incorporating the SiN and SiO_2 gate insulators. In this figure, the data have been normalized to the sheet conductance G (in reciprocal ohms per centimeter) versus the total induced charge density Q (in electrons per square centimeter). The induced charge density is proportional to the gate voltage, and the sheet conductance is proportional to the source–drain current, which is calculated as

$$Q = \left(\frac{V_G \varepsilon_{\rm ins}}{q d_{\rm ins}}\right) \tag{1}$$

$$G = \frac{I_{SD}}{V_{SD}\left(\frac{W}{L}\right)} \tag{2}$$

where V_G is the gate bias, $\varepsilon_{\rm ins}$ is the dielectric constant of the gate insulator material, $d_{\rm ins}$ is the gate insulator thickness, I_{SD} is the source–drain current, V_{SD} is the source–drain bias, and W/L is the width/length ratio of the ZnO-TFT channel. By normalizing the characteristics, the data from devices with different insulators can be directly compared.

In Fig. 1, it is evident that the subthreshold slope S of the nitride device, which is, in effect, a measure of the rate at which a device "turns on," is steeper than that of the oxide TFT. Indeed, the S values for these devices are 1.06 $\rm V \cdot dec^{-1}$ (2.98×10^{11} electrons $\cdot\ \rm cm^{-2} \cdot dec^{-1}$) and 2.08 $\rm V \cdot dec^{-1}$ (4.55×10^{11} electrons $\cdot\ \rm cm^{-2} \cdot dec^{-1}$), respectively. This indicates that there is an increased density of states in the upper part of the band gap for the oxide transistors, as compared to the nitride devices. The extrapolated threshold voltages (not shown) are comparable at $\sim$5 V (i.e., 1.09×10^{12} and 1.41×10^{12} electrons $\cdot\ \rm cm^{-2}$ for the oxide and nitride devices, respectively). However, the turn-on voltage $V_{\rm on}$ [1], i.e., the gate voltage at which the drain current begins to increase in a transfer characteristic, is marginally negative for the oxide transistors. Whereas these devices are both enhancement mode, as demonstrated by a positive V_T, this signifies that a negative gate voltage is required to deplete the oxide TFT channel layer of electrons and fully "turn off" the device. Additionally, the drain current ON/OFF ratio for the nitride devices is on the order of $\sim 1 \times 10^5$, whereas for the oxide transistors, the ON/OFF ratio is $\sim 2-3 \times 10^4$.

S can be related to the density of trap states $N_{\rm SS}$ at the semiconductor/insulator interface by the following relation, assuming the traps are isotropic [11]:

$$N_{\rm SS} = \left(\frac{\log(e) S}{kT/q} - 1\right) \frac{C_{\rm ins}}{q} \tag{3}$$

where k is Boltzmann's constant, T is the temperature (in this case, 298 K), q is the electron charge, and $C_{\rm ins}$ is the gate insulator capacitance (45 and 35 nF/$\rm cm^2$ for the SiN/SiO_2 stack and SiO_2, respectively). For these devices, indicative values of $N_{\rm SS}$ are $\sim 4.90 \times 10^{12}$ $\rm cm^{-2}$ for nitride transistors and $\sim 7.68 \times 10^{12}$ $\rm cm^{-2}$ for oxide TFTs. These are high values as compared to Si/SiO_2 (around 10^{10} $\rm cm^{-2}$), but could explain the performance parameters previously detailed.

The most important parameter of TFT performance is channel mobility. Effective channel mobilities $\mu_{\rm eff}$, as obtained from the linear region of the transfer characteristics for typical devices, are in the range between $\sim$0.2 and 0.7 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$ for nitride TFTs and between $\sim$0.1 and 0.25 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$ for oxide transistors. It is evident that these values are at the lower end of those reported in the literature for ZnO-TFTs ($\sim$0.2–25 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$) and suggest that given the reasonable subthreshold behavior and ON/OFF ratios, grain-boundary scattering at the interfacial region of the channel and insulator layers could be limiting the device performance.

Typical measured $I_D - V_D$ characteristics of the devices with two sets of insulators of identical channel lengths are shown in Fig. 2. Fig. 2 reveals saturation at high gate voltages and the absence of current crowding at low gate voltages, indicative of good ohmic contacts.

B. Device Stability

The effect of applying a gate bias stress of 30 V to the gate contact of a ZnO-TFT test structure, with SiN as the insulator, for 10^3 s is shown in Fig. 3 (top). There is a positive displacement of the transfer characteristics along the voltage axis. Also shown is a transfer characteristic taken 15 min after the stress bias has been removed. It is evident that the device regains its characteristics to near-original performance after the short period of relaxation. Similarly, when a bias of -30 V is applied to the gate, the characteristics shift in the

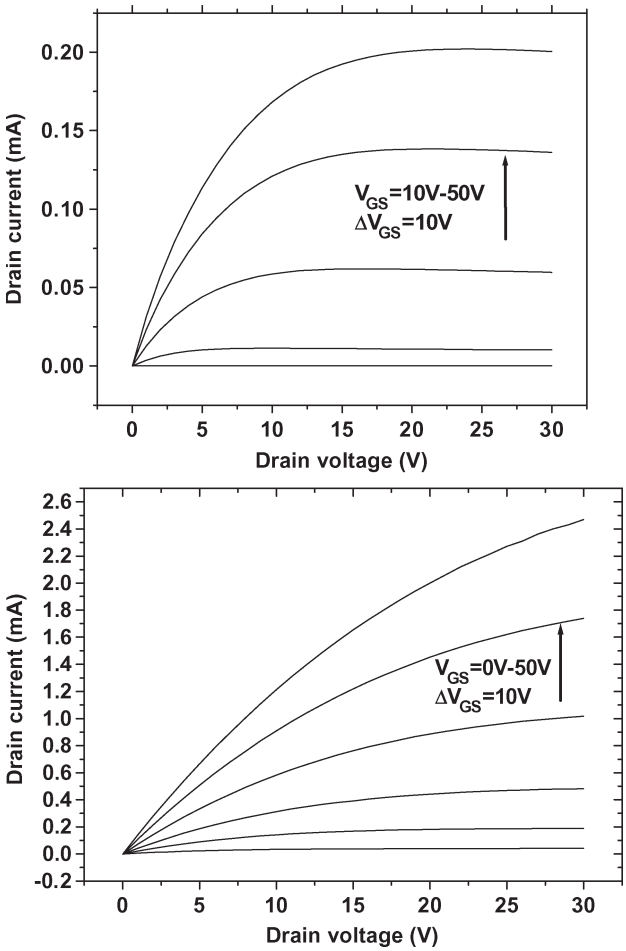

Fig. 2. $I_D - V_D$ characteristics of identical channel lengths ZnO-TFTs with SiN (top) and SiO_2 (bottom) as gate insulators. The insulators have different equivalent oxide thicknesses, as indicated in the text.

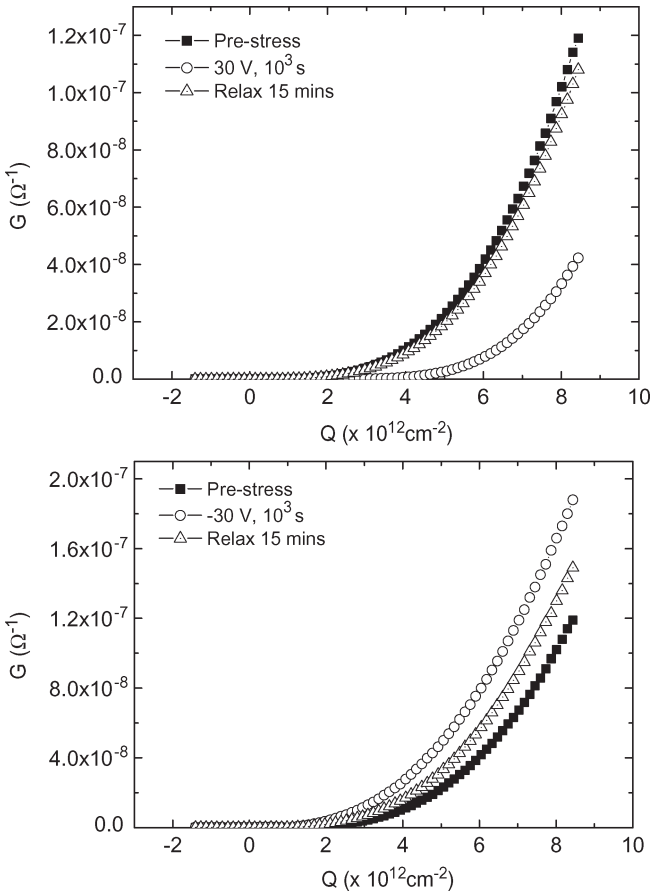

Fig. 3. Effect of positive bias stress (top) and negative bias stress (bottom) on the transfer characteristics of a ZnO-TFT with SiN as the gate insulator.

negative direction after 15 min of relaxation (Fig. 3, bottom). Under negative bias stress, device recovery to near-original characteristics takes several hours and is not shown here.

These characteristics indicate that during the periods of stress, depending on the polarity of the applied bias, electrons are temporarily trapped/detrapped in the gate insulator or semiconductor or at the channel/insulator interface at pre-existing traps. Upon the removal of stress, these carriers are then gradually released from the trap states, resulting in the as-fabricated characteristics again being obtained. We have previously demonstrated that similar qualitative behavior is evident when a SiO_2 layer acts as the gate insulator [10].

The threshold voltage shift for both sets of transistors has been studied under a range of different gate bias values. These results, which are converted to the total trapped charge, are shown in Fig. 4. It is evident that the shift in the threshold voltage is greater for each bias stress value for the oxide devices, as compared to the nitride transistors. This could suggest that the interface of the ZnO channel layer and the SiO_2 insulator has a higher concentration of trap states within the interfacial region than that of SiN, which, under stress, act as trapping centers for carriers during the stressing period. This would correlate with the estimated density of interface trap states extracted from the previously detailed subthreshold slope parameter.

Fig. 5 shows a comparison of the time dependence of the threshold voltage shift for the ZnO-TFT test structures. Both sets of devices demonstrate a logarithmic time-dependent threshold voltage shift rather than a power law relationship at different rates, indicative of charge trapping as a dominant cause of instability.

The shift in the nitride transistors after a stressing period of 10 s is greater than that of the oxide devices over the entire range of bias stress values. However, as the stressing time increases, the shift in the threshold voltage in the oxide TFTs becomes greater and increases more rapidly. This indicates that the trap states either existing at the interface before the stress period or created during stress are different in nature between the two sets of device structures.

A logarithmic time dependence has previously been ascribed to charge trapping instabilities in other TFT structures [8]. Once a charge has been trapped in an insulator or new defects have been created in a channel layer/interface, the energy needed to remove this charge or to anneal/passivate the defects can usually only be provided by thermal and/or bias annealing. The fact that both ZnO test structures nearly recover their original characteristics and behavior after a period of relaxation, without the need for any bias or thermal annealing, suggests that the device instability could result from fast interface states, with a short relaxation time even at room temperature. Some of the states could arise from the semiconductor, but the difference

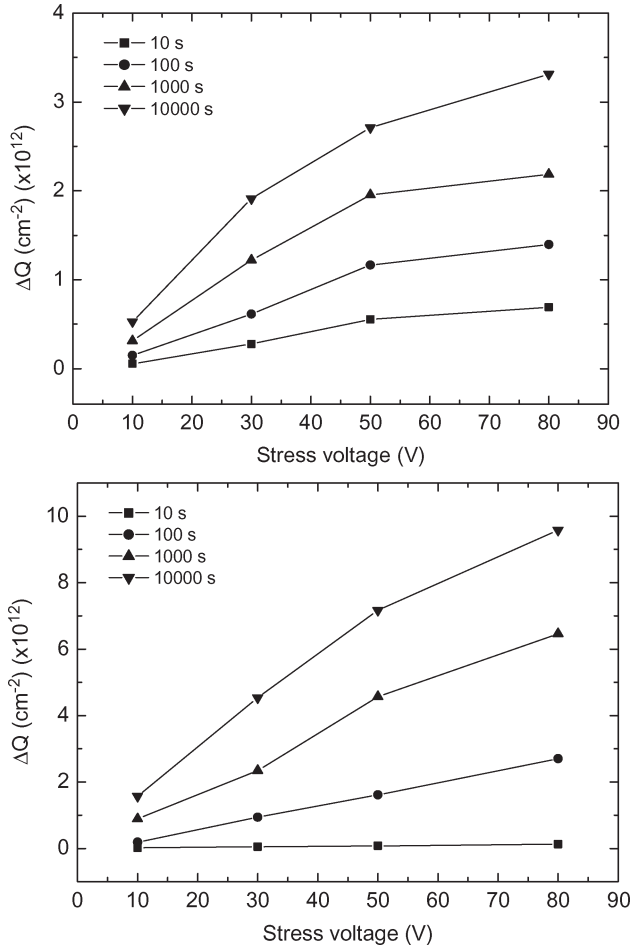

Fig. 4. Threshold voltage shift (converted to electrons per square centimeter) as a function of the bias stress voltage for a range of stress times from 10 s to 10 000 s for ZnO-TFTs with SiN as the gate insulator (top) and SiO_2 as the gate dielectric (bottom).

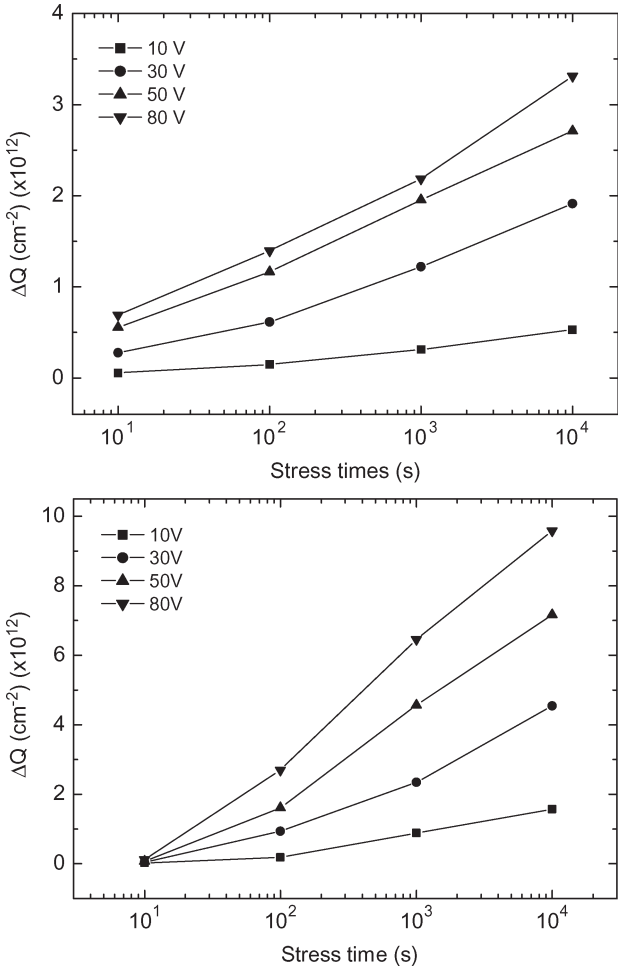

Fig. 5. Time dependence of the threshold voltage shift (converted to electrons per square centimeter) for a range of bias stress voltages for ZnO-TFTs with SiN (top) and SiO_2 (bottom) as the gate dielectrics.

in quantity of interface traps with insulator suggests that they could be predominantly interfacial.

The degradation of the normalized subthreshold slope for both sets of devices for a bias stress of 30 V is shown in Fig. 6. This behavior was qualitatively the same for all stress biases. The change in S is due to trap generation at the ZnO/insulator interface and/or at the grain boundaries in the ZnO channel region. It should be noted that the degradation is greater for the SiO_2 devices, indicating a greater increase in the trap state concentration than the ZnO/SiN devices.

This increase in the trap state concentration for both devices results in a decrease of the effective channel mobilities (Fig. 7). This implies that the density of trap states in the upper half of the band gap of the ZnO layer has changed as a result of the stress and that there is a net increase in the acceptor traps in this region.

In an effort to clarify the effects of bias stress, the evolution of some device parameters during the stressing periods has been studied. Fig. 8 (top) shows the change with stress time of the normalized maximum transconductance $\mathrm{Gm}/\mathrm{Gm}_O$, where Gm_O and Gm are the maximum transconductances before and after stress, respectively, for a stress bias of 30 V. It can be clearly seen that Gm decreases for both device structures and

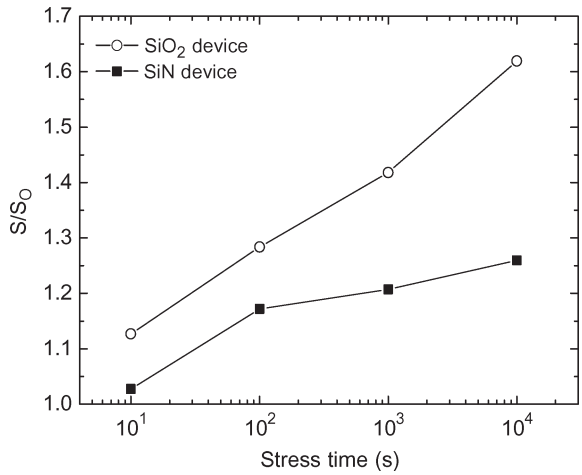

Fig. 6. Time dependence of the degradation of the normalized subthreshold slope for a bias stress voltage of 30 V.

that, for longer stressing times, the degradation is greater in the oxide transistors. Similarly, there is a reduction in the normalized OFF-state leakage current I_L/I_{LO}, where I_{LO} and I_L are the leakage currents before and after stressing, respectively, at $V_G = -5$ V and for $V_D = 2$ V (Fig. 8, bottom). However, the reduction in the OFF current for the nitride devices

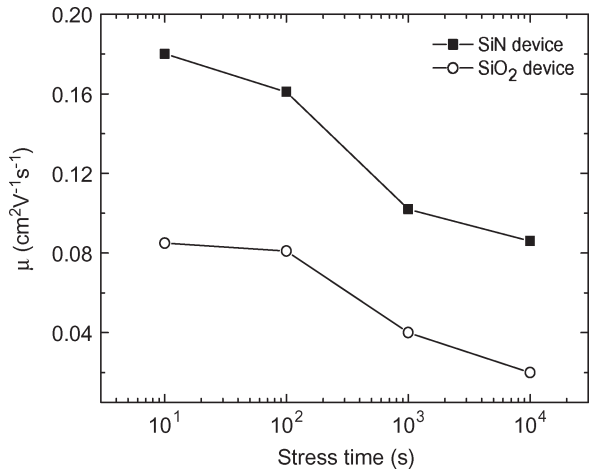

Fig. 7. Time dependence of the effective channel mobility for nitride and oxide ZnO-TFTs for a bias stress voltage of 30 V.

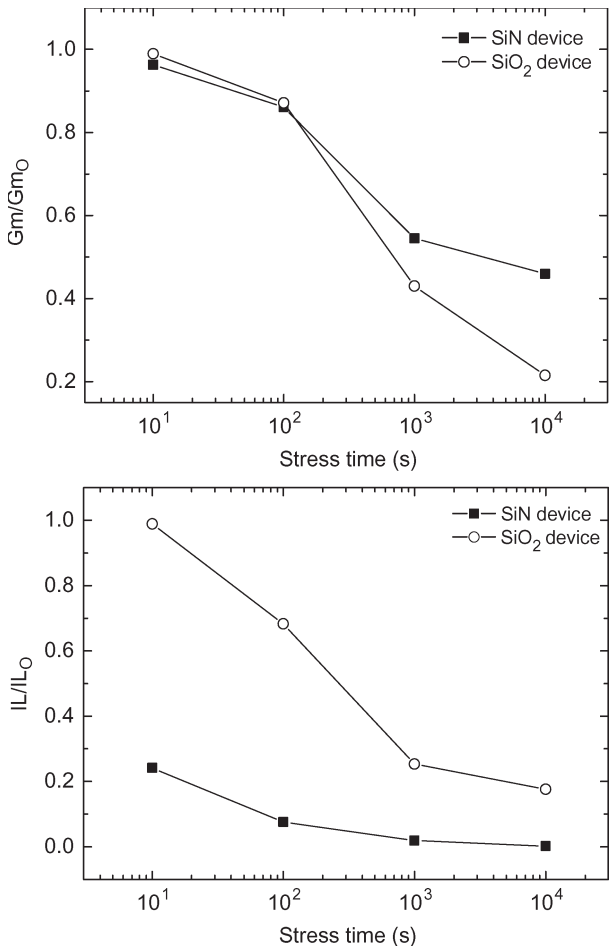

Fig. 8. Normalized maximum transconductance (top) and normalized OFF-state leakage current (bottom) as a function of the stress time (at 30 V) for both nitride and oxide device structures.

is greater and occurs much more quickly than in the oxide TFTs. The origin of the OFF-state leakage current in TFTs incorporating polycrystalline silicon as the channel layer has been attributed to field-enhanced carrier generation at grain-boundary dangling-bond trap states, whose energy levels lie deep within the band gap [13]. As ZnO is also a polycrystalline material, this argument could be qualitatively applied here.

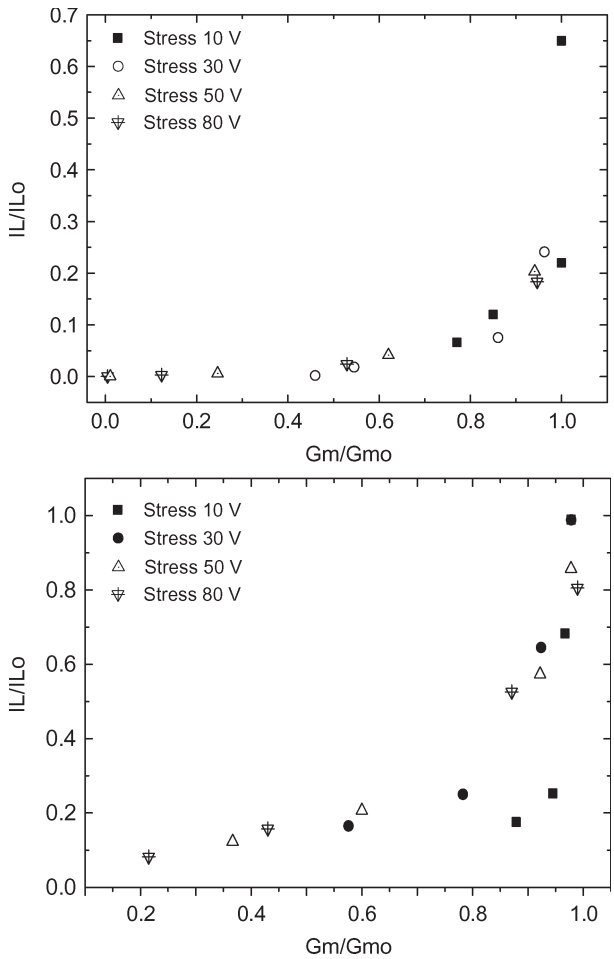

Fig. 9. Correlation between the normalized leakage current and normalized transconductance for various stress bias values for nitride (top) and oxide (bottom) TFTs. Each point for each bias value represents one decade of stressing time.

Therefore, the suppression of the leakage current during the previously demonstrated stressing periods could be due to the passivation of these grain-boundary trap states. Reduction in transconductance has been previously described as a function of the density of strained-bond tail states [14]. Therefore, the results in Fig. 9 (top) correlate with an increase in the density of these trap states for both oxide and nitride TFTs as a result of stressing. It is to be noted that the gate leakage currents in these transistors are negligible.

The correlation between the normalized leakage current and the transconductance for both sets of devices is shown Fig. 9. Whereas the overall degradation of the transconductance and reduction of the leakage current for both oxide and nitride TFTs is comparable, the rate at which these changes occur is different.

Most of the reduction in the leakage current for both devices takes place within the first 1000 s of stress, after which there is little change. However, there is a more gradual degradation in the transconductance throughout the stressing period. This suggests that the passivation of the deep defect levels responsible for the leakage current occurs more quickly than the generation of tail states resulting from strained bonds that cause a reduction in the device transconductance.

The changes in and the recovery of device performance as previously detailed could be qualitatively explained by the charging and discharging of preexisting traps at the interfaces and within the channel regions of the two structures.

Under positive bias stress, electrons are attracted toward the interfacial region and captured in interface trap states. At longer stress times/higher stress biases, more traps are filled. This results in a temporary fixed negative charge, which causes changes in the band bending and charge distribution in the channel region. In effect, a proportion of electron traps in the channel that are occupied at equilibrium in an as-deposited device is emptied, leading to an increase in the effective density of these trap states in the channel. This could explain the increase in the threshold voltage and the change in the subthreshold slope in the subsequent transfer characteristic measurement.

Commonly, defects in ZnO are attributed to instances of zinc interstitials or vacancies of oxygen and zinc. These defects contribute to the carrier concentration of the material causing its resistivity to decrease. However, current–voltage (I–V) measurements of the channel material used here revealed a resistivity of $\sim 10^8\ \Omega \cdot \mathrm{cm}$, indicating a low concentration of structural defects in its as-deposited state. Therefore, the unstable nature of these devices during bias stressing could be due the interface between the SiN and SiO_2 layers and the sputtered ZnO having a high concentration of trap states caused by a lattice mismatch between the layers.

Sputtered ZnO consists of tightly packed column grains with a high concentration of grain boundaries similar to nanocrystalline silicon [15]. The diameter of these columns is not uniform and decreases from the top of the grain to the bottom. Hence, as these devices are inverted-staggered structures, the channel of the TFT forms at the interface of the ZnO and the dielectric layers at the bottom of the film where the diameter is the smallest. Therefore, this high concentration of grain boundaries could be responsible for the higher trap density at the interfaces and, hence, contributes to the instability.

In an effort to investigate this further, AFM measurements were taken of the sputtered ZnO surface after deposition onto the insulator layers. These results are shown in Fig. 10.

It is evident that there are clear differences between the two topographies. The shape of the ZnO grains grown on top of SiN is elongated, as opposed to the conical shape demonstrated by the material grown onto SiO_2, with estimated grain sizes in the region of $\sim$90 nm for the ZnO/SiN and $\sim$60 nm for ZnO/SiO_2. The overall surface roughness of ZnO/SiO_2 is also greater than that of the ZnO/SiN stack with values of 4.223 and 0.663 nm, respectively. Despite the fact that the ZnO material was deposited under identical sputtering conditions to the same thickness, the resulting granular structure appears to be very different. This may be explained by the differences in the lattices at the interface between the ZnO and SiN/SiO_2 layers and, hence, contributes to the disparities in the performance of the two sets of devices.

IV. Conclusion

The performance and stability of ZnO-TFTs with SiN and SiO_2 as the gate dielectrics have been investigated and compared. The performance of the devices incorporating SiN, as measured by standard TFT parameters, was found to be superior to that of the SiO_2 transistors. The threshold voltage shift of both sets of devices under gate bias stress was found to have a logarithmic time dependence, indicating that charge trapping is the dominant instability mechanism. In addition, device parameters such as channel mobility, subthreshold slope, and transconductance were all degraded, whereas the OFF-state leakage current was found to decrease. It is suggested that temporary charging and discharging of preexisting trap states within the band gap and band tails of the ZnO channel layer is responsible for the deterioration of these device parameters.

The results suggest that the ZnO channel layer and/or the interface between the ZnO and the gate insulator layers are susceptible to charge trapping/defect formation instabilities due to lattice mismatch. These instabilities, however, were found to be reversible at room temperature to near-original values without any need for thermal or bias annealing.

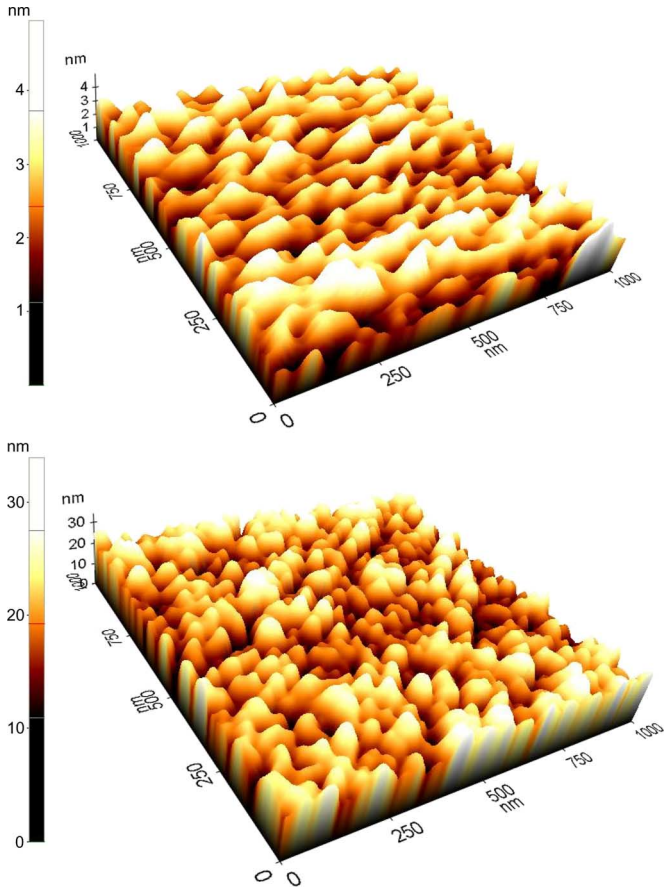

Fig. 10. AFM topographies of the sputtered ZnO surface deposited onto SiN (top) and SiO_2 (bottom) gate dielectric layers.

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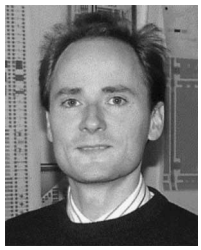
R. B. M. Cross was born in the U.K. in 1975. He received the B.Sc. (Hons.) degree in physics and the M.Sc. degree in information technology from De Montfort University, Leicester, U.K., in 1997 and 1998, respectively, and the Ph.D. degree from the Emerging Technologies Research Centre (EMTERC), De Montfort University, in 2005. His doctoral research involved the development of a low-temperature deposition process for hydrogenated amorphous silicon for thin-film transistor (TFT) applications.

Since April 2005, he has been a Research Fellow with EMTERC, working on different TFT technologies and the growth and characterization of semiconducting nanostructures.

Maria Merlyne De Souza was born in India in 1964. She received the B.Sc. degree in physics and mathematics from the University of Bombay, Mumbai, India, in 1985, the B.E. degree in electronics and communications engineering from the Indian Institute of Science, Bangalore, India, in 1988, and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1994.

Since November 2007, she has been with the University of Sheffield, Sheffield, U.K., where she holds a Chair in Microelectronics at the Department of Electronic and Electrical Engineering. From 1995 to 2007, she was with the Emerging Technologies Research Centre, De Montfort University (DMU), Leicester, U.K., where she was one of the founding members. She held a Chair in Electronics and Materials at DMU from 2004 to 2007. She has authored or coauthored more than 150 papers published in international journals and conference proceedings. Her main research interests include ultrashallow junctions, reliability, functional materials, high-k gate dielectrics, RF power and power semiconductor devices and technologies, and large-area electronics.

Dr. De Souza is a Fellow of the Institute of Physics and the Institution of Engineering and Technology. She has been serving on the Technical Program Committee of the International Reliability Physics Symposium since 2003. She was a member of the Editorial Board of *Microelectronics Reliability* from 2001 to 2005.



Steve C. Deane received the B.A. degree in electronic and information sciences and the Ph.D. degree in the understanding of amorphous silicon from the University of Cambridge, Cambridge, U.K., in 1988 and 1992, respectively.

He is a designer of circuits and displays using amorphous and polysilicon thin-film transistors, as well as conventional silicon technology. In 1992, he joined Philips Research Laboratories, Surrey, U.K., where he has been working on a wide variety of display and novel thin-film electronics projects. His current research interest includes laboratory-on-glass technology for healthcare applications.

Nigel D. Young received the B.Sc. (Hons.) degree in physics and the Ph.D. degree in solid-state physics from the University of Leeds, Leeds, U.K., in 1980 and 1984, respectively.

In 1984, he joined Philips Research Laboratories, Surrey, U.K., where he worked on hot electron transistors. Since 1986, he has been working in the field of MOS devices and technology within the polysilicon TFT program. He has run projects developing processes and applications on glass, metal, and plastic substrates and has demonstrated many applications, including AMLCDs, AMOLEDs, EEPROMs, and fingerprint scanners. His current research interest includes laboratory-on-glass technology for healthcare applications.