The RISC-V in implantable medical devices

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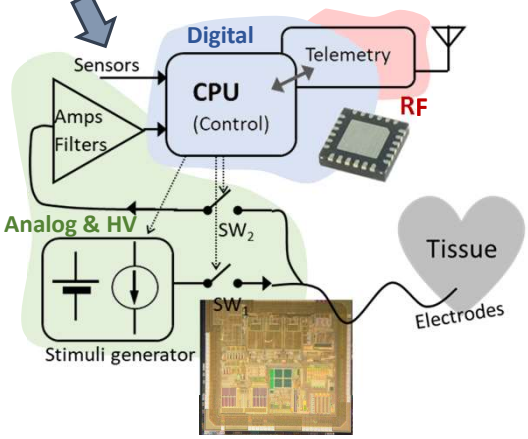
The RISC-V in IMDs … why?

IMD scheme:



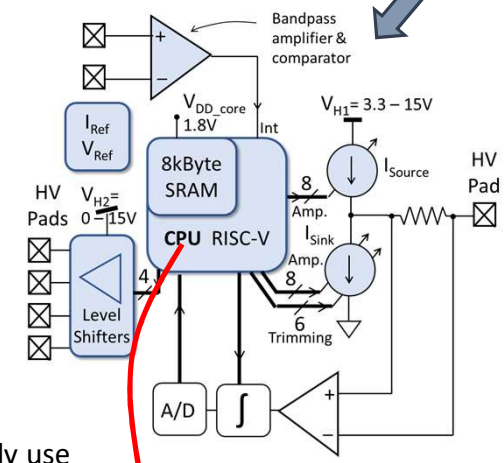
Small-medium companies, startups normally use **(ASIC + µC)** because of cost & complexity

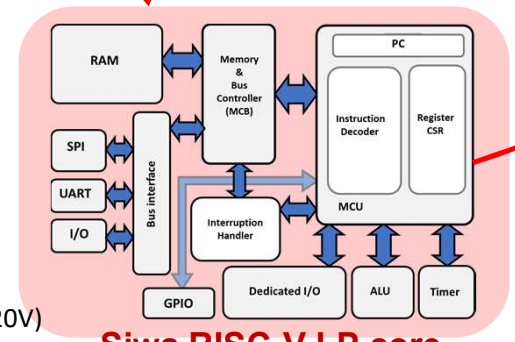
RISC-V to help integrate a SOC !!

Specific IMD ASIC issues:

- Low volume, development cost $, per-chip cost $$$$
- Reliability and safety issues
- Minimum power consumption, battery ~ yrs., minimum sleep ↔ wake-up power.
- SOC (digital+analog) in HV technology (up to 20V) Flash desired, HV ESD & special PADs.

The proposed SOC





Siwa RISC-V LP core

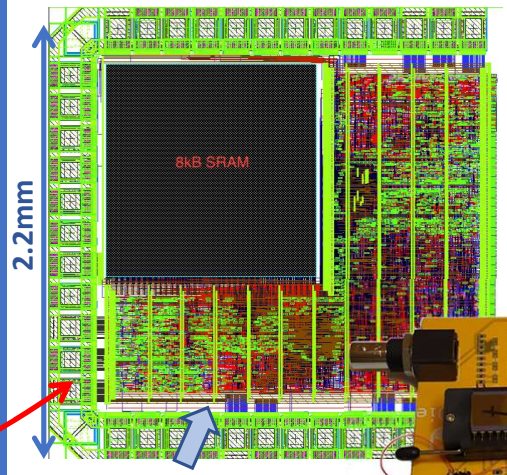
The fabricated chip

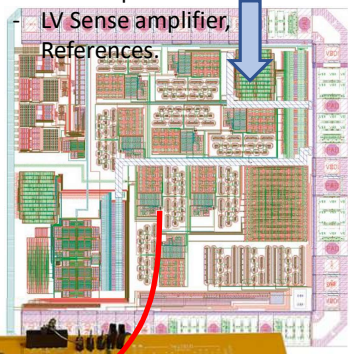
Circuit fabricated in .180µ HV-CMOS

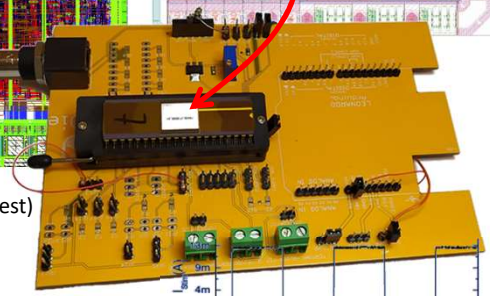
- HV up to 45V, 200V transistors
- Dense 1.8V digital, FLASH, SOI available for reliability, latch-up, etc.

Analog & HV circuit blocks

- 15V, (8+6) bits programmable sink/source current source.
- HV I/O ports (up to 18V).
- HV ESD protection.
- LV Sense amplifier, References.

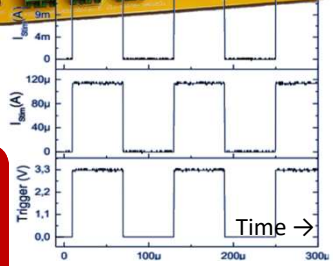






SIWA RISC-V core (under test)

- 32RVI 0.82mm^2 core
- SPI, UART, GPIO, 8kB SRAM
- packet-based bus & memory controller
- 20MHz@1.8V, < 47 pJ/cycle
- reliability and safety issues considered

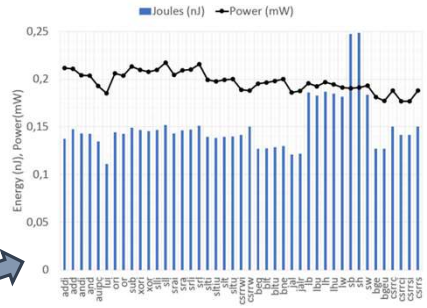


Measured programmable current source.

Simulation results

Siwa comparison @20MHz, 1.8V V_{DD}

Core	Siwa	Mriscv [3], [4]	Riscy [5]	Zero-Riscy [5]	Micro-Riscy
Technology	180 nm	130 nm	65 nm	65 nm	65 nm
Frequency	20MHz	160MHz	N.D	N.D	N.D
ISA	RV32I	RV32IM	RV32IM+DSP	RV32IM	RV32E
Program Memory	8 kB	4 kB	N.D	N.D	N.D
Average CPI	4	N.D	1.27	1.49	1.49
pJ/cycle	48.31	850	63.68	26.12	23.61
Core Area (μm^2)	672146	350250.4	703296	326592	200448

Core	Siwa	8051-Compatible [10]	Atmega328p [7]	PIC16LF1823 [8]	MSP430 [9]
Technology	180 nm	180 nm	N.D	N.D	N.D
Instruction word size (bits)	32	N.D	16	8	16
Program Memory	8 KB	N.D	32 KB FLASH	2 KB	8 KB RAM
Clock freq.	20 MHz	13 MHz	0-20 MHz	31 kHz- 32 MHz	4-16 MHz
Average CPI	4	N.D	1.62	1.1837	≈ 1
pJ/cycle	48.31	70.6	360	54	803
Average power (μW)	70@1MHz@1.8V	918@13MHz@ -	360@1MHz@1.8V	54@1MHz@1.8V	803@1MHz@2.2V

Energy consumption per instruction