A RISC-V Based Medical Implantable SoC for High Voltage and Current Tissue Stimulus

A. Arnaud*, M. Miguez*, J. Gak*, R. Puyol*, R. Garcia-Ramirez†,
E. Solera-Bolanos†, R. Castro-Gonzalez†, R. Molina-Robles†, A. Chacon-Rodriguez†, and R. Rimolo-Donadio†
*Depto. de Ingeniería Eléctrica, Universidad Católica del Uruguay
†Escuela de Ingeniería Electrónica, Instituto Tecnológico de Costa Rica
Email: {aarnaud, mmiguez, jgak}@ucu.edu.uy {rgarcia, esolera, rmolina, alchacon, rrimolo}@tec.ac.cr

***Abstract*—A RISC-V based System on Chip (SoC) for high voltage and current tissue stimulus, targeting implantable medical devices, is presented. The circuit is designed in a 0.18μm HV-CMOS process, including the RISC-V 32RVI based micro-controller core, called Siwa —which includes SPI, UART and GPIO interfaces, a packet-based bus and memory controller, and 8kB SRAM—, combined with several biological tissue stimulus and sensing circuits. The complete test chip (analog+RISC-V) occupies a 5mm^2 area but only 0.82mm^2 correspond to the RISC-V micro-controller, which operates up to 20MHz, with average energy needs of less than 48 pJ/cycle (3pJ STD), and for which several reliability and safety issues were considered.**

***Index Terms*—Implantable medical devices, CMOS HV, RISC-V, level shiters, current sources, biomedical circuits.**

I. Introduction

A generic implantable medical device (IMD) typically includes electrodes connecting the tissue to the device through one or multiple pass-switches, sensors, amplifiers a nd filters for the signal conditioning of body's natural electrical activity, an intelligent programmable control logic (CPU) deciding when and for how long a stimulus should be applied, a telemetry block for communicating data when necessary, and a stimulus section composed of voltage and/or current sources. In the case of mature products like pacemakers or cochlear implants and large IMD manufacturers, both the micro-controller and sensing/stimulus circuits are integrated into the same SoC. In other cases, an off-the-shelf micro-controller is used, usually combined with an analog ASIC for sensing/stimulus functions [1], but this option unnecessarily increases power consumption, PCB size, and production costs. IMD ASICs are usually implemented in a HV technology (able to withstand up to 20V, which is necessary for tissue stimulation), with micropower consumption (assuring battery lifetimes of years), with safety-oriented and reliable circuits and systems [1], and typically with low volume production needs, (thousands to hundreds of thousands).

In this context, an open instruction set, scalable CPU based on the RISC-V ISA would allow small to medium-sized biomedical companies to afford their own CPU-based ASICs.

[1]A reliable circuit is less likely to fail; a safety compliant circuit means it will not result harmful for the patient even in the case of a single failure event.

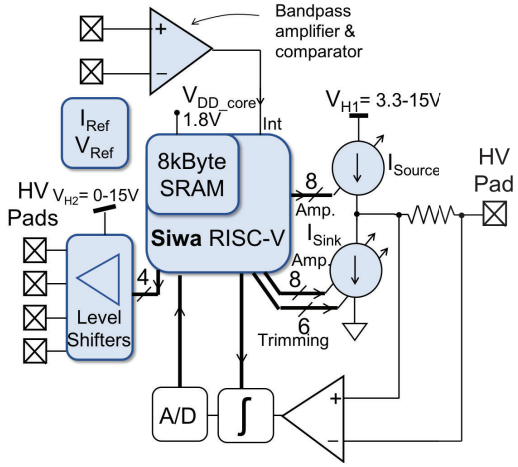

Figure 1. The proposed IMD SoC Siwa-based application topology (blocks designed in this work are colored).

While a 32-bit CPU may sound complex or power hungry, recent advances in Application Specific Processors (ASP) allow to implement efficient controllers even for the case of medical applications. The idea is to remove unnecessary features like floating point capabilities, predictive execution modes, superscalar pipelines, multi-level cache and/or DMA, etc. As pointed by Strydis *et al* in [2], this strategy enhances system reliability and simplifies making the system safe.

Figure 1 shows this work's proposed IMD SoC topology. After a thorough state-of-the-art review on microprocessor based IMDs, and to the authors' best knowledge, this is the first proposal made for a RISC-V based IMD found in the literature [3]. This paper is organized as follows: Section II details the design of biological stimulus circuit implemented for the SoC IMD; Section III describes Siwa, the RISC-V RV32I based programmable controller core (PCC) proposed for the IMD, and compares it to other processors commonly used in implantable medical devices; finally, Section IV gives some conclusions of this work, as well as some prospects of its further development.

II. Biological tissue stimulator block

The system in Fig. 1 requires that the CPU amplifiers and sensors' supply voltage be V_{DD} connected directly to the

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battery powering the IMD, or derived from an efficient DC-DC down-converter [4], [5]. On the other hand, the electrical stimuli to be delivered to the tissue are either voltage or current pulses (or pulse trains), ranging from a few hundreds of mV to well over 15V, or from a hundred μA to tens of mA. In this context, relatively high voltage circuits are necessary to implement the current or voltage sources connected to tissue and, if necessary, to open/close the HV switches.

This work's IMD SoC includes several HV sink and source 8-bit programmable current sources, and a 4-bit HV port using level shifters capable to translate from the 1.8V core supply to a range from 0 to 15V. A ULP bandpass amplifier and a comparator block were also included in order to test the CPU's interrupts system, with ULP voltage and current references for the analog blocks.

A. High voltage stimulus circuits

Stimulus voltage magnitudes in IMDs depend on the patient, treatment, and device state. Thus, circuits must operate in a wide voltage range. Level shifters (LS) are therefore essential blocks, translating logic levels between voltage domains. LS can be useful in several applications: communicating a low V_{DD} processor to a 5V peripheral, driving HV displays, handling large voltages necessary in non-volatile memories, driving the gate of a high-side pass transistor in a switched converter, or in medical devices in order to implement tissue-stimulus delivery subsystems [6]–[9]. While in the first examples the design of a LS is simple because V_{DD} and V_H are fixed, the latter example becomes challenging if V_H is unknown. In IMDs, V_H can be either 15V, 5V or 300mV depending on the device state or the programmed stimulus values (V_H either above or below V_{DD}).

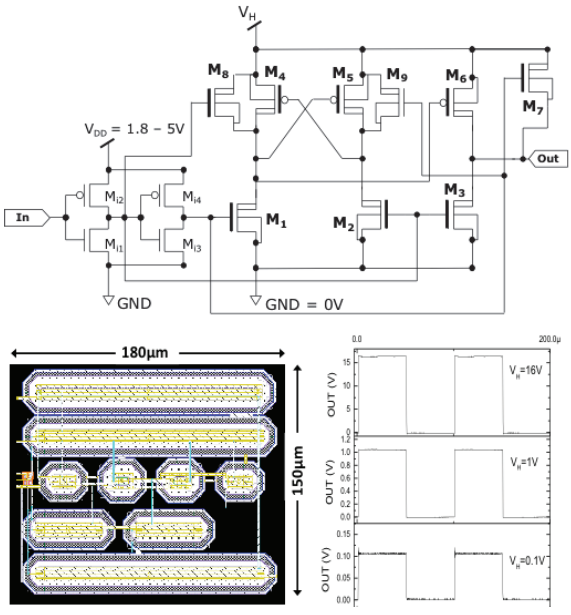

Figure 2. The proposed level shifter schematic (top), and its layout (bottom left). Measured output data from a prior test structure (bottom right) shows the output's 16V full range with a 3V, 10kHz input.

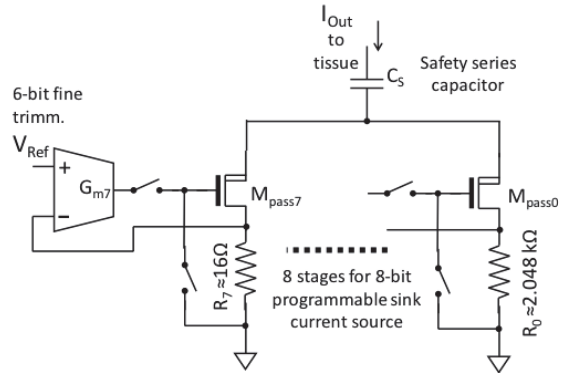

Figure 3. Proposed programmable current sink circuit.

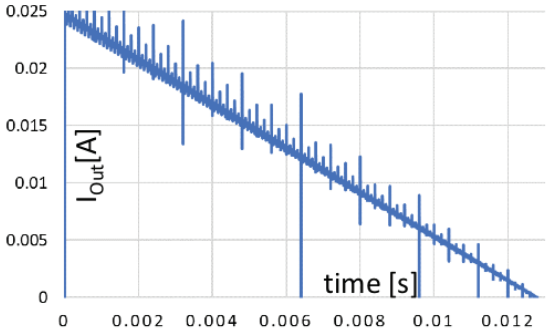

Figure 4. Transient simulation of the programmable sink current source covering 256 steps.

Figure 2 shows the implemented level shifter, a variation of the classic level shifter [6], [10]–[12] but following the guidelines in [7]. HV-NMOS transistors $M_{7,8,9}$ are placed in parallel with HV-PMOS to cover low voltage V_H values. V_H in Fig. 2 may be as low as 0V, and with proper transistor sizing may be as large up to the maximum gate-source voltage—V_{GSmax} = 18V—that M_{1-6} can withstand. Note that HV transistors in modern HV-CMOS technologies include a thick gate oxide for a V_{GSmax} up to 18-20V, and an extended drain to avoid large electric fields that allows elevated maximum drain to source voltages (V_{DSmax} up to 6V to 700V), depending on transistor construction and technology. Transistors M_{1-6} in Fig. 2 are HV, having a different symbol indicating the thick oxide and marking the extended drain; note that only the drain is extended so HV transistors are not symmetrical. A section of the LS layout is shown in Fig. 2, including large HV transistors designed to drive a 200pF output load, as well as the measured LS output from a previous version of the same LS.

B. Programmable sink/source current sources

The designed programmable sink current source (I_{sink}) is shown in Fig. 3 (sink = lower current source of Fig. 1). It is composed of 8 parallel HV pass transistors $M_{pass7:0}$, each one with its corresponding feedback OTA $G_{m7:0}$ and feedback resistor $R_{7:0}$, imposing approximately a 200mV resistor voltage drop. Pass transistors $M_{pass7:0}$ are sized from the MSB,

with a $(W/L)_7$ = 3000μm/2.9μm the widest (for a minimum worst-case voltage drop V_{DS} = 250mV @I_D = 12.5mA and a `ws` transistor model) to LSB $(W/L)_0$ = 400μm/2.9μm the narrowest. An input symmetrical OTA is used, and the switches in Fig. 3 are transmission gates or NMOS transistors. With this configuration, an 8-bit programmable current source with 100μA steps up to 25.5mA was implemented. The voltage reference V_{Ref} = 200mV for all the eight stages may be trimmed by the Siwa processor with a 6-bit resistive voltage divider. In this way, while integrating the overall output current like in Fig. 1, it is possible to adjust V_{Ref} in the sink current to match it to the upper current source (assumed to be equally programmed). Both current sources must be matched in order to deliver balanced bipolar current pulses to the tissue (minimizing passive charge balance requirements [1], [13]). The objective is to reduce the net error between both currents below 1%. In Fig. 4 a transient simulation is shown for the current source in Fig. 3 covering the 256 steps, 50μs each. While transient current peaks are observed, due to parasitic capacitors' charge/discharge, the current source properly sets the 256 current steps. The sink current source occupies an approximated 500μm × 500μm die area.

The upper current source in Fig. 1 (I_{source}) is similar to the one in Fig. 3, but: the pass transistors are now PMOS; a HV symmetrical OTA substitutes that one of Fig. 3; HV switches are used to open/close the feedback loop including LS like the one in Fig. 2 to control the switches from the Siwa processor; V_{Ref} is not adjustable. Because of larger HV transistors, the upper current source occupies more than twice the area of the lower one.

The output resistor in the current sources is used to measure the output current using a low offset (autozero) amplifier and a configurable integrator; the PCC controls the amplifier's gain and the integration parameters. It is important to measure the output current for two reasons: to measure the output impedance of the electrode connected to the tissue, to track the electrode's state and stimulus effectiveness, and to allow the trimming of the sink current source to match the upper current source. The current/impedance measurement sub-system has not been included in the present version of the SoC. Layout of the stimulator circuit is shown in Fig. 5.

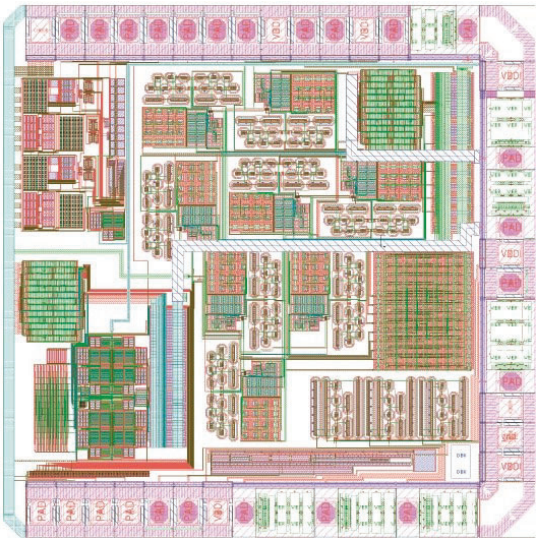

Figure 5. Layout of the analog section of the SoC, with guard rings used to avoid digital noise coming from the PCC. The PCC is connected to the left (not shown).

III. Programmable Controller Core

A RISC-V RV32I open architecture was selected as programmable controller core (PCC). The micro-architecture was customized for the intended high voltage, low power application. This meant generating a full in-house RTL micro-architecture specification, instead of opting for open implementations available, with several sections of the RISC-V modified accordingly. Particularly, the prevalent use of latches instead of standard master-slave flip-flops, allowed for smaller area and energy, and a finer-grain timing control.

The final PCC, called Siwa, is presented at the block level in Fig. 6. It includes a main control unit (MCU), 8 kB SRAM, a memory-bus controller unit (MBC), an ALU intended for integer arithmetic, a timer, and an interrupt handler. The MCU interfaces the memory mapped I/O units through a packed-based central bus; communications from the system to the MCU are queued, and accessible through custom control and storage latch-based registers (CSRs) via interrupts. The MCU is single threaded, with its 53 instructions and CSRs adapted from the standard RISC-V ISA. I/O interfaces include a UART, an SPI and 8 GPIOs; also, dedicated I/O channels controllable via custom CSRs are included for the HV stimulators. The bus interface and the I/O controllers may be disabled at will by the programmer to save dynamic power. SPI and UART interrupts may also be disabled; data from these interfaces is queued as well, in order to wait for critical tasks preventing immediate handling of interrupts from the communication ports. Interrupts may be generated from an external pin too. The bootstrap is carried out through an external serial flash memory connected to the SPI interface.

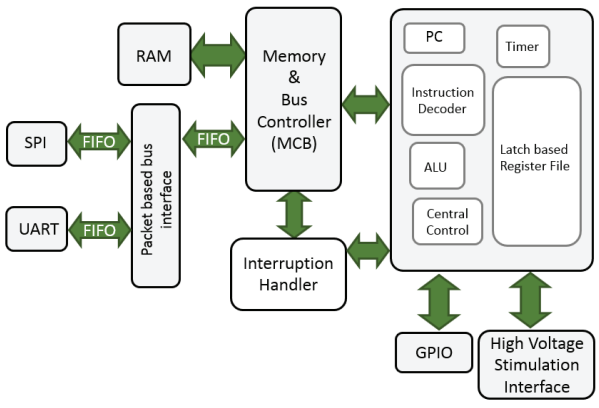

Figure 6. Siwa RISC-V CPU topology: a multicycle architecture, with clock-gated blocks that can be turned off and on from provided custom assembler instructions.

Table I
COMPARISON OF THE PROPOSED MICRO-ARCHITECTURE WITH OTHER IMPLEMENTATIONS IN THE IMD FIELD

Core	Siwa	8051-Compatible [14]	Atmega328p [15]	PIC16LF1823 [16]	MSP430 [17]
Technology	180 nm	180 nm	-	-	-
Instruction word size (bits)	32	-	16	8	16
Program Memory	8kB	-	32kB FLASH	2kB	8kB RAM
Clock freq. range	1-20MHz	13MHz	0-20MHz	31kHz-32MHz	4-16MHz
Average CPI	4	-	1.62	1.1837	≈ 1
pJ/cycle	48.31	70.6	360	54	803
Average power (μW)@clk, V_{DD}	70@1MHz, 1.8V	918@13MHz, -	360@1MHz, 1.8V	54@1MHz, 1.8V	803@1MHz, 2.2V

Siwa was verified using a UVM framework and then fully tested on a FPGA (including bootstrap and I/O, running several compiled applications). Post-placed-and-route static timing analysis was carried out to check for the critical latch-based timing paths. The PCC is implemented using low power high density library cells provided by the foundry: there are four separate voltage domains for independent power control, including the SRAM's, and providing 3.3V digital interfacing to the biological stimulator, placed on top. The total cell count is 11817, excluding pads and the SRAM. The estimated average energy consumption per clock cycle is under 48pJ/cycle, well under what is typical for common micro-controllers in the IMD industry, such as the MSP430, at 803pJ/cycle, as shown in Table I.

IV. CONCLUSIONS

A proposal for a RISC-V based implantable SoC has been presented, with several HV stimulus delivery subsystems, as necessary in most active implants. The SoC includes two 100μA to 25.5mA programmable HV current sources, current and voltage references, a biomedical amplifier and filter, and 4 bits HV level shifters. Siwa, the RISC-V RV32I based PCC was area/power optimized, and is competitive in terms of estimated performance with and energy consumption of under 48 pJ/cycle. The final circuit occupies a total area of 3mm$\times$1.5mm in the target 0.18μm HV-CMOS technology, including HV ESD protected pads.

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