Enhanced ICMR amplifier for high CMRR biopotential recordings

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***Abstract*— This paper presents an integrated biopotential preamplifier architecture targeting applications that simultaneously require high common-mode rejection ratio (CMRR), low noise, high input common-mode range (ICMR), and current-efficiency (low Noise Efficiency Factor or NEF). A biopotential preamplifier, which performs well in line with the state-of-the-art of the field while providing enhanced ICMR and CMRR performance, was fabricated in a 0.5 μm CMOS process. Results from measurements show that the gain is 47 dB, the bandwidth ranges from 1 Hz to 7.7 kHz, the equivalent input noise is 1.8 μV_{rms}, the CMRR is 100.5 dB, the ICMR is 1.7 V and the NEF is 3.2.**

I. Introduction

The preamplifier is probably the most important part of a biopotential recording system (see Fig. 1), because it is the part of the system that is in closer contact with the biological medium and it has to deal with the particular characteristics of the targeted signals. According to the nature of the biopotentials and the target application, the preamplifier must meet challenging requirements, which usually are contradictory: ultra-low-power consumption, low noise, small size, high input impedance, high input common-mode range (ICMR), high common-mode rejection ratio (CMRR) and reject input dc values that are much higher than the input signal amplitude.

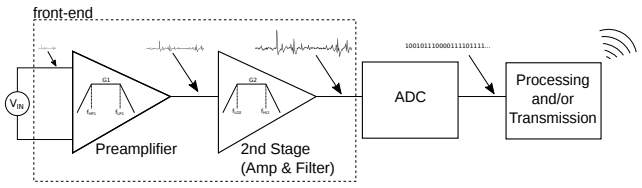

Fig. 1. A Top-level schematic of a typical biopotential recording system (shown for only one channel and only the acquisition/transmitter side).

Based on a modified differential difference amplifier (DDA [1], [2]), in [3] an architecture of a neural recording band-pass amplifier was introduced. [3] focuses on applications that specially require an amplifier with low noise, high CMRR and current-efficiency (low Noise Efficiency Factor or NEF). The amplifier improves the performance with respect to capacitive feedback neural amplifiers (i.e. [4]) by taking advantage of the high CMRR achievable in a standard DDA structure without jeopardizing power consumption. However, this architecture presents a limited ICMR: about 380 mV from a power supply of 3.3 V.

This work introduces a variation of the architecture proposed in [3] aiming to increase the ICMR. In addition, the variation of the gain and CMRR with the input dc voltage ($V_{IN,dc}$) is analysed. The remainder of this paper is organized as follows, in Section II we introduce and describe the circuit architecture. Next, in Section III we present the main aspects of the implementation. Then, in Section IV we present experimental results. Finally, Section V contains concluding remarks.

II. Architecture

The main difference between [3] and this work lays on the structure of the main transconductor input stage (see Fig. 2). Our main transconductor Gm1 is formed by M1-M12 and its transconductance is $Gm1$. Gm2 and Gmf are symmetrical OTAs (Operational Transconductance Amplifiers) whose respective transconductances are $Gm2$ and Gmf. $g_{m2} = K_{G_{m2}} G_{m2}$, where $K_{G_{m2}}$ is the copy factor of the current mirrors of Gm2, as indicated in Fig. 2, and g_{m2} is the transconductance of input transistors of Gm2. In the same way we introduce $K_{G_{mf}}$ such that $g_{mf} = K_{G_{mf}} G_{mf}$ and g_{mf} is the transconductance of the input transistors of Gmf.

The M6-M9 block, jointly with Gmf and C_F, are dedicated to establish the high-pass characteristic and to block the dc input (we refer to the interested reader to [3] for further details on the functioning of this part of the circuit). In small-signal operation M6-M7 and M8-M9 can be interpreted as asymmetrical differential pairs where α defines the degree of asymmetry. $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m9}$, where g_{m6}, g_{m7}, g_{m8} and g_{m9} are the transconductance of M6, M7, M8 and M9 respectively. α is a key parameter that rule the trade-off between dc block capacity and gain. For instance, in this work an $\alpha \gg 1$ is adopted, which implies that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m9}$. In this case the loss of gain will be negligible, but the capacity of blocking high levels of dc input signals (named $V_{IN,dc}$) will be reduced (this is later quantified in Table II).

A. Transfer function

Gm1 is an OTA with a differential input (v_{IN}) and a single ended input (v_F). This single ended input is used in the local feedback loop at the output for dc blocking. The transfer function of Gm1 is as follows (see Fig. 2):

$$i_{Gm1} \cong G_{m1} v_{IN} + (g_{m6} + g_{m9}) v_F \quad (1)$$

where G_{m1} is the Gm1 transconductance ($G_{m1} = g_{m1}$ where g_{m1} is the transconductance of M1 and M2).

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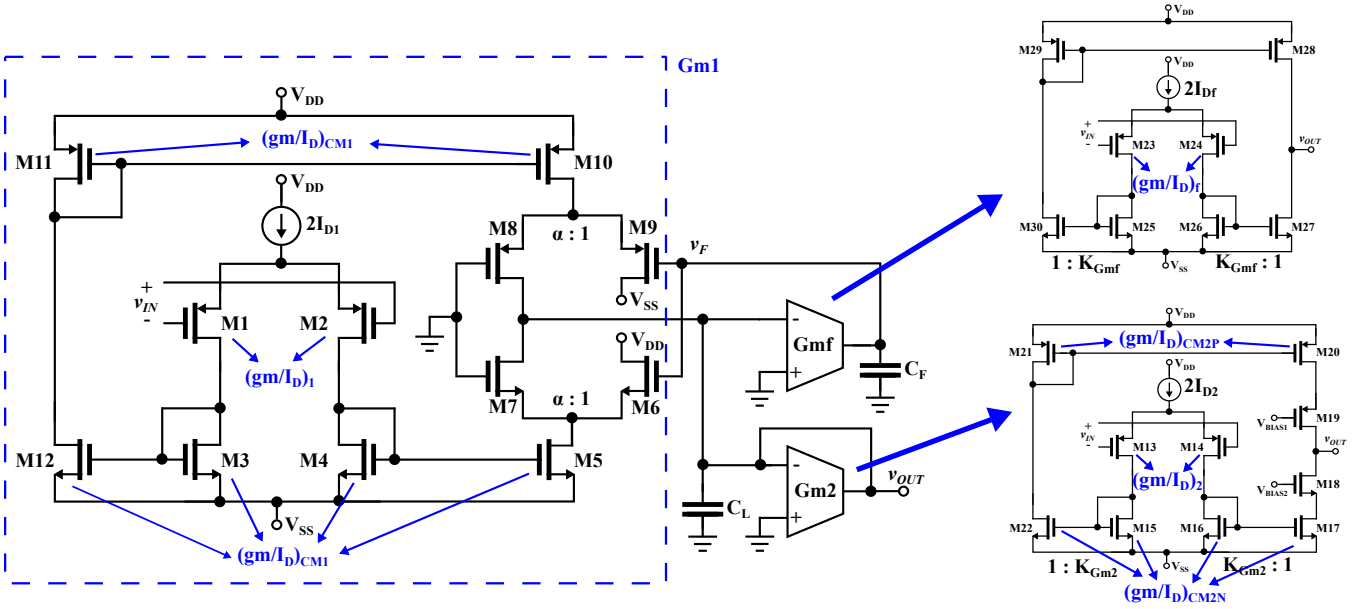

Fig. 2. Block diagram of the proposed architecture. M1-M5 and M10-M12 are the Gm1 core. High pass characteristic is fixed through M6-M9, Gmf and C_F. Gm2 and Gmf are implemented with symmetrical OTAs.

The circuit depicted in Fig. 2 has the transfer function presented in Eq. 2,

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L}s}{s^2 + \frac{G_{m2}}{C_L}s + \frac{(g_{m6}+g_{m9})G_{mf}}{C_L C_F}} \tag{2}$$

and the low-pass frequency $f_{low-pass}$ is given by Eq. 3, the bandpass gain G by Eq. 4 and the high-pass frequency $f_{high-pass}$ by Eq. 5,

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{3}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{4}$$

$$f_{high-pass} = \frac{(g_{m6}+g_{m9})}{G_{m2}}\frac{G_{mf}}{2\pi C_F} \tag{5}$$

B. Noise

It can be proved that the thermal noise input-referred power spectral density S_{ni}^{total} for the circuit shown in Fig. 2 is:

$$S_{ni}^{total} \cong \frac{2\gamma nkT}{G_{m1}}.[A + \frac{I_{D2}}{I_{D1}}.B] \tag{6}$$

where γ is the excess noise factor ($\gamma = 2$ in weak inversion and $\gamma = 8/3$ in strong inversion), n is the slope factor, k is the Boltzmann constant, T is the absolute temperature, and, A and B are:

$$A = 1 + 2\frac{(g_m/I_D)_{CM1N}}{(g_m/I_D)_1} + \frac{(g_m/I_D)_{CM1P}}{(g_m/I_D)_1} \tag{7}$$

where $(g_m/I_D)_1$ and $(g_m/I_D)_{CM1i}$ are respectively the transconductance to dc drain current ratio of the input transistors of Gm1 (M1 and M2) and of the current mirror transistors of Gm1 (M3-M5 and M10-M12, the subscript i indicates whether it is an NMOS or PMOS transistor),

$$B = \frac{(g_m/I_D)_2}{(g_m/I_D)_1 K_{G_{m2}}^2} + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}^2} + \\ + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}} + \frac{(g_m/I_D)_{CM2P}}{(g_m/I_D)_1 K_{G_{m2}}} \tag{8}$$

where $(g_m/I_D)_2$ and $(g_m/I_D)_{CM2i}$ are respectively the transconductance to dc drain current ratio of the input transistors of Gm2 (M13 and M14) and of the current mirror transistors of Gm2 (the subscript i indicates whether it is an NMOS or PMOS transistor), and $K_{G_{m2}} = g_{m2}/G_{m2}$. These equations show the contribution of $K_{G_{m2}}$ in the noise reduction.

In order to reduce noise, according to Eqs. 6 and 7, M1 and M2 have to be biased in weak inversion (high (g_m/I_D)), and M3-M5 and M10-M12 in strong inversion (low (g_m/I_D)).

III. Implementation

V_{DD} = 1.65 V and V_{SS} = −1.65 V were set. The node depicted as ground in Fig. 2 was set in the midpoint of the power supplies: $(V_{DD}+V_{SS})/2$ = 0 V. C_L was implemented as a poly-poly capacitor and its value is 10 pF, while C_F is external and its value is 22 nF. In order to reduce flicker noise, the area of the input transistors of Gm1 was increased in order to get a noise corner frequency of 250 Hz. In Table I we present the main parameters of Gm1 and Gm2. The amplifier was fabricated in a 0.5 μm standard CMOS process (see Fig.3).

TABLE I

GM1 AND GM2 MAIN PARAMETERS (POST-LAYOUT SIMULATIONS).

Transistors	L (μm)	W (μm)	I_D (μA)	g_m/I_D (V^{-1})	Description
M1, M2	2.6	1200	3.7	24.6	Gm1 input differential pair (subscript 1)
M3-M5, M12	84	40	3.7	5.1	Gm1 NMOS current mirror (subscript CM1)
M10, M11	40	55	3.7	4.6	Gm1 PMOS current mirror (subscript CM1)
M8	1	240	3.5	24	Gm1 PMOS cascode
M9	1	12	0.2	23.7	Gm1 PMOS cascode
M7	1	180	3.5	26	Gm1 NMOS cascode
M6	1	9	0.2	25.7	Gm1 NMOS cascode
M13, M14	2	1	0.4	6.6	Gm2 input differential pair (subscript 2)
M15, M16	20.9	1	0.4	3	Gm2 NMOS current mirror (subscript CM2N)
M20, M21	65	1	0.04	2.9	Gm2 PMOS current mirror (subscript CM2P)
M17, M22	188	1	0.04	2.8	Gm2 NMOS current mirror (subscript CM2N)
M19	65	1	0.04	2.9	Gm2 PMOS cascode
M18	188	1	0.04	3	Gm2 NMOS cascode

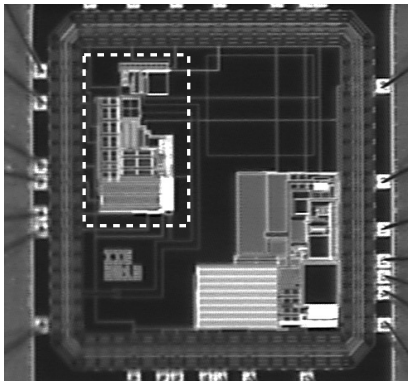

Fig. 3. Fabricated chip (dashed white rectangle).

TABLE II

TESTBENCH RESULTS

	Simulation	IC#01	IC#02
Gain (dB)	46.4	46.7	47.0
$f_{high-pass}$ (Hz)	1.4	1.0	1.0
$f_{low-pass}$ (kHz)	7.7	7.7	7.5
Supply current (μA)	16.1	16.1	16.1
Input noise (μV_{rms})	3.1	2.6	1.8
NEF	5.5	4.6	3.2
CMRR @ 1 kHz (dB)	N/A	87.6	100.5
Gain w/$V_{IN,dc}$ = 50 mV (dB)	39.6	39.7	39.7
Gain w/$V_{IN,dc}$ = 100 mV (dB)	33.1	30.4	29.8

IV. TESTBENCH RESULTS

This Section presents results of the experimental characterization of two samples of the same chip (named IC#01 and IC#02) and post-layout simulations (see Table II). Particularly, the variation of CMRR with dc input $V_{IN,dc}$ is introduced in Table III. In this table it is shown that the CMRR remains higher than 84 dB for dc input voltages in the range of $\pm$100 mV.

Fig. 2 presents the measured frequency response and CMRR. The performance in terms of CMRR is outstanding: below 3 kHz is always greater than 80 dB, at this frequency it starts to fall, and at 10 kHz still presents a high value, around 70 dB. In addition, at 50 Hz the measured value is 99.5 dB.

TABLE III

VARIATION OF CMRR WITH DC INPUT $V_{IN,dc}$ (IC#01).

$V_{IN,dc}$ (mV)	CMRR @ 1 kHz (dB)
-100	93.6
-50	90.4
0	87.6
+50	85.1
+100	84.0

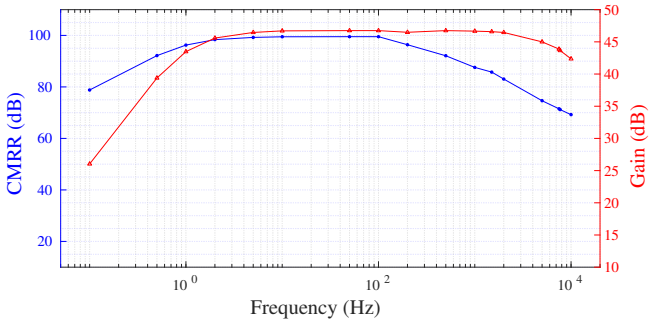

Fig. 4. Measurement of frequency response and CMRR.

The amplifier input common-mode range ICMR is approximately 1.7 V (within a $\pm$ 1.65 V power supply). This value of ICMR assures a loss of gain lower than 0.5 dB and a CMRR greater than 80 dB (see Fig. 5).

V. CONCLUSIONS

The proposed architecture enable a current-efficient biopotential preamplifier with high CMRR, low noise and high ICMR. As it is theoretically expected, a little loss of gain and almost no CMRR variation were registered when varying the input dc voltage ($V_{IN,dc}$). The measured characteristics of the amplifier shows a state-of-the-art performance (see Table IV).

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TABLE IV

COMPARISON WITH PRIOR WORK.

	[4]	[5]	[6]	[7]	[8]	[3]	This work
Technology (μm)	1.5	0.13	0.065	0.35	0.18	0.5	0.5
Gain (dB)	39.5	47.5	52.1	46.0	70	49.2	47
$f_{low-pass}$ (kHz)	7.2	6.9	8.2	10.0	1.0	10.3	7.5
$f_{high-pass}$ (Hz)	25m	167	1.0	200	0.5	0.1	1.0
Supply current (μA)	16.0	1.6	3.3	22.4	2.2	8.5	16.1
Input noise (μV_{rms})	2.2	3.8	4.1	2.9	1.2	1.9	1.8
NEF	4.0	2.3	3.2	6.6	2.4	2.1	3.2
$CMRR_{measured}$ (dB)	83	83	80	110	110	88	100.5
V_{DD} (V)	5.0	1.2	1.0	3.3	1.0	3.3	3.3

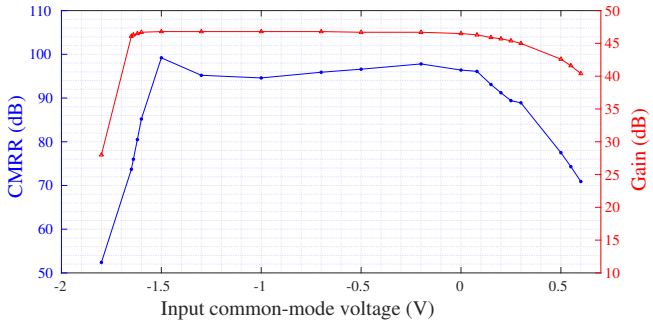

Fig. 5. Measurement of input common-mode range (ICMR). IC#01 Gain (blue) and CMRR (red) measurements for different dc input common-mode voltages (referred to ground). The figure shows that the ICMR is 1.7 V (with a $\pm$1.65 V power supply). These measurements were performed at 200 Hz.

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