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Proposed model for bistability in nanowire nonvolatile memory

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Cadmium sulfide nanowires of 10-nm diameter, electrodeposited in porous anodic alumina films, exhibit an electronic bistability that can be harnessed for nonvolatile memory. The current–voltage characteristics of the wires show two stable conductance states that are well separated (conductances differ by more than four orders of magnitude) and long lived (longevity >1 yr at room temperature). These two states can encode binary bits 0 and 1. It is possible to switch between them by varying the voltage across the wires, thus "writing" data. Transport behavior of this system has been investigated at different temperatures in an effort to understand the origin of bistability, and a model is presented to explain the observed features. Based on this model, we estimate that about 40 trapped electrons per nanowire are responsible for the bistability. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1937477]

I. INTRODUCTION

There is significant current interest in nonvolatile memories utilizing nanostructures since they promise extremely high packing density. A popular rendition of such devices is the quantum-dot flash memory based on charging and discharging of quantum dots or nanocrystals embedded in the gate insulator of a standard metal-insulator-semiconductor field-effect transistor.[1] These flash memories have an innate disadvantage. The difference between the two memory states depends on the charge stored in the quantum dots or nanocrystals. This charge must be considerably larger than the charge in the inversion layer of the transistor in order for the two memory states to be well separated and distinguishable in a noisy environment. Normally, this is difficult to achieve since the dot density is less than $10^{11}/\text{cm}^2$ so that the dots cannot hold a significantly larger amount of charge than the inversion layer. This shortcoming may become serious impediment to large-scale implementation of quantum-dot flash memory.

In the recent past, we found an electronic bistability in electrochemically self-assembled nanowire arrays embedded in an anodic alumina matrix.[2] This can lead to a nonvolatile memory that is free of the disadvantage mentioned above. We found that the current–voltage characteristic of the self-assembled system exhibits two stable conductance states that are separated in value by *four orders of magnitude*. Furthermore, we produce the wires by electrochemical synthesis in a beaker.[3] This technique is extremely inexpensive and also leads to a very *uniform* wire density exceeding $10^{11}/\text{cm}^2$. The wire diameter is 10 nm, with less than 1-nm standard deviation. In fact, both the density and positioning of the wires are extremely uniform, far more uniform than the nanocrystal distribution in the gate insulator of the quantum-dot flash memory. As a result, unoptimized devices, synthesized using beaker electrochemistry, show only $\sim 20\%$ variation across 20 samples tested.

Conductance bistability has also been found in molecular/organic structures where the two conductance states are separated by five orders of magnitude.[4] It has also been found in ferroelectric nanowires.[5] In many ways, the bistability phenomenon in these structures has striking similarity with what we find, although the underlying mechanisms are very different. Molecules and organics, however, are usually not compatible with conventional silicon device processing because they often cannot withstand high temperatures. Our fabrication methodology does not suffer from this shortcoming since we deal with semiconductors that can withstand much higher temperature than most organics. Therefore, it is possible that memory devices described here can be integrated with conventional silicon chips quite easily, unlike many organics.

II. ELECTRONIC BISTABILITY

The details of fabrication and electrical measurements of the self-assembled nanowire samples were presented in Ref. 2 and will not be repeated here. In Fig. 1(b), we present "schematically" the measured current–voltage ($I-V$) characteristic of an array of nanowires with current flowing between a top gold contact (contacting one end of the nano-

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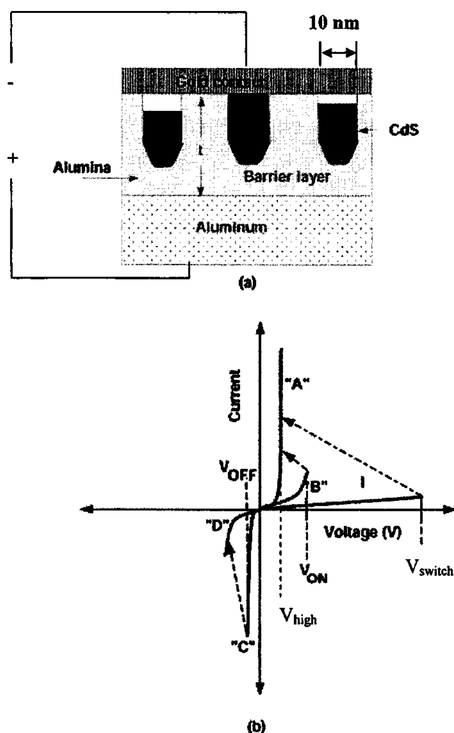

FIG. 1. (a) Sample configuration of the quantum wires. Current flows vertically between the top gold contact and the bottom aluminum contact. The "barrier layer" is depicted. (b) Schematic representation of the current–voltage characteristics of self-assembled quantum wires in alumina matrix showing the conductance bistability. This diagram is not to scale. The differential conductance in the characteristic "A" is actually four orders of magnitude larger than that in characteristic "B." Actual measured data can be found in Ref. 2. A and "C" are the high-conductance states, while B and "D" are the low-conductance states.

wires) and a bottom aluminum contact (contacting the other end through a tunnel barrier). Figure 1(a) shows the sample configuration. The actual measured data (composite of 20 different measurements) were presented in Ref. 2.

The $I-V$ characteristic is nonlinear. Forward bias corresponds to the case when the potential applied to the top gold contact is more *negative* than that applied to the aluminum back contact (note that there is a typographical error in Ref. 2 where the opposite polarity was indicated).

During the first pass under forward bias, the $I-V$ characteristic traces out the linear curve "I" and the sample conductance is very low (resistance >50 MΩ). When the bias reaches a voltage V_{switch}, the sample switches abruptly to the *high-conductance* state (curve "A"). Thereafter, the $I-V$ characteristic traces out the nonlinear curve A under forward bias, at least up to a current of 50 mA (we did not go past 50 mA to prevent sample overheating). If the forward bias is then gradually decreased, curve A is traced back with no discernible hysteresis. Finally, if we go past zero bias and reverse the polarity of the applied voltage, then curve "C" is traced out in reverse bias. It too has a high differential conductance. However, when the reverse bias voltage reaches a voltage V_{OFF}, the sample abruptly switches from curve C to a low differential conductance state and traces out the curve "D." Curve D is traced out in reverse bias, without hysteresis, at least up to a voltage of −30 V (again, we did not go past −30 V to prevent sample overheating). Then, if the voltage polarity is flipped back to forward bias, curve "B" is traced. This is also a low-conductance state. From this state, there is an abrupt switching to the high-conductance state (curve A) when the voltage over the sample reaches a threshold voltage V_{ON}. Both V_{ON} and V_{OFF} are depicted in Fig. 1(b). Note that curves A and C are the low-conductance states while curves B and D are the high-conductance states.

III. MEMORY APPLICATION

We intend to use the states "A" and "B" in forward bias [see Fig. 1(b)] to encode binary bits 0 and 1. The differential conductance dI/dV in these two states differs by four orders of magnitude[2] [note that Fig. 1(b) is schematic and not to scale]. For read/write operations, we can access the memory states as follows: to "read" the stored bit, one could probe the differential conductance with a small ac bias and thus retrieve the stored information. The "writing" strategy is the following. Precede the write cycle with a read cycle. If the stored bit is already the desired bit, do nothing. Otherwise, do the following: (i) if the device is in the low-conductance state B (logic 0) and the desired state is A (logic 1), then simply apply a forward dc bias past the threshold for switching (V_{ON}). This will switch the device to the desired state A (logic 1) and thus write the desired bit. (ii) If the device is in the high-conductance state A (logic 1) and the desired state is B (logic 0), then apply a reverse bias to take the system to state C, then exceed the threshold V_{OFF} to switch to state D, and finally reverse the voltage polarity to reach state B (logic 0). Note that if the device is "on," it must be reverse biased before it can be switched "off," since the characteristic B is not directly accessible from characteristic A. One has to go through C and D to reach B from A. However, if the device is off, then it is possible to switch it on without having to go through reverse bias because the high-conductance state A can be directly accessed from the low-conductance state B by applying a voltage V_{ON}.

Over a period of one year, we have cycled several samples numerous times (each more than 100 times) between the two memory states and always found switching between two well-separated states. The bistability is robust and long lived. The current–voltage characteristic presented in Ref. 2 [schematically reproduced in Fig. 1(b) here] was the composite trace of 20 different measurements on different samples produced in the same run. The results of these measurements varied by less than 20%. There are much larger variations between samples produced in *different* runs, but this is not unexpected given that electrochemical synthesis is not as well controlled as state-of-the-art semiconductor processing. Improving the device reproducibility between samples produced in different runs will require better-controlled electrochemical synthesis, which is currently being investigated.

The memory states are "nonvolatile;" if a sample is left in the high differential conductance state A, it remains there for at least 1 yr before decaying to the low differential conductance state B. If the sample is left in the low differential conductance state B, it remains there for no less than 1 yr, and possibly much longer.

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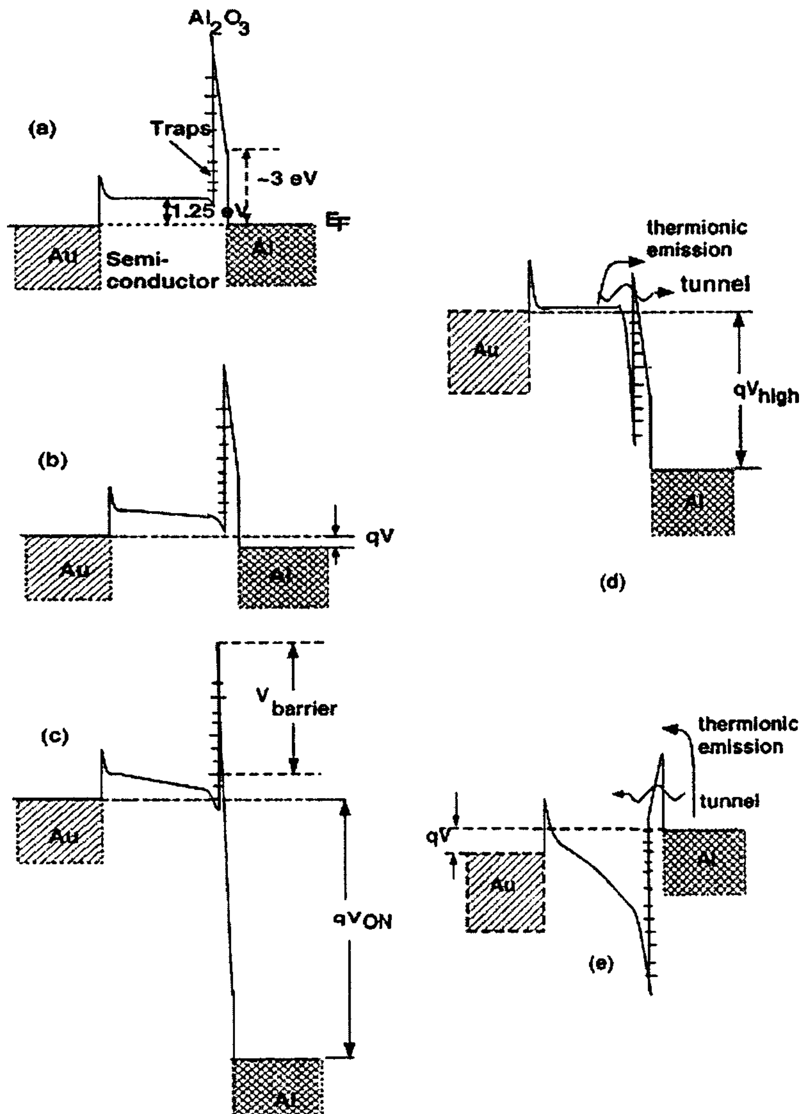

FIG. 2. Energy-band diagram (not to scale). The conduction band in the semiconductor represents the bottom of the lowest quantized subband in the cylindrical quantum wire: (a) equilibrium, (b) under a small forward bias when the conductance is low, (c) under a forward bias corresponding to V_{ON} when device is poised to switch from the characteristic "B" to "A," (d) after switching from B to A is complete, and (e) under reverse bias when the characteristic "C" is traced and just before switching to characteristic "D" with an applied bias V_{OFF}. Reproduced with permission from J. Nanosci. Nanotech. **5**, 753 (2005).

IV. ORIGIN OF BISTABILITY: PHENOMENOLOGICAL MODEL

We have postulated a model that could explain the bistability. This model is *speculative*, but it explains all the observed features in the $I-V$ characteristic.

During the first pass, when the device is in the characteristic I, the thin alumina barrier layer separating one end of the semiconductor nanowire from the aluminum contact [see Fig. 1(a)] is severely stressed (the electric field over the barrier layer approaches 20 MV/cm). This barrier layer is typically about 20–30 nm in thickness as revealed by cross-section transmission electron micrography in the past.[6] We believe that it causes irreversible migration of atomic species in the barrier layer and possibly results in the generation of traps at the interface between the CdS and alumina. These traps lower the barrier to conduction and cause switching from characteristic I to A when enough traps have accumulated at the CdS/alumina interface. How traps can lower the barrier is explained later in this section. The state I is visited only once during the life of a sample. After the device switches from this state to A, state I is never visited again.

To explain the bistable switching behavior, we will assume that the device was left in the low-conductance state B when power was switched off. The reader will understand that the same model holds if the device had been left in the high-conductance state A. The majority carriers causing transport through the quantum wires are electrons. This was verified with capacitance–voltage spectroscopy in the past.[3]

In Fig. 2(a), we show the equilibrium energy-band diagram along the length of a cylindrical CdS wire when the device is in state B. There are *unfilled* electron trap states at the semiconductor/alumina barrier interface that are indicated by the short lines in the diagram. They are above the Fermi level (determined by the contacts) and therefore unfilled with electrons. Application of a small *forward* bias bends the bands and causes some current to flow. The Au contact makes a nearly Ohmic contact with the semiconductor so that the carriers from the Au contact can easily tunnel through the narrow triangular conduction-band barrier at the Au/semiconductor interface and arrive at the alumina barrier. Once there, they are thermionically emitted over the barrier to the Al contact. This is the mode of conduction in state B. The bottleneck to conduction (the region that dominates the resistance of the structure) is the alumina barrier layer. As

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long as the traps states are unfilled with electrons, the barrier is high, the current is small, and the device is in the low-conductance state B. This situation is shown in Fig. 2(b).

When the bias is increased to V_{ON}, the band bends just enough that the lowest interface trap state energy approaches within a kT energy of the quasi-Fermi level and gets filled with electrons (kT=thermal energy). This situation is shown in Fig. 2(c). This leads to a negative surface charge density ρ_s forming at the interface of the semiconductor and alumina. The charges contributing to ρ_s (namely, the charges captured by the interface traps) flow in from the Au contact on the left. Nothing flows in from the right since the alumina barrier is fairly opaque and does not allow any appreciable current through it. As the trap state is filled with electrons and ρ_s increases in magnitude, the electron concentration n at the interface increases. Since

$$E_F - E_c = kT \ln(n/N_c), \tag{1}$$

where E_F is the local Fermi level, E_c is the conduction-band edge, and N_c is the effective density of states in the conduction band (for this "qualitative" discussion, we will not differentiate between Boltzmann and Fermi–Dirac statistics), therefore, an increase in the electron concentration at the interface pulls the conduction-band edge at the interface further down below the Fermi level to increase $E_F - E_c$. This pulls the next interface trap level down below the Fermi level and it gets filled with electrons. This increases ρ_s even more, resulting in more band bending at the interface and more trap states getting pulled down below the Fermi level to get filled. Thus, a chain reaction ensues. Traps are rapidly filled till no more empty trap states are left. The system quickly goes from the energy diagram in Fig. 2(c) to Fig. 2(d). Note that the interface charge screens the electric field in the *bulk* of the semiconductor, so that electric field in the bulk actually decreases with increasing ρ_s, but the electric field at the *interface* increases because of increased band bending to accommodate more interface charges.

Once the state in Fig. 2(d) is reached (and it is reached quite abruptly because of the chain reaction), the barrier is significantly lowered and the thermionic emission current increases tremendously since it depends exponentially on the barrier height. Simultaneously, tunneling through the barrier can also increase tremendously. At this point, the voltage over the sample is V_{high}, and we have switched to the high-conductance state A from the low-conductance state B.

The time required for charges to flow in from the Au contact (transit time through the semiconductor) plus the time required to fill the traps (determined by the capture cross section of the traps and trap density) is the time required to switch from the low- to the high-conductance state.

Once in the high-conductance state, the trapped charges at the interface cannot escape through the alumina barrier layer by tunneling (since this barrier is quite opaque), nor can they travel against the potential gradient to the Au contact on the left. Therefore, they remain trapped in the triangular potential well at the interface and the high-conductance state A persists for a long time until we loose the trapped charge by some vestigial tunneling through the barrier and some thermionic emission. This process takes at least 1 yr. This is the origin of the nonvolatility in the high-conductance state. In the low-conductance state, on the other hand, the trap states are above the quasi-Fermi level and cannot get filled spontaneously. This makes the low-conductance state nonvolatile, as well.

The storage time in the high-conductance state is determined by a number of parameters, including the conduction-band offset between CdS and alumina, density of traps, energy distribution of traps, band bending in the semiconductor, and temperature. Not all of these quantities are known at this time, so that we cannot estimate this quantity theoretically. The storage time during the low-conductance state also depends on the energy distribution of the traps and the temperature.

An interesting experimental observation was that the storage time in the high-conductance state seems to depend strongly on how narrow the nanowire is. We have made two distinct sets of samples, one using anodization of alumina in sulfuric acid (see Ref. 2 for the fabrication procedure), which leads to nanowires with a diameter of 10 nm, and the other using anodization in oxalic acid that leads to nanowires with diameter of 50 nm. The latter set showed no discernible bistability, even after testing many samples of this set. We believe that this happens because the bistability is not sufficiently long lived for observation in these samples. In other words, the memory effect is too volatile in 50-nm diameter wires. Because narrow wires (10 nm) result in nonvolatility and wider wires (50 nm) do not, we find that small size is important. We cannot identify precisely why smallness is important. It may be that in wider samples there are leakage paths through the barrier layer (effective shorts), which cause the trapped charges to drain out quickly, making the high-conductance state short lived. At this time, the origin of the size dependence of the storage time remains a mystery.

So far, we have explained how switching from B to A takes place. In order to switch back from A to B, the interface charges contributing to ρ_s must be drained and the traps emptied. If we apply a very high forward bias, we may ultimately bend the aluminum oxide barrier enough that the charges can tunnel out (or thermionically emit) across the barrier to reach the aluminum contact. However, we never apply such a large bias to avoid sample heating. Therefore, the device cannot switch from the high-conductance state A to the low-conductance state B *directly* under forward bias. We have to first apply a reverse bias and then switch the device off.

When the bias is reversed, the bands bend in the opposite direction. At low reverse bias, the trapped charge cannot escape through the alumina barrier, nor can it flow out in the other direction to the Au contact since it is trapped in the triangular well at the interface. As long as the trapped charge is there, the alumina barrier is held low and therefore the device is in the high-conductance state C. This situation is shown in Fig. 2(e). However, when the reverse bias is large enough and the bands in the semiconductor bend so much that the triangular potential well becomes too flat to contain the charges, the trapped charge ρ_s can flow out to the left Au contact. At this point, when the reverse voltage is V_{OFF}, we loose the interface charge. Since it is the interface charge that

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keeps the alumina barrier low, loss of this charge raises the barrier again and causes the device to revert back to the low-conductance state D. Thus, we can switch to the low-conductance state D from the high-conductance state C. Thereafter, if the voltage polarity is flipped and the device is forward biased, we will end up in the state B since the barrier remains high. This explains how one can switch from A to B.

The time to switch from the high-conductance state C to the low-conductance state D depends on the time required to release the trapped charges, plus the time required for these charges to drift and diffuse through the semiconductor to the Au contact. We have measured this time, and the details will be reported in a different publication.

Finally, the model should explain why the magnitudes of V_{ON} and V_{OFF} are very different. V_{ON} is the voltage that must be applied on the sample to pull the first trap level down to within a kT or so of the Fermi level at the CdS/alumina interface. V_{OFF}, on the other hand, is the reverse voltage that must be applied on the sample to tilt the conduction-band notch in CdS, at the interface with alumina, just enough to let the trapped charges escape. Since these voltages depend on different quantities, they are expected to be significantly different. The quantities that determine V_{ON} are temperature dependent so that V_{ON} has significant temperature dependence. On the other hand, V_{OFF} is relatively temperature independent. At room temperature, V_{ON} is about 40 V in the samples we have measured,[2] while V_{OFF} is 1–2 V.[2] By raising the temperature, we can reduce V_{ON} and bring it closer to V_{OFF}. This is discussed in more detail in Sec. V.

The above model *qualitatively* elucidates the bistability and the observed $I-V$ characteristic. It is a phenomenological model and obviously cannot be used to extract "quantitative" data. However, based on this model, we can estimate some limits.

A. Trap density

One quantity that will be of interest to know is the trap density responsible for the bistability and how many traps participate in each nanowire. We can estimate a lower limit on the trap density as follows.

Note that the voltage V applied on the sample is always the sum of the voltages dropped over alumina and CdS. If we assume that the alumina contains no charges, then Poisson's equation dictates that the electric field in the alumina is spatially invariant. At the threshold of switching from the low- to the high-conductance state [see Fig. 2(c)], the voltage across a nanowire is V_{ON} given by

$$V_{ON} = V_{CdS} + E'_i x_i, \tag{2}$$

where V_{CdS} is the voltage dropped over the CdS, E'_i is the (constant) electric field in the alumina and x_i is the thickness of the alumina. Since at this point, there is still no interface charge, $\varepsilon_s E'_s - \varepsilon_i E'_i = 0$, where E'_s is the interface electric field in the CdS (at the interface with alumina), and ε_s and ε_i are the dielectric constants in the semiconductor and alumina. Therefore, Eq. (2) can be recast as

$$V_{ON} = V_{CdS} + (\varepsilon_s/\varepsilon_i) E'_s x_i. \tag{3}$$

After the switching is complete and the device is in the high-conductance state [corresponding to Fig. 2(d)], the electric fields in the semiconductor and alumina at the interface are related by

$$\varepsilon_i E_i - \varepsilon_s E_s = \rho_s, \tag{4}$$

where E_s and E_i are the electric fields at the interface on the semiconductor and alumina side, respectively. The voltage V_{high} on the device is given by

$$V_{high} = V'_{CdS} + (\varepsilon_s E_s - \rho_s) x_i/\varepsilon_i, \tag{5}$$

where we have used Eq. (4) to relate the electric field in the alumina to the interface field in CdS. Obviously, $E_s > E'_s$ and $V'_{CdS} > V_{CdS}$. Therefore,

$$\rho_s > \varepsilon_i (V_{ON} - V_{high})/x_i. \tag{6}$$

In Ref. 2, V_{ON} was measured to be 40 V and V_{high} was 10 V. The relative dielectric constant of alumina is about 4 and the thickness of the alumina barrier layer was determined in the past by high-resolution transmission electron microscopy (TEM) to be 20–30 nm.[6] Therefore, we estimate that $\rho_s > 3.54 \times 10^{-6}$ C/cm^2. If we assume that each trap is singly charged, then this corresponds to a trap density of $n_{trap} = 2 \times 10^{13}$/cm^2. Since the density of nanowires is about 5×10^{11}/cm^2, the number of traps in each nanowire is about 40. Therefore, we observe an effect associated with about *40 trapped electrons* in each nanowire.

B. Band bending and barrier lowering caused by trapped charges

From the estimated concentration of trapped charges, we can roughly estimate the amount of band bending or barrier lowering caused by these charges. They reside in a discontinuous quasi-two-dimensional layer at the interface of CdS and alumina. Assuming that only one subband is filled, we find that at the interface, the conduction-band edge E_c is below the quasi-Fermi level in the left contact E_{FL} by [see Fig. 2(d)]

$$n_{trap} = \frac{4\pi m^*}{h^2}(E_{FL} - E_c), \tag{7}$$

where $4\pi m^*/h^2$ is the two-dimensional density of states.

Since the effective mass of electrons in CdS is 0.21 times the free-electron mass,[7] we find that $E_{FL} - E_c = 71$ meV.

In equilibrium state, there are hardly any carriers in CdS, so that at best the Fermi level is close to the conduction-band edge of CdS. Therefore, the trapped charges lower the barrier by at least 71 meV ($\cong 3kT$) by causing band bending. This causes the thermionic emission current to increase by a factor of $e^3 \approx 20$. The tunneling current also increases. The latter is by far the dominant effect since the current actually increases by a factor of 10^4.

V. TRANSPORT BEHAVIOR IN THE TWO CONDUCTANCE STATES

Whenever we measure the conductance of a sample, either in the off state or in the on state, we always measure the

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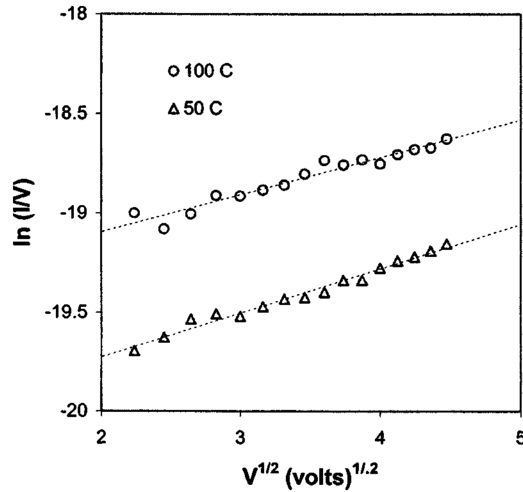

FIG. 3. The typical $I-V$ characteristics under reverse bias in the low-conductance state (characteristic "D"), measured at two different temperatures. The dominant conduction mechanism at high reverse bias voltages appears to be the Poole–Frenkel emission from traps in the alumina.

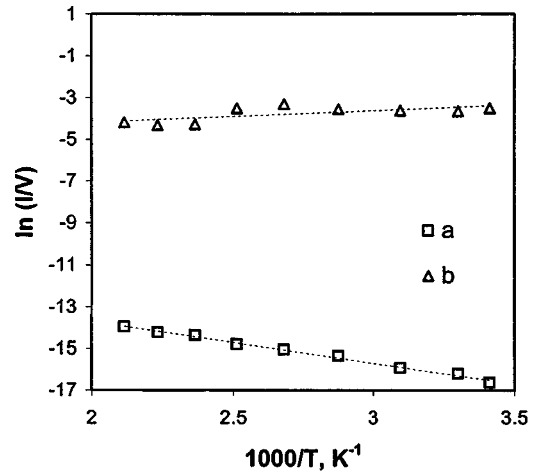

FIG. 4. Temperature dependence of (a) reverse bias low conductance (in characteristic "D") at a reverse bias voltage of −10 V, and (b) forward bias high conductance (in characteristic "A") at a forward bias voltage of 0.25 V. The activation energy of the traps estimated from curve a is 0.17 eV.

conductance of two "resistors" in parallel. One is the resistor composed of the nanowires. The other is the resistor composed of the surrounding alumina matrix, which also makes electrical contact with the contact pads [see Fig. 1(a)]. When the nanowires are in the high-conductance (on) state, we can ignore the second resistor since it has a much higher resistance. However, when the nanowires are in the low-conductance (off) state, the second resistor cannot be ignored and, in fact, may have lower resistance than the nanowires, so that it could become dominant. To investigate this possibility, we have measured the temperature dependences of the $I-V$ characteristics in both the high- and the low-conductance states using a thermostatic chamber with a temperature range of 20–200 °C.

A. Low-conductance state

The typical measured $I-V$ characteristics in the low-conductance (off) state under reverse bias (characteristic D) are shown in Fig. 3. If the nanowires are the dominant transport path, then current will flow mostly via thermionic emission over the barrier layer or tunneling. Otherwise, current will flow through the alumina. In order to resolve between these two possibilities, we have plotted the current–voltage characteristics in coordinates $\ln(I/V)$ vs $V^{1/2}$. At high reverse bias voltages, the characteristic in Fig. 3 is linear. This is not consistent with anything except Poole–Frenkel emission from the traps in the alumina. If tunneling or thermionic emission was dominant, then the temperature dependence will be very different (see Ref. 7 for the temperature dependences of various possible conduction processes through an oxide). Therefore, we can conclude that in the off state, the major conduction is through the alumina and not the nanowires. This means that in the off state, we do not even probe the nanowires; we are probing the alumina instead. The nanowires are switching the device from one state to another by cutting in and out of conduction. This is why we call this device "nanowire memory."

A second conclusion that we can draw is that the traps in the alumina tend to emit via the Poole–Frenkel mechanism. In the Poole–Frenkel emission, the $I-V$ relation is[7]

$$I \sim V \exp[(q/\pi\varepsilon_i d)^{1/2} V^{1/2}/kT - q\varphi/kT], \tag{8}$$

where d is the thickness of the effective potential barrier surrounding a trap and φ is the activation energy of the trap. This relation nicely fits the observed $I-V$ characteristics *at high reverse bias voltages*.

The significance of identifying the precise emission mechanism is the following. When the device switches from the on state to the off state, the traps must emit the captured charges. This process will determine the time to switch off the device. In order to engineer this time, we need to establish the precise mechanism by which the traps (in either bulk alumina or those at the interface with CdS) release the charges. If it happens to be the Poole–Frenkel mechanism, then we may be able to shorten this time by raising the temperature, although that will also adversely affect the nonvolatility. We are currently investigating this scenario.

B. Temperature-dependent transport in the off state, trap barrier, and trap energy

We can estimate the thickness of the effective potential barrier that traps electrons in a trap from the slope of the lines in Fig. 3, by fitting the lines with Eq. (8). The value we obtain is $d=2$ μm. This value is very close to the total thickness t of the alumina layer between the Al and Au contacts. This suggests that all of the alumina layers surrounding a trap act as barriers to a captured charge.

The temperature dependence of the reverse bias conductance (I/V) in characteristic D is shown in Fig. 4 (curve a) at a reverse bias voltage of −10 V. The activation energy of the traps, estimated from this curve, is $\varphi=0.17$ eV. Therefore, we expect a dominant trap level to reside about 0.17 eV below the conduction band of alumina. In order to verify this, we carried out Fourier transform infrared (FTIR) spectroscopy of the alumina matrix. We lifted off the matrix by dissolving the underlying aluminum in $HgCl_2$ and transferred

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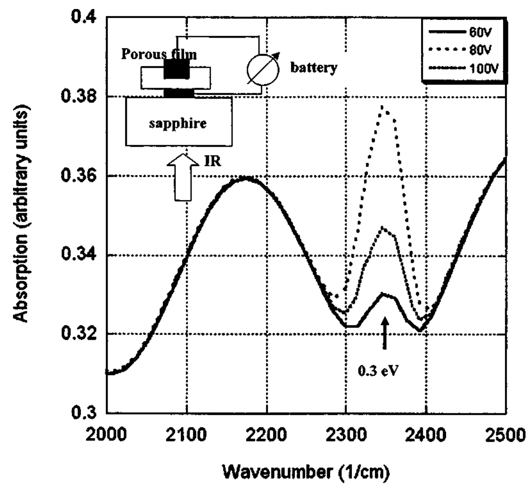

FIG. 5. Infrared absorption in anodic alumina before and after being stressed by high electric fields. The experimental setup is shown in the inset. There is a peak at a photon energy of 0.3 eV which appears only after stressing past 60 V. This voltage is dropped across the barrier layer, resulting in an average electric field of 20–30 MV/cm across this layer. We believe that this peak is indicative of the creation of traps in the barrier layer as a result of the high-field stressing. The height of this peak increases to a maximum at 80 V and then decreases slightly stabilizing at 100 V. The peak itself may correspond to the excitation of electrons from the generated trap state to the conduction band in alumina.

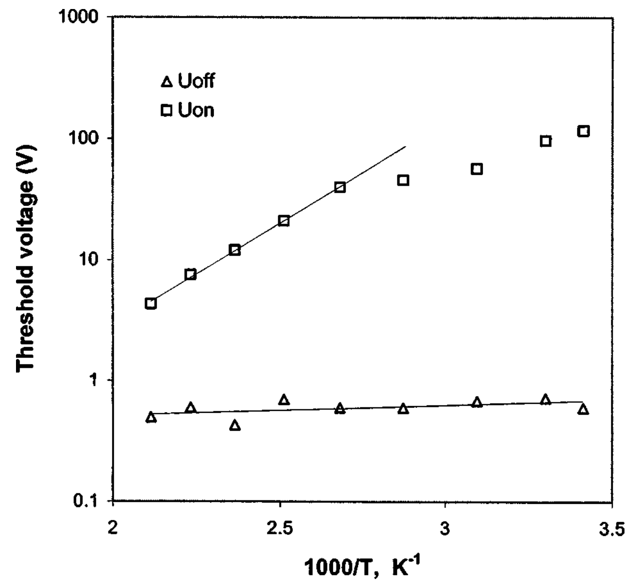

FIG. 6. Temperature dependences of the threshold voltages V_{ON} and V_{OFF}.

the matrix to a sapphire substrate. Contacts to the matrix were made on the top and at the bottom with silver paint before the transfer. We then monitored the infrared absorption while we applied a voltage between the contacts. This voltage is dropped across the "barrier layer" and stresses it. A sharp absorption peak close to 0.3 eV appeared when the applied voltage exceeded 60 V (see Fig. 5). Since the barrier layer width is 20–30 nm, the corresponding electric field across it is 20–30 MV/cm. The height of this peak increased when the voltage was increased to 80 V and then decreased slightly stabilizing at 100 V. Further increase of the voltage did not affect the peak height indicating that the electrical stress is creating a trap state below the conduction-band edge of alumina and infrared photons with an energy of 0.3 eV are exciting electrons from this trap state to the conduction band. We tested six samples and all but one showed this peak. The onset voltage varied between 60 and 80 V and the peak stabilized beyond 100 V in all cases. The peak always appeared at a center frequency corresponding to 0.3 V. This indicates that there is a major trap level about 0.3 eV below the conduction band of alumina. Since these samples are not compatible with traditional deep-level transient spectroscopy (DLTS) measurements, we cannot, at this time, probe deeper traps that are not accessible by FTIR spectroscopy.

The trap energy found from temperature dependence of reverse bias conductance (φ=0.17 eV) is only about one-half of that found from the infrared absorption (φ=0.3 eV). This discrepancy can be explained by the fact that the reverse bias is distorting the potential well associated with the traps, thereby making it appear shallower than it actually is.

C. Temperature-dependent transport in the on state

The temperature dependence of the conductance (I/V) in the high-conductance state under forward bias (characteristic A) is shown in Fig. 4 (curve *b*) at a voltage of 0.25 V. The conductance did not depend on temperature within our experimental accuracy. This is consistent with the model presented in Sec. IV. When the device is turned on, current flows via either thermionic emission over the barrier or tunneling [see Fig. 2(d)]. While the former is temperature dependent, the latter is not. Since we observe no perceptible temperature dependence, we conclude that the main mechanism of transport in the high-conductance state is by tunneling through the barrier.

D. Temperature dependence of V_{ON}

We have also studied the temperature dependences of the threshold voltages for switching. Under forward bias (characteristic B), we measured V_{ON} as a function of temperature and found that it decreases substantially with increasing temperature (Fig. 6). According to our model, V_{ON} is the voltage required to bring the first trap level within a kT or so of the Fermi level. Therefore, it depends on the energy distance between the first trap level and the Fermi level, as well as the thermal energy kT. The thermal energy alone will cause a linear temperature dependence of V_{ON}. The energy distance, on the other hand, is determined by the band bending in the semiconductor and the energy location of the trap level. Both these quantities are temperature dependent. The band bending depends on temperature since the Debye screening length in a nondegenerate semiconductor is temperature dependent. The trap level could also be temperature dependent. If new *empty* traps become available at higher temperatures (they could be filled at lower temperatures but empty at elevated temperatures) that could cause a temperature dependence of the trap level. Finally, the capture rate of a trap is $C=\sigma v_{th}$, where σ is the capture cross section and v_{th} is the thermal velocity. Since the latter depends on temperature, a trap, already close to the Fermi level but which did not have a sufficient capture rate at room temperature and therefore was not effective, can become effective at elevated temperatures. This can significantly reduce the energy distance between the

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first trap level and the Fermi level, which, in turn, will drastically reduce V_{ON}.

The dependence of V_{ON} on temperature is shown in Fig. 6 in coordinates $\ln V_{ON}$ vs $1/T$. At high temperatures, this dependence becomes approximately exponential and the characteristic activation energy of this dependence is found to be about 0.34 eV. It is important to note that V_{ON} can be as small as 5 V at elevated temperatures (as opposed to 40 V at room temperature). It is reassuring to find that the switching voltage can be lowered to a reasonable value ($\sim$5 V) by raising the temperature. This will also have the beneficial effect of reducing the switch off time by increasing the emission rate of traps, but it will impair the nonvolatility because it will increase charge leakage by promoting thermionic emission over the confining barrier.

E. Temperature dependence of V_{OFF}

Under reverse bias (characteristic C), we measured the temperature dependence of V_{OFF}, which is plotted in Fig. 6 in coordinates of $\ln(V_{OFF})$ vs $1/T$. The activation energy of this dependence is too small to be measured reliably and V_{OFF} does not appear to depend on temperature within the experimental accuracy we can achieve. This is also consistent with the model in Sec. IV. The device is turned off by causing sufficient band bending in the semiconductor to allow the trapped interface charges to escape to the Au contact. The band bending has a temperature dependence in a *nondegenerate* semiconductor (as mentioned before) because the Debye screening length depends on temperature. However, in a degenerate semiconductor, the band bending is determined by the Thomas–Fermi screening length rather than the Debye screening length. The Thomas–Fermi length is independent of temperature. In the presence of trapped charges, the semiconductor conduction band may be pulled well below the Fermi level [as shown in Figs. 2(d) and 2(e)] making it degenerate. In that case, we do not expect significant temperature dependence of the band bending.

VI. CONCLUSIONS

We have proposed and experimentally tested a model to explain an electronic bistability observed in electrochemically self-assembled nano wires embedded in an anodic alumina matrix. This bistability effect is robust, repeatable, and very long lived. It has applications in nonvolatile memory leading to extremely high-density static random access memory (SRAM).

Within the framework of the model, we have established transport mechanisms in the on and off states, estimated a lower limit on the number of traps per nanowire that cause the bistability effect, identified a likely trap discharge mechanism, and carried out measurements to establish the temperature dependence of the threshold voltages required to switch the device from one state to the other. We have shown that the threshold voltage for switching the device off (which is $\sim$40 V at room temperature) can be reduced to 5 V by raising the temperature to 200 °C, while the threshold voltage for switching the device on (which is only 1–2 V at room temperature) is more or less temperature independent.

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