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Tuning of electrical properties in InAlN/GaN HFETs and $Ba_{0.5}Sr_{0.5}TiO_3$/YIG Phase Shifters

Jacob H. Leach

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VIRGINIA COMMONWEALTH UNIVERSITY

Tuning of electrical properties in InAlN/GaN HFETs and $Ba_{0.5}Sr_{0.5}TiO_3$/YIG Phase Shifters

Jacob H. Leach

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Abstract

Engineers know well from an early point in their training the trials and tribulations of having to make design tradeoffs in order to optimize one performance parameter for another. Discovering tradeoff conditions that result in the elimination of a loss associated with the enhancement of some other parameter (an improvement over a typical tradeoff), therefore, ushers in a new paradigm of design in which the constraints which are typical of the task at hand are alleviated. We call such a design paradigm "tuning" as opposed to "trading off", and this is the central theme of this work. We investigate two types of microwave electronic devices, namely GaN-based heterostructure field effect transistors (HFETs) and tunable ferroelectric-ferrite-based microwave phase shifters. The "tuning" associated with these types of devices arises from the notion of an optimal 2DEG density, capable of achieving higher performance in terms of electron velocity and enhanced reliability in the case of the HFET, and the coupling of ferroelectric and ferrite materials in tunable microwave phase shifters, capable of achieving high differential phase shifts while at the same time mitigating the losses associated with impedance mismatching which typically arise when the phase is tuned.

Promises and problems associated with HFET devices based on the intriguing InAlN/GaN material system will be described. We focus on the fundamental problem associated with the induction of the large density of carriers at the interface, namely the disintegration of an excess of longitudinal optical phonons (hot phonons) in the channel. We use microwave measurements in conjunction with stress tests to evidence the existence of an optimal 2DEG density wherein the hot phonon effect can be "tuned," which allows for enhanced high frequency performance as well as device reliability.

Next, we focus on the design, fabrication, and measurement of tunable phase shifters consisting of thin films of $Ba_xSr_{1-x}TiO_3$ (BST), which has the advantage of having high dielectric tunability as well as relatively low microwave loss. We discuss the design, fabrication, and measurement of a simple coplanar waveguide (CPW) type of phase shifter as well as a more complicated "hybrid" phase shifter consisting of a ferrite (YIG) in addition to BST. The use of such a bilayer allows one to "tune" the impedance of the phase shifters independently of the phase velocity through careful selection of the DC biasing magnetic fields, or alternatively through the use of an additional piezoelectric layer, bonded to YIG whose permeability can then be tuned through magnetostriction.

1. Introduction

The ability to perform a task in such a way as to squeeze the highest level of performance from the undertaking is a central theme in the design of any system. The design of electronic devices is no different and engineers know well from an early point in their training the trials and tribulations of having to make tradeoffs in order to optimize one performance parameter for another. Discovering tradeoff conditions that result in the elimination of a loss associated with the enhancement of some other parameter (an improvement over a typical tradeoff), therefore, ushers in a new paradigm of design in which the constraints which are typical of the task at hand are alleviated. Such are the discoveries that "change the game" and future endeavors in designing solutions for the task at hand can be closer to achieving a whole solution, wherein the old tradeoffs no longer yield advances in one parameter at the expense of another. In a word, "tuning" of performance parameters as opposed to "trading off" of parameters are the result of the game changing discoveries.

"Tuning" of performance parameters is the central theme of this work. Specifically, we will investigate two types of microwave electronic devices, namely GaN-based heterostructure field effect transistors (HFETs) and tunable ferroelectric-ferrite-based microwave phase shifters. The "tuning" associated with these types of devices arises from the notion of an optimal 2DEG density, capable of achieving higher performance in

terms of electron velocity and enhanced reliability in the case of the HFET, and the coupling of ferroelectric and ferrite materials in tunable microwave phase shifters, capable of achieving high differential phase shifts while at the same time mitigating the losses associated with impedance mismatching which typically arise when the phase is tuned.

In the first section of this thesis, we will first outline the theoretical expectations and our experimental results for HFET devices based on the intriguing InAlN/GaN material system, followed by a discussion of the technological problems associated with InAlN compounds and the fundamental problems associated with the induction of the large density of carriers at the interface, namely the disintegration of an excess of longitudinal optical phonons (hot phonons) in the channel.[1] Evidence for the existence of an optimal 2DEG density, well below that which are typically achieved in an InAlN-based structure, will be presented. We use microwave measurements in conjunction with reliability tests to further demonstrate the fact that the high carrier density in InAlN-based HFETs is in fact detrimental to device performance and as well bodes poorly for the device's reliability. Specifically, we extract the intrinsic transit times of operating devices at various gate voltages, thereby demonstrating that at the optimal gate voltage (carrier density) a maximum transit time can be obtained. Additionally, we demonstrate the importance of hot phonons on the reliability of the devices as we show that HFET device degradation rates are correlated with the carrier density in identical devices through the gate bias.

The second section of the thesis consists of the design, fabrication, and measurement of tunable phase shifters. These tunable phase shifters consist of thin films of ferroelectric

materials, which generally show a high dielectric permittivity that can be controlled by application of small DC bias voltages[2] to give rise to small, fast, and cost effective devices. We employ $Ba_xSr_{1-x}TiO_3$ (BST),[3,4] which is one of the most popular ferroelectric materials, and has been utilized in the demonstration of various tunable microwave components including phase shifters,[5,6] resonators,[7] and filters.[8] BST has the advantage of having high tunability as well as relatively low microwave loss. We will discuss the design, fabrication, and measurement of a simple coplanar waveguide (CPW) type of phase shifter based on thin films of BST. Additionally, we will demonstrate more complicated phase shifters consisting of a ferrite/ferroelectric phase shifter wherein the characteristic impedance of the phase shifter is maintained through a careful selection of the DC biasing magnetic fields as well as through the use of a piezoelectric layer, bonded to a ferrite material whose permeability can be tuned through magnetostriction. The hybrid ferrite/ferroelectric design addresses the inherent problem of changing phase shift (through a change in the dielectric permittivity) in turn changing the characteristic impedance of the device. The use of the ferrite/ferroelectric device can result in phase shifting while maintaining impedance matching.

2. The InAlN/GaN HFET

Heterostructure field effect transistors (HFETs) are transistors in which a semiconductor is epitaxially grown on another semiconductor with a different bandgap. Carriers from the wide bandgap layer can then diffuse into the narrower bandgap layer, where they are confined in a quantum well, resulting in transport in only 2-dimensions. The motivation to design such devices as opposed to, e.g. MESFET or MOSFET types of devices is that much higher mobilities (and subsequently higher carrier velocities and switching times) can be achieved in the 2D-systems when the charge carriers in the device channel are physically separated from the donors from which they originated. Traditional HFETs based on the GaAs/AlGaAs system relied on the doping of the wide bandgap layer in order to form this 2D electron gas (2DEG) at the GaAs/AlGaAs interface. As such, these were initially termed modulation-doped field effect transistors (MODFETs). Since their inception, MODFETs based on GaAs have come to dominate the high frequency communications market, appearing in many defense, industrial, and consumer applications.

In the quest for increased power at microwave frequencies, wide bandgap semiconductors such as GaN and SiC were proposed for FET devices. These materials were expected to outperform their GaAs/AlGaAs predecessors due to the wide bandgaps (which yield very low intrinsic carrier densities which makes them suitable for operation at much higher

temperatures) and the high dielectric breakdown afforded by these materials (allowing higher drain biases and thus higher power to be achieved). Estimated breakdown fields could be extended to ~5×10^6 V/cm and ~3×10^6 V/cm for GaN and SiC, respectively. Due to these high breakdown fields, as compared to the mature GaAs-based devices (with a breakdown field of ~4×10^5 V/cm), devices based on the wide bandgaps offered the promise for >10-fold increase in operation voltages at microwave frequencies, in turn offering a similar increase in the available output power, when one simply considers the breakdown voltages alone (of course the high current in the (GaN-based) devices also contribute to the power that can be achieved). Although work proceeded on both GaN as well as SiC on basic MESFET or MOSFET types of devices for high power, the GaN system eventually became accepted as the material system of choice, due to the fact that HFET structures of AlGaN/GaN or InAlN/GaN could be grown with abrupt interfaces (as opposed to SiC which has no suitable wider bandgap sister layer with which to generate the HFET device), and currently enjoys some market penetration, particularly in high power military applications. Fortuitously, the band offsets afforded by AlGaN/GaN or InAlN/GaN heterointerface are additionally much larger than those which can be achieved in GaAs-based heterostructures (thus increasing the confinement of the electrons in the 2DEG, which would allow higher voltages to be applied without carriers escaping the potential well and additionally leads to lower output conductances). The HFETs described in this work are thus exclusively those of the GaN variety.

In addition to the benefits of wide bandgap and subsequent high dielectric breakdown, the high ionicity of the bonds in GaN affords GaN high spontaneous and piezoelectric polarization coefficients in the *c* direction, which is the technologically viable growth

direction. Thus, high (vertical) electric fields can be present in the device under zero bias conditions. This in turn can lead to very high densities of electrons in the induced 2DEG even without the modulation doping. As such, the term MODFET has fallen from fashion for these devices to be replaced with the more general term HFET. In addition to the polarization, the high ionicity results in very strong electron-phonon coupling, which turns out to be the ultimate performance-impeding parameter of the material, the final frontier of the device engineering, and the focus of this thesis.

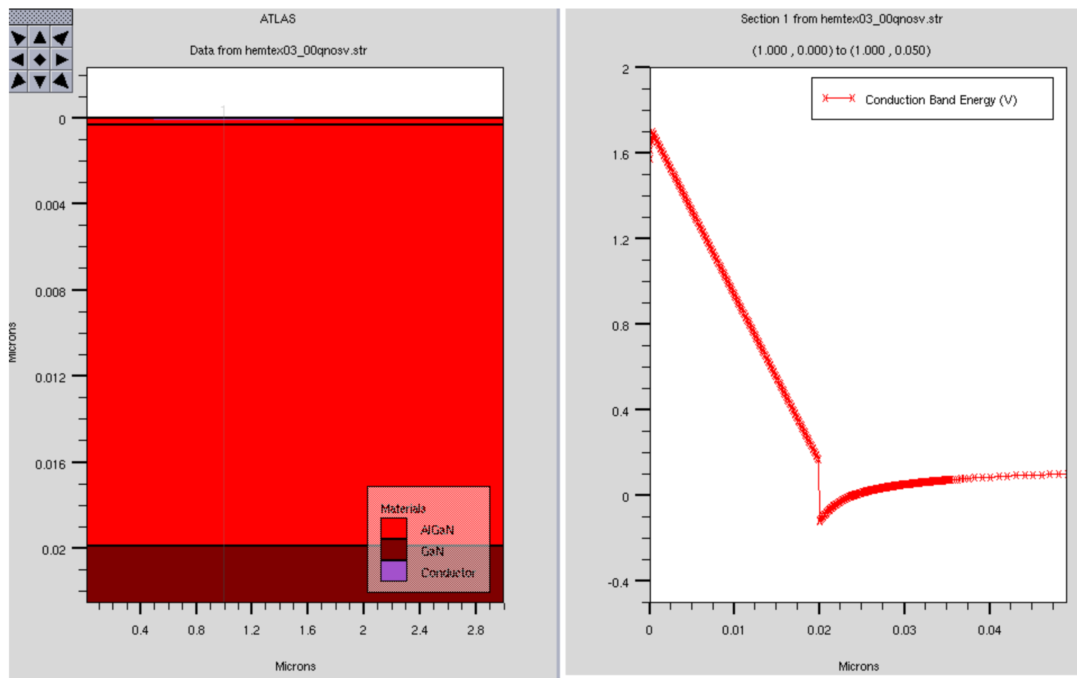


Figure 1. (Left) Schematic and (right) conduction band edge of the simple InAlN/GaN HFET structure.

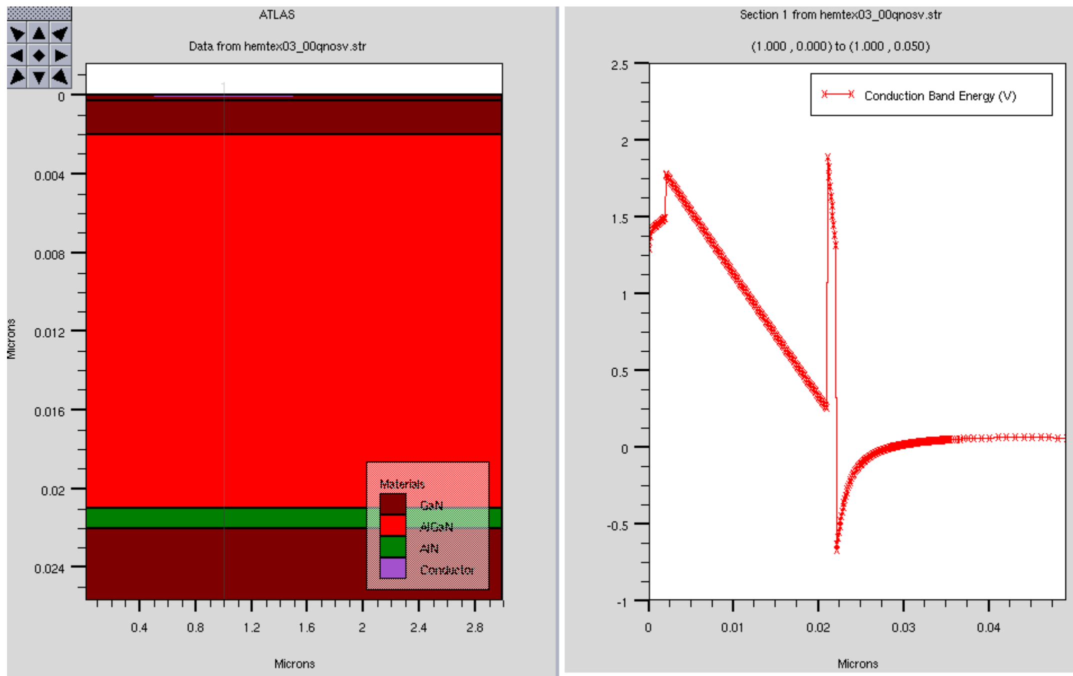


Figure 2. (Left) Schematic and (right) conduction band edge of the more typical GaN/InAlN/AlN/GaN HFET structure. The GaN cap layer is employed to reduce the ohmic contact resistance for the source and drain pads and the AlN spacer layer is employed to improve the transport in the channel. The effective band offset is increased when the AlN spacer layer is used and the scattering related to the inhomogeneity of the InAlN barrier is reduced as well.

The most simple as well as a more typical advanced structure and conduction band edge for an HFET based on GaN are shown in Figure 1 and Figure 2, respectively. Figure 1 shows the output from a Silvaco simulation of the cross-sectional structure (left) and the conduction band profile (right) for a simple InAlN/GaN (a very similar structure appears for an AlGaN/GaN heterostructure with the difference being a reduced band offset at the heterointerface) while Figure 2 shows the same for a more sophisticated GaN/InAlN/AlN/GaN heterostructure. The purpose of the additional GaN layer is to reduce the ohmic contact resistance while the AlN layer is included to enhance the confinement of carriers in the quantum well and enhance the mobility through the suppression of alloy scattering (arising from the wavefunction overlap from the well into the ternary barrier layer). Note that in both cases, the GaN channel is where transport

takes place, so to first order, the use of one barrier layer of another (i.e. AlGaN or InAlN) should only have effects on the confinement of the electrons in the well, the density of carriers in the well through the polarization charge, and any effects related to strain in the barrier layer.

As alluded to earlier, GaN-based HFETs exhibit very respectable performance in the high frequency-high power arena.[9,10] In fact, AlGaN-based HFET structures are already available commercially for high power, moderate frequency applications.[11] AlGaN became the barrier layer of choice mainly for technological reasons, it could be grown in typical molecular beam epitaxy (MBE) or metalorganic chemical vapor deposition (MOCVD) systems, and has currently reached a relatively modest state of maturity. Nevertheless, a great deal of research is currently focused on the substitution of the AlGaN barrier with an $In_xAl_{1-x}N$ barrier.[12,13,14,15,16,17,18] The motivation for such a shift when AlGaN/GaN HFETs are already near adoption is essentially the ability to induce an even larger carrier density (>2.5 x 10^{13} cm^{-2}) due to the relatively large difference in polarization at the interface where the 2-dimensional electron gas (2DEG) resides coupled with the larger conduction band offset afforded to InAlN as compared to typical AlGaN barrier layers, resulting in better carrier confinement in the quantum well.[19] Additionally, the pairing of InAlN with GaN is attractive because these materials can be lattice matched, circumventing strain related maladies that plague the AlGaN/GaN system.[20,21]

High sheet density coupled with respectable mobilities at room temperature (for example, n_s=2.6 x 10^{13} cm^{-2} and μ=1170 cm^2/V/s for a product of over 3x10^{16} $V^{-1}s^{-1}$)[22] promises high current density in InAlN channels. In fact, record current densities of 2.3A/mm and

2.8A/mm have been achieved with forward biased gates in DC and pulsed modes, respectively.[23] Regarding device scaling, Medjdoub *et al*. showed no change in sheet carrier density down to 9nm and operation down to 3nm InAlN barrier thicknesses, demonstrating the benefits in terms of scalibility of InAlN barrier layers over AlGaN barriers. Additionally, the same group[23] demonstrated FET performance at 1000ºC, which may have never been demonstrated in ANY device prior to this point and upon returning to room temperature after operation at up to 1000^{0}C, it appears that I_D, gate leakage, and pinchoff voltages are all preserved. These are the factors that motive the further development on InAlN-based HFETs. In the following we will discuss our own respectable or record results, discuss the specter of hot phonon lifetime, which will limit the ultimate performance of the HFETs, and provide experimental evidence of the ability to tune the hot phonon effects, resulting in enhanced microwave performance and reliability of InAlN-based HFET devices.

2.1. Promises in using InAlN

As mentioned in the introductory material above, the reason for the drive to InAlN-based FETs is primarily twofold. First, the InAlN can be grown at a particular mole fraction so that it is lattice matched to the GaN. This is important since the strain present in an a typical AlGaN-based HFET could be eliminated, which bodes well for the long term reliability of the devices.[24,25,26] Second, the bandgap of the lattice matched InAlN is actually larger than that of a typical AlGaN (with an Al mole fraction of 30%, the AlGaN bandgap is 4.19eV, while lattice matched InAlN has a bandgap of 5.04 using 16% In mole fraction and the values of bandgap and bowing parameter given by Vurgaftman

and Meyer[27]). Third, the spontaneous polarization charge for this lattice matched material is larger than that of a typical AlGaN barrier; for example, a typical $Al_{0.3}Ga_{0.7}N$/GaN interface would have a difference in spontaneous polarization of 0.017 C/m^2 while an $In_{0.16}Al_{0.84}N$/GaN interface would have a difference of 0.048 C/m^2, according to Vurgaftman and Meyer's recommended values of polarization. The larger bandgap results in an enhancement of the confinement of the carriers in the well, which would tend to allow more carriers to fill the well, keep those carriers in the well, thus keeping the output resistance of the device high. The larger number of carriers that tend to accumulate in the 2DEG results in larger sheet carrier densities and correspondingly larger current and power densities than those that can be achieved in the more mature AlGaN/GaN system. Finally, as one attempts to reduce the gate lengths of transistor devices, one must scale the thickness of the barrier layer or else suffer from short channel effects. In this vein, attempting to reduce the thickness of the AlGaN barrier suffers from the fact that the sheet carrier density decreases when the barrier thickness goes below about 20nm.[28,29] Attempts to increase the barrier thickness by increasing the mole fraction of Al in the AlGaN beyond 30% have serious technological challenges,[30] as well as suffer from continuing to increase the tensile strain in the AlGaN barrier layer. With increasing Al mole fraction from 30% to 100%, the critical thickness of AlGaN decreases from about 20-30nm to about 3nm.[31] Lastly, dipole scattering, present when the alloy disorder couples with the (piezoelectric) AlGaN does not exist in lattice matched InAlN.

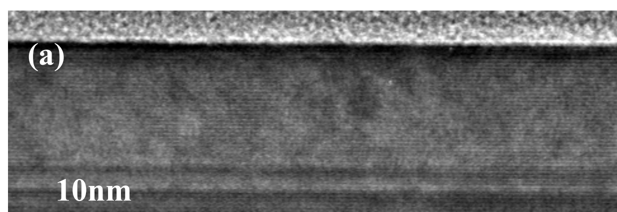
2.2. Problems with using InAlN

Despite all of these motivating factors in favor of using of an InAlN barrier as opposed to an AlGaN barrier, there are some serious challenges to achieving the high performance promised by the use of this barrier. Technological issues continue to plague the InAlN-based system. Typically In-containing nitride compounds must be grown at a relatively low temperature while Al-containing nitride compounds are grown at relatively high temperatures. Indium-containing compounds grown at higher temperatures suffer from In segregation and the formation of In-clusters in the layers.[28] These In-rich compounds are known to segregate toward dislocations, exacerbating the already nonuniform system. The local inhomogeneities in composition are problematic for a number of reasons. For example, a region of In-rich InAlN would have a lower bandgap than the surrounding InAlN, would have a lower polarization, and would be compressively strained as compared to GaN. This strain in turn would cause the piezoelectric polarization to again appear, and these effects coupled together would give rise to local inhomogeneties in the 2DEG density, yield regions of increased alloy scattering due to the enhanced penetration of the electron wavefunction into the barrier layer, and furthermore the issues of coupling of electrons to acoustic phonons through the deformation and piezoelectric potentials would rise up again. In short, the InAlN barrier layer would be best if it were uniform. For these reasons, we use growth temperatures of 750-800°C for the InAlN growth,[32] however the GaN and AlN layers are grown at relatively high temperatures (~1050°C) under a hydrogen environment. These high growth temperatures coupled with the fact that InAlN is typically grown under a nitrogen environment means that during the growth there is an interruption between the growth of the AlN spacer layer and the InAlN barrier layer. This growth interruption is the subject of serious scrutiny. During the interruption,

it seems that a layer of GaN may inadvertently be deposited from existing Ga inside the chamber and in particular on the sample holder. We have observed such a Ga-rich region in TEM analysis of our InAlN layers.

2.2.a. The Inadvertent GaN Interlayer

The inadvertent GaN layer can be observed in conventional TEM and is particularly evident in high-angle-annular dark-field (HAADF) scanning transmission electron microscope (STEM) images of the HFET structure, as shown in Figure 3(a) and (b), respectively. The bright-field image (a) reveals the presence of a ~2-nm-thick darker contrast region just above the lighter contrast AlN layer, whereas the HAADF STEM image (b) shows the characteristic lighter contrast associated with a higher atomic weight material. As revealed by the energy dispersive x-ray spectroscopy (XEDS) line profile in Figure 3 (c), this region unexpectedly contains a considerable quantity of gallium.[33] The fact that the parasitic layer is well defined with abrupt interfaces indicates that it is deposited during the time when the chamber is ramping its temperature and evacuating its residual gas from the levels using during the previous AlN spacer layer growth, in preparation for deposition of InAlN. That said, the existence of Ga in the InAlN barrier layer, resulting in our ternary barrier being in fact some sort of quaternary cannot be ruled out. This would have the effect of reducing the bandgap of the barrier as well as the difference in polarization, resulting in a reduced 2DEG density. Additionally, the barrier would no longer be lattice matched. Such problems have been observed by other groups as well.[34]



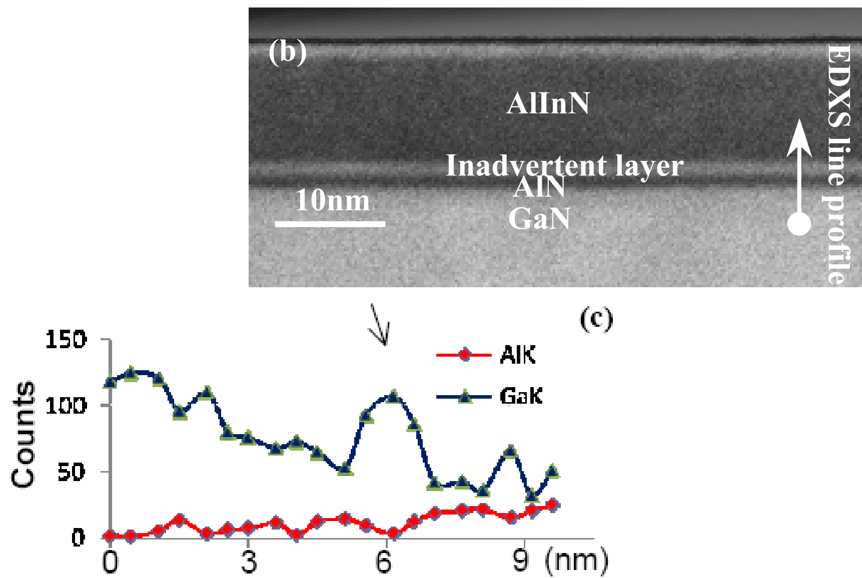


Figure 3. (a) Bright-field TEM image; (b) High-angle annular-dark-field (HAADF) scanning transmission electron microscopy (STEM) image; and (c) corresponding EDXS line profile of the InAlN/AlN/GaN region illustrating inclusion of the inadvertent Ga interlayer. The EDXS line profile demonstrates that the inadvertent layer contains considerable Ga.

In addition to be being undesirable for obvious controllability reasons, we have found that in some of our layers of InAlN, the sheet density as measured by the Hall effect is much lower that that which is predicted by the theory. This is expected as an inadvertent layer of GaN in such a location would constitute a quantum well, since the conduction band minimum of GaN is much lower than the neighboring AlN spacer and InAlN barrier layers. The effect of such an additional quantum well would be to effectively partition the electrons that would normally have filled the intentional triangular quantum well at the AlN/GaN (lower) interface. The percentage of electrons residing in the unintentional well depends critically on its thickness, the spontaneous polarizations of the constituent

materials, the strain state of the system, and the gate voltage (V_G). Table 1 shows ATLAS simulation results for the density of electrons in the intentional and unintentional quantum wells for various thicknesses of the unintentional interlayer at zero bias and assuming a Pt gate (with a workfunction of 5.6eV). The spontaneous polarization values taken from ref 35 are 5.62 x 10^{13}, 2.12 x 10^{13}, and 4.61 x 10^{13} e^-/cm for the AlN, GaN, and $In_{0.15}Al_{0.85}N$, respectively. Taking the AlN spacer layer to be fully strained induces an additional piezoelectric polarization of 2.90 x 10^{13} e^-/cm. The InAlN layer's polarization is assumed to have a bowing parameter of -4.37 x 10^{13} e^-/cm, and the composition of 15% In was used, which is closer to being lattice matched than the typically reported lattice matched composition of 17% for our (compressively strained) GaN on sapphire films.[36] The total concentration of electrons in the system slightly decreases while the fraction of electrons in the unintentional layer increases with the thickness of the unintentional well, as shown in Table 1. Moreover, any strain relaxation in the AlN spacer layer would reduce the polarization's piezoelectric component and tend to decrease the electric field in the inadvertent well, thereby increasing its carrier density. The unintentional GaN channel begins to fill appreciably with electrons for thicknesses ~1-2nm. The calculated conduction band edge and electron concentrations are shown in Figure 4 for the cases with no interlayer and a 2nm unintentional interlayer.

Thickness of GaN interlayer (nm)	**0**	**1**	**2**	**3**	**4**
Intentional 2DEG [with 20% relaxed AlN] (x 10^{13})	2.45 [2.41]	2.24 [2.21]	2.06 [1.91]	1.68 [1.55]	1.42 [1.31]

Unintentional [with 20% relaxed AlN] (x 10^{13})	-	2.24 [0.0]	0.11 [0.25]	0.48 [0.61]	0.74 [0.85]
% in Unintentional	-	0% [0%]	5.1% [11.6%]	22.2% [28.2%]	34.3% [39.3%]

Table 1. Calculated 2DEG density in the intentional and unintentional quantum wells as a function of the unintentional GaN interlayer thickness. The values in brackets represent the same assuming that the AlN is partially relaxed (20%). The electron population in the unintentional layer quickly increases when the AlN spacer layer relaxes.

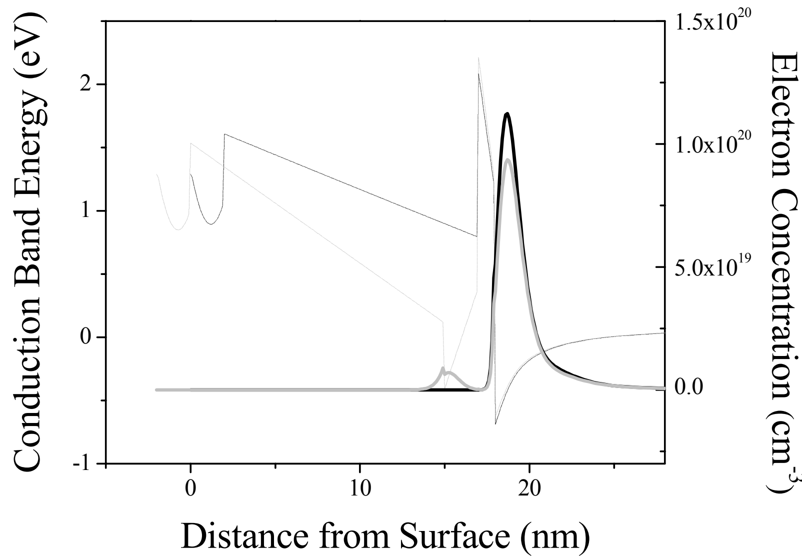


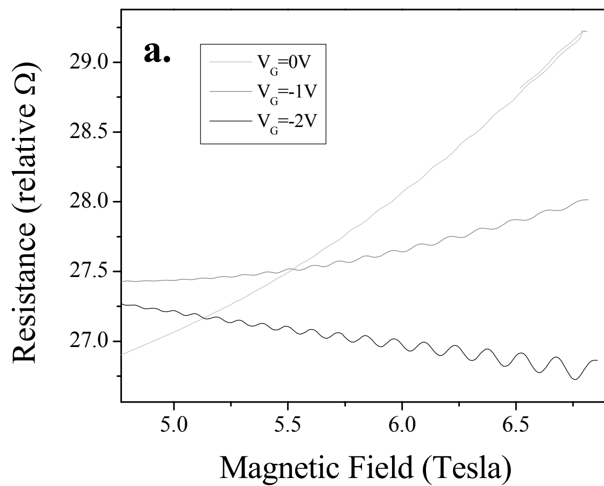
Figure 4. Calculated band diagrams (dotted lines) and electron concentrations (solid lines) at zero gate bias for the InAlN/AlN/GaN HFET structure with no unintentional GaN interlayer (black) and with a 2nm GaN interlayer between the AlN spacer and the InAlN barrier layer (gray). The plot for the structure which includes the 2nm GaN layer is shifted in such a way as to make the intentional triangular well at the AlN/GaN interface overlap.

We believe that the unintentional interlayer forms as a result of GaN being deposited on the sample holder during growth of the GaN buffer layer (3 μm-thick). After the AlN spacer layer is grown, we ramp down the temperature to 740°C and switch the carrier gas from H_2 to N_2. During this time (6.5 minutes), GaN deposited on the holder may migrate and be deposited onto the sample surface. Such a mechanism seems plausible considering

the abruptness of the unintentional GaN interlayer's interfaces, as shown in Figure 3. In order to test this possibility, we grew another structure wherein the growth was interrupted prior to the deposition of the spacer and barrier layers. The sample holder was then replaced with a clean (GaN free) one, and subsequently the growth was resumed with a 100 nm-thick GaN layer, followed by the AlN spacer, AlInN barrier, and GaN cap layers. The subsequent TEM analysis demonstrated that the unintentional GaN interlayer in this epilayer was much thinner (~1nm) than the interlayer unintentionally deposited when the growth was not interrupted. Of course, these findings also imply that there may be unintentional Ga being incorporated in all layers (i.e. the AlN and InAlN layers).
To delineate the impact of the inadvertent layer on conductivity, we performed longitudinal magnetoresistance and Hall measurements at magnetic fields up to 6.9 T on a gated Hall bar structure at 4.2 K. For gate voltages smaller than -1.5 V, we observe well-pronounced Shubnikov-de Haas (SdH) oscillations as shown in Figure 5(a). This is consistent with full depletion of the parasitic channel so that only the primary (intentional) 2DEG layer is present. At higher V_G (toward zero bias), the magnitude of the SdH oscillations decreases with bias while their period remains fixed, which appears to correlate with onset of the parasitic channel located between the 2DEG and the top gate . We could hardly resolve SdH oscillations for gate biases greater than -1V, where the population of electrons in the unintentional GaN layer is no longer negligible. The carrier density extracted from the period of the SdH oscillations (1.34×10^{13} cm^{-2} at V_G=-2V) agrees well with that obtained from the Hall measurements.

Figure 5(b) plots carrier densities (filled points) and mobilities (open points) derived from the Hall and magneto-resistivity measurements at each gate voltage. The squares in this

figure are taken from the "raw" magneto-transport data assuming a single electron species. However, mixed conduction effects are expected to arise at gate biases for which the unintentional parasitic channel becomes populated. To quantify this contribution, we treated the same magnetic-field-dependent Hall and resistivity data with the quantitative mobility spectrum analysis (QMSA), [37] which is able to delineate multiple conduction channels having differing mobilities. The stars in Figure 5(b) display the resulting QMSA densities and mobilities for the primary 2DEG channel at various gate biases, which are seen to be effectively unchanged from the "raw" results represented by the squares.



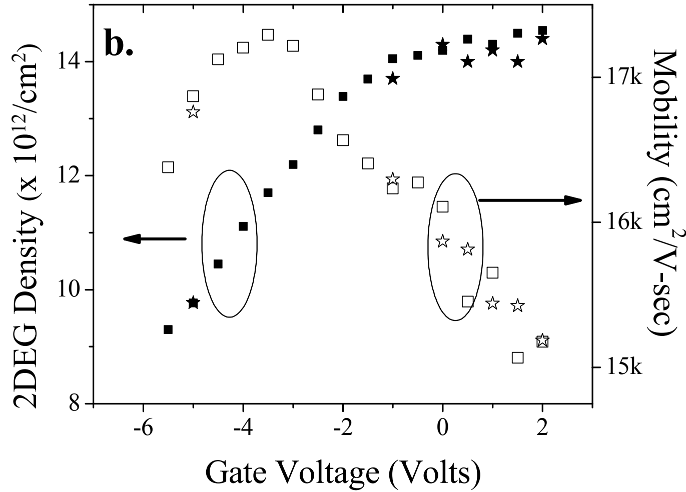
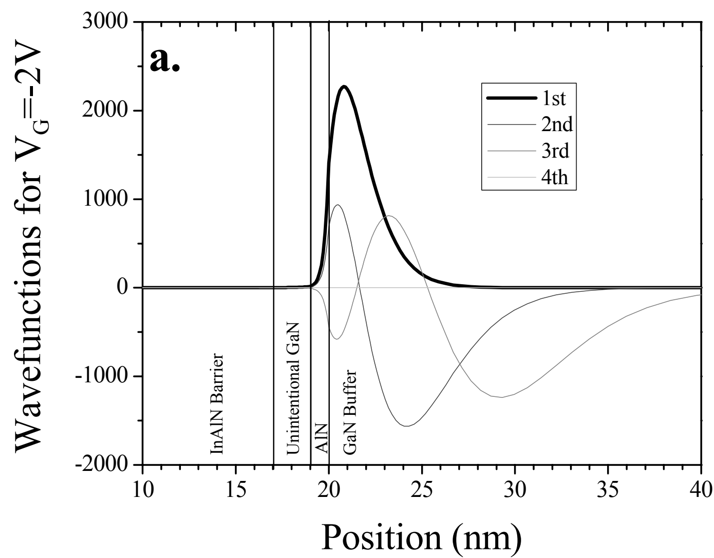


Figure 5. (a) Shubnikov-de-Haas oscillations for gate biases of -2V, -1V, and 0V (the 0V curve is offset for clarity). The oscillations are strongest when the parasitic channel is depleted at large negative biases, become weaker for -1V with the onset of parasitic conduction, and are barely discernable at all for 0V where the parasitic channel is more heavily populated. (b) Carrier density (solid points) and mobility (open points) for the InAlN-barrier HFET structure shown in Figure 1, as determined from gated Hall bar measurements. The squares are "raw" data (assuming no mixed conduction), while the stars are the intentional 2DEG layer's density and mobility as extracted from the quantitative mobility spectrum analysis (QMSA).

QMSA additionally determines that for zero and positive gate biases, but not $V_G \leq -1$V, a second electron species with very low mobility contributes in parallel to the primary high-mobility carrier. This finding is consistent with the bias-dependent SdH data, and also with the simulation discussed above, if the lower-mobility species is associated with electrons residing in the unintentional GaN interlayer. Since the mobility of the second population is quite low in relation to the maximum available magnetic field strength of 6.9 T (*i.e.*, $\mu B_{max} \ll 1$), QMSA cannot reliably extract its density and mobility separately but only the net conductivity corresponding to the density-mobility product. This additional conductivity contribution is found to increase by a factor of ~6 as the gate bias increases from 0 to 2 V. If we further take the parasitic channel's carrier density at zero

bias to be 5.1% of the total, as calculated by the simulation summarized in Table 1 for a 2-nm-wide interlayer, QMSA derives a mobility of 110 cm^2/Vs for that layer. Performing the same analysis with a channel width of 3 nm (22.2% of the carriers in the interlayer) implies a corresponding mobility of 21 cm^2/Vs. Such a low mobility in this range is expected inside the unintentional well, due to the large alloy potential of InAlN (compared to AlGaN)[38] and the large subsequent alloy scattering.[39,40] Typical Hall measurements would not capture the contribution by carriers populating the unintentional layer due to their very low conductivity (at most 0.25% of the total).

Despite the nearby presence of the parasitic layer, we expect the intentional channel to maintain its high mobility because its electron wavefunctions do not extend into the lower-quality region. Figure 6 illustrates simulated wavefunction distributions for the structure with a 2nm unintentional GaN interlayer at V_G = -2V and 0V. Under reverse bias, none of the four lowest energy levels reside in the parasitic channel, hence it is unpopulated. At zero bias, the second-lowest level resides in the unintended layer, although each wavefunction continues to reside in one layer or the other with negligible overlap. Furthermore, the enhanced screening from alloy scattering afforded by the additional GaN spacer layer may actually *improve* the overall mobility as previously demonstrated for an AlGaN/GaN/AlN/GaN structure.[41]



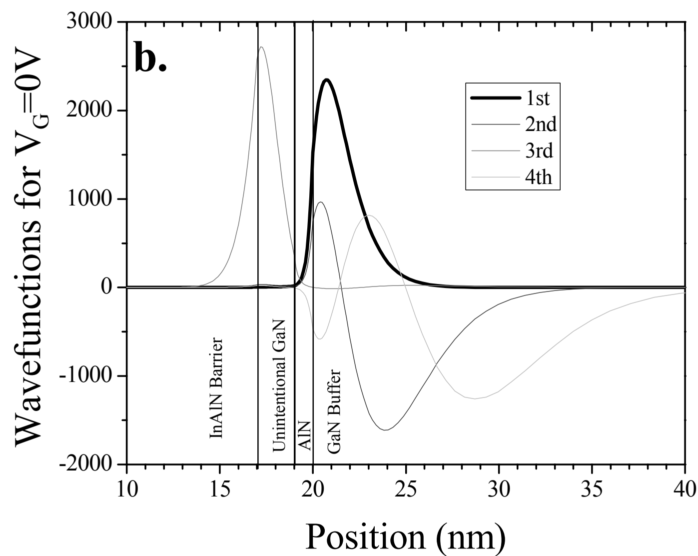


Figure 6. Wavefunctions for the InAlN/GaN/AlN/GaN heterostructure with a 2nm GaN interlayer at applied gate biases of (a.) -2 volts and (b.) zero volts. There is very little overlap, if any, between the wavefunctions associated with the two channels, therefore one would not expect the high electron mobility associated with the intentional 2DEG to be degraded appreciably when the second channel is populated.

2.2.b. The Real Lattice Matching Condition

Another issue with the InAlN/GaN system, perhaps on a more fundamental level is that the lattice matching condition is not precisely known as there is some scatter in the literature in values of the lattice parameters of the binaries, as well as uncertainty in the amount of deviation from Vegard's law (bowing). Additionally, the lattice matching condition will change depending on the lattice constant of the GaN layer in hand. As an example, we measured the photoluminescence (PL) spectra of our own GaN layers grown on sapphire substrates at 10K and compared it to that from a 250μm thick layer of freestanding bulk hydride vapor phase epitaxy (HVPE)-grown GaN in order to determine the residual strain in the underlying GaN buffer layer, Figure 7. The energy of the free A-exciton (FX_A) transition was found to be blue shifted by 21.8 ± 1 meV. This shift corresponds to a strain of -0.227 ± 0.009 % in the *a*-axis or 0.11 ± 0.05 % in the *c*-axis of GaN grown on sapphire, relative to the bulk, as evidenced in Figure 8. Using Vurgaftman and Meyer's "recommended" values[27] of the bulk *a* lattice parameters of 3.189, 3.112, and 3.545Å for the GaN, AlN, and InN binaries, respectively, and considering the bowing parameter of the *a* lattice constant of InAlN to be –0.01,[42] this amount of strain translates into a lattice matched composition (matching the *a* parameter) of x=15.8% for $In_xAl_{1-x}N$ barrier layers (we have assumed that the bulk layer has the aforementioned lattice parameter and is additionally strain free). If one were to disregard the strain present in the GaN after growth on sapphire substrates, using the above-mentioned values for the lattice constants of the binaries, one would expect lattice matching at x=17.4%. Therefore, it is clear that the strain in the underlying layer is important to consider when attempting to ascertain the composition required to match InAlN to the GaN layer in hand.

Furthermore, the picture is clouded somewhat when one considers the uncertainty in the lattice parameters of the binaries, particularly InN, as well as the uncertainty in the bowing parameters. For example, taking the values of the *a* parameters of the binaries to be 3.185, 3.111, and 3.5377 Å for GaN, AlN, and InN as done by Lorenz *et al.*, one obtains the lattice matched condition to be 17.0% and 15.3% on bulk GaN and strained GaN, respectively.

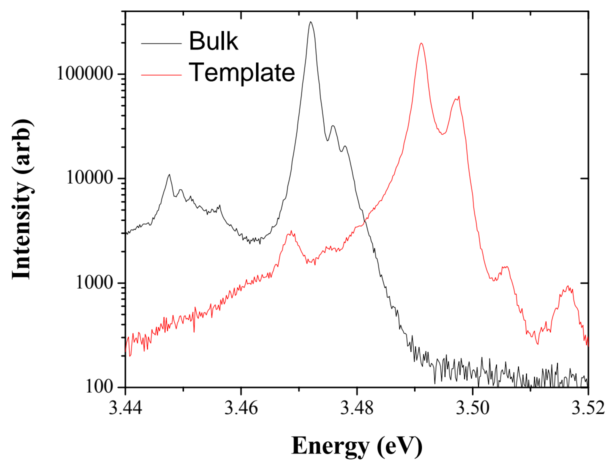


Figure 7. 4K PL data for bulk GaN and GaN on sapphire. The shift indicates strain in the layer. We assume that the bulk GaN layer is fully relaxed, which may not be strictly valid. The shift of 21.8meV corresponds to a shift in the lattice parameters of -0.2265% (*a* parameter) and 0.11% (*c* parameter).

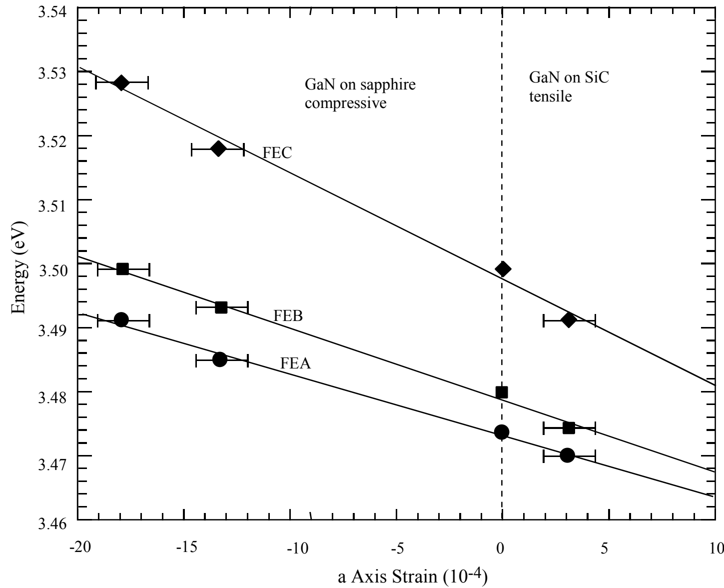


Figure 8. Shift in the free exciton binding energies as a function of the in-plane strain (the *a* lattice parameter). From 19.

2.3. Growth and Fabrication of InAlN-based Transistor

2.3.a. Growth of InAlN and determination of composition

Throughout these studies, we grew InAlN/AlN/GaN FET structures on both 2 inch c-sapphire (0001) substrates and bulk HVPE-grown Fe-doped GaN from Kyma Technologies, Inc., by using a vertical low pressure Metal-Organic Chemical Vapor Deposition (MOCVD) system. Trimethylgallium (TMGa), trimethylaluminum (TMAl), trimethylindium (TMIn), and ammonia were used as the Ga, Al, In, and N sources, respectively. Growth on (0001) sapphire substrates was initiated with a 270nm AlN buffer layer deposited at ~1050°C, followed by growth of ~3.7μm of GaN at 200 torr. Next an AlN spacer layer was grown at various pressures (30-120 torr) to thicknesses of 0.4-1.5nm. Next, the wafer was cooled down after the spacer layer deposition to 780-800 °C, and additionally the carrier and dilution gases were switched from H_2 to N_2 to grow

the InAlN barrier. The In composition in the barrier was controlled by growth temperature. Finally, a 2nm GaN cap layer was grown atop the barrier layer. When we grew on the bulk GaN[43], before loading into the MOCVD chamber, the substrates were first etched ~600nm in a SAMCO inductively coupled plasma (ICP) system with Cl_2 and Ar gases to remove the damaged surface layer caused by chemical mechanical polishing (CMP). Next, we cleaned in aqua regia, rinsed in deionized water, and loaded into the growth chamber. Prior to growth, the GaN substrates were additionally treated *in situ* with H_2 for 30 minutes under the protection of an NH_3 ambient at 900°C. After the H_2 treatment, which is estimated to remove an additional 50 nm of GaN surface layer, a 2 μm undoped GaN was deposited at a temperature of ~1000 ºC at 200 Torr. By developing this procedure, we removed the thin (silicon and oxygen-containing) layer at or near the regrowth interface, which could result in a parallel conduction channel as reported in reference 44. We believe that this layer appears as a result of the CMP process which the substrates undergo or simply as a result of being exposed to the atmosphere; the removal of this layer is critical for good HFET performance.

As mentioned above, the composition of the InAlN layers is difficult to ascertain due to the uncertainty in the lattice parameters as well as the bowing for the ternary. This means that X-ray diffraction (XRD) measurements are insufficient as an exclusive tool for determining the lattice parameter of an InAlN film. As an experiment we grew four layers using descending temperatures for the InAlN deposition, which we will call samples A, B, C, and D. We then performed XRD to estimate the composition and additionally, by resolving the thickness interference fringes we determined the barrier thicknesses to be ~20nm for each of the layers. The composition can be estimated

thorough a measure of the shift in the angle of reflection between the GaN (0002) peak and the InAlN peak in the 2θ-ω scan, which allows one to determine the InAlN *c* parameter through the Bragg relation, $n*\lambda = 2*d*\sin\theta$ where n is an integer, λ is the wavelength of the incident X-ray (1.5406Å for the Kα line of the copper target used in our system), *d* is the interatomic spacing (related to the *c* lattice parameter in this case, the value depends on which reflection we are observing (i.e. the (001) or (002) peak) and θ is the angle at which the diffraction peak occurs. Knowing the angle at which the GaN peak should occur (note that we must use a *c* GaN parameter of 5.1907Å, which takes into account the -0.2265% change in the lattice parameter due to (compressively) strained GaN on sapphire, see Figure 7 and the associated text) we can calculate the value of the *c* lattice parameter of the InAlN through the expression $c\Big|_{InAlN} = \frac{\sin\theta\big|_{GaN}}{\sin\theta\big|_{InAlN}} c_{GaN}$. We can then use this value of the *c* lattice parameter to estimate the composition of the InAlN layer assuming a bowing parameter of the *c* lattice parameter of –0.075. Of course, this method first assumes that the layers are fully pseudomorphic and free of strain; however in reality only a structure that is in fact lattice matched is free of strain. We do know, however that the layers B and C are in fact pseudomorphic from a reciprocal space mapping measurement conducted about the (102) axis, Figure 9. By using the *c* lattice parameters given by Vurgaftman and Meyer[27] (5.185, 4.982, and 5.703 for GaN, AlN, and InN, respectively), we estimated the In composition of the InAlN barriers for samples A, B, C, and D to be 10.5% 14.7%, 16.6%, and 21.7%, respectively. If we had used the values given by Lorenz *el al.* (taking the *c* parameters to be 5.188, 4.98, and 5.7037) we would have found layers A, B, C, and D to have compositions of 11.3%, 15.5%, 17.4%,

and 22.0% respectively. As such we consider sample “A” to be nearly lattice matched (under tensile strain), “B” to be closest to being lattice matched, sample “C” to be nearly lattice matched (under compressive strain), and sample “D” to be lattice mismatched (compressively strained). If we changed the InAlN bowing parameters of the *a* and *c* lattice constants to those reported in reference 45, we would have the lattice matching conditions (using lattice parameters from 27) of 20.1% and 18.3% (without and with the underlying strain of the GaN), with our layers having compositions of 9.6%, 13.4%, 15.2%, and 19.9%, thus sample D would be closest to being lattice matched. Considering our results as well as the grazing incidence refraction (GID) results reported in ref. 42 which showed contradictory behavior when the bowing parameters of ref. 45 were used in conjunction with their experimental data, our data are consistent with the bowing parameters of reference 42. In Section 2.4.c. Transient Measurements, we will return to these four layers where we will further elaborate on our technique to ascertain which layer, given a set of InAlN layers of comparable crystal quality, is in fact closest to being lattice matched.

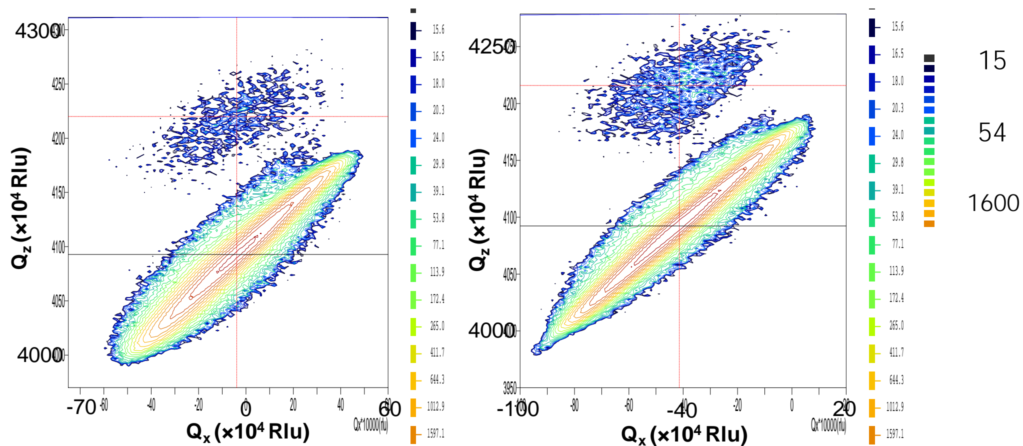


Figure 9. Reciprocal space maps of the (102) axis of (left) sample "B" (~15%, closest to lattice matched) and (right) sample "C" (~17%, slightly lattice mismatched, compressively). The InAlN (blue cloud) is pseudomorphic to the underlying GaN (intense rings).

2.3.b. Fabrication of InAlN HFETs

Fabrication of the InAlN HFETs consisted of the following: First, ohmic contacts were defined for the source and drain contacts. The standard procedure for ohmic contact deposition consists of first cleaning the wafers with acetone, methanol, and DI water for 3 minutes each, in an ultrasonic bath (called organic cleaning). This is followed by boiling the wafers in aqua regia (3HCl:1HNO3) for 10 minutes, rinsing copiously with DI water and blowing dry with nitrogen. Next, the wafers are covered with positive photoresist (spin at 5000 RPM, resulting in ~1.2μm of PR) baked for 5 minutes at 90°C, exposed to the UV source and developed. The contacts are then formed by evaporating Ti/Al/Ni/Au (30/100/40/50nm) (e-beam evaporation for Ti, Ni; thermal evaporation for Al, Au), followed by a liftoff in acetone and concluding with an additional organic cleaning. Next, the PR step is repeated, mesas are defined photolithographically, and etched (150nm) using an inductively coupled plasma (ICP) source with $SiCl_4/Cl_2/Ar$ chemistry to isolate the active regions of the devices. Rapid temperature annealing (RTA) is next conducted to alloy the ohmic contact. After another organic cleaning, gates are defined by another photolithography/liftoff procedure using Pt/Au for the gate electrode. We found that Pt contacts exhibit about an order of magnitude lower gate leakage current as compared to Ni-based contacts, similar to the results reported in ref. 46. The gate lengths range from 0.65 to 2μm with widths of 90, 170, and 290μm.

The annealing temperature and metal thickness are two major factors which significantly affect the ohmic contact resistance; low resistance source and drain ohmic contacts are

key to obtaining the highest saturation DC drain current and transconductance of the completed devices, and additionally are required for good RF performance.

Optimization of the annealing temperature in the RTA includes the annealing temperature (soak temperature), temperature ramp rate, and annealing (soak) time. It was found that a high ramping rate is beneficial to the ohmic contact. Samples with the highest ramping rate (125ºC/second) exhibited the lowest contact resistances and specific contact resistances. We found that 800ºC is the optimal temperature for our FET samples on InAlN. At this annealing temperature, annealing times were optimized systematically. 60 seconds is the optimal annealing time in that the contact resistance is reduced to 0.2Ω·mm. Annealing at 800°C for 60 seconds results in the specific contact resistance as low as $1.2\times10^{-6}\Omega\cdot cm^2$. Interestingly, a TEM study of the annealed ohmic contacts as a function of the temperature used found that at the optimal temperature (800°C), the highest density of contact inclusions was observed. These inclusions consisted of a crystalline TiN structure surrounded by a Au "shell". Lower densities of these inclusions occurred at lower and higher temperatures.

Next, the metal thickness of the ohmic contact was optimized. As we know, in the Ti/Al/Ni/Au system, the Au cap layer acts as the isolation layer to prevent metal oxidation during annealing. Ni is the barrier layer to avoid Ti and Al out-diffusion. The most important layers for contacts are Ti and Al, and the final contact resistance depends critically on their thicknesses.[47] Therefore, in this optimization we kept the Au and Ni thickness constant (Ni: 40nm and Au: 50nm) and changed the Ti and Al thickness. The Ti and Al thicknesses resulting in the lowest contact resistances for InAlN/AlN/GaN was 30nm and 100nm.

2.4. Performance of an InAlN-based Transistor

2.4.a. Mobility and DC Performance

The deeper triangular well that arises from the heterostructure of InAlN/AlN/GaN allows more electrons to be contained in the well, which in turn allows for much higher current densities. Kuzmik predicted current densities of 2.2A/mm and 3.3A/mm for lattice matched InAlN/GaN structures and InAlN/InGaN structures, respectively.[12] A second-order benefit falling out of the enhanced confinement is that the electron wavefunction of the 2DEG is more effectively confined to the GaN channel. This means that the effect of the naturally occurring alloy disorder in the ternary barrier layer is reduced, as there is less probability of an electron being scattered by the random alloy. Recall that in AlGaN, the alloy disorder scattering can dominate the 2DEG mobility, particularly at low temperatures, and particularly for large sheet carrier densities.[48] Despite stating this, it should be noted that increased sheet carrier density results in the center of the electron wavefunction being closer to the heterojunction interface. Therefore, the mechanism of suppression of alloy scattering by enhanced confinement is offset by the drifting of the electron wavefunction toward the interface due to the increased sheet density. Further clouding the picture is the controversial alloy potential of the InAlN ternary. If one were to use the popular estimation of the difference in conduction band offsets between the constitutive binary compounds, clearly the InN-AlN alloy potential would be larger than AlN-GaN. Additionally, the calculations of Chin *et al.*[49] showed that the alloy scattering in InAlN was even more significant then that in AlGaN, furthering the point that the alloy scattering can be quite significant in InAlN-based structures. In any case, the insertion of the AlN spacer layer between the GaN channel and the InAlN barrier is practically

required in order to achieve high mobilities and thus mutes the point, due to the reduction in the penetration of the electron wavefunction into the barrier layer. For example, for an $In_{0.145}Al_{0.855}N$ barrier, self consistent calculations result in ~8.7% of the electron wavefunction penetrating into the barrier, while the introduction of a 1nm thick AlN interlayer, due to the higher band offset, results in only ~2.5% penetration with a depth of ~0.7nm (so that the wavefunction only penetrates into the spacer layer and thusly the 2DEG does not suffer from alloy scattering).[50]

Variable temperature Hall measurements were performed using a van-der-Pauw geometry. At room temperature, respectable mobility values of 850, 1020, 1050, and 1350cm^2/Vs with corresponding sheet densities of 3.4 x 10^{13}, 2.95 x 10^{13}, 2.6 x 10^{13}, and 1.5 x 10^{13} for samples A, B, C, and D, respectively, were measured. These mobility values are comparable with the highest reported thus far in the literature for sheet densities over 2.5 x 10^{13}.[15,16] The low temperature mobility is expected to be much more sensitive to electron concentration as well as to defects and imperfections in the crystal, and as such we can use it to compare the quality of similar structures. Shown in Figure 10 (a) is the mobility vs. sheet density at 77K for our layers with high sheet carrier density (samples A, B, and C) as well as other high quality nearly lattice matched, Al-rich InAlN layers, and an AlN/GaN layer from the literature for comparison. Figure 10 (b) shows for the same set of samples the true figure of merit for the 2DEG transport, the mobility-sheet carrier density product, which is inversely related to the sheet resistance of the layer.

We can attribute the high mobility and high mobility-density product at low temperature to the high quality of our InAlN/AlN/GaN layers. As we expect the centroid of the 2DEG

wavefunction to approach the interface as the density is increased, the mobility of the high density 2DEG will be affected by alloy scattering and interface roughness scattering at low temperatures. The alloy scattering is effectively suppressed as mentioned in reference 51, which reported a self-consistent calculation resulting in a penetration depth of the 2DEG of only ~0.7nm when a 1nm AlN spacer layer is employed. Therefore, the wavefunction only penetrates the AlN spacer and alloy scattering should be negligible. Of course, the effective band offset changes with the composition of the barrier layer and would be reduced as the In composition increases, increasing the electron wavefunction penetration slightly. In any case, the alloy scattering is expected to be low when an AlN spacer layer is employed. Furthermore, the inadvertent layer of GaN discussed in 2.2.a. The Inadvertent GaN Interlayer would also tend to reduce the alloy scattering, as the (binary) GaN interlayer would further suppress penetration of the wavefunction into the (ternary) InAlN. As such, the interface roughness may dominate the low temperature mobility, as reported recently by Tülek *et al.*. We attribute our low interface roughness to a smooth growth front, as well as our optimization of the thickness and deposition pressure of the high temperature AlN spacer layer.[32]

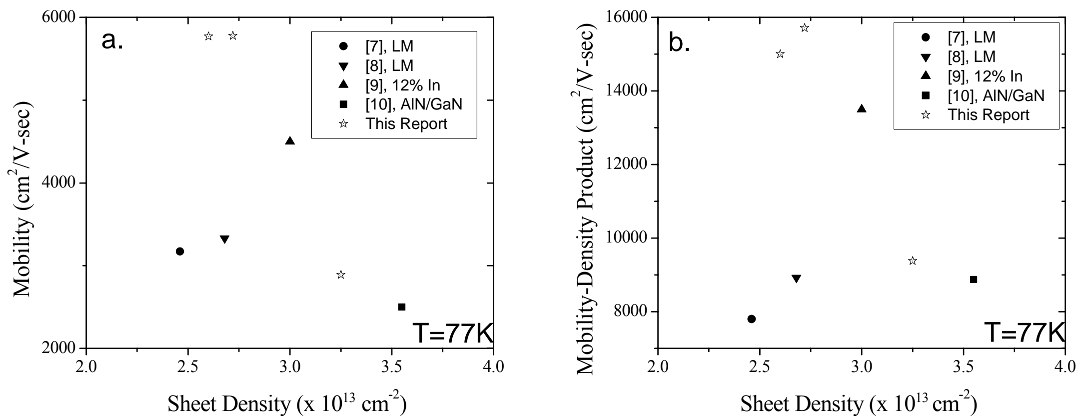


Figure 10. (a) Mobility and (b) Mobility-density product vs. sheet density at 77K for the InAlN/AlN/GaN heterostructures from our laboratory (stars) as well as data from the literature for comparison. Circle and downward triangle are for nearly lattice matched layers [15] and [16], upward triangle uses an In composition of 12% [17], and the square is for a AlN/GaN heterostructure [18].

HFET devices, as described in 2.3. Growth and Fabrication of InAlN-based Transistor**,** have been measured and exhibit respectable performance. On sapphire substrates, for a layer very closely lattice matched (In~15%) the peak drain current density is over 1.5A/mm at DC (about 2.0A/mm pulsed mode) at a forward gate bias of +2V for gate lengths of 1.2μm and source-drain separations of 3.5μm. The pulsed measurements are taken from quiescent bias point of V_G=0, V_D=0, using a pulse width of 1μs and a 0.1% duty cycle. The reduction in drain current at DC as compared to pulsed mode can be ascribed to the self heating effect which is exacerbated by the low thermal conductivity of the sapphire substrate, and is particularly evident at high drain current levels. The measured peak transconductances were about 275mS/mm at DC and over 300mS/mm under pulsed mode, for a drain voltage of 7V. The data in Figure 11 are from a device with a gate width of 45 μm, but devices with gate widths of 145 μm exhibited similar performance. Devices further from the lattice matched condition (with higher In compositions) have lower drain current densities, as expected.

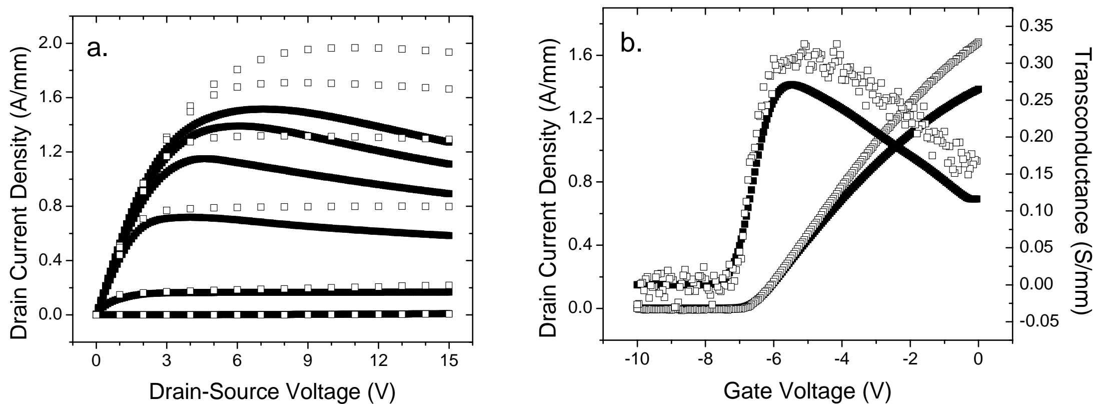


Figure 11. (a) DC (solid squares) and pulsed (open squares) I_D vs. V_{DS} curves for the InAlN/AlN/GaN structure that is closest to being lattice matched, "B". The peak drain current is over 1.5A/mm for a gate voltage of +2V at DC and about 2.0A/mm for a pulse width and period of of 1μsec and 1msec, respectively. The difference stems from the low thermal conductivity of the sapphire substrate which results in self-heating effects suppressing the drain current during the DC measurement. The gate voltage steps are from +2V (top) to –10V in –2V steps. (b) I_D vs. V_G curve demonstrating a peak transconductance of ~275mS/mm at DC (solid squares) and over 300mS/mm using a 1sec pulse (open squares). The drain voltage is 7V.

Although the performance of these devices is quite respectable and approaches that of some of the best reported in the literature, we anticipate that further improvements in device performance and stability can be expected as the crystal quality continues to improve. Along this line, semi-insulating GaN substrates would be the ideal candidates to replace the lattice mismatched foreign sapphire substrates, as well as the SiC substrates which are typically employed by other groups for high performance devices. The switch to a GaN substrate would obviously be beneficial to the quality of the epitaxial HFET structure since the lattice mismatch would in principle be zero, as compared to ~3.5% for SiC substrates. Be that as it may, SiC still boasts a slightly larger thermal conductivity than bulk GaN (4.5 vs. 2.3 W/cmK in undoped material), but the difference is not large enough to sway the picture in favor of SiC because of the adverse effect of lattice mismatch on GaN quality and heat dissipation to SiC due to low interfacial layer quality. To elaborate further, the thermal barrier which resides at the relatively defect ridden SiC-GaN interface might in fact negate the benefits of using the SiC substrate in the first place.[52] Since overall thermal management requires that acoustic phonons efficiently couple into the heat sink (i.e. through the substrate), such a thermal barrier is detrimental to devices on SiC but is absent when using a bulk GaN substrate. On the other hand, the most important point for performance as well as reliability of these devices is the transfer of heat out of the channel itself (this issue is described further in 2.5. Phonons and Device

Performance/Reliability). As such, devices on bulk GaN substrates were also produced.[53] For devices with a similar In composition to those showcased in Figure 11, we obtained very promising results as displayed in Figure 12. Note that the drain current does not tend to decrease with an increase in drain voltage as compared to the devices on sapphire, and additionally the pulsed data more closely follows the DC data, as compared to the device shown in Figure 11 (on sapphire). Both of these observations are attributed to the improved heat removal from the device through the bulk GaN substrate as compared to the sapphire substrate.

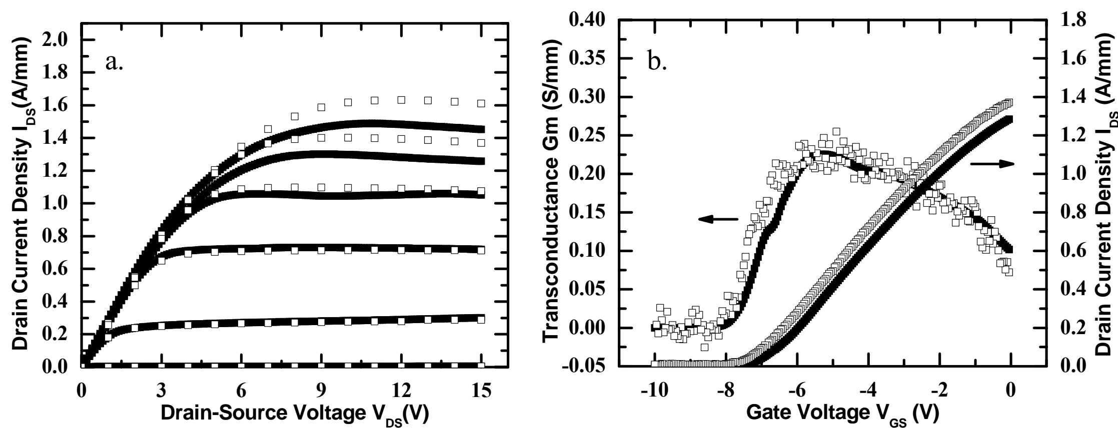


Figure 12. (a) DC (solid squares) and pulsed (open squares) I_D vs. V_{DS} curves for the InAlN/AlN/GaN structure grown on bulk GaN. The peak drain current is about 1.45A/mm for a gate voltage of +2V at DC and about 1.6A/mm for a pulse width and period of of 1μsec and 1msec, respectively. The low difference as compared with the device on sapphire stems from the low thermal conductivity of the sapphire substrate which results in self-heating effects suppressing the drain current during the DC measurement. The gate voltage steps are from +2V (top) to –10V in –2V steps. (b) I_D vs. V_G curve demonstrating a peak transconductance of ~225mS/mm at DC or using a 1sec pulse (open squares). The drain voltage is 7V.

2.4.b. RF Performance

Microwave performance perhaps best indicates the overall quality of the crystal, device design, and technology. Additionally, it is the measurement that is likely the most near to

the actual operating conditions that the device ultimately would be subjected to. As such, it is arguably the performance that matters the most. The most basic form of the microwave measurement is the scattering parameter (S-parameter) measurement. In this case, incident electromagnetic waves of varying frequencies are driven into the input and output ports of the device and a network analyzer determines the four scattering parameters representing the input and output reflection coefficients and transmission coefficients. The S-parameters tell of the device's response to a small signal at a given bias. Of course in the end, a large signal would be applied to a power device in order to obtain the most output power from the device, but the small signal measurement taken at many bias points could be used in principal to determine the large signal response. In addition to the cutoff frequencies of the device, the S-parameter measurement can also be used to estimate the average electron velocity in the channel of the device as discussed below. For further reading on the theory of the S-parameter measurements as well as the network analyzer, please see Appendix 1 and Appendix 2.

If one browses the literature, one can find that a small-signal cutoff frequency (unity current gain cutoff frequency) of 53GHz for a gate length of .2μm (for an f_T*L_g product of 10.6) has already been demonstrated for devices with InAlN barrier layers;[54] additionally, a power of 3.8 W/mm at 10GHz with 30% power added efficiency has been demonstrated.[55] Our best results utilizing InAlN barrier layers (on freestanding GaN wafers) in terms of cutoff frequency are 23.7GHz and 14.2GHz using gate lengths of 0.65μm and 1.1 μm, respectively (for f_T-L_G products of 15.4 and 15.6).[56,57] Plotted in Figure 13 as an example is the current gain, H_{21}, along with the maximum available gain (MAG) for a device with a gate length of 1μm and a source-drain separation of 3μm. The

highest cutoff frequency determined is 14.3 GHz near pinchoff using a drain voltage of 15 V and a gate voltage of -8V (also achieved at a bias of V_D=10, V_G=-7).

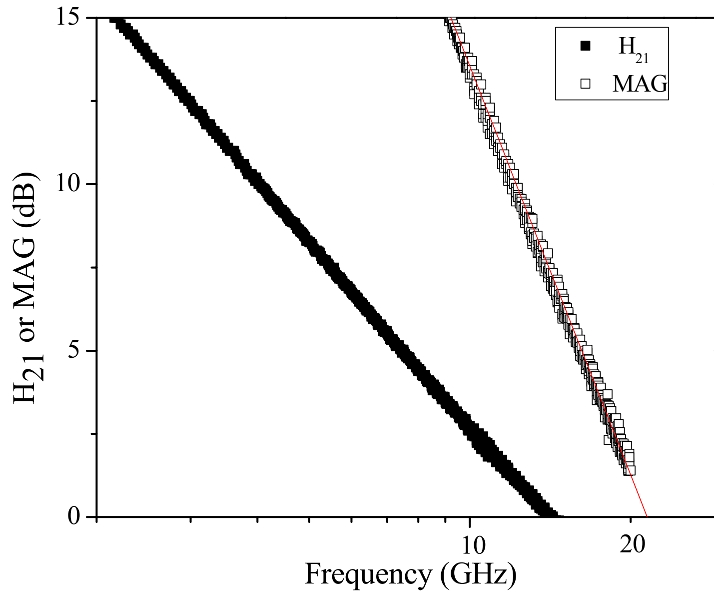


Figure 13. Unity current gain (solid symbols) and the maximum available gain (open symbols) for an InAlN/AlN/GaN device fabricated on a bulk semi-insulating GaN:Fe substrates with a gate length of 1 µm. f_T=14.3 GHz and f_{max}=21.5 GHz at a bias of V_D=15V, V_G=-8V.

As mentioned above, the small signal measurement can be used to estimate the electron velocity in the channel. This is done as follows: the measured cutoff frequency is related to the total device delay time, τ_{tot}, through

$$f_T = \frac{1}{2\pi\tau_{tot}}$$

Equation 1

and τ_{tot} can be written

$$\tau_{tot} = \tau_{\text{int}} + \tau_d + \tau_{RC}$$

Equation 2

where τ_{int} is the intrinsic delay time, τ_d is the delay time associated with the electron drift through the depletion region extending out from the gate on the drain side, and τ_{RC} is the parasitic delay time associated with charging of the RC circuit components. As the intrinsic delay time is related to the saturation velocity through

$$v_{sat} = \frac{L_G}{\tau_{\text{int}}}$$

Equation 3

we can extract the intrinsic delay time from the measured total times. This is readily achieved through the analysis proposed by Moll *et al.* [58]. Measurements of the cutoff frequency at various gate and drain biases allows us to perform the analysis, as shown in Figure 14. In this example, first the drain voltage is varied from 8 to 18 V at a constant gate voltage of -8V and the total transit time is plotted versus the voltage drop across the channel, as shown in Figure 14 (a), i.e. $V_{Channel}=V_{DS}-I_{DS}(R_S+R_D)$, where V_{DS} is the applied drain to source voltage, I_{DS} is the drain to source current, and R_S and R_D are the source and drain resistances, respectively. Extrapolating the linear portion to zero channel voltage would give the total transit time minus that associated with drain delay, as the additional depletion region associated with the drain bias would become negligible at this point. Using measured R_S and R_D values of 2.5 and 5Ω, respectively, and the channel current of ~1mA at the gate voltage of -8V, we obtain $\tau_{\text{int}} + \tau_{RC}$ as 10.12 ps. Next, the gate voltage is varied at a constant drain bias (10 V in this case) in order to generate the plot of total transit time versus inverse drain current shown in Figure 14 (b). In this case, extrapolation back to the origin can be considered to be the total transit time minus that

which is associated with the charging up of parasitic RC components in the equivalent circuit, as the charging time associated with them would go to zero in the case of infinite current. Doing so allows us to arrive at a $\tau_{\text{int}} + \tau_D$ value of 11.12 ps. To obtain the intrinsic delay, we can first either solve for τ_D or τ_{RC} by subtracting $\tau_{\text{int}} + \tau_{RC}$ or $\tau_{\text{int}} + \tau_D$, respectively, from the total transit time. Using $\tau_{\text{int}} + \tau_{RC}$ we obtain τ_D = 11.74ps - 10.12ps = 1.62ps. The intrinsic delay is therefore τ_{int} =11.12ps – 1.62ps = 9.5ps, which corresponds to an average carrier velocity of 1.05 x 10^7 cm/sec. In case we have overestimated the contribution related to the drain delay for this bias point, we can give a more conservative estimate by using the minimum value of total transit time measured at V_G=-8V (Figure 14 (a), for V_D~14V), 11.11ps, resulting in τ_{int} = 11.11ps - 10.12ps = 0.99ps. Using this value of τ_D and $\tau_{\text{int}} + \tau_D$ = 11.12ps obtained from Figure 14 (b) gives τ_{int} = 11.12ps – 0.99ps = 10.13ps, which corresponds to an average carrier velocity of 0.99 x 10^7cm/sec. Reported values of electron velocities in GaN two-dimensional electron gas (2DEG) systems include 1.1 x 10^7 cm/sec for a gate length of 0.29µm[59], 1.32 x 10^7 cm/sec for a gate length of 0.15µm[60], 1.75 x 10^7 cm/sec for a gate length of 0.09µm[61] and 2.2 x 10^7 for L_G=0.23µm when an AlGaN/GaN/AlN barrier was employed. Considering that in this study we are using a gate length which is much larger than those typically previously used for such analysis, the extracted velocity of ~1.0 x 10^7 cm/sec is remarkable. Clearly, short gate length devices should be realized.

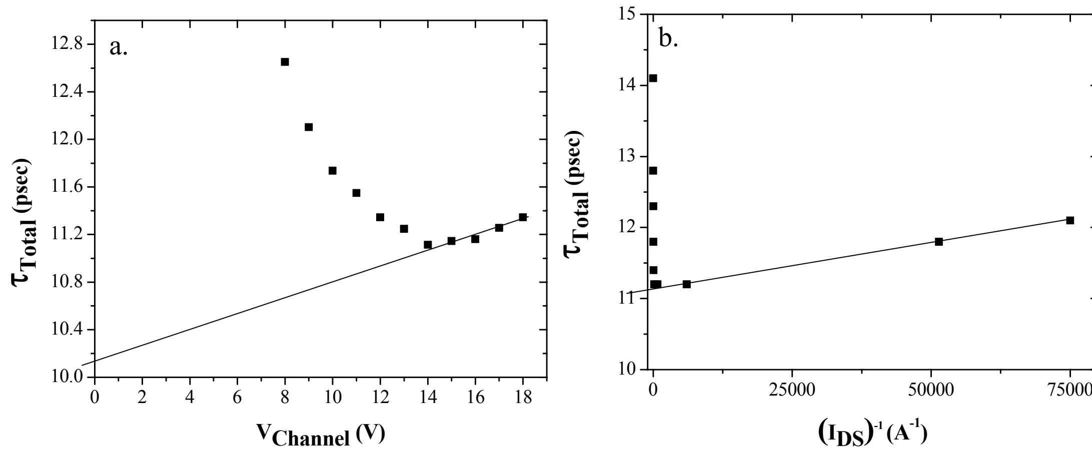


Figure 14. Plots of total delay time: (a) vs channel voltage to extract the total time excluding drain delay (10.12ps) and (b) vs inverse current to extract the total time excluding parasitic RC delay (11.12ps). The solid lines are the extrapolation to (a) zero channel voltage and (b) infinite drain current.

The high velocity can be attributed to the quality of the layer, and/or to the reduced lattice temperature expected in our layers grown on semi-insulating GaN:Fe, similar to the enhancement of electron velocity for identical devices realized on SiC as opposed to sapphire substrates. Additionally, it has been recently shown using the pulsed IV measurement technique that very high velocities in GaN 2DEGs using ungated structures are attainable when using InAlN as a barrier material as opposed to AlGaN;[62] a velocity of 3.2 x 10^7 cm/s was obtained at a field of 180kV/cm with no saturation. This value exceeds previously reported values for velocity in ungated structures utilizing AlGaN/GaN[63] and AlGaN/AlN/GaN[64] of 2 x 10^7 and 1.1 x 10^7, respectively. Electron velocities in high density 2DEG channels typical of GaN-based HFETs would typically be explained in terms of the hot phonon effect: considering that the hot phonon scattering is the primary detractor from carrier velocity at high fields (assuming that defect related scattering, alloy scattering, and real space transfer can be avoided), conditions at which electrons can dissipate the most power through their interaction with hot phonons should

result in the highest velocities. However, for the InAlN/AlN/GaN and AlGaN/AlN/GaN layers mentioned above, one would expect the hot phonon effects to be similar (since they have similar sheet densities, see

2.5.d. The Hot Phonon Lifetime). Therefore, the physical reason behind the apparent higher velocities achievable using InAlN as opposed to AlGaN are unclear as of yet.

2.4.c. Transient Performance and Trapping

Transient measurements are useful in studying the trapping-related phenomena that give rise to undesirable device performance. Let us first describe some of the terms found in the literature related to trapping, namely current collapse, dispersion, gate/drain lag, slump, and drift. The term *current collapse* has come to mean any sort of degradation resulting in reduced current or power available, although it historically meant the reduction in drain current that occurs after the application of a high drain bias;[65] the phenomenon is reproducible and recoverable, and illustrated in Figure 15. The collapse in GaN can be recovered or avoided by heating or illuminating the sample, indicating that it is a phenomenon related to trapping.[66,67] *Dispersion* refers to the reduction of some parameter (such as transconductance) as the frequency is increased. In the best case scenario, collapse and dispersion would compromise the performance of a device and force designers to implement sophisticated feedback and control circuitry to compensate for the device's failure to produce, i.e. a stable amount of output power; in the worst case, since we expect both phenomena to be associated with traps and associated defects, it would lead to catastrophic failure of the devices in the long term as the high fields and strain present in the nitride system would tend to accelerate the creation of even more

traps. These nonidealities can be classified as either recoverable (*drift*) or nonrecoverable (*slump*), both of which can be manifested in terms of current, power, transconductance, etc. (*current drift, power slump, etc*). Drifts are manifestations of trapping (lag) phenomena; *gate lag* and *drain lag* correspond to time delays in the drain current when the gate voltage or the drain voltage is suddenly changed, respectively; as an example, Figure 16 shows a measurement of the gate lag as well as its manifestation in a pulsed gate IV measurement. This would have a profound effect on the RF performance of the devices in question. As such, these measurements can be used as a predictor of how well the device will perform under large signal operation,[68] but are also of utility in determining trap levels within the semiconductor or on the surfaces.[69,70,71] Unfortunately, there is not a one-to-one correlation between types of traps and observable effects.

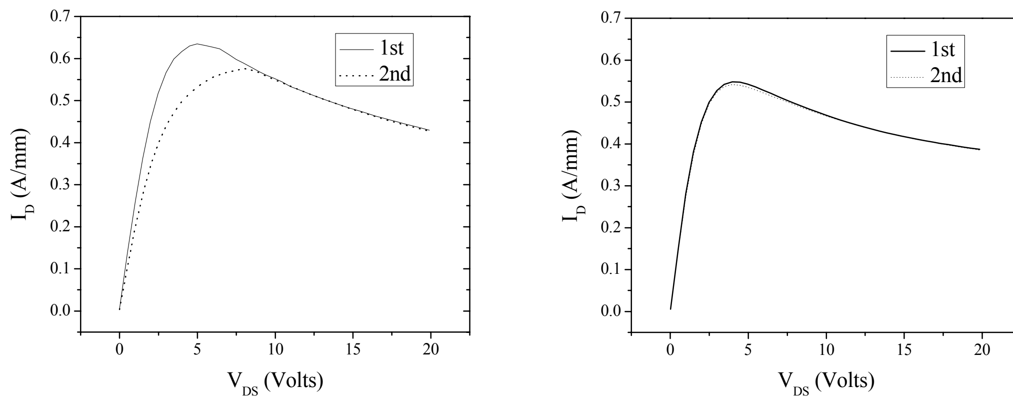


Figure 15. Measurement of current collapse; the drain-source voltage is swept to 20V (V_{GS}=0V) twice consecutively in the dark. (Left) A device exhibiting current collapse and (right) demonstration of the absence of such an effect in a similar device. The only difference between the devices is in the buffer layer growth conditions.

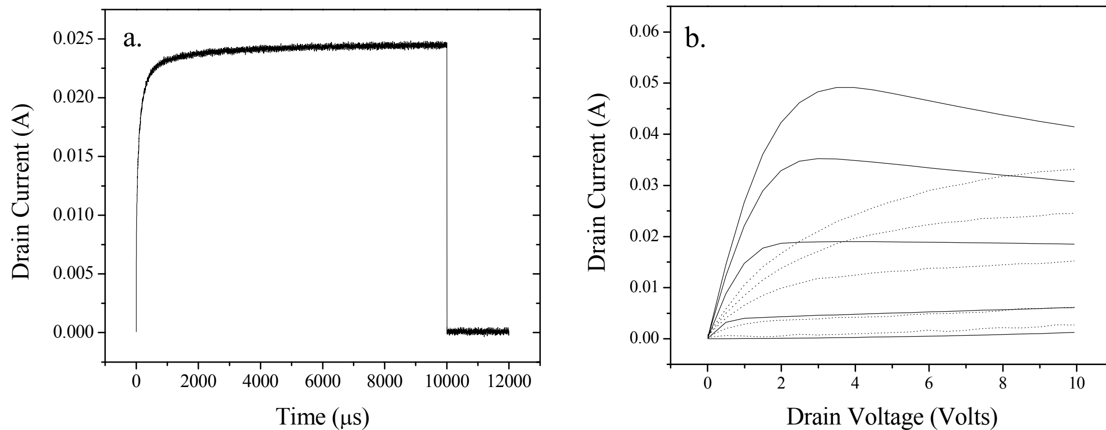


Figure 16. (a.) Measurement of gate lag. The drain current does not immediately respond to a pulsed gate. (b.) Manifestation of gate lag in a pulsed IV measurement--drain current only reaches a fraction of its DC value, resulting in markedly lower current. The quiescent bias voltage is V_G=-4V, V_D=0V, pulse width is 1 μs.

In general, traps in both the barrier and buffer layers as well as at the heterointerface and on the surface are sites at which a carrier may reside, resulting in virtual gating, current reduction, and frequency dispersion as traps have some charging and discharging time constants associated with them. Additionally, high resistivity buffer layers are imperative for good microwave performance as well as to improve carrier confinement and avoid short channel effects. Layers with high densities of dislocations[72] or employing intentional dopants such as iron[73] or unintentional dopants such as carbon in the buffer layer can compensate the unintentionally incorporated donors (such as oxygen or silicon), resulting in the desired semi-insulating (SI) GaN buffer layers. Dislocations are known to both collect traps and form other complexes, but are also known to be effective leakage sites for reverse-biased GaN Schottky contacts, and are therefore undesirable as solutions to achieve SI GaN.[74] Dopants also are in general unwanted as they can result in trapping. For example, by analyzing the wavelength dependence of light incident on the sample

surface on the recovery of the current in a biased device, Klein *et al*.[75,76] estimated the depth of trapping centers responsible for current collapse to be 1.8 and 2.85 eV below the conduction band with densities of mid-10^{11} cm^{-3}. More severe current collapse was coupled with an increase in the density of the trap at 2.85eV occurring in layers grown at lower pressures which was correlated by secondary ion mass spectroscopy (SIMS) with higher levels of carbon incorporation (the SIMS measurement demonstrated C concentration to be in the mid 10^{16} to low 10^{17} range).[77] Intentional doping of buffer layers with iron, on the other hand, is being employed with success although Fe suffers from a memory effect in growth reactors and trapping could in principal still occur.[78,79] In short, the ideal way to address the need for SI buffer layers would be though improved layer quality (intrinsic carrier concentrations in the wide bandgap GaN is vanishingly small) rather than intentional compensation, but in reality Fe doping may be the more feasible approach.[80]

InAlN-based HFET devices already seem to be more immune from the issue of gate lag as compared to their AlGaN-based predecessors.[36,81,82,83] Reduced gate lag is largely credited to the absence or reduction of virtual gating which in turn has been attributed to the absence of piezoelectric polarization in the barrier. Though gate lag can arise due to traps on the surface or in fact anywhere in the gate leakage path, in high quality layers, gate lag has been attributed to being a manifestation of slowly moving charges interacting with the polarization charge that resides near the surface.[84,85,86,87] In fact, nearly dispersion free layers utilizing AlGaN/GaN HFET structures without passivation were reported in references 84, 86, and 87. In these cases, the GaN cap layer was much thicker

(250nm) than that used for a typical HFET structure (a thin cap is typically employed to reduce the ohmic contact resistance), Si doping of the barrier as well as a 5nm thick cap layer was employed,[86] and some other novel heterostructure was used to avoid the instable charges at the surface, respectively.[87]

We believe that the success of lattice matched InAlN layers in terms of their immunity to gate lag is due to the absence of piezoelectric polarization present in the InAlN barrier layer. In order to be manifested as lag, the trapped electrons must respond more slowly to changes in gate potential than the time associated with the lag measurement (1μsec). Traps whose time constants are much faster than the measurement would not contribute to the lag. However, the lag is exacerbated when traps on the surface interact with the dipole charges on the surface associated with (piezoelectric) polarization. In order to be recollected by the gate (and not contribute to the virtual gating and subsequent lag) electrons emitted by the traps must quickly leave the surface. The dipole charges associated with the polarization are an impedance to this movement, thus quickly responding traps may still contribute to lag when they are coupled with these polarization charges. As such, layers further from the lattice matched condition should exhibit more lag due to the piezoelectric polarization present in those layers.

In order to test this theory, pulsed measurements with 1μs long pulses and 1msec period under various quiescent voltages were performed on the same four layers with different In compositions, as described in Section 2.3.a. Growth of InAlN and determination of composition. We first pulse from a quiescent voltage representing the open channel state (V_G=V_D=0); this of course results in the highest current values. This is considered the "baseline" to which further pulsing will be compared in order to quantify the degree of

gate lag. Next we pulse from other quiescent bias points, specifically from points using a reverse biased gate. Figure 17 shows the pulsed drain current (squares) as well as the DC I_D curve (line) at a gate bias of 0 volts for the InAlN barrier HFET layer, "C" (slightly lattice mismatched, compressively strained). The pulsed measurements are obtained using quiescent bias points of V_G=0V, V_D=0V (baseline), V_G=-4V, V_D=0V (about halfway pinched off channel), and V_G=-8V, V_D=0V (nearly pinched off channel). The drain current decreases as the magnitude of the quiescent gate voltage increases—this is due to gate lag. It is important to note that a "lag-free" device should have its pulsed I_D curve following the pulsed curve using a quiescent bias of V_G=0V, V_D=0V as opposed to following the DC value (the increase in current under pulsed mode as compared to DC is due to the reduced Joule heating in the device under pulsed mode). Figure 18 shows lag measurements for each of the four devices at many quiescent (gate bias) points for a drain voltage of 7V. The lag is quantified as the percentage change in the drain current between pulsing from a nonzero quiescent bias voltage on the gate and the baseline. Clearly, the degree of lag is correlated to the degree of lattice mismatch of the layer. It is interesting to note that when the layers are compressively strained (samples "C" and "D"), the gate lag suffers markedly, while tensile strained layers are not as adversely affected (sample "A"). Additionally, we believe that the degree of lag is unrelated to the quality of the layer, as the quality at least among the two layers closest to being lattice matched are thought to be similar (as illustrated in Figure 9).

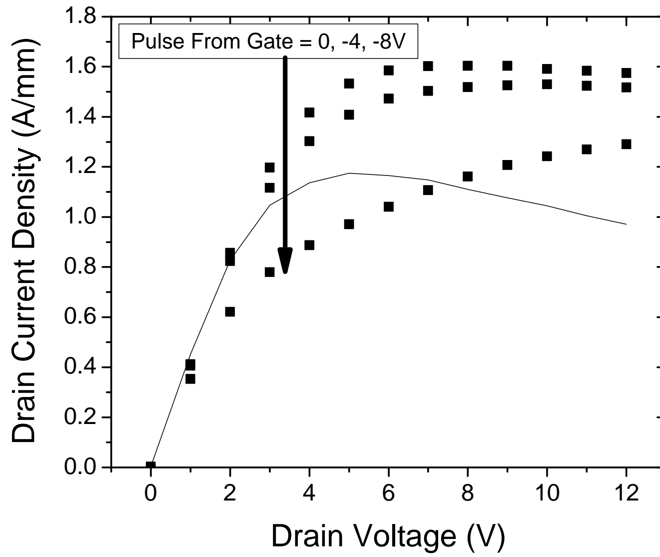


Figure 17. DC (solid line) and pulsed IV (solid squares) demonstrating the gate lag effect in a slightly lattice mismatched InAlN device, "C". The pulses (1μsec) are from quiescent voltages V_D=0V, V_G=0, -4, -8 (pinchoff). If one were to compare only to the DC values, the pulsed curve at V_{GQ}=-4V might be called "lag free" but in fact should be compared to the baseline (pulsing from V_D=V_G=0V).

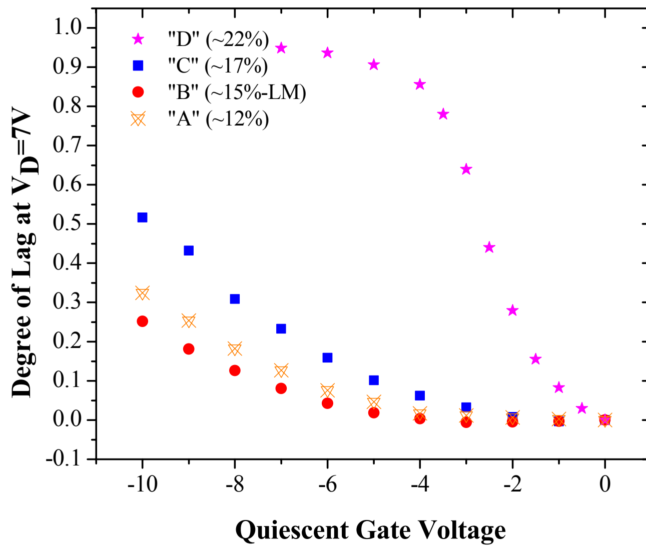


Figure 18. The degree of gate lag as a function of quiescent bias voltage on the gate. Degree of lag is the percent difference between the pulsed value of I_D when pulsing from a quiescent bias voltage on the gate and that at 0V. The leakage current density for the devices "A", "B", "C", and "D" shown in the figure at V_G=-10V and V_D=7 is 68μA/mm, 44μA/mm, 72μA/mm, and 25μA /mm, respectively. Thus the overall gate leakage is not responsible for observed differences in lag. The pulse lengths are 1μsec and the drain voltage is 7V.

We believe that the amount of lag is *directly* related to the number of electrons trapped either on the surface of the semiconductor or within the barrier of the device, acting as a virtual gate,[88] not to the amount of *leakage current* from the Schottky gate metal. Devices with relatively high and low gate leakage on the same sample have reasonably similar degrees of lag; furthermore, devices with similar gate leakage on samples with different barriers have very different degrees of lag. Therefore, the structure of the device is a better predictor of whether a device will exhibit lag than is the gate leakage current. As an example, the gate leakage current density for the devices shown in Figure 18 at V_G=-10V and V_D=7 is 68µA/mm (A), 44µA/mm (B), 72µA/mm (C), and 25µA /mm, (D). Having said this, we observe that the lag is still somehow related to the gate current for the devices that show moderate to significant amounts of lag (i.e. samples C and D) as illustrated in Figure 19. Here, the derivative of the gate leakage current (solid lines) changes abruptly around the same voltage bias at which the amount of gate lag effect exhibits an increase (symbols). The heavy line and stars represent gate leakage and lag for one device on the lattice mismatched layer (D) while the lighter line and squares represent gate leakage and lag for another device on the slightly mismatched layer (C). This may indicate that for some devices, there is a threshold in the gate potential beyond which electrons have access to new leakage paths and subsequent access to traps thereby markedly increasing the gate lag. This would be evidence for the gate lag effect being attributable to electrons that are trapped somewhere in the gate leakage path. However, such a correlation between the derivative of gate current and the amount of lag was not observed for the devices on sample B, which showed very little lag. Further work to

elucidate the mechanisms of the gate lag under various bias conditions and at various temperatures would be fruitful.

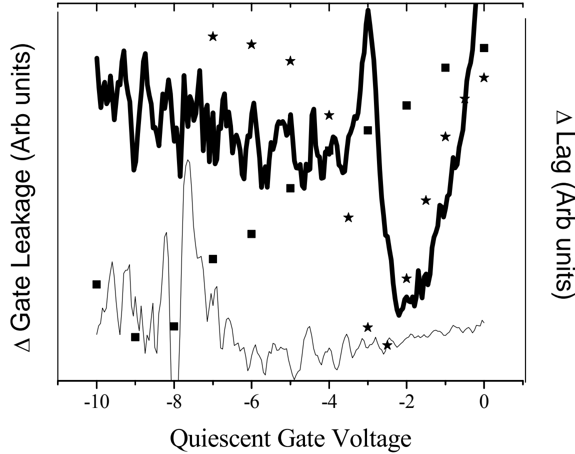


Figure 19. Derivative of gate leakage (lines) and the change in the degree of gate lag (symbols) versus quiescent gate voltage demonstrating the correlation between gate leakage and the gate lag effect for the slightly lattice mismatched layer, "C" (solid line and squares) and the lattice mismatched layer, "D", (heavy solid line and stars) barriers. The drain voltage is measured at 7V, the pulse width is 1μsec, and the period is 1msec.

To further reduce the gate lag, passivation[89,90] is often employed. For example, minimal collapse after extended DC stress and an improvement by up to 100 times of the rate of degradation of microwave output power under CW operation were reported for PECVD-deposited SiN_x passivation layers wherein a pretreatment step in NH_3 plasma was employed.[91] However, the degree of success in terms of mitigating the trapping effects are highly dependant on the procedures and processing, and reliable recipes which can be universally employed are lacking. Passivation in general constitutes a rather broad topic and will not be discussed further, more details can be found in 10 and the references therein.

As mentioned above, pulsed IV measurements can also be of use in determining the levels of traps within the structure (which can be responsible for causing lag). We choose a device similar to the one illustrated in Figure 17 (with an In composition similar to that of sample “C”) since the lag is evident in this layer. The devices were subjected to long (up to 250mesc) gate “filling pulses” of –4V while the drain bias was held constantly at 5V. The drain current was then measured as a function of time after the gate voltage was switched back to the open channel condition (0V). The times allowed for emission of trapped electrons from the traps was increased until the value of drain current reached the steady state condition.

Figure 20 shows the direct measurement of this “drain current recovery” experiment at a number of temperatures. The measurement is performed at a constant drain bias of 5V.

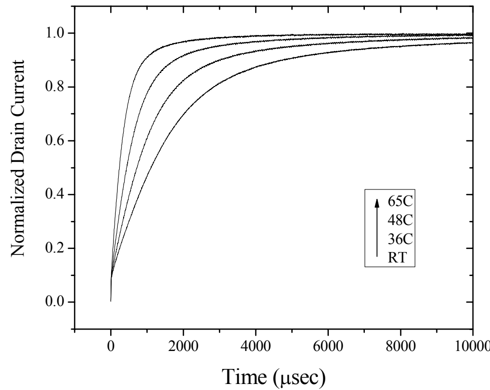


Figure 20. Direct measurement of the gate lag for an InAlN device at various temperatures. The current recovery is suppressed; the device recovers in several milliseconds as opposed to an ideal device which would recover instantaneously. The “filling pulse” of the gate is 250msec at –4V.

Next, the same measurements were carried out at various temperatures in an effort to extract the emission rates, *e(T)*, as a function of temperature, assuming that carriers trapped in levels within the bandgap of the barrier or on the surface are the source of the

gate lag. The traps can be identified by experimentally determining the emission rate as a function of temperature and using the principle of detailed balance:

$$e(T) = AT^2 \exp\left(-\frac{E_A}{kT}\right)$$

Equation 4

The electrons can escape from the traps if they have sufficient thermal energy and the traps can be probed spectroscopically by measuring the emission rate as a function of temperature.

Shown in Figure 21 is the recovery of the drain current, ΔI_d, as a function of time at various temperatures. The function ΔI_d is the normalized percent difference of the drain current from the steady-state value of the drain current:

$$\Delta I_d(t) = \frac{I_{dss} - I_d(t)}{I_{dss}}$$

Equation 5

Two different decay channels can be identified from the figure, a faster transient occurring in the first few milliseconds and a slower one acting over tens of milliseconds. These two regimes of linear behavior in the semilog plot indicate that an activated process such as the one in Equation 4 may be at play for each of the decay channels. Accordingly, the transients are fit to a bi-exponential decay function and the emission rates are plotted into an Arrhenius plot in Figure 22. The activation energy, E_A, extracted from the Arrhenius plot of the faster transient has a value of 123meV, which is similar to the activation energy measured for a trap that we have measured by DLTS in a similar sample.[92] It should be recognized, however, that the values obtained by this method are

not the zero-field activation energies, and influence of the drain bias on the apparent activation energy should be considered (i.e. Poole-Frenkle lowering of the electron barrier under the applied electric field).[93] In addition to this trap, the slower transient can be fit to an Arrhenius plot with an activation energy of 80meV.

In general, devices which cannot be fit to exponential decay functions (or can only be fit to “stretched exponential functions”) might appear in the case in which there a number of trap levels within the bandgap. Devices which can be fit to exponential functions but which do not fit well to an Arrhenius plot might indicate that the simple model of thermionic emission from a trap is insufficient. Thus, emission from multiple traps or electric field enhanced emission (since the field varies spatially) would confound the analysis. In short, the technique is only useful in some situations; further refinement of the models is in order.

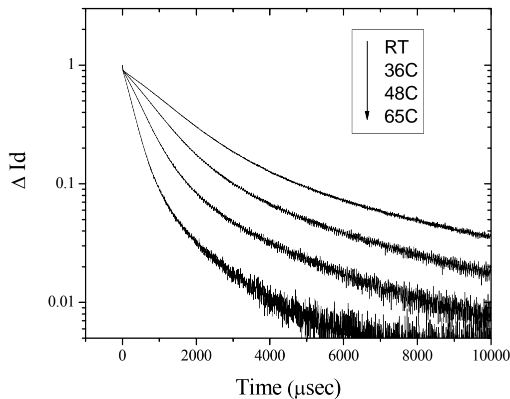


Figure 21. ΔI_d as a function of time.

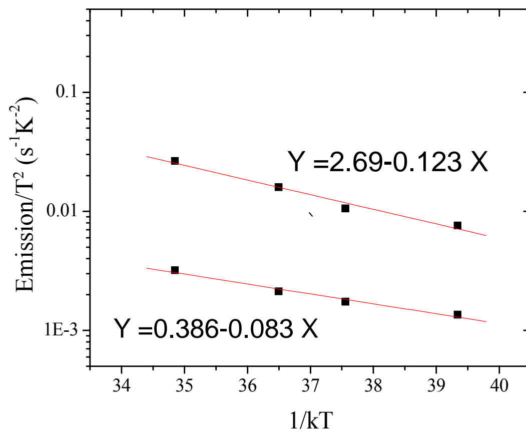


Figure 22. Arrhenius plot of the fast and slow transients for a sample which shows significant gate lag. Two exponential functions are fitted to give two emission rates as a function of temperature.

The discussion of traps in devices leads us naturally into a discussion of device reliability, as the existence of defects in a device would tend to enhance the generation of further defects in a device when the device is under bias, particularly for a highly ionic and piezoelectric semiconductor such as GaN. As such, a description of reliability as it pertains to GaN HFETs follows.

2.4.d. Reliability of GaN-based HFETs

Reliability of GaN-based HFET devices represents the largest impediment to widespread commercialization of the technology. Though great strides have been made, to the extent that some HFET manufacturers already boast device lifetimes (expressed as a mean time to failure, MTTF) of $> 10^7$ hours (measured under accelerated DC[94] and RF[95] stress tests), a major problem still to be addressed is the vast variation among HFETs on the same wafer[96,97] and perhaps more importantly, the question remains of the viability of the 3T

test itself, since the extracted activation energies vary widely from laboratory to laboratory under both DC and RF stressing.

From a statistical point of view, reliability is a measure of the repeatability of an experiment or process. Therefore, in the realm of devices, the reliability is a measure of the consistency of the method of production of a population of devices, i.e. a population with high reliability boasts more devices behaving similarly than a population with low reliability. Often, the parameter of interest is the expected lifetime of a population of devices, and in this view, reliability can be defined as the probability that a given device will perform to its specifications for a given period of time. The challenge, therefore, is pushing the devices to achieve longer and longer lifetimes and additionally maintaining the process so that one could expect an entire population to have the same failure rate. The genesis of the reliability problem is therefore difficult to comprehend unless the specific failure mechanism is illuminated. In GaN, there appear to be several degradation paths which play roles in causing device failure which are accessible under different biasing or environmental conditions. These pathways include high field-driven, hot electron/hot phonon driven, and ambient temperature driven (metallurgical) mechanisms. In terms of characterizing failure, the typical GaAs-based approach[98] is depicted schematically in Figure 23. Depending on the failure rate vs. operating time, there are three regimes of failure termed infant, random, and wear-out. Some devices suffer what is called the early (infant) failure, which are failures occurring very early in the operating life of a device and are addressed commercially by a "burn in" procedure which screens a portion of or all of the population of devices, so that infant failure occurs in the factory as opposed to the customer's hands. This is followed by random failure, which generally

occurs at a relatively constant rate over the lifetime of a device. Finally, devices enter the realm of wear-out failure, altogether leading to a bathtub-shaped dependence in time. Ideally, it would be desirable to eliminate the infant and random failures and reduce the wear-out failure rate to the extent possible.

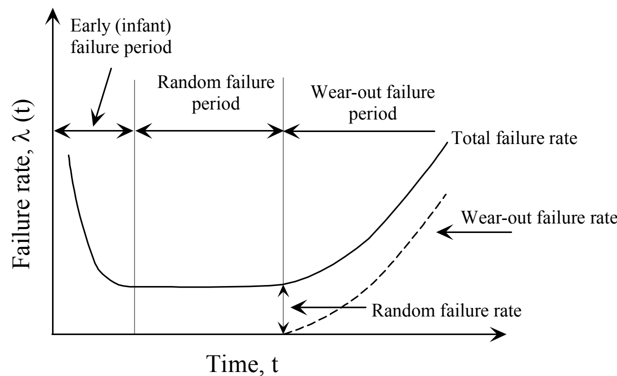


Figure 23. A schematic representation of the three failure regions, namely the infant failure period (experienced very early on), the random failure period, and the wear-out failure period. After 98.

A typical procedure to ascertain the reliability of various types of devices is the accelerated life test. Accelerated life testing is typically performed at three different but elevated temperatures in which cumulative failure rates are recorded and the mean time to failure (MTTF) for each of the three temperatures is established. The test is therefore referred to as the three-temperature (3T) life test. The failure is defined as e.g. a reduction in the drain current by 10%. The MTTF figures so determined are then converted to a single Arrhenius plot wherein the MTTF values are plotted in the log scale as a function of inverse temperature. Extrapolation to a given temperature then determines the expected MTTF for an HFET operating at that temperature, or more applicably that channel temperature, which is always higher than the case temperature, see Figure 24.

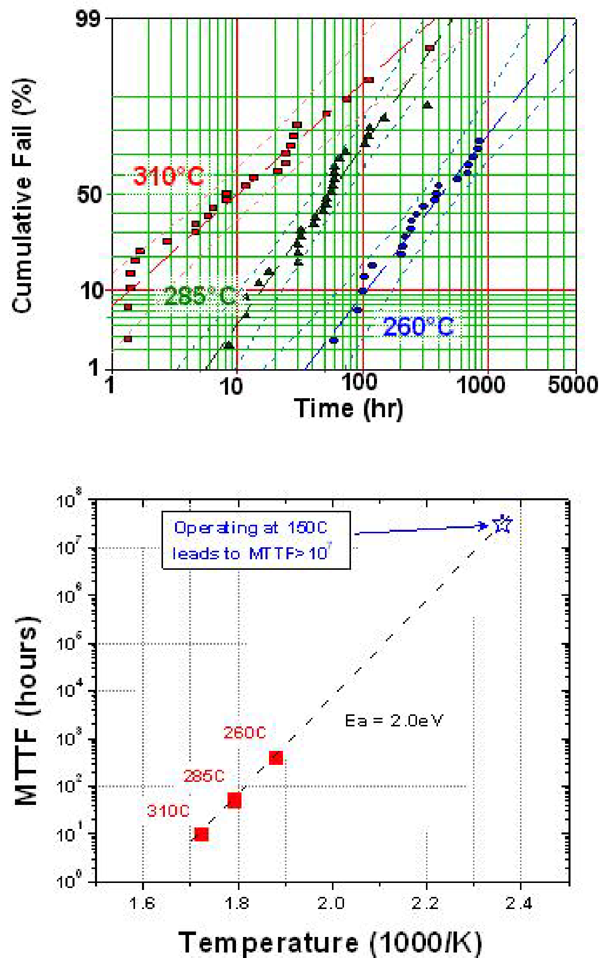


Figure 24. (Top) Three-temperature (3T) lifetime test data showing the cumulative failure rates vs. time obtained at 3 different temperatures, namely 260, 285, and 310 ^{o}C. The σ values for 260 and 285 ^{o}C are approximately 1 but that at 310 ^{o}C is 1.5 which might imply contribution by infant failure. (Bottom) Arrhenius plot of the MTTF determined at three different temperatures, 260, 285, and 310 ^{o}C, which lead to an activation energy of about 2 eV and an extrapolated MTTF value greater than 10^7 hours at 150°C. Courtesy of Dr. A. Hanson of Nitronex, Ref. 99.

Although widely used, the 3T method provides a limited test in that the peak junction temperature at the heterointerface should be measured as opposed to the surface temperature, which can be difficult to access, particularly when a field plate is used which obstructs optical access to the semiconductor. More fundamentally, the assumption of the 3T test is that the channel temperature (as opposed to, i.e. the hot electron temperature) is most important and furthermore that the failure mechanism follows an Arrhenius-type dependency, which may not be valid; perhaps in some cases the increased

temperature would reduce the rate of degradation as the electron mean free path is reduced. Such difficulties may be one source of the wide range of activation energies reported by various laboratories under RF: -0.15eV [100], 1.05eV [78], 1.8eV [95], as well as DC: 1.6eV [101], 1.7eV [102], 1.81eV [97], 2.0eV [99], 2.47eV [94] stress conditions. The fact that different slopes for different temperatures are observed in Figure 24 could indicate that different mechanisms are taking place with different activation energies. An additional observation related to the wide range of activation energies reported has been reported by Li *et al*. who concluded that the activation energies of HFETs on SiC tended to decrease with the strain (thickness) of the underlying GaN buffer layer.[103]

In any case, accelerated stress tests provide a means to attempt to determine the lifetime of a population without having to operate devices for unreasonably long periods of time, assuming that the increased temperatures utilized during the tests constitute well-controlled degradation (i.e. that the elevated temperatures do not introduce artifacts such as unrealistic failure modes). Various accelerated tests can delineate different failure mechanisms, and tests can consist of simply storing devices or subjecting them to various biases such as under operating conditions, under forward biased gates, under pinchoff, etc.

Of course, tests during which the devices operate very close to the actual system working conditions (typically under RF bias), so that reliability predictions can be more accurate and representative would be most desirable. However, it is not easy to control RF working conditions during life testing, so it is possible to introduce spurious failure mechanisms due to overstress, input/output impedance mismatching, in particular at high

temperature, etc. In any case, it would be wise not to limit the characterization to classical transistor parameters (drain saturation current (I_{DSS}), pinch-off voltage (V_p), transconductance (g_m), etc.) but also to include the measurement of other parameters, such as parasitic resistances, gate diode characteristics etc. which can help to correctly identify the actual failure mechanisms. Finally, in addition to the electrical stress on devices, environmental testing on packaged devices to ascertain the product's robustness to vibration, moisture, shock (i.e. electrostatic discharge), pressure, etc, would be imperative prior to insertion in real applications.

As a final note, it should be stressed that meaningful reliability figures cannot, in principle, be condensed into a single number such as an MTTF. To illustrate the need to divulge more information than a simple MTTF, a plot of reliability vs. time for three sets of mock data with identical MTTF (arbitrarily chosen to be 10^6 hours) but different values of σ (the standard deviation of the distribution function) is presented in Figure 25. We assume the failure to follow a lognormal probability distribution function (PDF), which is typically used when fitting measured failure rates of actual devices in the "normal" (random wear-out period) phase of product lifetime. Although the sets of devices have identical MTTF, the expected percentages of failed devices range from 99.98% to 70.4% after operating for 10^5 hours when σ increases from 0.5 to 1.5. Along this line, other metrics such as T1% or T10% could be more useful (which would be the times when 1% or 10% of the population fails, respectively). Furthermore, the assumption of a lognormal distribution only holds when the failure rate is **constant** in time, meaning the random failure period indicated by the "bottom of the bathtub" in Figure 23, which in fact may have nonzero slope. The overall bathtub including infant

failure and wearout phases are generally modeled using Weibull analysis. See Ref. 104 for the authoritative handbook.

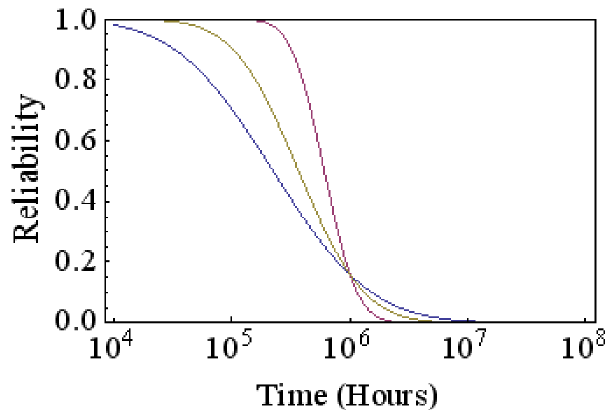


Figure 25. Simulated reliability versus time curves for three sets of mock data with failures following lognormal probability distribution functions, each of which has an MTTF of 10^6. Despite having identical MTTF, the three sets of data illustrate that the expected percentage of failed devices after 10^5 hours are 99.98%, 90.4%, and 70.4% for σ = 0.5, 1, and 1.5, respectively.

As device failure is not always catastrophic, failure in a typical 3T test is often defined when one parameter, e.g. I_{DSS}, is reduced to e.g. 90% or 85% of its initial value, as in [94] or [99], respectively. While the lack of a standard for GaN-based HFETs makes for difficult comparison of raw MTTF figures given by manufacturers, phenomena such as "sudden degradation" or the slow initial degradation[105] further confounds the issue. The sudden degradation phenomenon refers to the case when drain current under pinchoff conditions suddenly increases, usually within the first couple of hours of stress, and can be present or absent in devices on the same wafer. Slow initial degradation refers to the reports wherein degradation tends to occur more strongly in e.g. the first 10 hours of stressing with relatively little degradation appearing in the subsequent 100's of hours of stress. A burn-in treatment could be used to screen devices in either case, but in the end, it should be made clear whether the stated MTTF of a population includes or excludes devices exhibiting sudden degradation or slow initial degradation. The sudden

degradation phenomenon has been found to be correlated to higher degrees of initial current collapse as well as higher initial gate leakage current.[106]

Let us turn now to the physical mechanisms which give rise to device degradation. We identify three primary classes of degradation mechanisms: high field driven, hot electron/hot phonon driven, and ambient temperature driven (metallurgical).

At the heart of the high field driven degradation is the piezoelectric response of GaN and the use of strained barrier layers in typical devices (typical ones being of the AlGaN variety). In general, strain has an important role on the reliability (in terms of RF output power) of HFET devices. Lee *et al.* reported that degradation (in terms of slumping I_{Dmax}) as a function of barrier thickness (and therefore strain) decreased in an $Al_{0.32}GaN_{0.68}N$ barrier HFET when decreasing the thickness of the barrier from 26 to 13.8nm; additionally, variation of V_{pinch} (attributable to trap generation under the gate) was more pronounced after long-term RF stress in devices with higher Al mole fraction in the barrier.[107] Strain relaxation of AlGaN/(AlN)/GaN through the generation of dislocations at the interfaces is therefore a formidable source of degradation.[108] Along these lines, the so-called inverse piezoelectric effect has been proposed as a mechanism of degradation of operating devices.[109,110] The effect states that applied vertical fields (due to potential difference between the gate and channel) would increase the strain in the already tensile strained AlGaN barrier and that this increased strain would cause relaxation through defect generation. The result is increased gate leakage and access resistances as well as decreased I_{Dmax}.[111] Increased strain, attributed to increased vertical field (with increasing drain bias) was in fact experimentally observed by using μ-Raman spectroscopy.[112] Chowdhury *et al.* has studied the TEM of devices after having been stressed at various

temperatures under V_D=40V and suffering subsequent degradation.[113] Pit shaped defects were observed after stress, and some of the more degraded devices showed a crack, as evidenced in Figure 26. The degradation occurred on the drain side of the gate where the electric field is highest. Amounts of degradation in terms of the change in drain current correlated well qualitatively to the amount of "disfiguration" indicated from the TEM images.[96,113] One question to ponder is the role of the gate current in this degradation since electrons which might tunnel out of the gate during application of this high V_{DG} could have kinetic energy sufficient to damage the semiconductor surface.

Figure 26. Cross-sectional TEM image of a degraded AlGaN/GaN FET. The crack observed on the drain side of the gate (right hand side of the image) is indicative of degradation. (After 113)

Metallurgical degradation such as metal-semiconductor diffusion, phase changes in metal stacks, and electromigration within the metal are sources of potential permanent degradation. Electromigration of the gate electrode metal, impurity activation, and contact diffusion effects are reasonably well understood particularly in conjunction with, e.g. GaAs based devices. However, GaN based devices push the metallization technology to its limit causing some metallurgical changes, particularly under prolonged high current or high temperature operation. Ti/Al-based metallization schemes are typically utilized for the Ohmic contacts to AlGaN/GaN HFET structures and indeed are being used by the

commercial entities[94,96] but Mo/Al, Ta/Al, V/Al, and Ti/W based systems have also been explored. The Al in the contacts to the AlGaN or GaN cap layers are susceptible to oxidation and cracking, therefore top metal layers of Ti/Au, Ni/Au, Pt/Au, Pd/Au, Mo/Au, Ta/Au, Ir/Au, Nb/Au, TaN, TiN, ZrN, TiB_2, CrB_2, and W_2B_5 have been used to varying degrees of success (See Reference 19 and the references therein for details). Additionally, the thicknesses and ratios of various components within the same stack are important.[114] Reports on thermal stability are difficult to compare since various authors use different thermal stressing schemes to ascertain the quality of their ohmic contact metallization, but long term thermal stability tests (representing aging of the device) have been demonstrated with some success in terms of minimal to no change in the contact resistivity of the ohmic metals in some systems. However, there is no universal consensus as to the "best" metal scheme to employ in terms of performance and long term reliability, although the Ti/Al/Ni/Au is likely the most widely adopted.[115] More work would need to be done in order to determine whether degradation of the contacts comes as a result of operating at high temperature, high current, or both. In terms of the thermal stability, the ohmic contacts are likely less of an issue as compared to the Schottky contacts,[116] which even in the absence of applied bias, may show some change with time under elevated temperatures.

Schottky gate contacts have been demonstrated with Ni/Au, Mo/Au, Pt/Au, Ni/Ti/Au, Pt/Ti/Au, ZrB_2/Ti/Au, TiB_2/Ti/Au, CrB_2/Ti/Au, and W_2B/Ti/Au with varying degrees of success (Again, see Reference 19 and the references therein). Interdiffusion of the metals at elevated temperatures would obviously be an issue for the reliability. In fact, Pt-Au interdiffusion is known to occur at temperatures as low as 200^oC.[117] Although it is

unclear precisely what role gate leakage plays in the degradation of the HFETs, it has been suggested that a silicide can form in devices employing Ni-based Schottky contacts and SiN_x passivation layers at the SiN_x-Ni interface and that the reduced barrier height of the Ni-silicide contact causes higher gate leakage. Additionally, the nonuniform nature of the silicide results in localized leakage conduction paths, which results in current crowding and gate electrode degradation, an increased instance of the "sudden degradation" phenomenon, and much lower device lifetimes. In any case, gate leakage should in principal be avoided as electrons flowing from the gate could be trapped on the surface or within the underlying layer resulting in "virtual gating" mentioned above, and also because leakage would reduce the efficiency and gain, as input power would increase with no coordinate increase in output power.

An increase in the Schottky barrier height has been determined as a cause for the decrease in I_{DSS} and subsequent decrease in absolute value of the pinch off voltage in structures of AlGaN/GaN on Si after being subjected to DC stress tests at T=200°C, V_D=28V. Physical analysis of the stressed devices using scanning tunneling electron microscopy (STEM) showed that a thin interfacial layer that exists between the gate and the AlGaN barrier layer had been consumed during the stress. In the same report, the use of a gate anneal step prior to stress reduced the I_D drift by 50%, and in a similar study, the increase of the Schottky barrier height stabilized after 1000 hours of stress.[116] In another stress study, STEM showed that some devices that demonstrated the most degradation after stress at high temperature and at V_D=40V for long times (up to 1000hr) suffered from diffusion of gate metals into the AlGaN barrier layer.

Degradation arising from hot electrons and hot phonons plague GaN even moreso than GaAs.[98,116,118] During device operation, particularly at the high fields that would typically be employed in GaN-based HFETs, electrons could be imparted with enough kinetic energy (“heating” them up) to begin to cause physical damage to the crystal in the buffer or barrier layer. This would form new traps and has been observed via increased gate lag as well as reduced I_{Dmax} and transconductance after the application of “on-state” stress.[119] Simulations placing traps both in the buffer and on the surface as well as in the buffer, the barrier, and on the surface are sufficient to replicate the experimental degradation.[120] Additionally, threshold voltage shifts are typically observed after on-state biasing, which are attributable to some metallurgical change at the gate/semiconductor interface (due to heating),[102] but could also be explained in terms of trapped electrons in the barrier layer under the gate. In any case, it is likely that at least some portion of the degradation that is attributed to hot electrons is in fact dovetailed with hot phonons, which in any case cannot be decoupled, since the ionic nature of GaN yields very strong electron-phonon coupling (perhaps as high as some 30 times stronger as compared to that in GaAs). The slump that the device would suffer as a result is not incorporated in many statistical models that are often applied to GaN. This constitutes a very important source of physical degradation, and as will be shown below, an important impediment to achieving the optimum performance from devices.

2.5. Phonons and Device Performance/Reliability

The fields which are present in an HFET device give rise to large densities of electrons and phonons which are not in equilibrium (referred to as “hot”) and the understanding of

the role which these hot electrons and hot phonons play is crucial to the further advancement of HFET devices. The accumulation of hot phonons, which will inevitably be a source of degradation in the device, and the fact that LO phonon (longitudinal optical phonon) scattering is the primary scattering mechanism at high fields in GaN means that ridding the channel of or minimizing these existence (in time) of hot phonons is the overall goal. Fortunately, the lifetime of the LO phonons is not constant, and it will be through the exploitation of this fact that we gain the ability to tune the performance and reliability of HFETs. This may be achieved through proper device design and by operating the HFETs at particular bias conditions which tend to lend themselves to short LO phonon lifetimes.

2.5.a. Measured Drift Velocities in GaN 2DEGs

The primary performance parameter for a HFET is the velocity, v, which can be achieved by electrons in the channel of the device. At low fields, the velocity follows a simple relation, namely the product of the low field mobility, μ, and the applied electric field, F.

$$v = \mu F$$

Equation 6

This is the ohmic regime of device operation, where the velocity increases linearly with the applied field. However, at high fields, the mobility in a semiconductor ceases to be independent of the applied field as additional scattering suffered by the electrons tends to cause the velocity to saturate. In the traditional view, one can expect the velocity of an electron in a polar semiconductor to saturate when the electron kinetic energy approaches the optical phonon energy, $\hbar\omega_{LO}$; here electrons tend to emit copious quantities of optical

phonons. The emission and reabsorption of optical phonons constitute the dominant scattering mechanism at high fields and this scattering limits the mobility and subsequently the velocity of the carriers:

$$v_{sat} = \sqrt{\frac{\hbar\omega_{LO}}{m_e^*}}$$

Equation 7

where m_e^* is the effective mass of the electron in the channel. For a GaN channel, $\hbar\omega_{LO} \approx 92$ meV and m_e^*=0.24 which results in an expected saturation velocity of ~3 x 10^7 cm/s. In fact, a GaN HFET oftentimes achieves a maximum velocity 2-3 times lower than this, which was the source of some controversy until recently.

Although a GaN p-i-n diode was observed to have a peak velocity as high as 7 x 10^7 cm/s (under a femtosecond pulse-probe measurement), this constitutes a peak transient value, occurring during the first picosecond or so of applied bias. Of course, we are interested in the steady state velocity, at least after the density of optical phonons has reached its (nonequilibrium) steady state value. Generally, velocity in a 2DEG is measured either through an analysis of cutoff frequency measurements (as explained in 2.4.b. RF Performance), or through a pulsed IV technique wherein the velocity is deduced by applying a voltage between two ohmic contacts. Correcting for the contact resistance must be taken into consideration, wherein the actual applied field, *F*, is then deduced:

$$F = \frac{(V - IR_C)}{L}$$

Equation 8

Where L is the separation between contacts and R_C represents the total contact resistance. If care is taken to ensure that the electron concentration is independent of the applied field (i.e. no electron injection), the drift velocity can be deduced as:

$$v_d(E) = \frac{J(E)}{Ne}$$

Equation 9

Where *J(E)* is the current density and *N* is the electron concentration. By using short pulses of voltage (in the range of nanoseconds), the effect of Joule heating can be avoided; that said, the nanosecond time scales of the pulses are long enough for the system to reach its steady state (in terms of the phonon population). The LO phonon population reaches its steady state in timescales on the order of 5ps.[121]

Using this pulsed IV method to ascertain electron velocities, Barker *et al*[122]. claimed to have measured a peak velocity in $Al_{0.25}Ga_{0.75}N$/GaN of 3.1 x 10^7 cm/s at a field of 140kV/cm. They compared their results to a Monte Carlo simulation that did not include hot phonons[123] and yet had reasonable matching with their data. They claimed that the quality of the contacts was very important as one device was presented with a maximum velocity of ~1 x 10^7 which had "Ti deficient" contacts. The effect of self heating may have played a role in their measurements as the velocity exhibited a peak—they used 200ns pulse width at 60Hz. Also suspicious is that the sample apparently had a sheet density of 1.95 x 10^{13} with mobility of 435, which is an exceedingly high sheet density and an unrealistically low mobility for an $Al_{0.25}Ga_{0.75}N$/GaN structure. Ardaravicius *et al.* measured an AlGaN/GaN structure using 3ns pulses to find a maximum velocity (no saturation) near 2 x 10^7 cm/s at a field of 130kV/cm. Their Monte Carlo simulation is in close agreement with the experimental values. In another report, using the same

technique but with 1ns pulse widths, Ardaravicius *et al.* reported a maximum velocity of near 2 x 10^7 cm/s at a field of 200 kV/cm (no saturation) for an AlGaN/GaN heterostructure while a structure with a 1.5nm AlN spacer layer exhibited a maximum velocity of 1.1 x 10^{13} cm/s at 100kV/cm. The low carrier density (4 x 10^{12} cm^{-2}) in the layer without the spacer is apparently the reason that the hot phonon effect is weaker as compared to the layer containing the AlN spacer layer (n_s=1.4 x 10^{13} cm^{-2}). Monte Carlo simulations match the experiment up to 30kV/cm using hot phonon lifetimes of 0.7ps and 1ps for the samples without and with the AlN spacer layer, respectively. Palacios *et al*. demonstrated an improvement in electron velocity when the AlN spacer layer was replaced with a GaN/AlN spacer layer (as already mentioned in 2.2.a. The Inadvertent GaN Interlayer). Using the pulsed current technique, the velocity observed increased from 1.2 x 10^7 (in the standard $Al_{0.22}Ga_{0.78}N$/GaN structure; n_s=9 x 10^{12} cm^{-2}, μ=1650 cm^2/V-s) to 1.5 x 10^7 cm/s (in the $Al_{0.22}Ga_{0.78}N$ /GaN/AlN/GaN; n_s=5-7.5 x 10^{12} cm^{-2}, μ=1460 cm^2/V-s structure) around 50kV/cm. Using the Moll analysis, a velocity of 1.6-1.8 x 10^7 cm/s was deduced for the standard structure while a velocity of 2.2 x 10^7 cm/s was deduced for the layer with a GaN/AlN spacer layer. The highest measured electron velocity in a GaN channel using this pulsed IV technique was obtained for an InAlN/AlN/GaN channel. The measured value of drift velocity was 3.2 x 10^7 cm/s. As already mentioned, it is unclear the reason for the enhanced velocity in this structure as compared to a structure with an AlGaN barrier and a similar carrier density.

This uncertainty aside, in order to obtain an understanding of the reason for the velocity saturation, we must have a discussion on scattering at high fields (which means LO

phonon scattering), inclusive of the effects of the buildup of LO phonons (hot phonons), all of which is discussed next.

2.5.b. Phonons in GaN

Before we explain the significance of the phonons on the drift velocity in a GaN 2DEG, let us briefly make some general statements about phonons. As is well known, the phonon is the quantum of momentum. Phonons can be visualized as vibrational modes among atoms in the unit cell. Therefore, phonons are synonymous with heat in a semiconductor. The phonon dispersion curves along several high symmetry directions along with the decay mechanisms for the dominant A_1(LO) phonon (red and blue arrows representing the anharmonic interaction via the "Ridley mechanism" LO→TO+LA) in bulk GaN is shown in Figure 27. As is expected from the fact that there are 4 atoms in the unit cell of GaN, there are a total of 12 phonon branches, 3 (low energy) acoustic, and 9 optical. Among these distinctions, the branches can be classified into longitudinal (vibrations in the direction of the phonon wavevector, q; 1 acoustic and 3 optical modes) and transverse (vibrations are perpendicular to the direction of the wavevector; 2 acoustic and 6 optical modes). The acoustic modes are associated with Joule heat and their interaction with electrons dominates at very low fields. At higher fields, electron coupling with acoustic modes becomes unlikely and the dominate mechanism of electron scattering is scattering (emission or absorption) with the optical modes. It turns out that the electron-TO scattering rate is more than two orders lower than the electron-LO

scattering rate,[124] and as such, the LO phonon modes are most important when considering electron scattering mechanisms at moderate to high fields in GaN.

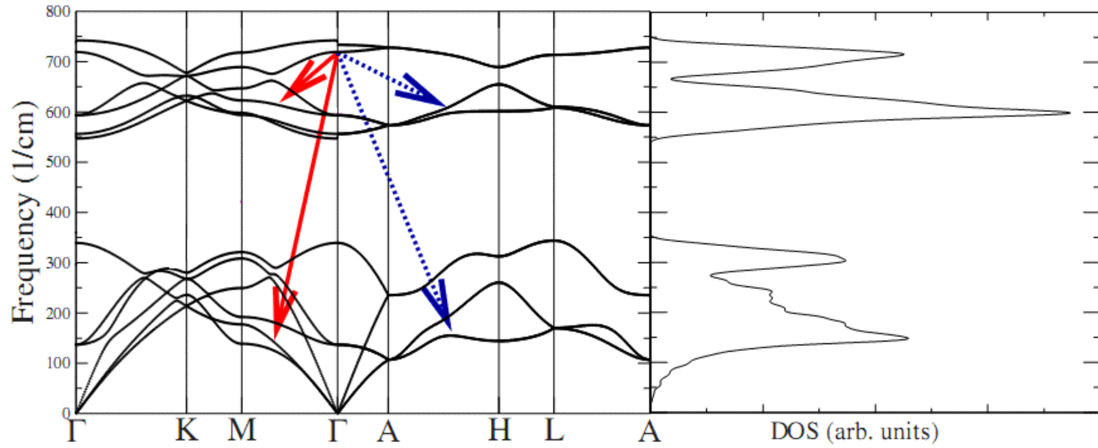


Figure 27. Phonon dispersion curves for GaN. The dominant decay routes are indicated by the arrows. After 125.

In order to understand the limit of the electron velocity in an HFET channel, one must consider the physical phenomena occurring as electrons traverse the channel. In the first place, one might attempt the use of the balance equations for energy and drift velocity:

$$\frac{\partial E}{\partial t} = (-eF)v_d - \frac{\hbar\omega_{LO}}{\tau_E(T_E)}$$

Equation 10

$$\frac{\partial v_d}{\partial t} = \frac{eF}{m_e} - \frac{v_d}{\tau_m(T_E)}$$

Equation 11

Where F is the electric field and $\tau_E(T_E)$, $\tau_m(T_E)$ are the energy and momentum relaxation times, respectively, as functions of electron temperature. The steady state solution of these equations is given by:

$$v_d = \sqrt{\frac{\hbar\omega_{LO}}{m_e}}\sqrt{\frac{\tau_m}{\tau_e}}$$

Equation 12

Unfortunately, these expressions cannot in general be used in a 2DEG because of the need to introduce a single electron temperature and particularly because the degeneracy in a 2DEG means that relaxation times are not simple functions of temperature. What can be said, however is that in a 2DEG, LO phonon scattering plays two roles in the drift velocity: on one hand, the momentum scattering tends to reduce v_d—this can be envisioned as electrons emit and reabsorb phonons at very high rates, this leads to no change in electron energy, but effectively randomizes the momentum of the electrons; this causes the drift velocity to decrease. On the other hand, the phonons give the electrons their only opportunity to dissipate their energy—without the phonon scattering, the electrons would reach energies in the conduction band where either scattering to satellite valleys or the negative effective mass in the Γ valley would begin to come into the picture—resulting in perhaps an even more dramatic reduction in drift velocity, but ultimately putting into question the feasibility of achieving negative differential resistance as the optical phonon scattering would preclude the electrons from reaching energies high enough to allow for scattering into upper valleys. Thus, the role of phonon scattering is beneficial in this regard. The LO phonon scattering turns out to be necessary yet limiting the electron drift velocity that can be achieved. The key turns out to lie in the "lifetime" associated with the conversion of the energy contained in the LO modes into modes which can carry the energy away from the channel.

With this knowledge we now turn more specifically to the phenomenon of LO phonon buildup in the channel which again, is the limiting factor for electron drift velocity.

2.5.c. Removal of Heat—Hot Phonons

The primary consideration to achieve the optimal performance from a device which operates under high fields is the removal of heat (phonons) from the device. When considering the removal of heat from devices, the classic approach that practitioners employ is with regard to the removal of acoustic phonons (Joule heat) through the system heat sink. Of course in this vein, a substrate with a high thermal conductivity (such as SiC) has found widespread popularity. However, the dissipation of energy (heat) of electrons in an FET channel is only limited by the removal of acoustic phonons through the heat sink for very low supplied powers imparted on the electrons (>1nW/electron). At higher supplied powers (which would be present in practically any GaN-based HFET), the temperature of electrons in the channel increases rapidly until electrons are capable of emitting longitudinal optical (LO) phonons.

Phonons can be thought of like an ordinary boson "gas" of particles; as such, we consider them to have a distribution congruent with a boson gas heated to a temperature T_{ph}:

$$N_{ph} = \frac{1}{e^{\frac{\hbar\omega}{k_B T_{ph}}} - 1}$$

Equation 13

If one were to compare the power supplied to electrons in a GaN 2DEG to the amount of power that would be dissipated by an equilibrium distribution of LO phonons (cold phonons), one arrives at the conclusion that the dissipated power actually exceeds the supplied power by a factor of 30.[126] Obviously, this cannot be—an equilibrium distribution of phonons is incorrect—the phonons have some other distribution associated with elevated temperatures, we have "hot" phonons. Therefore, we have essentially two

sets of phonons in the channel, the "hot" modes, associated with the nonequilibrium "hot phonons", and additionally the equilibrium "cold" modes (associated with the lattice temperature). The physical origin of the hot phonons is the fact that the time associated with the emission of LO phonons is much shorter than the time associated with the decay of these LO phonons into propagating LA modes (Ridley mechanism). Thus, the (relatively stationary) LO phonons tend to build up and it is no longer possible to describe them in terms of their equilibrium distribution.

Considering that energy is conserved, supplied energy must equal dissipated energy. The energy dissipation is given by:

$$P_d = \frac{\hbar\omega}{\tau_{sp}}\left(1+N_{ph}\right)p_ - \frac{\hbar\omega}{\tau_{abs}}N_{ph}p_+$$

Equation 14

Where τ_{sp}, τ_{abs} are the average times associated with spontaneous emission of and absorption of an LO phonon by a hot electron, respectively, and $p_$, p_+ are the probabilities of finding a hot electron ready to emit (-) or absorb (+) an LO phonon:

$$p_\pm = \frac{1}{n_{2D}}\int D(E)f(E)\left\{1-f\left(E\pm\hbar\omega_{LO}\right)dE\right\}$$

Equation 15

Where E is electron energy, $f(E)$ is the temperature dependant Fermi function, $D(E)$ is the density of states and n_{2D} is the density of the 2DEG.

Thus, we can plot the power dissipated by a distribution of hot phonons at arbitrary temperatures and graphically obtain the phonon temperatures as a function of the (measured) electron temperatures, Figure 28. By collecting the intersection points in Figure 28, we find that the phonon and electron temperatures are very close to one another, Figure 29. Thus, the hot electrons and hot phonons constitute an isolated (since

electron interaction with acoustic modes is very weak) subsystem, where the only way to drain energy from the subsystem is to remove the LO mode heat through LO mode decay.

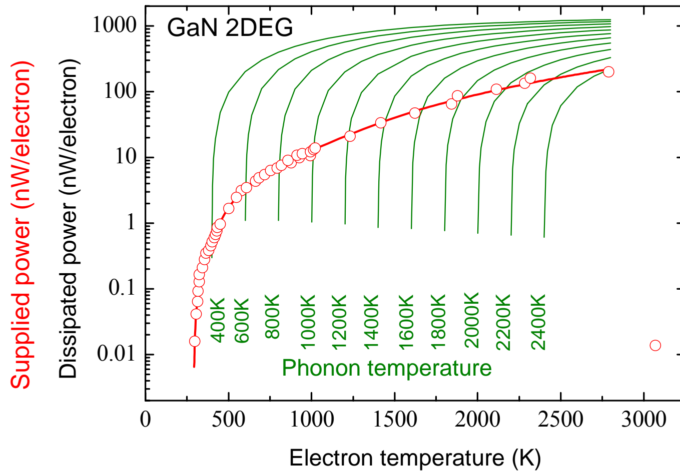


Figure 28. (Green curves) power dissipated by hot phonons at a number of phonon temperatures. (Red) experimental electron temperature as a function of supplied power. The intersection of the curves gives hot phonon temperature for a given hot electron temperature. After 127.

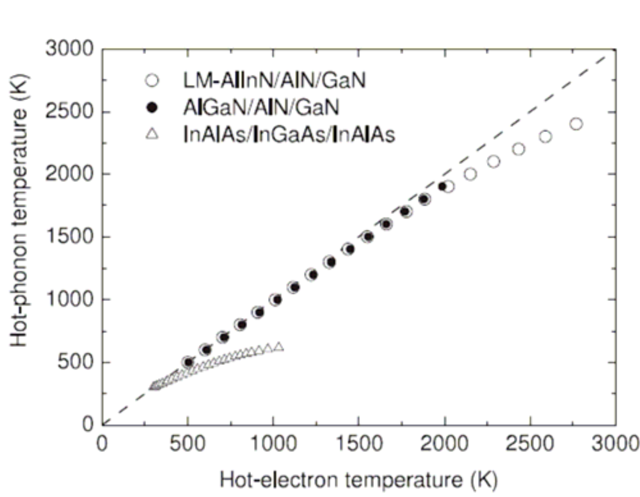


Figure 29. Hot electron temperature and hot phonon temperature. The dashed line represents hot phonon temperature equals hot electron temperature; it is clear that in GaN channels, the hot phonon and hot electron temperatures are nearly equal. From 128.

This phenomenon is illustrated schematically in Figure 30. Since the hot electrons cannot efficiently dissipate their energy into acoustic modes and the hot electron and hot phonon

temperatures are very close to one another, the hot electrons and hot phonons constitute a nearly isolated subsystem wherein their only access to the thermal bath is through the decay of the hot phonons into acoustic modes.

Reiterating from the previous section, once an electron has emitted an LO phonon, the extraordinarily high Fröhlich interaction afforded GaN means that the likelihood of reabsorption of the LO phonon is very high. Thus, if the emission and reabsorption of LO phonons takes place before the LO phonon disappears (it disappears only if the LO phonon were to decay into propagating acoustic modes, since group velocity of LO phonons is very low, see Figure 27), the energy of the electron would be largely unchanged while the momentum were effectively randomized. It is the slowness of this LO→LA conversion process which gives rise to the so-called “phonon bottleneck” in GaN, which ultimately limits the performance of the HFET (in terms of electron velocities which can be achieved) and in fact is intimately linked to the reliability of GaN-based HFET devices.

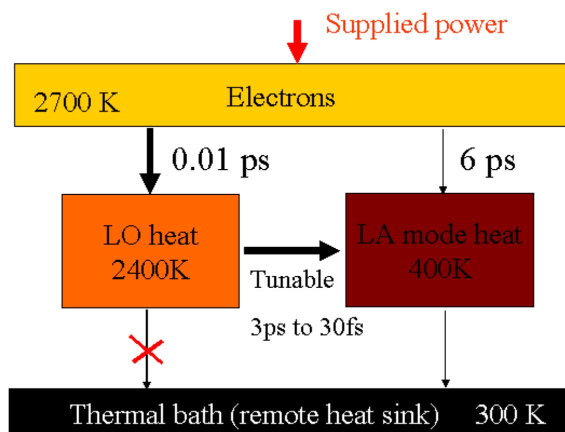


Figure 30. Schematic of the dissipation of heat in GaN at high fields. The only means of transferring energy out of the hot electron/hot phonon subsystem is through the hot phonon decay into acoustic modes. Note that if the hot electron and hot phonon temperatures were equal, no energy would be dissipated. After 129.

As mentioned above, the dissipation of the energy of the electrons in a GaN channel cannot be described in terms of equilibrium phonons. The nonequilibrium LO phonons launched by hot electrons are intimately related to the velocity which can be achieved by an HFET device. In addition to affecting the performance of the HFET device, the nonequilibrium phonons are linked to the reliability of the GaN-based FET devices in that the generation of large quantities of hot phonons will inevitably lead to the generation of defects, particularly in a piezoelectric and pyroelectric material such as GaN. In order to understand why the hot phonons would generate defects, consider that the distribution function for hot phonons in the channel of an FET is such that the occupation is extremely dense, that is in a relatively narrow portion of the k-space, Figure 31. In this regard, the generation of locally large atomic vibrations and subsequent new crystal defects is likely.

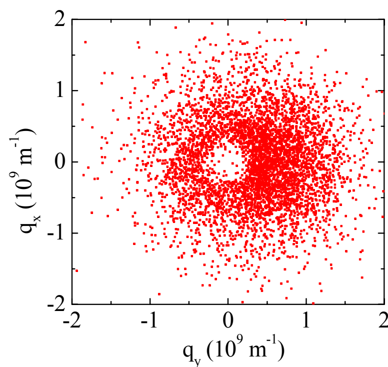


Figure 31. Calculated distribution of hot phonon modes in AlGaN/AlN/GaN at room temperature for an applied electric field of 20kV/cm. After 130.

As mentioned above, it is the so-called lifetime of the LO phonon that is the culprit for the phonon bottleneck and the subsequent deleterious impact on performance and reliability. While there are a number of decay channels available to optical phonon modes

in the general sense, the highly ionic nature and large value of the energies of the optical phonon branches (compared to the acoustic branches) of GaN makes all but the so-called Ridley mechanism inaccessible.[131] In the Ridley mechanism, the LO phonon is known to decay: LO→TO+LA.[132] However, this Ridley process takes place in characteristic time scales much longer than those associated with LO phonon emission or electron-phonon scattering for that matter. Therefore, the density of LO phonons can build up[133] and cause even more scattering between the electrons and these phonons.[134] The TO phonon lifetime is known to be shorter than the LO mode, and additionally electron-TO scattering is known to occur a rate two orders of magnitude lower than the electron-LO scattering; thus, once the LO phonon has decayed, via the Ridley mechanism, we can disregard the effect of the daughter TO mode.

As phonons build up and exceed the equilibrium concentration of phonons, N_0, we refer to them as "hot". The time associated with the disintegration of these hot phonons into the short lifetime TO and more mobile LA phonons can be referred to as the hot phonon lifetime. Clearly, this lifetime is responsible for the density of the phonons that are built up in the channel.

A long lifetime leads to a larger buildup of hot phonons in the channel, and as one would expect, causes more scattering and in turn causes the overall drift velocity to suffer. Figure 32 shows the results from a Monte Carlo simulation of the drift velocity in an AlGaN/GaN channel versus the hot phonon lifetime.[135] Clearly, a short hot phonon lifetime is desirable for HFETs so that drift velocity, v_{sat}, can be maximized and therefore from a performance point of view, cutoff frequency, $f_T = \frac{L_G}{2\pi v_{sat}}$, for a given gate length can be increased.

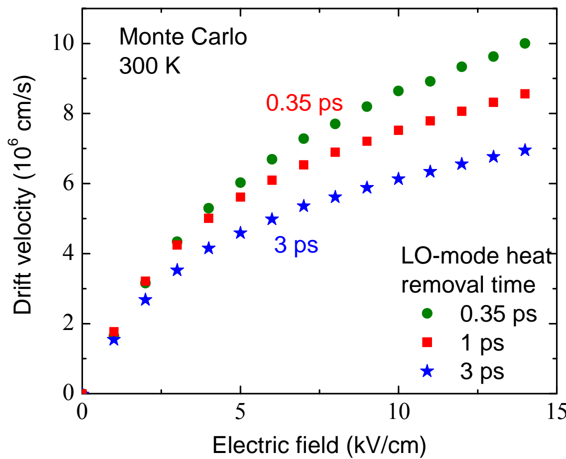


Figure 32. Monte Carlo simulation of the electron drift velocity (vertical axis, x 10^6 cm/s) versus applied electric field under the assumption various LO phonon lifetimes. After 135.

The decay of hot phonons is the fundamental bottleneck for transferring heat out of the channel of the FET and the fundamental reason for reduced average carrier velocities in GaN channels in HFET devices. This gives rise to both a reliability problem as the heat buildup can cause defects to form, particularly in the case when existing defects are already present, and additionally, causes the frequency performance of the devices to suffer. The question then is what the value of the hot phonon lifetime is and how one might attempt to design a device in such a way as to minimize it.

2.5.d. The Hot Phonon Lifetime II and its Measurement

In addition to the traditional influence of the anharmonic interaction on decay of LO phonons, it has become clear that the hot phonon lifetime is also related to the density of carriers in the system. Subpicosecond time-resolved Raman studies showed that the hot phonon lifetime decreased from about 2.5ps to 0.35ps as the carrier density increased

from 10^{16} to 10^{19} cm^{-3} (Figure 33).[136] Estimating the "bulk" carrier density in an HFET channel simply by dividing the sheet density by the width of the triangular quantum well at the Fermi energy we see that such densities and even higher are readily attainable in the GaN channel of a HFET. In actual HFET structures, however, the Raman measurement is difficult to perform and in actuality the measurement of hot phonon lifetime is carried out using the microwave noise technique.[137]

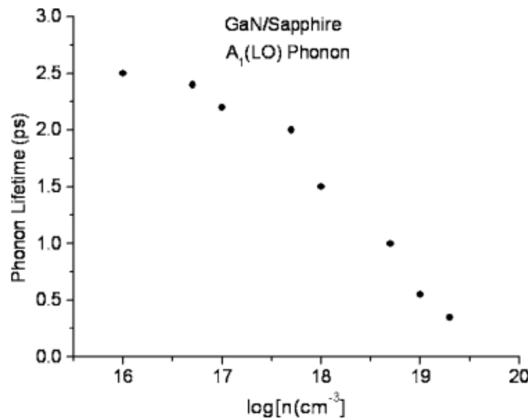


Figure 33. Hot phonon lifetime measured by time-resolved subpicosecond Raman spectroscopy. After 136.

In the noise technique, a sensitive radiometer is placed at the output of a pair of ohmic contacts. During the voltage pulse, the noise power (the noise arises due to current fluctuations in the channel) is measured and compared with that of a blackbody which has a known temperature. When the two powers are equal, it is deduced that the electron noise temperature is equal to the temperature of the blackbody. Thus, the electron noise temperature can be measured. The measurement is performed at high frequency (10GHz) where the low frequency sources of noise such as 1/f noise and those associated with trapping can be neglected. If the confining barriers are high enough such that real space transfer of the electrons is suppressed (when an AlN spacer layer is employed), the noise

can only be attributed to electron-phonon interactions. Further experimental evidence that the electron noise temperature very nearly equals the noise temperature was independently observed in electroluminescence[138] and photoluminescence[139] measurements.

Armed with the electron temperature and knowing the power supplied to the channel, the energy relaxation time of the electrons can be estimated as

$$\tau_{energy} = k_B \frac{dT_e}{dP_{\sup}}$$

Equation 16

Experimental and calculated results using this technique are shown in Figure 34. As expected, at very low powers, energy relaxation times are very long, associated with electron interaction with acoustic phonons. At high fields when electrons have sufficient energy to emit optical phonons, the LO phonon interaction dominates and relaxation time becomes nearly independent of the supplied power. Also evident is the rise in energy relaxation time as the electron density increases—the hot phonon effect is stronger when electron density is high when degeneracy is taken into consideration. This is understood as follows: If one were to ignore the Pauli principle for a moment, it is more probable that the electrons scatter into states such that their velocity after scattering is very close to the direction of the applied electric field, “small angle events”. When one obeys the Pauli exclusion principle, these “small angle” states to which electrons prefer to scatter are more likely to already be occupied when there are more electrons in the system; electrons will tend to scatter to higher angles, which of course implies a longer energy relaxation time.[140]

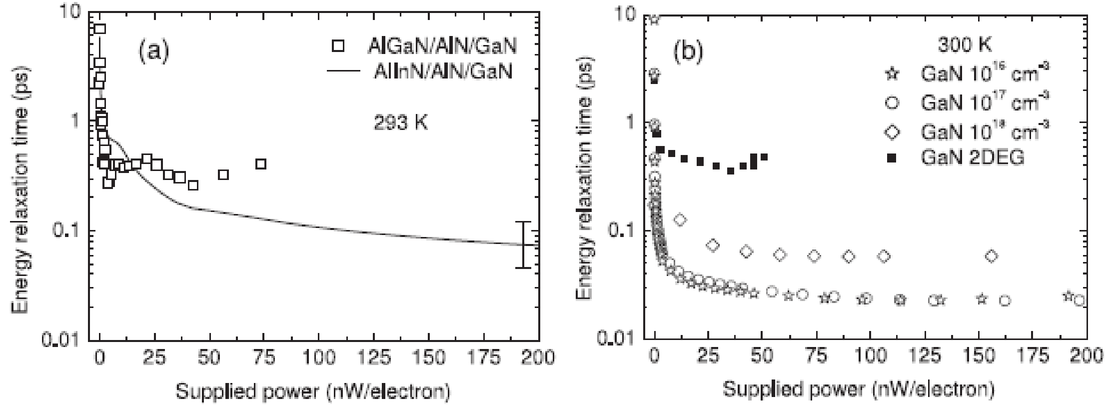


Figure 34. (Left) Experimental and (right) Monte Carlo simulation of energy relaxation time as a function of the supplied power to various GaN channels. As the 2DEG density increases, the relaxation time increases. From 128.

The data assumed a constant lifetime of the LO phonons (lifetime for the disintegration of phonons). However, in the case of our InAlN/AlN/GaN HFET, the measured noise temperature (electron temperature) versus supplied power was not linear. This suggests that the hot phonon lifetime was in fact NOT constant in supplied power. According to 135 the lifetime of the hot phonon is related to the occupancy of the hot phonon modes:

$$\frac{dN_{ph}}{dt} = -\frac{N_{ph} - N_0}{\tau_{ph}}$$

Equation 17

Where N_0 is the equilibrium LO phonon mode occupancy and N_{ph} is the occupancy, Equation 13, at the hot phonon temperature. From Figure 28 and Figure 29, we have all that is necessary to determine the hot phonon lifetime as a function of supplied power using the noise technique.

The first work utilizing this technique found a hot phonon lifetime of 350fs for an AlGaN/GaN 2DEG. While this value was nearly an order of magnitude lower than Raman measurements of hot phonon lifetimes in bulk GaN, very similar results (380fs)

were obtained for similar samples (grown in the same laboratory) when measured by an intersubband absorption technique.[141] The noise technique proved to be a valuable tool for the measurement of hot phonon lifetime in a 2DEG (measurements of hot phonon lifetimes in 2DEGs using the Raman technique are difficult if not impossible to obtain). Various experimental data on the hot phonon lifetime in GaN 2DEGs obtained through this noise technique are illustrated in Figure 35 (red points). Also shown in the figure is the available data of the energy relaxation time in a GaAs-based channel (black). The nonmonotonic behavior is explained next.

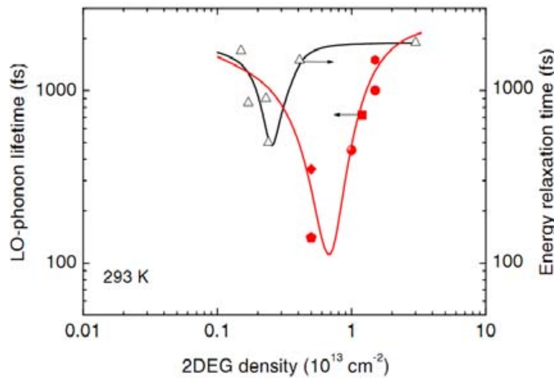


Figure 35. A survey of measured hot phonon lifetimes for various 2DEG channels utilizing GaN (red points and curve) and measured energy relaxation times in various GaAs channels (black points and curve). After 128.

The dependence of the lifetime on the density of carriers is understood in terms of the coupling of LO phonons with plasmons.[142] Figure 36 shows the dispersion curves for phonons and plasmons; at some "ideal" density, phonon-plasmon resonance is achieved and phonons and plasmons constitute a coupled mode (a phonon-plasmon quasiparticle). Since we know the energy of the coupled mode to be close to that of the bare LO phonon, we call this entity the hot phonon. In the following, we will consider the plasmon modes which exist in the 2DEG to be "bulk" modes, despite the obvious problem that the 2DEG

is NOT an infinite electron plasma. Considering the 2DEG to be an infinite electron plasma, the plasmon and phonon frequencies are in resonance when the electron density,

$$n_{res} = \omega_{LO}{}^2 \frac{m_e^* \varepsilon}{e^2}$$

Equation 18

where ω_{ph} is the phonon frequency and ε is the dielectric constant.[143] This optimal electron density for GaN is estimated to be around 6.5 x 10^{12} cm^{-2} for a 2DEG GaN channel. This means that for electron densities greater than or less than the density at phonon-plasmon "resonance", the lifetime increases which bodes poorly in terms of performance and reliability. Therefore, optimal performance will be achieved only when care is taken to optimize the actual density of carriers in the channel of the HFET.

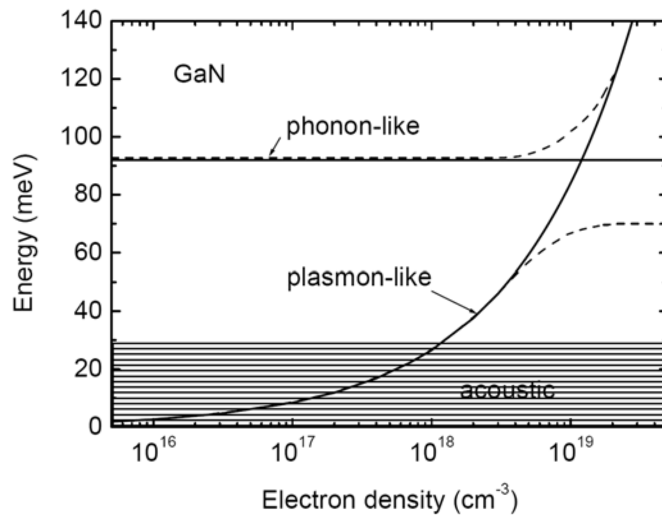


Figure 36. Dispersion of phonons and plasmons on electron density for bulk GaN. The solid lines neglect the coupling while the dashed lines include coupling.

Despite the crudeness of the model put forth (i.e. assuming that the plasmon modes are bulk-like), the prediction of an optimal phonon lifetime for an electron density near 7 x 10^{12} cm^{-2} for a GaN channel appears to be in reasonable agreement with measured values of hot phonon lifetimes at low fields for various layers with different 2DEG densities, as

shown in Figure 35 (red curve and data points). Such a phenomenon also appears in the GaAs case; the effect of phonon-plasmon resonance can be observed when considering the electron relaxation time versus the 2DEG density since the decay of hot phonons limits the hot-electron relaxation time. The resonance occurs at a lower 2DEG density in the GaAs system due to the smaller phonon frequency and effective mass in the GaAs channel, as expected. While the coupled phonon-plasmon model seems reasonably accurate in its prediction of the behavior of hot phonon lifetime in terms of its dependence on carrier density in GaN channels, it is not well understood what the actual mechanism for hot phonon decay truly is. Initially, Dyson put forth a "migrating phonon" model where the lifetime was reduced effectively by the physical removal of the hot phonon from the channel, once the phonon was coupled with a plasmon. The group velocity of the hot phonon-plasmon quasiparticle was shown to be several orders of magnitude larger than that of the LO phonon itself.[144] The idea being that the quasiparticle simply migrates to the edge of the channel where it subsequently decays. Unfortunately, the quasiparticle cannot exist outside of the channel (no plasmon modes exist in the insulating layers outside of the channel) and this model assumes that decay occurs immediately when the quasiparticle reaches the channel/dielectric boundary, reflection of the quasiparticle back into the channel was neglected. Nevertheless, the model is unreasonable in light of the results in reference 145. This will be explained further shortly. Further refinement of the phonon-plasmon model is required to more fully understand the mechanism of the hot phonon decay in HFET devices.

In light of the evidence that an optimal hot phonon lifetime exists, the use of very high density 2DEGs in structures employing, i.e. InAlN barriers, must be reconsidered. That

said, the inclusion of a GaN interlayer can reduce the 2DEG density as described in 2.2.a. The Inadvertent GaN Interlayer, which if controlled, could allow for the benefits of a stain free layer (high reliability) coupled with a short hot phonon lifetime. This would constitute one way to engineer or tune the hot phonon lifetime in the growth stage. Nevertheless, in a given device with a known 2DEG density, if we can change the density in some systematic way by using bias, we could also tune the hot phonon lifetime. Such tuning will essentially amount to a tuning of the device performance or reliability, if performance and reliability are in fact related to hot phonons, as we have argued. The tuning of both the performance and reliability of HFETs using bias to tune the hot phonon lifetime constitutes the first demonstration of tuning on which this thesis now focuses.

2.5.e. Tuning of the hot phonon lifetime

The information that is coming to light regarding an optimal 2DEG density in terms of hot phonon lifetimes must be exploited in order to devise schemes to maximize device performance. We seek to somehow increase the decay rate of hot phonons. With the promise of the existence of an optimal 2DEG density, one can take care to design devices or bias them in such a way as to achieve the optimal 2DEG density, at a given bias point, if one wishes to achieve the best possible frequency performance from the devices.

2.5.e.i. Ungated Structures

The first evidence of the ability to tune the hot phonon lifetime was performed by Matulionis *et al*.[145] In this work, the hot phonon lifetime was controlled by changing the

power applied to a gateless channel of an InAlN/AlN/GaN HFET structure, Figure 37. The power dependant measurement allows probing of the hot phonon lifetime versus sheet density because as the power applied to the channel increases, electron temperature increases and the wavefunction spreads over a wider spatial range, due to the filling of upper subbands in the quantum well, which effectively decreases the value of the carrier density, Figure 38. This being the case, one should consider the effect of the applied power on the value of the density at which resonance occurs; as the carriers become hot, the plasmon resonance frequency reduces and the sheet density associated with the point at which resonance occurs actually increases, which also increases the value of the "ideal" sheet density. This means that under high bias the "ideal" sheet density of 6.5 x 10^{12} cm^{-2} increases, even before one considers the reduction in 2DEG density associated with high carrier temperatures. Evidence for the power dependent hot phonon lifetime was presented in Ref. 145, and is illustrated alternatively in Figure 39, along with a number of other GaN 2DEGs (open squares, details on each of layers are in 145). For a device with a 2DEG density of 0.8 x 10^{13} cm^{-2} (closed squares), the value of hot phonon lifetime tends to decrease to a minimum and subsequently begins increasing again as the power applied to the 2DEG is increased further and further, Figure 1, closed squares. The solid lines are a fit to the data using a simple resonance curve:

$$\tau_{LO} = a\left\{1 + \frac{b}{\left(\sqrt{n} - \sqrt{n_{res}}\right)^2 + c}\right\}^{-1}$$

Equation 19

where n is the 2DEG density, n_{res} is the 2DEG density at the phonon-plasmon resonance, and *a, b,* and *c* are fitting parameters which control the value of the lifetime far from

resonance, the “sharpness” of the resonance curve, and the value of the minimum lifetime. The value of n_{res} is shifted to higher electron densities as the applied power increases, to match the data reported in 145. The minimum hot phonon lifetime of ~30fs was measured at a power of ~20nW/electron, which is the lowest observed hot phonon lifetime in a GaN 2DEG channel, Figure 37.[145] Since the sheet density was only very slightly above the resonance condition at zero field (8 x 10^{12} cm^{-2}), a relatively low power was necessary to effectively shift into the resonance condition. This translates into a hot electron temperature of only 600-700K, which is too low for the migrating phonon model discussed above to cause the observed decrease in hot phonon lifetime.

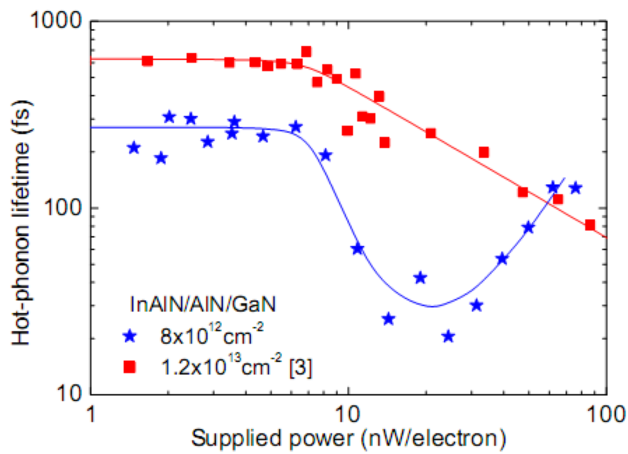


Figure 37. Hot phonon lifetime versus applied power for two InAlN/AlN/GaN channels demonstrating the effect of the phonon-plasmon resonance. After 145.

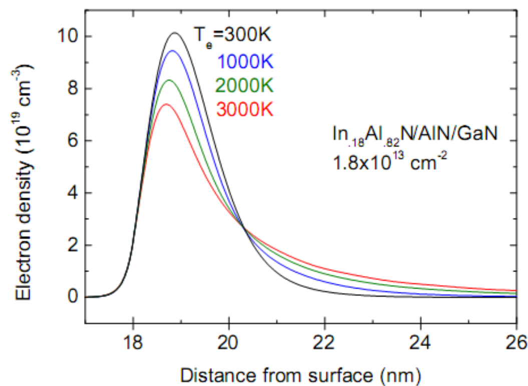


Figure 38. Electron density at various electron temperatures. After 143.

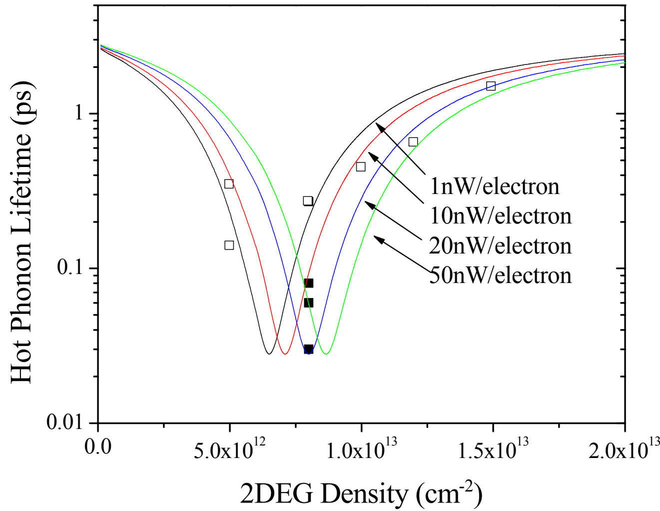


Figure 39. Fitted phonon-plasmon resonance curves after Equation 19 (solid lines) for measured phonon lifetimes at low field (open square), and for selected powers applied to the device presented in Figure 37.

2.5.e.ii. Gated Structures—Transit Time

The evidence presented thus far related to an optimum 2DEG density and the ability to tune the hot phonon lifetime by changing the applied power was all gathered using gateless channels (simple ohmic contacts on an etched mesa that are separated by a distance ~5-10μm). Such structures are simpler to analyze because the electric field is readily available through the applied voltage, separation between contacts, and the ohmic contact resistance. However, in order to truly exploit the information that has been gathered related to hot phonon lifetimes in GaN channels, we would like to find similar evidence in more realistic device structures, or in actual devices. While the analysis becomes difficult to quantify when using actual devices, the search for a dependence of hot phonon lifetime on sheet density is the focus of the following and the subsequent

sections, and constitutes the HFET performance tuning that we set out to demonstrate in the first place.

As already mentioned, we expect that in actual HFET structures, the mitigation of hot phonon effects through bias tuning should allow us to enhance the performance of the device. Specifically, we expect that the intrinsic transit time should be shorter at the particular sheet density associated with minimum hot phonon lifetime as opposed to densities slightly higher and lower than this density due the reduction in the deleterious hot phonon effects under the gate at the optimal 2DEG density. Although we are uncertain of the actual distribution of electric field and 2DEG concentration under the gate of a biased FET device, we expect to be able to observe a change in the intrinsic transit time as a function of bias.

We start the experiment by selecting an InAlN/GaN HFET device which has good microwave performance. The details of the fabrication and DC performance of typical devices was already discussed in 2.3.b. Fabrication of InAlN HFETs and 2.4.a. Mobility and DC Performance.

Next, capacitance-voltage (C-V) measurements on Schottky diodes, which were fabricated alongside the HFET devices were conducted in order to estimate the 2DEG density by using the typical expression of:

$$n = -2\left\{ \varepsilon q A^2 \frac{d\left(1/C^2 \right)}{dV} \right\}$$

Equation 20

Here ε is the dielectric constant ($8.0*\varepsilon_0$ for InAlN), q is the electron charge, and A is the area of the diode. The electron concentration as a function of the depletion depth, $\frac{\varepsilon A}{C}$, is

plotted in Figure 40. An estimate of the 2DEG density as a function of applied voltage can then be obtained by integrating the density vs. depth profile with respect to the applied voltage, as shown in the inset to Figure 40. The 2DEG density changes linearly with the applied voltage, and the value at which the density approaches zero is estimated to be close to -4V, which is consistent with the transistor pinchoff voltage. The 2DEG density is an estimate because we know that the 2DEG density is not uniform under the gate when the device is under bias (i.e. at high drain biases). Nevertheless, such a technique constitutes a reasonable approximation of the 2DEG density as a function of the gate bias.

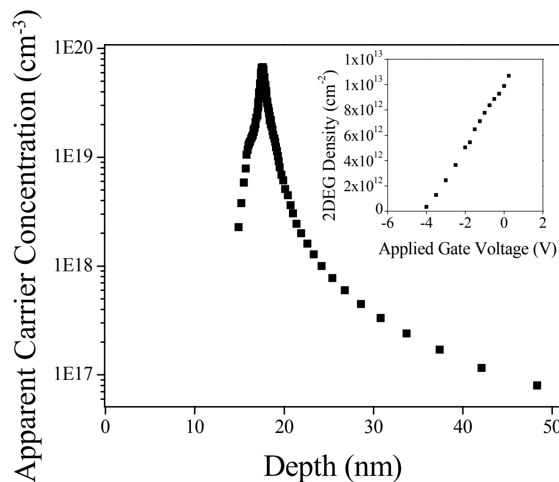


Figure 40. Electron density vs. depth profile deduced from the capacitance-voltage measurements of a Schottky diode and (inset) integrated electron density for various biases. The values represent the approximate 2DEG density at various biases.

Then, microwave measurements were performed and the transit time analysis was performed as discussed in 2.4.b. RF Performance. After determining $\tau_{int} + \tau_{RC}$ and $\tau_{int} + \tau_D$, we can calculate the intrinsic transit times at a given bias. The intrinsic transit time is plotted in Figure 41 as a function of the 2DEG density determined from the CV measurements (Figure 40, inset) for each of the drain biases used in the analysis. One can

see that a clear minimum in the intrinsic transit time exists for 2DEG densities near 9.3 x 10^{12} cm^{-2} for each drain bias. The electron velocity corresponding to the minimum transit time is estimated to be $v = \frac{L_G}{\tau_{\text{int}}}$ ~1.75 ± 0.1 x 10^7 cm/sec. Also in the figure, we include a fitting after Equation 19 (bold solid line); the best fit occurs using an optimal electron density of 9.5 x 10^{12} cm^{-2}.

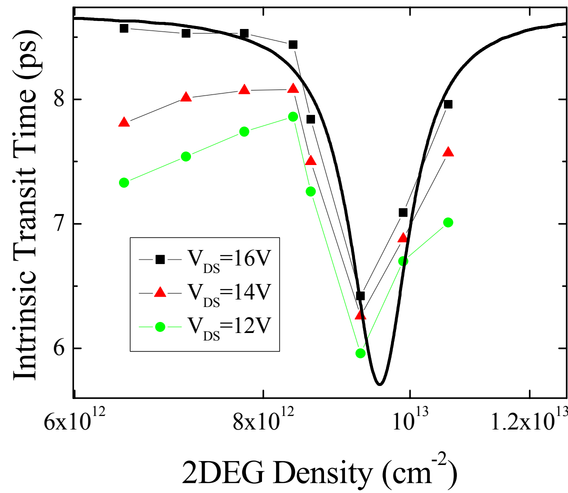


Figure 41. Intrinsic transit time as a function of the 2DEG density for three drain biases as well as the best fit using an optimal electron density of 9.5 x 10^{12} cm^{-2} (heavy solid black line). The 2DEG density corresponding to the minimum in the intrinsic transit time is consistent with that corresponding to the minimum in the hot phonon lifetime.

The existence of a minimum in the intrinsic transit time, or equivalently, a maximum in the electron velocity at a particular 2DEG density can be understood in terms of the hot phonon effect on the device performance which we discussed earlier. In the regime where the hot phonon effect is prominent, i.e. when electric field in the channel is high, we expect the velocity to increase as the hot phonon lifetime decreases. As illustrated in Figure 35, the hot phonon lifetime is a non-monotonic function and exhibits a minimum

for a 2DEG density near 6.5 x 10^{12} cm^{-2} at low fields, which increases with application of power. We estimate the applied power to electron in our device (at the bias conditions at which the intrinsic transit time is minimum) to be 0.058[A] x ($V_{applied}$ − (24[Ω]*0.058[A])) after correcting for the source and drain access resistances (measured under bias using the method presented in 146). Using this and the estimate of the number of electrons at the minimum (3[μm] x 90[μm] x 9.3 x 10^{12} [electrons/cm^2]), we estimate the average power dissipated per electron to be ~25-35nW/electron, for V_{DS} between 12 and 16V. Note that the difference in the powers applied when changing drain voltage from 12 to 16 only corresponds to an increase in power applied to the electrons of 1.25; therefore we do not expect to be able to resolve different positions of the velocity maximum (in terms of 2DEG density) for the drain biases shown in Figure 41. From the power dependent data presented in Figure 39, we would expect that a shift in the hot phonon lifetime curve resulting in a minimum lifetime occurring around 9.3 x 10^{12} should correspond to an applied power of ~>50nW/electron. Considering the simplicity of our approximations, and the fact that the actual electric field and subsequently the actual power applied is a function of the spatial position under the gate (in the region where hot phonon effects would tend to play the most important role, near the drain side of the gate, the actual electric field is quite large and the density of carriers would be reduced; the energy of these electrons would likely be much higher than the values estimated above), this value of 2DEG density for a minimum hot phonon lifetime in our device of 9.3 x 10^{12} cm^{-2} is quite reasonable in our opinion. The reason for the decrease in intrinsic transit time at higher reverse gate biases for the lower drain bias conditions is not fully clear at this time but could tentatively be attributed to a mitigation of the hot phonon effect for

low density 2DEGs or simply to a reduction in the Joule heating of the sample under lower applied power.

Summarizing this demonstration of hot phonon lifetime tuning, we observed a non-monotonically varying electron velocity in InAlN/AlN/GaN HFET structures, which we associate with the non-monotonic change in independently determined hot phonon lifetime. In light of the deleterious effects of hot phonons on device performance and reliability, we propose that optimal performance can only be expected when the device is operating under optimal bias conditions in which the 2DEG density associated with the given bias condition is congruent with the value associated with the shortest hot phonon lifetime. Such a demonstration of the tunability of the hot phonon lifetime arms us with the ability to control the device performance. As mentioned briefly before, we expect that the buildup of hot phonons should also play a negative role in the reliability of HFET devices. Knowing that we can control the hot phonon lifetime through the gate voltage, we are ready to demonstrate this additional deleterious effect of hot phonons. This is the subject of the next section.

2.5.e.iii Gated Structures—Reliability

In addition to the enhanced performance demonstrated in the previous section, we expect the degradation associated with the buildup of hot phonons in the channel, particularly at the drain side of the gate, to be reduced when the bias employed is that associated with minimum hot phonon lifetime. Furthermore, the InAlN system provides a unique opportunity for researchers to study the reliability of HFET structures in a material system that is not under tensile strain, which is fundamentally different than the existing

AlGaN-based HFETs. In this sense, we can expect the reliability of the InAlN-based structures to be even better than their AlGaN cousins since strain relaxation would not be a mode of degradation as the layers are not under strain. This paves the way for the buildup of hot phonons to be a major degradation mechanism in InAlN/GaN HFETs, and it is this mechanism and the mitigation of it through the tuning of the hot phonon lifetime which we will now demonstrate.

As we know, the nonequilibrium (hot) optical phonons have very low group velocity and as such tend to remain localized to the region where they are initially emitted, Figure 31. This means that at high fields, such as those present in an FET device, we expect phonons to actually build up in the region where they are being emitted (i.e. at the drain side of the gate where the field is largest). One can imagine that such a localized high density of phonons is likely a place where actual crystal defects may be formed. Subsequently, the formation of defects would cause observable changes in the performance of the transistor. Our aim is to observe the degradation of the performance of InAlN-based FETs as the devices are subjected to continuous operation under high fields for long periods of time. In our experiment, we controlled the electron density with the gate voltage and used gated Hall effect measurements for an estimation of the 2DEG density. Armed with this knowledge, we subjected the HFET devices to high field stress (V_D=20V) in the dark at room temperature. We stressed the devices for periods of time up to 20 hours, and observed the maximum drain current, peak transconductance, and channel access resistances every hour or half hour in order to quantify the device degradation. Simultaneously, we measured the gate leakage current during the stress and observed the level of degradation, at a fixed electron density, as a function of the total charge passed

through the drain and the gate electrodes. In this vein, we can fairly compare degradation of the devices subjected to low, moderate, and high current.

For all devices subjected to high field stress we observed a general trend of a reduction of maximum drain current and peak transconductance, as well as an increase in channel access resistances as stress proceeded. These observations are consistent with other reports in which devices were subjected to high fields and subsequent hot electron effects.[147,148,149,150] As plotting one of the parameters versus time would unfairly favor the low drain bias over the high drain bias (the assumption is that more current translates into more degradation since degradation should scale with the temperature in the channel—see Figure 24 and associated text—which is generally linear with the applied power[151]), we plotted the maximum drain current versus the cumulative current that has flowed rather than the time, Figure 42. We focus on the change in the maximum drain current as it is the most prominent feature of the degradation. The stress condition was V_D=20V, and V_G ranging from -3.5V to -6.5V. The highest degradation (which is associated with the largest changes in maximum drain current) takes place at high and low values of drain current, rather than being high for high drain current and low for low drain current, as would be expected if only the device temperature were driving the degradation.

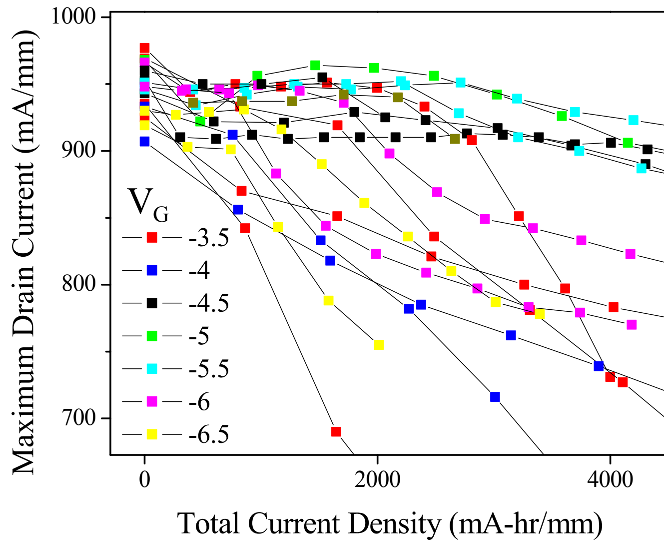


Figure 42. Maximum drain current measured as devices are subjected to DC biasing at V_D=20V, V_G=varied for a nearly lattice matched InAlN layer ("B"). The lowest rates of degradation occur not at highest or lowest currents, but at a moderate current, associated with the optimal 2DEG density. The maximum drain current is shown not as a function of time, but as a function of total drain current that has passed through the device.

In Figure 43, we replot the change in the maximum drain current for the specific case in which charge of 1500mA-hr/mm has passed through the drain. Here we have transformed the applied gate voltage to the measured value of the 2DEG density at each voltage, obtained from a gated Hall bar measurement. The stars in Figure 43 show the same albeit for devices wherein the drain voltage was reduced so that the drain–gate bias (V_{DG}=24V) is maintained in order to exclude possible degradation due to high V_{DG} for devices subjected to high negative gate bias, corresponding to electron densities below 9 x 10^{12} cm^{-3}. Clearly, the degradation rate exhibits a minimum at electron densities around 10^{13} cm^{-2}. This dependence on the 2DEG density shown in Figure 43 is strikingly similar to the dependence of the LO phonon lifetime on the 2DEG density, Figure 35. The figure shows that the degradation rate decreases to a minimum, then increases again as a

function of the average channel sheet density. This is despite the fact that at lower sheet densities, the devices are being subjected to lower power densities (and therefore channel temperatures)[152] and additionally devices subjected to comparable lateral fields still tend to degrade at higher rates. As such, we propose that the buildup of hot phonons plays a considerable role in the device degradation.

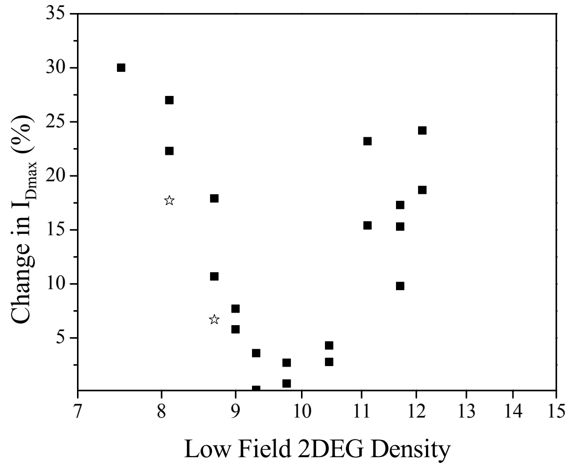


Figure 43. (a.) Change in maximum drain current after subjecting devices to high field electrical stress. The change is given for devices which have passed 1500mA-hr/mm of charge. The electron density is controlled by the gate bias. The stars represent devices that were stressed at a reduced drain voltage so that the devices were subjected to V_{DG}=24V, which is the same as that employed for the devices stressed with 2DEG density~10.5 x 10^{12} cm^{-2}.

If the degradation were attributable to the buildup of hot phonons, the least degradation would be expected at the 2DEG density around 6.5 x 10^{12} cm^{-2} where the shortest lifetime τ_{ph} is expected, Figure 35. Our stress measurements show the weakest degradation for slightly higher electron densities. This can be understood in light of the power dependence on hot phonon lifetimes presented in 2.5.e.i. Ungated Structures. Hot electrons tend to occupy a larger volume in real space when they gain energy from the electric field. Therefore, the “bulk” density of electrons decreases as the field applied to the channel increases. As a result, a higher 2DEG density is needed to reach the phonon–

plasmon resonance, and the minimum LO phonon lifetime is achieved at a 2DEG density exceeding the optimum value measured at low fields.

As a final endeavor in attributing the buildup of hot phonons as the primary degradation mechanism rather than some gate leakage related mechanism, we quantified the degradation for all the devices in this study as a function of the total amount of charge which has leaked through the gate, Figure 44. No systematic degradation with the gate leakage is found; some devices suffer high degradation with little gate leakage, some suffer little degradation with high gate leakage. The lack of the dependence on the gate leakage leads us inevitably to conclude that the gate leakage is not a major contributor to the degradation for these devices.

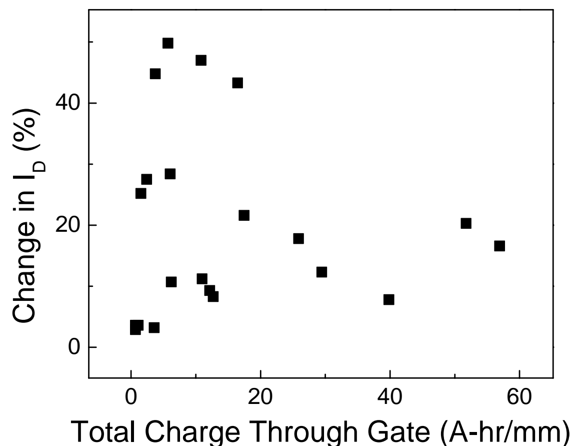


Figure 44. The total change in drain current for all devices in this study versus the total charge passed through the gate. The lack of any discernable dependence of degradation on the gate leakage indicates that the primary degradation mechanism is not related to the gate leakage.

In summary, we have demonstrated the importance of the buildup of hot phonons on the reliability of HFET devices. Furthermore, we have demonstrated that the tuning of the hot phonon lifetime, simply through the application of suitable gate voltages in order to achieve the optimal 2DEG density, is sufficient for enhancing the performance in

addition to enhancing the device lifetime of HFET devices. It is critical to be cognizant of such effects in order to achieve the ultimate performance from GaN-based HFETs.

2.6. Future Work for HFETs

The effect of hot phonons on HFET devices cannot be overstated—it is the reason that early Monte Carlo simulations predicted higher velocities than were initially achieved, it is a formidable source of degradation in HFET devices, and it essentially puts a damper on attempts to increase the 2DEG density in HFET channels in order to achieve higher and higher output powers. For this reason the ability to tune the LO phonon lifetime is an important finding and crucial for the graduation to the "next level" of device design. The hot phonon effect in GaN means that heat removal from devices must be contrived in the vein of removing energy from the channel itself as opposed to removing Joule heat through the heatsink—to a large degree, it moots the point of thermal conductivity when debating the use of one substrate over another. In addition to HFET devices studied in this thesis, the high Fröhlich interaction of GaN means that the hot phonon effect may plague other types of devices based on GaN, perhaps most importantly LED devices. In fact, the carrier spillover effect[153], a likely cause for the efficiency droop problem (the debate on its source rages today) on the LED front may in fact find some additional traction when hot phonon effects are taken into consideration. For example, as an electron comes travels into an active region of an LED structure (i.e. into a quantum well), it suddenly has an exceedingly high kinetic energy (dependant on the depth of the well), which means it will copiously emit optical phonons. A nonequilibrium distribution

of phonons could arise and then one can imagine electrons floating on the “pillow of hot phonons” rather than thermalizing and recombining in the well. This phenomenon would exacerbate the carrier spillover effect which has very important implications in the efficiency of LEDs at high injection levels.[154]

We know that the hot phonon effect can only be mitigated in 2DEG channels if the lifetime of hot phonons can be reduced. This may be achieved technologically by carefully designing the heterostructure such that the 2DEG density is optimal or through applied bias (via the power applied or gating) in order to reach the phonon-plasmon resonance when hot phonon lifetime is minimized. Of course, this means that the device would only operate optimally at this single bias condition.

If one were to ignore the plasmon effect on hot phonon lifetime, the only way to reduce the phonon lifetimes would be through an enhancement of the anharmonic rate, perhaps achievable by localizing the phonons in real space through the breaking of the crystal symmetry via intentionally introducing disorder into the system. As an example, by replacing the GaN channel with an InGaN channel[155], the alloy disorder might provide the random potential necessary to scatter the LO phonons and therefore the overall hot phonon lifetime in this system might be reduced. Of course, any benefits to be gained by the intentional introduction of disorder must offset the negative effect on electron scattering that disorder would also bring. Also the replacement of the GaN channel with an InGaN channel would help mitigate the hot phonon effect as the lifetime of LO modes is known to be shorter in InN as compared to GaN.[156]

However, if one is cognizant of the plasmon effect on hot phonon lifetime, one can envision using a carefully tailored heterostructure in which the total number of carriers in

the channel is high but the channel is designed in such a way as to effectively spread the 2DEG out, resulting in a lower density of the 2DEG. In this way, high powers can be achieved while simultaneously reducing the hot phonon lifetime. Simulation results of such a heterostructure, utilizing a 5nm $In_{0.11}Ga_{0.89}N$ "2DEG spreading layer" are presented in Figure 45. The number of electrons in the 2DEG of the GaN/InAlN/AlN/GaN/InGaN/GaN heterostructure is high (1.78 x 10^{13} cm^{-2}) but the density is lower than would be expected for such a large number of carriers (Figure 38 also shows the electron concentration for a 2DEG with the same number of carriers (1.8 x 10^{13} cm^{-2}); we have reduced the density by a factor of two by employing the InGaN spreading layer). Experimental work to realize such a structure would be an interesting piece of future work.

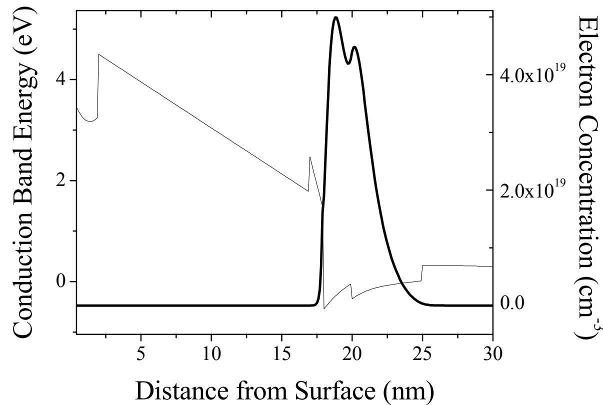


Figure 45. Conduction band edge and electron density for a novel GaN/InAlN/AlN/GaN/InGaN/GaN heterostructure with an $In_{0.11}Ga_{0.89}N$ "2DEG spreading layer" designed to have a large number of carriers but with a reduced density in order to mitigate the hot phonon effect. Experimental results utilizing such a structure should be performed in the future.

3. Tunable Phase Shifters

Tunable phase shifters are of practical importance for phased array antenna systems. The desire to develop radar systems wherein each antenna component can continuously tune the phase at which it is transmitting or receiving motivates the development of continuously tunable phase shifters, which are critical to the operation of phased array systems. Additionally, these systems are typically very large (on the order of meters) due to the large size of each of the antenna components. Therefore, continuously tunable, small phase shifters are desired for such systems.

Thin films of ferroelectric materials generally show a high dielectric permittivity that can be controlled by application of small DC bias voltages[157] to give rise to small, fast, and cost effective devices. As such, they have been studied for their adoption in advanced phased array systems. $Ba_xSr_{1-x}TiO_3$ (BST),[158,159] one of the most popular ferroelectric materials, has been utilized in the demonstration of various tunable microwave components including phase shifters,[160,161] resonators, and filters.[162] The high tunability of BST, defined as

$$Tuning = \frac{\varepsilon_r\big|_{0V} - \varepsilon_r\big|_{Vapplied}}{\varepsilon_r\big|_{0V}}$$

Equation 21

coupled with relatively low loss (loss tangent or tan δ) at microwave frequencies, fuels the further development of this promising ferroelectric material.

Although we mentioned that the films are ferroelectric, we would like to use a ferroelectric material in the paraelectric state. This means that the temperature of operation (i.e. room temperature) should be above the ferroelectric Curie temperature for the material. The motivation to use a ferroelectric in its paraelectric state is primarily because we want high tuning *and* low loss simultaneously. High tuning can be achieved in general in either state (ferro- or para-) for a ferroelectric film, when operating near the Curie temperature (also in fact, tunability tends to be high throughout the ferroelectric state); but in order to achieve low loss simultaneously, we want to avoid the intrinsic losses associated with the material in its ferroelectric state. As such, we choose to use a composition of BST of 50%, which has a Curie temperature of about 250K.[163] Perhaps more of a motivating factor is the fact that ferroelectric films will retain remnant polarization after being poled, which is not desirable for tunable microwave devices. This point perhaps more important only because regardless of whether we use BST films in the paraelectric state OR the ferroelectric state, the extrinsic losses (associated with defects and local regions of the crystal interacting with the microwave field) tend to dominate the loss that is achieved by researchers (particularly when using thin films), and perhaps the argument of using paraelectric films over ferroelectric films is not as important in terms of loss alone.

We will discuss the design, fabrication, and measurement of simple interdigitated capacitor (IDC) and coplanar waveguide (CPW) structures which can be used to determine the dielectric properties of the BST. A schematic of an IDC and a simple

symmetric CPW structure is outlined in Figure 46 (in general any two or three metal lines on a dielectric substrate can be considered as CPW lines, the symmetric style is easiest to model and suitable for our purposes). In addition to being useful for determining dielectric properties of the underlying films, the CPW structures can be used as simple phase shifters to determine the feasibility of using our films of BST for more advanced phase shifter designs or other passive microwave components. Additionally, we discuss our work with hybrid BST/ferrite based films, which are notable for use in phase shifters because of their unique property of being able to tune both the permittivity of the BST as well as the permeability of the ferrite films independently. This allows one to change the phase shift while independently changing the impedance of the device, which is important in attempting to address issues related to impedance matching and associated loss in the simple BST-based phase shifters.

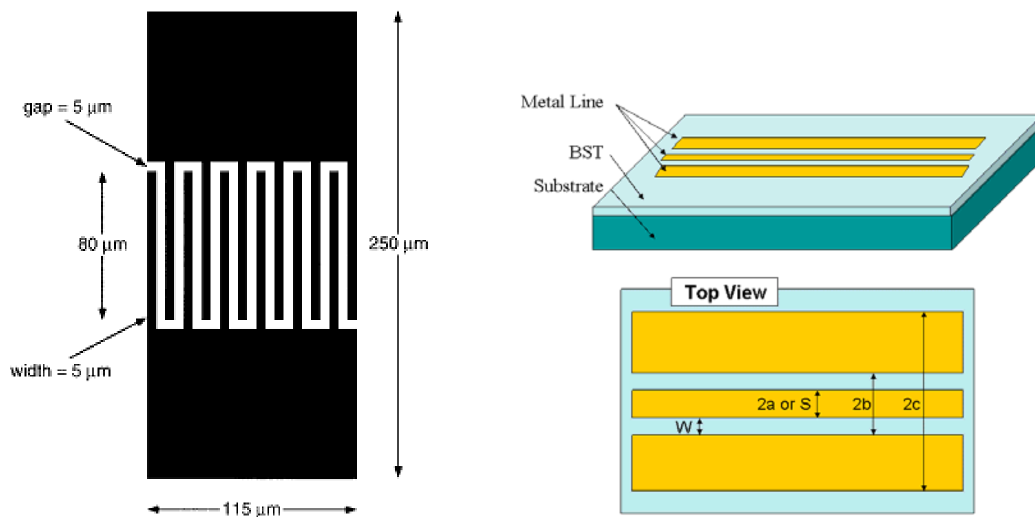


Figure 46. (Left) Layout and dimensions for the interdigitated capacitor structures used in this work, as well as in the work done by the NRL group (eg. Ref. 164) and (Right) Schematic of a coplanar waveguide. The center line is the "signal" line while the two outer lines constitute the "ground plane." The design geometries of interest (widths and separations of the lines) are indicated in the top view. Our CPW devices employ a signal line width, *S*, of 60µm and a separation between the edge of the signal line and the ground plane, *W*, of 5µm.

3.1. Growth of BST

A great deal of the existing reports on BST films have mainly focused on BST growth on MgO substrates.[164] However, the large lattice mismatch (6.3%) does not bode well for achieving high crystal quality of BST grown on MgO (poor crystal quality would lead to higher extrinsic losses in the BST films); additionally, MgO is a highly hygroscopic material, making working with MgO complicated. While we did some very preliminary work on MgO substrates in an effort to assure our ability to simply grow the films, the focus of this discussion is on BST on strontium titanate (STO) substrates, since we have a body of work on this material system. At first glance, STO appears to be a suitable substrate for BST thin films due to its very close lattice matching to BST (1.1% for $Ba_{0.5}Sr_{0.5}TiO_3$ films which are of interest to us), and in fact we have achieved very high quality films (in terms of XRD, (001) rocking curves show a FWHM as low as 2.4arcmin for thin films). Additionally, STO substrates are favorable for growth of BST as STO has the same perovskite structure as BST, negligible thermal mismatch[165], and a similar chemical nature (avoiding interface reactions and interdiffusion during the growth). Growth was done by pulsed laser deposition or sputtering.

Growth of BST thin films by sputtering was performed in an off-axis RF magnetron sputtering system using a 3-inch-diamater $Ba_{0.5}Sr_{0.5}TiO_3$ stoichiometric target. Ar and O_2 gases were introduced into the growth chamber through mass flow controllers to maintain the growth chamber pressure at 2 mTorr with an Ar-to-O_2 ratio of 6:1. During growth, the substrate temperature was nominally 750°C according to the thermocouple reading, and the RF sputtering power was set at 120 W. These growth conditions yield a deposition

rate of about 450 Å/h for the BST layers.[166] We studied properties of these sputtered films and additionally, used the sputtered films as seed layers for additional growth by PLD.

Our sputtered films of BST on STO substrates tend to suffer from a clamping effect, regardless of the growth temperature or other growth parameters (pressure, reactant gas flow rates, etc.), although thicker layers tended to relax somewhat as compared to thin films, Figure 47, and films grown at higher temperatures tended to have sharper XRD linewidths and were relaxed very slightly as compared to films grown at lower temperatures. The combination of these effects led to an improvement in tunability as compared to layers grown at low temperature, albeit the values of device tunability were still quite low as compared to other researchers' reports of BST on e.g. MgO substrates. The effect of clamping and the subsequent biaxial strain BST films is twofold: compressively strained BST films not only suffer from having an increased Curie temperature (below which the films are ferroelectric), also the (compressively) strained films suffer from lower dielectric constants, as predicted in 167, and lower tunability as reported in 168. In our films, the dielectric constant reduced from ~325 to ~125 at room temperature as the film thickness reduced from 1000nm to 160nm. As such, after initial growth experiments, our attempts shifted from improvement crystal quality to enhancement of strain relaxation.

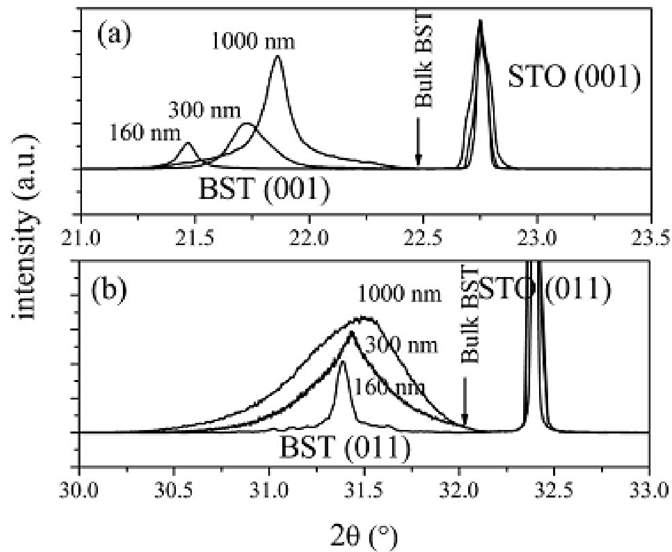


Figure 47. XRD of BST think films on STO with thicknesses ranging from 160 to 1000nm: (a.) symmetric (001) 2t-o scans and (b.) asymmetric (011) 2t-o scans. The expected position of bulk BST (3.497Å, ref. 169) is shown for comparison. After 159.

The clamping effect can be quantified by the ratio of the *c* to *a* lattice parameters measured from the symmetric and asymmetric XRD scans. A *c/a* ratio of 1 would correspond to an unstrained layer. For the "standard" layers shown in Figure 47, the *c/a* ratio decreases from 1.059 to 1.040 to 1.025 as the thickness of the layers increases from 160nm to 300nm to 1000nm. This compares to a value of 1.023 for the film grown at the highest temperature (1000nm thick), which in turn reduces to 1.019 upon annealing for 8 hours at 950ºC. In light of this effect of annealing, we performed a post-growth annealing procedure in practically all films grown on STO substrates. In an effort to further relax the BST films, we employed a novel growth scheme wherein a low temperature "compliant" layer was grown initially on the STO substrate or between two higher temperature BST films. The compliant layer tends to relax quickly, resulting in a more relaxed film overall, particularly after annealing, as evidenced by *c/a* ratios for a 500nm thick film of 1.054 and 1.022 before and after annealing; additionally, the films which

employed compliant layers resulted in a marked improvement in BST tunability, discussed in more detail in 3.3. Interdigitated Capacitors on BST.

Growth of BST by pulsed laser deposition (PLD) is a very high energy technique, and as such, results in films which are not clamped to the underlying substrate (that is, they have lattice parameters very close to those of bulk BST). The films grown by PLD studied in this work were grown at 750 °C in a 100 mTorr oxygen atmosphere. The energy fluence and repetition rate for the 248 nm KrF laser was 1.7 J/cm^2 and 25 Hz, respectively. The deposition was done for about 1 hr and the target-substrate distance was 7.5 cm. These conditions produce a ~3 μm thick BST film (as measured by cross sectional SEM imaging). The films grown by PLD do not exhibit the clamping effect from which the sputtered films suffer, as evidenced by the *c/a* ratios of 1.0 and 0.997 prior to and after annealing, respectively. The film becomes slightly tensile strained after annealing due to the relaxation of the underlying seed layer; in essence the PLD film is “clamped” to the seed layer.

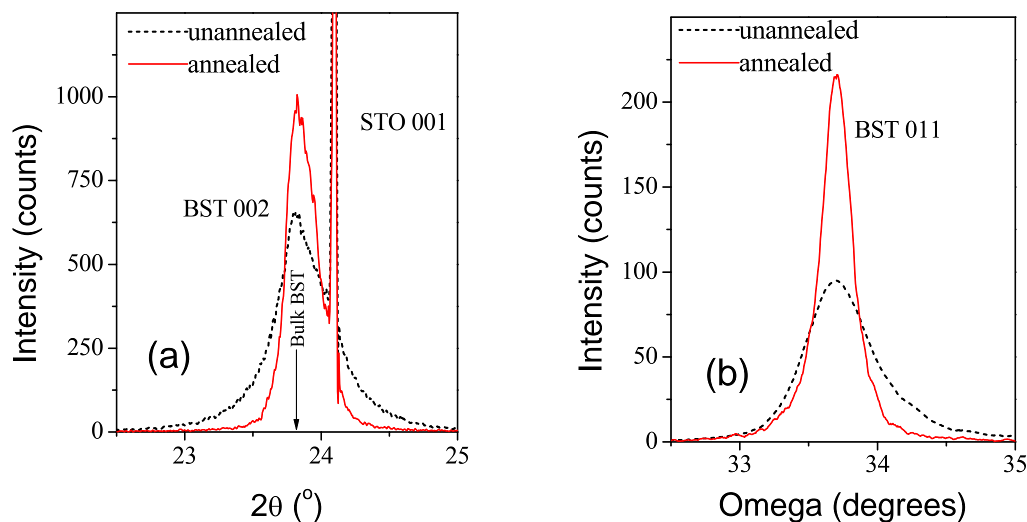


Figure 48. XRD of BST films grown by PLD on a sputtered seed layer. The layer grown by PLD suffers from little to no strain.

3.2. Fabrication of BST Devices

Although thin metal films are sufficient for studying the electrical properties of the BST at low frequencies, in order to produce low loss microwave devices, thick metal films must be employed in order to minimize the ohmic loss associated with high frequencies (See Appendix1: Loss). For this purpose, a trilayer liftoff procedure was employed as opposed to the typical liftoff procedure used in depositing thin metal films (using photoresist). In the trilayer technique, a thick film of poly(methyl methacrylate) (PMMA), is first spun onto the sample surface. The thickness of the PMMA should be larger than the target thickness of the electrodes; we use a PMMA thickness of ~2.5μm as our metal films are ~ 2μm thick. Next a 50nm film of chromium is electron beam evaporated onto the surface of the PMMA. Ordinary photoresist is then spun onto the bilayer and lithography is performed. The photoresist is then used as a mask to wet etch the Cr layer into the pattern of interest. After removing the PR mask, the Cr acts as a mask to expose the PMMA to the 253.7nm line of a mercury bulb. Care must be taken to avoid heating of the sample as the glass transition temperature of PMMA is 97ºC. Of course, a dedicated deep UV source would be optimal for this process but the mercury bulb can also be used as it is available in typical contact aligners, although the additional wavelengths emitted from the Hg bulb can cause excessive sample heating. The exposed PMMA is then developed using an MIBK-IPA developer. The samples can then be loaded into an evaporator for thick metal deposition. We use Cr/Ti/Ag/Au

(50/25/2000/50nm) deposited by electron beam evaporation (thermal evaporation for Au) for all devices. We found that the Ti was necessary in order to promote Ag adhesion. Liftoff consists of placing the samples in acetone for several hours after metal deposition and simply blowing clean with N_2.

3.3. Interdigitated Capacitors on BST

Our initial work focused on studying interdigitated capacitor structures, as was done in earlier reports. These structures are desirable because they are relatively easy to fabricate, are small so many devices can be fabricated on a single sample, and are relatively easy to analyze due to their symmetry.[170] In fact, the IDC structures are small easy-to-fabricate varactors and as such are often used in the first assessment of the quality of BST (electrical quality, in terms of the tunability of BST). In this approach, one can simply measure the capacitance as a function of applied electric field (CV) to estimate the tunability of BST and make comparative analyses among a group of BST films. A typical CV measurement for a film of BST on STO is shown in Figure 49(left), along with the same for the same layer after annealing for 8 hours at 950ºC, Figure 49(right). The tuning curves shown are from the BST films grown at the highest temperature available in our sputtering system (temperature set to maximum ~763ºC and utilizing a metalized backside to increase heat absorption; temperature is likely close to 800ºC), and represent the largest tuning achieved from a "standard" BST on STO growth (up to nearly 4% for the annealed layer). Note the difference between the curves when sweeping from positive to negative bias and vice versa (the shape of the curve is such that the curves are often refered to as "butterfly shaped", we will also use such a term). The difference arises due

to the internal polarization (electric field) in the layers, arising from the ferroelectric nature of BST. While the composition of BST that we employ (50% Ba and 50% Sr) is known to be paraelectric at room temperature, the strain suffered by these layers tends to increase the ferroelectric Curie temperature[171] and therefore causes our layers to be somewhat ferroelectric. Note that annealing tends to reduce the trend (due to the relaxation of the layer), and increases the tunability of the devices. Also worthy of note is the increase in overall capacitance for the annealed layer; since the geometry and film thicknesses are identical in each of these layers, the capacitance increase can be attributed to an increase in the dielectric constant of the film. As such, annealing appears to be beneficial all around, and in general was employed for all the BST films which we grew.

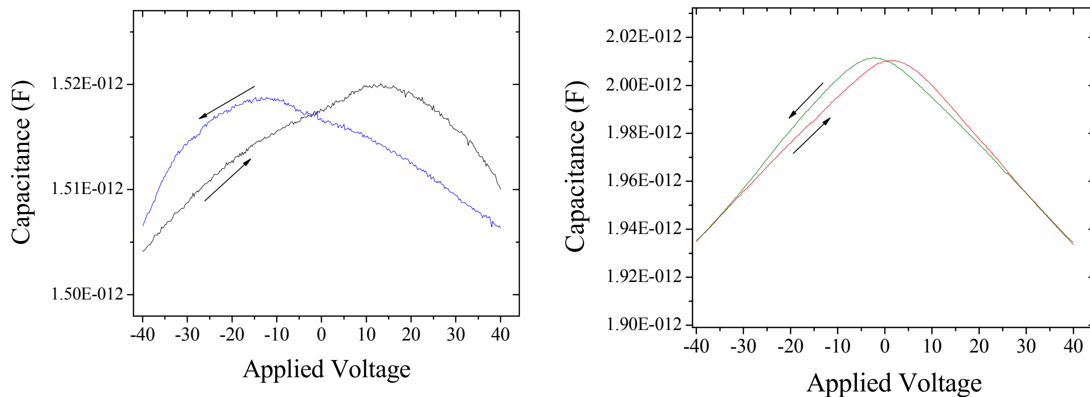


Figure 49. Typical BST tuning curve for a thin film grown by sputtering at highest temperature on an STO substrate: (left) standard growth prior to annealing; the tuning is <1%. (right) the same sample after annealing 8 hours at 950ºC; the tuning is 3.8% and the curves come much closer together, indicating a more relaxed film.

We mentioned above that the clamping constitutes an impediment to optimal device performance and that we attempted to employ "compliant layers" in the structure in order to mitigate the detrimental effects of the compressive strain. The achievement for an initial layer employing a compliant layer (50nm low temperature (400ºC) compliant layer

+ 450nm high temperature (763ºC) film; additionally, the film was annealed for 8 hours at 950ºC) is shown in Figure 50. The first items to note from the figure are the high tunability and high dielectric constant. Considering that the thickness of this film is only 500nm, it is remarkable that the tunability is as high as 9.2%. Recall that the highest tuning observed using standard growth schemes was below 4% and that this was for a 1µm thick layer (Figure 49). Thinner layers should exhibit lower values of tuning as the electric field is shared with the substrate more so in thinner films. Furthermore, the value of the capacitance is of the same order as the results in Figure 49. This means that the dielectric constant must also be larger in the film with the compliant layer since the thickness is reduced. The next observation apparent from the figure is that this layer appears to have a strong ferroelectric component, as evidenced from the butterfly shape of the difference in the tuning curves when sweeping in opposite direction (black and red curves); however, as we mentioned in the previous section, we employed compliant layers in order to *reduce* the strain, not enhance it, as mentioned in 3.1. Growth of BST). The reason for the apparent ferroelectric behavior is due to the slowness of the response of the devices to the applied electric field. The blue curve in Figure 50 illustrates that the film is not actually ferroelectric. First we apply a high voltage (-40V) to pole the BST. Next we allow the BST to relax (at 0V, couple of minutes of time) and then sweep the voltage from 0 to +40 and observe the capacitance versus applied voltage. Repeating this using the opposite polarity completes the blue curves. Apparently, the remnant polarization associated with ferroelectricity is not present when we wait a couple of minutes before sweeping to high field after previously poling with a field of the opposite

polarity. Thus the films are in fact paraelectric, as we expect. All films that we grew on STO substrates exhibit slow responsiveness, to some degree.

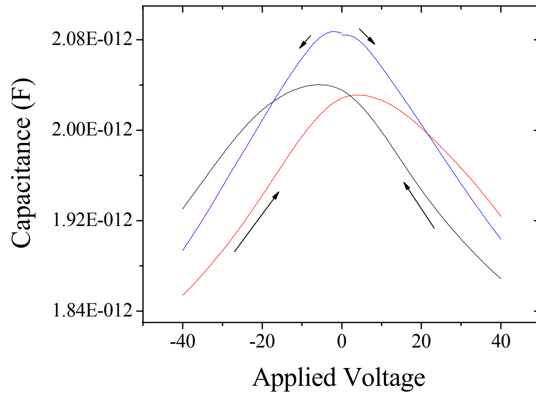


Figure 50. Tuning curves for the BST film atop a low temperature BST film ("compliant layer"). The tuning is 9.2%, while the film is only 500nm thick. The film also boasts a high dielectric constant, as evidenced from the high capacitance.

The fact that the film takes a long time to respond to a changing field is troubling and in fact, moots one of the main points for using a ferroelectric material in developing tunable microwave components; the speed with which one can tune a device is limited to the speed with which the film can respond. Nevertheless, since most of the tuning for a given device occurs very quickly, with a slow response "superimposed" on the primary response, we will proceed with our analysis of BST on STO while in the meantime, we hope to correlate the slow response with some sort of trap or defect in the films.

While IDCs can be useful for a comparative analysis of tuning at low frequencies, one must be very careful. This is because when STO is used as the substrate (with ε=300), a significant portion of the electric field lines may be confined to the STO substrate, which would cause the amount of tuning of the BST itself to be reduced. Further exacerbating this situation is the fact that the amount of confinement depends on the actual value of the

dielectric constant of the BST film as well as the BST film's thickness, particularly when the dielectric constant is near or below 300 or when the film is very thin. In this vein, similar layers may appear to have vastly different tuning performances, but in fact the different only arises from the difference in dielectric constants and thicknesses. The conclusion is that the STO substrates are not the optimal substrates for tunable devices fabricated from BST. As an example, in Figure 51 we have calculated the apparent tuning (the capacitance of a coplanar waveguide structure shown in Figure 46) assuming BST with thicknesses of 500nm and 3000nm, using a starting value of ε of 500 (left) and 1000 (right), and on STO and MgO (with ε=10), substrates as a function of the actual dielectric constant tuning. The solid black curves represent the case when the apparent tuning matches the actual dielectric constant tuning. The figure shows that layers on low dielectric constant substrates tend to show more tuning than those on high dielectric constant substrates. The phenomenon is exacerbated when the value of dielectric constant is lower or when the BST films are thinner. Therefore, devices based on thin films of BST on STO substrates will not exhibit the highest device tunability as compared to the same devices on low dielectric constant substrates (assuming that a similar BST film can be grown on such a substrate), and this effect is worst for low ε BST films and very thin BST films.

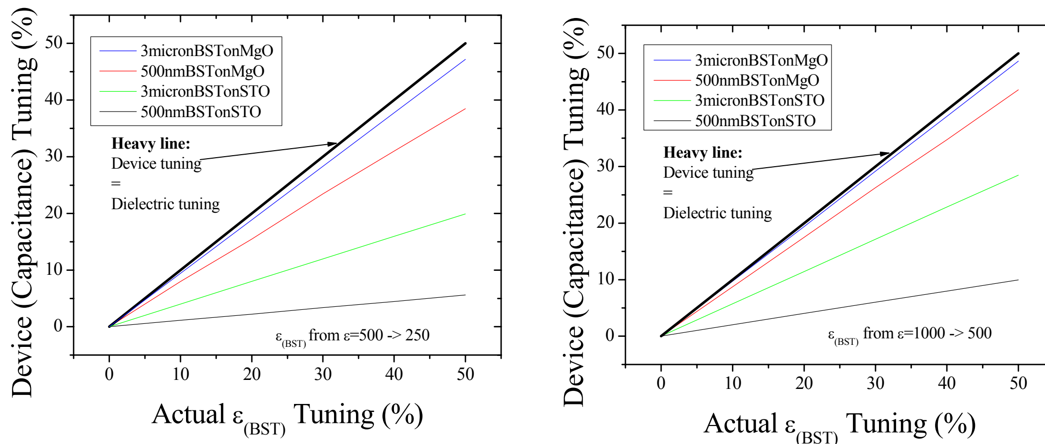


Figure 51. Calculated device tuning as a function of the actual ε tuning for films of BST on STO (ε=300) and MgO (ε=10) substrates. The films grown on STO show much lower device tuning due to the confinement of the applied electric field to the STO substrate, as compared to a lower dielectric constant substrate (MgO). The effect is exacerbated for thinner films (red and green lines) and for BST films of lower dielectric constant (left).

Despite this gloomy outlook, we can still proceed with our analysis of BST films on STO, knowing that in the end, unless the films are relatively thick or can be made to have very high dielectric constant (i.e. >1000), BST on STO *for use in coplanar devices* will not be as effective as an identical BST layer on a low dielectric constant substrate.

3.4. CPWs on BST

The desire to use the BST films at microwave frequencies motivates us to do measurements at microwave frequencies in order to characterize the BST films at conditions under which they would typically be used. In this case, simple CV measurements cannot be employed and we must use network analysis techniques to measure the complex impedance of the IDC varactors. In this case, to asses the actual

dielectric constant of the BST, a relatively complicated conformal mapping technique must be utilized due the relatively complicated geometry of the IDC. However, the mapping requires that the structures be small enough to be considered single, lumped elements if the mapping is to be done for measurements performed at high frequencies. While suitable for low dielectric constant BST films (~<500 for ~500nm films, thinner films would allow for higher values of ε), problems arise when attempting to use the IDCs to extract film parameters for high ε films or using high ε substrates, particularly at higher and higher frequencies. That said, it is generally desirable to achieve very high dielectric constant films of BST in order to shrink device geometries, therefore it is somewhat paradoxical that the technique is best suited to less desirable devices.

This problem is evidenced in Figure 52 for a BST layer grown on MgO with a high dielectric constant (>1000). In order to extract meaningful information at the frequencies which are of interest to us (i.e. X-band 8-12GHz and above), the high dielectric constant of the BST itself causes a "self resonance" phenomenon to occur, at frequencies as low as ~2GHz. As such, the IDC structures are unsuitable for high frequency measurements, especially when we have very high dielectric constant films (which we want). For this reason, we moved to a dielectric parameter extraction routine which exclusively employed CPWs for high frequency electrical characterization.

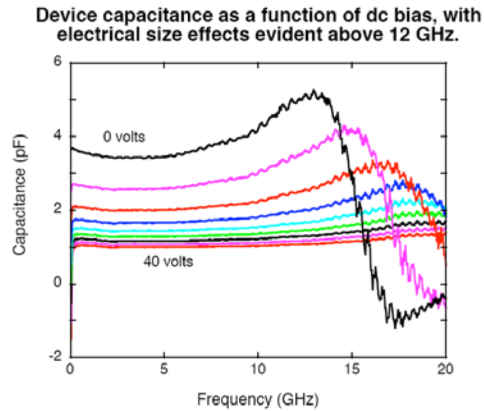


Figure 52. Capacitance of an interdigitated capacitor structure under various biases. When the overall dielectric constant is too high, the wavelength becomes small (on the order of the size of the device) and the capacitor cannot be described as a lumped element. Courtesy of Steve Kirchoefer at NRL.

In order to avoid the use of IDCs, coplanar waveguide structures were fabricated in order to determine dielectric properties of the BST as well as to act as simple phase shifters. In addition to avoiding the issues related to the resonance, as shown in Figure 52, CPWs allow us to determine the actual tunabilty of the BST itself, to avoid the ambiguity associated with the effect of the substrate. While the actual devices fabricated in a CPW geometry are not necessarily immune to the issues giving rise to the phenomonenon present in Figure 51, the ability to analyze the CPW structure without the need to consider it to be a lumped element allows us to determine the actual properties of the BST films.

CPWs serve as calibration standards to perform multiline thru-reflect-line (TRL) calibrations[172] using the MultiCal software developed by National Institute of Standards and Technology (NIST). Although this is technically a calibration technique, it can be used to directly determine the dielectric constant as well as the loss tangent of the BST film. The other benefit of using this technique is that after we have performed the calibration, we can immediately measure devices in the BST (i.e. phase shifters), as the

system is already calibrated. The benefit of using a TRL-based technique is that after calibrating, the reference plane is placed in the center of the thru line (which is very short—this means that any impedance mismatches that occur at the CPW probe/sample interface are effectively calibrated out). This is to be contrasted with a typical SOLT calibration technique where the reference planes are directly at the probe tips—after calibrating, if one were to measure a device embedded in a material with a different dielectric constant than that of the calibration standards (an alumina substrate in the case of the SOLT technique), impedance mismatches at the reference plane would add to the measurement error. TRL-based techniques avoid this typically prevalent problem.

The MultiCal technique determines the complex propagation constant, $\gamma=\alpha+j\beta$, as a function of frequency. From the complex propagation constant, the effective relative permittivity is determined through the following equation:[173]

$$\varepsilon_{r,eff} = -\left(\frac{c\gamma}{\omega}\right)^2$$

Equation 22

Using this effective relative permittivity value, we can determine the dielectric constant of the BST layer itself, ε_{r2}, using the closed form expression found from conformal mapping, discussed in the next section. The value of α which is determined from the MultiCal technique allows us to determine the loss in the BST films.

3.4.a. CPWs for Determination of Material Properties

After obtaining values of effective permittivity as well as the loss coefficient, α, we can determine the actual dielectric constant and loss tangent of the BST films in the following manner:[174]

$$\varepsilon_{r,eff} = 1 + \left(\varepsilon_{r1} - 1\right)\left[\frac{1}{2}\frac{K(k_1)}{K(k_1^{'})}\frac{K(k_0^{'})}{K(k_0)}\right] + \left(\varepsilon_{r2} - \varepsilon_{r1}\right)\left[\frac{1}{2}\frac{K(k_2)}{K(k_2^{'})}\frac{K(k_0^{'})}{K(k_0)}\right]$$

Equation 23

where ε_{r1} and ε_{r2}, are the dielectric constants of the substrate and BST layer, respectively, *K(k)* is the complete elliptic integral of the first kind, $k_0 = k_1 = S/\left(S + 2W\right)$ with *S* being equal to the signal linewidth and *W* to the separation between the edge of the signal line and ground plane, $k_2 = \sinh\left(\pi S/4h_2\right)/\sinh\left[\pi(S + 2W)/4h_1\right]$ with h_1 and h_2 being equal to the thicknesses of the STO substrate and the BST film, respectively, and $k_i^{'} = \sqrt{1 - k_i^2}$.

The terms in square brackets can be referred to as q_1 and q_2, the filling factors of the substrate and BST films, respectively. The CPW line also has a characteristic impedance, Z_0, associated with it, defined as

$$Z_0 = \frac{1}{cC_{air}\sqrt{\varepsilon_{eff}}} = \frac{30\pi}{\sqrt{\varepsilon_{eff}}}\frac{K\left(k^{'}_0\right)}{K\left(k_0\right)}$$

Equation 24

The characteristic impedance will play a major role in the ohmic loss that a CPW line suffers, and interestingly the optimal characteristic impedance (in terms of minimal ohmic loss) is around 50Ω.

As an example of the results obtained from such a technique, let us consider devices fabricated on the films which employed the PLD-grown films, which we know to be the most relaxed films and promising for real phase shifter applications.

Figure 53 shows the effective dielectric constant, calculated using Equation 23, for both the as-grown (open symbols) and the annealed (closed symbols) BST films versus applied electric field. Note that we use a simple estimation of the electric field by dividing the bias voltage by *W*. Of course, this is an overestimation of the actual field within the BST layer since the field decreases with depth within the film. Dispersion in the dielectric constant versus frequency is relatively small for the as-grown layer and increases markedly for the annealed one. The tuning at 60kV/cm (applied bias of 30V) for the as-grown sample is 41.8% and 40.5% at 10 and 20 GHz, respectively, while the tuning for the annealed film improved to 58.6% and 51.3% at 10 and 20 GHz, respectively. This improvement in the value of dielectric constant and its tuning is expected considering the improvement in crystal quality as well as the slight strain that is induced after annealing, as evidenced by the HRXRD measurements.[175]

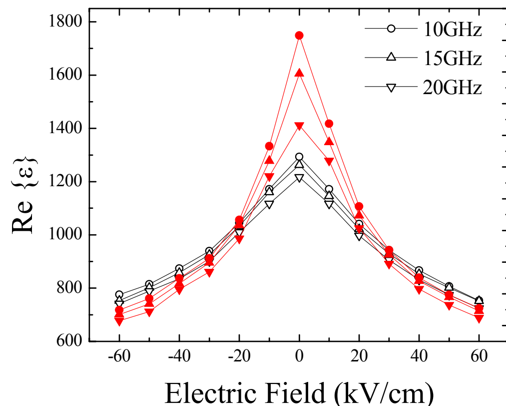


Figure 53. Measured relative dielectric constant of the BST layers grown by PLD on sputtered seed layers before (open symbols) and after (closed symbols) annealing at 950 ºC for 8 hours.

In order to estimate the loss tangent for the BST, we again use expressions derived from the conformal mapping analysis. We will assume that all of the loss in the system is due to either the conductor loss, α_c, or dielectric loss, α_d (i.e. no radiation or surface wave losses). Under the aforementioned assumption, the total loss is simply the sum of the conductor and dielectric losses:

$$\alpha = \alpha_c + \alpha_d$$

Equation 25

We first estimate the conductor loss as

$$\alpha_c = \frac{R_{center} + R_{ground}}{2Z_0}$$

Equation 26

where R_{center} and R_{ground} represent the series resistances per unit length of the center and ground conductor planes, respectively:

$$R_{center} = \frac{R_{skin}}{4S(1-k_0{}^2)K^2(k_0)}\left\{\pi + \ln\left(\frac{4\pi S}{t}\right) - k_0\left(\frac{1+k_0}{1-k_0}\right)\right\}$$

Equation 27

$$R_{ground} = \frac{k_0 R_{skin}}{4S(1-k_0{}^2)K^2(k_0)}\left\{\pi + \ln\left(\frac{4\pi\left(S+2W\right)}{t}\right) - \frac{1}{k_0}\left(\frac{1+k_0}{1-k_0}\right)\right\}$$

Equation 28

where t is the metal thickness, assumed to be much thicker than the skin depth, and

$$R_{skin} = \frac{1}{\delta\sigma}$$

Equation 29

is the surface resistance due to the skin effect. Here δ is the skin depth and σ is the conductivity of the metal.

With this, and under the assumption that the only losses are attributable to ohmic and dielectric loss, we can take the difference between the measured loss and the calculated ohmic loss to be the dielectric loss:

$$\alpha_d = \frac{\pi}{\lambda_0} \frac{\varepsilon_r}{\sqrt{\varepsilon_{eff}}} q \tan \delta_e$$

Equation 30

From which we can obtain the loss tangent, tan δ_e.

The total measured loss from the MultiCal calibration is displayed in Figure 54. As expected, the loss decreases with increasing bias electric field. Part of the reason for the large loss of the lines is the inherent loss associated with the geometry of CPW structures. As discussed in reference 176, the optimal characteristic impedance, Z_0, of a CPW line is around 50 Ω. In order to achieve such a Z_0 value on a substrate with a large dielectric constant (i.e. the BST, with a dielectric constant over 1000), an unreasonably thin center line (which would increase the ohmic loss), or a ground plane separation which is larger than that which could be supported by the pitch of the probes (150μ) would be necessary. Additionally, increasing the ground plane separation would reduce the loss of the CPW lines as described in Ref. 176 (it would also increase the bias voltage required to reach the same electric field). In fact, an identical calibration using the same CPW geometries on a bare STO substrate (with measured relative dielectric constant of ~300) results in loss of 12 ± 0.2 dB/cm at frequencies between 10 GHz and 20 GHz.

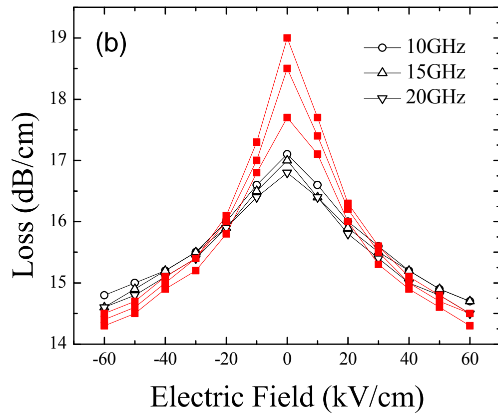


Figure 54. Measured loss (in dB/cm) of the BST layers grown by PLD on sputtered seed layers before (open symbols) and after (closed symbols) annealing at 950 ºC for 8 hours.

In our endeavors we use a 2 micron thick metal and assume a conductivity of 6.173 x 10^7 S/meter for the calculations (representing the thickness and conductivity of the silver in the metal stack). Utilizing these numbers we can obtain the metal contribution to the loss at high frequencies, i.e. where the metal thickness is > 4δ; under this constraint we assess values of loss tangent at frequencies of 18GHz. At 18GHz, we obtain a metal-related loss of 8.0dB/cm, 11.2dB/cm, and 12.1dB/cm for metal films on a bare STO wafer, and on the unannealed and annealed PLD layers of BST on STO, respectively. Clearly, the metal contribution to the loss is dominant due to the nonoptimal geometry of the device and subsequent low characteristic impedances.

For the bare STO substrate, we deduce $\tan\delta$ to be 0.0098 at 18GHz. For the BST on STO layers, we can write the following expression to deduce the effective $\tan\delta$ of the BST/STO system after Equation 30:

$$\alpha_d = \frac{\pi}{\lambda_0}\frac{1}{\sqrt{\varepsilon_{eff}}}\left\{\varepsilon_{r1}q_1 + \varepsilon_{r2}q_2\right\}\tan\delta_{eff}$$

Equation 31

From this, we obtain the effective tanδ, tanδ_{eff}, of the unannealed and annealed films to be 0.018 at 18GHz. Finally, in order to obtain the loss tangent of the BST film alone, we write

$$\varepsilon_{eff} \tan\delta_{eff} = q_1\varepsilon_{r1} \tan\delta_1 + q_2\varepsilon_{r2} \tan\delta_2$$

Equation 32

and obtain the loss tangents of the BST films to be 0.02 at 18GHz, for both the unannealed and annealed films. It is interesting to note that despite the improvement in crystal quality, the dielectric loss is unchanged after annealing. With these results, an intrinsic figure of merit which is defined as the tunability (in percent) divided by tanδ would be ~2000 and ~2500 for the unannealed and annealed layers, respectively, near 20GHz at a applied voltage of 30V.

3.4.b. CPWs as phase shifters using BST

In addition to using the CPW lines as a means to determine the dielectric constant and the loss in the BST, after calibrating the network analyzer we can simply measure long CPW lines, as they constitute the most simple type of phase shifter. Such a device is simple in the sense that a DC electric field present between the signal and ground lines of a coplanar waveguide (CPW) transmission line is used to polarize the BST, subsequently changing the dielectric constant of the BST and causing the phase velocity of the propogating microwave radiation, $\frac{1}{\sqrt{\mu_{eff}\varepsilon_{eff}}}$, to change. This in turn causes a change in the phase between input and output ports as a function of the applied field. Though such

devices can exhibit respectable performance, the problems with such a design are twofold. First, the design is constrained in the sense that the field that can be applied is now coupled to the impedance of the structure (since the characteristic impedance of a CPW waveguide is related to its geometry, Equation 24). The second problem which was evidenced by the high apparent loss in the devices mentioned in the previous section is that for high dielectric constant materials, such as BST, the geometry that must be used in order to be able to apply a reasonable voltage and subsequently achieve a modest field to induce a phase shift is such that the signal and ground lines are close together, which is inherently lossy for a CPW line. This arises from the point that the geometry will result in an impedance that is very low (~several Ohms) and that ohmic losses will dominate at high frequencies for low impedance CPW lines. In addition to this, most devices operate in a 50Ω environment, which would require impedance matching to be employed prior to adopting such a device into any real system. Attempting to design a 50Ω device of this type on a substrate with a very high dielectric constant (>1000) in CPW generally will require a center signal line exceedingly thin (<100nm), which would also be very lossy. As such, the simple types of these phase shifters are generally lossy and additionally not 50Ω.

Despite these setbacks, we can proceed to characterize the simple types of phase shifters; we choose to continue with the characterization of the same PLD layers measured in the previous section. After calibrating, which allows us to determine the dielectric constant as well as the loss of the BST as done above, the phase shift along the coplanar waveguide lines was measured as a function of applied field. These results are displayed in Figure 55 for CPW lines with a length of 1.5mm fabricated on both as-grown and annealed

samples. At a bias voltage of 30V, we observed a differential phase shift of 45° and 87° at 10 and 19GHz, respectively, for the as-grown layer and a differential phase shift of 90° and 140° at 10 and 19GHz, respectively, for the annealed sample.

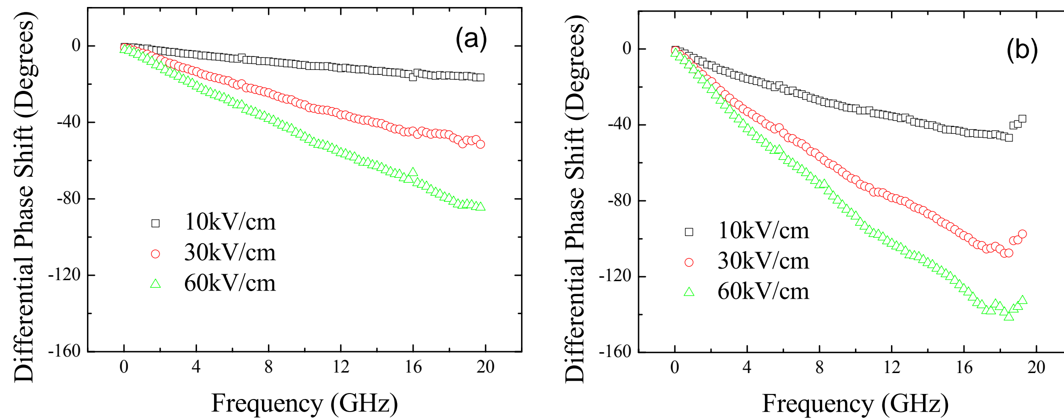


Figure 55. (a) Measured differential phase shift for various applied fields for as-grown (b) as well as annealed layers.

Using the measured loss (Figure 54) at zero field, where loss is at its maximum, as a function of frequency and normalizing the differential phase shift to unit length, we can determine the typically reported figure of merit for these devices in terms of degrees of phase shift per dB of loss, as displayed in Figure 56. We obtain a figure of merit of 19°/dB and 34°/dB at 10 and 19 GHz, respectively for the as-grown layer and a figure of merit of 35°/dB and 55°/dB at 10 and 19GHz, respectively, for the annealed sample. It is remarkable that these figures of merit, particularly the ones for the device fabricated on the annealed layer, compare well with some of the best ones reported in the literature considering the relatively large amount of loss present in the system.[5,6,177,179] Further work involving more complicated phase shifter designs, such as those presented in [5, 177], can improve the performance in terms of loss, and are the subject of the section, 3.6. Future Work .

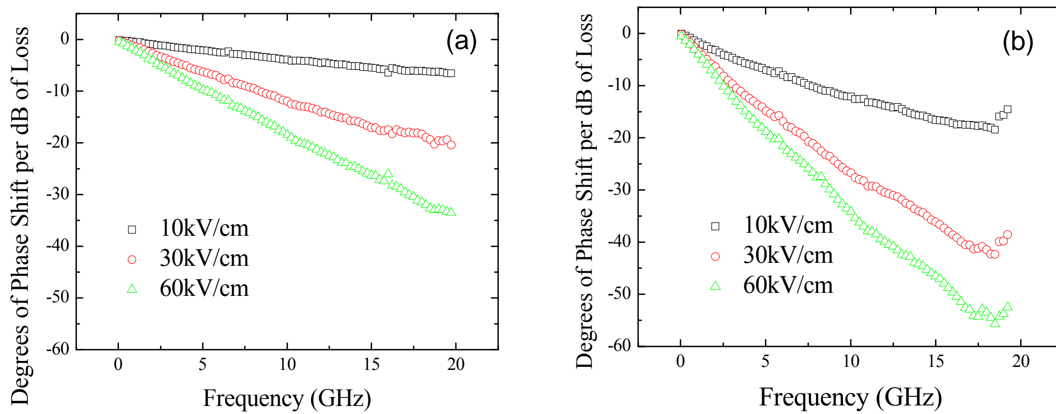


Figure 56. Measured figure of merit (differential phase shift in degrees per loss in dB) for various applied fields for (a) as-grown and (b) annealed BST layers.

After a survey of the existing literature on tunable phase shifters based on BST, we wish to comment on the use of an alternative figure of merit, taking into account the strength of electric field required to achieve a given phase shift. As the voltage required to realize a given phase shift is important in actual devices in real systems, we propose to simply divide the traditional figure of merit by the applied field, which yields a figure in units of °-cm/dB-kV, and allows one to more effectively compare devices produced in different laboratories. Table 2 displays this new figure of merit for our devices as well as for devices from other laboratories for comparison. For all the devices, we define the field to be simply the voltage divided by the separation between the electrodes that generate the tuning (in our case, between the signal and ground planes which is 5μ). As mentioned above, this overestimates the actual field in the BST layer for coplanar structures. Therefore, our estimation of the improved figure of merit is a conservative one. For our CPW structures, we achieve 1.2°-cm/dB-kV and 1.8°-cm/dB-kV at 10GHz and 19GHz, respectively, for the annealed sample. Note that this value does not correspond to the maximum applied field for our layers. It is interesting that the highest values for this

alternative figure of merit are achieved using simple CPW designs (this work and reference 178), which do not involve any periodic loading of a synthetic transmission line.

Figure of Merit (deg-cm/dB-kV)	Bias Voltage	Frequency	Type of Phase Shifter	Reference
0.40	**20V**	**23.7GHz**	**Coupled Microstrip**	**[6]**
0.22	**5V**	**10GHz**	**Parallel Plate Loaded CPW**	**[5]**
0.18	**10V**	**20GHz**	**IDC Loaded CPW**	**[177]**
1.14	**20V**	**20GHz**	**CPW**	**[179]**
1.8	**5V**	**19GHz**	**CPW**	**This Work**

Table 2. Comparison of experimentally achieved figure of merit for various types of phase shifters for various laboratories.

3.5. Hybrid BST/Ferrite Devices

The ability to design the device to any impedance is of course desirable, but we must consider that as the device tunes, the impedance will change. This brings us to the second device in this section of the dissertation, that which employs the integration of a ferrite material with the ferroelectric BST. Since, in general, the impedance of a medium can be described as $\eta_0 = \sqrt{\frac{\mu_{eff}}{\varepsilon_{eff}}}$, we see that if the tuning of the permittivity were coupled with the tuning of the permeability, one could obtain simultaneous phase shift as well as maintaining impedance matching.

We can tune the permeability of a ferrite material through the application various external magnetic fields. In this way, phase shifters on bilayers of BST and a ferrite would allow for tuning of both the permeability as well as the permittivity of the overall device—this

way we can have a phase shifter that maintains its impedance while changing its phase shift.

In order to analyze such a device, we generalize the typical expressions used in the analysis of a CPW line (in which only the permittivity affects the phase velocity of the traveling wave) to include the effect of the permeability:

$$\beta^2{}_{eff} = \frac{L_{tot}C_{tot}}{L_0 C_0} = \frac{\beta'^2{}_{tot}}{\beta'^2{}_0}$$

Equation 33

where $\beta'^2{}_0$ represents the reactance of the CPW line in air:

$$\beta'^2{}_0 = 4\mu_0\varepsilon_0 \frac{K(k')}{K(k)}$$

Equation 34

and $\beta'^2{}_{tot}$ represents the sum of all of the reactances of the each of the layers:

$$\beta'^2{}_{tot} = \sum \beta'^2{}_i = \sum 2\mu_0\varepsilon_0 \left(\mu_{ri}\varepsilon_{ri} - \mu_{r(i-1)}\varepsilon_{r(i-1)}\right) \frac{K(k)}{K(k')} \frac{K(k_i')}{K(k_i)}$$

Equation 35

In these expressions, *K(x)* is the complete elliptic integral of the first kind with arguments:

$$k = \frac{c}{b}\sqrt{\frac{b^2 - a^2}{c^2 - a^2}}$$

Equation 36

and

$$k_i = \frac{\sinh\left(\pi c / 2h_i\right)}{\sinh\left(\pi b / 2h_i\right)} \sqrt{\frac{\sinh^2\left(\pi b / 2h_i\right) - \sinh^2\left(\pi a / 2h_i\right)}{\sinh^2\left(\pi c / 2h_i\right) - \sinh^2\left(\pi a / 2h_i\right)}}$$

Equation 37

In these expressions h_i is the thickness of the ith layer, c is half the width of the entire CPW line, including the ground planes, b is half the width of the CPW line excluding the ground planes, and a is half the width of the center signal line alone.

Figure 57 shows the result from the TRL calibration, the square of the normalized effective phase constant (which is the imaginary part of the propagation constant, γ, normalized by c/ω), as well as the loss (in dB/cm) for the bilayer structure under zero applied DC electric field using no magnetic field (thin lines) and under an applied magnetic field of ~1700 Oe (thick lines). When the magnetic field is applied, the effective phase constant of the system changes from being essentially constant (with a value of ~32) to having features associated with the nonconstant permeability of the YIG, which changes as a function of frequency. We expect the permeability of the YIG to be ~1 at frequencies much greater than the ferromagnetic resonance (FMR) frequency and to be some value >1 for frequencies much less than the FMR, as evidenced in Figure 57. The frequency at which FMR occurs is apparent from the figure (~6.75GHz) as the effective phase constant shows asymptotic behavior (due to the asymptotic behavior of μ); additionally the loss is very large near the FMR frequency.

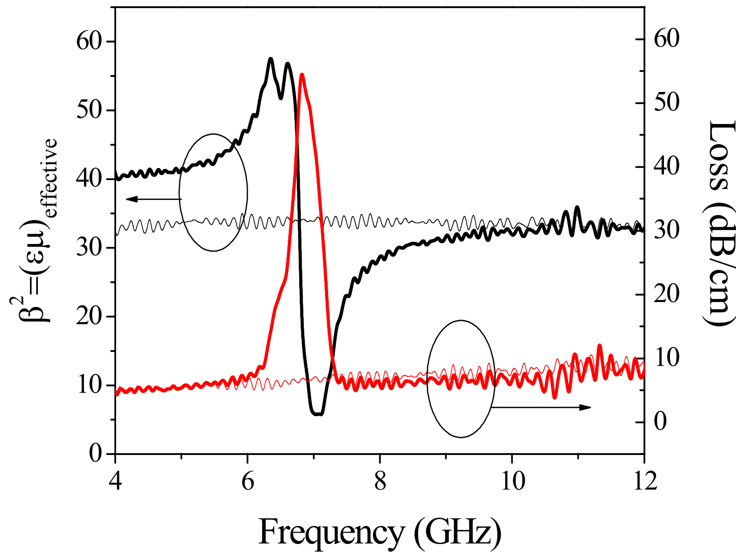


Figure 57. Square of the phase constant, *β*, and loss (in dB/cm) for the BST/YIG bilayer under zero applied magnetic field (thin lines) and under a DC magnetic field of 1700Oe (heavy lines).

By using a relative permittivity of 15 and 12 for the YIG and GGG substrate, respectively, we can determine the BST relative permittivity to be 185 ± 5 (determined under zero applied magnetic field or, equivalently, at frequencies above the FMR frequency in the case when the magnetic field is applied). In order to determine the permeability of the YIG, we assume that all layers, GGG, BST, and YIG have relative permeabilities equal to one under conditions of zero magnetic field. Next, under the application of a magnetic field, we see that the effective phase constant changes for frequencies near and below the FMR frequency. Assuming that the permittivity of each of the layers is unchanged under application of the magnetic field, we can determine the effective phase constant of the YIG using the above equations. At the low frequency side of FMR, this value for YIG is determined to be ~105. Since the square of the phase constant represents the product of permittivity and permeability, we can conclude that the relative permeability of the YIG at frequencies below FMR to be 7 ± 1, assuming that the

actual relative permittivity of the YIG is 15. Of course, the permeability increases as the FMR frequency is approached and approaches a value of 1 at frequencies >>FMR.

Next, the effective phase constant of the bilayer is tuned under the application of both electric as well as magnetic fields. Figure 58 shows the effect of applying a DC electric field (a) as well as increasing and decreasing the DC magnetic fields (b). By holding the magnetic field constant and changing the applied electric field Figure 58(a), the effective phase constant shifts toward lower values throughout the frequency band due to the reduction in the permittivity of the BST under applied electric field. The value of permittivity of the BST changes from ~185 to ~154 as the voltage applied to the lines is increased from 0 to 30V, representing a tunabilty of the BST of ~16.8%. By holding the electric field constant at 0V and changing the magnetic field Figure 58(b), the value of the ferromagnetic resonance frequency changes, which in turn causes an apparent shift in the effective phase constant in frequency. At a frequency of 6GHz, the relative permeability of the YIG layer changes from ~18 to ~12 for magnetic fields of 1600 and 1800Oe, respectively. Note that we do not observe any evidence of coupled spin waves[180], as there is not an apparent change in the value of the FMR frequency under application of an electric field, see inset to Figure 58(a). This is likely due to the fact that the electric field is applied only between the signal and ground planes in the CPW structure, so that the only tuning of permittivity that occurs is local tuning of the BST between these electrodes. Most of the BST (by volume) continues to have a permittivity equal to the value observed when no voltage is applied.

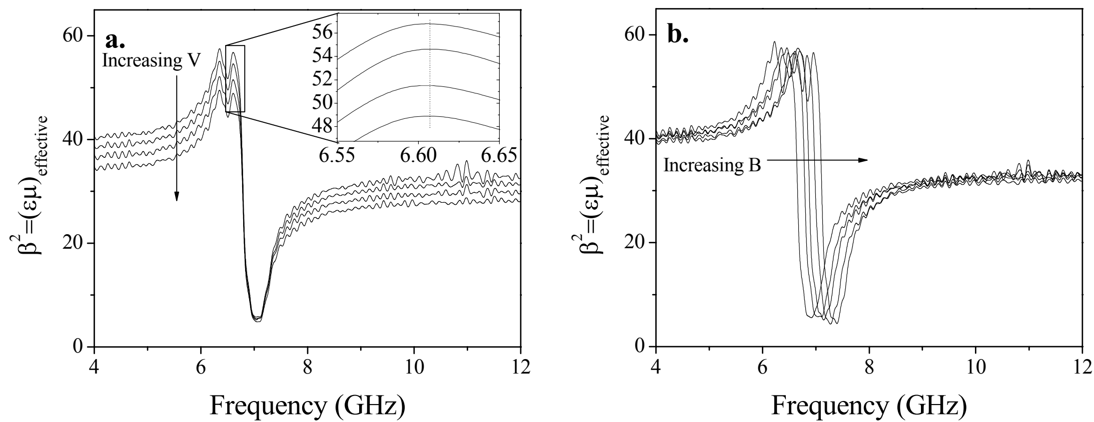


Figure 58. Tuning of the effective phase constant of the bilayer (a) by changing the applied electric field (applied voltage ranges from 0 to 30V) under static magnetic field and (b) by changing the applied magnetic field (applied field ranges from 1600 to 1800Oe) under zero electric field.

The differential phase shift achieved by applying 30V to a 1.1-mm-long CPW line is shown in Figure 59 for the nominal magnetic field of ~1700 Oe as well as at increased and decreased magnetic fields from this value. The differential phase shift is linear in frequency below and above the FMR frequency, as expected for a device with static (in frequency) values of μ and ε. However, near the FMR frequency, the permeability of the YIG layer is not constant, which results in a deviation from linearity of the differential phase shift curves. Let us consider a narrow band of frequencies just below the FMR frequency around 6GHz. This is the range where the device will be most useful as a phase shifter. As the magnetic field is increased (decreased), the permeability of the YIG at 6 GHz decreases (increases), Figure 58. Since the tuning of the phase shifter under an applied electric field alone is through a reduction in the permittivity, a reduction (increase) in the permeability would tend to increase (decrease) the overall tuning of the phase constant of the device, as evidenced in Figure 59. The magnitude of the differential phase shift increases from ~38º/cm to ~52º/cm by increasing the magnetic field and

decreases to ~8º/cm by decreasing the magnetic field. At frequencies very close to FMR (~6.5-7.5GHz), the loss is exceedingly high and the phase shifter is not useful.

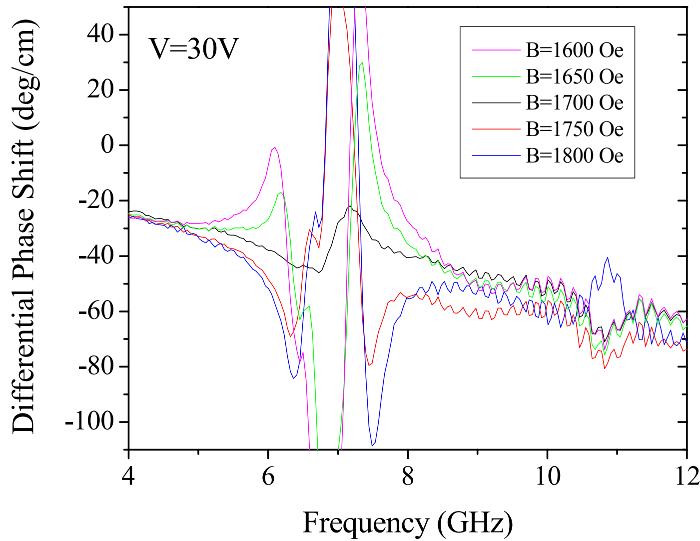


Figure 59. Differential phase shift (degrees/cm) of a 1.1mm CPW line after applying 30V to the center line, under various magnetic fields ranging from 1600 to 1800 Oe.

In addition to increasing the differential phase shift at frequencies near FMR, the increase of the magnetic field should allow the device to recover the impedance it had before the electric field was applied. Recall that the permittivity decreased after applying an electric field, so if one also decreases the permeability (which is possible at some frequencies by increasing the magnetic field), the loss of the device associated with the mismatch that occurs due to the change in impedance can be eliminated. Such an effect is illustrated in Figure 60. The heavy line in Figure 60 shows the return loss of the 1.1-mm CPW line at zero DC electric field and at a magnetic field of ~1700 Oe. Mismatch occurs throughout the band when the electric field is applied in order to cause a phase shift; this is evidenced by a decrease in the return loss from the value at 0 V. By changing the magnetic field the return loss changes since the permeability of the YIG changes for

frequencies near FMR. At 6 GHz, the return loss changes from 27 dB to 22.4 dB after application of the electric field. Then, by changing the magnetic field, the return loss can be improved to 24.9 dB by increasing the magnetic field (inset to Figure 60). Correspondingly, by decreasing the magnetic field the return loss decreases to 18.4 dB at 6 GHz. Thus, the increase of the applied magnetic field is beneficial in terms of increasing the overall device tuning (phase shift) as well as decreasing the loss that can be achieved.

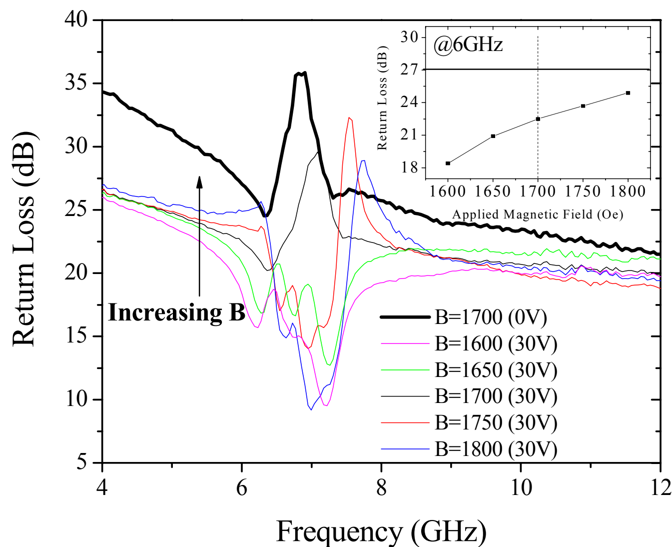


Figure 60. Return loss for the 1.1mm CPW phase shifter under zero applied electric field (heavy line) and at 30V applied electric field under magnetic fields from 1600-1800Oe. Inset shows the return loss at 6GHz at 30V applied electric field under magnetic fields from 1600-1800Oe. Horizontal line in inset is the return loss at 0V applied field under 1700Oe (the calibrated condition).

Although the permeability can be tuned via the tuning of the applied magnetic field, the power consumed in order to bias the devices is quite high. The ability to tune such devices using electric fields instead opens up the opportunity to reduce the power consumption and the overall device size as well as increase the speed with which one can change the frequency of operation. Thusly, in our alternative approach to achieve devices

with dual degrees of freedom for tuning of both permittivity and permeability, we make use of magnetoelectric effects of YIG mechanically bonded a slab of <001> PMNPT using a cynoacrylate-based epoxy. Magnetoelectric effects manifest themselves as an electric polarization induced by a magnetic field or a magnetization induced by electric field through magnetostriction and piezoelectricity[181]. In both cases, it is the mechanical aspect of piezoelectricity or magnetostriction that mediates the transfer of energy from magnetic fields into electric and vice versa. The magnetoelectric susceptibility, α, can be considered a second rank tensor that relates the polarization, P, induced by a magnetic field, H:[182]

$$P = \alpha H$$

Equation 38

As a first demonstration of this magnetoelectric effect, we bonded bulk layers of single-crystal (111) yttrium iron garnet YIG (400 μm-thick) to single-crystal (001) lead magnesium niobate-lead titanate (PMNPT) slabs with Cr/Au electrodes already deposited on either side. Then we directly measured the ferromagnetic resonance frequency of the YIG layer by placing the bilayer on top of an alumina microstrip line and measuring the reflection after performing a simple response cal (which is suitable since only the magnitude of the reflection is important), the setup is shown in Figure 61. Due to the magnetoelectric coupling between the two layers, the FMR frequency of the YIG can be shifted through the application of a DC electric field to the PMNPT, as shown in Figure 62. We achieve a tuning of FMR frequency of over 14MHz under an applied electric field of 20kV/cm for an ME coefficient of 0.7MHz-cm/kV. This result compares reasonably well with the best coefficients available in the literature, around 2.5MHz-cm/kV[183]; our results might be improved by using different bonding agents.

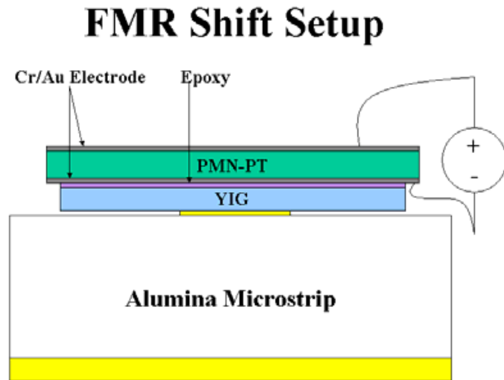


Figure 61. Schematic of FMR measurement setup. DC voltage is applied to the PMN-PT, and the piezoelectric strain that is induced is transferred to the YIG resulting in a shift in the FMR frequency through magnetostriction.

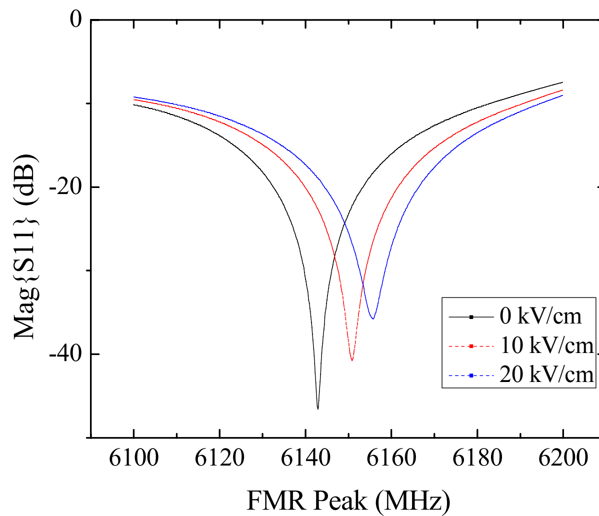


Figure 62. Shift of the ferromagnetic resonance of a layer of YIG via DC applied bias to a layer of PMN-PT, which was bonded to the YIG.

In order to build on this result, we bonded PMNPT to the backside of the sample to which was already characterized above, shown in Figure 58, Figure 59, and Figure 60. We mechanically polished off the GGG substrate from the measured device. Next, we bonded a slab of PMNPT to the underside of the YIG-BST bilayer using Krazy Glue and remeasured the effective phase constant as done above. The result is shown in Figure 63.

The area shown in the figure is near the peak in phase constant, very close to the FMR frequency. By applying a field of only 10kV/cm, the FMR frequency shifts by ~5MHz. Larger fields could be applied if higher voltages were available or thinner PMNPT were employed, which would result in a larger shift in the FMR frequency. Since the absolute value of the phase constant is not reliable due to uncertainty into the TRL calibration stemming from the fact that the bilayer structure cracked during the PMNPT bonding procedure (none of the longest CPWs survived the procedure), we have elected to show only the region of interest near FMR in Figure 63 merely to demonstrate the feasibility of using magnetostriction to tune the permeability of YIG. Further work must be done to optimize this procedure for use in actual phase shifter devices, but in any case, we have demonstrated two methods to dually tune BST/YIG hybrid phase shifters for use in high performance microwave applications.

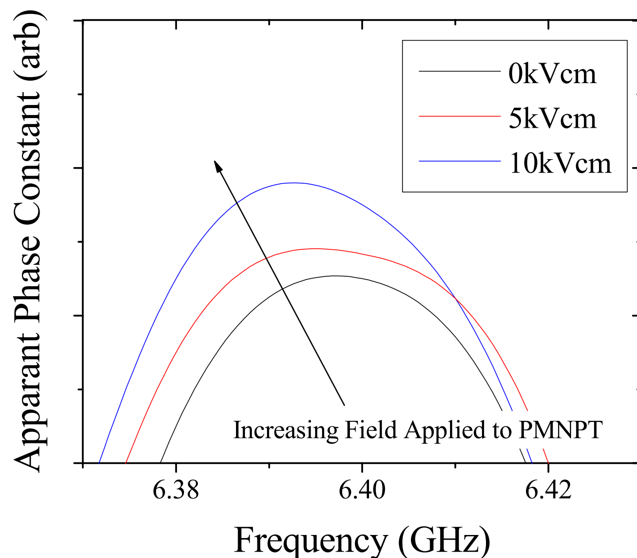


Figure 63. Change in the apparent phase constant as a function of applied field to the PMNPT layer.

3.6. Future Work for Tunable Phase Shifters

First and foremost, any work to be done in the realm of tunable phase shifters should attempt to move away from the use of STO substrates to avoid the effect of the high dielectric constant material below the film of interest. One substrate that would satisfy both needs for low dielectric constant and low loss would be the commercially available and relatively inexpensive sapphire substrate. In this regard, a preliminary growth on sapphire is very promising, as shown in Figure 64. A thin film of BST was sputtered on an MBE grown MgO layer on MBE grown ZnO on a c-sapphire substrate. Tuning for this layer is about a factor of 10, which is extremely high. At present, these layers suffer from very high leakage current, likely due to conduction through the ZnO layer. It appears that studies of BST films on sapphire substrates would be promising and fruitful future work.

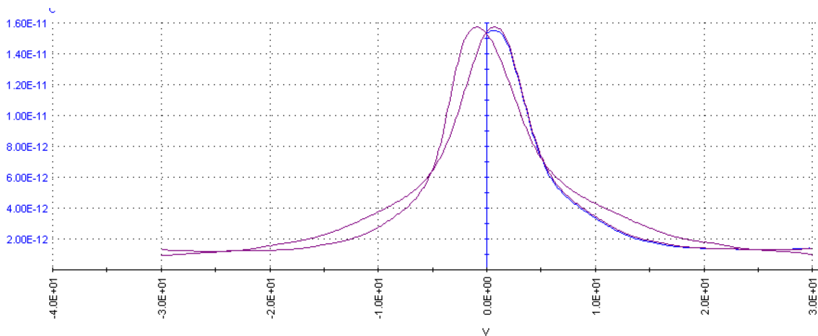


Figure 64. Measurement of capacitance versus applied voltage for a preliminary layer of BST on c-sapphire on a ZnO/MgO MBE film. The tuning is unbelievably high (factor of 10). Most devices suffer from high leakage current, likely due to conduction through the ZnO layer.

Although we achieved respectable performance from the “simple” phase shifters presented above (despite the high losses associated with the inherent metal losses expected for devices with very low characteristic impedance), a more carefully designed phase shifter could yield both large phase shift while at the same time have an impedance which is more amenable for achieving low ohmic loss. Specifically, the design should

employ transmission lines which are periodically loaded with tunable components, so that the impedance of the overall structure can be controlled in the design, and the tunability and losses associated with the device are not limited by the impedance of the line. A schematic of such a "synthetic transmission line" phase shifter[184] is shown in Figure 65. In this configuration, a CPW line with large signal-ground separation, which will result in higher impedance (and therefore lower ohmic loss), is periodically loaded with tunable components which can be either parallel plate capacitors or interdigitated capacitors (shown in the figure). In addition to low loss, this device has the benefit of being able to be designed to be any impedance, for example, 50Ω.

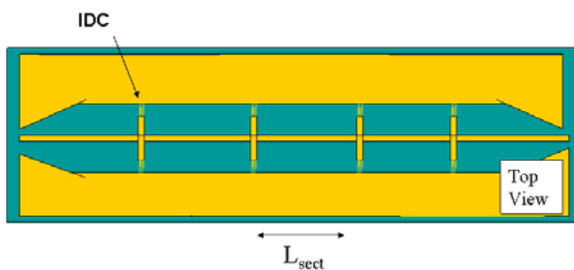


Figure 65. Schematic of the "synthetic transmission line" phase shifter. The overall impedance of the line can be designed to be 50Ω, and the large distance between signal and ground lines of the CPW on which this is built is large, resulting in low loss.

In this realm we now present a design for such a synthetic transmission line phase shifter which would hypothetically be produced on a sapphire substrate, although the design could of course be modified for BST on some other low dielectric constant substrate. We know that the equivalent circuit of a transmission line can be thought of as incremental elements of serial inductors and parallel capacitors, see **APPENDIX1:** Basic Transmission Line Theory. Along these lines, we present in Figure 66 the schematic and equivalent circuit of the synthetic transmission line.

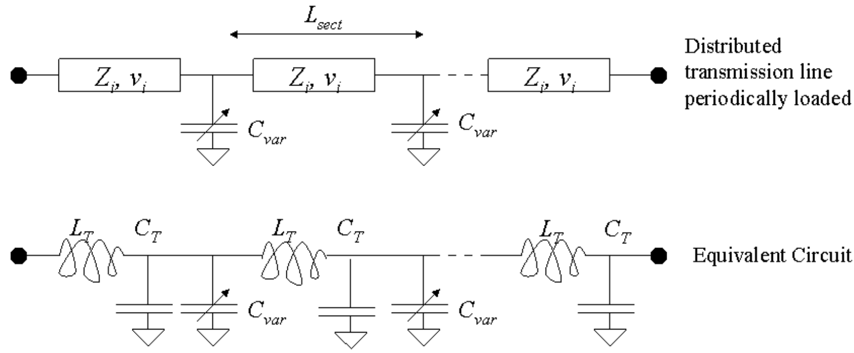


Figure 66. Schematic of the synthetic transmission line. (Top) a transmission line which is periodically loaded with variable capacitors. (Bottom) the equivalent circuit of the synthetic transmission line.

The transmission line is described in terms of its impedance and phase velocity:

$$Z_{tot} = \sqrt{\frac{L_l}{\left(C_l + C_{\text{var}}(V) / L_{\text{sect}}\right)}}$$

Equation 39

$$v_{phase} = \sqrt{\frac{1}{L_l\left(C_l + C_{\text{var}}(V) / L_{\text{sect}}\right)}}$$

Equation 40

Where C_l and L_l are the primary line capacitance and inductance (i.e. without the variable capacitances), normalized to unit length:

$$C_l = \frac{1}{Z_i v_i}$$

Equation 41

$$L_l = \frac{Z_i}{v_i}$$

Equation 42

Where Z_i and v_i are the impedance and phase velocity of the primary CPW line (again, without the variable capacitances).

The impedance of a CPW line is given in Equation 24 and the phase velocity is simply:

$$v_{phase} = \frac{c}{\sqrt{\varepsilon_{eff}}}$$

Equation 43

The synthetic transmission line appears to be like a typical transmission line with its variable capacitors spread out over a "unit cell" of the transmission line, L_{sect}. However, the periodicity of the structure means that this analysis is only valid below the so-called Bragg frequency:

$$f_{Bragg} = \frac{1}{\pi\sqrt{L_T\left(C_T + C_{\mathrm{var}}\right)}}$$

Equation 44

Where C_T and L_T are simply the capacitance and inductance per unit cell, given by the product of L_{sect} with Equation 41 and Equation 42, respectively.

If we define a "loading factor",

$$x = \frac{C_{\mathrm{var}}^{\max} / L_{\mathrm{sect}}}{C_l}$$

Equation 45

we can write an expression combining Equation 41, Equation 42, and Equation 44 to link the Bragg frequency to the spacing between the variable capacitors:

$$L_{\mathrm{sect}} = \frac{v_i}{\pi f_{Bragg}\sqrt{1-x}}$$

Equation 46

By taking care to ensure that the Bragg frequency is larger than the highest frequency of interest, we can relatively easily design the synthetic transmission line phase shifter, assuming of course that we know a priori the BST film's properties so that we can determine the impedance and phase velocity of the primary transmission line. Utilizing such an approach allows for a sophisticated transmission line to be developed, which operates around 50Ω (of course the impedance changes as the variable capacitances change!), resulting in a low loss phase shifter. If control over growth were tight enough, one could even make use of the synthetic transmission line on the hybrid structures for optimal performance.

APPENDIX1: **Basic Transmission Line Theory**

When the frequency of operation of a circuit gets high enough that elements of the circuit, or more typically, interconnect lines of the circuit, become of the order of a wavelength, traditional circuit methods can no longer be used. This can be envisioned easily when one considers that the underlying assumption of basic (low frequency) circuit theory depends on the point that a voltage (or current) along a conductor is constant. However, when the frequency gets large enough (remember that $v = \lambda f$, where v is the (phase) velocity of EM radiation, λ is the wavelength, and f is the frequency), so that, say, an interconnect line, is of the order of a wavelength, one can see that the voltage or current **along** the line will be changing. Obviously, one needs a new technique to analyze such circuits.

The technique that is used in this situation is called transmission line theory, after the need for a circuit analysis that allows for changing voltages along (very long) power carrying transmission lines (or power lines). There are two approaches to transmission line theory, a rigorous field-based approach which we can develop from Maxwell's equations, and a more simple "distributed circuit" technique which arrives a similar results for many cases of interest. Although the field approach is more rigorous and quite useful for developing a sense of how electric and magnetic fields behave in different media and with different geometries the technique become cumbersomely difficult and hopelessly inefficient many cases of interest. In the Maxwellian approach, small perturbations or additions to the system require a complete reassessment of the problem, while the circuit theory, though not applicable in every circumstance, allows for general

rules to be developed and therefore additions to the circuit at hand are easily addressed. In this regard, it is the distributed circuit techniques that are typically used whenever possible, and in the cases in which uncharted territory is covered, the field analysis serves as an assurance that the simplifications that were made in implementing the circuit technique are in face still valid for the problem at hand. It will be the circuit approach that we first develop now.

Consider a distributed circuit as pictured in Figure 67. One can see that the line consists of incremental elements of serial resistances (representing the ohmic loss) and inductances, as well as parallel conductances (representing the dielectric loss) and capacitances. If the line were completely lossless we could neglect the series resistances and parallel conductances.

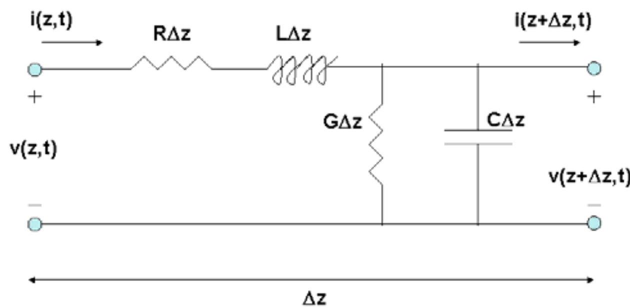


Figure 67 The distributed incremental piece of transmission line with voltages and currents defined. After 185.

From transmission line theory[185] we write the wave equations for *V(z)* and *I(z)*:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 V(z) = 0$$

and

$$\frac{d^2 I(z)}{dz^2} - \gamma^2 I(z) = 0$$

Equation 47

with

$$\gamma = \sqrt{(G + j\omega C)(R + j\omega L)}$$

Equation 48

These wave equations have plane wave solutions:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}$$

and

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}$$

Equation 49

where $e^{-\gamma z}, e^{\gamma z}$ represent the forward and backward traveling waves, respectively.

Let us also define a characteristic impedance, Z_0:

$$Z_0 = \frac{V_0^+}{I_0^+}$$

Equation 50

Combining and rearranging Equation 48 and Equation 49, we can write:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \frac{R + j\omega L}{\gamma}$$

Equation 51

A transmission line is, therefore described by its propagation constant as well as its characteristic impedance.

Loss

There are four types of loss that must be accounted for in microwave media: **metal loss** arising from the ohmic loss from the finite conductivity of the metal (proportional to the square root of the frequency), two types of **dielectric loss: intrinsic dielectric loss** (or loss due to **loss tangent**) arising from a nonzero imaginary component of the complex dielectric function, or more appropriately a nonzero imaginary component of the displacement current (proportional to frequency) and the **dielectric conductivity loss** which is often neglected for nonconductive dielectrics and can be lumped into the loss tangent term (though the dielectric conductivity loss is essentially independent of frequency), and finally the **radiation loss** which arises due to efficient coupling to the air and leakage of energy out of the line like an antenna.

The losses can be generically written in terms of the circuit elements shown in Figure 67 in order to develop a feel for the sources of loss. The actual dependencies will depend on the type of waveguide employed as well as its geometry.

The metal loss tends to be the most predominant loss at high frequencies since the other losses can be minimized through proper design and selection of a low-loss substrate. Using the circuit elements, we can write as a rule of thumb:

$$\alpha_c = \frac{R\Delta z}{2Z_0}$$

Equation 52

Where

$$R \propto \sqrt{\frac{f\mu_r}{\sigma}}$$

Equation 53

σ is the conductivity of the metal. Clearly, a higher impedance design and lower resistance metal traces will allow for the minimization of the metal loss.

The intrinsic dielectric loss can also be a significant source of loss, particularly at high frequencies.

$$\alpha \propto f(C\Delta Z)Z_0 \tan\delta$$

Equation 54

The frequency dependence means that dielectric loss will be more important at higher and higher frequencies.

The dielectric conductivity loss is generally lumped into the intrinsic loss or neglected since it arises from a conductive substrate (which is typically avoided).

$$\alpha_G \propto (G\Delta Z)Z_0$$

Equation 55

Note that this loss mechanism has no frequency dependence.

Finally, the radiation loss is generally small and is essentially loss to the atmosphere in the form of radiated energy. As there is no simple “circuit” rule of thumb to account for it, some type of 3D electromagnetic simulator software is typically used to model the radiation loss.

Types of Waveguides

Now that we have discussed some of the basics of transmission line theory, we can discuss the properties of the actual physical devices that are to be used to carry microwave power. In the general sense, anything that is capable of carrying microwave power can be called a waveguide. In practice, many of the waveguide components that are used can be described as transmission lines (which need two conductors by definition to be distinguished from "waveguide". Depending of the application at hand, ease of production (cost), power handling capability, frequency of operation, and ease of design of components, a number of different structures could be implemented in the design of a particular device.

The "waveguide" devices (rectangular waveguide, circular waveguide) have the advantages of being capable of carrying a lot of power, they have very low loss, but are bulky and expensive to implement. These waveguides have a single conductor and can support a true TEM mode of energy propagation. Coax or rectax (rectangular coax or "recticoax") are typical transmission lines used in test scenarios, they can also support a true TEM mode (meaning no dispersion), but also can be difficult or expensive to fabricate various components within. The drive to shrink geometries that has pushed the semiconductor industry for 50+ years also exists in the passive microwave components arena and certainly has contributed to the increasing popularity of "planar" transmission lines such as microstrip, slotline, stripline, coplanar waveguide (CPW), and a host of other schemes. Some of these can support true TEM modes (stripline), while others with electric field lines penetrating air as well as the dielectric of which the transmission line

is made (yielding an "effective" dielectric constant) can only support "quasi-TEM" type modes (such as coplanar waveguide, CPW).

One of the most important transmission line schemes is the coplanar waveguide, first introduced in 1969 by Wen.[191] The coplanar waveguide or CPW as it will be referred to from here is important for a number of reasons. The most obvious reason, and perhaps most important for mass productions is the ease with which CPW can be fabricated. Along this vein, the characteristic impedance is determined solely by the size of the structures (*S* and *W* in Figure 46) which means that the lines and components could in principal be scaled to small sizes, increasing the density of the devices, and since a ground plane exists between any two given signal lines, the amount of crosstalk between lines is much lower than that of (more conventionally used) microstrip.[186] That said the losses in the system tend to increase as the signal width, *S*, decreases, as evident from Equation 27 and Equation 28. The quasi-TEM mode means that the dispersion of the line is low, which means that the bandwidth of operation for devices in CPW is large.
The pertinent geometrical details and analysis of the CPW lines are covered in the body of this dissertation, 3.4. CPWs on BST.

APPENDIX2: Network analysis

At high frequencies, it is difficult to generate a short or an open that behaves in the ideal sense. "Shorts" tend to have some parasitic inductance and "opens" tend to have some parasitic capacitance (additionally they may "leak" some energy to atmosphere if they are properly matched—i.e. they may behave like an broadcasting antenna!). Without genuine opens and shorts at one's disposal, it is impossible to measure a circuit in terms of its impedance or admittance parameters (Z or Y parameters, as could be easily measured for a circuit at low frequencies). It is because of this that we must formulate and use so-called "scattering parameters" of a circuit (the circuit is more generally called "network").

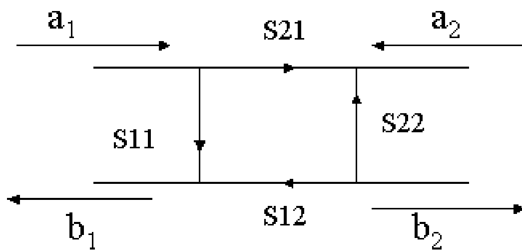


Figure 68 Definitions of the traveling waves for a two-port network.

The Network Analyzer

The machine that measures the scattering parameters of an N-port network is called a network analyzer. In the simplest sense, the network analyzer is made up of four main components: a source of RF energy, a set of devices to separate forward and reverse traveling waves (a_1, b_1, a_2, b_2 in Figure 68), a computer system to calculate the S-

parameters and display them, and finally the necessary cabling to connect devices to be tested and standards that will be used when calibrating.

First, some sort of high frequency signal that will be used as the test signal and reference signal must be generated. This is typically achieved by a voltage controlled sweep oscillator (VCO) (such as the HP 8350) or (with much better frequency accuracy) a synthesized sweeper. The signal is then fed into a test set, which in turn performs several functions. The block diagram of the 4-sampler test set (for example the HP8514B) is shown in Figure 69 and the test set behaves as follows: The transfer switch is first set to port 1 or port 2, which directs the RF energy from the source into the port to be stimulated (set to port 1 in the figure). Next, a power divider diverts a portion of the energy into the ports reference receiver (R1 and R2 in the figure), which allows the VNA to determine the amount of energy which is being directed out to the device under test (DUT). Near the output of each of the ports is a bidirectional coupler which separates forward and backward traveling waves. Energy measured by the measurement samplers (A and B in the figure) determine the backward flowing energy. The ratio of the backward traveling wave to the forward traveling wave represents the reflection of the DUT when the switch is set to the same channel as the measurement sampler (measuring A/R1 or B/R2) and the forward or backward transmission when the switch is set to the opposite channel (measuring A/R2 or B/R2). With these measurements, all four of the scattering parameters can be determined without the need to change the configuration of the device or the system (this architecture is called a S-parameter test set, to be contrasted with a transmission/reflection test set which has no switch and only directs energy out to one of the ports; also to be contrasted with a 3-sampler architecture which has a single

reference receiver and a single power divider, placed *in front* of the switch. An imperfect switch makes this architecture inferior to the 4-sampler architecture, since the reference signal is measured to be the same in both channels).

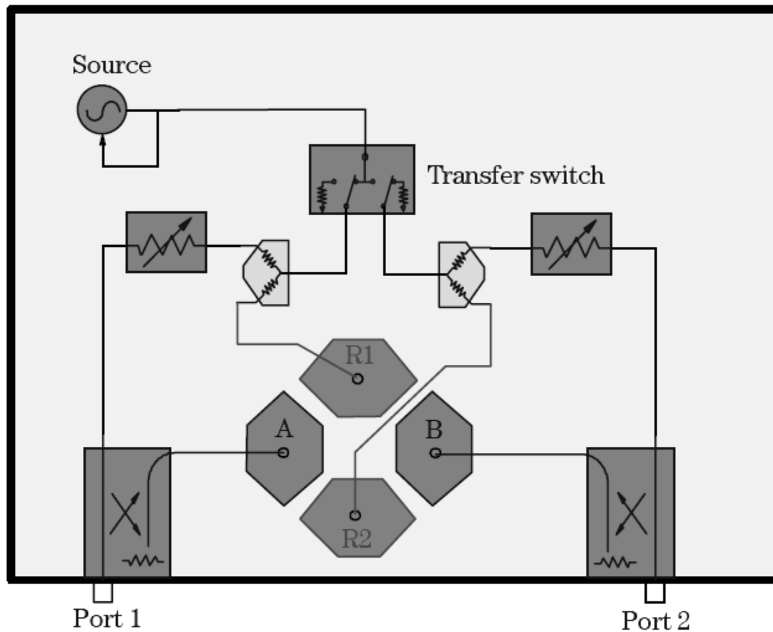


Figure 69. Schematic diagram of the inside of a two-port test set with a four-sampler architecture. Bias tees can also be implemented at the ports for DC biasing of active devices.

The computer system that is used to calculate and display the results from the measurements is technically called the network analyzer, vector network analyzer (VNA), or automatic network analyzer (ANA). The VNA is the device that holds the error correction terms and calculates the "correct" S-parameters after the calibration procedure and uncorrected measurement of a device of interest. The VNA is the heart of the system and typically is the device with which the user interacts. An interface typically allows the user to use the VNA as a controller for all of the other components of the network analyzer, so that the frequency of interest, power level, number of data points, calibration to be used, etc. can be defined.

In addition to this hardware, one might consider the associated cabling and adapters which are necessary to connect the VNA to an actual device part of the network analyzer.

Network Analyzer Calibration

When making microwave (3-30Ghz) measurements, one must consider the systematic errors that are inherent to the test system. Though random errors will also be present, by definition they are not systematically removable. The errors arising from an imperfect switch in the test set, impedance mismatches at the test set ports, frequency response of the transmission and reflection paths, and coupling of fields at input and output (crosstalk) constitute the systematic errors which can be removed. There are essentially two types of error correction schemes that can be applied in order to accurately make microwave measurements, depending how the signal flow is defined. The two types of correction are the 12-term which constitutes two independent forward and reverse "error adapters" and the 8-term "error box" model which is perhaps more intuitive and can be shown to be equivalent to the 12-term.[187] The differences in the error correction will become more clear as we apply them to the error correction scheme or calibration method that will be used to correct the systematic errors in the VNA.

Considering the signal flow in the forward and reverse directions, their combination yields "the error adapter, yielding 12 error terms. (See Figure 70) By measuring enough "standards" (physical devices: shorts, opens, thrus, loads) with known physical and electrical properties, equations describing the scattering matrices of the entire system (error adapter plus standard) can be simultaneously solved, resulting in a known error

adapter, which can then be mathematically removed from further measurements of devices that one wishes to measure, as well as define a “reference plane”: the plane at which the analyzer, cables, probes, connecters, etc. end and the DUT begins.

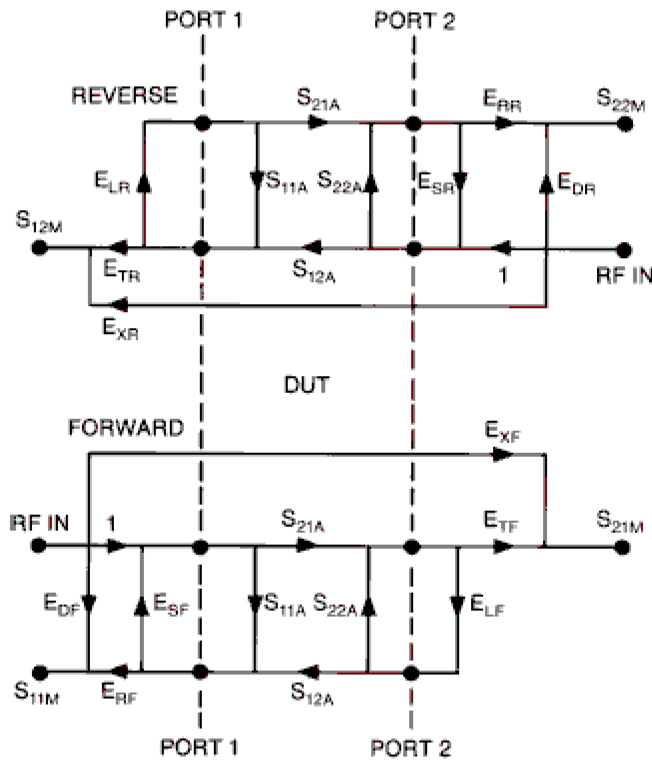


Figure 70 Edf, Edr: directivity (crosstalk within a port from source directly through the directional coupler); Esf, Esr: source match (closeness of Rl to 50ohm), Elf, Elr: load match (quality of load path’s Rl termination), Erf, Err: reflection tracking (frequency response tracking, how well the magnitude and phase of a signal tracks the reference signal), Etf, Etr: transmission tracking (transmission mismatch due to impedance mismatch between test systems ports and DUTs ports); Exf, Exr: isolation (leakage of energy b/w test & ref. channels in VNA) Figure from [188].

Although several methods exist for the full twelve-term error correction, only two are directly implementable in the popular HP8510 series: SOLT and TRL. It should be noted that only two-port test sets (S-parameter) can fully determine all of the sources of error (as opposed to one with two ports and only reflection/transmission capabilities).

SOLT is the most popular method of calibration, due in large part to the facility of use and the dedication on the part of HP in making precision coaxial standards. It is well known, however, that small deviations from ideal in the definitions of the standards can result in large errors,[189] also the characterization of standards above 20GHz becomes quite difficult.[190] For this reason, standards embedded in coplanar waveguide[191] are difficult to realize for this technique due to the fact that the positioning of the probes is not precise. There is therefore ambiguity in the position of the reference plane.

TRL calibration process does not determine the characteristic impedance that is the reference for the subsequent S-parameters. Often assumptions and measurements must be made to find Z_0 and renormalize (to say 50Ω). If this is not done and the imaginary component of the characteristic impedance and the frequency dependence are ignored, at low frequencies (up to 1GHz) the ohmic loss dominates the inductive reactance (per unit length) and the imaginary part of Z_0 can be quite large. This can also cause some ambiguity in the position of the reference plane. TRL is suitable for on-wafer characterization of devices (meaning the calibration standards must be fabricated alongside the DUT, on the same substrate) and problems regarding reference plane position can be circumvented if the DUT is effectively placed behind a transmission line half the length of the thru. At low frequencies, however, the TRL calibration still often fails. Although TRL can be much more accurate than SOLT at high frequencies, and the standards are simpler to fabricate since there is no need for a precise, well defined line, it consumes valuable space on the wafer (long lines (up to 40mm) are required to calibrate down to low frequencies (1GHz)) and the bandwidth of the standards only spans a 8:1

range of frequency in the traditional TRL[192]. As such, discontinuities at these frequencies often result in discontinuities in the measured S parameters of devices, which has no physical meaning, also the reference impedance is set by the characteristic impedance of the line (it must therefore be known precisely) and the reference plane is set at the center of the thru, which can cause a problem in nonzero length thrus (as all in CPW must be) applying an offset delay is possible in the 8510, but this assumes linear phase of the line which is only rigorously valid in coaxial media (again the moding effects of the CPW are the source of problem).

Many other calibration schemes exist, but some of the more accurate schemes are the line-reflect-reflect-match (LRRM) and the Multiline TRL[193] calibrations. LRRM is a patented calibration algorithm that requires additional software (WinCal), which is for sale by Cascade Microtec. Additionally, a program called MultiCal, which runs in HPBasic (interpreted language of the HP9000 OS) environment) provides a simple solution to performing the Multiline TRL calibration and is available freely from NIST. In addition to being the most accurate calibration technique, the Multiline TRL calibration directly provides the user with the propagation constant of the line standards that are used in the calibration. This can be of much assistance in, for example, determining the dielectric properties of the substrate on which the calibration is performed, as discussed in the body of this dissertation.

Calibration Checks

There are several approaches used in order to verify that the calibration performed on the network analyzer is accurate. The most accurate technique would be the use of a "golden standard," that is, the measurement of a device whose S-parameters are well known and can be reproducibly verified by different VNAs in different laboratories when measured under identical situations. Obviously this would be difficult to achieve considering that one would ideally need a device that has been measured by a number of laboratories, but such standards exist and can be obtained from NIST.[194]

Perhaps more realistically, one can use some of the following quick checks, from HP's "10 Hints for making better VNA measurements." The criterion set forth in the following tests are, however, arguably lax. If any of the following tests fail, there are serious problems with your calibration or the cal technique or waveguide type are unsuitable for the frequency at which you are interested. With both ports probes or connectors in air S11 and S22 should measure 0dB plus/minus 1dB. This shows that the reflection coefficient of an air open is very nearly 1. On the Smith Chart (format available in most all VNAs) the reflection coefficient should be on the far right hand side (infinite impedance). In addition, connecting shorts to both ports should give similar results, albeit with the Smith chart showing the reflection coefficient on the left hand side of the chart (zero impedance). By connecting loads to the ports, S11 and S2 should be less than the specified calibrated directivity of the analyzer (usually less than –30dB). Also with the loads connected, measurement of S21 or S12 should be lower than the specified isolation of the VNA (usually –80dB). See **Figure 70** for a pictorial representation of these sources

of error. Finally, when connecting a thru between ports 1 and 2, S21 and S12 should be around 0dB, unless the thru line is particularly long or lossy.

Comparison of Popular Calibration Methods

SOLT (SOLR): commonly used, standards ideal, known C(open), L(short), non-self-consistency, sensitive to probe placement, Zo reference: trimmed resistor, fair accuracy

TRL (LRL): easy to fab. standards, self-consistent, 8:1 frequency range, standards must be on wafer, Zo ref: transmission line, propagation constant determined (shift ref. plane) "poor-fair accuracy"

TRM (LRM): standards easier than SOLT to fab., open/short C/L unknown, Zo ref: trimmed resistor, better frequency range than TRL, propagation constant unknown (cannot shift ref. plane)

LRRM: must have Cascade software, very good accuracy

NIST TRL: (using MultiCal**)** multi-line removes 8:1 issue, propagation constant delivered from cal (can shift ref plane), best accuracy

VITA

Jacob Leach was born in 1980 in Richmond VA. He earned B.Sc. degrees in physics and electrical engineering in 2004 from Virginia Commonwealth University, where he was on Provost's Scholarship, and the M.Sc. degree in engineering in 2007, also from Virginia Commonwealth University. He is affiliated with the following organizations: Member, **Materials Research Society** (2007-present); Member, **Toastmasters** Club #9134 (2003-present); Student Member, **IEEE** (2002-present); President, Vice President Education, **Toastmasters** Club #9134 (2004-2005); Vice President, **Society of Physics Students**, **Sigma Pi Sigma** (2003-2004) where he co-organized and hosted the Zone 4 Conference, in April 2004; Charter President, **Tau Beta Pi** Engineering Honor Society (2002-2003) in which he petitioned to the National Convention in Detroit in October 2002 to secure a chapter of Tau Beta Pi at VCU (Installed March 2003). He has author a number of scientific publications listed below:

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