2012

AlGaN/GaN Dual Channel HFETs and Realization of GaN Devices on different substrates

Mo Wu
Virginia Commonwealth University

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A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at Virginia Commonwealth University

Mo Wu

Director: Dr. Hadis Morkoç
Founders Professor of Electrical and Computer Engineering

Committee in charge

Prof. Morkoç, Hadis

Prof. Atkinson, Gary

Prof. Bandyopadhyay, Supriyo

Prof. Baski, Alison

Prof. Özgür, Ümit

Prof. Reshchikov, Michael

Virginia Commonwealth University
Richmond, Virginia
July, 2012

Acknowledgement

It is my great pleasure to thank many people who have helped me and gave me lots of suggestions to my PhD research work.

Firstly and most importantly, I would like express my great appreciation to my advisor Hadis Morkoç. It is very lucky for me to be brought to this creative research group. Prof. Morkoç created a very productive environment in our research group by providing all kinds of resources to help us grow. In these years, he offered me tremendous help and encouragement. His work ethics, integrity on research, and profound knowledge impressed me all the time and will continuously light up my future life.

I am indebted to my Ph.D. committee members, Professors A. Baski, S. Bandyopadhyay, M. Reshchikov, G. Atkinson, Ü. Özgür for their time and effort. Their advice and support are highly appreciated throughout this endeavor.

Thanks to our group members for their warm-hearted help! Andy Xie always discusses and shares his experience with me when I have problems. Xing Gu, Yi Fu, Bo Xiao, Xiangfeng Ni taught me many things on the research. Thanks to Jacob H. Leach and A. Vitaliy with the great discussion and help. Thanks to Xing Li and Fan Zhang for the help with MOCVD growth. Thanks to Congyong Zhu for the help with the device measurement and characterizations. Thanks to Huiyong Liu, Amy Liu, Emmanuel Rowe and Shujian Liu for the valuable discussion.

At last I would like to thank my family greatly! Thanks to my parents! Whenever I have problems, they always stand on my back! Thanks to my wife, Yan Lu, for the tremendous love and support! Thanks to my sister and brother-in-law for the support in these years!

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Abstract

GaN-based HFETs demonstrate ubiquitous high power and high frequency performance and attract tremendous research efforts. Even though significant advances have been achieved, there still exist some critical issues needed to be investigated and solved. In particular, high defect densities due to inhomogeneous growth and operation under high power conditions bring many unique problems which are not so critical in the conventional Si and GaAs materials systems. In order to reduce the defect density and heat dissipation of GaN-based HFETs, research work on the realization of GaN-based HFETs on bulk GaN substrate has been carried out and the key problems have been identified and solved. Hot phonon scattering is the bottleneck which limits the enhancement of electron velocity in the GaN 2DEG channel. It is found that the plasmon-phonon coupling is the mechanism for converting of hot phonons into high group velocity acoustic phonons. In order to push more electrons into the GaN 2DEG channel in the plasmon-phonon coupling regime and to further reduce the hot phonon lifetime, a novel AlGaN/GaN dual channel HFET structure has been proposed. The growth, fabrication and characterization of such a AlGaN/GaN dual channel HFET structure has been carried out.

Conventionally GaN-based light emitting diodes and laser diodes are grown and fabricated using the *c*-plane III-nitride expitaxy layers. In *c*-plane III-nitride epi-layers, the polarization-induced electric field introduces spatial separation of electron and hole wave functions in quantum wells (QW)s used□LEDs and laser diodes LDs and degrades quantum efficiency. As well, blueshift in the emission wavelength becomes inevitable

with increasing injection current unless very thin QWs are employed. The use of nonpolar orientations, namely, *m*-plane or *a*-plane GaN, would solve this problem. So far, *m*-plane GaN has been obtained on $LiAlO_2$ (100), *m*-plane SiC substrates, and *m*-plane bulk GaN, which all have limited availability and/or high cost. Silicon substrates are very attractive for the growth of GaN due to their high quality, good thermal conductivity, low cost, availability in large size, and ease with which they can be selectively removed before packaging for better light extraction and heat transfer when needed To realize the low cost and improve the internal quantum efficiency of GaN based light emitting diodes, the process for *m*-plane GaN growth on Si (112) substrates has been studied and optimized. The continuous *m*-plane GaN film is successfully grown on Si (112) substrates.

Chapter 1 Introduction

1.1 Background and Motivation

GaN based Heterostructure Field Effect Transistors (HFETs) have been intensively studied for high power and high frequency applications because of high electron density and mobility of AlGaN(AlInN)/GaN 2DEG channel [1] [2]. Compared with the conventional GaAs and InP based pHEMTs, the GaN HFETs demonstrate the high power density [3] and high breakdown voltage [4]. In order to achieve the high cut-off frequencies, many attempts have been carried out and some records have been reported [5] [6] [7].

The outstanding performance of GaN based HFETs origins from the unique material properties of III-nitride materials. The effective mass of GaN is 0.22, almost three times higher than GaAs [8]. As a result the low-field mobility of bulk GaN is much lower than that of GaAs. However, GaN has a larger peak electron velocity, larger saturation velocity, higher thermal stability, and a larger band gap, which is very suitable for the high frequency and high power devices. As well known, the major difference between the Wurtzite III-nitrides and conventional III-V materials (GaAs, InP, i.e.) is the strong spontaneous and piezoelectric polarization [9].

Wurtzite GaN, AlN and InN are the noncentrosymmetric structures, with two different sequences of the atomic layering in the two opposing directions parallel to certain crystallographic axes. Therefore crystallographic polarity along these axes can be observed. Typically along [0001] direction, there are two opposite polarities for Ga and N face GaN, just as shown in Figure 1.1. Since the bond between the Ga and N atoms is not

purely covalent. There is a displacement of the electron charge cloud towards one atom in the bond. As the result the dipolar points from Ga site to N site. The spontaneous polarization is pointed from epi-surface to substrate for the commonly grown Ga-face GaN. While the direction of spontaneous polarization for N-face GaN is opposite.

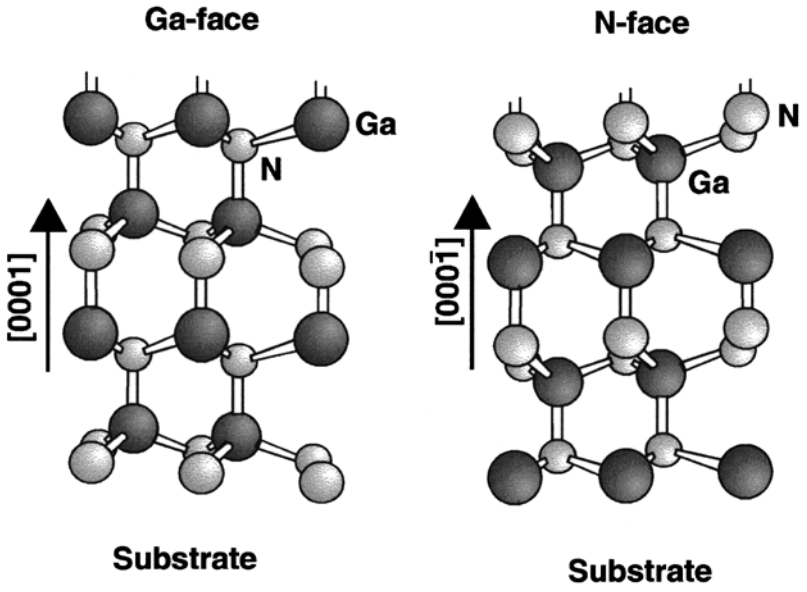


Figure 1.1 Schematic drawing of the crystal structure of wurtzite Ga-face and N-face GaN.

In addition, the piezoelectric polarization introduced by the strain in III-nitrides heterostructure is the other source for the high sheet density in GaN based HFETs. For example, the lattice constant of AlGaN grown on GaN is smaller than that of GaN buffer layer, a strong tensile strain exists in AlGaN barrier layer. The strain-induced distortion forms the piezoelectric polarization field at the AlGaN/GaN interface due to the large piezoelectric coefficient of III-nitride materials. As well the spontaneous polarization in AlGaN layer is greater than that in GaN buffer, there is spontaneous polarization difference in the AlGaN/GaN interface. As demonstrated in Figure 1.2, both the spontaneous and piezoelectric polarization point in the same direction and introduce the large sheet density in AlGaN/GaN 2DEG channel for the Ga (Al) face AlGaN/GaN

heterostructure. The polarization effect induces a high two-dimensional electron gas (2DEG) density at the interface between the barrier and the channel, even without intentionally doping in the barrier layer.

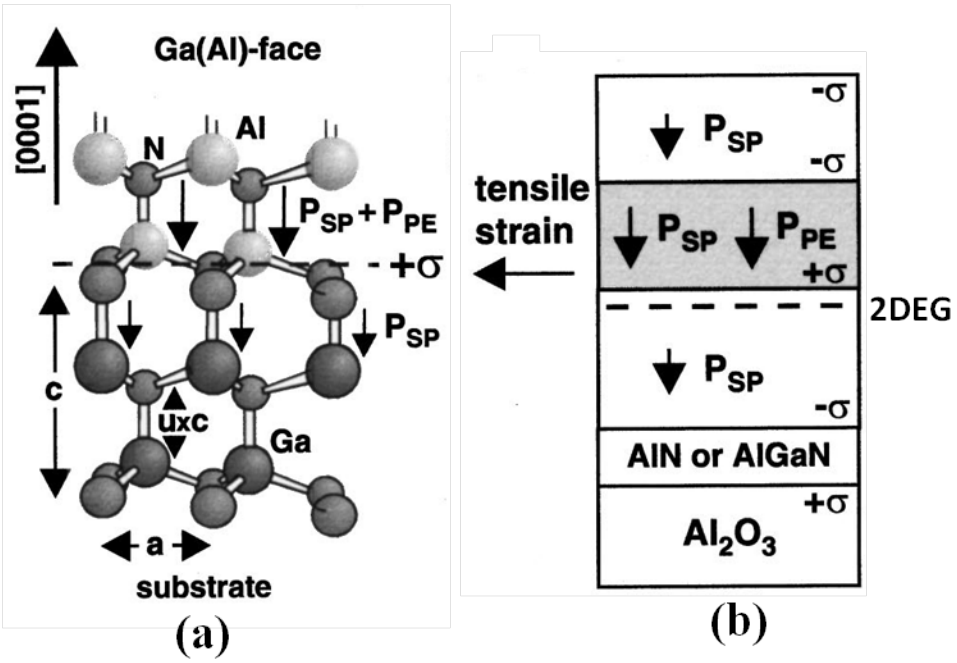


Figure 1.2 (a) Crystal structure, polarization induced bound sheet charge, piezoelectric and spontaneous polarization, of pseudomorphic AlN/GaN heterostructures with Ga(Al)-face polarity. (b) Spontaneous polarization, piezoelectric polarization bound interface charges, and 2DEGs in pseudomorphic GaN/AlGaN/GaN heterostructures with Ga-face polarity.

The high electron velocity of GaN indicates the high operation frequency of GaN-based HFETs. In addition, the better thermal conductivity of GaN than GaAs and InP also helps the heat dissipation in GaN-base HFETs and provides the much larger room for the GaN-based high power devices.

Even though there are many advantages in GaN system and many great performance records reported, some critical problems need to be solved. As mentioned above, the electron velocity of GaN is high; but the measured electron velocity in GaN-based HFETs is lower than the theoretical value. The hot phonon scattering is found as the major obstacle lagging the electron velocity in GaN 2DEG channel. In order to improve

the operation frequency and power of GaN based HFETs, it is necessary to understand the physics of hot phonon scattering and further decrease increase the electron velocity in GaN 2DEG channel by designing device structure and avoiding the hot phonon scattering. To date GaN materials and devices are commonly grown on Sapphire and SiC substrates. Due to the lattice mismatch between GaN-based epi-layers and inhomogeneous substrates, the high density of defects and dislocations formed and propagated to device structure. Therefore the device performance is highly degraded. The best option is to grow the GaN structures on GaN substrate. In this way, the interface quality between substrates and epi-layers can be improved considerably. The dislocation density of device epi-layers can minized. Compared with the commercially used Sapphire substrate, GaN bulk substrates also show much high thermal conductivity, which is good for the heat dissipation.

At last the driving force of reducing the cost of GaN based devices pushes the research on the realization of GaN devices on Si substrates. As we know, GaN based LEDs (Light Emitting Diodes) are grown on Sapphire substrates commercially. If the GaN LED structures can be grown on Si substrates, the cost can be reduced significantly and the GaN devices can be integrated with the mature Si industry in the future.

According to the aspects mentioned above, the research work of my thesis has been carried out from the points of the device physics, design, fabrication and simulation.

1.2 Device Physics

As introduced in the first part, 2DEG formed by the polarization effects between AlGaN barrier and GaN buffer is the essential part of GaN based HFETs. Without intentionally doping the high sheet density can be realized. The cross section diagram and band structure of AlGaN/GaN HFETs are shown in Figure 1.3.

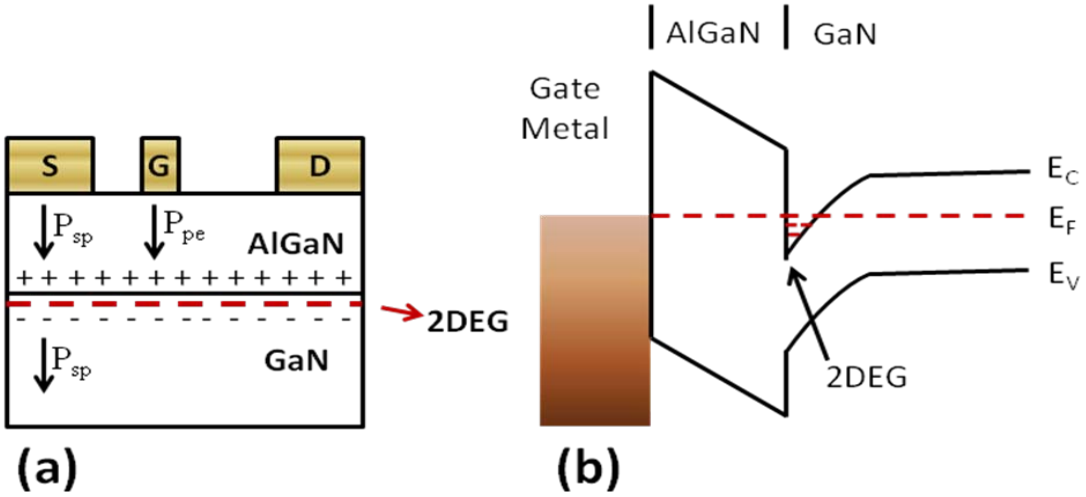


Figure 1.3 The typical device structure of (a) and the band diagram (b) of AlGaN/GaN HFET

In this diagram the typical AlGaN barrier layer is shown. However for GaN based HFETs, InAlN barrier has also been widely studied due to the large banggap difference of InAlN with GaN and the lattice match condition can be realized on GaN buffer. Typically the conduction band difference between lattice matched $In_{0.17}Al_{0.83}N$ and GaN buffer is 1.31eV [10]. That for $Al_{0.2}Ga_{0.8}N$ and GaN is only 0.4eV. Even though usually the barrier layer is undoped, it can be also doped with Si to supply more electrons to 2DEG channel. In order to reduce Ohmic contact resistance, a GaN cap layer is grown on top of barrier layer. As we know, the alloy scattering of AlGaN barrier is major source degrading 2DEG electron mobility. To prevent the alloy scattering and improve the electron mobility, a thin layer of AlN spacer is inserted between AlGaN barrier layer and GaN buffer. In our research group, the thickness of AlN spacer has been optimized as

~1nm. Especially for InAlN barrier HFETs, the electron mobility can be significantly enhanced by using AlN spacer layer. When it comes to buffer layer, the insulate GaN buffer layer is necessary for GaN based HFETs. Due to the lattice mismatch between GaN and commonly used substrates, such as SiC and Sapphire, a large amount of dislocations and defects are formed in buffer layer, which directly cause the buffer leakage. In order to prevent buffer leakage, usually AlN nucleation layer is grown before the GaN buffer growth. In addition, Fe doping is also commonly used to insulate GaN buffer layer [11].

1.3 Device fabrication

The fabrication of GaN HFETs in our research group usually includes three major steps: (1) device mesa isolation; (2) source and drain Ohmic contact; (3) gate patterning and metal evaporation.

The detailed process is shown in the table below:

Table 1.1 The Process Flow for GaN based HFET Fabrication

1. Mesa Etching and Device Isolation	
Sample cleaning	• Acetone, methanol, DI-water ultrasonic cleaning for 3 minutes each.
Photoresist coating	• Spin SPR 3012 photoresist for 30 seconds at 5000 rpm. Soft bake for 10 minutes in 90 °C oven.
Alignment, exposure and developing	• Exposure in 436nm UV light for 90 seconds with power intensity of 8.5 mW/cm^{-2}. Develop in MF-CD-26 for 40 seconds, rinse in DI water for 1 minute.
RIE mesa etching and device isolation	• Etch in ICP system for 3 minutes, with $Cl_4/SiCl_4/Ar$ flow rate is 30/5/18 sccm; chamber pressure is 0.6 Pa, and RIE/ICP power is 80/30 W.

2. Ohmic Contact Formation for Source and Drain	
Sample cleaning	• Acetone, methanol, DI-water ultrasonic cleaning for 3 minutes each. • Clean in boiling aqua regia for 10 minutes, followed by DI-water rinse for 3 minutes.
Photoresist coating	• Spin SPR 3012 photoresist for 30 seconds at 5000 rpm. • Soft bake for 10 minutes in 90 °C oven.
Alignment, exposure and developing	• Exposure in 436nm UV light for 90 seconds with power intensity of 8.5 mW/cm^{-2}. • Develop in MF-CD-26 for 40 seconds, rinse in DI water for 1 minute.
Metal deposition and lift off	• Deposit Ti/Al/Ni/Au metals with thickness of 30/100/40/50 nm in the pressure of 10^{-6} Torr. • Soak the sample in acetone for 2 minutes, apply ultrasonic appropriately for through metal lift-off. • Clean sample in acetone, methanol, DI-water 3 minutes each, and dry it with N_2 blow.
RTA (Rapid Temperature Annealing)	• 800 °C 1 minute in N_2 ambient for rapid thermal annealing.
3. Gate Definition and Metal Deposition	
Sample cleaning	• Acetone, methanol, DI-water ultrasonic cleaning for 3 minutes each. • Clean in boiling aqua regia for 10 minutes, followed by DI-water rinse for 3 minutes.
Photoresist coating	• Spin SPR 3012 photoresist for 30 seconds at 5000 rpm. • Soft bake for 10 minutes in 90 °C oven.
Alignment, exposure and developing	• Exposure in 436nm UV light for 90 seconds with power intensity of 8.5 mW/cm^{-2}. • Develop in MF-CD-26 for 40 seconds, rinse in DI water for 1 minute.
Metal deposition and lift off	• Deposit Ni/Au metals with thickness of 30/50 nm in the pressure of 10^{-6} Torr. • Soak the sample in acetone for 2 minutes, apply ultrasonic appropriately for through metal lift-off.

Typically there are two kinds of HFET patterns. The gate lengths of them are 1μm and 0.7μm respectively. The first critical process is the Ohmic contact. The lower

contact resistance is essential for the high performance RF devices. The metal stack used for Ohmic formation is Ti/Al/Ni/Au. The main mechanism of Ohmic contact formation on GaN is caused by the reaction between Ti and N and Ti-Al alloy formation [12] [13]. The reaction of Ti-N will generate N vacancies on the interface of GaN, which are known to be shallow donor type defects. Therefore, the interfacial region becomes highly doped, which provides a good tunneling status for introducing the Ohmic contact on GaN. On the other hand, the reaction Ti-Al is used to decrease the resistivity in comparison with only Ti metallization. The role of Ni layer is to prevent the diffusion of Al into top gold who serves as the cap layer to avoid oxidization. The most widely used method for determining the specific contact resistance of Ohmic contact is the Transmission line model (TLM) method [14], by which a linear array of contacts with various spacing is fabricated and contact resistances between contacts are measured. The specific contact resistance can be determined from linear interpolation of those resistances. By optimizing the metal thickness and RTA temperature, the contact resistance of 0.4 Ωmm can be realized. The metal thickness is Ti/Al/Ni/Au (30/100/40/50nm) respectively. The annealing temperature is 800°C.

The second critical process is the gate lithography. In our lab, the 0.7 and 1μm gate length devices can be fabricated by using the contact aligner, as shown in Figure 1.4.

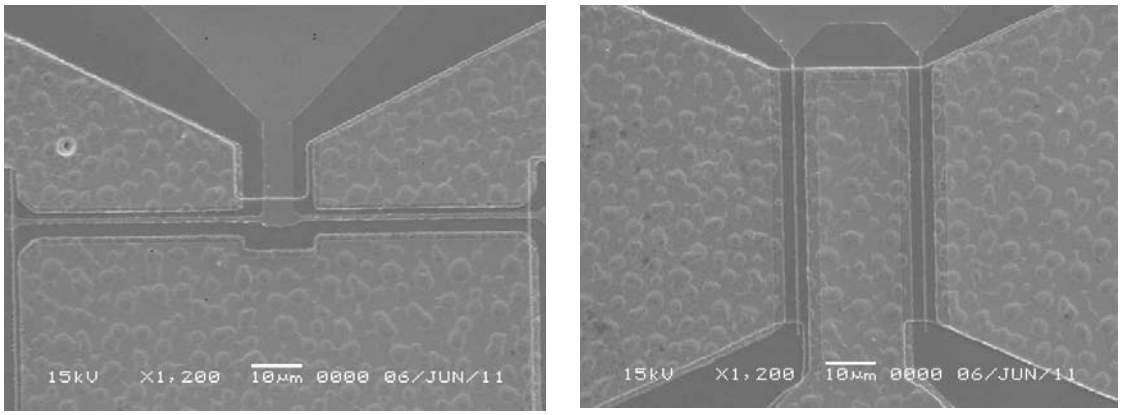


Figure 1.4 SEM images of 1µm (left) and 0.7µm (right) gate length HFETs

1.4 Dissertation synopsis

My dissertation will present the experimental results, discussion and analysis on the AlGaN(InAlN)/GaN HFETs on alternative substrates, the novel device structures to improve the 2DEG channel electron velocity and avoid the hot phonon scattering, and the realization of GaN m-plane epi-layers Si substrates.

Chapter 1 Introduction

In this chapter a review on the developments of the GaN based devices are discussed. As well the background and motivation of the research of this dissertation will be introduced.

Chapter 2 InAlN/GaN HFETs on GaN Bulk Substrates

As mentioned in the introduction, the GaN bulk substrates are the best option for the growth and fabrication of GaN based HFETs. The exploration and attempts of InAlN/GaN HFET structures on GaN bulk substrates will be presented in detail.

Chapter 3 AlGaN/GaN Dual Channel HFETs and Hot Phonon Scattering

Hot phonon scattering is found to be the bottle neck to enhance the electron velocity in GaN 2DEG channel. In this chapter, some investigations based on our previous hot phonon life time measurements are discussed. A novel AlGaN/GaN dual channel HFET structure are introduced to reduce the hot phonon life time and decrease the hot phonon scattering in 2DEG channel.

Chapter 4 Process and Growth of m-plane GaN on Si (112) substrates

In order to reduce the cost of GaN LEDs and improve the IQE (Internal Quantum Efficiency) of GaN LEDs, the efforts on process and growth of m-plane GaN on Si (112) substrates are discussed in this chapter.

Chapter 5 Summary and Future Works

Finally the contributions and critical points of this dissertation work will be summarized. Furthermore, the future works based on the finished research of this dissertation will be discussed.

Chapter 2 InAlN/GaN HFETs on GaN Bulk Substrates

2.1 Motivation and Advantages of InAlN barrier HFETs

AlGaN/GaN HFETs have been intensively studied and commercialized on the RF power amplification applications. As discussed in the introduction chapter, the piezoelectric and spontaneous polarization effects on AlGaN/GaN heterostructure introduces the 2DEG in the interface between AlGaN barrier and GaN buffer layer. In order to avoid the alloy scattering from AlGaN barrier layer, a 1nm AlN spacer layer is usually inserted between AlGaN barrier layer and GaN buffer layer. Even though many decent results and records came out from the AlGaN barrier HFETs, there are still some essential problems originated from AlGaN barrier itself needed to be solved for the further improvement. First of all, there exists tensile strain in AlGaN barrier layer grown on GaN buffer since the smaller lattice constant of AlGaN than that for GaN. This kind of tensile strain also contributes the piezoelectric polarization for AlGaN/GaN HFETs. In terms of the reliability of AlGaN/GaN HFETs in the power applications, the strained AlGaN layer might be a source of the formation of defects after long time stress, which would degrade the performance of HFETs. However the lattice match condition can be realized between InAlN and GaN epi-layers. As indicated in Figure 2.1 [15], the lattice constant of AlN is larger than that of GaN. The lattice constant of InN is smaller than that of GaN. By carefully choosing the composition of InAlN epi-layer, the in-plane lattice

constant of InAlN layer can be matched with that of GaN. In this case the InAlN layer grown on GaN buffer is strain free. Without the strain built in InAlN barrier, the device reliability problem can be relieved to some extent. In addition, even though the lattice constant of InAlN is matched with that of GaN, the bandgap of InAlN is much higher than that of GaN. The bandgap difference between InAlN and GaN is much larger than that for AlGaN/GaN heterostructure, which indicates the better electron confinement in GaN 2DEG channel.

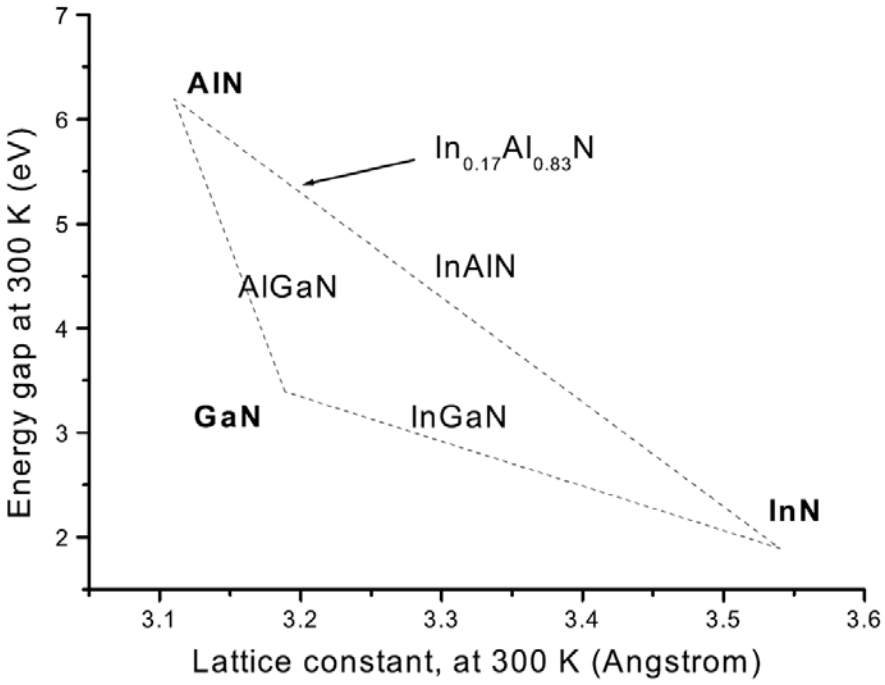


Figure 2.1 III-nitrides energy gap ΔE_g schematic dependence on lattice constant a_0.

Another key issue of AlGaN/GaN HFETs is the maximum current provided by the 2DEG. In order to improve the power capacity of AlGaN-based HFETs, the current density and in turn the sheet density of 2DEG channel should be increased. To increase the sheet density in AlGaN/GaN heterostructure, the Al composition of AlGaN barrier layer should be increased to introduce more polarization charge and further more sheet density in GaN 2DEG channel. However, with the Al composition increased, the tensile

strain in AlGaN barrier layer is increased as well. With the Al composition high enough, cracks appear on AlGaN barrier. As well the crystal quality of AlGaN layer would degrade significantly. To avoid the cracks in AlGaN layer with high Al composition, the AlGaN thickness is highly restricted [16]. In addition, with Al composition exceeds 30%, there is significant drop on electron mobility of 2DEG channel [10]. The lattice matched InAlN can provide much higher sheet density than the commonly used $Al_{0.25}Ga_{0.75}N$ barrier layer without introducing strain. From the theoretical calculation, we can clearly see the polarization charge difference between InAlN and AlGaN. In Table 2.1, the piezoelectric parameter, lattice constant and spontaneous polarization data for III-nitride materials is shown [9].

Table 2.1 Piezoelectric parameter, lattice constant and spontaneous polarization data for III-nitrides

	AlN	**GaN**	**InN**
$e_{31}-(C_{31}/C_{33})e_{33}$ $(C\cdot m^{-2})$	-0.86	-0.68	-0.90
a_0 (Å)	3.112	3.189	3.548
P_{SP} $(C\cdot m^{-2})$	-0.081	-0.029	-0.032

For instance, the typical Al composition of AlGaN barrier used for AlGaN/GaN HFETs is 25%. The In composition of lattice matched InAlN barrier on GaN buffer layer grown on SiC is reported as 17%. The dependence of spontaneous polarization charge density on In composition for InAlN can be expressed as,

$$P_{SP}(In_xAl_{1-x}N) = -0.081 + 0.049C \cdot cm^{-2} \quad (2.1)$$

For InAlN with 17% In composition, the spontaneous polarization charge density would be -0.0727$C{\cdot}cm^{-2}$. Since the InAlN is lattice matched with GaN buffer layer, there is no piezoelectric polarization introduced by strain.

For AlGaN, the relation of spontaneous polarization charge density with Al composition is expressed as,

$$P_{SP}(Al_xGa_{1-x}N) = -0.052x - 0.029C \cdot cm^{-2} \tag{2.2}$$

If the Al composition of AlGaN is 25%, the spontaneous polarization charge density would be -0.042$C{\cdot}cm^{-2}$. Since there exists the tensile strain on AlGaN layer grown on GaN buffer, the piezoelectric polarization charge density should be included and calculated. The piezoelectric polarization charge density is related with lattice constant [9].

$$P_{PE} = 2 \cdot \frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \tag{2.3}$$

For the AlGaN/GaN heterostructure, we consider the GaN buffer layer is fully relax and AlGaN barrier layer is fully strained. Therefore, in this equation, a_0 is the lattice constant of GaN and a the lattice constant of AlGaN. Using the linear Vegard's law, we can have the lattice constant of $Al_{0.25}Ga_{0.75}N$ as 3.17$\AA$. The piezoelectric parameter of $Al_{0.25}Ga_{0.75}N$ can be calculated as,

$$\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)(Al_{0.25}Ga_{0.75}N) = (-0.86)\cdot 0.25 + (-0.68)\cdot 0.75 = -0.725C \cdot cm^{-2} \tag{2.4}$$

Therefore, the piezoelectric polarization charge density can be calculated as,

$$P_{PE}(Al_{0.25}Ga_{0.75}N) = 2 \cdot \frac{3.17 - 3.189}{3.189} \cdot (-0.725) = -0.0086C \cdot cm^{-2} \tag{2.5}$$

Finally the polarization charge density of $Al_{0.25}Ga_{0.75}N$ is,

$$P(Al_{0.25}Ga_{0.75}N) = P_{SP}(Al_{0.25}Ga_{0.75}N) + P_{PE}(Al_{0.25}Ga_{0.75}N)$$
$$= -0.042 - 0.0086C \cdot cm^{-2} = -0.0506C \cdot cm^{-2} \quad (2.6)$$

Compared with the polarization charge density of AlGaN, that for lattice matched InAlN, -0.0727$C{\cdot}cm^{-2}$, is much larger. Therefore, with InAlN barrier, more electrons can be introduced into the 2DEG density and higher sheet density can be obtained. Theoretically the calculated sheet density as high as $2.7\times10^{13}cm^{-2}$ [17] can be obtained in InAlN/GaN heterostructure and the record sheet density of $2.68\times10^{13}cm^{-2}$ [18] was reported as well. The results from our research group show that the electron mobility does not degrade obviously as the sheet density increased for InAlN barrier HFEs. By inserting a 1nm AlN spacer between $In_{0.18}Al_{0.82}N$ barrier and GaN buffer, the electron mobility of 1510 cm^2/Vs at 300K and 17600 cm^2/Vs at 10K is realized [2].

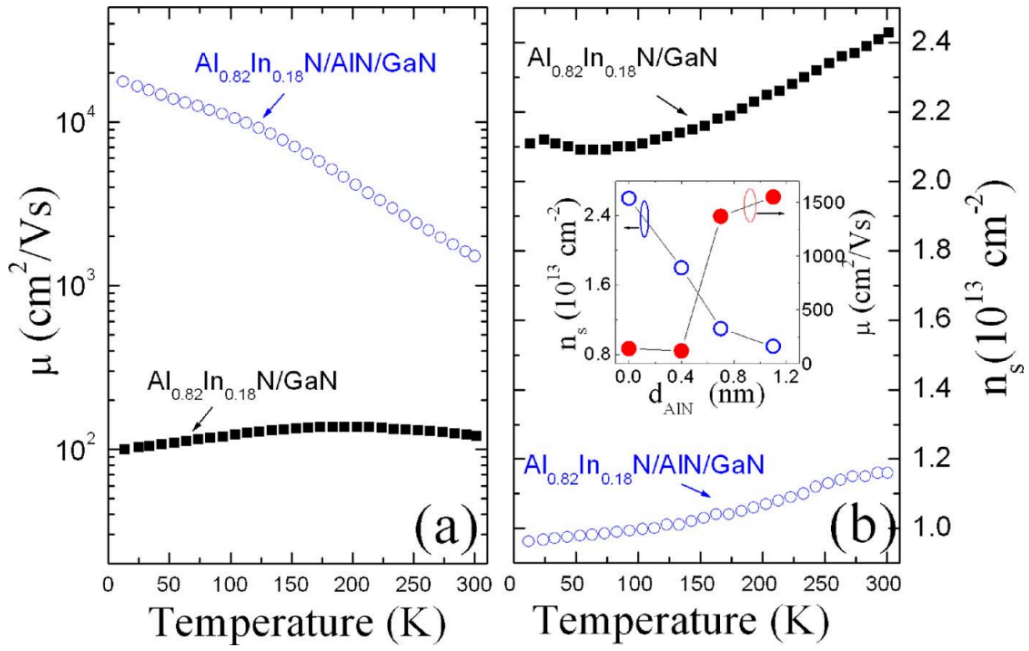


Figure 2.2 Temperature dependent (a) Hall mobility and (b) sheet carrier density for the nearly lattice-matched $Al_{0.82}In_{0.18}N$ / GaN HFETs with and without a 1 nm AlN spacer. The inset shows the effect of AlN spacer on Hall mobility and sheet carrier density of $Al_{0.845}In_{0.155}N$ /AlN/GaN HFET structures.

The last advantage of InAlN barrier over the conventional AlGaN barrier is on the barrier layer scaling. Even though AlGaN based HFETs show the decent power performance over GaAs and InP pHEMTs. It is very necessary to extend the operation of operation for GaN based HFETs. To obtain very high frequency performance, it is necessary to shrink the gate length while maintaining the structural aspect ratio of gate length to gate-to-channel separation [19] [20]. Usually the recess gate technique is used for the submicron gate length HFETs to extend the cut-off frequency. However, as far as AlGaN based HFETs is concerned, the sheet density already start to decrease for the typical 20nm barrier thickness. If the barrier underneath the gate area is etched down further, the corresponding sheet density would be reduced significantly. Therefore the available power density for HFETs would be reduced tremendously [16]. As shown in Figure 2.3, the sheet density of AlGaN/GaN heterostructure decreases significantly with the AlGaN barrier thickness decreased from 20nm to 10nm [21].

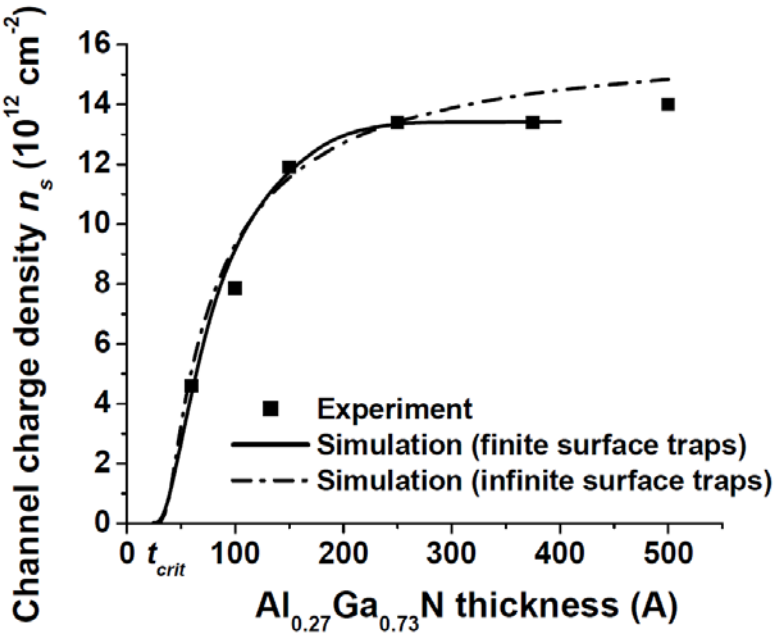


Figure 2.3 Simulated and the experimental dependence of the channel charge density n_s on the AlGaN thickness t_{AlGaN}.

On the contrary, the sheet density of InAlN/GaN heterostructure does not change obviously with the InAlN barrier thickness decreased to even 10nm, as shown in Figure 2.4. As the result, the high power density can be obtained at high operation frequency. Recently the power density of 5.8W/mm at the operation frequency of 35GHz has been reported on the InAlN/GaN HFET with only 9.8nm InAlN barrier [22].

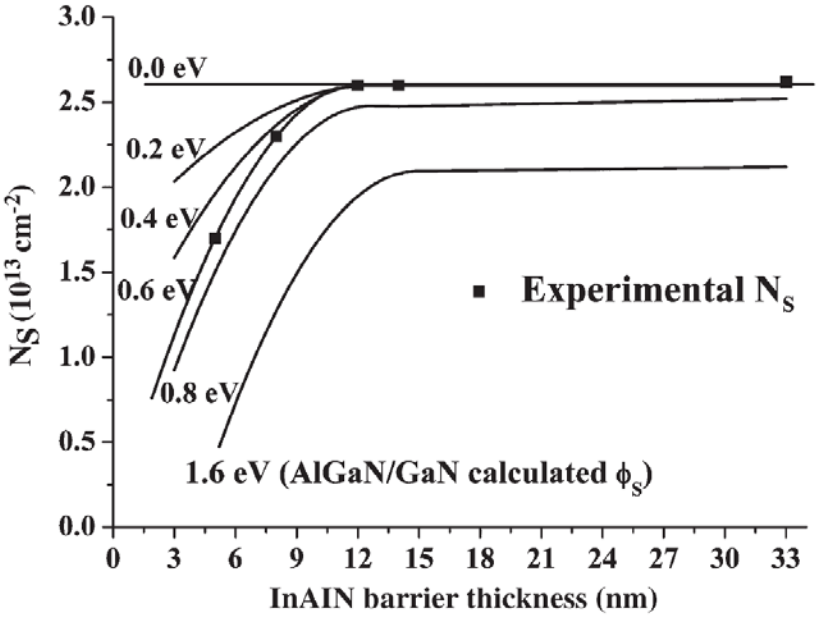


Figure 2.4 Simulated NS_{Hall} data as a function of the $In_{0.17}Al_{0.83}N$/GaN HEMT barrier thickness. The experimental results are indicated by the squares. Corresponding electron mobilities are approximately 1000 cm^2/Vs down to 9-nm barrier thickness and 600 cm^2/Vs for the 6- and 3-nm barrier thicknesses.

Overall the lattice matched InAlN barrier can be realized on GaN buffer, which can improve the reliability of GaN based HFETs. The large bandgap difference between InAlN barrier and GaN buffer layer can improve electron confinement of 2DEG channel. Without introducing extra strain in barrier layer, InAlN/GaN heterostructure has much larger polarization charge density and in turn much higher sheet density. At last InAlN barrier shows much less sheet density dependence on barrier thickness, which can be used for the high power application on high operation frequency.

2.2 Substrates for GaN based HFETs

Substrates for the growth of III-nitride materials are always a bottleneck for the performance improvement of GaN based devices. Back to several decades when GaN related research has been launched, there was no native GaN substrate available for GaN epitaxy. The popularly used substrates for GaN devices are Sapphire, SiC and Si. Due to the lattice mismatch of the inhomogeneous epitaxy, a substantial density of misfit and threading dislocations (in the range of 10^8 and 10^{10} cm^{-2}) is formed from the interface between III-nitride epi-layers and substrates, which degrade the device performance significantly. As far as Sapphire substrates is concerned, there is a 30° rotation for GaN epi-layers. The lattice mismatch between Sapphire and GaN is ~13%. In addition, the poor thermal conductivity of Sapphire substrate impedes the heat dissipation of GaN devices. GaN based HFETs grown on Sapphire substrates always show large current degradation at high drain voltage because of the self-heating effects. SiC substrates are mostly used for the growth of GaN based HFETs for their good thermal conductivity and relatively smaller lattice mismatch with GaN. However, the high cost of SiC substrates is a big issue for the commercialization of GaN HFETs. The defects and dislocations originated from interface also generate the trap related problems. Si substrates are the other option for the low cost and compatibility with mature Si process. But the large lattice mismatch plus the large thermal expansion difference with GaN make cracks come out on GaN epi-layers easily. The best substrate for GaN devices is the native GaN substrate. Recently the technologies of GaN bulk crystal and HVPE GaN substrate growth have been greatly developed. A small amount of GaN bulk substrates are available in the market. Compared with SiC substrates, GaN substrates have slightly

lower thermal conductivity, but the homogeneous growth can tremendously decrease dislocation density and enhance the performance of GaN based HFETs. In order to pave the road for the applications of GaN substrates on GaN based HFETs, it is necessary to investigate and introduce the techniques achieved on SiC and Sapphire substrates into GaN bulk substrates.

In this chapter the growth, fabrication and characterization of InAlN/GaN HFETs on GaN substrates will be discussed. Some key issues about the application of GaN bulk substrates on GaN based HFETs will also be addressed.

2.3 Growth and Fabrication of InAlN/GaN HFETs on GaN Bulk Substrates

So far there are still some issues needed to considered and solved for the GaN growth on GaN substrates, even though GaN bulk substrates have many advantages over the conventional substrates. When it comes to the HVPE GaN bulk substrates, the surface of the GaN substrate is usually composed with a thin layer of conductive layer introduced by the chemical mechanical polishing process. The GaN buffer directly grown on such kind of substrates would be conductive as well. It has been reported that the regrowth interface between the epitaxial GaN layer and GaN substrate also contains impurities such as Si, O, and C [23]. In particular, a thin Si doping layer at or near the regrowth interface due to the air contamination would result in a parallel conduction channel for GaN based HFETs. To solve this problem, the ultraviolet photoenhanced chemical (PEC) etching has been applied before MOCVD GaN growth on GaN bulk substrates [24]. By using ICP *ex-situ* etching and MOCVD *in-situ* H_2 etching, we successfully removed the conductive layer on the surface of GaN bulk substrates.

The GaN bulk substrates used for our experiments are 10×10 mm^2 Fe-doped semi-insulating *c*-plane GaN substrates produced by HVPE growth [25].The first surface treatment step is ICP *ex-situ* etching. Before loading into the OMVPE chamber, Fe-doped GaN substrates are etched about 600nm in a SAMCO inductively coupled plasma (ICP) system with Cl_2 and Ar gases to remove the damaged surface layer caused by chemical mechanical polishing. Then a combination of aqua regia and de-ionized water, in order, was used for cleaning the GaN substrates before transferring them to the deposition chamber. The second step is MOCVD *in-situ* H_2 etching. After the GaN bulk substrates are loaded into MOCVD chamber, prior to growth, the GaN substrates were also treated *in-situ* with H_2 for 30min under the protection of NH_3 ambient at 900°C. After the H_2 treatment, which is estimated to remove an additional 50nm of GaN surface layer. In this step, the H_2 etching can remove the defective surface caused by the physical ICP etching. In the meantime, the NH_3 ambient high temperature annealing can also heal the surface atom bonds damaged by the physical bombardment during the ICP etching. By using such a two-step etching, the high resistive GaN buffer can be realized on GaN bulk substrates. The results on the GaN buffer resistivity will be discussed in detail later.

In order to grow InAlN/GaN HFET structures on GaN bulk substrates, the lattice match condition of InAlN barrier with GaN buffer layer should be confirmed at first. Since the strain status of GaN buffers grown on different substrates are different, the lattice match condition for InAlN on GaN buffer grown on Sapphire substrates is different with that for InAlN on GaN bulk substrate. Based on XRD reciprocal space mapping measurement, Jacob found that the In composition of lattice matched InAlN on Sapphire substrates is ~15.4%. While that for lattice matched InAlN on GaN bulk substrates is ~18%.

Therefore, in our experiments, we grew the InAlN barriers with different In compositions on Sapphire and GaN bulk substrates accordingly. The XRD ω-2θ measurement was performed on the InAlN/GaN HFET structure grown GaN bulk substrate, as shown in Figure 2.5. The clear fringes indicate the good interface quality of InAlN/AlN/GaN heterostrucure.

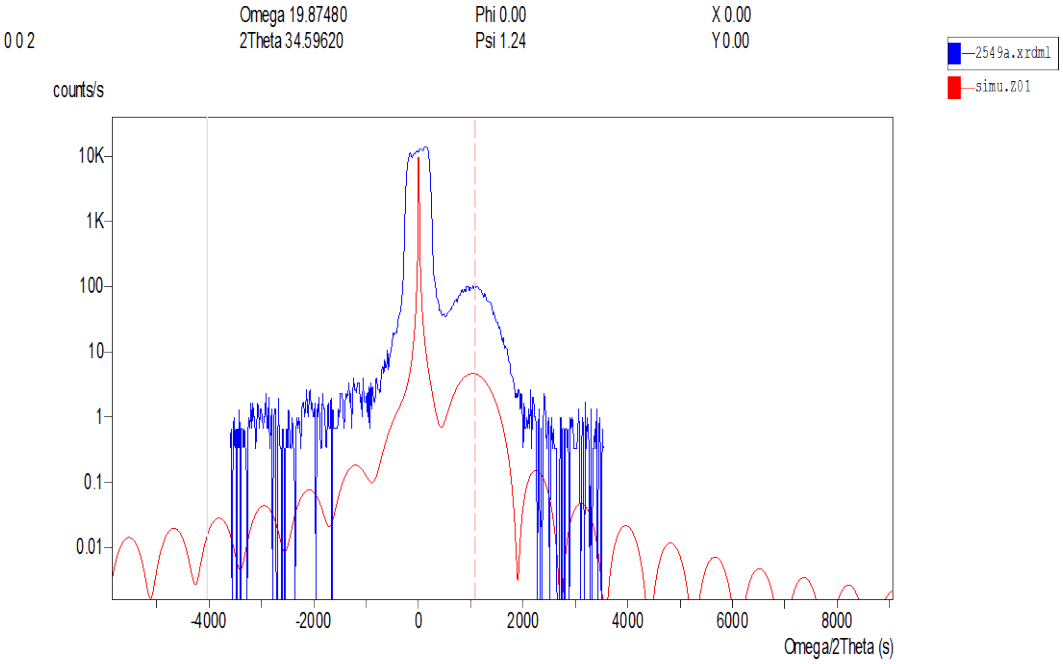


Figure 2.5 XRD *ω-2θ* measurement for the InAlN/GaN HFET structure grown on GaN bulk substrate. The blue curve is the measured data and the red one is the simulated data.

To demonstrate the advantages of GaN bulk substrates over Sapphire substrates, the InAlN/GaN HFET structure were grown on both Sapphire substrate and GaN bulk substrates for comparison. The epi-structure of InAlN/GaN on Sapphire substrates consists of 300nm AlN nucleation layer, 4μm GaN buffer, 1nm AlN spacer, 20nm 15.4% InAlN barrier and 2nm GaN cap layer. For InAlN/GaN on GaN bulk substrates, there are 2μm GaN buffer, 1nm AlN spacer, 20nm 18% InAlN barrier and 2nm GaN cap layer. After MOCVD growth finished, the HFETs were fabricated according to the standard

process discussed in the introduction chapter. At first, a metal stack of Ti/Al/Ni/Au (30/100/40/50 nm) was deposited on both samples by e-beam evaporation and then annealed at 800 °C for 60 s for Ohmic contacts. Finally, after mesa isolation by etching 150 nm of the epilayer in the ICP system using a Cl_2-based chemistry, the gate metal Pt/Au (30/50 nm) was deposited.

2.4 DC and Pulse I-V Characterization of InAlN/GaN HFETs on GaN bulk substrates

In order to investigate the device characteristics, the DC and pulsed current-voltage (I-V) measurements were performed on InAlN/GaN devices both on GaN and sapphire substrates. The I-V characteristics are shown in Figure 2.6. All the HFETs under discussion have 1.0μm gate length with 90μm gate width and 3.5μm source-drain separation. The pulsed measurements were set up as 1μs pulse length and 0.1% duty cycle, by using a Keithley 4200 parameter analyzer. InAlN/GaN HFETs on both GaN and sapphire substrates show very good pinch-off characteristics at -8 V gate bias without any noticeable current leakage. The knee voltage indicative of the current saturation point for the InAlN/GaN HFET on the GaN substrate is about 6V at zero gate bias, whereas that for the InAlN/GaN HFET on sapphire is only 4.5V, indicative of better Ohmic contacts in the latter. From the TLM measurement, it is found that the contact resistances (R_C) of the HFETs on the bulk GaN substrate and those on the sapphire substrate are 1.1 and 0.67Ω·mm respectively. At zero gate bias, InAlN/GaN HFETs on the GaN substrate have a peak saturation drain current density (I_{Dmax}) of about 1.3A/mm [Figure 2.6 (a)] compared to 1.38A/mm for that on sapphire. For InAlN/GaN HFETs on the GaN

substrate, the DC and pulsed I-V characteristics are nearly identical for gate biases from -2V to -8V. At a gate bias of V_{GS} = +2 V the I_{Dmax} at V_{DS} = +15 V is higher by only 10 % in the pulsed bias case compared to that under DC bias (1.6A/mm and 1.45A/mm, respectively). However, for the same HFET structure grown on sapphire, saturation drain current values under pulsed drain bias were much higher than those under DC bias (~2.0 A/mm versus ~1.25A/mm at a drain bias of V_{DS} = +15V and a gate bias of V_{GS} = +2V). It is well known that the drain current density degradation at high drain voltage bias is caused by the self-heating in the 2DEG channel due to the poor thermal conductivity of sapphire [26]. With the drain voltage is increased, the electric field increases in the 2DEG channel as well and electrons are highly accelerated and become hot. The heat generated in the 2DEG channel eventually dissipates through the substrate. Therefore, a GaN substrate is obviously advantageous as it has a much higher thermal conductivity than that of sapphire. It should be noticed that the pulsed saturation current for the HFET on the sapphire substrate is higher than that for the HFET on bulk GaN substrate. That is partially due to the lower In composition used for the HFET on the sapphire substrate in order to achieve lattice matching with the GaN buffer layer grown on sapphire substrate. Therefore, higher sheet density is expected for the HFET on the sapphire substrate.

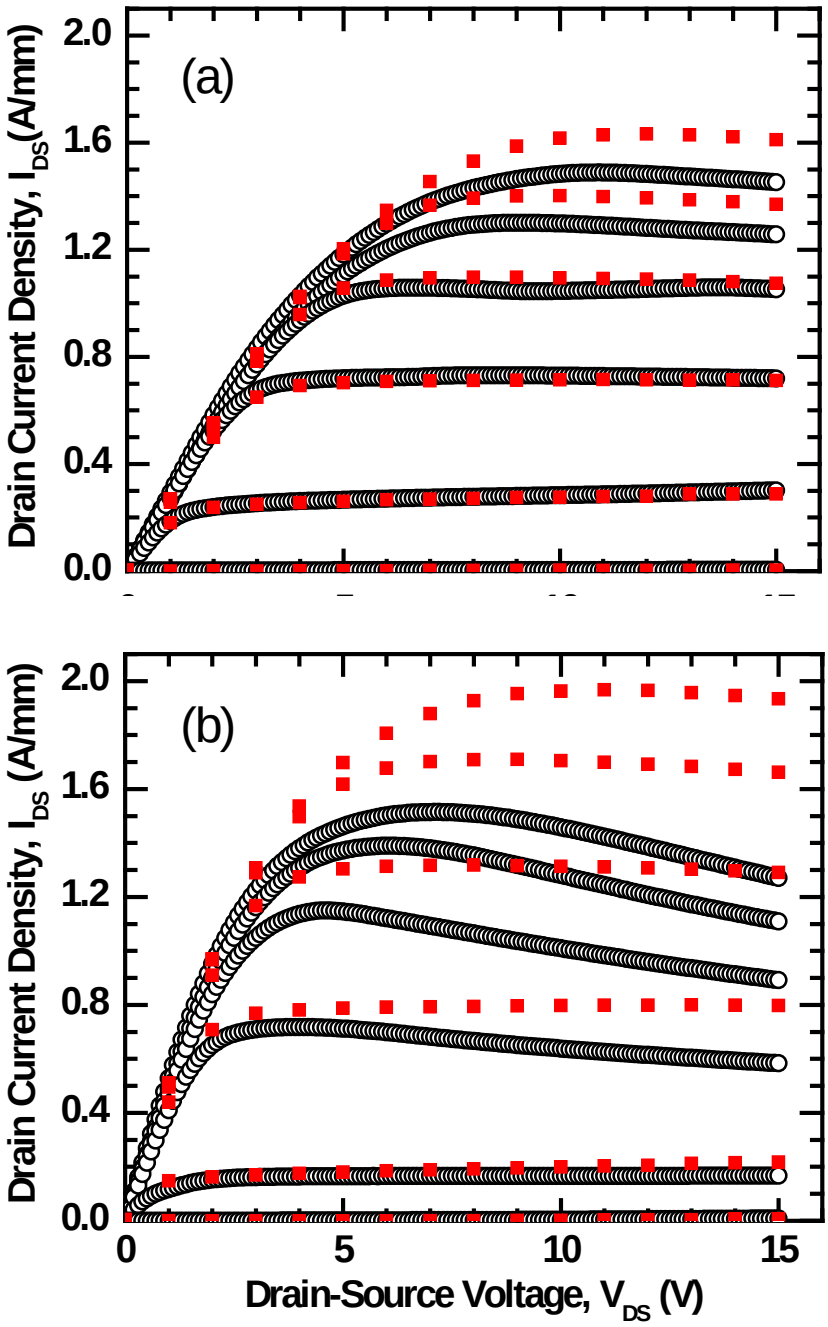


Figure 2.6 DC (black open circles) and pulsed (red closed squares) I–V characteristics of (a) an InAlN/GaN HFET on GaN substrate, and (b) an InAlN/GaN control HFET on sapphire. The gate voltage was varied from +2 V to -8 V with 2 V steps.

The transconductance (g_m) and drain current density measured versus gate bias in the range between 0 and -10V with V_{DS} = 7V are shown in Figure 2.7. The drain current densities under DC and pulsed measurements for the InAlN/GaN HFET on the GaN

substrate are nearly identical, consistent with the results shown in Figure 2.6. The maximum transconductance ($g_{m,max}$) for the InAlN/GaN HFET on GaN substrate under both DC and pulsed drain bias is about 225 mS/mm [Figure 2.7 (a)].

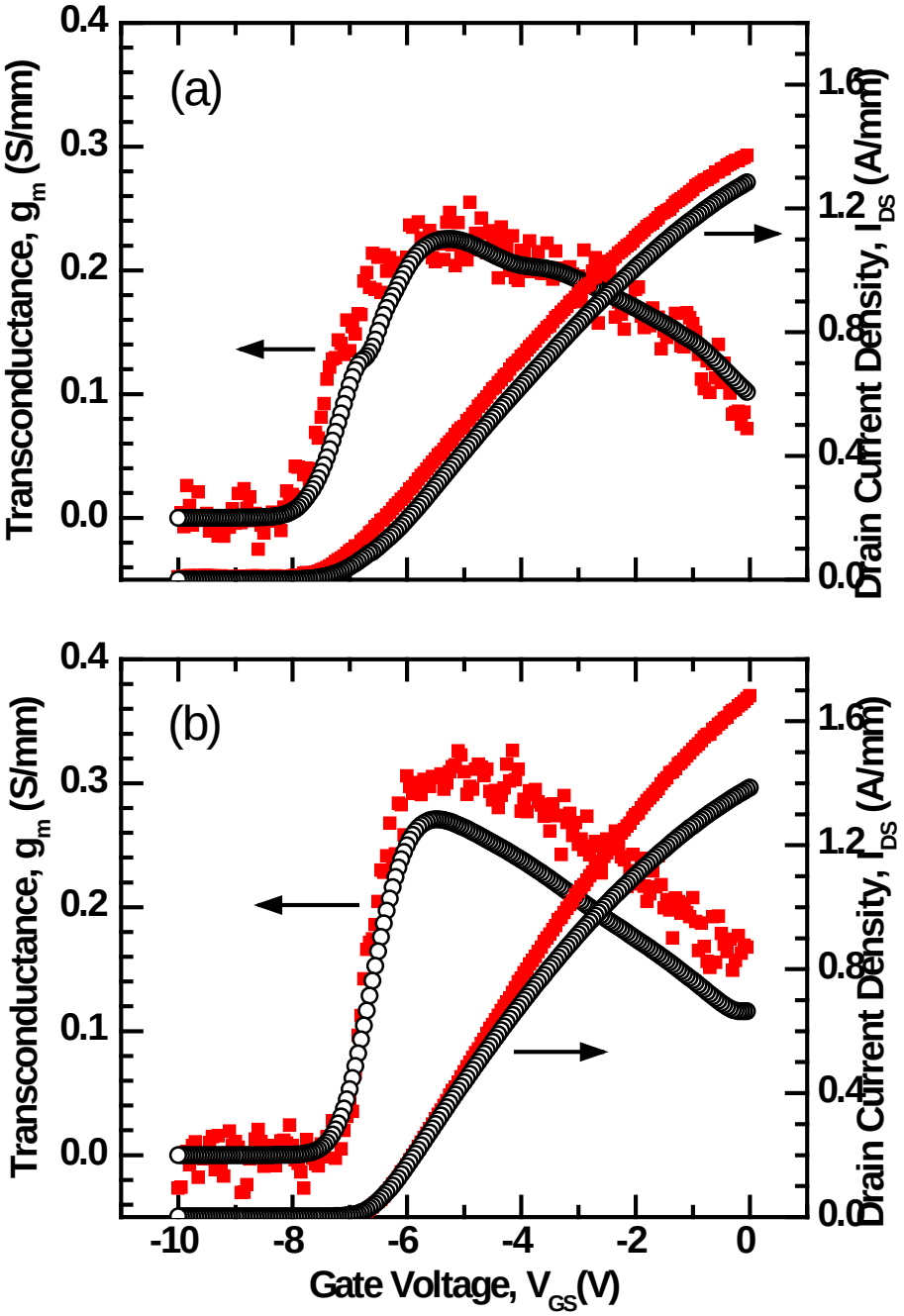


Figure 2.7 DC (black open circles) and pulsed (red closed squares) transfer characteristics and extrinsic transconductance at V_{DS} = 7 V for (a) an InAlN/GaN HFET on GaN substrate and (b) an InAlN/GaN control HFET on sapphire.

The InAlN/GaN control HFET on sapphire shows a higher $g_{m,max}$ (275mS/mm) [Figure 2.7 (b)], which we attributed to the lower Ohmic contact resistance. GaN buffer current leakage is an impediment to the performance of the GaN based HFETs. A large buffer current leakage would introduce an additional conduction path and compromise the gate control of the conduction channel. The defects formed in the GaN buffer layer on sapphire are considered to be the major source of current leakage. Homoepitaxy on a GaN substrate is the best alternative to improve the GaN buffer crystal quality and reduce the current leakage.

It has been reported that the regrowth interface between the epitaxial GaN layer and GaN substrate also contains impurities such as Si, O, and C. In particular, a thin Si doping layer at or near the regrowth interface would result in a parallel conduction channel. In the present work the ICP dry etching with Cl_2 and Ar gases combined with H_2 *in-situ* etching in NH_3 ambient in OMVPE has been used to eliminate the interface charges as judged from very low buffer leakage. When other recipes were used in our laboratory, we also observed unacceptably high buffer leakage currents. To test the GaN buffer leakage current, mesa-to-mesa I-V measurements were performed on the InAlN/GaN HFET samples.

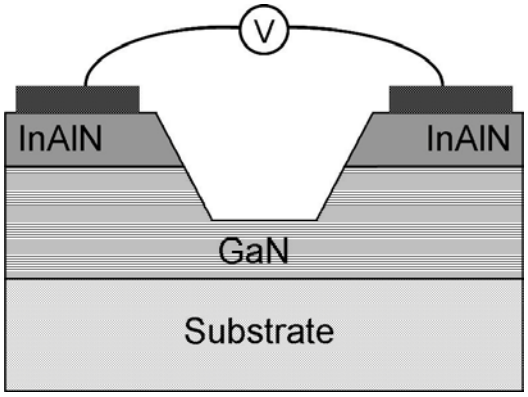


Figure 2.8 Diagram for the mesa-to-mesa I-V measurement

These test measurements are based on applying a voltage bias between the source pads of two adjacent devices and checking the resulting current density, just as sketched in the inset of Figure 2.8. Since every device on the wafer has been isolated by etching away a 150 nm-thick portion of the InAlN/GaN layer, the current is allowed to flow only through the GaN buffer layer from one source contact to the adjacent one. In our case the source pad width normal to the current flow direction is 320μm and the separation between two adjacent source pads is 100μm. As shown in Figure 2.9 the GaN buffer leakage current density measured on the GaN substrate is 3×10^{-9} A/mm at 10 V mesa-to-mesa voltage bias, which is much lower than that for the control HFET sample on sapphire (4×10^{-7} A/mm at 10 V). The corresponding GaN buffer resistivity is about $3.5\times10^{8}\Omega\cdot$cm, which is slightly lower than the resistivity of the substrate ($10^{9}\Omega\cdot$cm [21]) but higher than the recently reported values for AlGaN/GaN HFETs grown on SiC substrates by using an AlGaN interlayer in the GaN buffer to reduce the buffer leakage current ($10^{8}\Omega\cdot$cm [27]). From the leakage current data, it can be safely concluded that any regrowth interface charge if present is ineffectual and the employed etching method can effectively prevent the impurity contamination from the GaN substrate surface and or the processes employed.

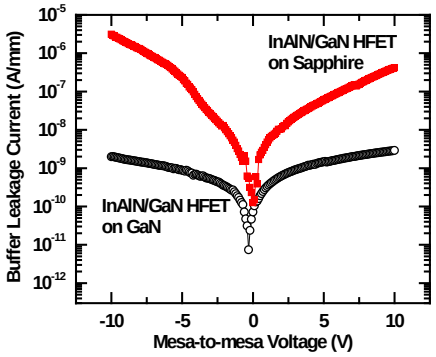


Figure 2.9 Buffer leakage current for of the InAlN/GaN HFETs on GaN (black open circles) and sapphire (red closed squares) substrates.

The last point to be mentioned is that the high gate leakage current has been reported in the InAlN/GaN HFETs. Approaches such as inserting a high-κ dielectric layer underneath the gate metal [28] and employing Pt/Au Schottky gate [29] have been shown to reduce the gate leakage. In the present work, Pt/Au metallization as opposed to conventional Ni/Au was used for the gate Schottky contact [30]. The resulting gate leakage current density at -10V was only 0.008mA/mm, which is comparable to some [31] or even lower by a factor of three than other reported results without any gate dielectric layer (0.065mA/mm [32]).

2.5 RF Characterization of InAlN/GaN HFETs on GaN bulk substrates

After the DC and pulse characterization, the RF performance of InAlN/GaN HFETs on GaN bulk substrates is measured by using the HP8510B network analyzer. The HP8510B network analyzer system is composed with HP 8510B network analyzer, HP 6629A DC power supply system, Electroglass wafer prober, HP8514B S-parameters test set which goes from 45 MHz to 20 GHz, HP 33150A bias tees, and two Cascade coplanar waveguide probes ACP 40. The bias tees consist of an inductor and a capacitor; the inductor keeps the AC signal from leaking into the DC power supply; and the capacitor keeps the DC power from interfering with the network analyzer. The configuration of the network analyzer system is shown in Figure 2.10. Before the s-parameter measurement, a series of calibration is carried out by using the standard calibration sample to deembed the contributions by the network analyzer and the measurement test bed. The “Short”, “Open” and “Load” method is used as the calibration procedure. After the calibration

finished, the s-parameters of HFET samples are measured with frequency varied from 2GHz to 20GHz.

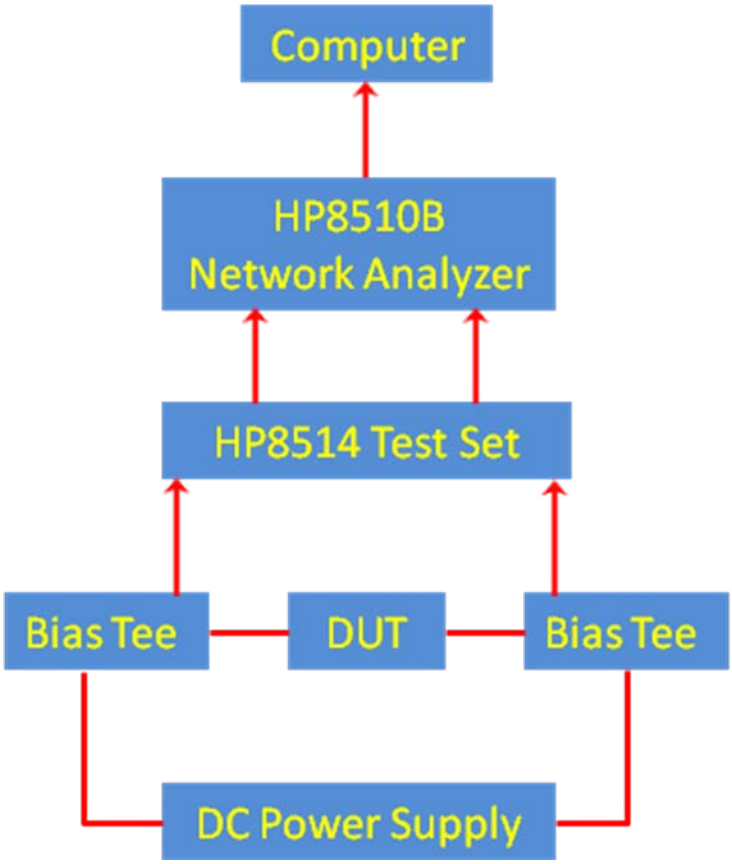


Figure 2.10 System configuration of network analyzer

After the s-parameters collected, they are converted into H-parameters. The unity current gain cut-off frequency (f_T) and maximum power gain cut-off frequency (f_{max}) are calculated from H-parameters, as shown in Figure 2.11. For the InAlN/GaN HFETs on GaN bulk substrates, the devices with the gate length of 1.1μm and 0.7μm were measured. The unity current gain cut-off frequency (f_T) of 1.1μm gate length HFETs is 14.3GHz under the drain bias of V_{DS}=15V and gate bias of V_{GS}=-6V. The corresponding maximum power gain cut-off frequency (f_{max}) is 21.5GHz. For 0.7μm devices, the f_T and f_{max} under the same DC bias is 20.4GHz and 24.8GHz.

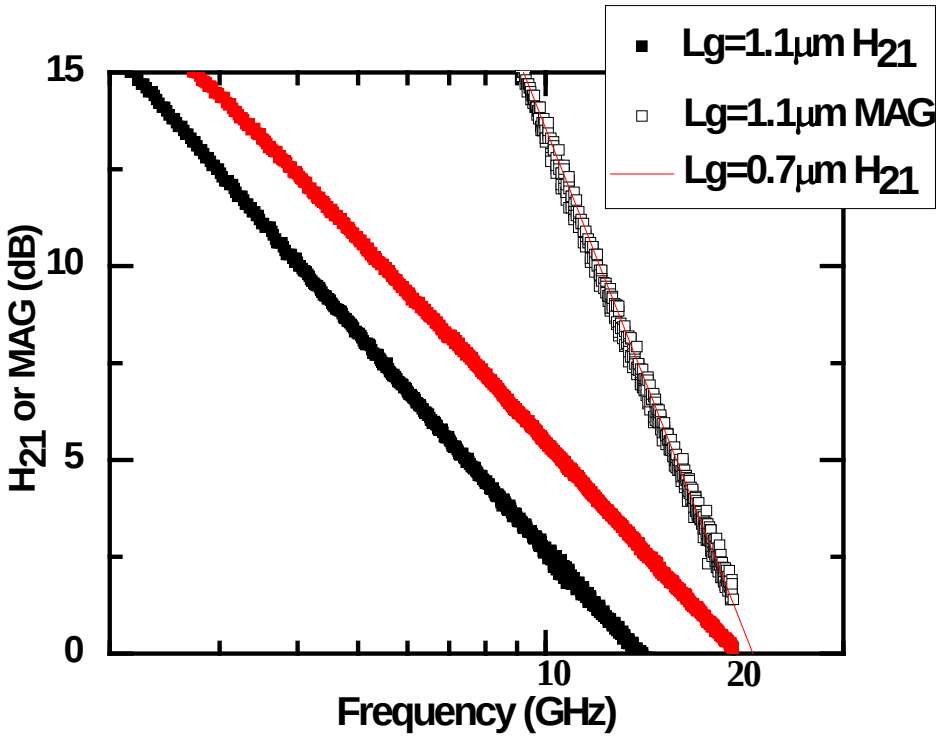


Figure 2.10 Unity current gain (solid black symbols for 1.1μm device and open black symbols for 0.7 μm device) and the maximum available gain (solid red symbols for 1.1um device) for an InAlN/AlN/GaN HFET fabricated on a bulk semi-insulating GaN:Fe substrates.

Recently several results about InAlN/GaN HFETs with high cut-off frequency have been reported. Lee D. S. *et. al.* reported the cut-off frequency of 245GHz on the 30nm gate length InAlN/GaN HFETs [33]. Tirelli S. *et. al.* demonstrated the 30nm gate length InAlN/GaN HFETs with 210GHz cut-off frequency [34]. Compared with the other results, our HFETs show very high product (product of L_g*f_T). For our 1.1μm and 0.7μm devices, the products are 15.6 and 15.4.

2.7 Summary

In conclusion, high drain current density InAlN/GaN HFETs were successfully fabricated on Fe doped semi-insulating GaN substrates without the notorious buffer leakage or the need to dope the buffer layer with Fe with adverse effects. The nearly lattice matched InAlN/GaN heterostructure can provide a much higher 2DEG sheet density than the conventional AlGaN/GaN heterostructures. The lack of drain current degradation at high drain bias voltages in devices grown on bulk GaN substrates as compared to those on sapphire was attributed to the better thermal dissipation of bulk GaN and the better GaN buffer crystalline quality as a result of GaN homoepitaxy. By using ICP dry etching and *in situ* H_2 etching, the interface impurity contamination was efficiently reduced, which resulted in a lower GaN buffer leakage level on a GaN substrate than that reported for HFETs on sapphire and SiC substrates. The InAlN/GaN HFETs with 1.1μm and 0.7μm gate length show the decent RF performance. The product of L_g*f_T is higher than the other reported values.

Chapter 3 AlGaN/GaN Dual Channel HFETs and Hot Phonon Scattering

3.1 GaN based HFETs and Electron Velocity in 2DEG channel

From the discussion above we can know that the high frequency and high power of GaN based HFETs is always pursuit by the scientists. When it comes to the fundamental physics for improve GaN based HFETs, we need to carefully analyze the functions of each part in HFETs. The operation frequency of a HFET is inversely proportional to the total delay of the electrons across 2DEG channel (τ_{total}). As described in Moll's paper [35] in detail, the total delay (τ_{total}) can be divided into three different components: intrinsic delay ($\tau_{intrinsic}$), channel charging delay ($\tau_{channel}$), and drain delay (τ_{drain}). $\tau_{intrinsic}$ is the time taken by the electrons to cross the channel region under the gate, $\tau_{channel}$ is the time needed to charge and discharge the parasitic capacitances and τ_{drain} is the time required by the electrons to cross the depletion region induced at the drain side of the gate.

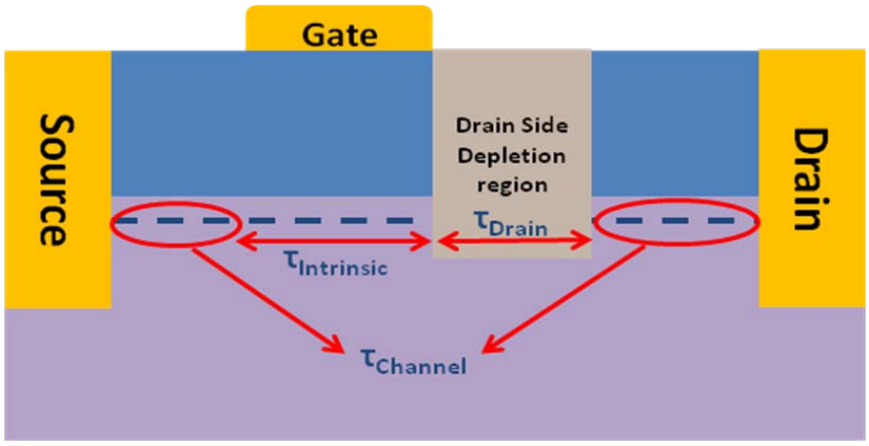


Figure 3.1 Schematic illustration of each delay factor, $\tau_{intrinsic}$, $\tau_{channel}$, and τ_{drain} in AlGaN/GaN HFET

Figure 3.1 show each delay component in a GaN based HFET. According to the analysis, the three kinds of delays should be minimized to improve the operation frequency of a HFET. The channel delay is related with the access region of HFET. In these regions, electrons operate at low electric field. The the velocity follows a simple relation, namely the product of the low field mobility, μ, and the applied electric field, F: $v = \mu F$. From this equation, we can see that the electron velocity is linearly proportional to the applied field. In order to increase the electron velocity and decrease the channel delay, electron mobility is the key factor and should be improved at first. For 2DEG channel underneath the gate, electrons operate under high electric field. At high electric field, the electron drift velocity is saturated. For the wurzite GaN system, the polar semiconductor, the electron kinetic energy approaches the optical phonon energy, $\hbar\omega_{LO}$, when the electron velocity is saturated. In this situation, the electrons tend to emit copious quantities of optical phonons. The emission and reabsorption of optical phonons constitute the dominant scattering mechanism at high fields and this scattering limits the mobility and subsequently the velocity of the carriers. From this point of view, the essential way to reduce the intrinsic delay and improve the operation frequency is to reduce the optical phonon scattering, especially LO (longitudinal optical) phonon scattering.

When it comes to the optical phonon scattering, it is necessary to introduce the definition of hot phonon in GaN 2DEG channel. The high electric field in HFET gives rise to a large amount of electrons with high energy, hot electrons. In the meantime, the hot electrons can generate large density of optical phonons in the 2DEG channel. Since the phonons are in not in equilibrium they are called as hot phonons. Hot phonons plays

a crucial role in GaN based HFET. At first hot phonon is the key factor hindering the increase of electron drift velocity. Secondly hot phonon is the bottleneck for the heat dissipation in 2DEG channel.

3.2 Hot Phonons and Heat Dissipation in GaN 2DEG channel

For GaN based HFET, the primary consideration to achieve the optimal performance is to remove the heat generated from devices working under high electric field. It is found that the acoustic phonon scattering related joule heat is the dominate mechanism for the heat dissipation at low electric field. The dissipation of energy (heat) of electrons in an FET channel is only limited by the removal of acoustic phonons through the heat sink. Therefore the thermal conductivity of substrates is very important and SiC substrate is popularly chosen as the substrate for GaN based HFETs. However for HFETs working under high electric field, the hot electrons accelerated by high electric field dissipate the chaotic energy (heat) mainly through interaction with LO phonons (hot phonons). The LO phonons, with very low group velocity, tend to remain in the channel, and their energy cannot be dissipated or removed from the channel unless they are converted to other modes with higher group velocities. The piled-up non-equilibrium LO phonons in 2DEG channel are called hot phonons.

The mechanism of heat dissipation in GaN 2DEG channel under high electric field is shown in Figure 3.2. As indicated, the interaction of hot electrons with hot phonons is very fast. The temperature of hot electrons and hot phonons is considered as the same. As well, the heat transferring from LA phonons to substrate is efficient. The only bottleneck of this process is the disintegration of LO phonons into LA phonons and the associated heat transferring. The key point is to reduce the time for this conversion. We

can treat this conversion in terms of hot phonon life time. Therefore it is very worthwhile to investigate the mechanism of LO→LA conversion process and optimized the heat dissipation efficiency.

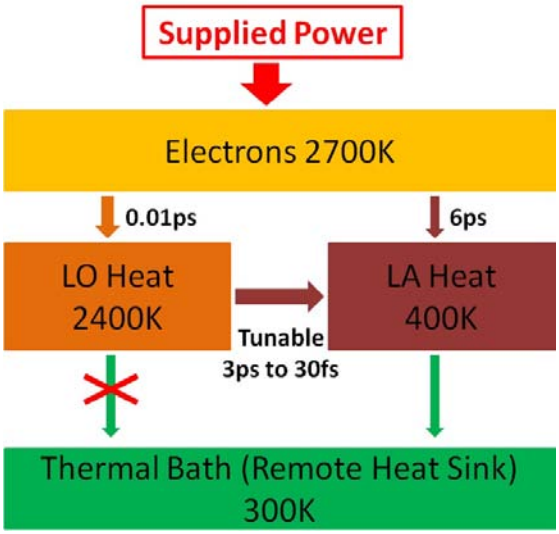


Figure 3.2 Schematic of the dissipation of heat in GaN at high fields. The only means of transferring energy out of the hot electron/hot phonon subsystem is through the hot phonon decay into acoustic modes.

The hot phonons are excited by hot electrons in 2DEG channel. The hot phonon life time is closely related with the 2DEG sheet density. Previously it has been indicated that LO phonons decay into transversely polarized LA mode phonons by the so-called Ridley mechanism: $LO \rightarrow TO+LA$ [36] [37]. This process is valid for the bare LO phonon in bulk GaN. But that is not true for hot phonons in 2DEG channel. Since the density of electrons is high in 2DEG channel, the interaction is no longer simple because of the coupling of coherent plasma oscillations with the LO phonons. The emission of coupled modes is so intense that the population of these "dressed" phonons greatly exceeds the equilibrium value, and the phonons are said to be hot. To what extent this happens depends crucially on the lifetime of the coupled mode. The decay mechanism is not as simple as the Ridley mechanism [38]. It is found that the decay of hot phonons in 2DEG channel can be

described as plasmon-phonon coupling. Here it is necessary to explain the origin of Plasmon. In physics, a plasmon is a quantum of plasma oscillation. The plasmon is a quasiparticle resulting from the quantization of plasma oscillations just as photons and phonons are quantizations of light and mechanical vibrations, respectively (though the photon is an elementary particle, not a quasiparticle). Thus, plasmons are collective oscillations of the free electron gas density, for example, at optical frequencies. Plasmons in GaN 2DEG channel is generated by the high density of 2DEG electron gas. That is to say, the decay of hot phonons in 2DEG is closely related with the interaction of hot electrons with hot phonons.

As discussed, it is important to monitor the hot phonon life time and enhance the hot phonon decay. So it is necessary to find a method to measure the hot phonon life time. The Raman scattering measurement is commonly used to study the LO phonon scattering in bulk GaN. Subpicosecond time-resolved Raman studies showed that the hot phonon lifetime decreased from about 2.5ps to 0.35ps as the carrier density increased from 10^{16} to 10^{19} cm^{-3} [39]

Estimating the "bulk" carrier density in an HFET channel simply by dividing the sheet density by the width of the triangular quantum well at the Fermi energy we see that such densities and even higher are readily attainable in the GaN channel of a HFET. However, this technique is not valid to investigate the hot phonons in 2DEG channel. Since the decay of hot phonon is described as plasmon-phonon coupling, the interaction can be screened or anti-screened depending on the wave vectors of hot phonons [40]. Raman scattering experiments examine optical phonons very near q=0, where q is the wave vector, in bulk material or when the carriers have been produced optically within,

typically, a micron. The group velocity of these long wavelength modes, when uncoupled at low densities, is negligible and, as a consequence, the migration of phonons out of the active region can be ignored. On the other hand, when the electrons are confined to the 2DEG channel, typically no more than 5 nm wide, migration of hot phonons out of the active area cannot be ignored since it will have the apparent effect of reducing the lifetime of hot phonons. Therefore it is hard to use Raman scattering method to monitor the decay mechanism of hot phonons. The best option for measuring the hot phonon lifetime is microwave noise technique [41].

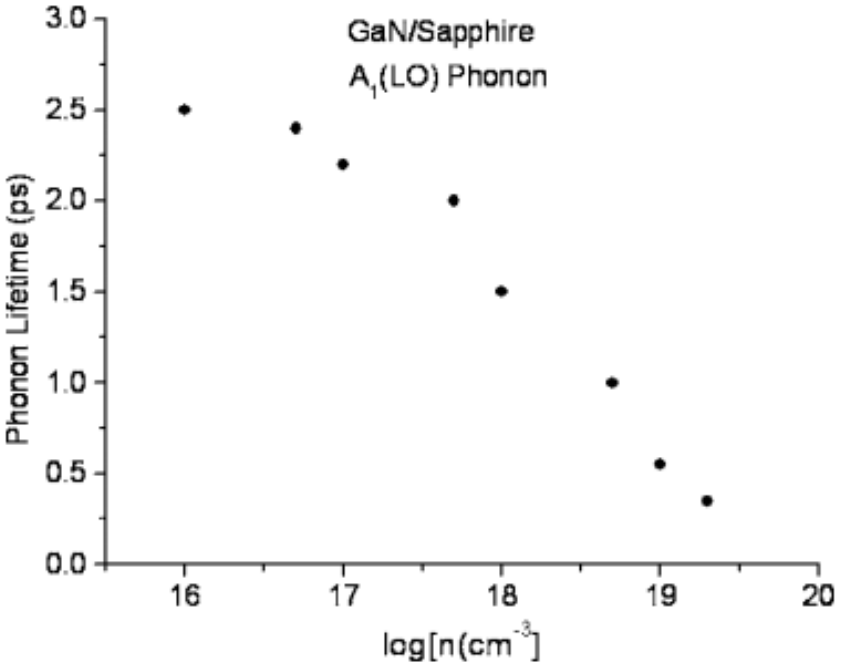


Figure 3.3 Hot phonon lifetime measured by time-resolved subpicosecond Raman spectroscopy.

3.3 Hot Phonon Lifetime Measurement

In the microwave noise technique, a sensitive radiometer is placed at the output of a pair of ohmic contacts. During the voltage pulse, the noise power (the noise arises due to current fluctuations in the channel) is measured and compared with that of a blackbody

which has a known temperature. When the two powers are equal, it is deduced that the electron noise temperature is equal to the temperature of the blackbody. Thus, the electron noise temperature can be measured. The measurement is performed at high frequency (10GHz) where the low frequency sources of noise such as 1/f noise and those associated with trapping can be neglected. If the confining barriers are high enough such that real space transfer of the electrons is suppressed (when an AlN spacer layer is employed), the noise can only be attributed to electron-phonon interactions. It is indicated that the electron noise temperature is just a couple percent higher than the electron temperature [42]. Armed with the electron temperature and knowing the power supplied to the channel, the energy relaxation time of the electrons can be estimated as

$$\tau_{energy} = k_B \frac{dT_e}{dP_{\sup}} \tag{3.1}$$

At low supply powers, electrons interact with acoustic phonons and energy relaxation times are very long. At high supply powers and high electric fields when electrons have sufficient energy to emit optical phonons, the LO phonon interaction dominates and relaxation time becomes nearly independent of the supplied power, which is coincided with the introduction above about the heat dissipation mechanism. Under high electric field, the bottleneck of heat dissipation is the decay of hot phonons, which is independent of the supplied powers. The experimental and simulated data is shown in Figure 3.4, as reported by Matulionis [43].

Once the electron temperature is measured, it is important to have the hot phonon temperature. It is found that hot phonon temperature is almost equal to electron temperature under the dominate electron-hot phonon scattering, as shown in Figure 3.5. Therefore the hot phonon temperature can be acquired from the microwave noise

measurement as well. Summarizing the conclusions related with electron noise temperature, electron temperature and hot phonon temperature, we can see that,

$$T_n \approx T_e \approx T_{ph} \tag{3.2}$$

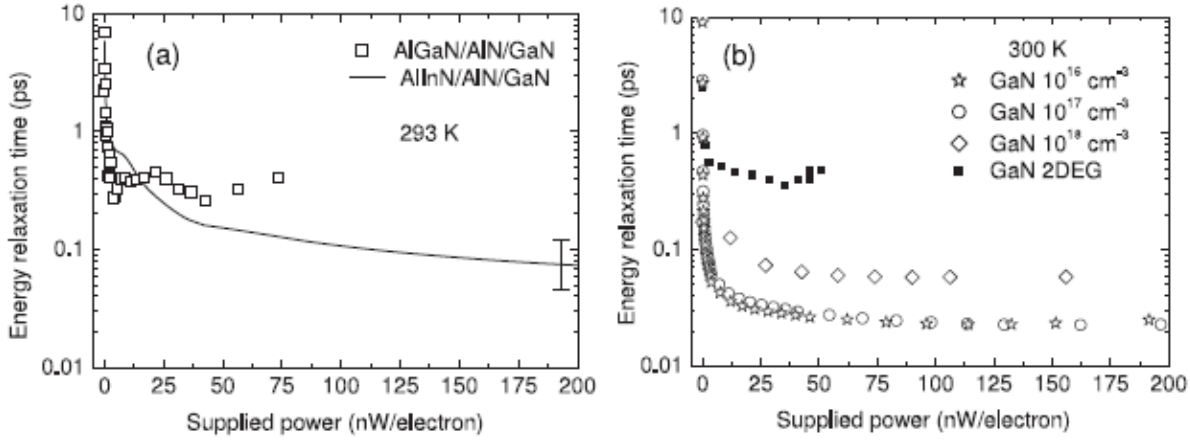


Figure 3.4 (Left) Experimental and (right) Monte Carlo simulation of energy relaxation time as a function of the supplied power to various GaN channels.

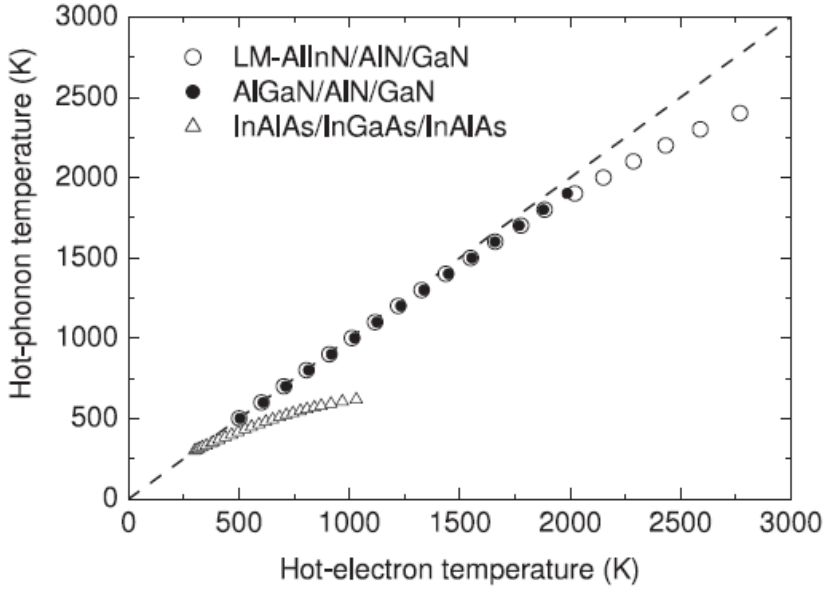


Figure 3.5 Hot electron temperature and hot phonon temperature. The dashed line represents hot phonon temperature equals hot electron temperature; it is clear that in GaN channels, the hot phonon and hot electron temperatures are nearly equal.

Finally the hot phonon lifetime can be estimated by fitting the curve of supplied power versus the inverse of electron noise temperature. As illustrated in Figure 3.6, the experimental results (symbols) are compared with the approximate fluctuation-dissipation relation for hot-electron scattering on hot phonons (solid curves) that contains only two fitting parameters: the LO-phonon energy $\hbar\omega_{ph}$ and the effective LO-phonon lifetime τ_{ph}^{*}:

$$P_d = \frac{\hbar\omega_{ph}}{\tau_{ph}^{*}}\left(\left[\exp\frac{\hbar\omega_{ph}}{k_B T_n}-1\right]^{-1}-\left[\exp\frac{\hbar\omega_{ph}}{k_B T_0}-1\right]^{-1}\right) \tag{3.3}$$

where T_0 is the ambient temperature, and k_B is the Boltzmann constant [44]. As we know the LO-phonon energy of GaN is 92meV. By fitting the curve, the effective hot phonon life time can be estimated. For 2DEG with high sheet density, the effective hot phonon life time is considered as the same with hot phonon life time.

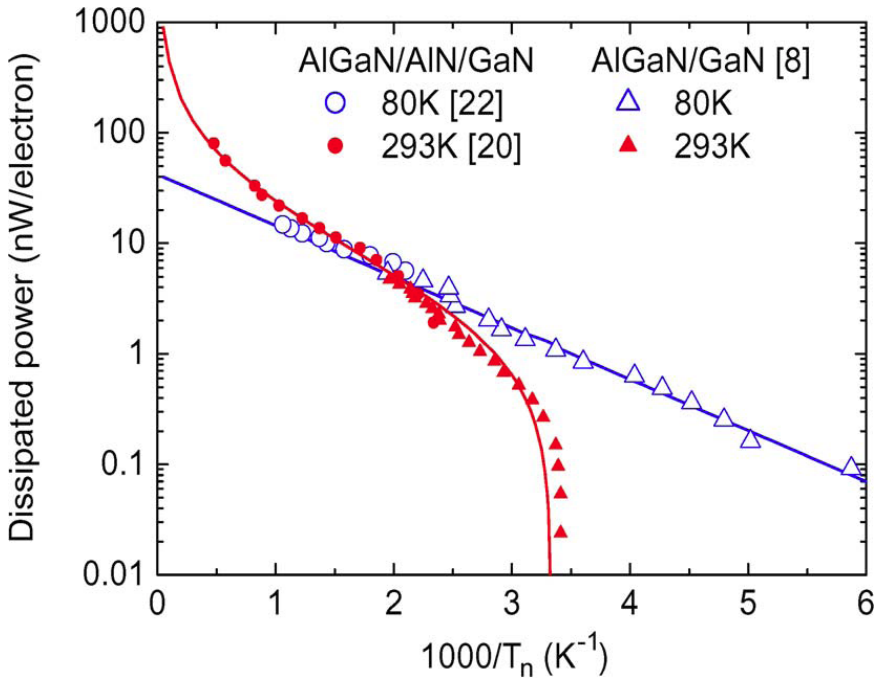


Figure 3.6 Dissipated power per electron against inverse noise temperature. Experimental data at 80K (blue open symbols) and at 293K (red closed symbols) for Al0.15Ga0.85N/GaN (triangles, 5×10^{12}cm^{-2}) and $Al_{0.33}Ga_{0.67}N$/AlN/GaN (circles, 1×10^{13} cm^{-2}).

As introduced above, the decay of hot phonons in GaN 2DEG channel is related with the coupling of LO phonons with plasmons. Figure 3.7 shows the dispersion curves for phonons and plasmons [45].

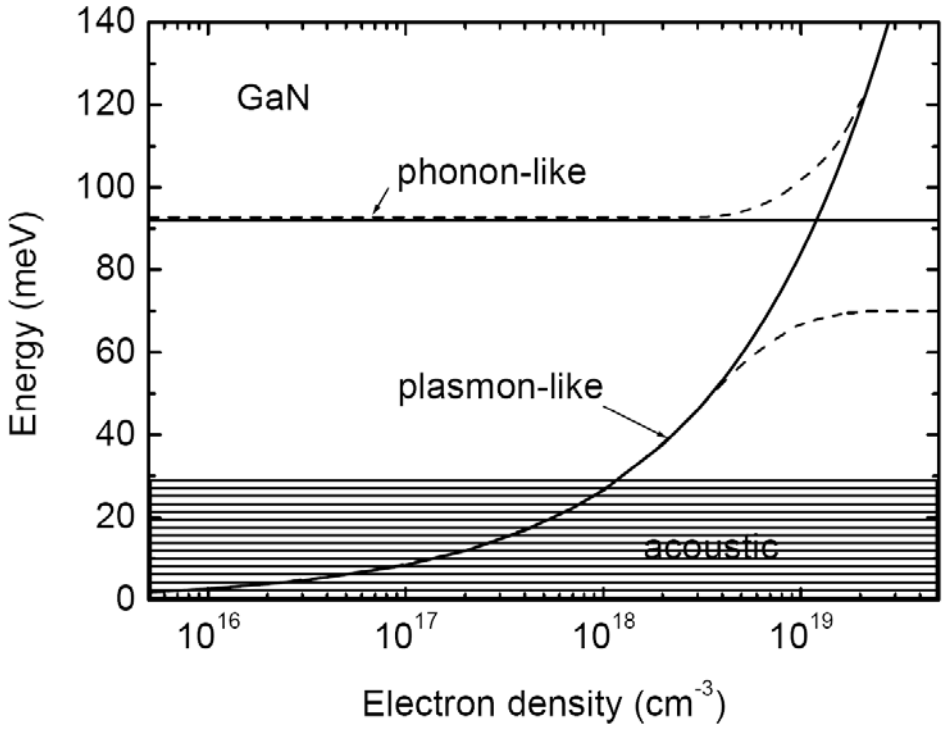


Figure 3.7 Dispersion of phonons and plasmons on electron density for bulk GaN. The solid lines neglect the coupling while the dashed lines include coupling.

From the dispersion curves we can see that phonon and plasmon couples at a certain electron density, around $10^{19}cm^{-3}$. This indicates the relation of phonon-plasmon coupling with the bulk electron density in GaN. Employing the microwave noise measurement technique to measure the hot phonon lifetime for various GaN based 2DEG channel with different sheet densities, the nonmonotonic dependence of hot phonon lifetime on the 2DEG sheet density is discovered. It is shown that there is a minimum phonon lifetime corresponding to a certain sheet density for both the GaAs and GaN system. The only difference is that the accordingly optimal sheet density for GaAs is lower than that for GaN [46]. According to the theory on phonon-plasmon coupling, this difference can be

explained by the lower LO phonon energy in GaAs. At room temperature the LO energy for GaAs is 36.1meV, and that for GaN is 92meV. The data in detail is shown in Figure 3.8.

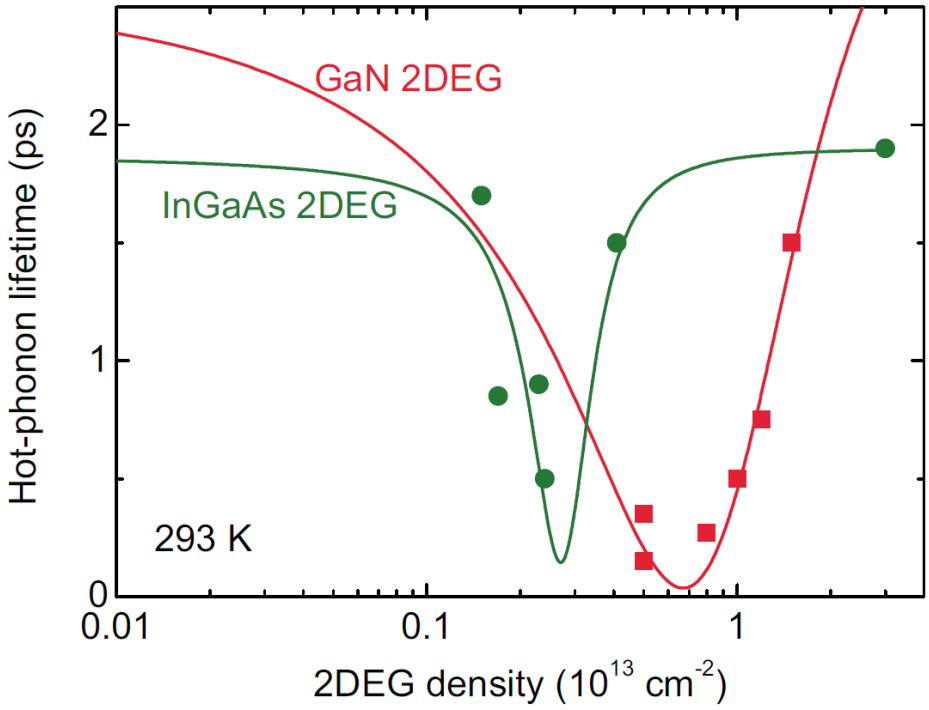


Figure 3.8 Hot-phonon lifetime for GaN-based channels (red points and curve) and hot-electron energy relaxation time for InGaAs 2DEG channels (green points and curve).

3.4 Resonance 2DEG Sheet Density and Tuning of Hot Phonon Lifetime

From the discussion above about the dependence of LO phonon lifetime on 2DEG density, we can see that there is an optimal sheet density where the LO phonon-plasmon coupling takes place and the LO phonon lifetime is the minimum. This means that for electron densities greater than or less than the density at phonon-plasmon coupling, the hot phonon lifetime increases which bodes poorly in terms of performance and reliability. Therefore, optimal performance will be achieved only when the optimal density of

carriers in the channel of the HFET is reached. From the further study, it is demonstrated that the optimal sheet density is not a fixed value. Matulionis *et al*. successfully pushed the optimal sheet density to the higher values by changing the supplied power to GaN 2DEG channel by using the un-gated TLM structure samples (simple ohmic contacts on an etched mesa that are separated by a distance ~5-10μm) [47]. The minimum hot phonon lifetime of ~30fs was measured at a power of ~20nW/electron, which is the lowest observed hot phonon lifetime in a GaN 2DEG channel. Based on the experimental data shown in Figure 3.9, the relation of resonance sheet density with hot phonon lifetime is fitted as

$$\tau_{LO} = a\left\{1+\frac{b}{\left(\sqrt{n}-\sqrt{n_{res}}\right)^2+c}\right\}^{-1} \tag{3.4}$$

where n is the 2DEG density, n_{res} is the 2DEG density at the phonon-plasmon resonance, and a, b, and c are fitting parameters which control the value of the lifetime far from resonance, the "sharpness" of the resonance curve, and the value of the minimum lifetime.

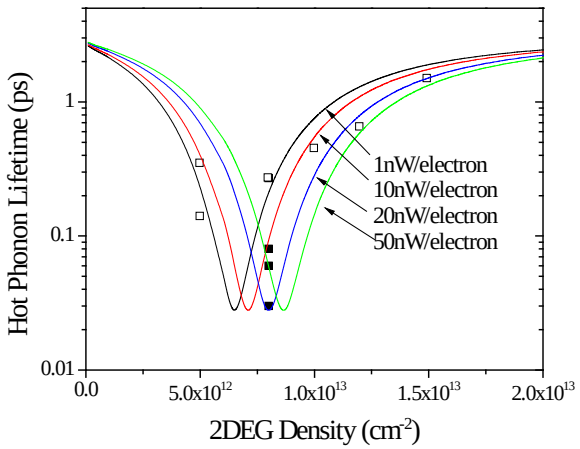


Figure 3.9 Fitted phonon-plasmon resonance curves after Equation (3.4) (solid lines) for measured phonon lifetimes with various supply powers

In addition to the un-gated TLM microwave noise measurement, the resonance phenomenon is also observed in the real GaN based HFEs. As we know, the hot phonon lifetime indicates the decay of hot phonons. With lower hot phonon lifetime in GaN 2DEG channel, the electron-hot phonon scattering is reduced as well. Therefore the electron velocity is enhanced. By checking the variations of the intrinsic delay of GaN based HFETs, that is, the electron velocity underneath the gate area, under different gate bias, the changing of hot phonon lifetime with sheet density is observed. J. H. Leach *et al.* [48] found that there exists a minimum intrinsic transit time delay and equivalently the maximum electron velocity at a particular 2DEG sheet density for InAlN/GaN HFETs, as shown in Figure 3.10.

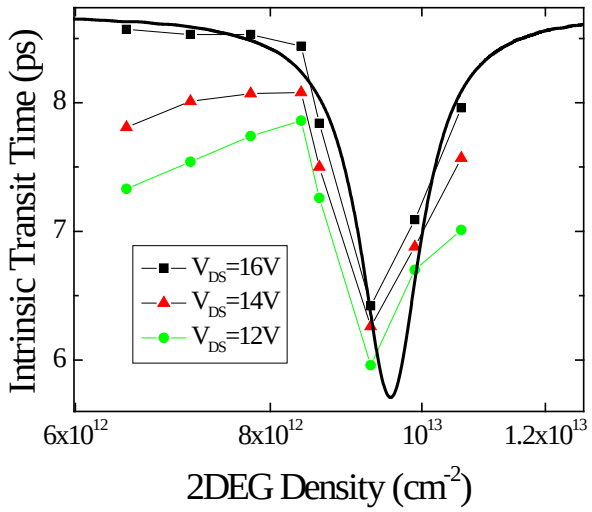


Figure 3.10 Intrinsic transit time as a function of the 2DEG density for three drain biases as well as the best fit using an optimal electron density of 9.5 x 10^{12} cm^{-2} (heavy solid black line). The 2DEG density corresponding to the minimum in the intrinsic transit time is consistent with that corresponding to the minimum in the hot phonon lifetime.

The optimal sheet density value is 9.5×10^{12} cm^{-2} which is a little bit higher than 6.5×10^{12} cm^{-2} as shown in Figure 3.8, since the applied power causes the minimum hot phonon

lifetime shifts. The supplied power versus hot phonon lifetime is consistent with the theoretical values shown in Figure 3.9

Based on the fundamental relations of hot phonon lifetime with the 2DEG sheet density and our previous experimental data, we can propose an idea that if we can tune the 2DEG sheet density of the HFETs and make HFETs operate at the optimal sheet density, the high frequency performance and heat dissipation of GaN HFETs can be significantly enhanced. As we discussed the introduction chapter, in order to increase the power of GaN-based HFETs, AlInN/AlN/GaN structure were introduced to replace the conventional AlGaN/GaN HFETs, for the reason that the AlInN/AlN/GaN heterostructure can generate much higher sheet density than the AlGaN/AlN/GaN structure and thus deliver more power. However, with the 2DEG sheet density increased, the hot phonon lifetime would be increased as well because the 2DEG sheet density is far from the plasmon-phonon resonance point. As indicated in Figure 3.7, the plasmon-phonon coupling point corresponds to the bulk electron density of $10^{19}cm^{-3}$. In GaN 2DEG channel, it is also proofed that there is a sheet density corresponding to the minimum hot phonon lifetime, that is, the plasmon-phonon coupling point. As discussed above, the most important parameter related with hot phonon lifetime is the sheet density in the 2DEG channel. With the conventional single heterostructures, each 2DEG corresponds to a certain electron concentration distribution. As shown in Figure 3.11, the electron concentration distributes with big variations in the 2DEG channel for InAlN/GaN heterostructure. The peak concentration is even more than $1.0\times10^{20}cm^{-3}$. That means most of electrons are not distributed in the optimal electron concentration area, where the plasmon-phonon coupling happens. However if we spread out the

electrons in a wider 2DEG channel and reduce the peak electron concentration without decrease the total 2DEG sheet density, we can tune the GaN-based HFETs to operate at the optimal condition without degrading the power performance. According to this expectation, we propose the double channel HFET structures.

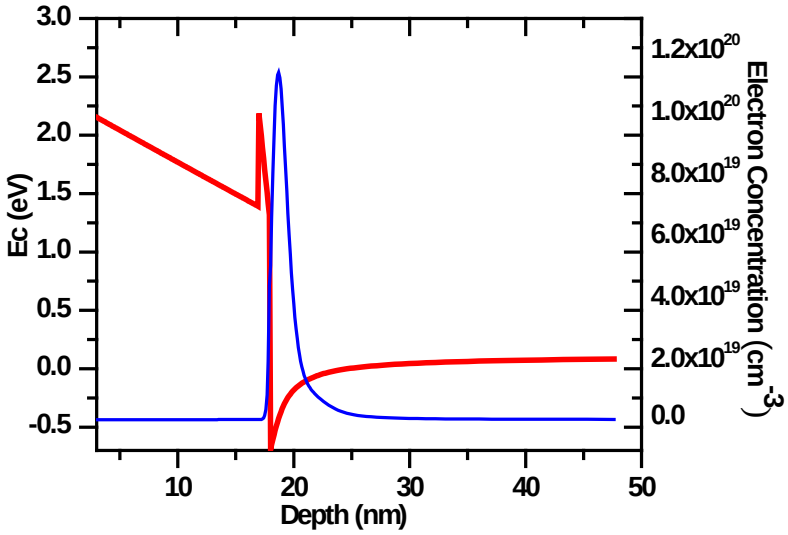


Figure 3.11 Conduction band diagram and electron concentration distribution in InAlN/AlN/GaN heterostructure.

3.5 Simulation and Optimization of the structures of AlGaN/GaN Dual Channel HFETs

As discussed above, we proposed to insert an extra channel between AlN spacer and GaN buffer layer, so that 2DEG channel becomes wider than the conventional 2DEG channel. In this case, the electron peak concentration would be reduced and more electrons would distribute near the optimal electron concentration point, $10^{19}cm^{-3}$. Therefore the electron-hot phonon scattering can be relieved by plasmon-phonon coupling and electron velocity can be enhanced. In this structure, we use AlGaN as the extra channel layer. The structure of dual channel HFET is show in Figure 3.12. Compared with the conventional GaN based HFET structure, there is an extra AlGaN

layer between AlN spacer and GaN buffer layer. The AlGaN channel will share 2DEG with GaN channel and spread out the electrons in a wider 2DEG channel.

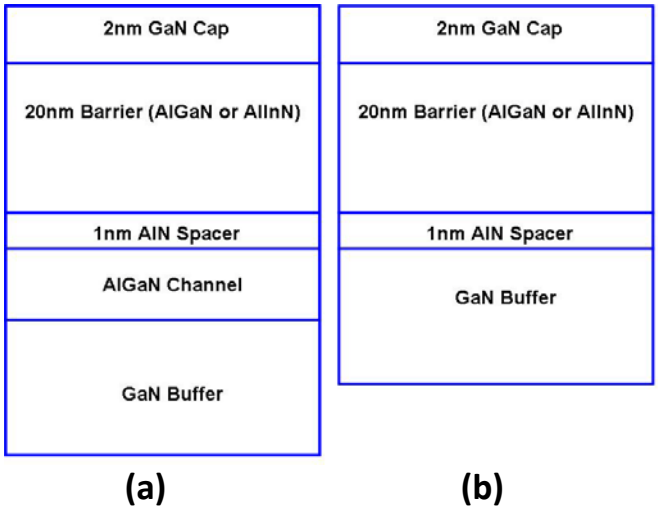


Figure 3.12 (a) The proposed AlGaN/GaN dual channel Heterostructure (b) conventional GaN-based Heterostructure

By using the TCAD simulation tool, the AlGaN channel thickness and Al composition is optimized firstly to maximize the electron spread-out in the dual channel. At first the Al composition of AlGaN channel layer is optimized. As shown in Figure 3.13, with the Al composition decreased, the electron concentration spread out more obviously. The AlGaN channels with 5% and 10% Al composition show the same level of peak electron concentration. In our experiment, the AlGaN channel with 10% Al composition is employed as the extra channel layer. Secondly the thickness of AlGaN channel layer is optimized. As shown in Figure 3.14, with the AlGaN channel thickness increased from 3nm to 5nm, the electrons spread out more into the AlGaN channel and the peak electron concentration decreases significantly. However, for the cases with 3 and 4nm AlGaN channel thickness, the electron concentration curves split into two separate peaks, which

means the two separate and parallel channels form. In addition, more electrons locate in the AlGaN channel layer other than the GaN channel layer. As we know, the alloy scattering would be introduced with AlGaN layer. If more electrons distribute in the AlGaN channel layer, the alloy scattering would degrade the electron mobility and increase the access resistance in the low field regions of HFET (the regions on the edges of source and drain) where channel resistance is dependent on the low field mobility.

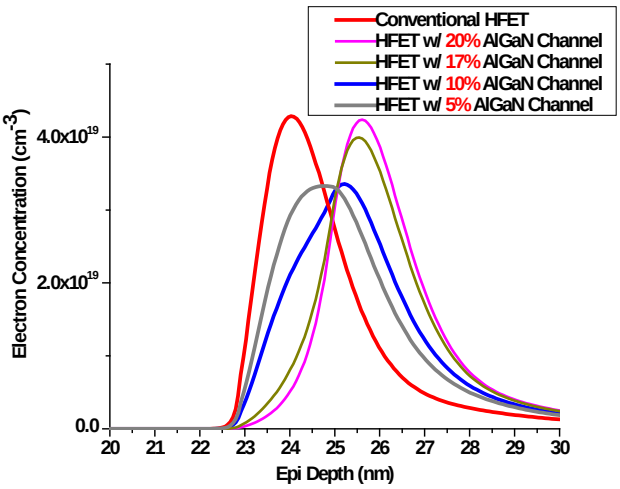


Figure 3.13 Electron concentration distributions for the AlGaN/GaN structure with AlGaN channel. (a) 2nm $Al_{0.2}GaN_{0.8}N$ (b) 2nm $Al_{0.17}GaN_{0.85}N$ (c) 2nm $Al_{0.1}GaN_{0.9}N$

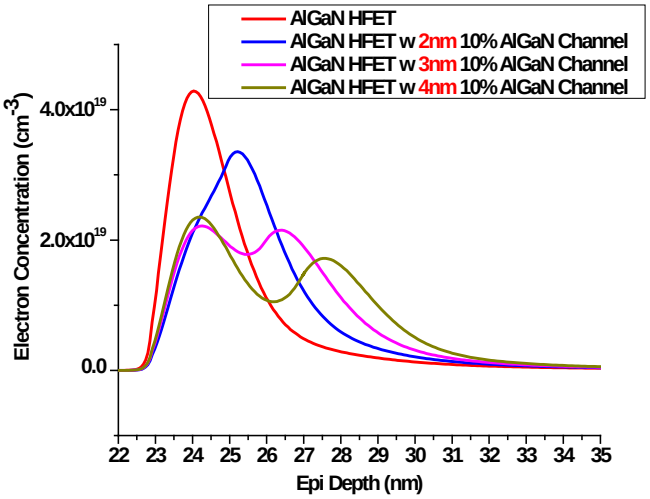


Figure 3.14 Electron concentration distributions for the AlGaN/GaN structure with AlGaN channel. (a) 2nm $Al_{0.1}GaN_{0.9}N$ (b) 3nm $Al_{0.1}GaN_{0.9}N$ (c) 4nm $Al_{0.1}GaN_{0.9}N$

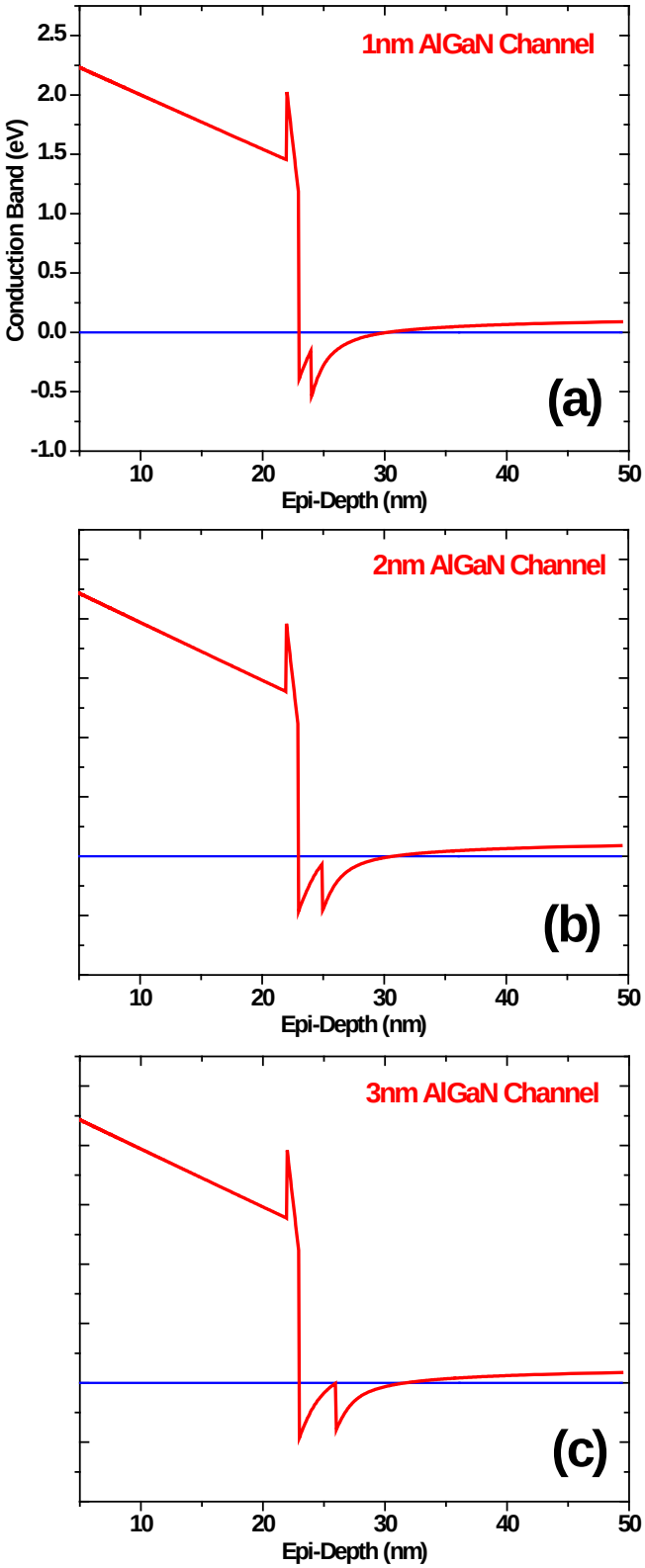


Figure 3.15 Conduction band diagrams for the AlGaN/GaN dual channel HFETs with 20 nm $In_{0.154}Al_{0.846}N$ barrier layer (a) 1nm $Al_{0.1}Ga_{0.9}N$ channel layer, (b) 2nm $Al_{0.1}Ga_{0.9}N$ channel layer, (c) 3nm $Al_{0.1}Ga_{0.9}N$ channel layer

According to the analysis above, the 2nm $Al_{0.1}Ga_{0.9}N$ channel layer is the best option for the AlGaN/GaN dual channel HFET structure. We applied this design into the InAlN barrier HFET structure and simulated it again. As we discussed before, the lattice match condition for InAlN barrier layer on GaN is 15.4% In composition. So in the simulation we used 20nm $In_{0.154}Al_{0.846}N$ as the barrier layer. From the electron concentration distribution shown in Figure 3.16, we can clearly see that the HFET structure with 2nm $Al_{0.1}Ga_{0.9}N$ channel shows obvious peak electron concentration reduction. In addition, there is no separate electron peaks and the electrons dominantly locate in the GaN channel layer. Figure 3.15 shows the conduction band diagrams for the dual channel HFETs with different AlGaN channel thickness. From the conduction band diagrams we can confirm the electron distribution shown in Figure 3.16. For 1nm AlGaN channel structure, the AlGaN channel area under the Fermi level is less than the GaN one. While for 3nm AlGaN channel structure, the case is opposite. Only for the case with 2nm AlGaN channel show the electrons almost equally distribute in AlGaN and GaN layers.

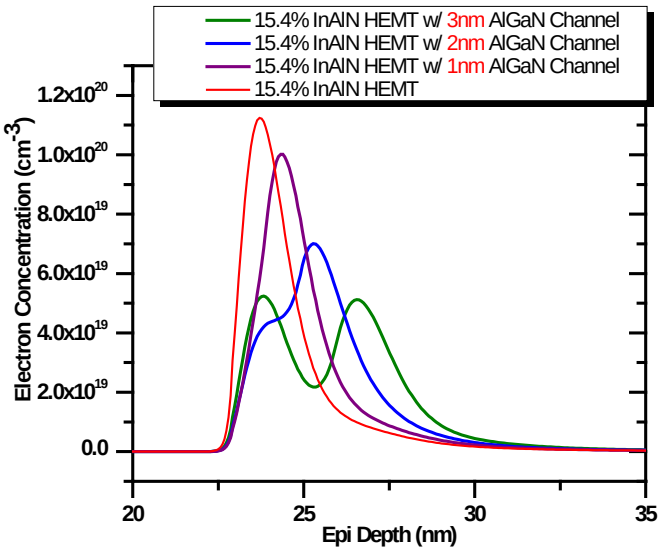


Figure 3.16 Electron concentration distributions for the $In_{0.154}Al_{0.846}N$/GaN structure with AlGaN channel. (a) 2nm $Al_{0.1}GaN_{0.9}N$ (b) 3nm $Al_{0.1}GaN_{0.9}N$ (c) 4nm $Al_{0.1}GaN_{0.9}N$

3.6 Growth, Fabrication and characterization of AlGaN/GaN Dual Channel HFETs

Based on the simulation and analysis above, the AlGaN/GaN dual channel structure with AlGaN barrier is used for our experiments. The structure in detail is shown in Figure 3.17. For comparison we grew a control AlGaN/GaN HFET with the same growth parameters except no AlGaN channel layer.

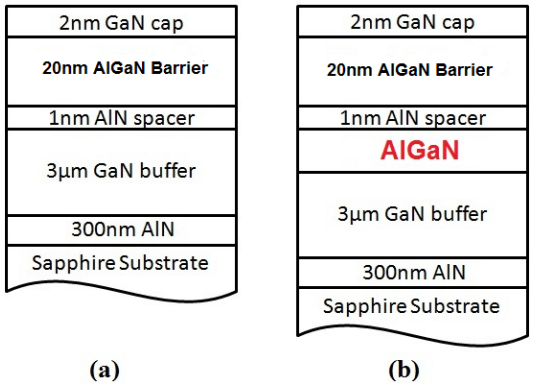


Figure 3.17 The diagram of conventional AlGaN/AlN/GaN (a) and novel AlGaN/AlN/$Al_{0.1}Ga_{0.9}N$/GaN (b) structures

In terms of MOCVD growth, AlGaN dual channel HFET and AlGaN control HFET structures were grown on 2 inch (001) sapphire substrates by a low-pressure custom-designed organometallic vapor phase epitaxy (OMVPE) system. Trimethylgallium, trimethylaluminum, trimethylindium, and ammonia were used as the Ga, Al, In, and N sources, respectively. For the AlGaN dual channel structure, a 3 μm undoped GaN was deposited at a temperature of 1000°C at 200 Torr after the 300nm AlN nucleation layer growth at 1030°C with a chamber pressure of 30Torr. This was followed by the growth of 3nm $Al_{0.1}Ga_{0.9}N$ layer, 1nm thick AlN spacer layer, and 20nm thick AlGaN barrier. For comparison, the AlGaN control HFET sample (AlGaN/AlN/GaN structure) is

different in that there is no AlGaN channel layer. The Al composition of AlGaN barrier layer is 25% for both samples. The growth was terminated with a 2nm thick undoped GaN cap layer. A metal stack of Ti/Al/Ni/Au (30/100/40/50nm) was deposited on both samples by e-beam evaporation and then annealed at 800 °C for 60 s for Ohmic contacts. Finally, after mesa isolation by etching 150 nm of the epilayer in the SAMCO ICP system using a Cl_2-based chemistry, the gate metal Pt/Au (30/50nm) was deposited.

In order to investigate the device characteristics, the DC current-voltage (I-V) measurements were performed on the AlGaN control HFETs as well as the AlGaN/GaN dual channel HFETs as shown in Figure 3.18. All the HFETs under discussion have a 1.1µm gate length with 90µm gate width and 4µm source-drain separation. It can be noted that the saturation current density (0.61A/mm) for the AlGaN/GaN dual channel HFET is comparable with the control HFET sample (0.60A/mm). The pinch-off voltage for AlGaN/GaN dual channel HFET is slightly higher than that for AlGaN control HFET because of the extra AlGaN layer and wider 2DEG channel. From the transfer characteristics shown in Figure 3.19, it can be seen that the extra AlGaN channel layer reduces the extrinsic transconductance slightly.

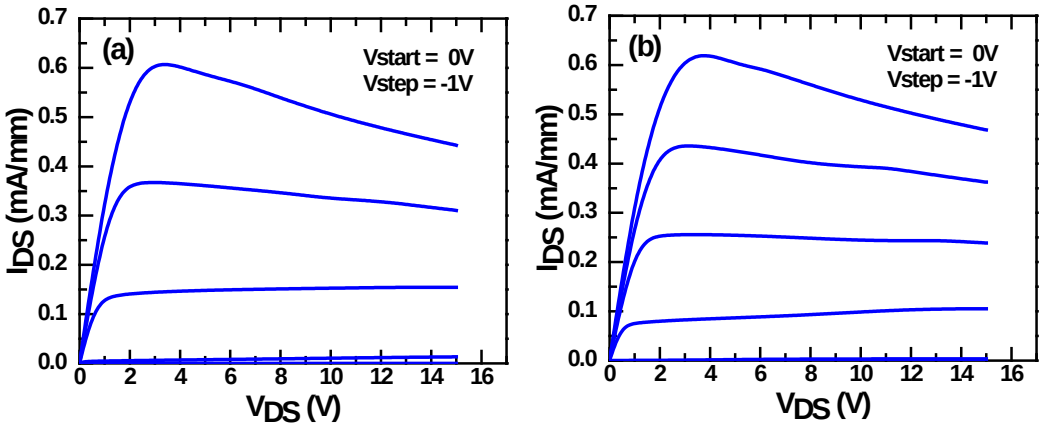


Figure 3.18 I-V characteristics of (a) AlGaN control HFET and (b) AlGaN/GaN dual channel HFET on sapphire substrate. The gate voltage was varied from 0 V to -3 V with 1V step for both HFETs. The pinch-off voltage is -4.0V and -3.2V for the AlGaN/GaN dual channel and control HFETs respectively.

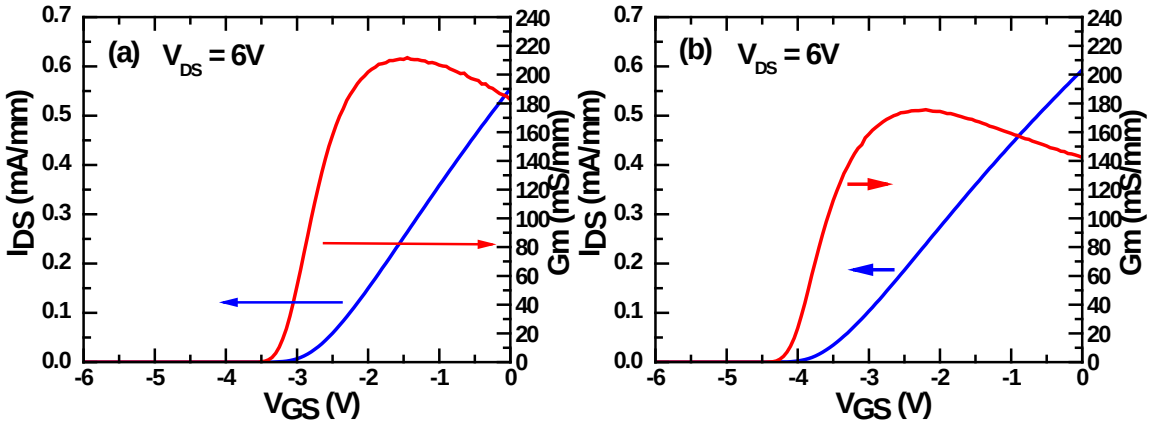


Figure 3.19 Transfer characteristics of (a) AlGaN control HFET and (b) AlGaN/GaN dual channel HFET on sapphire substrate. The applied drain voltage is 6V for both HFETs. The maximum transconductrance for AlGaN control HFET and AlGaN/GaN dual channel HFET are 210mS/mm and 174mS/mm respectively.

From the simulation, we know that the AlGaN/GaN dual channel HFET should have the wider 2DEG channel but the same 2DEG sheet density compared with the AlGaN control HFET. To verify the simulation results, the capacitance-voltage (C-V) measurement is employed to plot electron 3D density profile as a function of the depth into the epi-structure. The electron density peak of AlGaN/GaN dual channel HFET shifts about 3nm compared with AlGaN control HFET. The electron density profile spreads out obviously and the electron peak is lower for AlGaN/GaN dual channel HFET as shown in Figure 3.20.

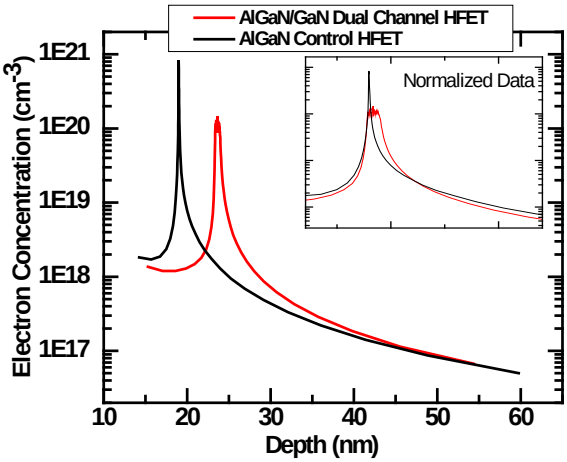


Figure 3.20 Electron concentration versus depth profile derived from the C-V data measured from the Schottky diode next to the HFET patterns. The red and black curves represent the AlGaN/GaN dual channel and AlGaN control HFETs respectively. In the inserted figure, the curves are zoomed out and the depth is normalized for a clear comparison.

On-wafer microwave measurements were carried out using the HP1850B vector network analyzer over a range of 2 to 20GHz. The S-parameters under different DC bias conditions were collected to calculate the small signal current gain, h_{21} and cut-off frequency. The maximum cut-off frequency for the AlGaN/GaN dual channel HFET is 9.0GHz, associated with the bias condition of V_{DS} = 20V and V_{GS} =-1.75V. Especially with the drain bias increased, it is not seen the cut-off frequency decrease in the measured drain bias range which indicates the high power operation capability of the AlGaN/GaN dual channel HFET. In comparison, that for AlGaN control HFET is 5.8GHz under the bias condition of V_{DS} = 6V and V_{GS} =-2V, as shown in Figure 3.21.

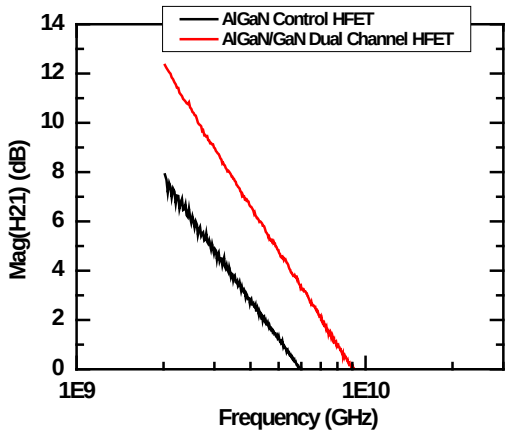


Figure 3.21 Unity current gain cut-off frequencies for the the AlGaN/GaN dual channel (red) and control HFET (black). The cut-off frequency f_T = 9.0GHz at bias of V_D =20V and V_G=-1.75V for the AlGaN/GaN dual channel HFET and f_T = 5.8GHz at bias of V_D =6V and V_G=-2.0V for AlGaN control HFET.

In order to verify the electrons transport in two channels for the AlGaN/GaN duall channel HFET, the channel transit time delay analysis is performed on both the AlGaN control HFET and AlGaN/GaN dual channel HFET, following Moll's method [49]. In Figure 3.22 the total transit time delays ($\tau = 1/2\pi f_T$) for both AlGaN/GaN dual channel

HFET and AlGaN control HFET are plotted in terms of the inverse of the drain current ($1/I_{DS}$) at different gate bias with the drain voltage fixed at 6V.

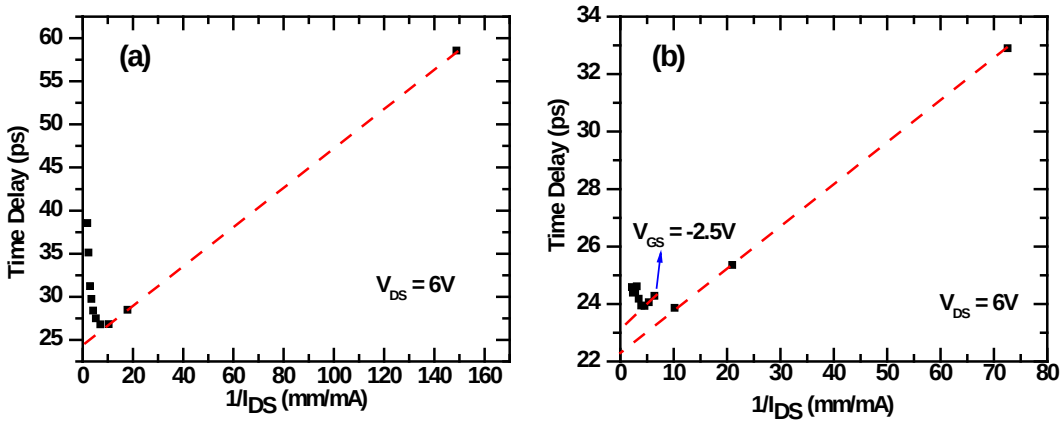


Figure 3.22 Extraction of channel charging delay for AlGaN control HFET (a) and AlGaN/GaN dual channel HFET (b)

The linear fitting of the total time delay for the AlGaN/GaN dual channel HFET indicates the two channel conduction mode. As the gate voltage greater than -2.5V, only the GaN channel is turned on. With the gate voltage less than -2.5V, both AlGaN channel and GaN channel are turned on. As compared, the AlGaN control HFET shows only one linear region. Therefore it can be confirmed that the AlGaN/GaN dual channel HFET does exist two channel conduction modes and with the gate voltage modulation, the AlGaN channel can be turned off at the alleviated gate bias.

The cut-off frequency variations with the drain bias and gate bias for AlGaN control HFET and AlGaN/GaN dual channel HFET is plotted in Figure 8. The gate bias V_{GS} for both of them is -2V. As can be seen in Figure 3.23(a), the cut-off frequency for AlGaN control HFET reaches the maximum (at V_{DS} = 6V) close to the knee voltage and then decrease continuously. With the drain bias increased to 14V, the cut-off frequency starts to increase again marginally. As compared, the cut-off frequency increases continuously with the drain bias. For the cut-off frequency variations with the gate bias, it can be seen

that the AlGaN/GaN dual channel HFET shows the higher peak cut-off frequency. In addition the cut-off frequency swing with the gate voltage is obviously smaller, which indicates the much better linearity.

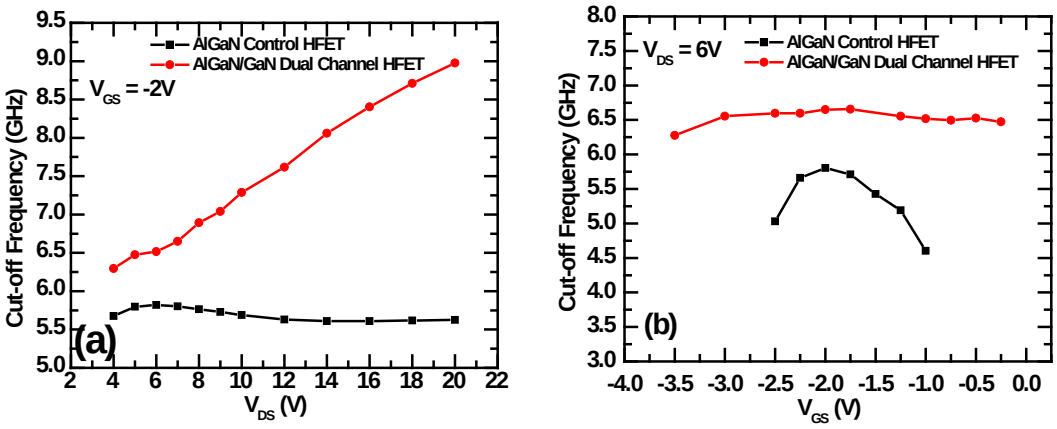


Figure 3.23 The Unity current gain cut-off frequencie variations with the drain bias (a) and gate bias (b) for the the AlGaN/GaN dual channel (red) and control HFET (black).

3.7 Small Signal Extractions for AlGaN/GaN Dual Channel HFETs

From the transit time analysis, it can be seen that the AlGaN/GaN dual channel HFETs show higher electron velocity with higher operation 2DEG density. To understand the dual channel HFET and predict the performance in the various conditions, it is necessary to analyze the equivalent circuit parameters by using the small signal extractions. In this section, the method for small signal extraction will be discussed and the equivalent circuit parameters of AlGaN/GaN dual channel HFETs are compared with those for the conventional HFETs.

When it comes to the mechanism of small signal extract in transistors, we should introduce the operation of signal amplification in transistor. The transistor is first properly DC biased so that the device is working at a quiescent point (Q-point) at which the V_{DS} determines the saturated output current, and V_{GS} is well away from the pinch off

value that determines the depletion width and channel resistances. If the input signal is small, then it will not affect the Q-point of the device. A small input voltage will produce approximately a linear response in the drain-source current. Or the equivalent circuit has linear response in the frequency domain without higher orders of harmonics. The output of the device has same frequency components as the input signal, only the phase and amplitude of the signal might be different.

Standard small signal extraction methods [50] [51] have been well-established for GaAs HFETs or SiC MESFETs. Basically, the equivalent circuit can be divided into the intrinsic part, for which the values are a function of bias, and the extrinsic part that has no dependence on bias conditions. Usually each element is obtained by fitting the scattering parameters measured directly from the device. The determination of the equivalent circuit always requires accurate S-parameter measurements, so that the extracted values can have physical significance. The general extraction procedures include two steps. The first step of the extraction is "Cold-FET" measurement to extract the extrinsic parameters such as parasitic resistances, inductances and capacitances. In the "Cold-FET" measurement, the FET channel is pinched off (V_{DS} = 0V, $V_{GS} \leq 0$). Under such a condition, the equivalent circuits can be simplified and the extrinsic parts can be extracted easy. The second step is extracting the intrinsic parameters. After the extrinsic parameters obtained, they are excluded from the equivalent circuits. The intrinsic parameters can be calculated from the s-parameters with extrinsic parts excluded.

At the beginning of the extraction, the equivalent circuit for our GaN based HFETs should be determined. The circuit model for GaN HFETs is usually more complicated than traditional FETs in order to account for behavior somewhat unique to GaN such as

the gate leakage current, self-heating, or defect-induced dispersion effects [52] [53] [54] [55] [56] [57] [58] [59]. In our extraction, the equivalent circuit for GaN based HFETs with 15 elements is chosen, as shown in Figure 3.24.

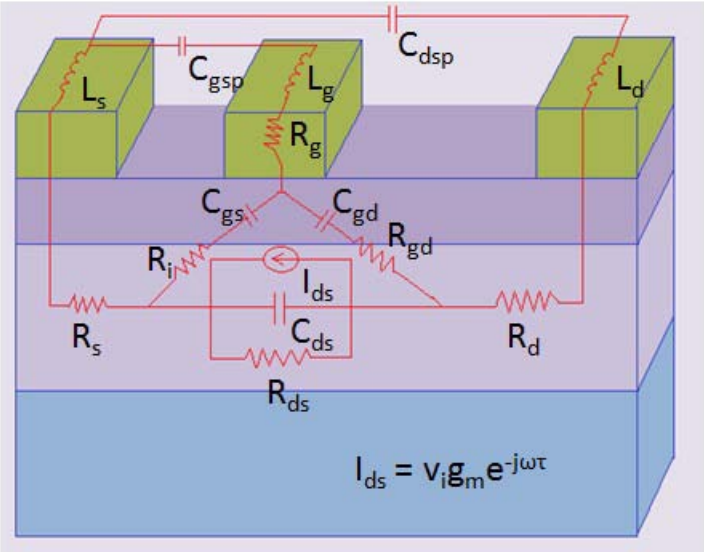


Figure 3.24 The schematic of the cross section and the physical origins of the small-signal equivalent circuit for a GaN based HFET

In this equivalent circuit, the C_{gsp}, C_{dsp}, L_s, L_g, L_d, R_s, R_d and R_g are the extrinsic parts. C_{gsp} and C_{dsp} are the gate-to-source and drain-to-source pad capacitance. L_s, L_g and L_d are the source, gate and drain inductance. R_s, R_d and R_g are the source, gate and drain resistance. The rest parts are belonged to the intrinsic circuit. C_{gs} and C_{ds} are the capacitances between the gate and source side of the channel and that between the gate and the drain side of the channel respectively. R_i is the channel charging resistance and it is included to account for the time delay of the charge at the source side of the channel in response to the gate signal. Its physical origin is complex and some people treat it as the physical resistance of the input part of the channel [60]. Similar to R_i, R_{gd} is the gate-drain charging resistance reflecting the time delay between the charge at the drain side of

the channel and the gate signal. g_m is the transconductance, and τ accounts for the time delay between the channel current and the gate voltage. C_{ds} is the channel capacitance between the drain and source. R_{ds} is the output resistance.

The first step is Cold-FET extraction. The pad capacitances can be extracted under a pinch-off cold-FET condition (V_{DS} = 0, V_{GS} << 0) at low frequencies (in the megahertz range) so that the influence of inductances can be minimized. Under the pinch-off bias conditions, the channel conductivity is negligible and the s-parameters measured exhibit capacitive properties. We assume the gate depletion region is symmetric toward source as well as drain. According to [61], the equivalent circuit complexity can be reduced as shown in the inset of Figure 3.25, if one considers only the imaginary part of the Y-parameters from which the capacitances are extracted. In the Figure, C_b is the total of the rest capacitances in HFETs. The extrinsic capacitances can be fitted as the equations (3.5), (3.6) and (3.7).

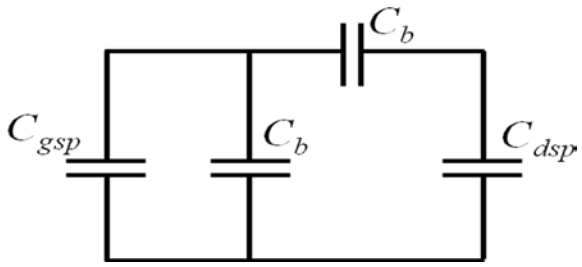


Figure 3.25 Reduced equivalent circuit for pinch-off Cold-FET condition, and the parasitic pad capacitances determined by linear regression at V_{DS} = 0V, V_{GS} = □8V.

$$\mathrm{Im}(\omega Y_{11}) = \omega(C_{gsp} + 2C_b) \tag{3.5}$$

$$\mathrm{Im}(\omega Y_{22}) = \omega(C_{dsp} + C_b) \tag{3.6}$$

$$\mathrm{Im}(\omega Y_{12}) = \mathrm{Im}(\omega Y_{21}) = -\omega C_b \tag{3.7}$$

By fitting the Y-parameters, the capacitances for AlGaN/GaN dual channel HFET are obtained as C_{gsp}=23fF, C_{dsp}=31fF and C_b=16fF respectively. The raw data is shown in Figure 3.26.

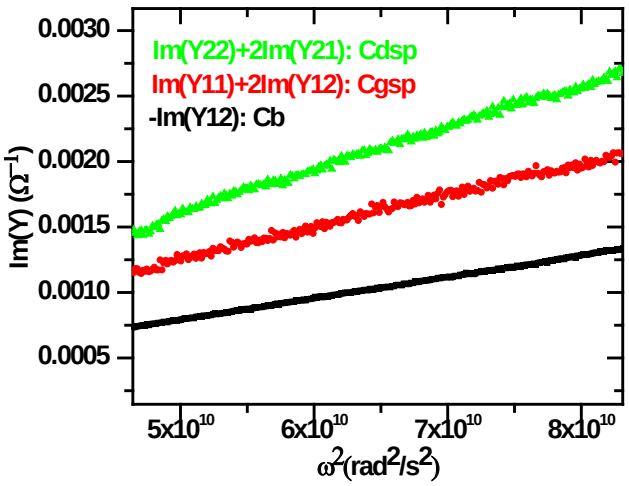


Figure 3.26 Extracted extrinsic capacitances for AlGaN/GaN dual channel HFET under pinch-off Cold-FET condition with DC bias condition as V_{DS} = 0V, V_{GS} = □8V

After the extraction of extrinsic capacitance, the parasitic inductances and resistances are extracted. Usually the parasitic inductances and resistances are measured under cold-FET conditions with large forward gate bias (V_{DS} = 0, V_{GS} >> 0) in order to reduce the depletion capacitance to a large extent [62].In such a condition, the gate current will be very high and the gate capacitance is shunt, and not only the g_m but also the capacitances inside the intrinsic circuit are ignored with only parasitic elements left. The inductances and access resistances can be easily calculated after subtracting the parasitic capacitances. But this kind of measurement condition is not suitable for GaN based HFETs. Since there exist gate differential resistances in HFET, the high forward gate bias is required to eliminate the channel capacitance, which is usually accompanied by the unrecoverable damage onto the gate. Therefore, for GaN based HFETs, the prevalent methods used to

extract these inductances and resistances are often conducted at zero or small negative gate bias conditions. After de-embeding the extrinsic capacitances, C_{gsp} and C_{dsp}, the rest parts are simulated and calculated by following the equivalent circuit shown in Figure 3.27. The DC bias condition for this measurement is $V_{DS} = 0$ and $V_{GS} = 0$.

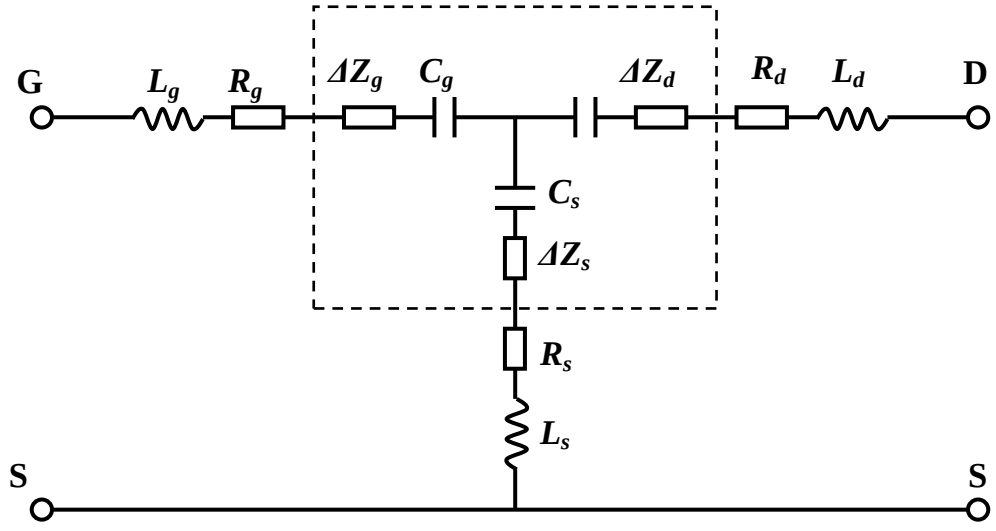


Figure 3.27 Reduced equivalent circuit for zero gate bias cold-FET condition, after removing the pad capacitances.

After subtracting the parts introduced by pad capacitances from the s-parameters, the s-parameters are converted into z-parameters. By linear fitting the Z_{11}, Z_{22}, and Z_{12} following the equations show below, we can have the *Ls*, *Ld* and *Lg* from the slops of the curves.

$$\mathrm{Im}(\omega Z_{11}) = \omega^2 (L_s + L_g) - (\frac{1}{C_s} + \frac{1}{C_g}) \quad (3.8)$$

$$\mathrm{Im}(\omega Z_{22}) = \omega^2 (L_s + L_d) - (\frac{1}{C_s} + \frac{1}{C_d}) \quad (3.9)$$

$$\mathrm{Im}(\omega Z_{12}) = \omega^2 L_s - \frac{1}{C_s} \quad (3.10)$$

The fitting curves are shown in Figure 3.28. From the fitting we can have the inductances as L_s = 6.1pH, L_d = 29.0pH and L_g = 39.1pH.

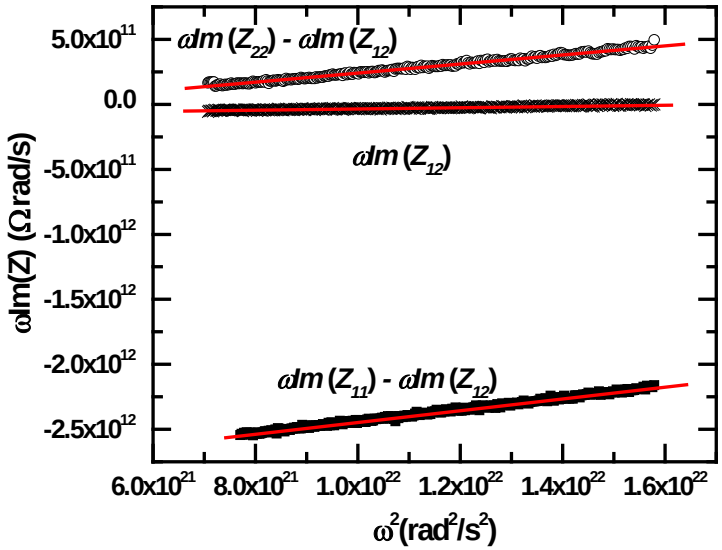


Figure 3.28 Fitting and Extraction of parasitic inductances determined from cold measurement at V_{DS} = 0 V, V_{GS} = 0 V

The extraction of parasitic resistances is most tricky part. We employed the method reported by A. Jarndal *et al.* by measuring the s-parameters under different small negative gate biases [55]. As the gate bias varied from zero to small negative, the parasitic resistances follow the equations shown below:

$$\mathrm{Re}(Z_{11}) = R_s + R_g \tag{3.11}$$

$$\mathrm{Re}(Z_{22}) = R_s + R_{ch}/2 \tag{3.12}$$

$$\mathrm{Re}(Z_{12}) = R_s + R_d + R_{ch} \tag{3.13}$$

In these three equations, R_{ch} is the channel resistance. As we know, under different gate bias the channel resistance changes with the sheet density in 2DEG channel. By measuring the Z-parameters under different negative gate bias, the Rs and Rd can be extracted by interpolating the curve of real part of Z_{22} and Z_{12} versus $1/(V_{GS}-V_{th})$, as illustrated by M. Berroth *et al.* [59]. Finally R_g can be obtained by subtracting the real part of Z_{11} with R_s.

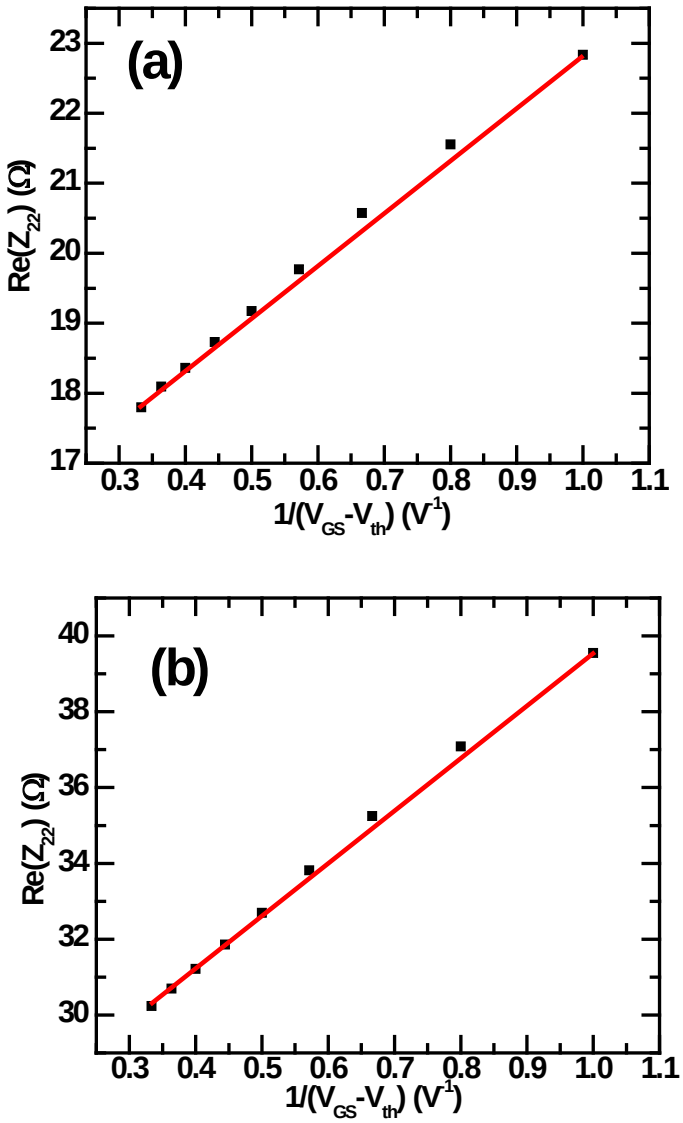


Figure 3.29 Fitting of $Re(Z_{12})$ and $Re(Z_{22})$ at various gate biases for the extraction of parasitic resistances

Following this method as fitted in Figure 3.29, the parasitic resistances are extracted as R_s = 15.33Ω, R_d = 10.26Ω and R_g = 30.26Ω.

So far, the extrinsic parameters for AlGaN/GaN dual channel HFETs are extracted. They are shown in Table 3.2 for summary.

Table 3.2 The extracted extrinsic parameters

C_{dsp}	C_{gsp}	L_s	L_d	L_g	R_s	R_d	R_g
31fF	23fF	6.1pH	29.0pH	39.1pH	15.33Ω	10.26Ω	30.26Ω

After the extrinsic parameters extracted, the intrinsic parameters can be calculated from the s-parameters with extrinsic parts subtracted. The basic formulas for the intrinsic extraction is,

$$[Y_{\text{int}}] = \begin{bmatrix} Y_{11i} & Y_{12i} \\ Y_{21i} & Y_{22i} \end{bmatrix} \tag{3.14}$$

Here Y_{int} is the intrinsic Y-parameters under a certain DC bias condition with the extrinsic parts subtracted.

$$Y_{11i} = \frac{\omega^2 R_i C_{gs}^2}{D_1} + \frac{\omega^2 R_{gd} C_{gd}^2}{D_2} + j\omega\left(\frac{C_{gs}}{D_1} + \frac{C_{gd}}{D_2}\right) \tag{3.15}$$

$$Y_{12i} = -\frac{\omega^2 R_{gd} C_{gd}^2}{D_2} + j\omega\frac{C_{gd}}{D_2} \tag{3.16}$$

$$Y_{21i} = -\frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega\frac{C_{gd}}{1 + j\omega R_{gd} C_{gd}} \tag{3.17}$$

$$Y_{22i} = \frac{\omega^2 R_{gd} C_{gd}^2}{D_2} + j\omega\left(C_{ds} + \frac{C_{gd}}{D_2}\right) \tag{3.18}$$

$$D_1 = 1 + \omega^2 R_{gs} C_{gs}^2 \tag{3.19}$$

$$D_2 = 1 + \omega^2 R_{gd} C_{gd}^2 \tag{3.20}$$

By solve the equations above; the intrinsic parameters can be extracted. However, in the actual operation, to directly solve the equation generally produces significant errors for some elements, due to the unavoidable measurement uncertainties and the inaccuracies

during the extraction of extrinsic elements. The accuracy of intrinsic parameters can be improved by linear aggression for a series of new-defined variables, as proposed by Jarndal *et al.* [52]. The detailed operations are described as follow.

The admittance of the intrinsic gate to source branch Y_{gs} is:

$$Y_{gs} = Y_{11i} + Y_{12i} = \frac{\frac{1}{R_{fs}} + j\omega C_{gs}}{1 + \frac{R_{gs}}{R_{fs}} + j\omega R_{gs} C_{gs}} \tag{3.21}$$

In this equation, the R_{fs} and R_{gs} is the resistance caused by the gate-source and gate-drain leakage current. In our simulation, it is found these resistances are very large due to the low leakage current. So they are not included in the equivalent circuit. Based on this equation, a new variable D_{Cgs} is defined as:

$$D_{Cgs} = \omega \frac{\left|Y_{gs}\right|^2}{\mathrm{Im}\left(Y_{gs}\right)} = \frac{1/R_{fs}^2}{C_{gs}} + \omega^2 C_{gs} \tag{3.22}$$

The value of C_{gs} can be obtained by fitting the slope of D_{Cgs} versus ω^2.

For extracting R_{gs}, the variable D_{Rgs} is defined as:

$$D_{Rgs} = \omega \frac{\left|Y_{gs}\right|}{\mathrm{Im}\left(Y_{gs}\right)} = \frac{1/R_{fs}^2\left(1 + R_{gs}/R_{fs}\right)}{C_{gs}} + \omega^2 R_{gs} C_{gs} - j \tag{3.23}$$

R_{gs} can be extracted by fitting the slope of D_{Rgs} versus ω^2 with C_{gs} divided.

To extract C_{gd} and R_{gd}, the admittance of the intrinsic gate to drain branch Y_{gd} is defined as:

$$Y_{gd} = -Y_{12i} = \frac{\frac{1}{R_{fd}} + j\omega C_{gd}}{1 + \frac{R_{gd}}{R_{fd}} + j\omega R_{gd} C_{gd}} \tag{3.24}$$

The new variable D_{Cgd} can be defined as:

$$D_{Cgd} = \omega \frac{\left|Y_{gd}\right|^2}{\mathrm{Im}\left(Y_{gd}\right)} = \frac{1/R_{fd}^2}{C_{gd}} + \omega^2 C_{gd} \tag{3.25}$$

The value of C_{gd} can be obtained by fitting the slope of D_{Cgd} versus ω^2. Similarly, D_{Rgd} is defined for R_{gd} extraction:

$$D_{Rgd} = \omega \frac{\left|Y_{gd}\right|}{\mathrm{Im}\left(Y_{gd}\right)} = \frac{1/R_{fd}^2\left(1+R_{gd}/R_{fd}\right)}{C_{gd}} + \omega^2 R_{gd} C_{gd} - j \tag{3.26}$$

The intrinsic transconductance branch Y_{gm} is defined as:

$$Y_{gm} = Y_{21i} - Y_{12i} = \frac{g_m e^{-j\omega\tau}}{1 + \frac{R_{gs}}{R_{fs}} + j\omega R_{gs} C_{gs}} \tag{3.27}$$

D_{gm} can be defined as:

$$D_{gm} = \left|\frac{Y_{gs}}{Y_{gm}}\right|^2 = \left(\frac{1}{g_m R_{fs}}\right)^2 + \omega^2 \left(\frac{C_{gs}}{g_m}\right)^2 \tag{3.28}$$

The value of g_m can be obtained by fitting the slope of D_{gm} versus ω^2 and $g_m = \frac{C_{gs}}{\sqrt{slope}}$.

The variable for D_τ is defined as:

$$D_\tau = \Phi\left[\left(\frac{Y_{gm}}{Y_{gs}}\right)\left(\frac{1}{R_{fs}} + j\omega C_{gs}\right)\right] = \Phi\left(g_m e^{-j\omega\tau}\right) = \omega\tau \tag{3.29}$$

The value of τ can be extracted by fitting the slope of D_τ versus ω.

The admittance of the intrinsic drain to source branch Y_{ds} is:

$$Y_{ds} = Y_{22i} + Y_{12i} = g_{ds} + j\omega C_{ds} \tag{3.30}$$

The value of gds can be obtained by fitting the slope of $\omega Re(Y_{ds})$ versus ω. A new variable D_{Cds} can be defined as:

$$D_{Cds} = \mathrm{Im}(Y_{ds}) = \omega C_{ds} \tag{3.31}$$

The value of C_{ds} can be extracted by fitting the slope of D_{Cds} versus ω.

Following the equations listed above, the values of parameters in the equivalent circuit can be extracted. To compare and analyze AlGaN/GaN dual channel HFETs with the conventional InAlN/GaN HFETs, the same extraction procedure was performed on both samples. Some critical parameters at various gate biases are compared to dig out the advantages of AlGaN/GaN dual channel HFETs.

The extracted intrinsic transconductance variations with the drain and gate bias is shown in Figure 3.30. The AlGaN/GaN dual channel HFET demonstrates the higher transconductance at the same drain bias. In addition, the intrinsic transconductance variations with the gate bias are much less for the AlGaN/GaN dual channel HFET, which confirms the better linearity. It is found that the access source resistance for AlGaN/GaN dual channel HFET is much higher than that for AlGaN control HFET. Therefore the AlGaN control HFET shows the higher extrinsic transconductance, even though the intrinsic transconductance of AlGaN/GaN dual channel HFET is obviously higher than that for AlGaN control HFET. The increased access source resistance of AlGaN/GaN dual channel HFET is caused by the degraded mobility of the AlGaN/GaN dual channel HFET in the access region due to the alloy scattering introduced by the extra AlGaN channel. With the drain bias varied, the intrinsic transconductance for AlGaN control HFET reaches the maximum close to the knee voltage and then decreases with the drain bias. However, that for AlGaN/GaN dual channel HFET continuously increases and the peak transconductance is at the drain bias of 14V. The variations of the

intrinsic transconductance for both AlGaN control HFET and AlGaN/GaN dual channel HFET is fairly similar with the variations of the cut-off frequencies.

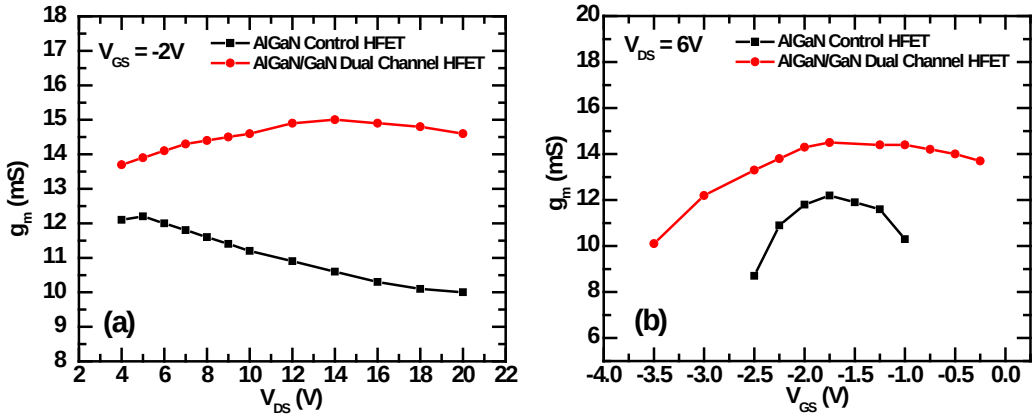


Figure 3.30 The extracted intrinsic transconductance for AlGaN control HFET and AlGaN/GaN dual channel HFET. The drain bias for AlGaN control HFET and AlGaN/GaN dual channel HFET is 7V and 22V respectively.

For the GaN-based HFETs, it is found that the virtual gate introduced by the surface traps plays the critical role [63] [64]. The surface charge on the drain side of the gate edge introduces the virtual gate and depletes the electrons in the channel and make the channel current prematurely saturates. With the drain bias increased to more than knee voltage, the virtual gate effect is more pronounced. For AlGaN control HFET, with the drain bias higher than 6V, the virtual gate depletes the electrons near the gate edge and causes the electron velocity saturate prematurely. Therefore, the cut-off frequency and intrinsic transconductance decreases as shown for the AlGaN control HFET in Figure **3.30**(a). At high drain bias, the electron velocity is accelerated further and punch through the depletion region introduced by the virtual gate so that the current density recovers marginally. As the result, the current gain cut-off frequency increases slightly, which has been simulated and explained clearly by Roff *et.al.* [65]. In contrast, the cut-off frequency increases continuously with the drain bias for the AlGaN/GaN dual channel HFET. As confirmed with the channel charging delay analysis, there are the upper

AlGaN channel and lower GaN channel conducting simultaneously. With the drain bias increased, the virtual gate depletes the upper AlGaN channel. However the upper AlGaN channel screens the vitual gate effect so that the electrons in GaN 2DEG channel are accelerated continuously with the drain bias without obviously saturation. The screening effect of second channel has been reported by Chu R. M. *et. al.* [66]. Once the AlGaN channel is totally depleted, the virtual gate effect appears on the GaN channel and the intrinsic transconductance starts to decrease for AlGaN/GaN dual channel HFET. However, in the meantime the gate-drain depletion region is extended so that the output resistance increases with the drain bias as shown in Figure 3.31(a). Even though the intrinsic transconductance is decreased slightly, the high output resistance helps the cut-off frequency increase continuously.

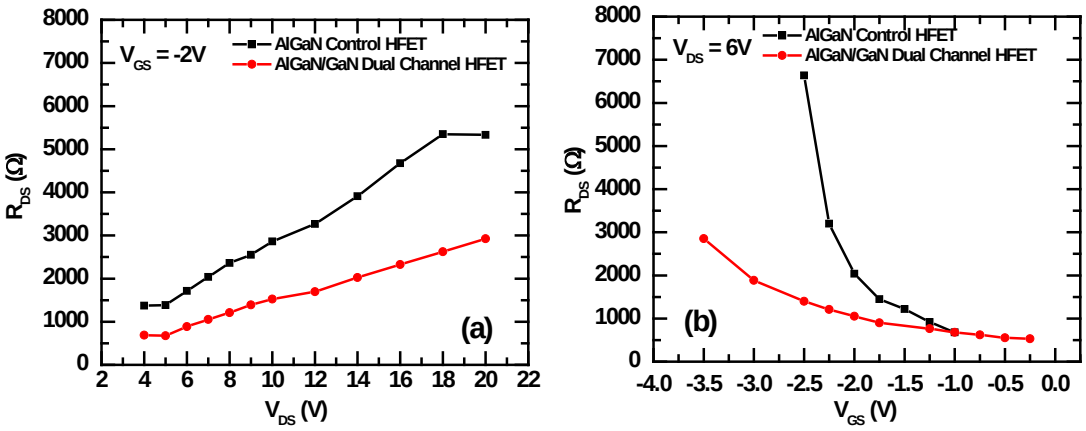


Figure 3.31 The extracted output resistance varying with the drain bias (a) and gate bias (b)

Since the electrons is spread out in a wider channel, the Lg/t aspect ratio (Lg/t, Lg is the gate length and t is the channel width) for AlGaN/GaN dual channel HFET is lower than that for the AlGaN control HFET. Therefore, it can be seen that the AlGaN/GaN dual channel HFET shows the lower output resistance as shown in Figure 3.31.

3.8 Summary

We introduced the novel AlGaN/GaN dual channel HFET structure and investigated its advantages over the conventional HFET structure. With the extra AlGaN channel inserted between AlN spacer and GaN buffer, the electrons spread out in a wider 2DEG channel and the peak electron concentration is lower than the conventional GaN 2DEG channel, which is confirmed by the C-V measurement. The maximum cut-off frequency of AlGaN/GaN dual channel HFET is much higher than that for AlGaN control HFET. The 2DEG density corresponding to the maximum cut-off frequency for AlGaN/GaN dual channel HFET is slightly higher than that for AlGaN control HFET. It is explained that the upper AlGaN channel screens the virtual gate effect introduced by the surface charge. Therefore with the drain bias increased there is no obvious current degradation and electron velocity premature in the gate edge of the drain side for the lower GaN channel. The cut-off frequency increases continuously with the drain bias. In addition, the AlGaN/GaN dual channel HFET shows the much better linearity than the AlGaN control HFET. With small signal extraction, we compared the parasitic parameters of the AlGaN/GaN dual channel HFET with the AlGaN control HFET. The output resistance of AlGaN/GaN dual channel HFET is lower than that for AlGaN control HFET due to the lower Lg/t aspect ratio.

Chapter 4 Process and Growth of *m*-plane GaN on Si (112) substrates

4.1 Introduction and Motivation of GaN growth on Si (112) substrates

Silicon substrates are very attractive for the growth and fabrication of GaN based devices, because of their high quality, good thermal conductivity, low cost and compatibility with mature standard Si process. Tremendous research has been carried on the GaN growth on Si substrates. GaN-based HFETs have been successfully fabricated on Si (111) substrates and are available on the market. The polarization effects necessary for GaN HFETs can also be used on GaN on Si (111) substrates. However, for GaN based light emitting devices (LEDs), the Polarization charge induced by both strain and compositional gradient cause a Stark Effect that substantially reduces the electron and hole wavefunction overlap in quantum wells, particularly at low injection levels. In this case Internal Quantum Efficiency (IQE) of LEDs is significantly reduced by the polarization effects. The elimination of the polarization fields therefore is expected to be very beneficial for the production of high efficiency and high power LEDs [67].

So far the *m*-plane and *a*-plane GaN growth on different substrates have been carried out but different research groups [68] [69]. As indicated in Figure 4.1, both the *m*-plane and *a*-plane GaN are non-polar orientation and promising for the non-polar LEDs. However *a*-plane GaN has a large concentration of stacking faults which hinder radiative recombination and produce films that are optically inefficient (<1% of *c*-plane GaN) and dismal In incorporation. The *m*-plane orientation of GaN is predicted to be better suited for optical applications. If m-plane GaN can be grown on Si substrate, the cost of LEDs

can be reduced significantly. Tanikawa T. *et. al.* have successfully grown $(11\bar{2}0)$ *a*-plane GaN on a patterned Si (110) substrate [70]. The growth is initiated on a $(\bar{1}11)$ side wall of a (110) Si substrate which was prepared by KOH anisotropic etching. Suzuki N. *et. al.* also grew the semi-polar $(11\bar{2}2)$ on a patterned Si (113) substrate by HVPE [71].

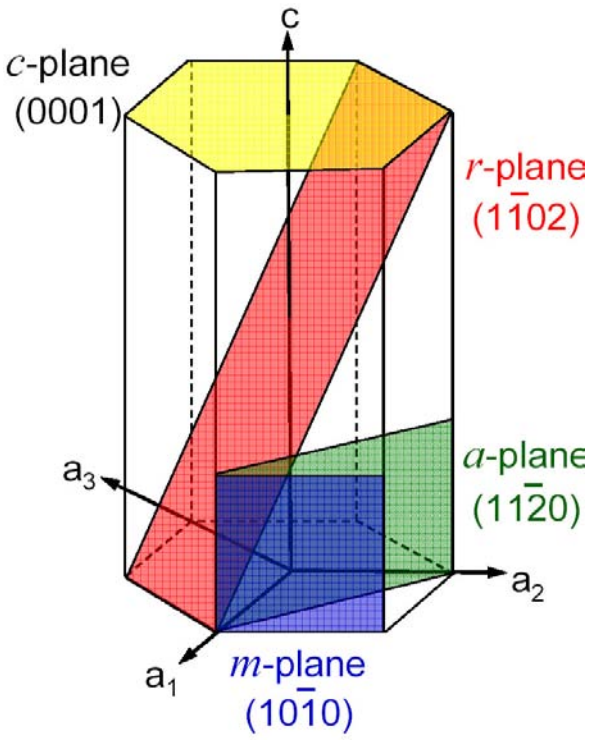


Figure 4.1 Most common crystal planes in wurtzite GaN.

Ignited from the work of GaN growth on patterned Si substrates, we can easily come out if it is possible to grow *m*-plane GaN on a patterned Si substrate. As known from the KOH anisotropic etching experiments for Si substrates, we can know that the etching rates for different facets are different. As indicated in Figure 4.2, the etching rate of Si (111) facet is the lowest among all the facets of Si crystal [72]. If carefully choosing the Si wafer orientation, we can have the Si (111) facet perpendicular to the wafer surface. In this case, hexagonal GaN crystal grows on Si (111) facet and the *c*-plane of this kind of

GaN is parallel to the wafer surface. That is to say, the hexagonal GaN is laid down on the Si wafer and *m*-plane GaN can be exposed as GaN epi-surface. Based on such a general idea, we can analyze the GaN growth orientation on Si substrate in detail.

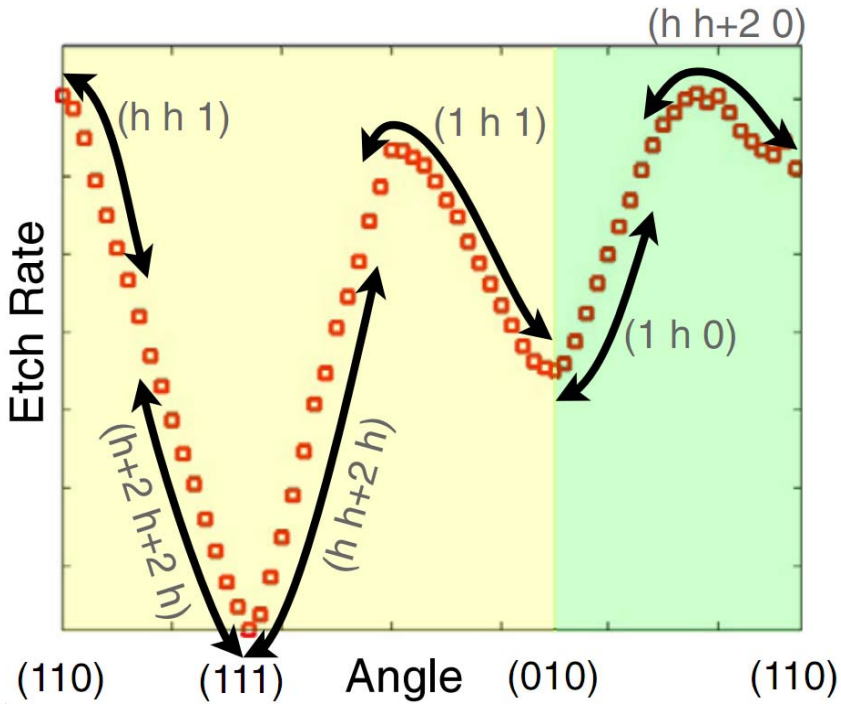


Figure 4.2 Etch rates for all the crystallographic orientations of Si

It is well known that hexagonal GaN(0001) grows on Si(111), with the following epitaxial relationships: GaN<0001>||Si<111> and GaN< $2\bar{1}\bar{1}0$ > ||Si<011>. GaN grown on other planes of Si, such as Si(100) is primarily a mixture of cubic and hexagonal phases [73] [74]. Semi-polar GaN has been grown on stripe-patterned Si(001) substrates that are miscut 7° toward Si<110> [75], where the growth of GaN was initiated on Si (111) side facets with GaN parallel to the substrate plane. For hexagonal phase GaN growth, nucleation takes place on the Si (111) surface. Based on the epitaxial relationships between GaN and Si (111), *a*-plane GaN ($11\bar{2}0$) aligns with Si(110). Similarly, it is possible to align *m*-plane GaN ($1\bar{1}00$) with Si (112), and semi-polar GaN

$(11\bar{2}2)$ with Si (113). In all of these cases, GaN growth is initiated on Si (111) facets, which requires patterning of Si substrate to expose and allow only certain (111) facets for growth initiation.

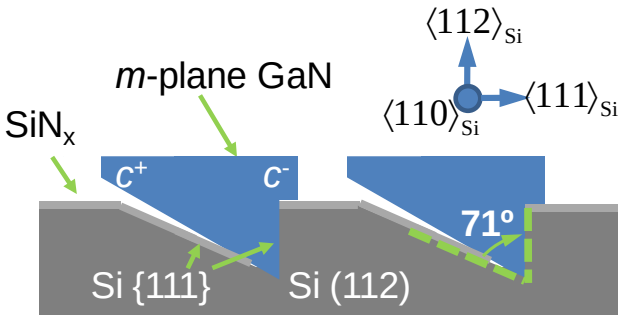


Figure 4.3 Schematic for *m*-plane GaN growth on a Si (112) substrate.

According to the growth orientation analysis discussed above, the *c*-axis of hexagonal GaN aligns with Si <111>, if vertical Si {111} surfaces can be generated and lateral growth along the c-axis is promoted, the nonpolar a- and m-planes of GaN parallel to the substrate plane can be obtained. In this manner, it should be possible to obtain m-plane GaN $(1\bar{1}00)$ on Si (112) substrates by initiating growth on Si {111} sidewalls as shown in Figure 4.3.

Based on the analysis above, the process and growth steps for *m*-plane GaN on Si (112) substrate is: (1) Prepare the Si (112) substrate with Si {111} facets exposed by using KOH etching; (2) Grow AlN nucleation on patterned Si (112) substrate; (3) Cover the Si (112) substrate except the Si (111) facets with SiN layer; (4) Grow GaN on the patterned Si (112) substrate covered with SiN.

4.2 Preparation of patterned Si (112) substrate

To pattern Si (112) substrate with Si {111} facets exposed, we apple SiN layer as the etching mask. At first Si (112) substrate is cleaned with standard RCA procedure. Then the Si (112) substrate is loaded into PECVD chamber and a SiN layer with thickness of 100nm is deposited on the Si (112) substrate. To obtain the Si {111} facets with one perpendicular to the Si (112) surface and the other angled 29° with Si (112) surface, we used the photolithography technique to pattern stripe shape mask on top of SiN layer. When the Si (112) substrate was loaded for photolithography, the wafer orientation is carefully calibrated to make sure that the stripes on the mask are along Si <110> direction. The periodic stripes are composed of 4μm mask strip and 10μm open window. After the photolithography, the Si (112) substrate is loaded into our SAMCO ICP system and SiN layer in the open window areas are dry etched with CF_4 gas. In the ICP etching, the flow rate of CF4 is 20sccm. The plasma bias power and ICP power is 150 and 40W respectively. The SiN layer in open window areas is removed after 1min etching with etching rate of 100nm/min. The process steps and final SEM image are show in Figure 4.4 in detail.

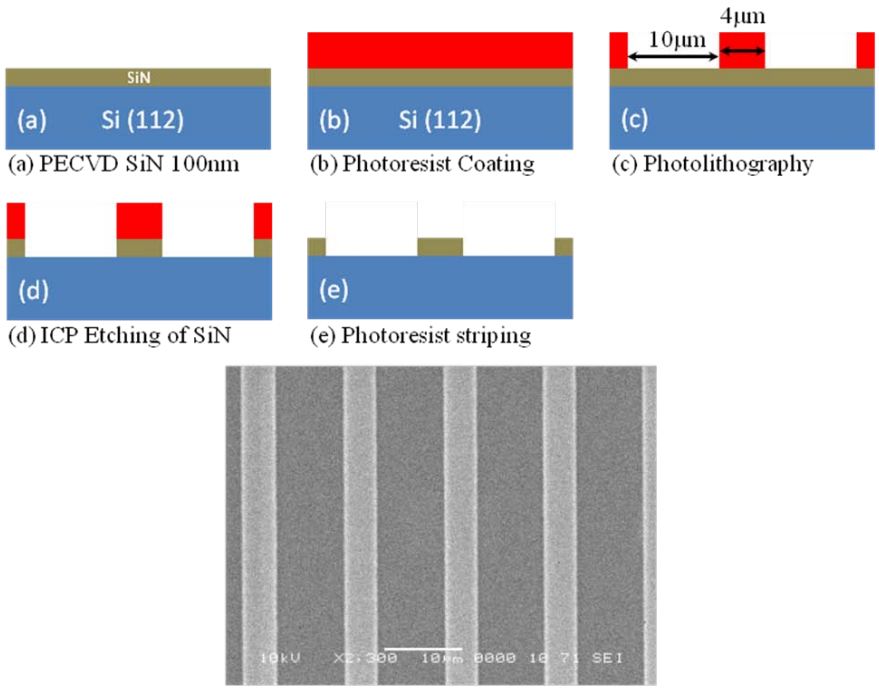


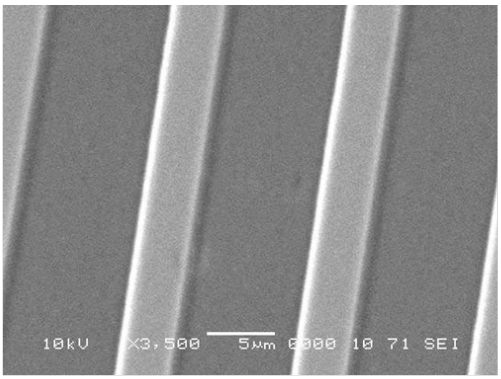
Figure 4.4 Patterning procedure of Si (112) substrate: (a)-(e) the process steps; (f) SEM image of Si (112) substrate after the SiN layer in the open window areas etched.

After the SiN ICP etching, the substrate was checked with SEM EDX to make sure the SiN layer in the open window areas are removed totally. So far the Si (112) substrate is prepared and ready for KOH wet etching. In this process, the alignment of the stripes along Si <110> direction is critical for the following wet etching. Otherwise the smooth Si {111} facets cannot be realized.

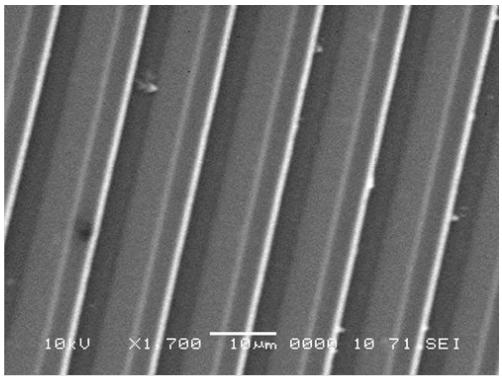
4.3 KOH anisotropic wet etching of Si (112) substrate

With patterned Si (112) substrate, the KOH wet etching is employed to form Si {111} facets. In order to obtain the smooth Si {111} facets, the concentration of KOH solution and the etching temperature is very important and optimized. The KOH solution is made of 5g KOH pellet, 25ml DI water, and 5ml Isopropyl alcohol (IPA). The IPA is used to buffer the wet etching and helpful for smoothing the surface. The optimized etching temperature is 45°C. Several patterned Si (112) substrates are prepared to test the wet

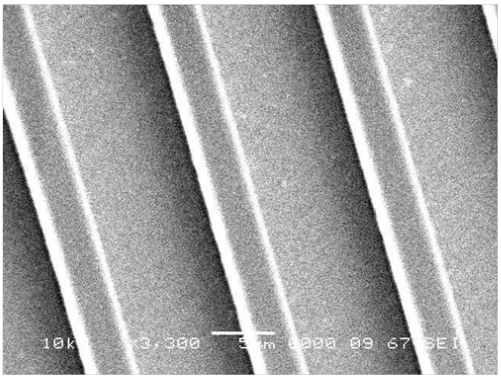
etching rate and find the optimum etching time. As discussed above, the etching rate of KOH on Si {111} facets is the slowest among all the crystallographic orientations. Once the patterned Si (112) substrates were dipped into the KOH solution, the Si (112) surface exposed to KOH was quickly etched. The angled trenches were formed in the open window areas. With the time passing by, the angle of the trenches was changed due to the competitive etching of different facets. Finally, the angle of the trenches should be formed as 71° once the Si {111} facets were reached. By using the SEM, we can check the cross section for different etching times. As indicated in Figure 4.5, the dark areas at one side of Si (112) open areas were formed. With the etching lasting, the dark area became larger for plan-view observation, which indicates the trench areas became larger and deeper. From the cross section view in Figure 4.5, after 50 minutes etching, the vertical Si $(\bar{1}\bar{1}1)$ and angled Si (111) facets were formed.



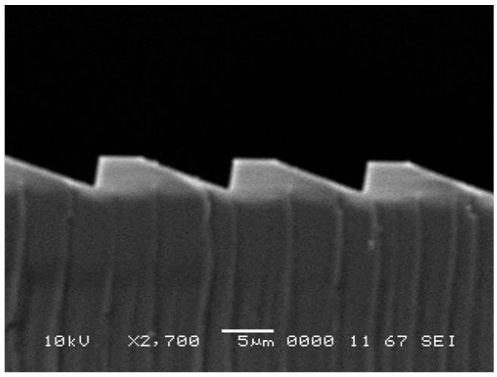
(a) After 10 min etching



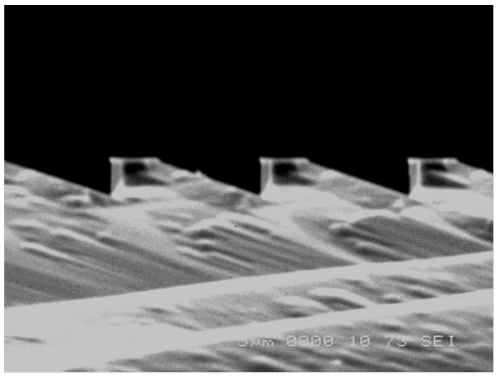
(b) After 40 min etching



(c) After 50 min etching



(d) Cross section for 40 min etching



(e) Cross section for 50 min etching

Figure 4.5 SEM images for the patterned Si (112) substrates with different KOH wet etching time.

4.6 AlN nucleation layer and GaN growth on patterned Si (112) substrate

Once the Si {111} facets are realized, the AlN nucleation layer should be deposited on the Si (112) substrates. As we know, AlN can easily nucleate on SiN amorphous layer besides the Si {111} facets. In order to grow GaN only on the vertical Si $(\bar{1}\bar{1}1)$ facets, it is very necessary to cover the AlN layer in other areas. The first experiment we had done is followed the steps as: (1) MOCVD AlN nucleation layer deposition; (2) SiO_2 deposition to cover the Si (112) and (111) surfaces; (3) MOCVD GaN growth on patterned Si (112) substrate. In this experiment, we can see that the residue SiN mask layers on top of Si (112) surfaces were not removed. In this case the randomly oriented AlN grains in the intersections areas between Si (112) and Si (111) facets cannot be fully covered by the SiO_2. Afterwards randomly grown GaN grains were formed in the intersection areas as well, which should be avoided. In all the experiments, the thickness of AlN nucleation layer is 150nm.

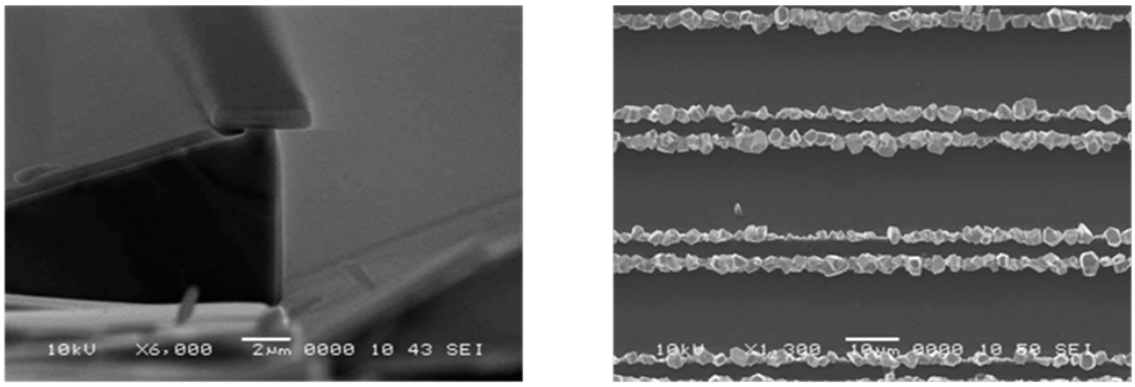
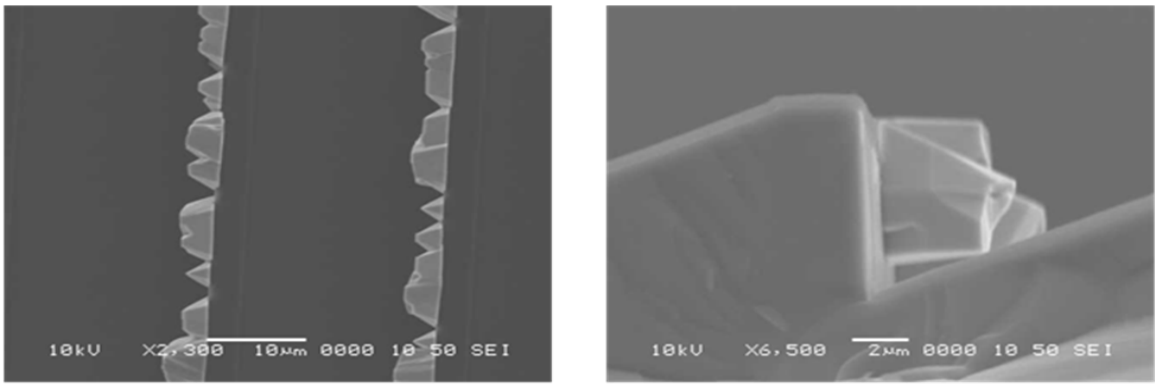


Figure 4.6 SEM images for patterned Si (112) substrate after SiO2 deposition and GaN growth

As shown in Figure 4.6, the big GaN random oriented grains are very difficult to avoid with SiN mask layer remained, since the AlN nucleation grown on the edges between Si

(112) and (111) facets provides the chance of GaN growth as well. In this case, the SiN mask layer should be removed after the KOH wet etching.

There are two methods to remove the SiN mask layers: dry etching and wet etching. With ICP dry etching employed, the SiN layers can be removed totally. But the damage to the Si $(\bar{1}\bar{1}1)$ facets during the ICP etching made growth of AlN nucleation layer and GaN not fully cover the entire Si $(\bar{1}\bar{1}1)$ facets. In addition, the GaN grains with other orientations also grew on the Si $(\bar{1}\bar{1}1)$ facets as shown in Figure 4.7. It is believed that the residue etchants during the ICP etching stayed on the Si $(\bar{1}\bar{1}1)$ facets, which hinders the nucleation of GaN.



(a) Plane-view of GaN growth on Si (112) with ICP SiN etching

(b) Cross-section of GaN growth on Si (112) with ICP SiN etching

Figure 4.7 Plane view and cross section of GaN growth on Si (112) substrate with ICP dry etching used for removing SiN mask layer

Therefore, the only option for removing SiN mask layers is to use wet etching. We used 37% HF solution to remove the SiN layers. Since the etching rate of HF to Si substrate is very slow and considered as neglected, the SiN layers can be etched away without damage the Si substrate. To make sure the SiN layers removed completely, we dipped the Si (112) substrate into HF for 40 minutes and also used the ultrasonic to enhance the

etching uniformity. The cross section of patterned Si (112) substrate after HF wet etching is shown in Figure 4.8. As well we used the SEM EDX to check if there is SiN left on the Si surfaces. After the HF wet etching, the 150nm AlN nucleation layer was deposited on the Si (112) substrate.

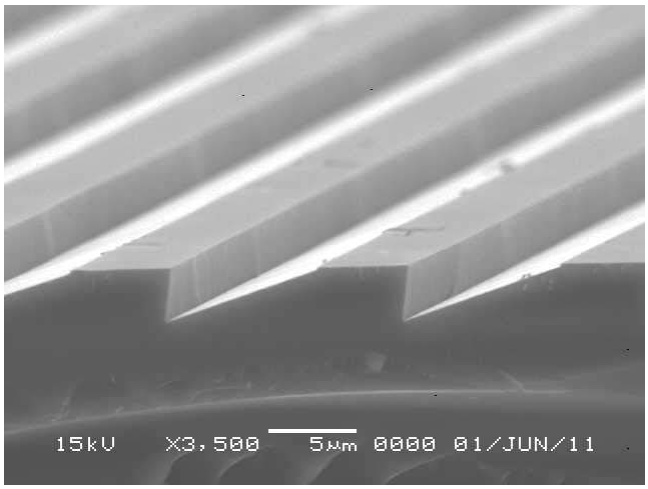
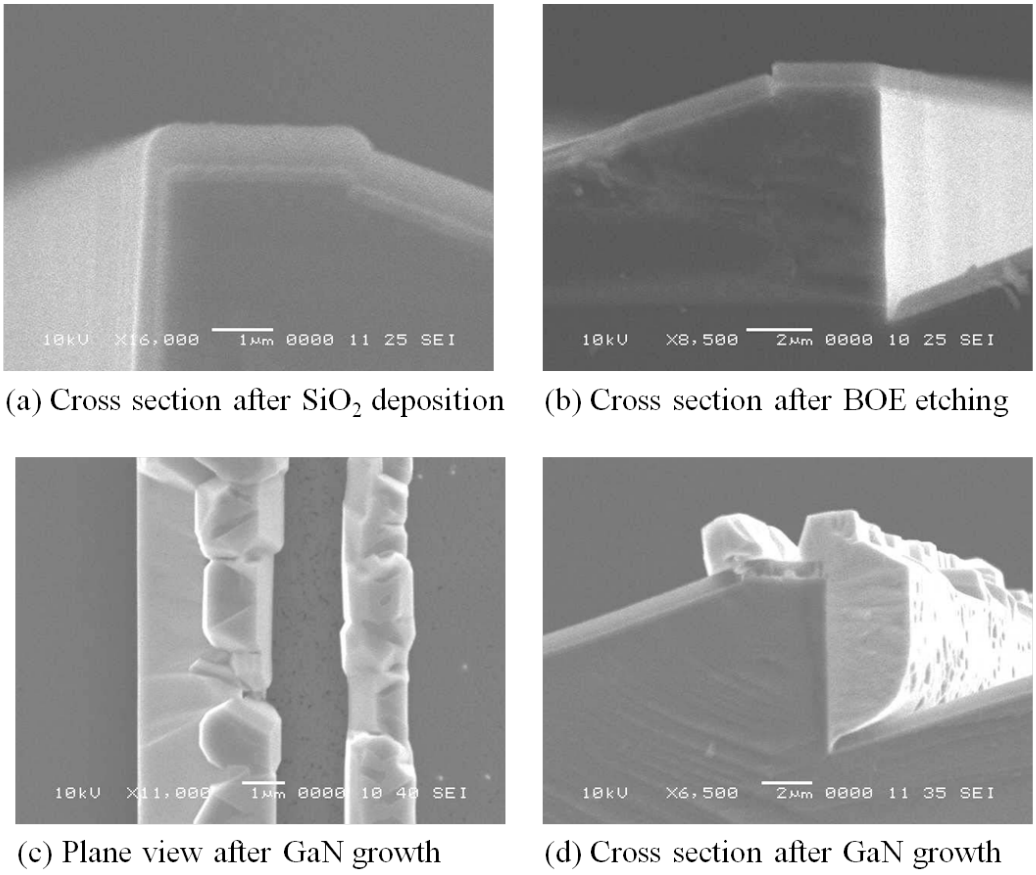


Figure 4.8 Crosse section of patterned Si (112) substrate after 40 minute HF etching

After the AlN nucleation layer deposition, it is important to cover the AlN layers on Si (112) and (111) facets and only Si $(\bar{1}\bar{1}\bar{1})$ facets for the next GaN MOCVD growth. We figured out two ways for the AlN covering: (1) SiO_2 PECVD deposition and wet etching; (2) Angled SiO_2 E-beam evaporation. The first method was chosen because of the high quality of PECVD SiO_2 layer. About 200nm SiN was deposited by using PECVD. Even though SiN layer was deposited uniformly on different Si facets during PECVD deposition, it is found that the wet etching rate for different facets varies. In order to make the etching rate in the controllable range, the BOE solution is diluted with DI water as the ratio as 1:50 (BOE: DI water). After 6 minutes etching, we can clearly see that the SiO_2 layers on Si $(\bar{1}\bar{1}\bar{1})$ facets is totally removed and those on Si (112) and (111) facets is still remained. However, the over etching in the edges between Si (112) and (111) facets

is very hard to control. The over etching crack is observed, as indicated in Figure 4.9. During the GaN MOCVD growth, the AlN nucleation layers in the crack areas also supplied the GaN nucleation. As the result, the GaN grains other than (0001) orientation were grown as well, as shown in Figure 4.9.



(a) Cross section after SiO_2 deposition (b) Cross section after BOE etching

(c) Plane view after GaN growth (d) Cross section after GaN growth

Figure 4.9 SEM images for the Si (112) substrate after SiO_2 deposition and after GaN growth

The other option for the SiO_2 covering is to use E-beam evaporation. Even though the quality of SiO_2 is not as good as PECVD SiO_2, the very good orientation of E-beam evaporation can help us cover AlN nucleation layer easily. When the patterned Si (112) substrate is loaded into the E-beam evaporator chamber, it is angled and the shadow of the Si (111) facets can prevent the SiO_2 deposition on the Si $(\bar{1}\bar{1}\bar{1})$ facets. The schematic

of the angled SiO_2 is shown in Figure 4.10. With careful organize and practice, the SiO_2 can be covered on Si (111) and (112) facets with Si $(\bar{1}\bar{1}1)$ facets exposed for GaN growth.

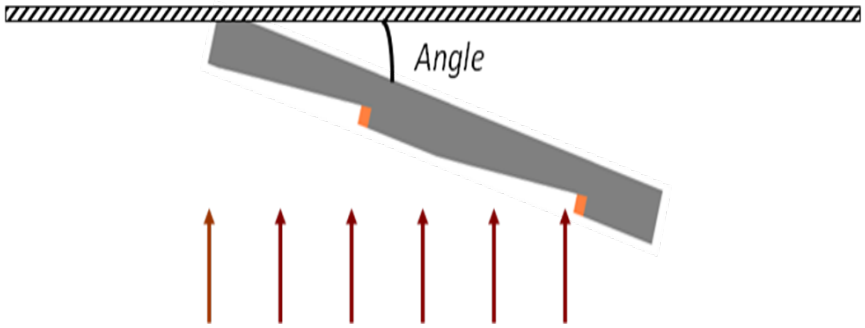


Figure 4.10 Schematic for angled SiO_2 evaporation

By using the E-beam evaporation, we managed to cover the AlN nucleation layers on Si (112) and (111) facets. As shown in Figure 4.11, the continuous SiO_2 layer covered the edge between Si (112) and Si (111) facets. In addition, the Si $(\bar{1}\bar{1}1)$ facet is clean without obvious SiO_2 particle.

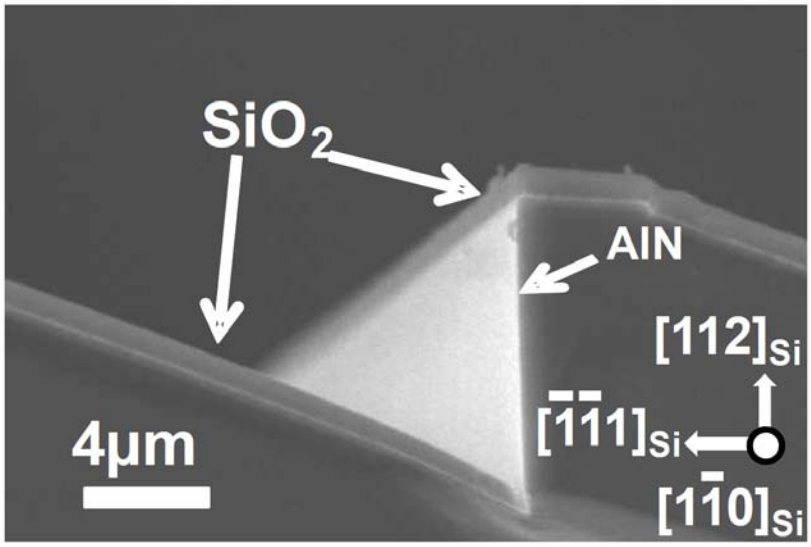
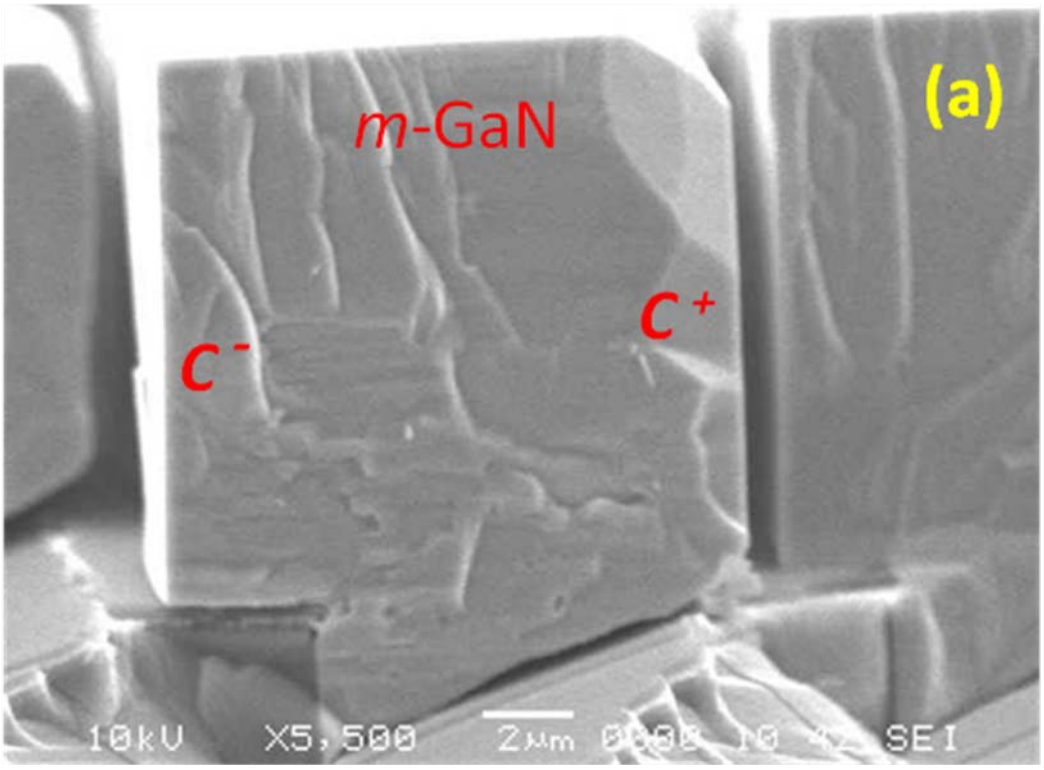


Figure 4.11 Angled cross section SEM image of patterned Si (112) substrate with E-beam evaporated SiO_2

After the SiO_2 evaporation, the Si (112) substrate is ready for MOCVD GaN growth and loaded into MOCVD chamber. GaN growth starts from the vertical Si $(\bar{1}\bar{1}1)$ facets laterally along GaN [0001] c^+ direction. In the meantime the vertical growth goes on. When the vertical growth is above the Si (112) facets, both N and Ga face GaN (0001) is exposed for the MOCVD growth. After a sufficient time of growth the GaN stripes will coalesces laterally and a continuous m-plane GaN film will be exposed on the surface.

Figure 4.12 shows the cross section view of GaN stripes grown from Si $(\bar{1}\bar{1}1)$ facets. It can be clearly seen that GaN laterally grew from Si $(\bar{1}\bar{1}1)$ facet. With good SiO_2 covering, no GaN nucleates on the SiO_2 surface. It is important to notice that the clear N and Ga face GaN planes appeared which is critical for the lateral coalescence of the GaN stripes.



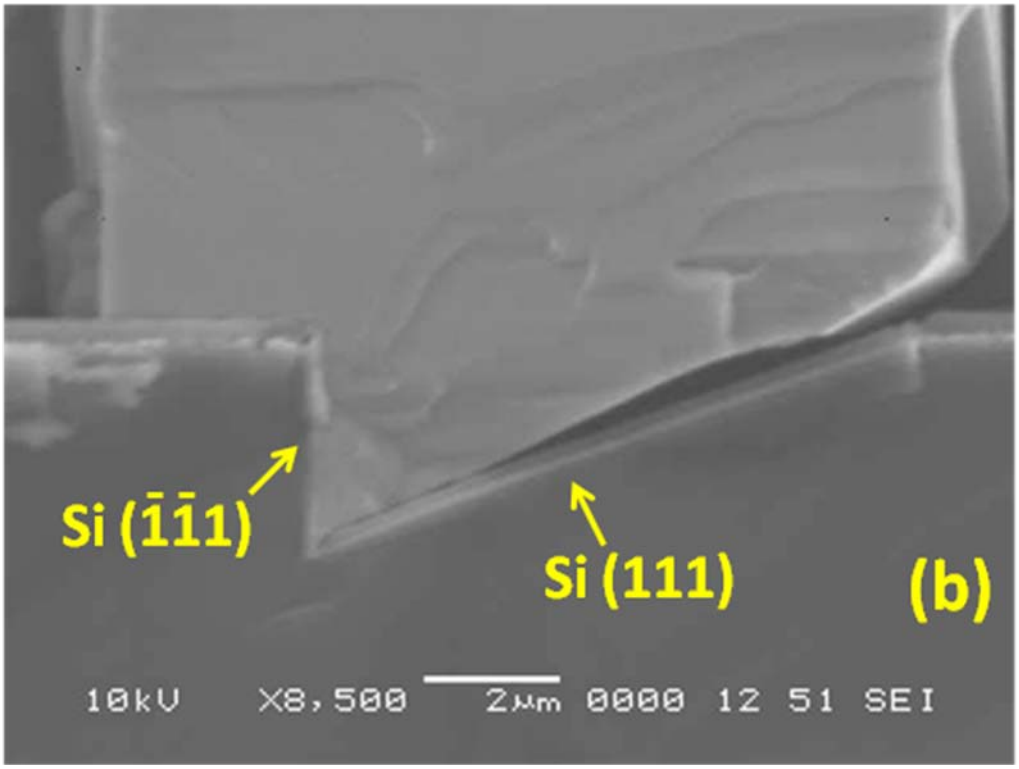
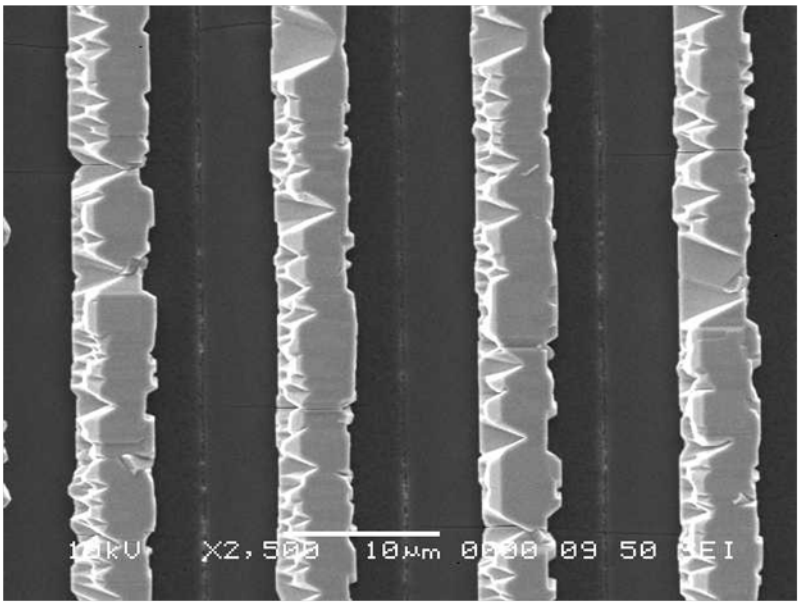
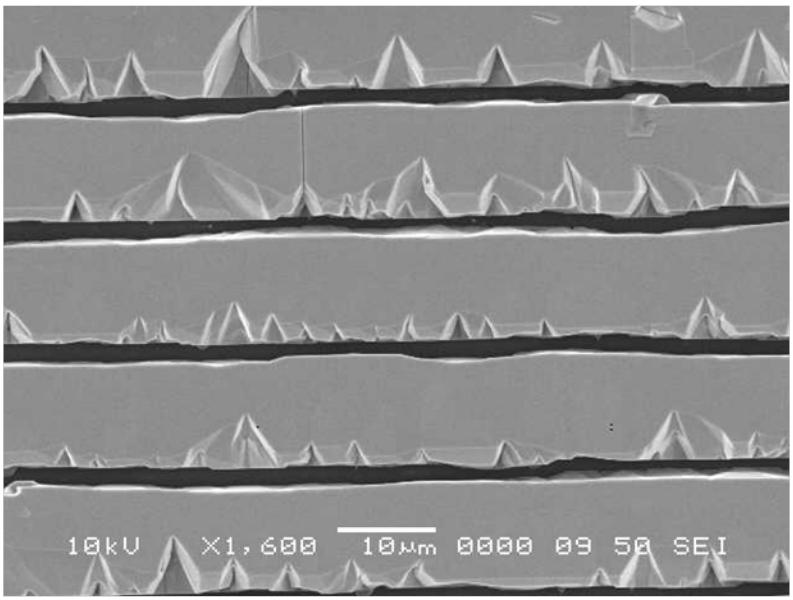


Figure 4.12 Cross section for GaN grown on patterned Si (112) substrate (a) angled cross section view of *m*-plan GaN after 3 hours growth; (b) enlarged cross section view

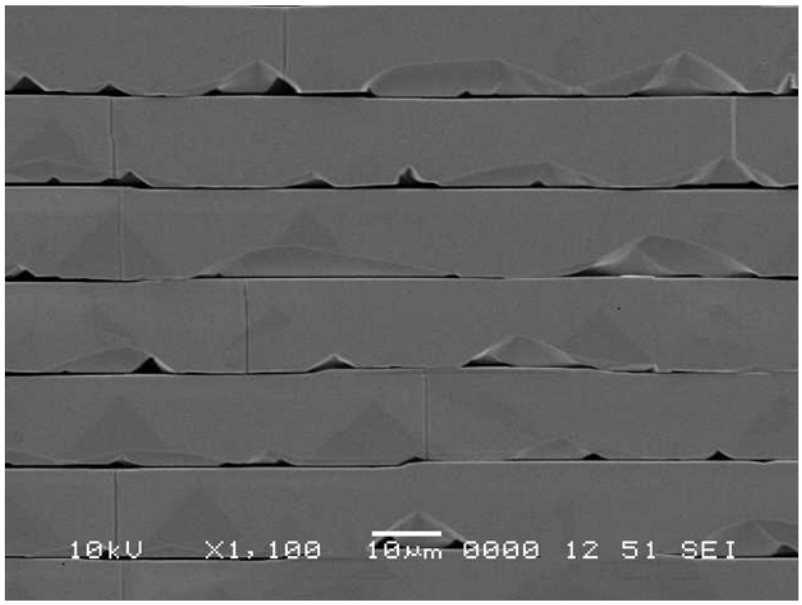
The GaN growth evolution is observed by using SEM. From Figure 4.13, we can see that GaN strips became thicker with the growth advanced, which indicates the lateral growth. No GaN grain nucleates on the other facets except Si $(\bar{1}\bar{1}1)$. At the beginning of the growth, the small GaN facets other than *m*-plan show on the GaN stripes. With the growth advanced, they are gradually replaced by the *m*-plan surface. After 3 hours growth, the *m*-plan GaN strips partially coalesce. Due to the thermal expansion difference between Si substrates and GaN, some cracks appear on the *m*-plan GaN strips.



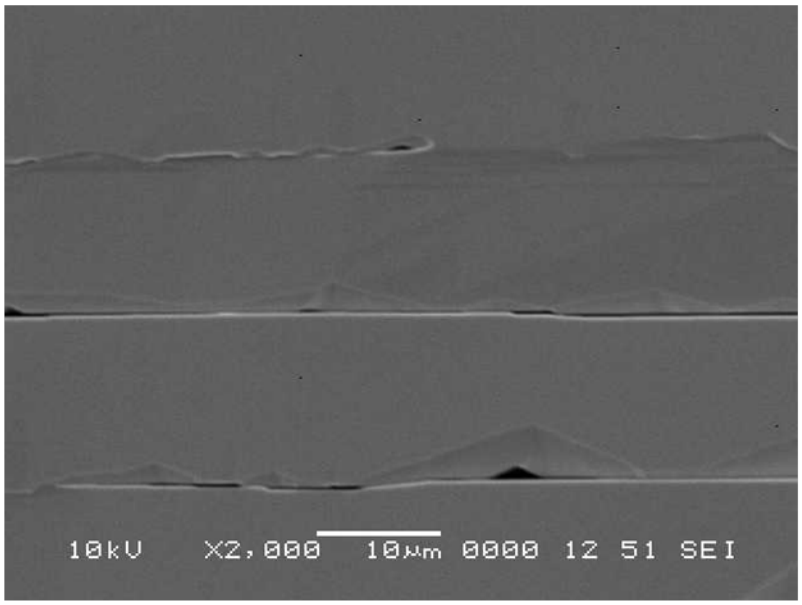
(a) Plan-view SEM image after 0.5 hour GaN growth



(b) Plan-view SEM image after 2 hours GaN growth



(c) Plan-view SEM image after 3 hours GaN growth (area 1)



(d) Plan-view SEM image after 3 hours GaN growth (area 2)

Figure 4.13 Plane view SEM images for GaN growth on patterned Si (112)substrates with different growth times

Figure 4.14 shows the tapping-mode atomic force microscopy (AFM) image of the m-plane GaN sample on Si. The image indicates a very smooth surface (RMS roughness of

~0.3 nm over an area of 2 μm × 2 μm) with clear atomic steps, indicating a step-flow growth mode for this sample.

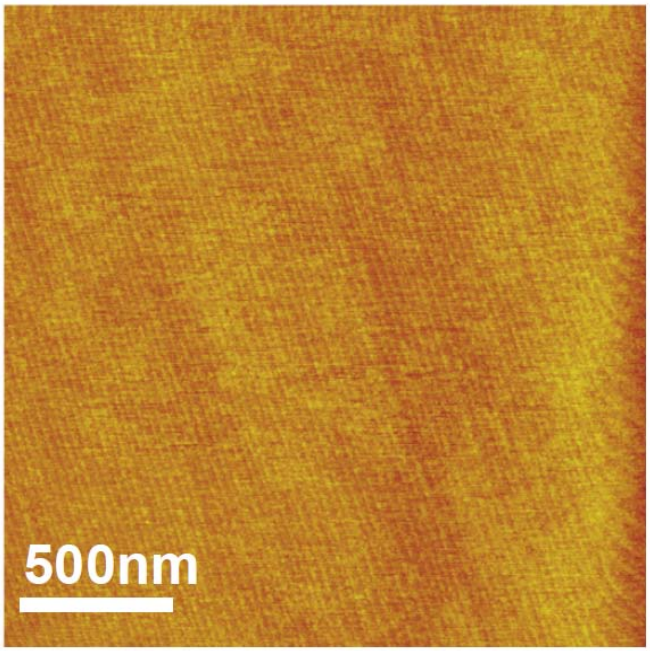


Figure 4.14 Tapping-mode AFM image (Δz = 10 nm) of an *m*-plane GaN sample (~12μm thick) grown on a patterned Si substrate. The AFM image indicates a very smooth surface (RMS roughness of ~0.3nm over an area of 2 μm×2 μm) with clear atomic steps.

In order to confirm the orientation of GaN epilayer on patterned Si (112) substrate, the XRD ω-2θ scan is employed. As indicated in Figure 4.15 (a), the *m*-plane GaN $(1\bar{1}00)$ and $(2\bar{2}00)$ diffraction peaks can be clearly seen. The XRD rocking curves are scanned toward *c*-axis and *a*-axis to check the crystal quality of m-pane GaN. As shown in Figure 4.15 (b), the rocking curve full width at half maximum (FWHM) is 9 arcmin when rocked toward the GaN *a*-axis, and 27 arcmin when rocked toward the GaN *c*-axis. Since the *m*-plane GaN stripes are laterally grown toward *c*-axis, the titling of the lateral grown wings broadens the rocking curve measured toward *c*-axis.

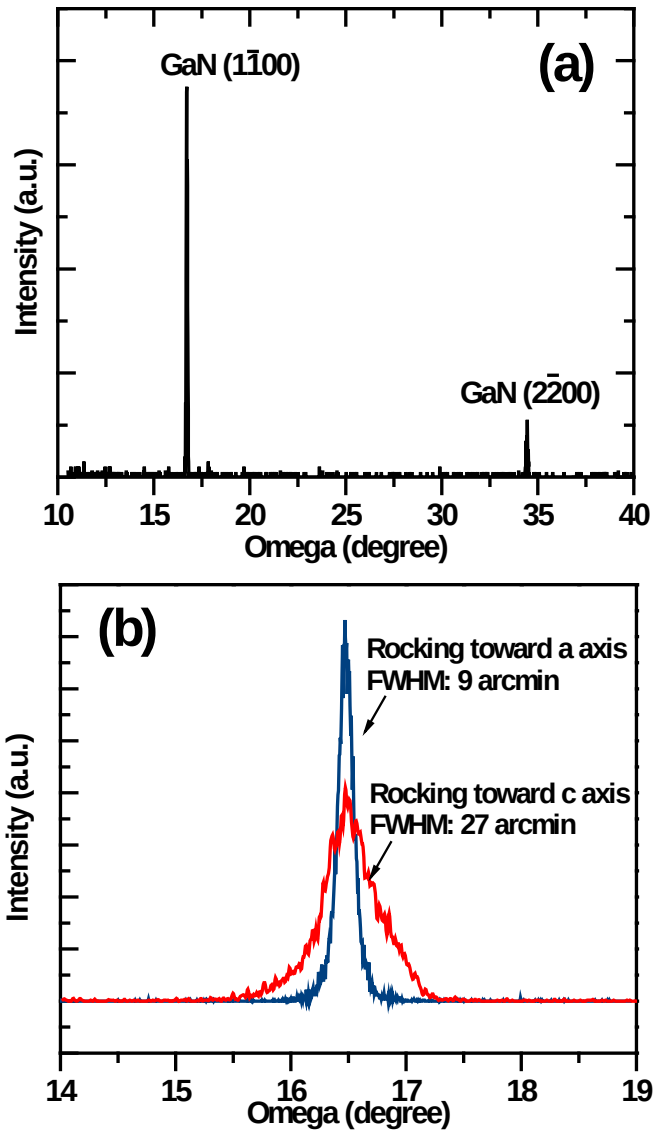


Figure 4.15 (a) XRD *ω-2θ* scan showing that the GaN has (1 100) m-plane orientation. The Si (112) plane does not have a diffraction peak due to diffraction extinction. (b) XRD rocking curves of GaN(1 100) m-plane after a 3 h growth, rocking toward the GaN *a*-axis and *c* axis.

4.7 Summary

The epitaxial growth of m-plane GaN films has been achieved on the vertical Si (111) sidewalls of patterned Si(112) substrates, as confirmed by XRD measurements. By using the KOH anisotropic wet etching, Si {111} facets is realized with one perpendicular to Si

(112) plane and one angled 39° with Si (112) surface. It is critical that after the wet etching the SiN etching mask should be removed to prevent the nucleation of AlN on SiN and random GaN grains grown on SiN layer afterwards. After AlN nucleation layer growth, the Si (112) and (111) facets are covered with SiO_2 layer by using the angled E-beam evaporation technique. After 3 hours growth, m-plane GaN is grown on vertical Si (111) sidewalls and partially coalesces. From the XRD rocking curve scanning, we can see that the rocking curve FWHM toward *c*-axis is wider than that toward a-axis, due to the titling of laterally grown swings toward *c*-axis.

Chapter 5 Conclusions and Future Work

5.1 Conclusions and future work for InAlN/GaN HFETs on bulk GaN substrates

Due to the lack of native substrates for the growth of GaN based devices, the large defect density and related problems impedes the improvement of GaN based HFETs. Recently the GaN bulk substrates have been worked out and are promising the future applications for GaN based power devices. In order to investigate the feasibility of the applications of the GaN bulk substrates on GaN based HFETs, lattice matched InAlN/GaN HFETs have been grown and fabricated on GaN bulk substrates. The defective interface problems caused by the mechanical polishing of GaN bulk substrates have been successfully solved by using the ICP dry etching and H_2 *in-situ* MOCVD etching. The lattice matched InAlN/GaN HFETs on bulk GaN substrates show the much better thermal dissipation features compared with those InAlN/GaN HFETs on Sapphire substrates. In addition, the homogenous growth guarantees the high quality and insulating GaN buffer layer. High cut-off frequencies have been realized for the 1μm and 0.7μm gate length HFETs on bulk GaN substrate.

Even though good performance has been demonstrated for the GaN based HFETs on bulk GaN substrates, there still exist some issues should be improved further. First of all, the reliability of GaN based HFETs on bulk GaN substrates should be investigated further. Especially the surface states related problems happen occasionally on HFET samples grown on some GaN substrates. Is the surface state related DC and RF dispersion is better or worse for the HFETs on bulk GaN substrates? What kind of special problems should be prevented and solved for HFETs on bulk GaN substrates?

5.2 Conclusions and future work for AlGaN/GaN dual channel HFETs

As we know, the hot phonon scattering is the bottleneck to limit the enhancement of electron velocity of GaN based 2DEG channel. As well the heat dissipation from GaN 2DEG channel is mainly impeded by the low efficiency of the conversion of hot phonons into high group velocity acoustic phonon modes. It is found that the plasmon-phonon scattering is the mechanism of the hot phonon decay and heat migration out from 2DEG channel. The optimal sheet density corresponds to the lowest hot phonon life time and highest electron velocity in 2DEG channel. Based on this knowledge, a novel AlGaN/GaN dual channel HFET structure has been proposed. By inserting an extra AlGaN channel layer between AlN spacer and GaN buffer layer, the electrons in GaN 2DEG channel are spread out in a wider channel. By using the gateless high frequency noise measurement, we confirmed that the AlGaN/GaN dual channel structure the AlGaN/GaN dual demonstrates the obviously shorter hot phonon life time and faster hot phonon decay. In terms of the HFET performance, the maximum cut-off frequency of AlGaN/GaN dual channel HFET is much higher than that for AlGaN control HFET. The 2DEG density corresponding to the maximum cut-off frequency for AlGaN/GaN dual channel HFET is slightly higher than that for AlGaN control HFET. It is explained that the upper AlGaN channel screens the virtual gate effect introduced by the surface charge. Therefore with the drain bias increased there is no obvious current degradation and electron velocity premature in the gate edge of the drain side for the lower GaN channel. The cut-off frequency increases continuously with the drain bias. In addition, the AlGaN/GaN dual channel HFET shows the much better linearity than the AlGaN control HFET. With small signal extraction, we compared the parasitic parameters of the

AlGaN/GaN dual channel HFET with the AlGaN control HFET. The output resistance of AlGaN/GaN dual channel HFET is lower than that for AlGaN control HFET due to the lower Lg/t aspect ratio.

By extracting the small signal parameters of AlGaN/GaN HFETs, we found the AlGaN/GaN HFET has obviously better linearity than the conventional GaN based HFETs. However, it is also indicated that the extra AlGaN channel degrades the electron confinement of 2DEG channel and shows worse output resistance than the conventional GaN HFETs.

In order to explore the advantages of the AlGaN/GaN dual channel HFETs, it is worth to exclude the surface state effects by using the passivation layer on the surface. In this way, we can clearly see the high frequency performance of AlGaN/GaN dual channel HFETs, compared with the conventional AlGaN HFETs.

5.3 Conclusions and future work for GaN growth on Si (112) substrates

Alternative substrates are always the very interesting topic for GaN based devices. In order to lower down the cost and improve the internal quantum efficiency of GaN based light emitting diodes, the process and growth of m-plane GaN on Si (112) has been investigated. By using the KOH anisotropic etching the Si (111) sidewalls are realized on Si (112) substrates. By using the E-beam SiO2 evaporation, the titled Si (111) and Si (112) surface have been successfully covered. In this way, GaN can only grow on the vertical Si (111) sidewall and continuous m-plane GaN has been grown on patterned Si (112) substrate. During the process and growth of m-plane GaN on Si (112) substrates, we found that there always come out some randomly orientated GaN grains due to the

poor SiO2 coverage over the titled Si (111) sidewall and Si (112) surface. The productivity of this process should be improved in the future.

6 Appendix

6.1 Extrinsic Parameters Extraction

```
clear all;

% Creat the omega matrix (2GHz-20GHz)%

k = 2:0.0225:20;

Omega0 = k.*2*pi*10^9;

Omega = Omega0(:);

% Load S parameters of Cold FET Measurement %

load *\S11.txt;

load *\S12.txt;

load *\S21.txt;

load *\S22.txt;

S11 = S11(1:801,1) + 1i.*S11(1:801,2);

S12 = S12(1:801,1) + 1i.*S12(1:801,2);

S21 = S21(1:801,1) + 1i.*S21(1:801,2);

S22 = S22(1:801,1) + 1i.*S22(1:801,2);

% Convert the S parameters to Y parameters %

Z0 = 50; % Ohm %


Y0 = 1/Z0; % Ohm-1 %

Y11 = Y0.* ((1-S11).*(1+S22)+S12.*S21) ./ ((1+S11).*(1+S22)-S12.*S21);

Y12 = Y0.* (-2.*S12) ./ ((1+S11).*(1+S22)-S12.*S21);

Y21 = Y0.* (-2.*S21) ./ ((1+S11).*(1+S22)-S12.*S21);
```

```
Y22 = Y0.* ((1+S11).*(1-S22)+S12.*S21) ./ ((1+S11).*(1+S22)-S12.*S21);

Cbfit = imag(Y12);

Cgspfit =imag(Y11)+2.*imag (Y12);

Cdspfit = imag (Y22)+imag (Y12);

  Cb = -polyfit(Omega,imag (Y12),1);

Cgsp =  polyfit(Omega,(imag (Y11)+2.*imag (Y12)), 1);

Cdsp =  polyfit(Omega,(imag (Y22)+imag (Y12)), 1);

%------Extrinsic Inducatance and Conducatance Extraction----------------%

%-------We should load several data with diferent bias points-----------%

% Creat the omega matrix (2GHz-30GHz)%

n = 2:0.0225:20;

Omega3 = n.*2*pi*10^9;

Omega_2_30GHz = Omega3(:);

Omega_2_30GHz_square = Omega_2_30GHz.^2;

Z0 = 50; % Ohm %

Y0 = 1/Z0; % Ohm-1 %

 load Remeasured\CVD3078\Pt_gate\D1D4\Vg-5_Vd0\S11.txt;

 load Remeasured\CVD3078\Pt_gate\D1D4\Vg-5_Vd0\S12.txt;

 load Remeasured\CVD3078\Pt_gate\D1D4\Vg-5_Vd0\S21.txt;

 load Remeasured\CVD3078\Pt_gate\D1D4\Vg-5_Vd0\S22.txt;

S11_0 = S11(:,1) + 1i.*S11(:,2);

S12_0 = S12(:,1) + 1i.*S12(:,2);

S21_0 = S21(:,1) + 1i.*S21(:,2);
```

```
S22_0 = S22(:,1) + 1i.*S22(:,2);
% 2-----Convert the S parameters to Y parameters %
Y11_0 = Y0.* ((1-S11_0).*(1+S22_0)+S12_0.*S21_0)./ ((1+S11_0).*(1+S22_0)-
S12_0.*S21_0);
Y12_0 = Y0.* (-2.*S12_0) ./ ((1+S11_0).*(1+S22_0)-S12_0.*S21_0);
Y21_0 = Y0.* (-2.*S21_0) ./ ((1+S11_0).*(1+S22_0)-S12_0.*S21_0);
Y22_0= Y0.* ((1+S11_0).*(1-S22_0)+S12_0.*S21_0) ./ ((1+S11_0).*(1+S22_0)-
S12_0.*S21_0);
%Deembed the extrinsic capacitance from Y parameters%
Y11_1 = real(Y11_0)+1i*(imag(Y11_0)-Omega_2_30GHz.*Cgsp(:,1));
Y12_1 = Y12_0;
Y21_1 = Y21_0;
Y22_1 = real(Y22_0)+1i*(imag(Y22_0)-Omega_2_30GHz.*Cdsp(:,1));
%Convert the Y parameters to Z parameters%
Z11_1 = Y22_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);
Z12_1 = -Y12_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);
Z21_1 = -Y21_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);
Z22_1 = Y11_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);

%----------Fitting the Ls Lg Ld Cs Cg Cd----------%
%          Im(wZ11)=w2*(Ls+Lg)-(1/Cs + 1/Cg)          &
%          Im(wZ22)=w2*(Ls+Ld)-(1/Cs + 1/Cd)          %
%          Im(wZ12)=w2*Ls-1/Cs                        %
```

```
%-----------------------------------------------------------%

Ls_fit = imag(Omega_2_30GHz.*Z12_1);

Ls_plus_Ld_fit = imag(Omega_2_30GHz.*Z22_1);

Ls_plus_Lg_fit = imag(Omega_2_30GHz.*Z11_1);

plot(Omega_2_30GHz_square,Ls_fit);

Rs_plus_Rg_fit = Omega_2_30GHz.*real(Z11_1);

Rs_pluse_half_Rch_fit = Omega_2_30GHz.*real(Z12_1);

Rs_Rd_pluse_Rch_fit = Omega_2_30GHz.*real(Z22_1);

Rs_Rg = polyfit(Omega_2_30GHz(399:801), Rs_plus_Rg_fit(399:801), 1);

Rs_half_Rch =  polyfit(Omega_2_30GHz(399:801), Rs_pluse_half_Rch_fit(399:801), 1);

Rs_Rd_Rch = polyfit(Omega_2_30GHz(399:801), Rs_Rd_pluse_Rch_fit(399:801), 1);
```

6.2 Intrinsic Parameters Extraction

```
clear all;

%Input the output parameters%

Cgsp = 17.542*10^(-15); %---unit: F---%

Cdsp = 29.271*10^(-15); %---unit: F---%

  Ls = 8.22*10^(-12); %---unit: H---%

  Lg = 29.76*10^(-12); %---unit: H---%

  Ld = 30.15*10^(-12); %---unit: H---%

  Rs = 9.56;           %---unit: Ohm---%

  Rg = 9.43;           %---unit: Ohm---%

  Rd = 24.14;          %---unit: Ohm---%

% Creat the omega matrix (2GHz-20GHz)
```

```
k = 2:0.0225:20;

Omega0 = k.*2*pi*10^9;

Omega = Omega0(:);

Omega2 = Omega.^2;

freq0 = k.*10^9;

freq = freq0(:);

%Convert the S parameters into Z parameters and exclude the extrinsic parameters%

Z0 = 50;

Y0 =1/Z0;

load Remeasured\CVD3078\Pt_gate\D1D4\Vg-8_Vd6\S11.txt;

load Remeasured\CVD3078\Pt_gate\D1D4\Vg-8_Vd6\S12.txt;

load Remeasured\CVD3078\Pt_gate\D1D4\Vg-8_Vd6\S21.txt;

load Remeasured\CVD3078\Pt_gate\D1D4\Vg-8_Vd6\S22.txt;

S11 = S11(1:801,1) + 1i.*S11(1:801,2);

S12 = S12(1:801,1) + 1i.*S12(1:801,2);

S21 = S21(1:801,1) + 1i.*S21(1:801,2);

S22 = S22(1:801,1) + 1i.*S22(1:801,2);

%Deembed the extrinsic capacitance from Y parameters%

Y11 = Y0.* ((1-S11).*(1+S22)+S12.*S21) ./ ((1+S11).*(1+S22)-S12.*S21);

Y12 = Y0.* (-2.*S12) ./ ((1+S11).*(1+S22)-S12.*S21);

Y21 = Y0.* (-2.*S21) ./ ((1+S11).*(1+S22)-S12.*S21);

Y22 = Y0.* ((1+S11).*(1-S22)+S12.*S21) ./ ((1+S11).*(1+S22)-S12.*S21);

Y11_1 = real(Y11)+1i*(imag(Y11)-Omega.*Cgsp(:,1));
```

```
Y12_1 = Y12;

Y21_1 = Y21;

Y22_1 = real(Y22)+1i*(imag(Y22)-Omega.*Cdsp(:,1));

%Convert the Y parameters to Z parameters%

Z11_1 = Y22_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);

Z12_1 = -Y12_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);

Z21_1 = -Y21_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);

Z22_1 = Y11_1 ./ (Y11_1.*Y22_1-Y12_1.*Y21_1);

%Deembed the extrinsic inductance and resistance from Z parameters%

Z11_2 = Z11_1 - (Rs + Rg) - 1i.*Omega.*(Ls + Lg);

Z12_2 = Z12_1 - Rs - 1i.*Omega.*Ls;

Z21_2 = Z21_1 - Rs - 1i.*Omega.*Ls;

Z22_2 = Z22_1 - (Rs + Rd) - 1i.*Omega.*(Ls + Ld);

%Convert the Z parameters to Y parameters%

Y11_2 = Z22_2./(Z11_2.*Z22_2-Z12_2.*Z21_2);

Y12_2 = -Z12_2./(Z11_2.*Z22_2-Z12_2.*Z21_2);

Y21_2 = -Z21_2./(Z11_2.*Z22_2-Z12_2.*Z21_2);

Y22_2 = Z11_2./(Z11_2.*Z22_2-Z12_2.*Z21_2);

%Extract the intrinsic parameters%

%------Extract Cgs Rgs-----------%

Ygs = Y11_2 + Y12_2;

Dcgs = Omega.*(abs(Ygs)).^2./imag(Ygs);

Cgs = polyfit(Omega2, Dcgs, 1);
```

```
plot(Omega2, Dcgs);

Drgs = real(Omega.*Ygs./imag(Ygs));

Ri_fit = polyfit(Omega2(260:801), Drgs(260:801), 1);

Ri = Ri_fit./Cgs(1:1);

plot(Omega2, Drgs);

%------Extract Cgd Rgd-----------%

Ygd = -Y12_2;

Dcgd = Omega.*(abs(Ygd)).^2./imag(Ygd);

plot(Omega2, Dcgd);

Cgd = polyfit(Omega2, Dcgd, 1);

Drgd = real(Omega.*Ygd./imag(Ygd));

Gfd = - real(Y12_2);

plot(Omega2, Drgd);

Rgd_fit = polyfit(Omega2(504:801), Drgd(504:801), 1);

Rgd = Rgd_fit./Cgd(1:1);

Rgd_2 = real(Y12_2)./(Omega.*Cgd(1:1).*imag(Y12_2));

%-------Extract gm and tau----------%

Ygm = Y21_2 -Y12_2;


Dgm = (abs(Ygs./Ygm)).^2;

plot(Omega2, Dgm);

gm_fit = polyfit(Omega2, Dgm, 1);

gm = Cgs(1:1)./(gm_fit).^(0.5);
```

```
%--------Extract Cds----------------%

Yds = Y22_2 +Y12_2;

Dds = imag(Yds);

Cds = polyfit(Omega, Dds, 1);

Gds_fit = Omega.*real(Yds);

Gds = polyfit(Omega(478:801), Gds_fit(478:801), 1);

plot(Omega, Gds_fit);

plot(Omega, Gfd);

Dtau=asin((imag(Y12_2)-imag(Y21)-Omega.*(-Ri(1:1)).*Cgs(1:1).*(real(Y21)-

real(Y12))).*gm(1:1));

Dtau2 = angle((Ygm./Ygs).*(1/5000 +1i.*Omega.*Cgs(1:1)));

plot(Omega, Dtau);

tau = polyfit(Omega(1:337), Dtau(1:337), 1);

Ft=1./(2.*pi.*((Cgs(1:1)+Cgd(1:1))./gm(1:1)+(Rs+Rd).*(Cgs(1:1)+Cgd(1:1))./(gm(1:1).*

(1/Gds(1:1)))+(Rs+Rd).*Cgd(1:1)));

fT_int = 1./(2.*pi.*((Cgs(1:1)+Cgd(1:1))./gm(1:1)));
```

7 References

[1] H. Morkoç, Handbook of Nitride Semiconductors and Devices (Wiley, Weinheim, 2008), Vol. II, Chapter III.

[2] J. Xie, X. Ni, M. Wu, J. H. Leach, Ü. Özgür, H. Morkoç, “High electron mobility in nearly lattice-matched AlInN/AlN/GaN heterostructure field effect transistors”, Appl. Phys. Lett., vol. 91, pp. 132116, SEP. 2007.

[3] Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, U. K. Mishra, “Very-High Power Density AlGaN/GaN HEMTs”, IEEE Trans. Elec. Dev., vol. 48, pp. 1438-1440, MAR. 2001.

[4] N. Q. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, T. P. Ma, "Kilovolt AlGaN/GaN HEMT", Phys. Stat. Solidi. (a), vol. 188, pp. 213-217, NOV 2001.

[5] T. Palacios, A. Chakraborty, S. Rajan, C, Pablenz, S. Keller, S. P. DenBaars, J. S. Speck, U. K. Mishra, "High-power AlGaN/GaN HEMTs for Ka-band applications", IEEE Elec. Dev. Lett., vol. 26, pp. 781-783, NOV 2005.

[6] H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J. -F, Carlin, M. Gonschorek, N. R. Grandjean, C. R. Bolognesi, "205GHz (Al,In)N/GaN HEMTs", IEEE Elec. Dev. Lett., vol. 31, pp. 957-959, SEP 2010.

[7] R. Wang, G. Li, O. Laboutin, C. Yu, W. Johnson, G. Snider, P. Fay, D. Jena, H. Xing, "210-GHz InAlN/GaN HEMTs With Dielectric-Free Passivation", IEEE Elec. Dev. Lett., vol. 32, pp. 892-894, JUL 2011.

[8] H. Morkoç, Handbook of Nitride Semiconductors and Devices (Wiley, Weinheim, 2008), Vol. I.

[9] O. Ambacher,J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures", J. Appl. Phys., vol. 85, pp. 3222-3233, MAR 1999.

[10] J. Kuzmik, "Power electronics on InAlN/(In)GaN: Prospect for a record performance", IEEE Elect. Dev. Lett., vol.22, pp.510-512, 2001.

[11] H. Akinaga, S. Nemeth, J. De Boeck, L. Nistor, H. Bender, G. Borghs, H. Ofuchi, M. Oshima, "Growth and characterization of low-temperature grown GaN with high Fe doping", Appl. Phys. Lett., vol. 77, pp. 4377-4379, DEC 2000.

[12] Z. Fan, S. N. Mohammad, W. Kim. Ö. Aktaş, A.E. Botchkarev, and H. Morkoç, “Very low resistance multilayer Ohmic contact to n-GaN”, Appl. Phys. Lett., vol. 68, pp. 1672, JAN 1996.

[13] N. Chaturvedi, U. Zeimer, J. Wurfl and G. Trankle, “Mechanism of ohmic contact formation inAlGaN/GaN high electron mobility transistors” Semiconductor Science and technology, Vol. 21,pp. 175-179, FEB 2006.

[14] H. H. Berger, “Models for contacts to planar devices”, Solid State Electronics, 15, 145, (1972)

[15] J Kuzmik, "InAlN/(In)GaN high electron mobility transistors: some aspects of the quantum well heterostructure proposal", Semicond. Sci. Technol., vol. 17, pp.540-544, MAY 2002.

[16] Guowang Li, Yu Cao, Huili Grace Xing, and Debdeep Jena, "High mobility two-dimensional electron gases in nitride heterostructures with high Al composition AlGaN alloy barriers", Appl. Phys. Lett., 97, vol. 97, pp. 222110, NOV 2010.

[17] J. Kuzmik, "Power electronics on InAlN/(In)GaN: Prospect for a record performance", IEEE Elect. Dev. Lett., vol.22, pp.510-512, 2001.

[18] K. Jeganathan, M. Shimizu, H. Okumura, Y. Yano, N. Akutsu, "Lattice-matched InAlN/GaN two-dimensional electron gas with high mobility and sheet carrier density by plasma-assisted molecular beam epitaxy", J. Cryst. Growth, vol. 304, pp. 342-345, MAR 2007.

[19] Y. Awano, M. Kosugi, K. Kosemura, T. Mimura, and M. Abe, “Shortchannel effects in subquarter micrometer-gate HEMTs: Simulation and experiment,” IEEE Trans. Elect. Dev., vol. 36, no. 10, pp. 2260–2266, OCT 1989.

[20] G. H. Jessen, R. C. Fitch, J. K. Gillespie, G. Via, A. Crespo, D. Langley, D. J. Denninghoff, M. Trejo, and E. R. Heller, “Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-Gate devices,” IEEE Trans. Electron Devices, vol. 54, no. 10, pp. 2589– 2597, OCT 2007.

[21] Naiqian Zhang, “High voltage GaN HEMTs with low on-resistance for switching applications”, PhD Dissertation, pp. 27, SEP 2002.

[22] A. Crespo, M. M. Bellot, K. D. Chabak, J. K. Gillespie, G. H. Jessen, V. Miller, M. Trejo, G. D. Via, D. E. Walker, Jr., B. W. Winningham, H. E. Smith, T. A. Cooper, X. Gao, and S. Guo, "High-Power Ka-Band Performance of AlInN/GaN HEMT With 9.8-nm-Thin Barrier", IEEE Elect. Dev. Lett. vol. 31, pp. 2-4, JAN 2010.

[23] M. Azize, Z. Bougriouaa, and P. Gibart, “Inhibition of interface pollution in AlGaN/GaN HEMT structures regrown on semi-insulating GaN templates”, J. Cryst. Growth, vol. 299, pp. 103-108, JAN 2007.

[24] J. P. Liu, J.-H. Ryou, D. Yoo, Y. Zhang, J. Limb, C. A. Horne, S.-C. Shen, R. D. Dupuis, A. D. Hanser, E. A. Preble, and K. R. Evans, "III-nitride heterostructure field-effect transistors grown on semi-insulating GaN substrate without regrowth interface charge", Appl. Phys. Lett., vol. 92, pp. 133513-133513, MAR 2008.

[25] T. Paskova and K. R. Evans, “GaN Substrates-Progress, Status, and Prospects”, IEEE J. Sel. Top. Quantum Electron. , vol. 15, pp. 1041-1052, AUG 2009.

[26] D. Albrecht, P. P. Ruden, S. C. Binari, and M. G. Ancona, “AlGaN/GaN heterostructure field-effect transistor model including thermal effects”, IEEE Trans. Elect. Dev., vol. 47, pp.2031, NOV 2000.

[27] Z. Chen, Y. Pei, S. Newman, R. Chu, D. Brown, R. Chung, S. Keller, S. P. DenBaars, S. Nakamura, U. K. Mishra, “Growth of AlGaN/GaN heterojunction field effect transistors on semi-insulating GaN using an AlGaN interlayer”, Appl. Phys. Lett., vol. 94, pp. 112108 MAR 2009.

[28] S. Abermann, G. Pozzovivo, J. Kuzmik, C. Ostermaier, C. Henkel, O. Bethge, G. Strasser, D. Pogany, J.-F. Carlin, N. Grandjean and E. Bertagnol, “Current collapse reduction in InAlN/GaN MOS HEMTs by in situ surface pre-treatment and atomic

layer deposition of ZrO2 high-k gate dielectrics", IEEE Elect. Lett., vol. 45, pp. 570 MAY 2009.

[29] J. Kuzmik, A. Kostopoulos, G. Konstantinidis, J.-F. Carlin, A. Georgakilas, and D. Pogany, "InAlN/GaN HEMTs: a first insight into technological optimization", IEEE Trans. Elec. Dev., vol.53, pp.422, MAR 2006.

[30] K. Suzue, S. N. Mohammad, Z. F. Fan, W. Kim, O. Aktas, A. E. Botchkarev, H. Morkoç, "Electrical conduction in platinum-gallium nitride Schottky diodes", J. Appl. Phys., vol. 80, pp. 4467, OCT 1996.

[31] G. Pozzovivo,J. Kuzmik, S. Golka, W. Schrenk, G. Strasser, D. Pogany, K. Čičo, M. Ťapajna, K. Fröhlich, J.-F. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, "Gate insulation and drain current saturation mechanism in InAlN/GaN metal-oxide-semiconductor high-electron-mobility transistors", Appl. Phys. Lett., vol. 91, pp. 043509, JUL 2007.

[32] A. Dadgar, F. Schulze, J. Bläsing, A. Diez, A. Krost, M. Neuburger, E. Kohn, I. Daumiller, M. Kunze, "High-sheet-charge–carrier-density AlInN/GaN field-effect transistors on Si(111)", Appl. Phys. Lett., vol. **85**, pp. 5400, OCT 2004.

[33] Dong Seup Lee, Jinwook W. Chung, Han Wang, Xiang Gao, Shiping Guo, Patrick Fay, and Tomás Palacios, "245GHz InAlN/GaN HEMTs with oxygen plasma treatment", IEEE Elect. Dev. Lett., vol. 32, pp. 755-758, JUN 2011.

[34] Ronghua Wang, Guowang Li, Oleg Laboutin, Yu Cao, Wayne Johnson, Gregory Snider, Patrick Fay, Debdeep Jena, Member, IEEE, and Huili (Grace) Xing, "210GHz InAlN/GaN HEMTs with dielectric free passiavtion", IEEE Elect. Dev. Lett., vol. 32, pp. 892-895, JUL 2011.

[35] N. Moll, M.R. Hueschen, and A. Fischer-Colbrie, "Pulsed-doped AlGaAs/InGaAs pseudomorphic MODFETs," IEEE Trans. Elec. Dev. Vol. 35, no. 7, pp. 879-886, JUL 1988.

[36] B. K. Ridley, "The LO phonon lifetime in GaN," J. Phys.: Condens. Matter, vol. 8, no. 37, pp. L511–L513, SEP. 1996.

[37] G. P. Srivastava, BOrigin of the hot phonon effect in group-III nitrides,[Phys. Rev. B, vol. 77, no. 15, pp. 155205/1–155205/6, Apr. 2008.

[38] A. Dyson, and B. K. Ridley, "Hot phonon-plasmon modes in GaN", Appl. Phys. Lett., vol. 108, pp. 104504, 2010.

[39] K.T. Tsen, J.G. Kiang, D.K. Ferry, and H. Morkoç, "Subpicosecond time-resolved Raman studies of LO phonons in GaN: Dependence on photoexcited carrier density," Appl. Phys. Lett., vol. 89, pp. 112111, SEP 2006.

[40] A. Dyson, and B. K. Ridley, "The lifetime of optical phonon scattering in a single heterostucture", J. Appl. Phys., vol. 109, pp. 054509, MAR 2011.

[41] E. Sermuksnis, J. Liberis, and A. Matulionis, "Microwave noise technique for the measurement of hot-electron energy relaxation time and hot-phonon lifetime," Lithuanian J. Phys,. vol. 47, no. 4, pp. 491-498, 2007.

[42] A. Matulionis and H. Morkoc¸, "Hot phonons in InAlN/AlN/GaN heterostructure 2DEG channels," in Proc. SPIE Conf. Photonics West 7216, Gallium Nitride

Materials and Devices IV, vol. 7216, H. Morkoc¸, C. W. Litton, J.-I. Chyi, Y. Nanishi, J. Piprek, and E. Yoon, Eds., Bellingham, WA, Feb. 2009, vol. 7216, pp. 721608/1–721608/14SPIE.

[43] A. Matulionis, “GaN-based two-dimensional channels: hot-electron fluctuations and dissipation,” J. Phys: Condens. Matter 21, 174203 (2009).

[44] Arvydas Matulionis, Juozapas Liberis, Ilona Matulioniene˙, Mindaugas Ramonas, and Emilis Sermuksnis, "Ultrafast Removed of LO-mode heat from a GaN-based two-dimensional channel,"Proceeding of The IEEE, vol. 98, no. 7, pp. 1118-1125, JUL 2010

[45] A, Matulionis and 1, Matulioniene, "Accumulation of hot phonons in GaN and related structures" in Gallium Nitride Materials and Devices II, edited by H, Morkog and C, W, Litton, Proc SPIE, vol. 6473, pp. 64730P-1-15, JAN 2007

[46] A. Matulionis, J. Liberis, I. Matulioniene, E. Sermuksnis, J. H. Leach, M. Wu, and H. Morkoc¸"Novel fluctuation-based approch to optimization of frequency perfromance and degradation of nitride heterostructure field effect transistors", Phys. Status. Solidi. A, vol. 208, no. 1, pp. 30-36, NOV 2010.

[47] A. Matulionis, J. Liberis, I. Matulionienė, M. Ramonas, E. Šermukšnis, J.H. Leach, M. Wu, X. Ni, X. Li, and H. Morkoç, “Plasmon-enhanced heat dissipation in GaN-based two-dimensional channels”, Appl. Phys. Lett., vol. 95, pp. 192102, NOV 2009.

[48] J.H. Leach, C.Y. Zhu, M. Wu, X. Ni, X. Li, J. Xie, Ü. Özgür, H. Morkoç, J. Liberis, E. Šermukšnis, A. Matulionis, T. Paskova, E. Preble, and K.R. Evans, “Effect of hot phonon lifetime on electron velocity in InAlN/AlN/GaN HFETs on bulk GaN substrates,” Appl. Phys. Lett., vol. 96, pp.133505, MAR 2010.

[49] N. Moll, M. R. Hueschen, and A. Fischer-Colbrie, IEEE Trans. Electron Devices 35, 879 (1988).

[50] B. Hughes and P. J. Tasker, “Bias dependence of the MODFET intrinsic model elements values at microwave frequencies,” IEEE Trans. Electron Devices, vol. 36, No. 10, pp. 2267–2273, Oct. 1989.

[51] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, “A new method for determining the FET small-signal equivalent circuit”, IEEE Trans. Microw. Theory Tech., vol. 36, No. 7, pp. 1151-1159, Jul. 1988.

[52] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, “Surface-related drain current dispersion effects in AlGaNGaN HEMTs,” IEEE Trans. Electron Devices, vol. 51, No. 10, pp. 1554-1561, Oct. 2004.

[53] A. E. Parker and J. G. Rathmell, “Broad-band characterization of FET self-heating,” IEEE Trans. Microw. Theory Tech., vol. 53, No. 7, pp. 2424-2429, Jul. 2005.

[54] J. Burm, W. J. Schaff, L. F. Eastman, H. Amano, and I. Akasaki, “An improved small-signal equivalent circuit model for III-V nitride MODFET’s with large contact resistances,” IEEE Trans. Electron Devices, vol. 44, no. 5, pp. 906-907, May 1997.

[55] A. Jarndal and G. Kompa, “A new small-signal modeling approach applied to GaN devices,” IEEE trans. Microw. Theory Tech., vol. 53, no. 11, pp. 3440-3448, Nov. 2005.

[56] S. Nuttinck, E. Gebara, J. Laskar, J. Shealy, and M. Harris, “Improved RF modeling techniques for enhanced AlGaN/GaN HFETs,” IEEE Trans. Microw. Wireless Compon. Lett. vol. 13, no. 4, pp. 140-142, Apr. 2003.

[57] E.Chigaeva, W. Walthes, D. Wiegner, M. Grözing, F. Schaich, N. Wieser, and M. Berroth, O. Breitschadel, L. Kley, B. Kuhn, F. Scholz, H. Schweizer, O. Ambacher, and J. Hilsenbech,“Determination of small-signal parameters of GaN-based HEMTs,” in Proc. 2000 IEEE/Cornell Conf. High Performance Dev., pp. 115-122, Aug. 2000

[58] G. Chen, V. Kumar, R. Schwindt, and I. Adesida, “A reliable low gate bias model extraction procedure for AlGaN/GaN HEMTs,” IEEE MTT-S Int. Microw. Symp., pp. 1097-1100, Jun. 2006.

[59] R. G. Brady, C. H. Oxley, and T. J. Brazil, “An improved small-signal parameter-extraction algorithm for GaN HEMT devices,” IEEE Tran. Microw. Theory Tech., vol. 56, no. 7, pp. 1535-1544, Jul. 2008.

[60] W. Liu, Fundamentals of III-V devices: HBTs, MESFETS, and HFETs/HEMTs, New York: Wiley, 1999.

[61] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," IEEE Trans. Microw. Theory Tech., vol. 36, no. 7, pp. 1151–1159, JUL 1988.

[62] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," IEEE Trans. Microw. Theory Tech., vol. 38, no. 7, pp. 891–895, JUL 1990.

[63] G. L. Bilbro and R. J. Trew, Electron. Lett., 42, 1425, (2006).

[64] A. Koudymov, M. S. Shur, and G. Simin, IEEE Electron Device Lett., 28, 332(2007).

[65] Chris Roff,Johannes Benedikt, Paul J. Tasker, David J. Wallis, Keith P. Hilton, Jessica O. Maclean, David G. Hayes, Michael J. Uren, Trevor Martin, IEEE Trans. Elec. Dev., 56, 13(2009).

[66] Rongming Chu, Yigang Zhou, Jie Liu, Deliang Wang, Kevin J. Chen and Kei May Lau, IEEE Transaction on Electron Devices, 52, 438 (2005).

[67] P. Waltereit, O. Brandt, A. Trampert, H. T. Grahn, J. Menniger, M. Ramsteiner, M. Reiche and K. H. Ploog, "Nitride semiconductors free of electrostatic fields for efficient white light-emitting diodes", Nature, vol. 406, pp. 865-868, AUG 2000.

[68] C.Q. Chen, J. P. Zhang, J. W. Yang, V. Adivarahan, S. Rai, S. Wu, H. M. Wang, W. H. Sun, M. Su, Z. Gong, E. Kuokstis, M. Gaevski, M. A. Khan, "A new selective area lateral epitaxy approach for depositing a-plane GaN over r-plane sapphire", Jpn. J. Appl. Phys., vol. 42, pp. L818-L820, JUL 2003.

[69] X. Ni, Ü. Özgür, A. A. Baski, and H. Morkoç, Lin Zhou, David J. Smith and C. A. Tran, "Epitaxial lateral overgrowth of (11-22) semipolar GaN on (1-100) m-plane sapphire by metalorganic chemical vapor deposition", Apply. Phys. Lett., vol. 90, pp.182109, MAY 2007.

[70] T. Tanikawa, D. Rudolph, T. Hikosaka, Y. Honda, M. Yamaguchi, and N. Sawaki, "Growth of non-polar (11-20)GaN on a patterned (110)Si substrate by selective MOVPE", J. Cryst. Growth, vol.310, pp.4999, NOV 2008.

[71] N. Suzuki, T. Uchida, T. Tanikawa, T. Hikosaka, Y. Honda, M. Yamaguchi, N. Sawaki, "HVPE growth of semi-polar (11-22) GaN on GaN template Si (113) substrate", J. Cryst. Growth, vol. 311, pp.2875-2878, MAY 2009.

[72] M A Gosalvez, Prem Pal, and K Sat, "Reconstructing the 3D etch rate distribution of silicon in anisotropic etchants using data from vicinal {1 0 0}, {1 1 0} and {1 1 1} surfaces", J. Micromech. Microeng., vol. 21, pp. 105018, AUG 2011.

[73] T. Lei, M. Fanciulli, R. J. Molnar, T. D. Moustakas, R. J. Graham, and J. Scanlon, “Epitaxial growth of zinc blende and wurtzitic gallium nitride thin films on (001) silicon”, Appl. Phys. Lett., vol. 59, pp. 944 , JUN 1991.

[74] B. Yang, A. Tampert, O. Brandt, B. Jenichen, and K. H. Ploog, “Structural properties of GaN layers on Si(001) grown by plasma-assisted molecular beam epitaxy”, J. Appl. Phys., vol. 83, pp. 3800, SEP 1998.

[75] Y. Honda, N. Kameshiro, M. Yamaguchi, N. Sawaki, “Growth of ($1\bar{1}01$) GaN on a 7-degree off-oriented (0 0 1)Si substrate by selective MOVPE”, J. Cryst. Growth, vol. 242, pp. 82–86, JUL 2002.