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Nanowire Zinc Oxide MOSFET Pressure Sensor

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NANOWIRE ZINC OXIDE MOSFET PRESSURE SENSOR

A research dissertation submitted in partial satisfaction of the requirements for the degree of Master of Science in Electrical Engineering.

by

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Bachelors of Science in Electrical Engineering, Virginia Commonwealth University, 2011

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Virginia Commonwealth University
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Abstract

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Fabrication and characterization of a new kind of pressure sensor using self-assembly Zinc Oxide (ZnO) nanowires on top of the gate of a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is presented. Self-assembly ZnO nanowires were fabricated with a diameter of 80 nm and 800 nm height (80:8 aspect ratio) on top of the gate of the MOSFET. The sensor showed a 110% response in the drain current due to pressure, even with the expected piezoresistive response of the silicon device removed from the measurement. The pressure sensor was fabricated through low temperature bottom up ultrahigh aspect ratio ZnO nanowire growth using anodic alumina oxide (AAO) templates. The pressure sensor has two main components: MOSFET and ZnO nanowires. Silicon Dioxide growth, photolithography, dopant diffusion, and aluminum metallization were used to fabricate a basic MOSFET. In the other hand, a combination of aluminum anodization, alumina barrier layer removal, ZnO atomic layer deposition (ALD), and wet etching for nanowire release were optimized to fabricate the sensor on a silicon wafer. The ZnO nanowire fabrication sequence presented is at low temperature making it compatible with CMOS technology.

Chapter 1 Introduction

A sensor is a device that converses nonelectrical physical or chemical quantities into electrical signal. This signal can be read by an observer or by an electronic instrument. They help electronics to have an interface with the real world. Sensor have become an essential element of process control and analytical measurement systems. There are innumerable applications for sensors of which most people are never aware. Applications include, for example, industrial monitoring, factory automation, the automotive industry, transportation, telecommunications, computers and robotics, environmental monitoring, health care, and agriculture; in other words, sensors are in all spheres of our life [1].

Rapid progress in semiconductor technology, involving microcomputers and VLSI (Very Large System Integration) has increased the capabilities of electronic equipment used in industry. New products and companies have emerged to develop an integration of sensors with electronic equipment [2]. This has stimulated sensor devices to development new kind of technology in sensor applications. There are different physical and chemical quantities in nature. For that reason sensor technology could be classified as thermal, mechanical, chemical, magnetic and radiant [3]. Sensors could be also be divided in two categories depending on whether they use auxiliary source or not. First, self-generating or passive sensing systems are devices that do not require an auxiliary source. Second, modulating or active sensors generate an output signal with the help of an auxiliary force.

A sensing system has three basic components. First, the input transducer is responsible to sense the outside world, and to gather information about a physical or chemical quantity. Second, signal processing is requires since the input signal is usually

weak and it needs some kind of signal amplifier before going to the actuator. Third, actuator gets the signal from the signal processing block and it converts it into some kind of action. Figure 1.1 shows a simple block diagram of a sensing system. The main goal of a sensing system is to making it smart where electrical signals created by the sensors are amplified, converted to digital form, and then transferred to a microprocessor all in one single chip.

Figure 1.1: Block diagram of a sensing system.

The global market for sensor systems was estimated at $56.3 billion in 2010 [4]. The sensor industry growth looks very promising for the future with an expected compound annual growth rate of 7.8% to nearly $91.5 billion by 2016. A very promising type of sensing system is the pressure sensor technology. The market is currently nominated by piezoresistive and capacitive sensor which are heavily used in automotive, medical, and petrochemical applications. New pressure sensor technology is been extended to automotive and medical application due to improved sensitivity. The market size for pressure sensor was about $5.11 billion in the year 2011, and it is expected to reach $7.34 billion by 2017 [5]. Vehicle production in emerging markets, government regulations, gradual reduction in size, and the fast growth of Asian economies are the factor that are contributing to the fast growth of market size of pressure sensors.

Most of pressure sensors are manufactured by a combination of mechanical and electrical components. The work presented in this thesis goes over the details of nanowire ZnO (Zinc Oxide) MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) pressure sensor. This nanowire pressure sensor has two basic electromechanical

components: 1) MOSFET device, and 2) ZnO Nanowires. Once established in a biased state and with a conducting channel, the MOSFET device will sense the bending of the ZnO nanowires due to additional mechanical pressure on top of them. Figure 1.2 shows the two main electrical components of the pressure sensor. The following section will explain basic concepts about the two components of the sensor.

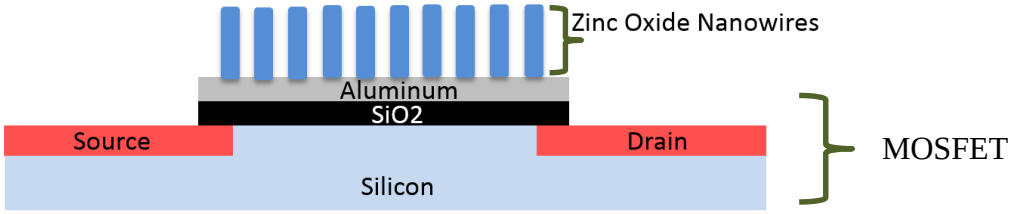


Figure 1.2: Pressure sensor description. ZnO NW on gate of a MOSFET device

1.2 MOSFET Basics

Of all technologies made by mankind, the MOSFET is one of the most frequently used. A MOSFET is a transistor used for amplifying or switching electronic signals. There are millions of MOSFETs in computers, cellphones, game consoles, basically anywhere where information is processed and stored. Digital information and logic can be processed by states in a MOSFET device as well as analog electrical circuits and signals. In simple terms, there is conducting channel formed and a flow of current during the ON state of a MOSFET when a voltage is applied to the gate [6]. When the voltage on the gate is removed, the conducting channel is removed and the current flow stop between the drain and source. This flow of current goes from the source and drain, and can also be modulated by the voltage applied to the gate. With the MOSFET in the ON state, small changes in the voltage applied to the gate produce corresponding larger changes in the magnitude of the drain current.

For a fixed applied voltage between the source and drain (V_D), the relationship between the drain current (I_D) and the applied gate voltage (V_G) is given by Eqn. 1.1, where μ_n is the charge-carrier effective mobility, W is the gate width, L is the gate length, C_{OX} is the gate oxide capacitance per unit area, and V_T is the threshold voltage.

$$I_D = \mu_n C_{OX} \frac{W}{L} \left[V_G - V_T - \frac{V_D}{2} \right] V_D \qquad (1.1)$$

A simple metal gate MOSFET, manufactured on a silicon substrate is illustrated in Fig. 1.3. The gate is responsible to allow the flow of current between terminals. This gate is usually made of a highly conducting material and it is separated from the semiconductor by a thin insulator layer, the gate dielectric. If sufficient voltage is applied to the gate (called the threshold voltage V_T), a channel is formed under the gate insulator, connecting the source and drain. MOSFETs can be of two types: NMOS or PMOS. In the case of NMOS, the source and drain are doped n-type, while the substrate is doped p-type, and vice-versa for PMOS. In NMOS, the channel is formed by electrons and the flow of current is due to the flow of these electrons between the source and the drain. In the case of the PMOS, the channel and drain current will be induced due to the flow of holes.

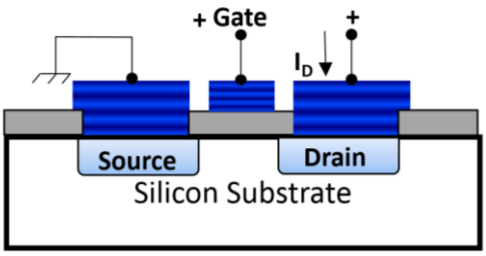


Figure 1.3: Typical Silicon MOSFET.

The drain current in a MOSFET is a function of both the applied gate voltage (V_G), and the magnitude of the drain to source voltage (V_D), as given by Equation. (1.1). This

relationship can be used to characterize the operation of a MOSFET, by generating a family of curves, showing the drain current I_D as a function of the drain to source voltage (V_D) as a function of the applied gate voltage V_G. A typical I_D vs. V_D characteristic for an NMOS transistor is shown in Figure 1.4.

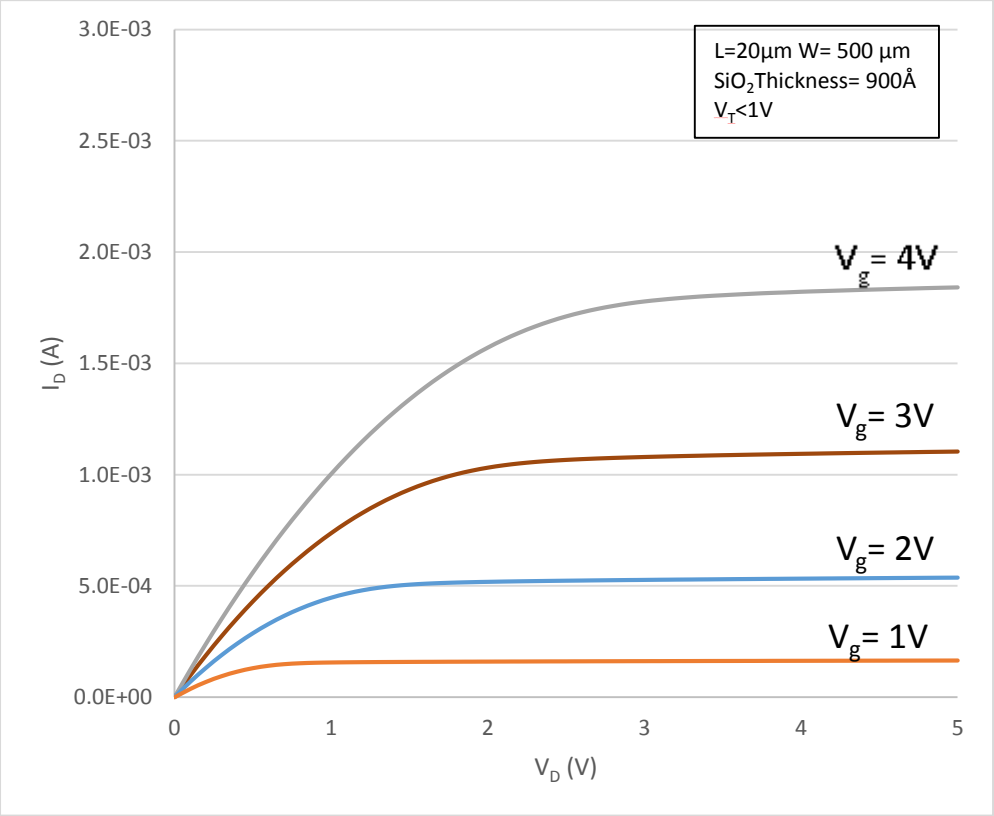


Figure 1.4: NMOS I_D vs V_D.

CMOS (Complementary Metal-Oxide Semiconductor) technology uses both types of transistors on the same type of substrate. The basic structure is that these two type of transistors behave as a pair of switches that act in a complementary form. Modern computer chips, memory and digital circuits are manufactured by the combination of billions of these type of structures.

1.3 Piezoelectricity

A piezoelectric material converts mechanical energy into electrical energy (Direct piezoelectric effect – Sensing), and vice versa (Inverse piezoelectric effect – Actuation) [7]. It was discovered by Jacque and Pierre Curie in 1880. It is a type of transducer which has electromechanical interaction between its mechanical and electrical state. Piezoelectric elementary cells change dimensions when an electric potential is applied. The most common piezo actuators consist of stacks of thin piezoelectric ceramic layers that extend when a voltage is applied. These stacks produce high forces and very short response times. In the other hand, shear actuators produce lateral motion that make a very compact XY positioners when stacked together [8].

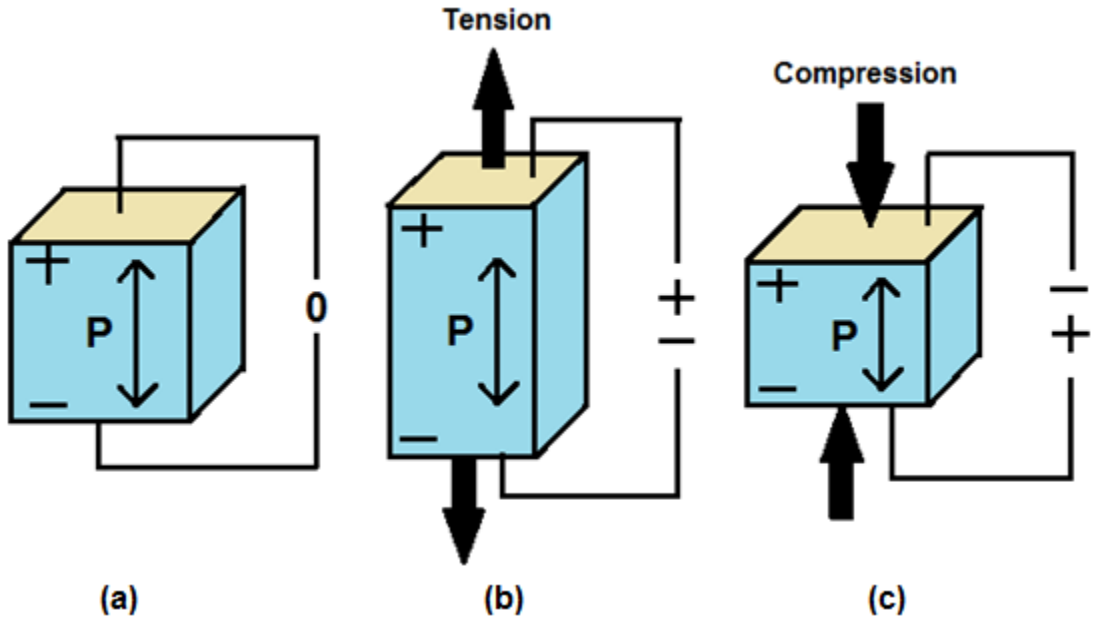


Figure 1.5: Schematic of direct piezoelectric effect; (a) piezoelectric material, (b) energy generation under tension, (c) energy generation under compression [9].

Some crystals (e.g. crystalline SiO_2 and $BaTiO_3$) become polarized when they are mechanically stressed which produces surface charges with a voltage difference between the two surfaces of the crystal. The same type of crystal could exhibit a strain or mechanical

distortion when they experience an electric field. The extension or compression of the piezoelectric material depends on the direction of the applied field or the polarity of the applied voltage.

The crystallographic structure of the solid determines if the material exhibits piezoelectric properties. A piezoelectric material does not have a center of inversion symmetry. In the case of direct piezoelectric effect, an array of aligned electric dipoles is created within the structure. That is the case of ZnO. The voltage generated (V) from a piezoelectric material can be calculated using Eqn 1.2, where S_v is the voltage sensitivity of the material, P is the pressure, and D is the thickness of the material [cite].

$$V = S_V * P * D \qquad (1.2)$$

The sensitivity values, S_v, depend on the material and different geometry cuts, and it is characterized by the charge sensitivity coefficient (d_{ij}). Eqn. 1.3 relates the amount of voltage generated from a force perpendicular to the plane, where $\Delta\sigma_j$ is the applied force, z is the distance of the applied force, ε_r is the relative permittivity, ε_o is the permittivity of free space.

$$\Delta V = \frac{d_{ij}\Delta\sigma_j z}{\varepsilon_r \varepsilon_o} \qquad (1.3)$$

In the case of ZnO, the charge sensitivity, S_v is 246 pC/N along the c axis of the crystal, for the pressure and voltages measured along this same axis.

In this work, a MOS transistor is fabricated with piezoelectric ZnO nanowires on top of the metal gate, in order to produce a novel pressure sensor. The nanowires process is a novel, low temperature fabrication process that can be readily integrated with MOS technology. With the MOS transistor biased into an ON state, it is expected that there will be a response in the drain current due to the added potential generated by pressure on the

ZnO nanowires fabricated on the NMOS gate contact. Figure 1.6 shows the two electronic components of the pressure put together. It shows the direction of the direction of the mechanical pressure on the ZnO nanowires, as well as the different terminals of the MOSFET device.

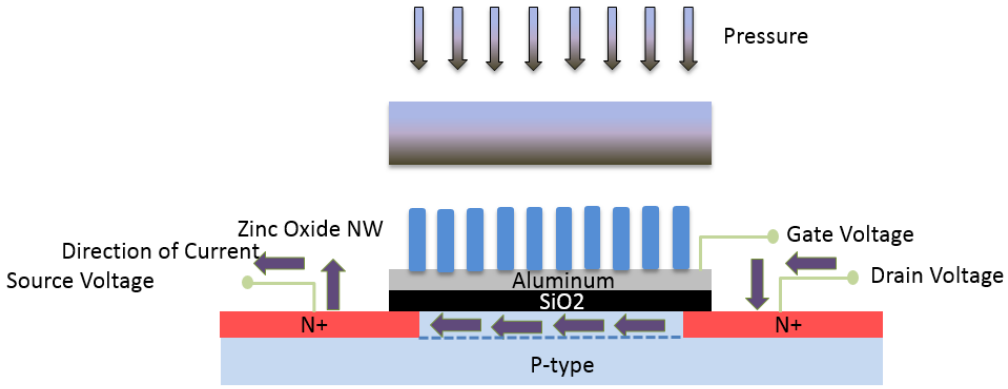


Figure 1.6: Description of the two components of the nanowire ZnO pressure sensor.

It is important to note that there is a response to pressure in the drain current due to two factors during the operation of the pressure sensor: 1) Piezoresistance coming from the silicon substrate. 2) Piezoelectricity coming from the of the ZnO nanowires. The main purpose of the ZnO nanowires is to improve the sensitivity of the device. It may also be possible to demonstrate a shear response to horizontal stress on the nanowires.

The ultimate goal of my project was demonstrate a versatile fabrication sensor technology that could be integrated with more complex CMOS digital and analog technology for the application to portable and mobile sensing technology. The following sections will explain with detail all the fabrication, and proof-of-concept of the nanowire ZnO MOSFET pressure sensor.

Chapter 2 MOSFET Design and Fabrication

Overview:

The final objective of this work is to have a clear understanding of how Zinc Oxide nanowire attached to the gate of a MOSFET behave due to a pushing mechanical force. To do that, NMOS and PMOS transistors were fabricated on a 4 inch silicon wafer. Different gates and transistors sizes were designed. PMOS's length were designed larger than in the case of the NMOS because of the different fall times during pull-up and pull-downs in the operation of the transistor. Body contact were also added to the layout of the transistors to ensure that there is no body bias present to affect the threshold voltage of the device. Each wafer contained 13 dies with PMOS and NMOS transistors, 2 dies with large geometry size transistors, 1 die with a set of 3 ring oscillators, and 4 dies with test structures. PMOS were fabricated on an N-type wafer and NMOS were fabricated on a P-type wafer with different photo masks. There were two metal mask that were used, one with pattern to characterize the transistor with nanowires and other mask to characterize the transistors without the nanowires.

2.1 Design Calculations

It was intended to design MOSFETS with 3µm, 5µm, 20µm, and 50µm physical gate widths of the transistors. These were chosen because 3µm - 5 µm is the minimum gate width that could be fabricated with the equipment in the VMC lab. The 20 µm and 50 µm gate widths will give added room for error if the previous transistors fail (the larger devices should be the easiest to fabricate). It is desirable to have the smallest possible devices on a wafer because the transistors can be packaged and used in an integrated circuit in a

microchip, and obviously the smaller the chip the better. Gate lengths are different in each die, the width remained constant. Another difference from die to die is the alignment tolerance and the transistor spacing. There were 4 dies with test structures such as resistors, capacitors, contact chains, and Van der Pauw for p-type and n-type diffusion characterization. Table 2.1 shows a summary of the difference between dies.

Die to Die Differences					
	Die #1	Die #2	Die #3	Die #4	Die #5
Devices	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters
Gate Widths (µm)	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50
Alignment Tolerance (µm)	25	25	25	5	5
Transistor Spacing (µm)	50	50	50	50	50
	Die #6	Die #7	Die #8	Die #9	Die #10
Devices	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters
Gate Widths (µm)	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50
Alignment Tolerance (µm)	5	1	1	1	25
Transistor Spacing (µm)	50	50	50	50	150
	Die #11	Die #12	Die #13	Die #14	Die #15
Devices	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters	Transistors, Inverters
Gate Widths (µm)	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50
Alignment Tolerance (µm)	25	25	5	5	5
Transistor Spacing (µm)	150	150	150	150	150
	Die #16	Die #17	Die #18	Die #19	Die #20
Devices	Transistors, Invertors	Transistors, Invertors	Transistors, Invertors	Transistors	Invertors
Gate Widths (µm)	3, 5, 20, 50	3, 5, 20, 50	3, 5, 20, 50	105	175
Alignment Tolerance (µm)	1	1	1	105	50
Transistor Spacing (µm)	150	150	150	100	100
	Die #21	Die #22	Die #23	Die #24	Die #25
Devices	Ring Oscillators w/Body	Test Structures 1	Test Structures 1	Test Structures 2	Test Structures 2
Gate Widths (µm)	20	N/A	N/A	N/A	N/A
Alignment Tolerance (µm)	25, 5, 1	N/A	N/A	N/A	N/A
Transistor Spacing (µm)	50	N/A	N/A	N/A	N/A

Table 2.1: Wafer design. Die to die Differences.

In order to fabricate working NMOS and PMOS structures, there are five basic design features that needed to be considered: gate length and width, threshold voltage, channel doping level, source and drain doping levels, and the gate oxide thickness. Because

one of the goals of the project was to design a working FET, the first design parameter that was calculated was the threshold voltage. It was important that the threshold voltage was in a measurable range because the ZnO nanowire were expected to produce a relative low potential and it should be detectable with the parameter analyzer. Ideally, the threshold voltage would be somewhere between 1V and 2 V because that is half of the bias voltage. It was then decided that a threshold voltage of 0.5V was the minimum acceptable value for the operation of the MOSFET device. The next variable needed to calculate the oxide thickness was the doping concentration of the channel. In the case of PMOS, an N-type wafer with a resistivity of roughly of 10 Ω-cm. which leads to a surface concentration of $1.5x10^{15}$ atoms/cm^3. In the case of NMOS, P-type wafers with a resistivity of 10 Ω-cm lead to a surface concentration of 8E14 atoms/cm^3. Originally, Eqn. 2.1 was used to calculate the threshold voltage, however it didn't account for higher order effects so Athena and Atlas were used to simulate for the threshold voltage to obtain a more accurate result. After adding room for non-ideal effects and giving room for oxide thickness variation across the wafer the ideal gate oxide thickness was calculated to be ~900 Å.

$$V_T = 2\phi_f + \frac{K_s x_o}{K_o}\sqrt{\frac{4qN_A}{K_s\varepsilon_o}\phi_f} \rightarrow x_o = \frac{(V_T - 2\phi_f)K_o}{K_s\sqrt{\frac{4qN_A}{K_s\varepsilon_o}\phi_f}} \quad (2.1)$$

Where,

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (2.2)$$

$$\phi_f = Source\ to\ Body\ Potential$$
$$V_T = Voltage\ Threshold$$
$$x_o = oxide\ thickness$$
$$K_s = Silicon\ Dielectric$$
$$K_o = Oxide\ Dielectric$$
$$N_A = Doping\ Concentration$$

Using Figure 2.1, the oxidation time was calculated to be roughly 2.5hr. Since both devices need the same threshold voltage and they both have the same oxide thickness the doping concentration needed in the NMOS device has to be $1.5x10^{15}$atoms/cm^3.

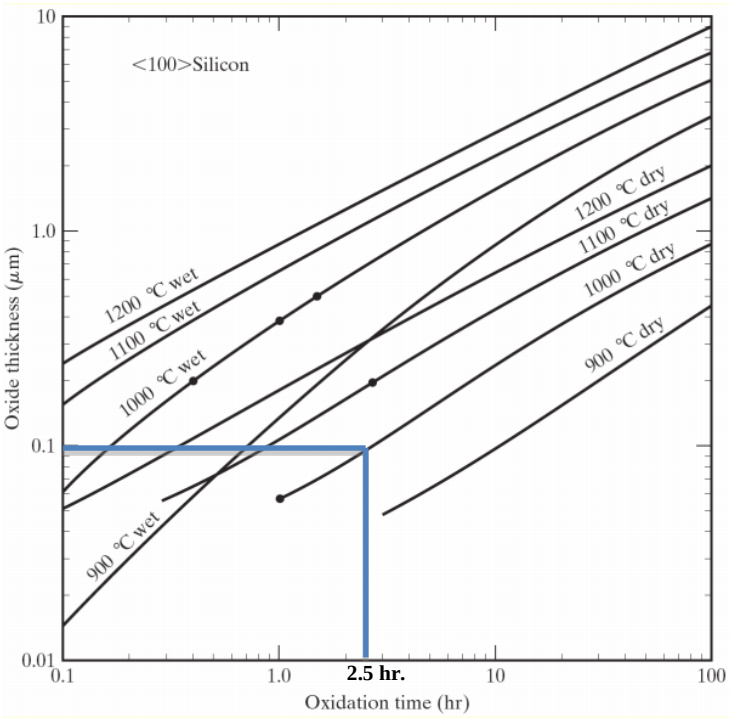


Figure 2.1: Oxidation time (2.5 hr.) calculation using dry oxidation thickness chart [10].

2.2 Simulation

A simulation using Athena and Atlas was performed to estimate the range of SiO_2 thickness, and pre-deposition and drive-in times. The overall threshold voltage was expected to be between 0.5V and 1.5 V using the simulation. Figure 2.2 and Figure 2.3 show a cross section of the transistor simulator using Athena which show surface concentrations at different parts of the device. Figure 2.4 also shows a threshold voltage calculation using Atlas. A copy of the Athena code used for the simulation is attached in the appendix.

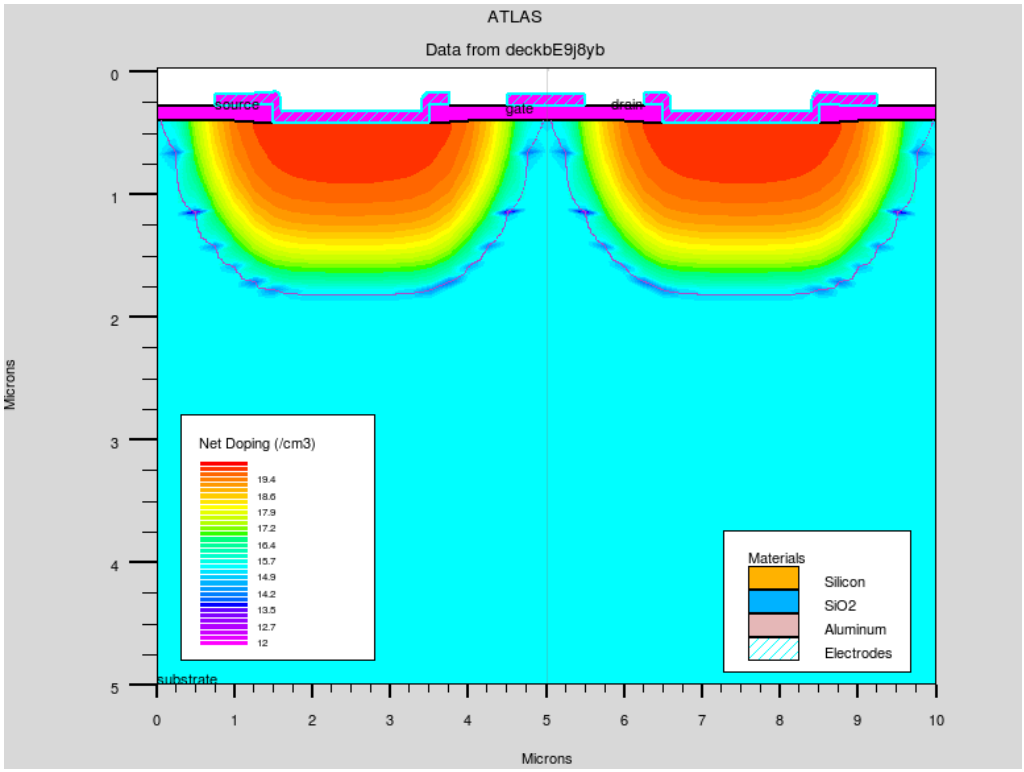


Figure 2.2: Cross section of NMOS simulation with Athena.

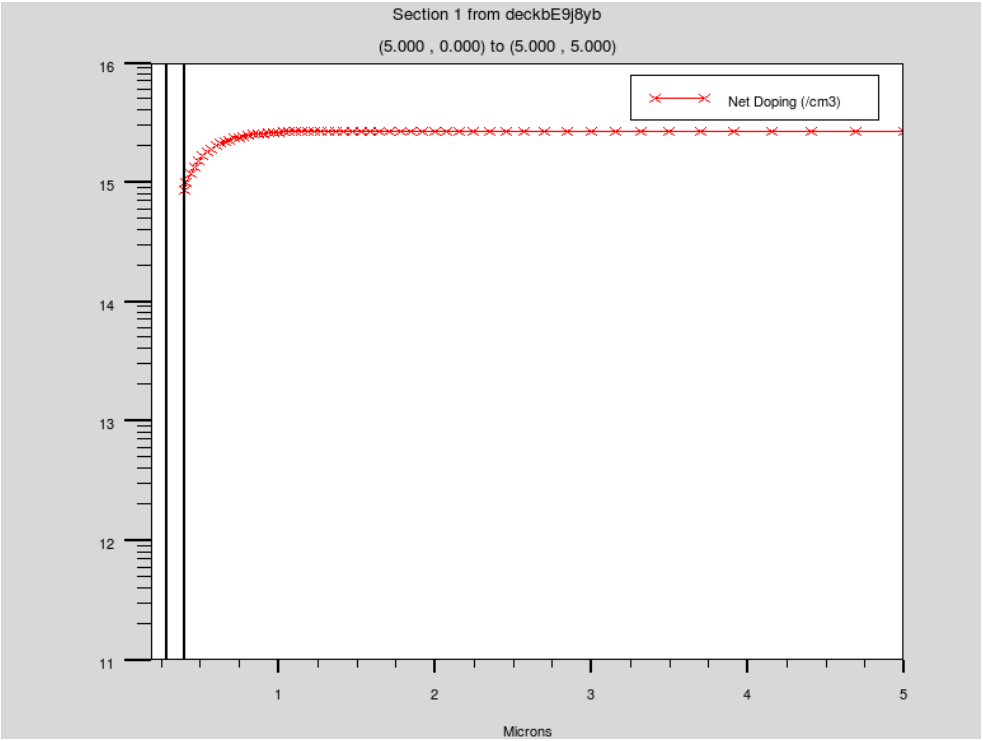


Figure 2.3: Simulation of surface concentration of NMOS device used for the ZnO pressure sensor

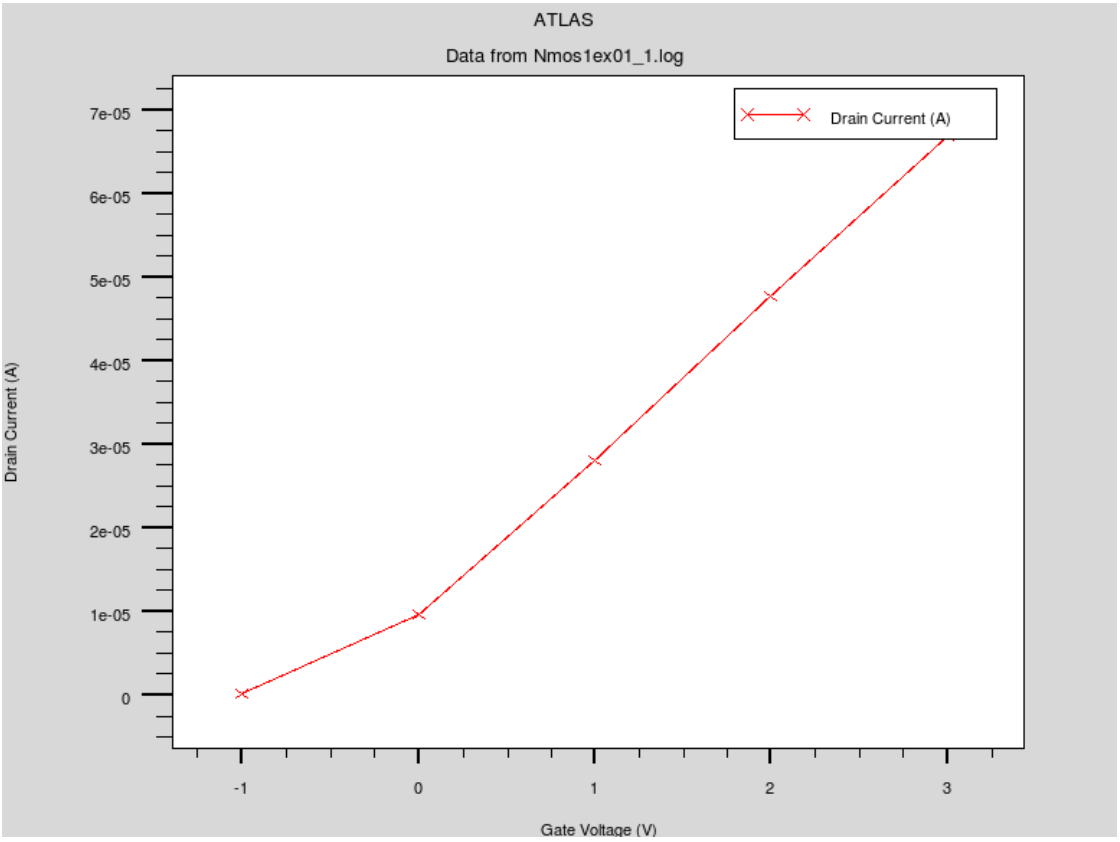


Figure 2.4: I_D vs. V_g of a simulated NMOS device.

2.3 Fabrication

PMOS and NMOs were fabricated 100% percent in the VMC. The combination of MOSFET and ZnO nanowire will produce the pressure sensor. This section will review all the key steps of the fabrication sequence used in the MOSFET fabrication.

2.3.1 Process Flow

With hand calculations and computer simulations, the next step was to create a wafer traveler. Table 2.2 below has a graphic representation and a brief description of key fabrication steps.

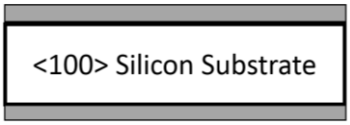
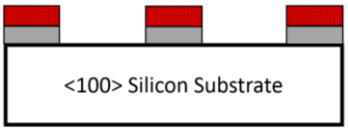
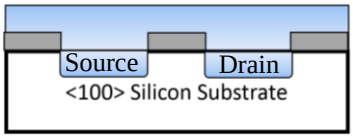
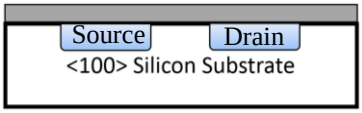
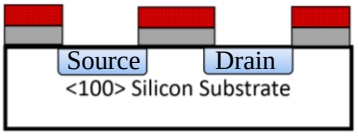
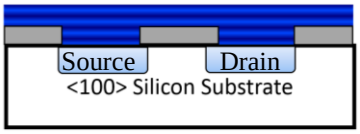
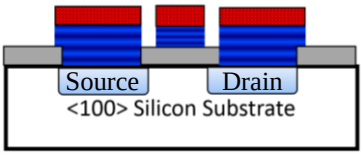
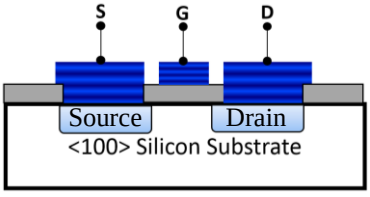
Graphic representation	Description
	Step 1: Wet Oxidation. To grow Silicon-dioxide (SiO_2). Necessary to prepare initial diffusion step.
	Step 2: Diffusion Photolithography. To accomplish the patter transfer for diffusion.
	Step 3: Diffusion. Spin-on glass diffusion process to dope source, and drain regions into the silicon substrate. PMOS- Boron SOG. NMOS-Phosphorus SOG
	Step 4: Strip & grow gate oxide. To remove the masking oxide/dopant layer and perform gate level oxidation.
	Step 5: Contact Lithography. To accomplish the pattern transfer for second diffusion (P-type).
	Step 6: Metallization. To deposit Aluminum for gates and contacts using the E-beam evaporator system.
	Step 7: Metal lithography. To accomplish the pattern metal layer.
	Step 8: Resist strip & sinter. To remove photoresist used in last step and final sinter to alloy contacts.

Table 2.2: NMOS & PMOS fabrication process flow.

2.3.1 Wafer Layout

The ultimate wafer layout goal was to fabricate PMOS and NMOS on the same wafer type. Therefore, the layout was designed to be implementing in a full CMOS fabrication process with a total of five implants for P-N wells, source/drain diffusion and voltage threshold adjustment. However, the pressure sensor was first made with PMOS and NMOS on separate wafers but eventually this wafer layout will help to fabricate CMOS devices with nanowires on the gate. There were a total of 9 mask designed to fabricate working PMOS and NMOS transistor:

1. Local Oxidation of Silicon (LOCOS)
2. P-Well
3. N-well
4. Source/Drain (PMOS)
5. Source/Drain (NMOS)
6. Contacts
7. Metal (Characterization)
8. Special Metal (Nanowire anodization template)
9. Nanowires pattern

Nevertheless, LOCOS, P-Well and N-well masks were not used in the work of this thesis and will serve for future work on more complex nanowire sensors. The wafer design was chosen to be a five by five die pattern that allowed a total of 25 dies to be fabricated, Figure 2.5. This design was used so that there was enough space for the required labeling while also leaving extra room between the features and dies. Furthermore, this design leaves

enough room to cleave the wafer so that dies can be packaged. Three different device concepts were designed:

- Transistors and inverters.
- Ring oscillator (CMOS).
- Test Structures.

The first design was utilized in dies 1-20. The second design was only fabricated on die 21. Different test structures such as capacitors, resistors, contact chains and Van der Pauw were assigned to dies 22-25.

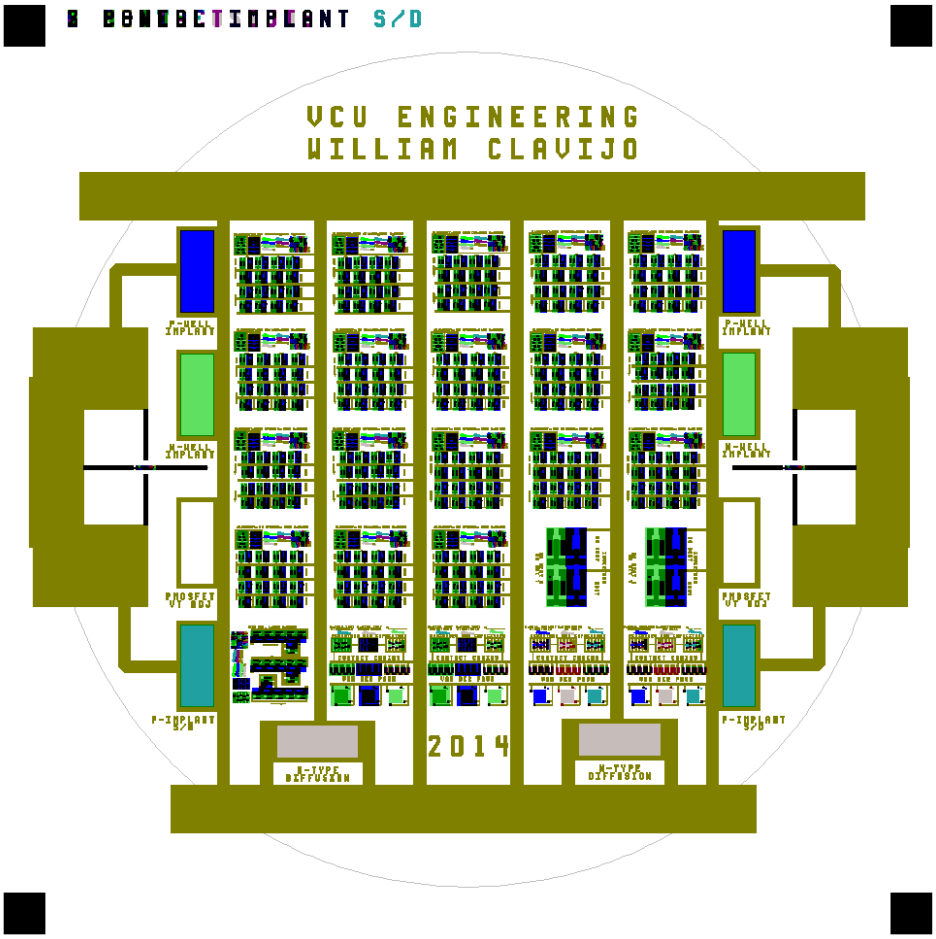


Figure 2.5: Wafer layout to fabricate PMOS and NMOS.

The first die design, seen in Figure 2.6, consists of five rows of devices. The first row of test structures will be used to check device parameters such as sheet resistance,

contact resistance, and the alignment variances between fabrication steps. The two rows of transistors each consist of four pairs PMOS and NMOS transistors. These transistors have varying gate lengths of 3µm, 5µm, 20µm, and 50µm, and the bottom row of transistors have body contacts on each transistor. The body contact on the transistor is used to ensure that there is no body bias present to affect the threshold voltage of the device. The two rows of inverters consist of four inverters each. The inverter design is simply a PMOS and NMOS transistor connected in series with one another. The bottom row of inverters will also have body contacts to prevent body biasing. The variations that will occur between dies 1-12 are the spacing of the transistors (seen in Figure 2.7) which will either be 50µm or 150µm, and the alignment tolerances of the gates which will be 1µm, 10µm, and 25µm.

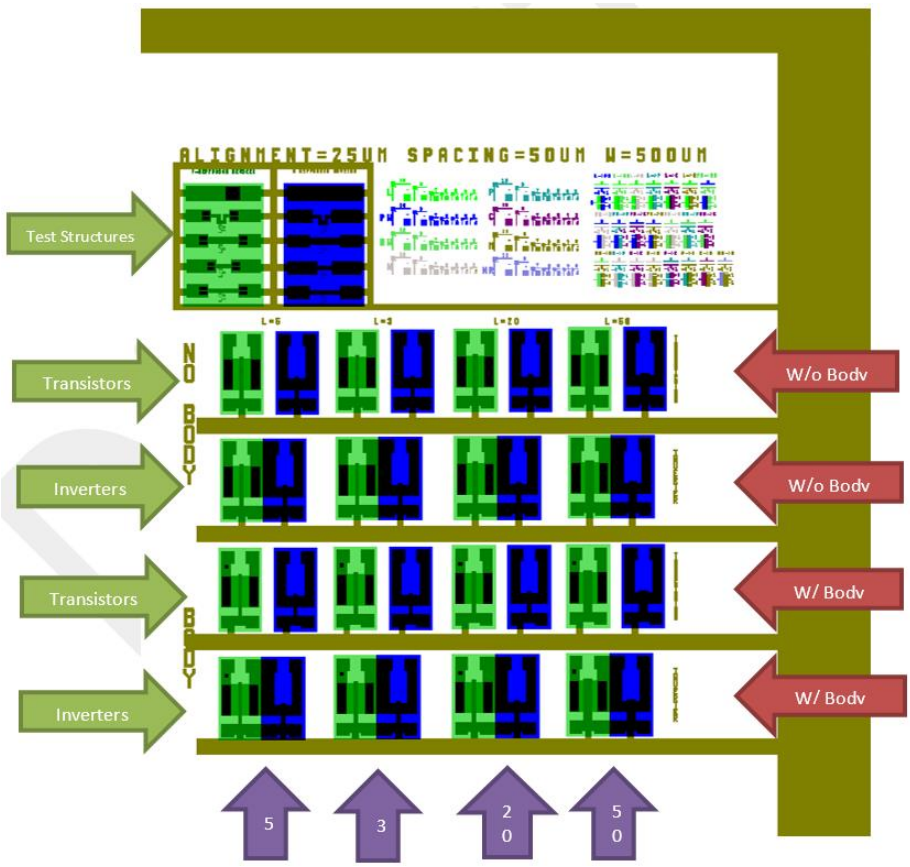


Figure 2.6: First die Design, transistor and inverters.

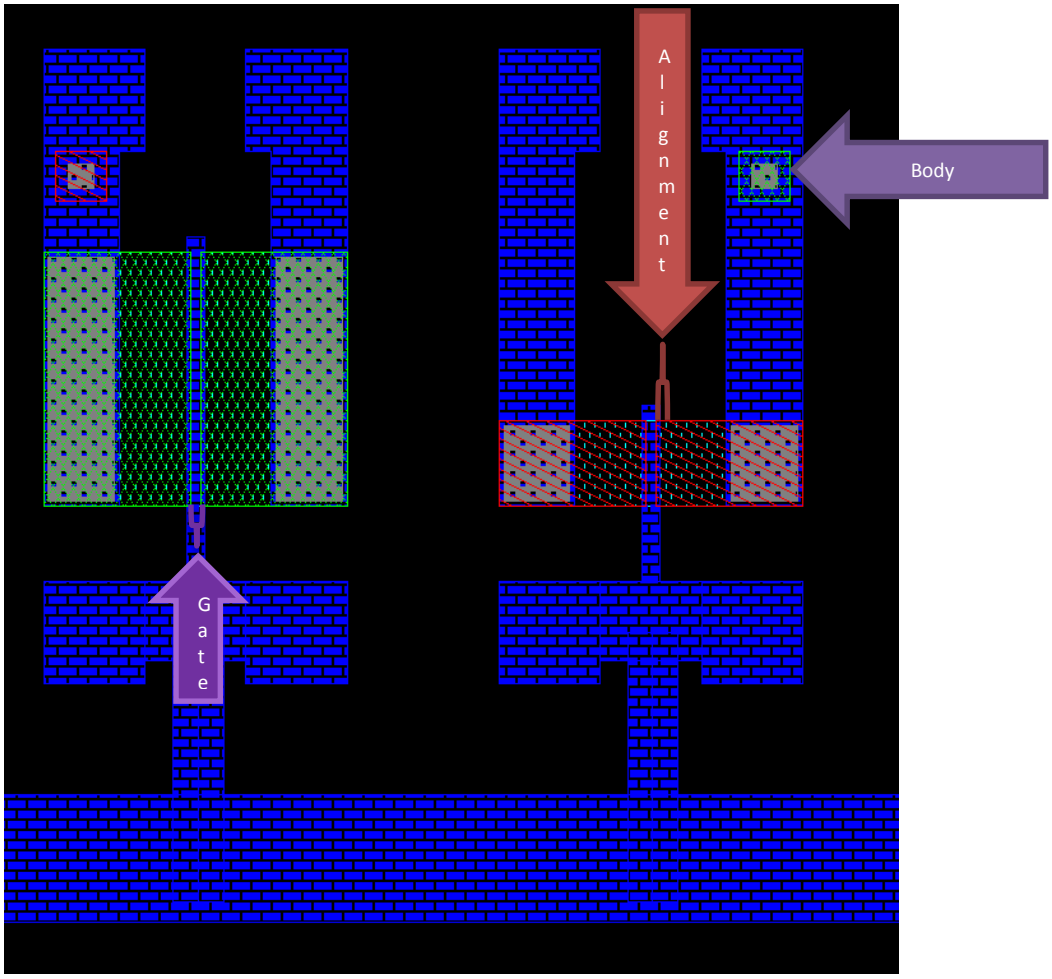


Figure 2.7: Transistor description; PMOS on left, and NMOS on right. Both transistor with body contact, gate length of 20 µm and alignment tolerance of 1µm.

Ring oscillators were the second die design which was not used in the fabrication of the pressure sensor, but will be used in future work. The third die design was a complete set of test structures for every diffusion step during the fabrication process. Figure 2.8 shows all the test structures that were used to characterized diffusion profiles for the pressure sensor.

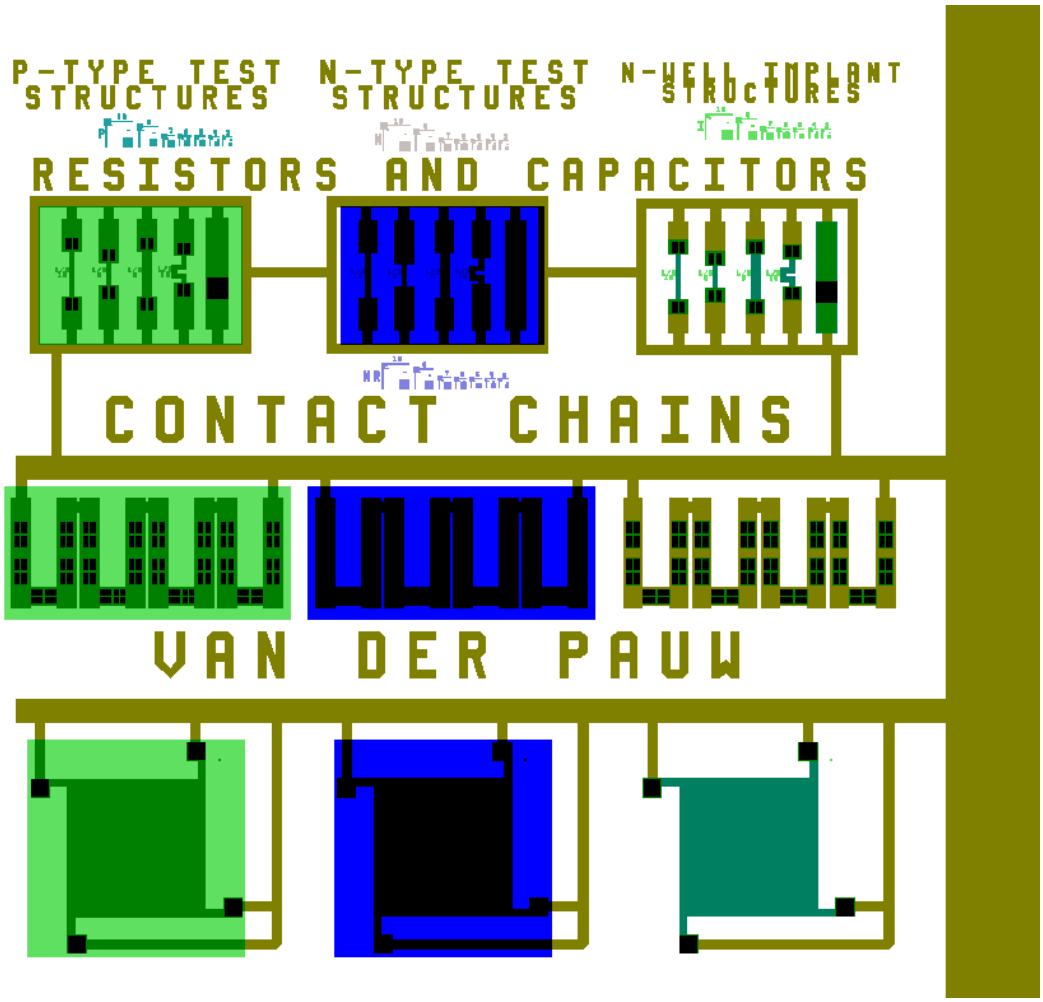


Figure 2.8: Third die design. Test structures to characterize diffusion profiles of transistors.

One key feature of the wafer layout is that it uses one special mask where all the gate metal contacts are connected to big electrodes on the wafer. The main reason for that was because once the transistor was ready for metallization, it could be anodized in a custom made setup. More detail anodization of aluminum will be covered in the next section. One way to understand how the ZnO nanowires work on a gate of a transistor was first to characterize PMOS and NMOS transistors without ZnO nanowires, a mask was design for that purpose. Figure 2.9 shows the complete wafer layout with the difference that the metal mask is different. In the other hand, Figure 2.2 shows the same transistor

design but with the only difference that the metal mask has electrodes in most parts of the wafer for the anodization of aluminum.

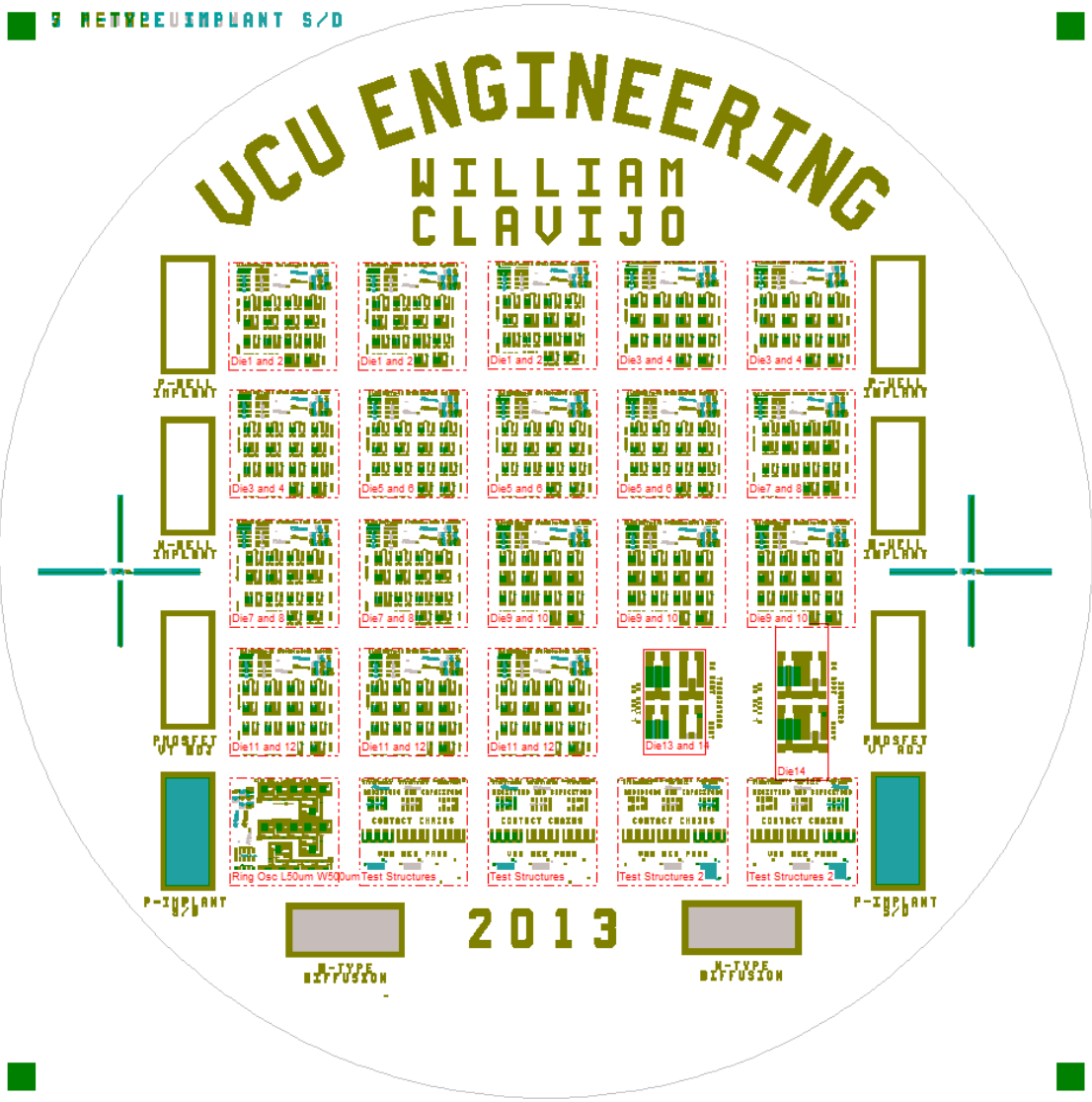


Figure 2.9: Wafer layout without nanowire metal mask.

Chapter 3 Electrochemical Self Assembly Technique to Fabricate Highly Ordered Nanowires

Overview:

ZnO nanowires were fabricated on top of the gate of a MOSFET transistor. The most important fabrication consideration was that the entire fabrication had steps that did not have temperatures greater than 90°C and it was CMOS compatible. The temperature of the different fabrication steps ranged from 24°C to 90°C. High temperature fabrication steps change the diffusion profile in the transistor. Therefore, a low temperature nanowire assembly is ideal for the fabrication of the pressure sensor. The fabrication of ZnO nanowires used a combination of aluminum deposition, aluminum anodization, chemical wet etching, and Zinc Oxide atomic layer deposition. Figure 3.1 shows and overview of the fabrication sequence of the ZnO nanowires. The following section will explain the most important fabrication steps to produce a high aspect ratio ZnO nanowires on a gate of a MOSFET.

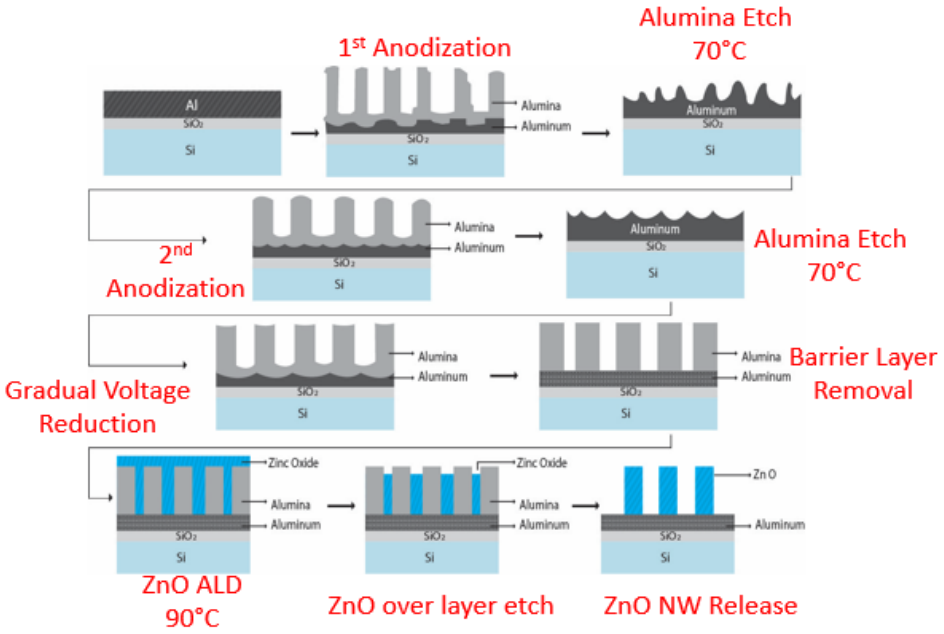


Figure 3.1: Ultra high aspect ratio ZnO nanowire fabrication.

3.1 Optimization of Ultra-Smooth Thick Aluminum Deposition

Aluminum Oxide (Al_2O_3), also known as Alumina, is made through the anodization of the aluminum layer. During the anodization process, the aluminum layer gets consumed. There are not specific alumina grow rates. All depends on the voltage, electrolyte, distance between the anode and cathode and temperature of the anodization of Aluminum. A more extensive detail discussion about anodization parameters will be presented in the next section. However, a relative ultra-smooth thick Al deposition is the first step necessary for the fabrication of the ZnO nanowires. In a typical MOSFET fabrication sequence, a thin layer of a metal is enough to make contact with the source, gate and drain. In our case, a thin layer of aluminum was not acceptable because the alumina growth is made consumption of the aluminum layer. There were four available options for film deposition using equipment in the VMC:

1. Thermal evaporation.
2. Aluminum Sputtering
3. Electroplating
4. E-beam evaporation.

Those options are usually used for thin layers no greater than 300 nm. Out of the 4 available options, e-beam evaporation was chosen because the system could be modified to deposit more than 300 nm of aluminum. The e-beam evaporator in the VMC has a 376 crucible indexer which allows the interchange of deposition targets during a metal deposition. Figure 3.2 shows a picture of the crucible indexer that was used during the Al deposition.

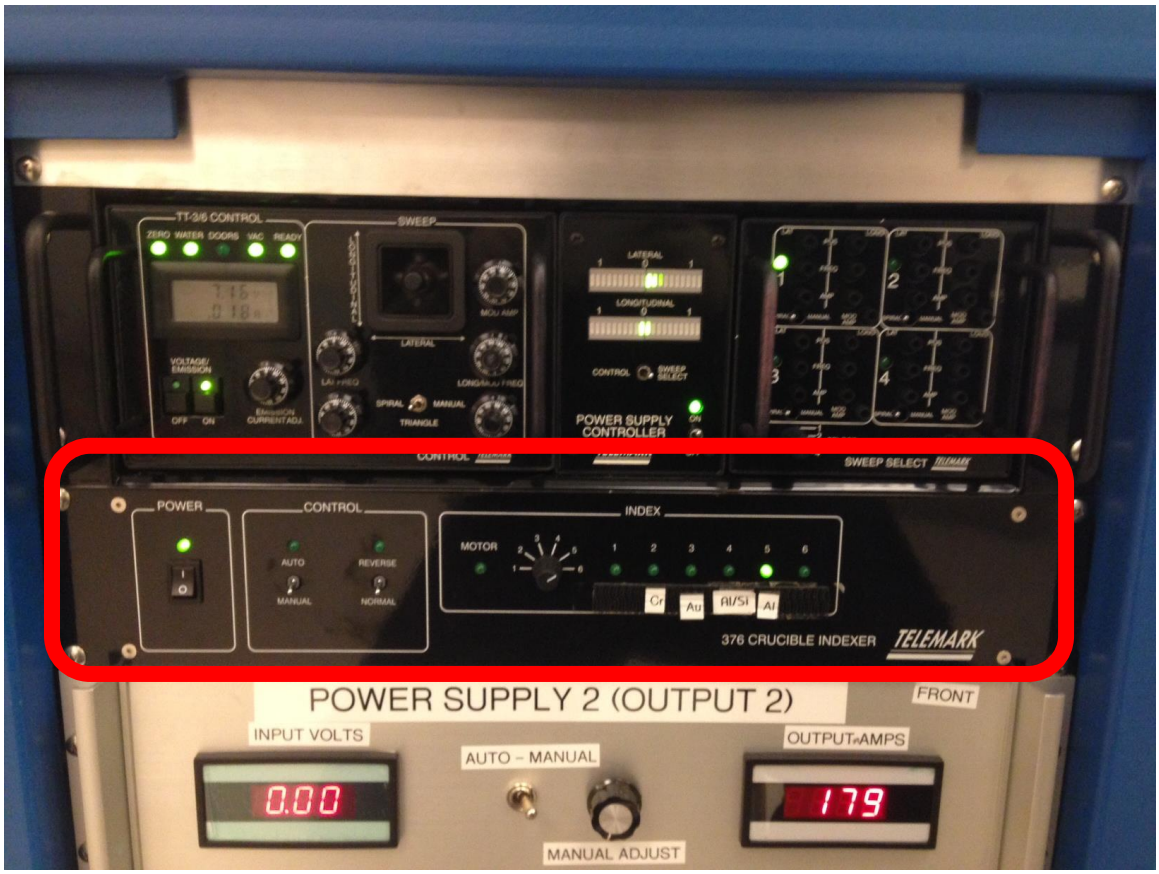


Figure 3.2: 376 Crusible indexer by TeleMark.

One of the goals of our work was to fabricate high aspect ratio nanowires on a silicon substrate. To achieve that goal, an Al layer of at least 1µm was necessary. There was not prove that the machine was capable of doing of such a film deposition. Since the crucible could be changed for a new one during a deposition process by rotation of the indexer, the e-beam evaporator was expected to grow relative thick aluminum layers. For a thick aluminum deposition, 3 crucibles full of 99.999% percent Aluminum pellets by Kurt J. Lesker Company were used. Each crucible was able to hold about 15 grams of 1/8" diameter by 1/8" long Aluminum pellets. There was not clear way to find out exactly the maximum aluminum thickness deposition per crucible, but after few experiments we found out that it takes about 1.75 hours to completely consume one crucible of aluminum pellets

with a total thickness of about 1.5µ– 2µm. Even though the e-beam evaporator comes with a crystal thickness sensor but it fails to give an accurate reading after a long deposition, 1-4 hours.

Another key parameter that was taking into account was the pressure of the chamber during the deposition. Adhesion between the aluminum layer and the SiO_2 was critical. Therefore, a high quality aluminum deposition was very necessary. To achieve that, the chamber was left into high vacuum for a minimum period of 12 hours before doing the deposition. A high quality aluminum film deposition was achieved when the chamber reached about 1E-7 – 3E-6 Torr. The maximum thickness achieved with the e-beam evaporator was about 4µm, but only 2.3 µm of aluminum was deposited for the fabrication on the ZnO nanowires for the pressure sensor (Figure 3.3).

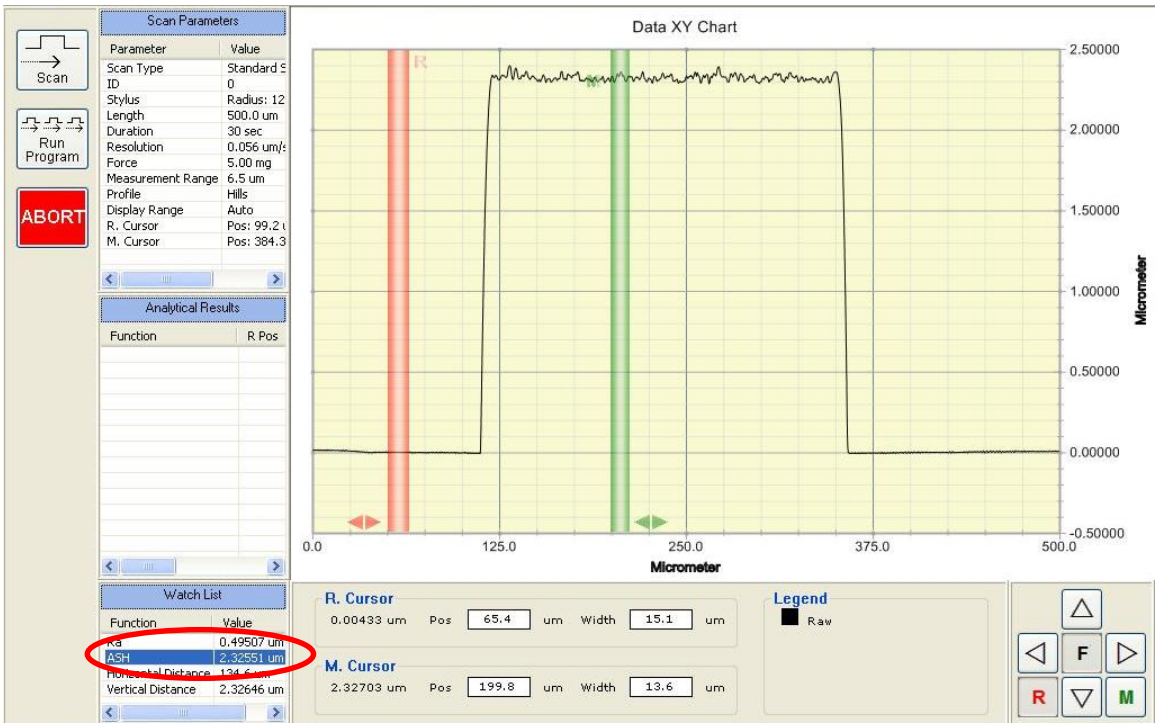


Figure 3.3: Dektak profiler, average step thickness, 2.3 µm aluminum thickness achieved by e-beam evaporation.

One way to find out that the crucible was running out of aluminum pellets was to closely pay attention to the deposition rate on the deposition controller. It is known that the crucible was normal when the deposition rate and the power percentage was constant during the deposition. The deposition rate starts to deviate after about 1.75 hours, which meant that it was time to change the crucible for a new one. It was very important to turn off the e-beam before changing the crucible using the crucible indexer. That helped to prevent impurities to reach the surface of the wafer. Figure 3.4 and Figure 3.5 show a comparison of the deposition controller display when the deposition rate is constant and when the deposition rate was abnormal.

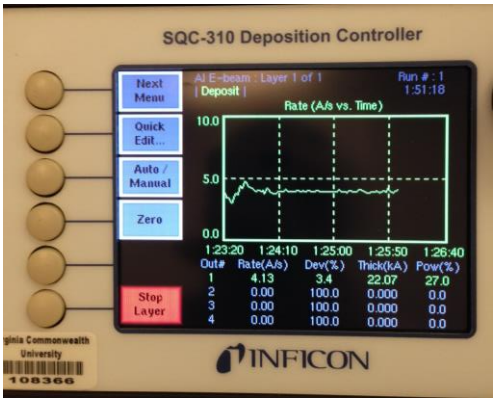


Figure 3.4: Deposition controller when there are still aluminum pellets in the crucible, deposition rate is constant.

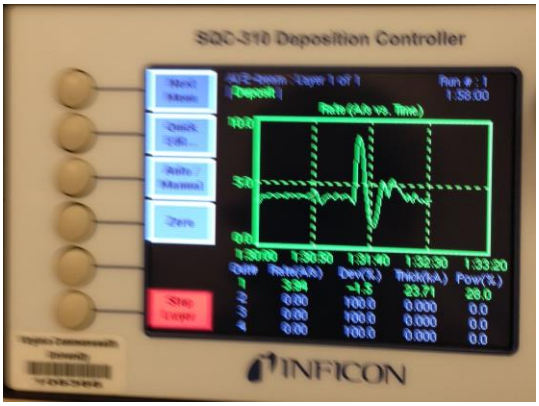


Figure 3.5: Deposition controller when the crucible is becoming empty, abnormal deposition rate and power percentage increased.

Most of the studies of Anodic Aluminum Oxide (AAO) in the past two decades generally required a smooth mirror like aluminum surface to achieve a highly ordered porous surface [11]. AAO templates are usually done with commercial available aluminum foils of about 250 μm thick with an electromechanical polishing step prior the anodization process. A typical electrochemical polishing consumes about 200 μm of the aluminum film. In our case, the thickness of aluminum deposited on the silicon wafer was not enough

to do an electromechanical polishing. The aluminum roughness is critical to fabricate highly ordered alumina pores, the lower the average roughness the higher ordered could be obtained. Another reason why aluminum e-beam evaporation was chosen is because the film deposition has a very low average roughness index. The roughness of the aluminum film was characterized with an optical profiler – Wyko. Figure 3.6 shows that the average roughness of the aluminum layer was low enough (1.43nm) to allow a high ordered alumina layer.

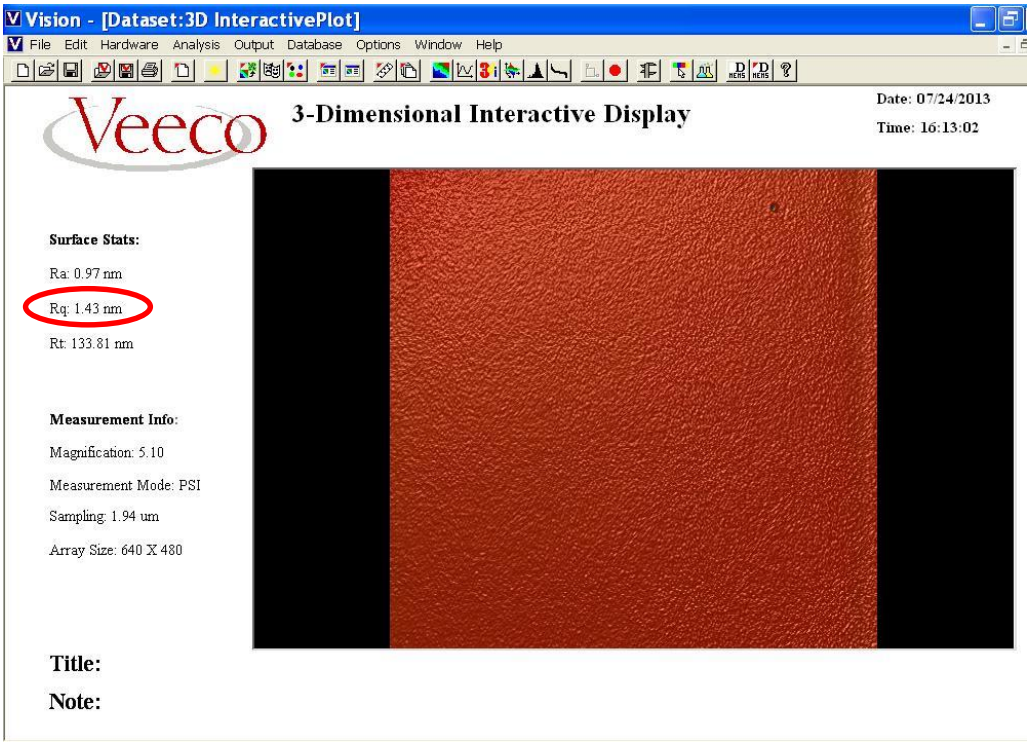


Figure 3.6: Average roughness number of an aluminum film deposited on a silicon wafer by e-beam evaporation.

3.2 Aluminum Anodization

The anodization of the aluminum film was conducted in a custom made flat cell that used the Silicon wafer with aluminum film as anode and a platinum mesh on the other

side as cathode. The following chemical reaction happens on the anode and cathode during the porous oxide growth [12]:

Anode: $2Al\ (s) + 3H_2O = Al_2O_3 + 6H^+ + 6e^-\ (s)$ (Oxidation of aluminum)
Cathode: $6H^+ + 6e^- = 3H_2$
$Al_2O_3(s) + 6H^+ = 2\ Al^{3+} + 3H_20$ (Dissolution of alumina)

The thickness the alumina layer depends on three parameter:

1. PH of electrolyte
2. Voltage
3. Time

The chemical reactions during the anodization of aluminum is continuous as long as there is a constant voltage across the anode and cathode. Therefore, a time controlled formation nanoporous aluminum oxide is required due to the fact that the Al film thickness is limited. The anodization process done for the pressure sensor was at 40V in a 3 wt. % Oxalic Acid electrolyte. Figure 3.7 shows the custom made fall cell used for aluminum anodization.

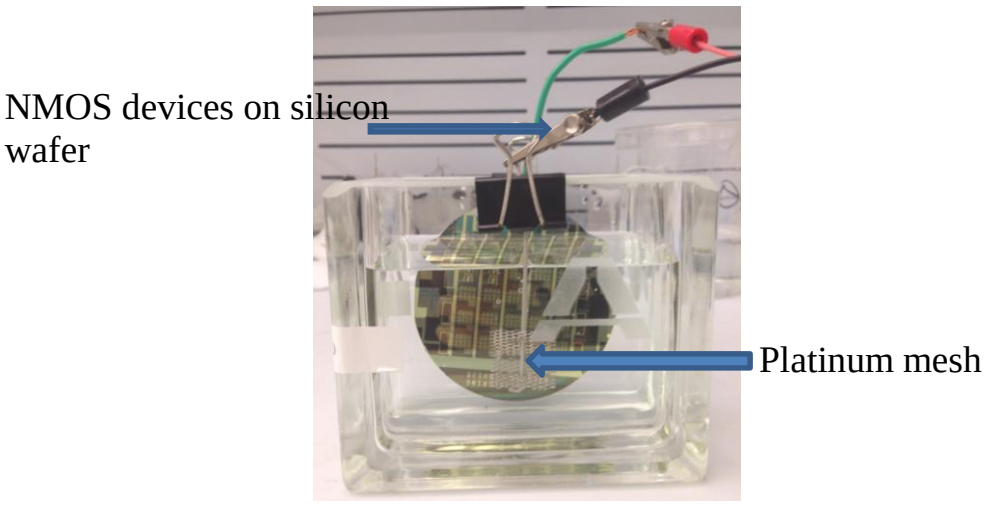


Figure 3.7: Silicon wafer with aluminum pattern in anodization cell connected to a DC Power source and a PC through GPIB interface.

This setup was connected to a HP DC Voltage power source with a custom made LabView interface to gather data and to closely monitor the current during the anodization process. Figure 3.8 and Figure 3.9 show the LabView interface for the power supply.

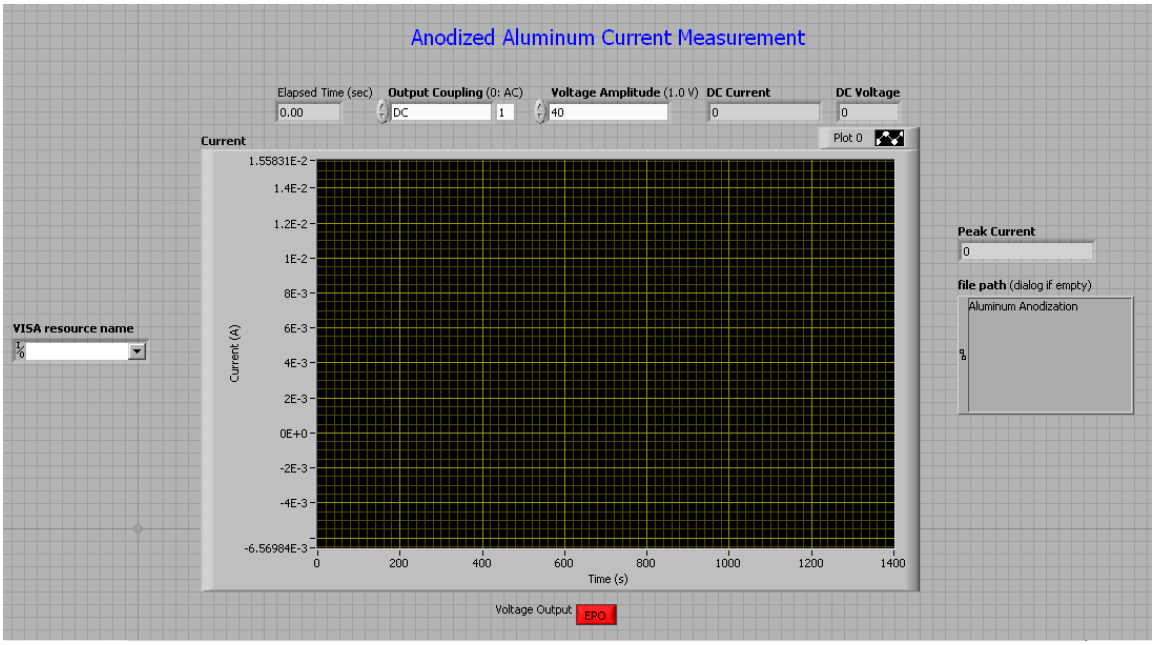


Figure 3.8: Optimized Labview interface for the power supply used for the aluminum anodization (Agilent 6811B).

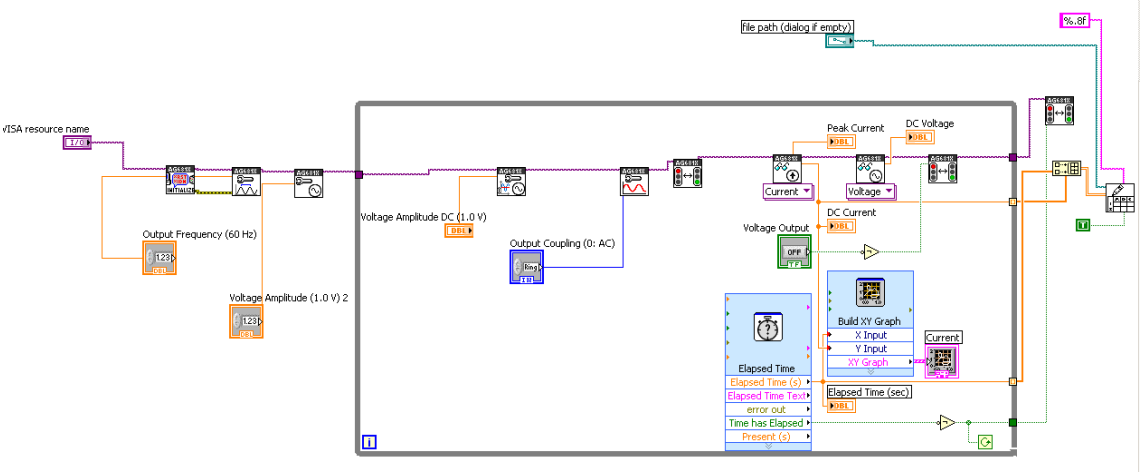


Figure 3.9: Optimized Labview block diagram for the power supply used for the aluminum anodization (Agilent 6811B).

A single step anodization process was first attempted. A typical current vs. time curve is shown in Figure 3.10. It was seen that the bigger the silicon piece with aluminum, the higher current was. That was expected since the current density in the electrolyte increases with the size of the sample that was submerged for anodization step. However, the same curve shape was always the same regardless of the size of the sample. In this particular step the size of the sample did not matter much.

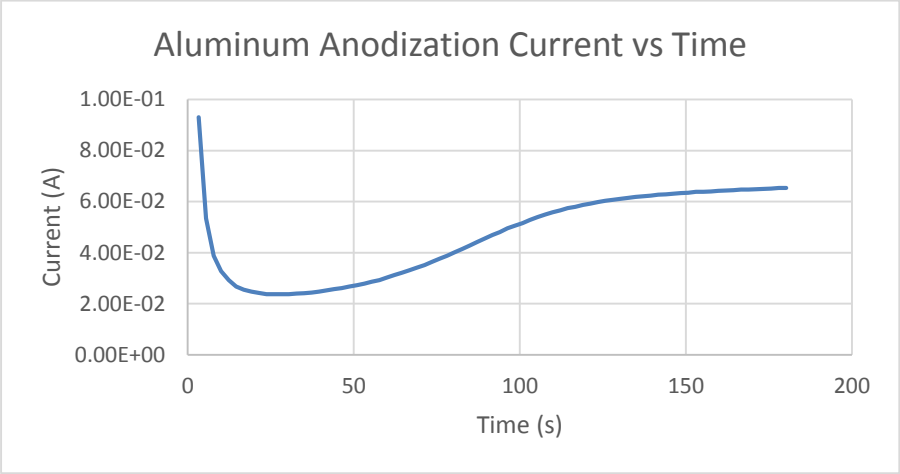


Figure 3.10: Typical 3 minute aluminum anodization current vs time curve. 40V in 3% Oxalic Acid, room temperature.

Figure 3.11 explains the sequence steps during the growth of the alumina layer. It was seen that the current drops in the first stage of the anodization process. Then, the rate of oxidation becomes greater that the rate of dissolution once the current reaches its minimum value. Current then starts to increase which means that pours continue to grow. Once the current is flat and steady, the rate of dissolution reaches the same rate of oxidation and the sample will continue to be oxidized continuously.

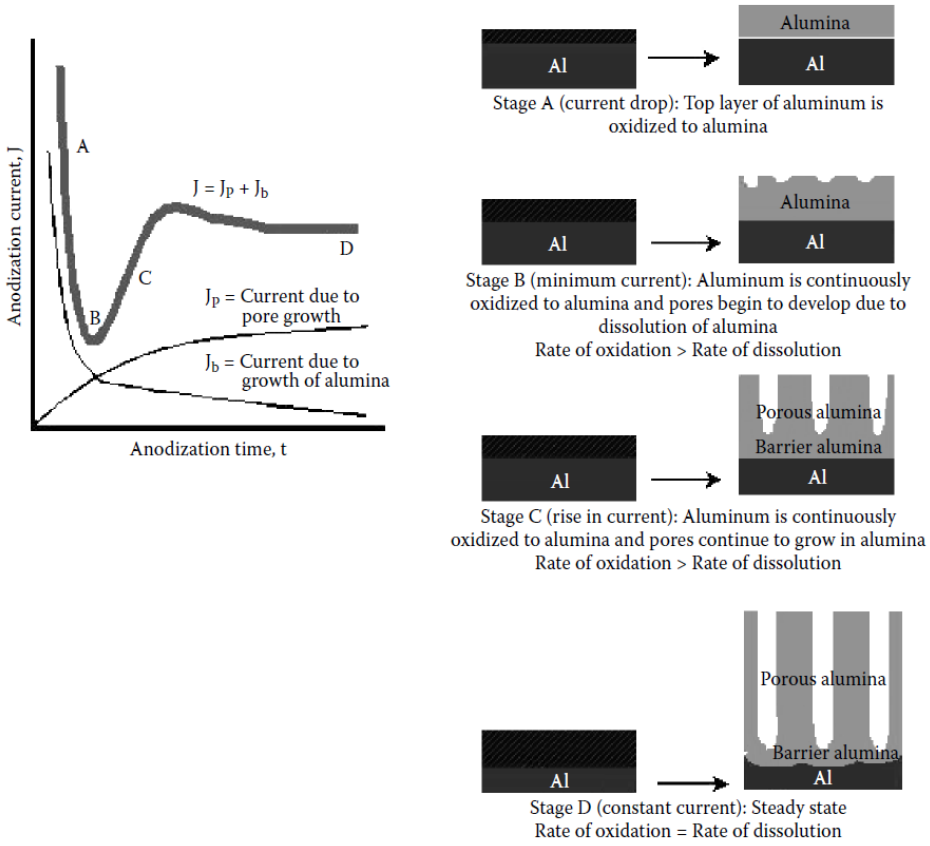


Figure 3.11: Sequence of steps explaining the growth kinetics of nanoporous alumina membrane. [12]

After a single step anodization, the alumina membrane did not have high uniformity pores. Figure 3.12 shows a SEM image of what happened to the aluminum film after a 3 minute single anodization step. Highly uniform surface was absolutely necessary in order to achieve a highly ordered nanowires on the gate of the MOSFET. Therefore, a multi-step anodization process was then tried as a second option.

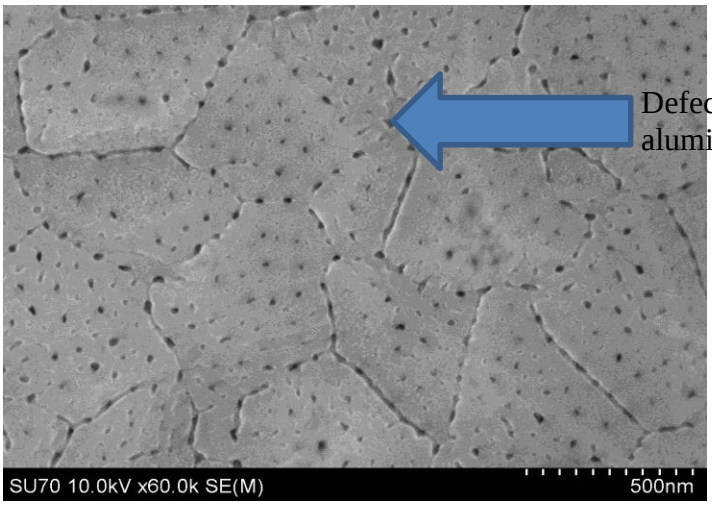


Figure 3.12: SEM image of aluminum 3 minute single step anodization process at 40 V in 3 wt. % Oxalic acid.

Masuda *et al*, [13] have proven that a multi-step aluminum anodization helps to obtain nanaporous alumina with high uniformity. That fabrication process requires a three step anodization technique. The usual multistep anodization process is usually done on an aluminum foil that requires one 5-10min long first anodization process, then a second 10-12 hour anodization, and lastly a 10 minute anodization step. Nevertheless, in our case that long anodization steps could not be done because of the limited thickness of the aluminum film that was deposited on the silicon wafer. An optimized multi-step anodization was develop specifically for an aluminum layer on a silicon wafer. It was calculated that the aluminate grow rate was about 1μm for every 5 minutes, which meant that the total anodization time could not exceed 10 minutes in the case of the film that was deposited on the MOSFET wafer. However, the longer the steps in the multistep anodization process the higher uniform pores pattern is made. After several experimental runs, it was decided that 3 minutes for the first two anodization steps then a 5 minute anodization was enough to fabricate highly ordered porous templates, Figure 3.13 and Figure 3.14.

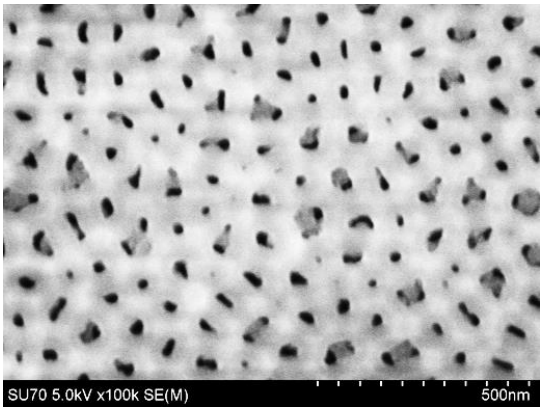


Figure 3.13: Top view SEM view of wafer sample with an aluminum film after a multistep anodization process at 40 V in 3% Oxalic Acid.

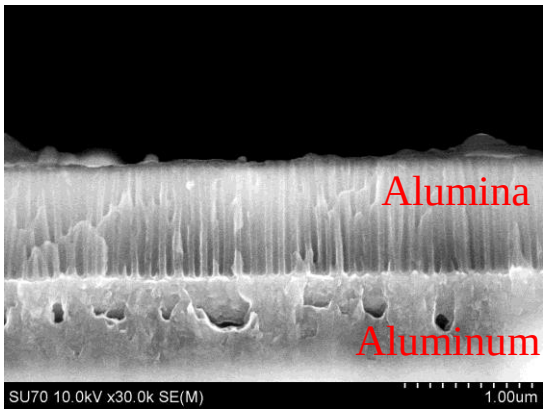


Figure 3.14: Cross section SEM view of wafer sample with an aluminum film after a multistep anodization process at 40 V in 3% Oxalic Acid.

A schematic diagram in Figure 3. 15 shows the entire sequence of the multi-step anodization process used for the pressure sensor with ZnO nanowires.

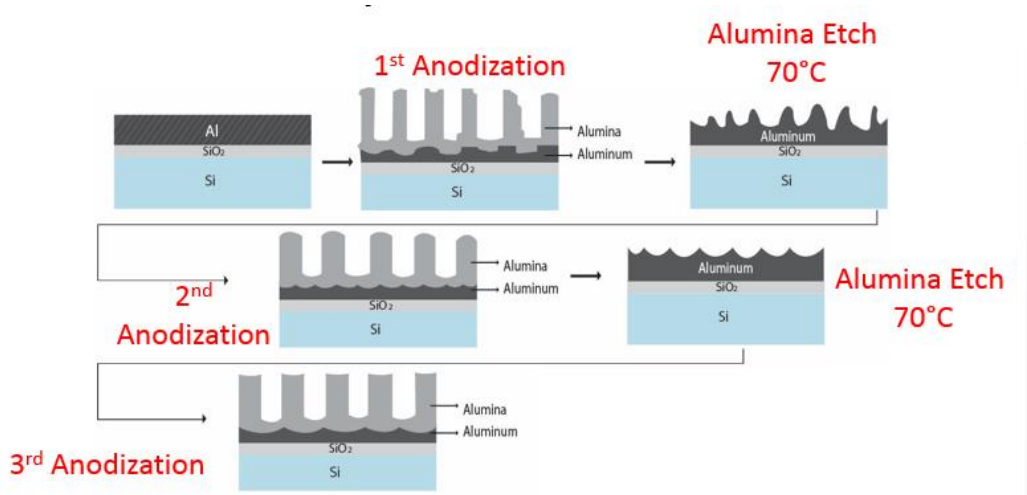


Figure 3.15: Schematic diagram of the optimization of the multistep anodization process for the pressure sensor.

3.4 Barrier Layer Removal

Porous alumina membranes have been used for different kinds of applications such as filtration, bioreactor, tissue culture and a variety of sensor [12]. The anodization of aluminum is a powerful technique that could produce a narrow pore-size distribution, high pore density and controlled alumina thickness. However, one of the disadvantages of this

technique is that the alumina membrane gets attached to the aluminum layer. The aluminum anodization leaves a thin layer of alumina at the bottom of the pores. That is not desirable if the material that needs to be inside the pores needs to be in contact with the substrate or the aluminum film. A process by Ferneaux *et.al*. [14] overcomes this issue by gradually reducing the anodizing voltage, which causes a perforation of the barrier layer right at the bottom of the pores between the alumina and the Al layer. The structure after the step anodization process leaves a thin barrier layer, Figure 3.16.

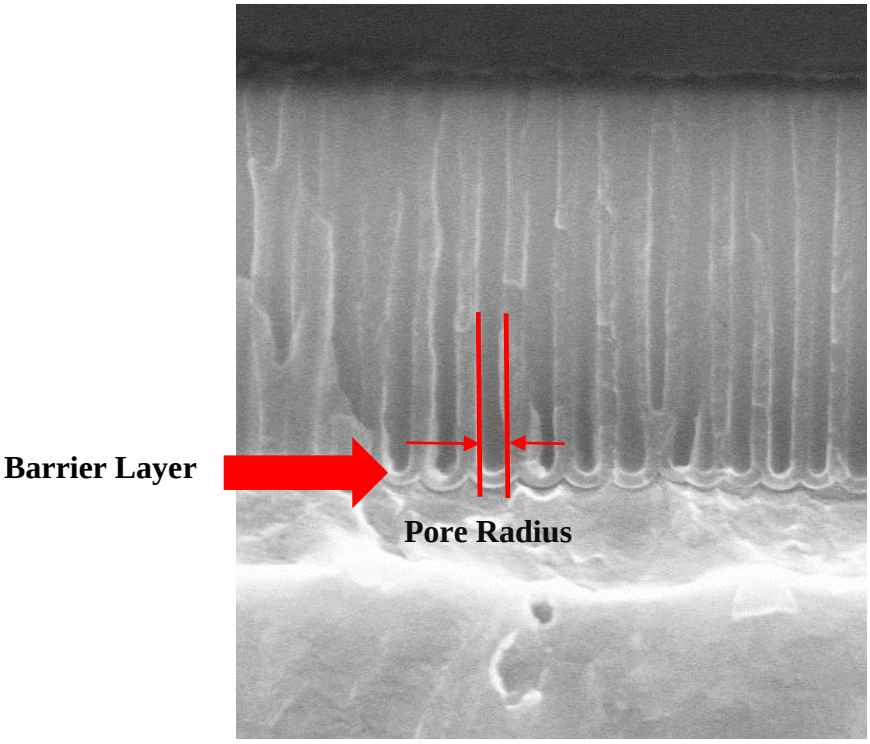


Figure 3.16: Description of a cross section SEM view of a porous film on an aluminum layer.

Gradual voltage reduction was accomplished during the 3rd step of the anodization process. The size of the samples is very critical during the barrier layer removal because the current density disseminates when the barrier layer is gone from the sample. The optimization of the gradual voltage reduction was characterized with sample from 1cm^2 to

5 cm^2. Samples longer or shorter than that will not work with the optimization of the gradual voltage reduction discussed below.

The gradual voltage reduction process has three different stages. First, a high voltage anodization of samples. This is where most of the alumina layer will grow. Second, gradual voltage decrease at a rate of 0.1V/sec all the way down until current reaches its minimum value (as close as 0 Amps as possible). Third, long low voltage anodization stage. That is where the alumina will be consumed slowly. Figure 3.17 shows a current vs. time of a usual gradual voltage reduction for the samples used for the sensor. The parameters used in the gradual voltage reduction were the following:

1st Stage: 40 V, Time 5 minutes.

2nd Stage: Voltage rate reduction: 0.1V/sec, Time: 5min 10 sec.

3rd Stage: Low voltage anodization. Voltage: 9V, Time 10 minutes.

The previous steps needed to be in a continuous anodization single step, without taking the sample out of the flat cell until all the three stages of the gradual voltage reduction were completed. A final 90 minute alumina wet etching in 5% Phosphoric Acid was necessary for pore enlargement, and to remove some of the alumina left at the bottom of the pores from the gradual voltage reduction step, Figure 3.18.

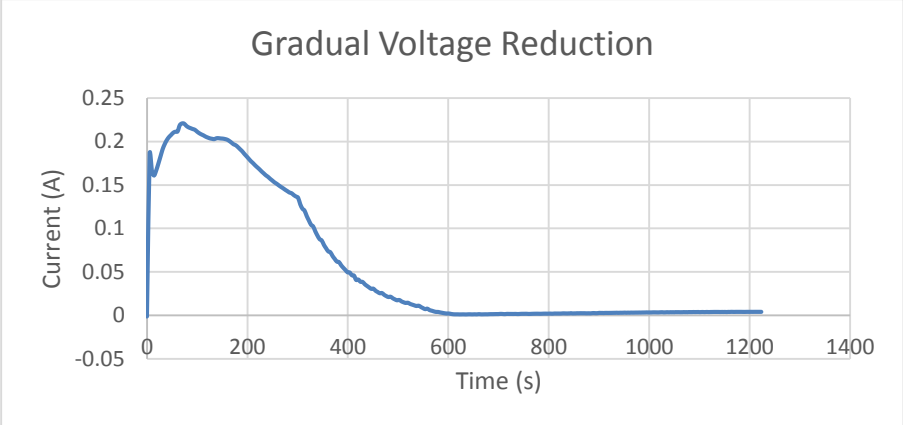


Figure 3.17: Curve description of current vs. time during the gradual voltage reduction step.

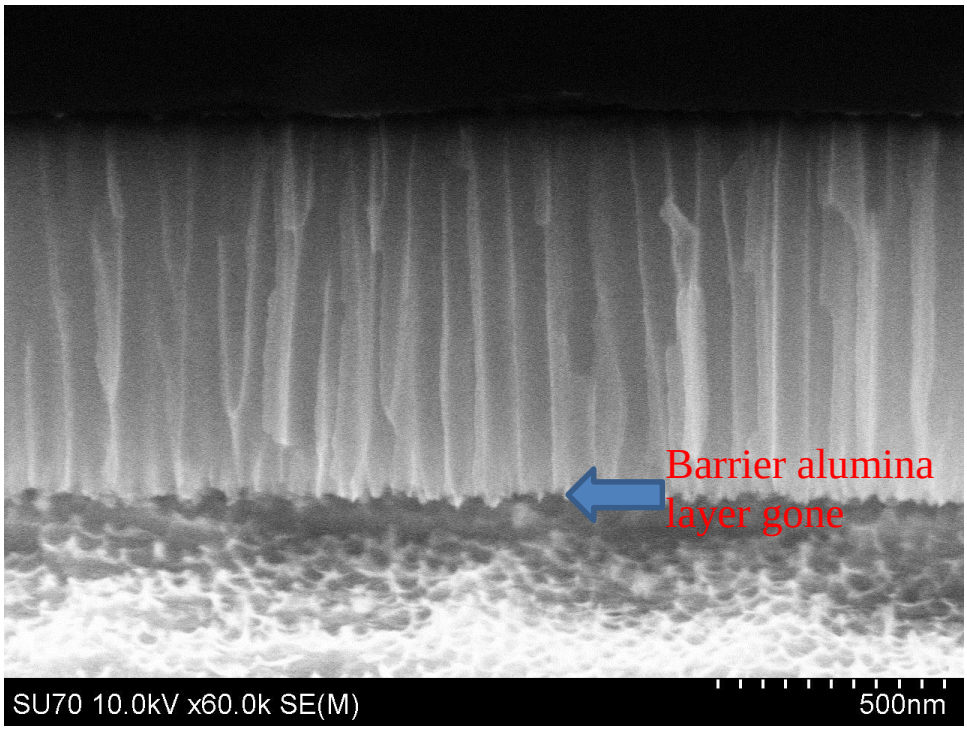


Figure 3.18: Cross Section SEM image of a sample after the gradual voltage reduction and after the 90 minute in 5% Phosphoric Acid alumina wet etching.

There were two ways to confirmed if the barrier layer was gone. First, visual check with a cross sectional SEM imaging, Figure 3.15. Second, a successful DC electroplating of any metal. One way to fill-up the pores was through DC electroplating. That techniques requires no barrier layer at the bottom of the pores. If the DC metal deposition was successful then it was a clear evidence that the alumina barrier layer was gone from the sample. Figure 3.19 and Figure 3.20 shows multiple images of pores filled with multiple metals through electroplating.

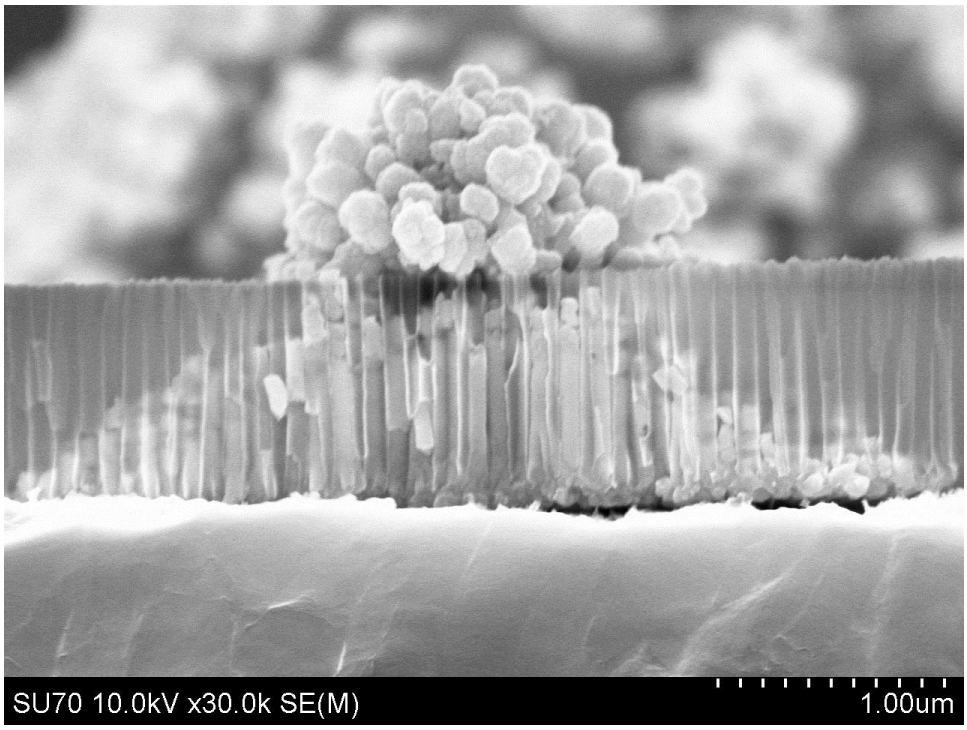


Figure 3.19: Cross section SEM image of AAO templates filled with Nickel.

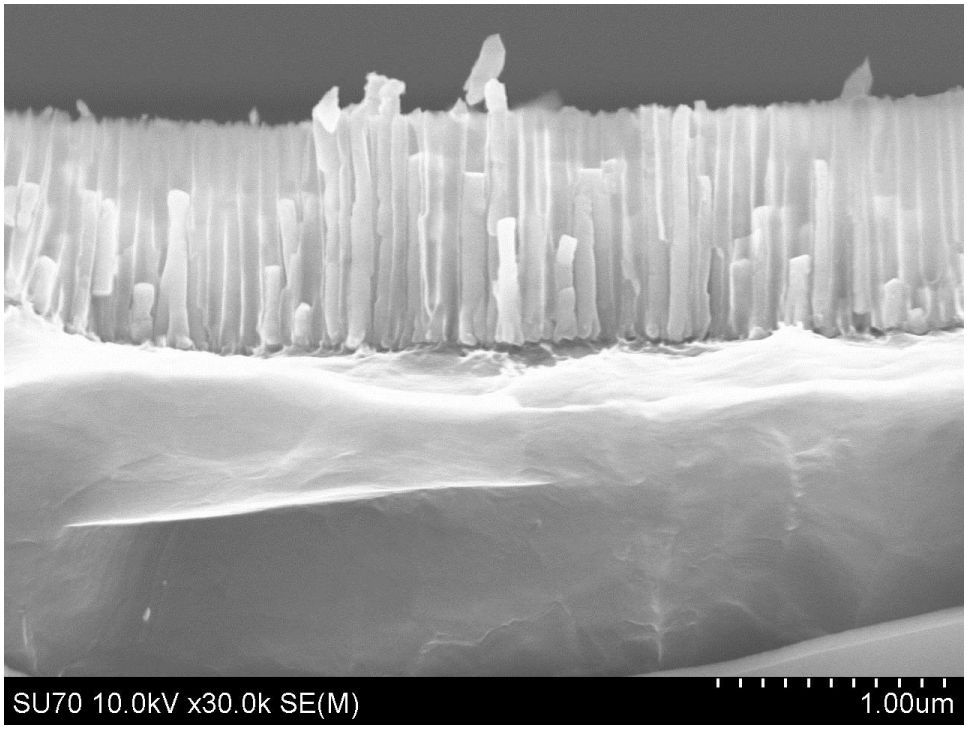


Figure 3.20: Cross section SEM image of AAO templates filled with Zinc.

The electrolyte for Nickel electroplating contained 0.1M NiSO4 ·6H2O and 0.1M H3BO3. While the electrolyte for Zinc DC electroplating contained 0.2M ZnSO4 ·7H2O and 0.1M H3BO3. Even though Zn was successfully deposited inside the pores through DC electroplating, it just filled about 20% percent of the pores across the sample. That was due to the natural process of Zn electroplating which happens randomly and there was not a good way to control the filling process.

3.6 Atomic Layer Deposition

Atomic layer deposition (ALD) is a very conformal process and the thickness of ZnO can be well controlled. ZnO ALD was chosen because we had more control of the deposition parameters and 100% of the pores were completely filled with ZnO. ALD is known also as a Pulsed Chemical Vapor Deposition technique. The ALD system deposits ZnO through pulses of Diethyzinc (DEZ) and DI water. The following parameters were used as the ALD ZnO deposition recipe:

- Number of Pulses: 800
- Temperature of Deposition: 90ºC
- Time of pulse: 20 ms

The thickness of the deposition was about 0.11μm and it took about 4.5 hours. Figure 3.21 and Figure 3.22 show a SEM top view and cross section of an AAO template after the ZnO ALD. It shows that 800 pulses were more than enough to cover the pores completely with a thin over layer.

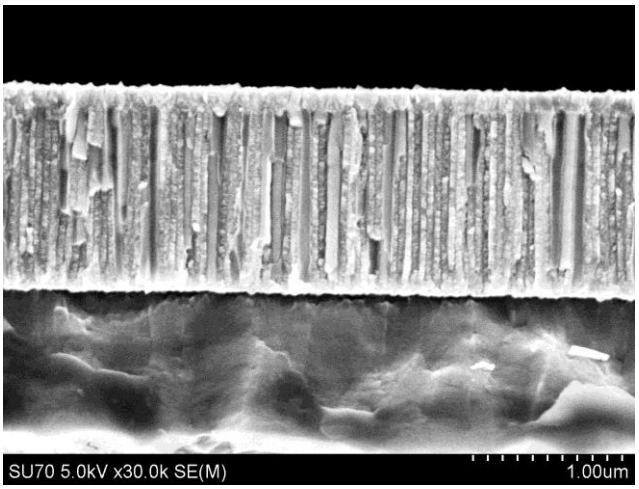


Figure 3.21: Cross Section SEM image of ZnO ALD used in for pressure sensor.

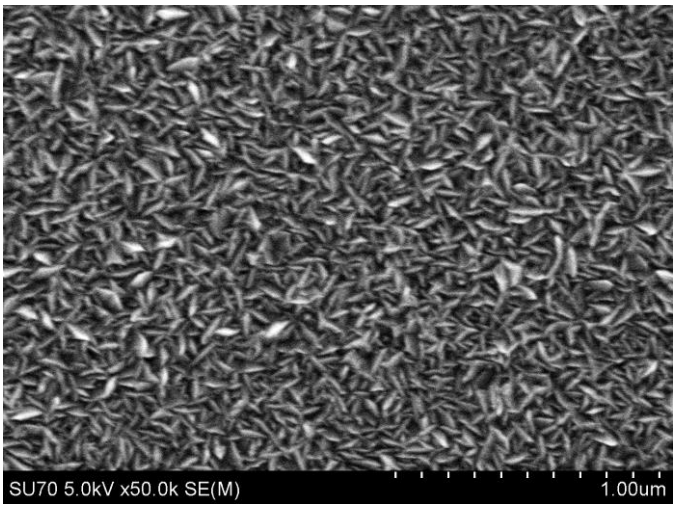


Figure 3.22: Top view SEM image of ZnO ALD used in for pressure sensor.

3.5 Nanowire Wet Etching Release.

The AAO membrane served as a template for the formation of the nanowires, but once the pores were filled with ZnO, the AAO membrane was no longer needed. However, as shown in figure 3.21, an excess thin layer of ZnO was left out at the top of the AAO template. A wet ZnO etching was first necessary prior the removal of the alumina layer. A solution of 330 ml of DI water and a droplet (0.02ml) of Hydrochloric Acid was used as etching solution. Figure 3.23 and Figure 3.24 show the ZnO sample etch with the HCl and DI water solution after 55 minutes.

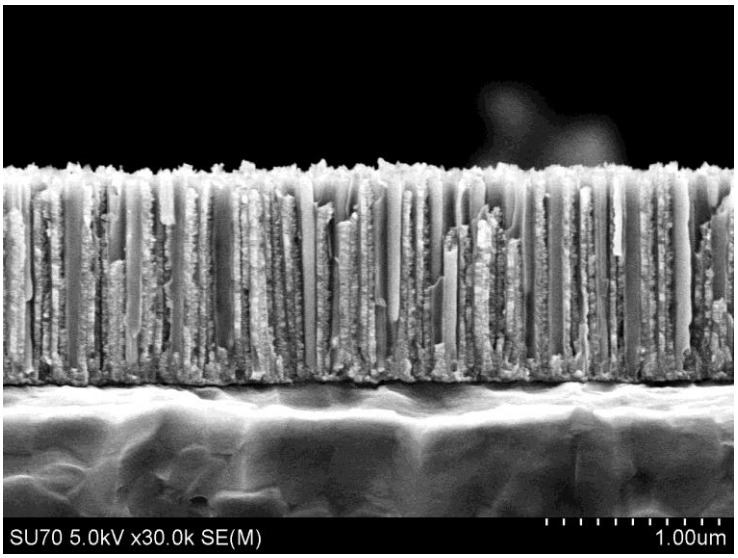


Figure 3.23: Cross Section SEM image of AAO templates filled with ZnO after 55 minutes ZnO wet etching using HCl-DI water solution.

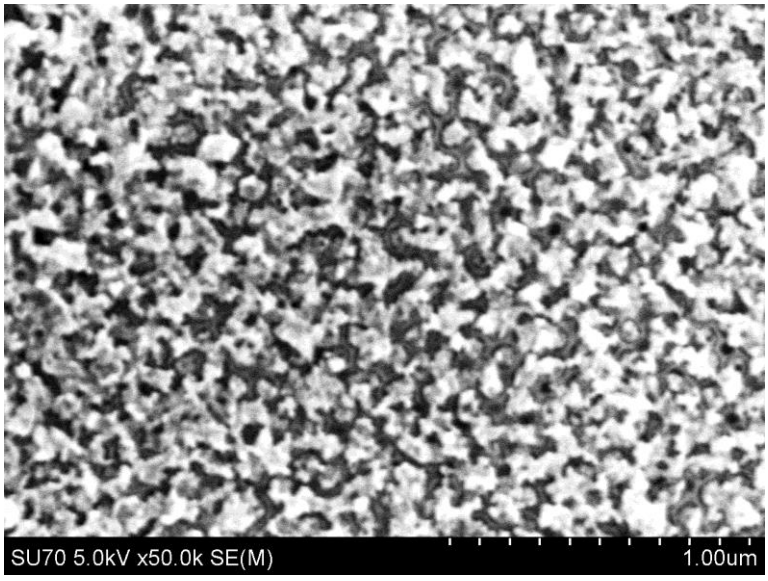


Figure 3.24: Top view SEM image of AAO templates filled with ZnO after 55 minutes ZnO wet etching using HCl-DI water solution.

The next step was to actually remove the AAO template and release the nanowires. It turned out that the Chromic-Phosphoric acid solution used previously was no longer useful because it also etches the ZnO nanowires. An etching solution that removes just the alumina without hurting the nanowires was needed. Buffered Oxide Etch (BOE), and Sodium Hydroxide were also tested as alumina etcher but the ZnO selectivity was really

low. Very diluted (0.5%) Potassium Hydroxide was successfully tested and the alumina layer was gone after 20 minutes. There were some unknown impurities left at the top oz the ZnO nanowires but that did not affect the wet etching of alumina, Figure 3.25. At the end, ultra high aspect ratio (700:8) ZnO nanowires were standing on the aluminum surface, Figure 3.26.

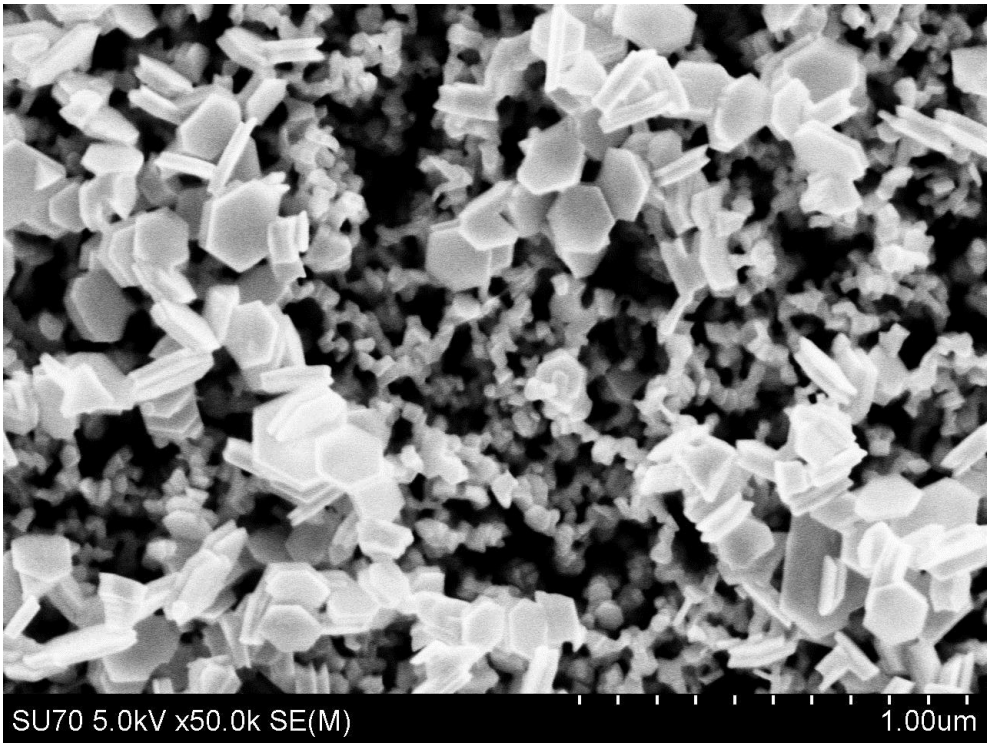


Figure 3.25: Top view SEM image of 5% KOH ZnO nanowire release after 20 minutes.

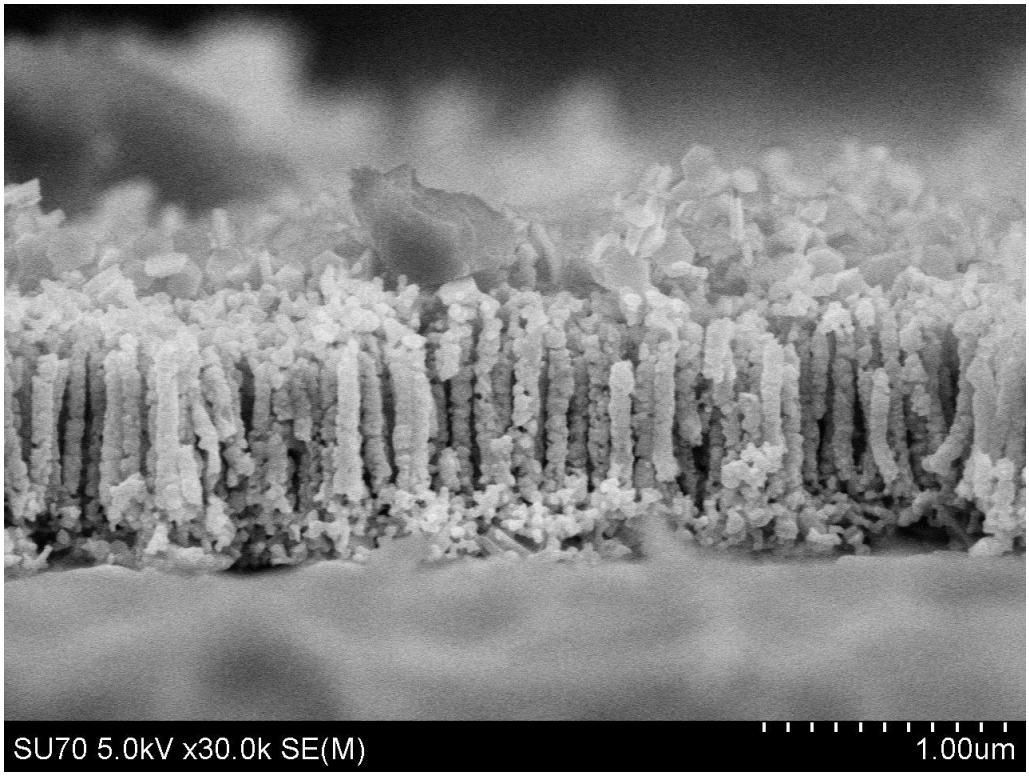


Figure 3.26: Cross Section SEM image of 5% KOH ZnO nanowire release after 20 minutes.

The pressure sensor is a combination of a MOSFET and the ultra-high aspect ratio ZnO nanowires. Figure 3.27 shows the final product after all the fabrication sequences.

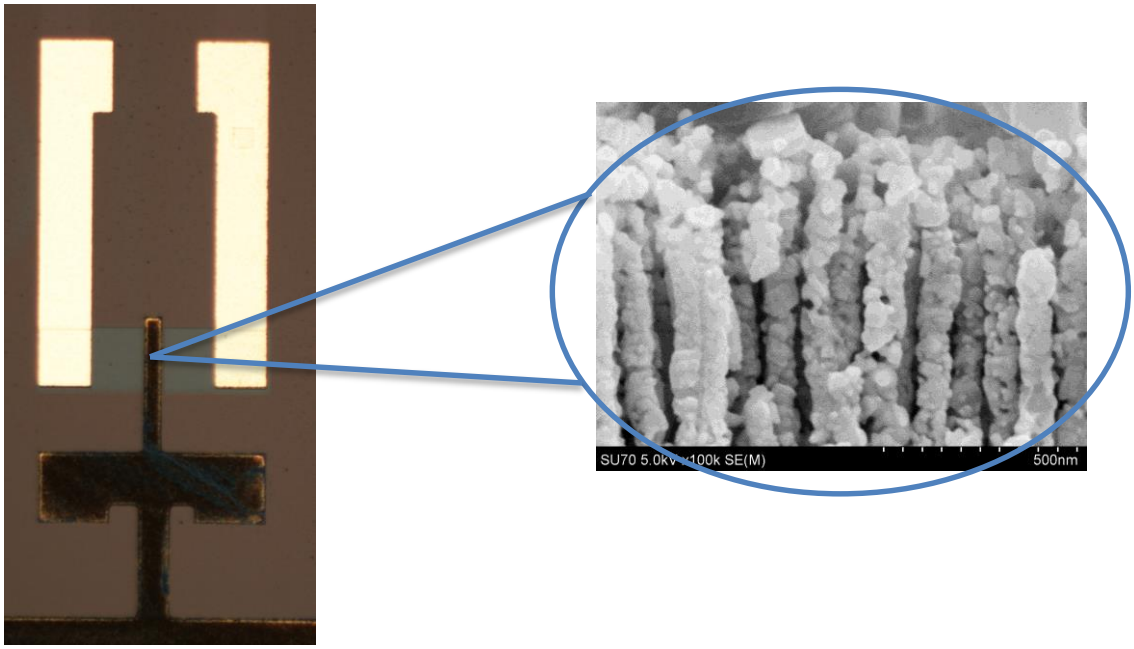


Figure 3.27: NMOS L=50µm W=500µm with Zinc Oxide nanowires on the gate.

Chapter 4 Characterization & Testing

4.1 Experimental Design

MOSFETs were specially design to be tested on a Cascade probe station connected to a HP Semiconductor Parameter Analyzer. The ultimate goal of the characterization of the device was to see if there was a response during a push of the nanowires. A sketch of the concept of the test is shown in Figure 4.1. Four probes were used to test the device:

1. SMU 1: Drain
2. SMU 2: Gate
3. SMU 3: Drain
4. Mechanical/Physical pressure (Ceramic Probe)

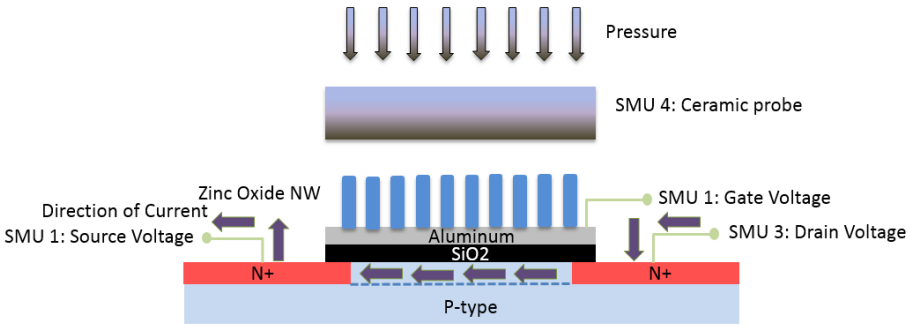


Figure 4.1: Stech of the concept of the test of the pressure sensor.

First of all, it was important to see how the MOSFET turned out without the nanowires on the gate and how that device responded with pressure at the gate. Then, the same experiment was completed with the MOSFET that had the ZnO nanowires on the gate. The following section will explain comparison of the characteristics during different points of operation of the transistors with ZnO nanowires and transistors without ZnO nanowires. A description of the actual testing set-up is shown in Figure 4.2 and Figure 4.3.

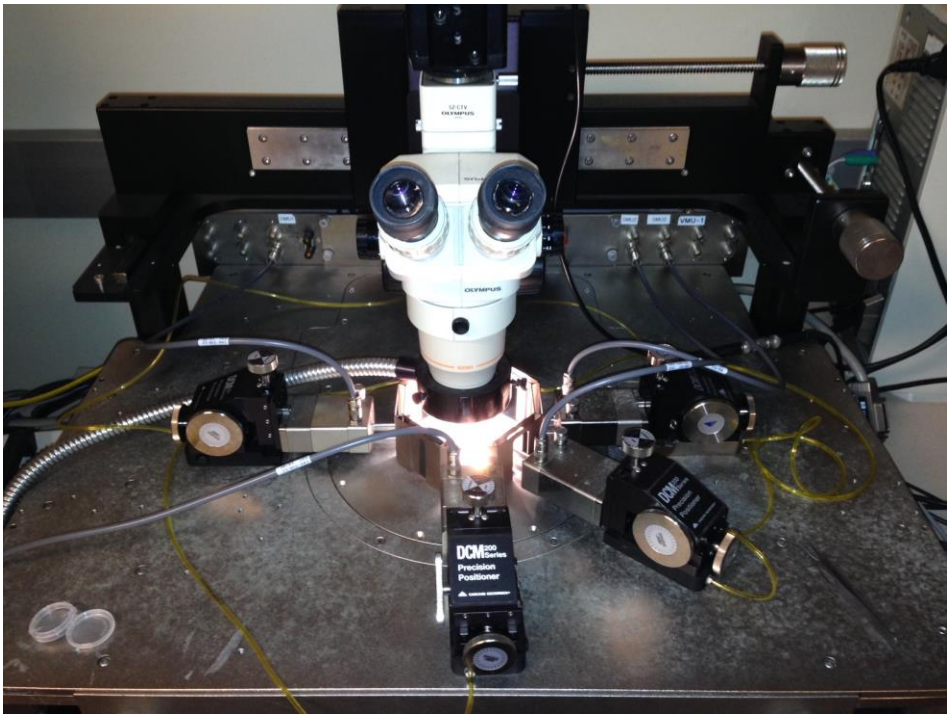


Figure 4.2: Cascade Probe station with 4 probes: SMU1, SMU2, SM3 and Mechanical/Pressure probe.

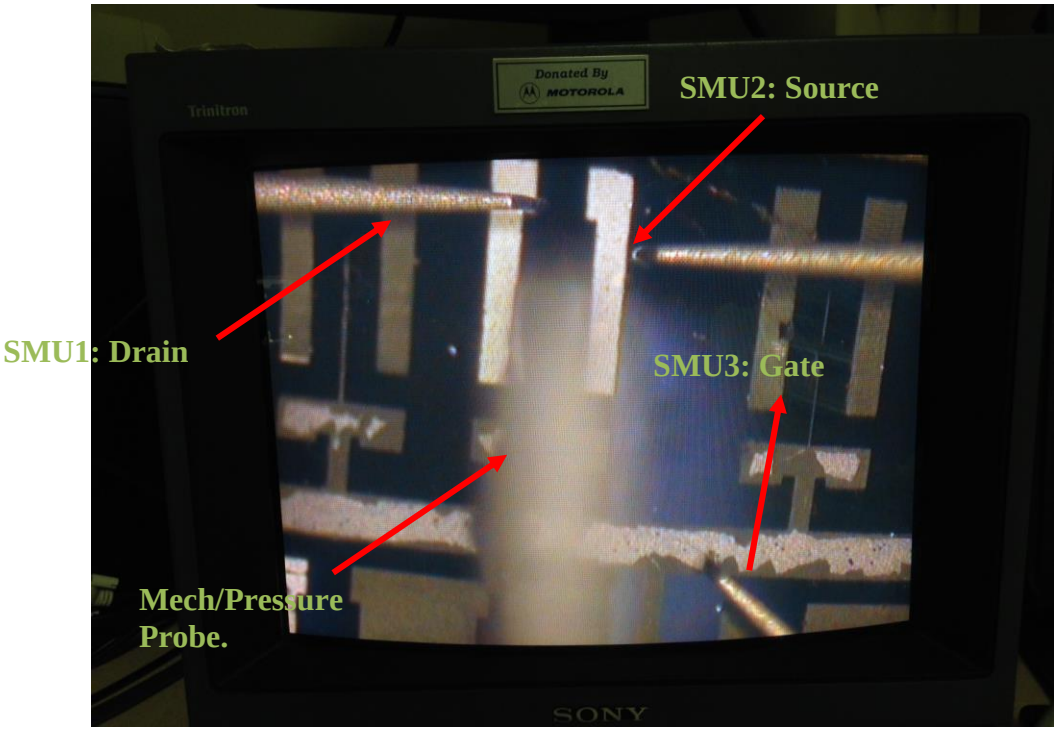


Figure 4.3: Description of the Cascade Probe station with 4 probes: SMU1, SMU2, SM3 and Mechanical/Pressure probe.

4.2 MOSFET Operation without nanowires

NMOS transistor without nanowires were characterized first. There were about 24 different kind of transistors on the wafer with different gate length, alignment tolerance and width of the source and drain. The drain current vs. drain voltage was the main parameter that was characterized. It has expected that piezoelectric nanowires would produce some kind of response in the drain current. Therefore, a drain current vs. drain voltage NMOS transistor extraction was needed. Id vs Vd family of curves was the most simple and convenient way to characterize NMOS transistor with and without nanowires. Out of 6 different die designs, just the die with alignment tolerance of 10µm, and transistor width of 500µm were carefully characterized in both way, with and without nanowires on the gate. The wafer that had no ZnO nanowires went through a 400°C sinter process for 20 minutes after the metal lithography. That is a process usually done for MOSFETs to alloy metal contacts. In the other hand, the wafer that went through the ZnO nanowire fabrication process, did not go through the standard sinter process. MOSFETs with ZnO nanowires just had a long low temperature (90°C) sinter process during the 4.5 hours in the Zn ALD step. Figure 4.4 shows the I-V characteristics of a NMOS without nanowires with the 400°C sinter process. While in Figure 4.5 shows the same kind of measurement but this time on a MOSFET with ZnO NW without any pressure on the gate.

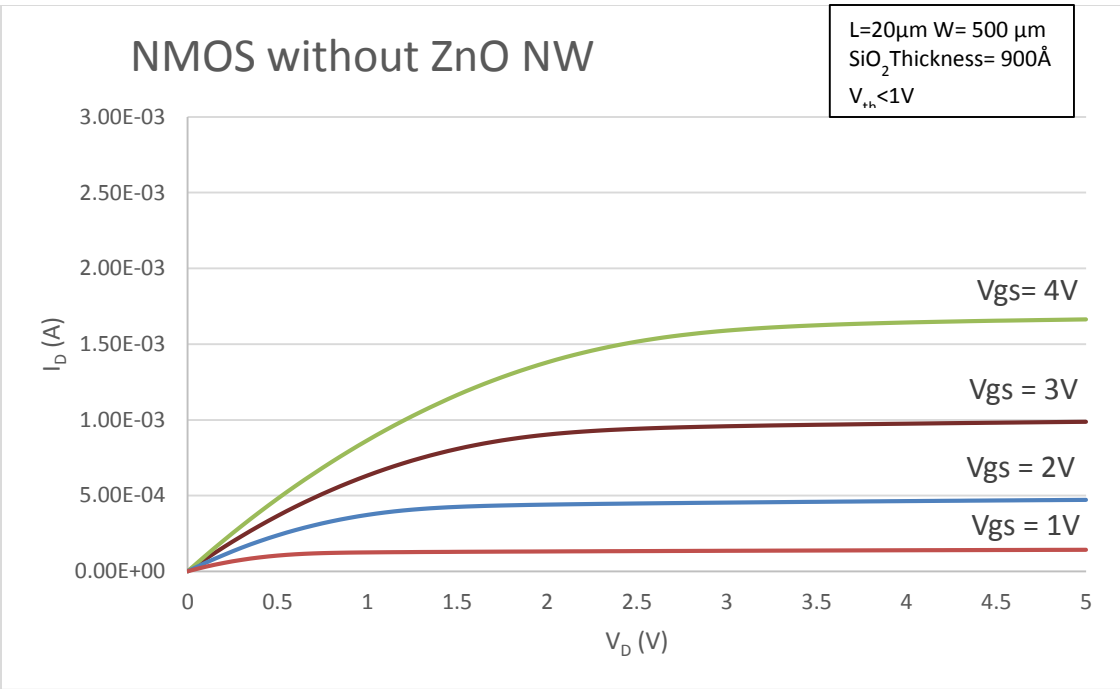


Figure 4.4: Id Vs. Vd of NMOS with a 20 min- 400°C sinter process.

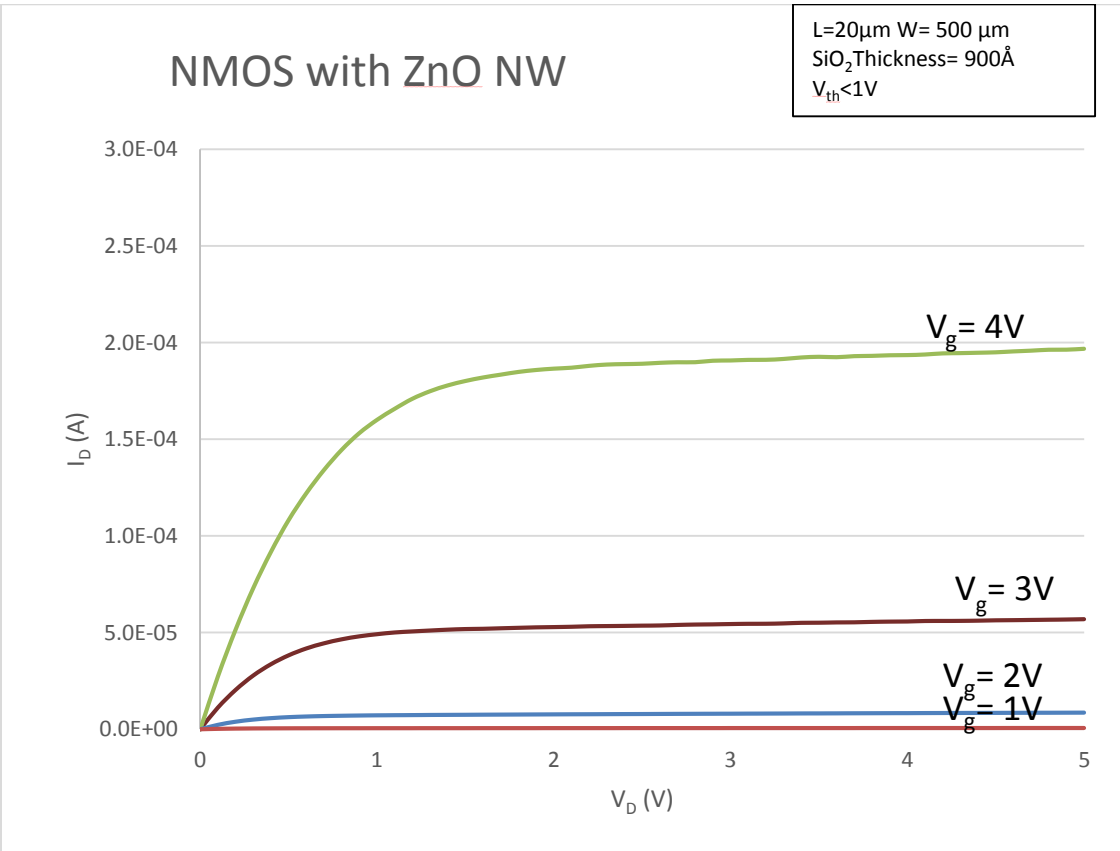


Figure 4.5: ID Vs. VD of NMOS with a 4.5 hours 90°C sinter process during ZnO ALD.

The main difference between the two devices was that the drain current dropped by one order of magnitude. One of the reason of the drain current drop was because there was a higher contact resistance in the device that had no 400°C sinter process. Regardless of this drain current drop, it was demonstrated that the NMOS with ZnO NW on the gate still has a threshold voltage of less than 1V and had the three operation modes of MOSFET (triode and saturation mode). Future work will required to actually meet the same characteristics of the same device with and without nanowires.

4.3 MOSFET operation of device without nanowires.

One way to understand the actual response of the drain current due to the pressure of the ZnO nw on the gate, was to find out if there was a response in the drain current with the device without nanowires during the ceramic probe was actually making pressure on the gate. Silicon is piezoresistive so there should be some effect from pressing on it. It was very important to know the magnitude of the piezoresistance effect in the silicon MOSFET and how large the overall effect is relative to that. Figure 4.6 shows a combination of I_D vs V_D characteristic of the MOSFET device that has no ZnO nanowires during a mechanical pressure on the gate.

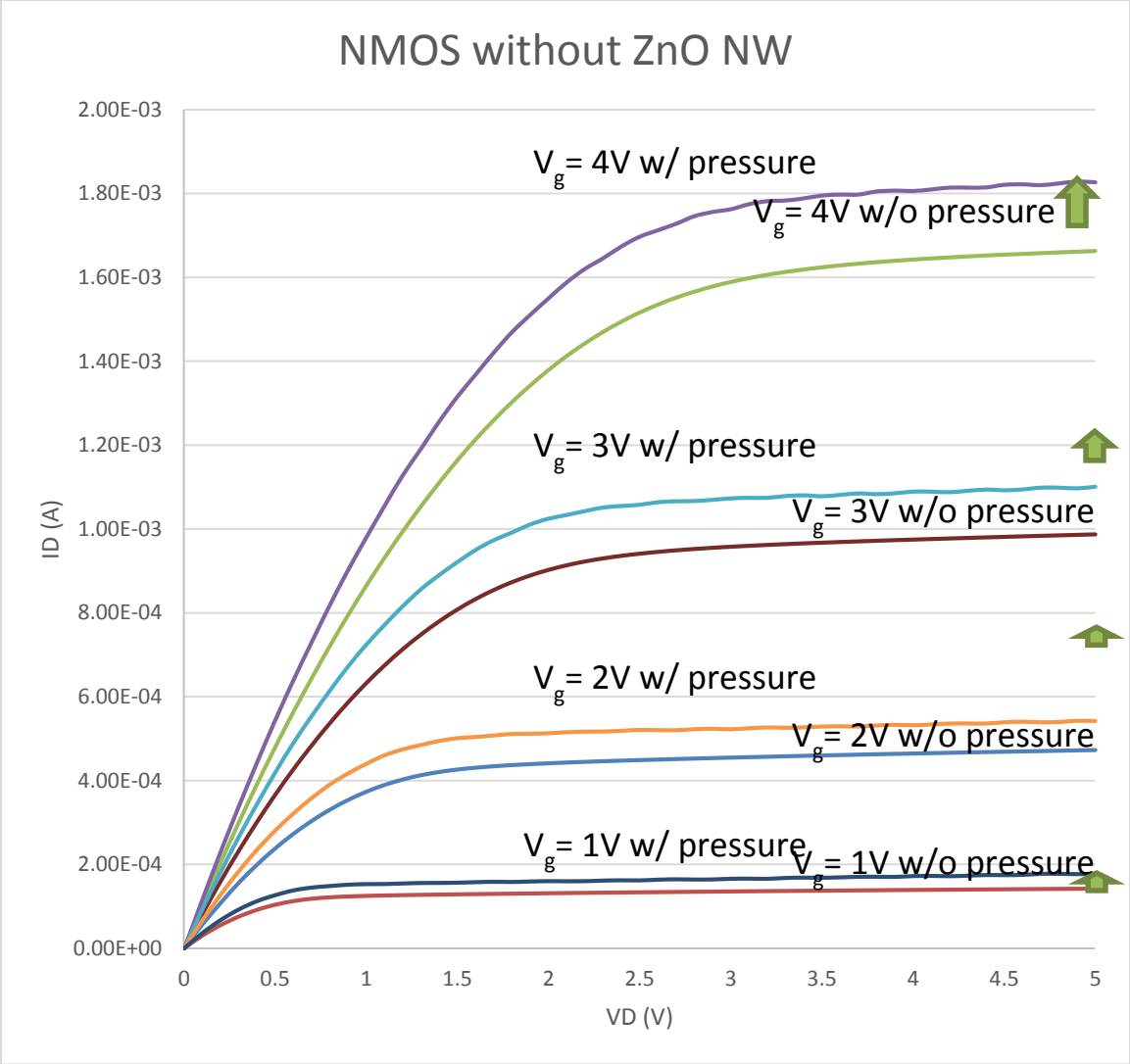


Figure 4.6: ID Vs. VD of NMOS with a 4.5 hours 90°C sinter process during ZnO ALD.

It seems that the MOSFET has some response in the drain current just with the ceramic probe making pressure right on the gate. The overall percentage response for the transistor without nanowires is presented in Figure 4.7.

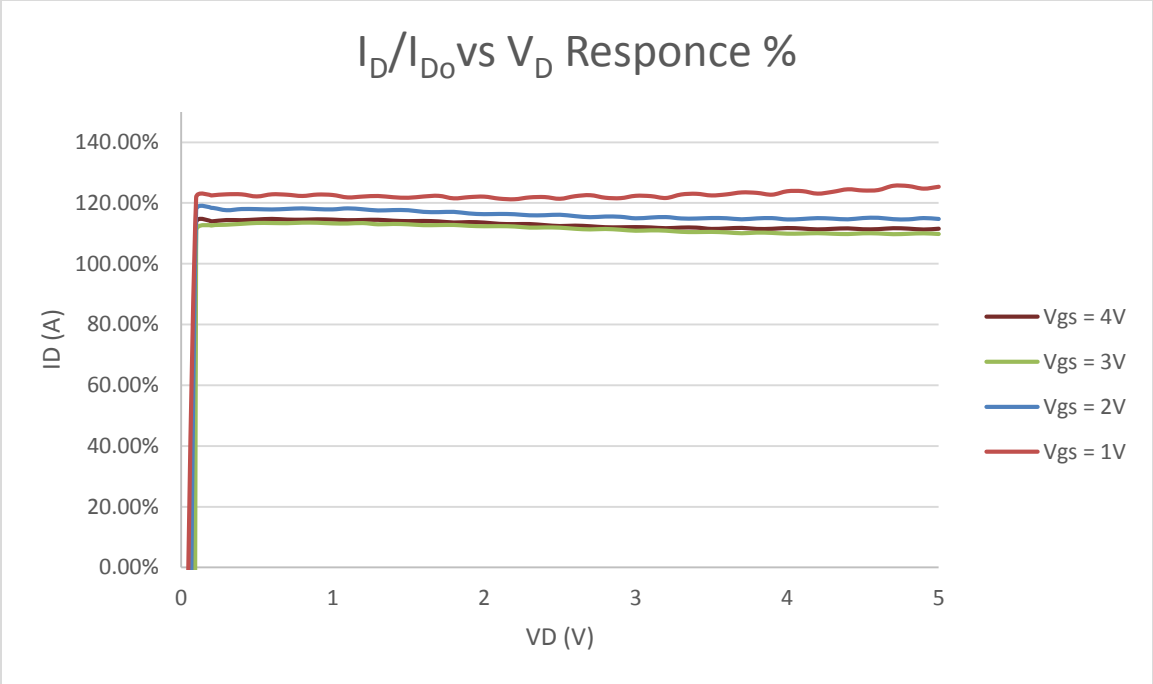


Figure 4.7: Overall response of NMOS device without ZnO NW.

4.4 MOSFET Operation with nanowires

NMOS transistor with the same characteristics were measured but this time with the ZnO nanowires on the gate of the transistor. There are two different stages during the operation of the nanowire pressure sensor. The first stage is where nanowires standing at the gate without any pressure. The second stage is where a mechanical force is applied right at the gate of the NMOS transistor. Both stages have different drain current. Figure 4.8 and Figure 4.9 shows a comparison between nanowires with pressure and no pressure. It was confirmed that there is a positive increase of drain current while the ZnO nanowires where under mechanical pressure.

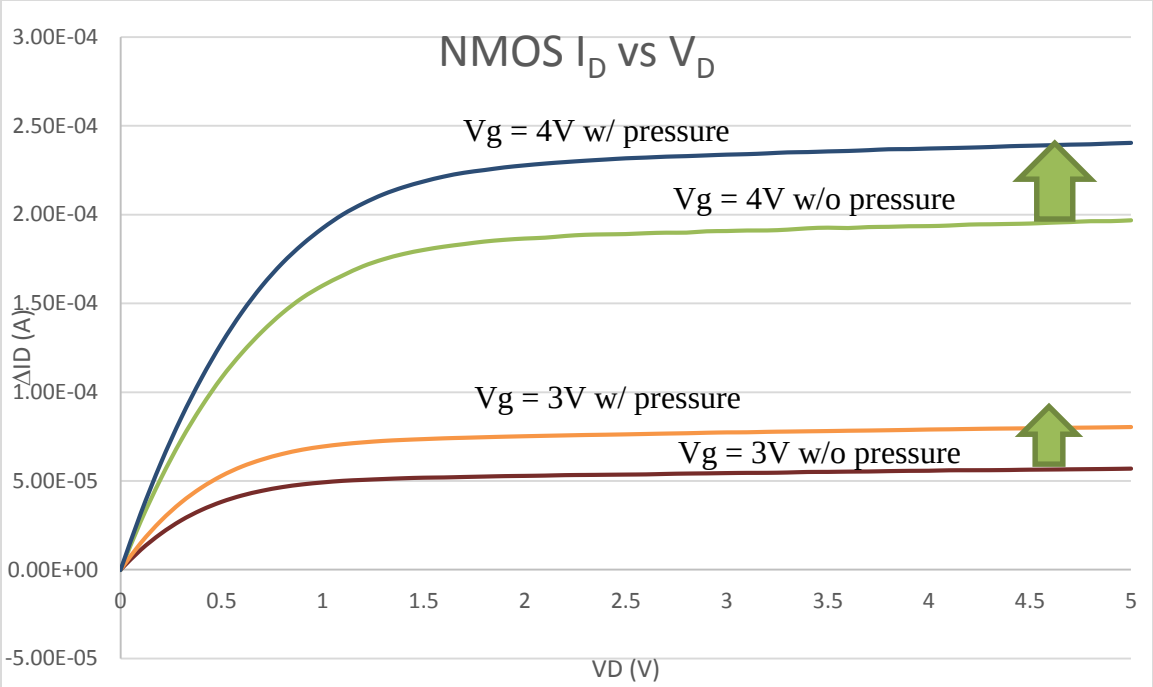


Figure 4.8: Comparison of transistor behavior with and without mechanical pressure for Vg= 4V and Vg= 3V.

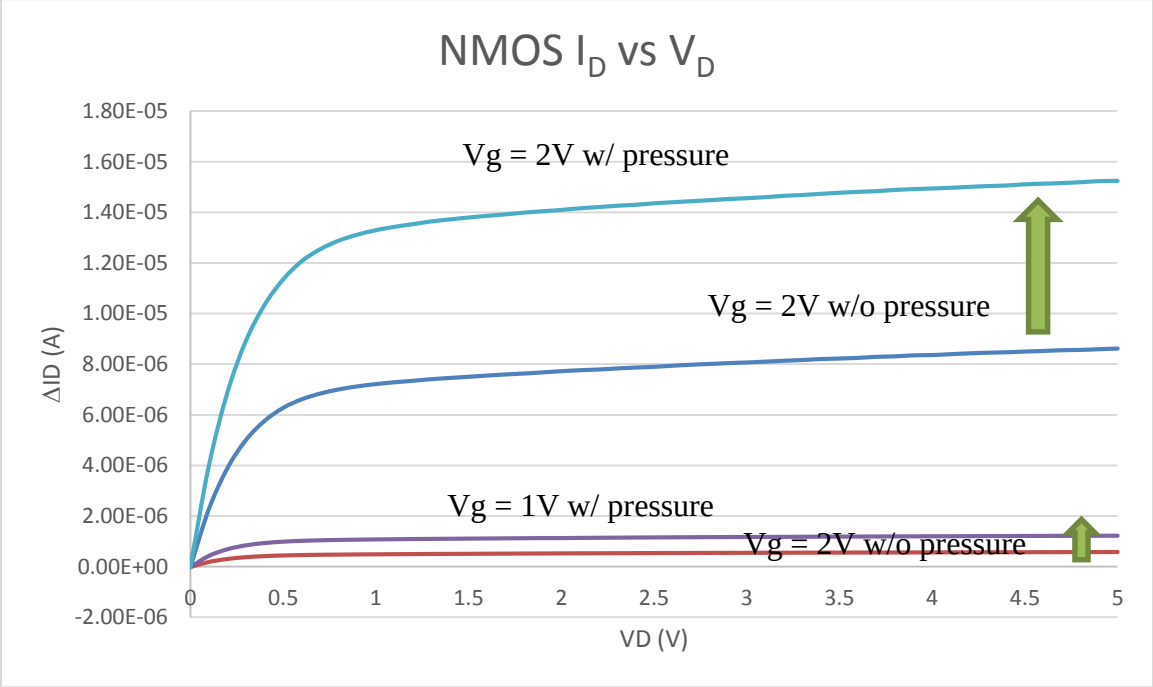


Figure 4.9: Comparison of transistor behavior with and without mechanical pressure for Vg= 2V and Vg=1V.

There was a jump in drain current while the ZnO nanowires where under pressure. For instance, Figure 4.10 shows what was the percentage difference in the drain current

when the sensor was with and without pressure. It seems that there is a bigger response of the transistor when it is at low gate voltage.

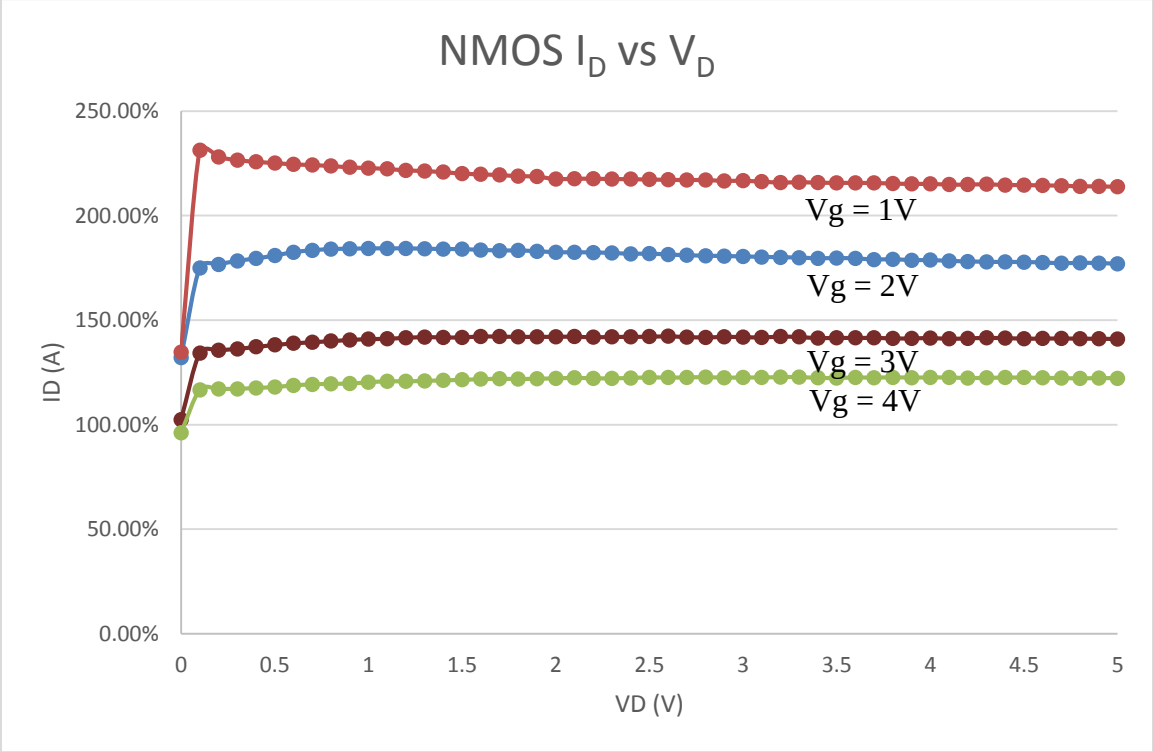


Figure 4.10: Overall response of NMOS device with ZnO NW.

4.5 Overall gain due to piezoelectric effect of ZnO Nanowires

The response drain current in the MOSFET device was due to two factor:

1. Silicon MOSFET piezoresistant effect
2. Piezoelectric ZnO nanowires effect.

To calculate the actual contribution of the ZnO nanowires in the drain current, the piezoresist effect was subtracted to the actual device with ZnO NW. Figure 4.11 shows the actual percentage response of the device due to the piezoelectric effect of the ZnO NW on the gate of the MOSFET.

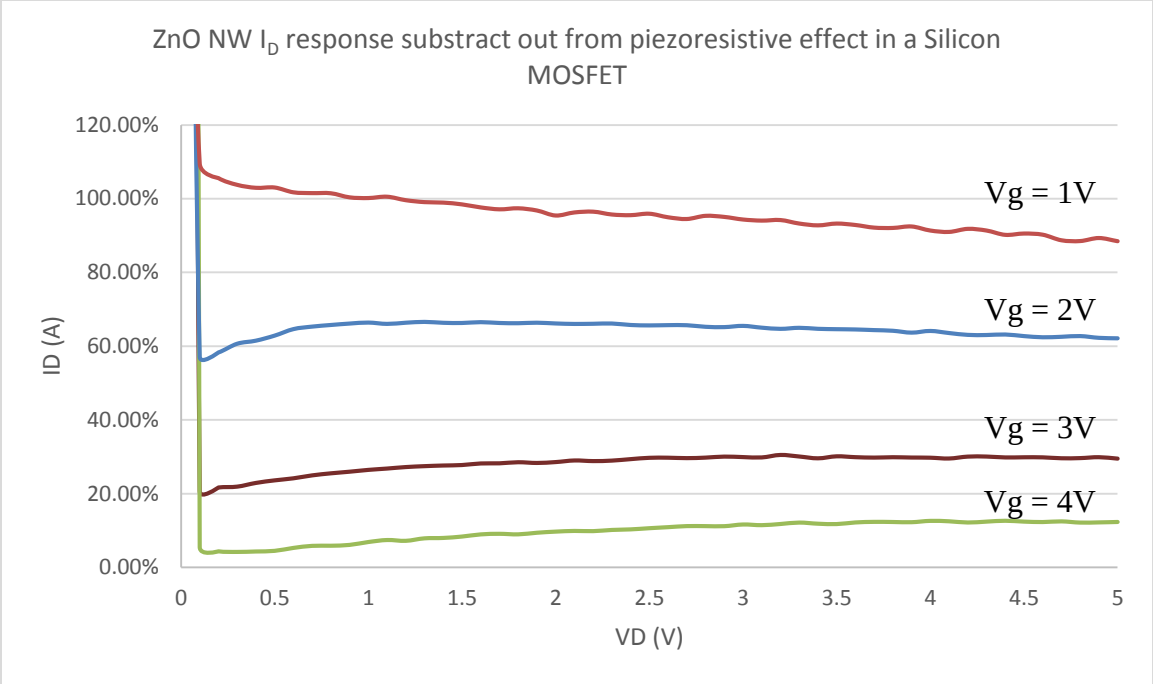


Figure 4.11: ZnO NW ID response subtracted out from piezoresistive effect in a Silicon MOSFET.

Chapter 5 Conclusions and Recommendation for Future Work

In this work a proof-of-concept ZnO nanowire MOSFET pressure sensor was demonstrated. The pressure sensor relied on a low temperature nanowire fabrication process that was integrated onto the gate of a simple NMOS transistor. The ZnO nanowire MOSFET pressure sensor showed significant response (give a number), beyond the expected response due to piezoresistivity. It appears that the additional response is due to the piezoelectric potential generated on the gate of the MOS transistor due to the ZnO nanowires.

The ZnO Nanowire MOSFET pressure sensor was fabricated using a self-assembled template of alumina nanopores. The optimization of the nanopores alumina template consisted of optimizing:

1. Aluminum deposition for self-assembly AAO templates on a silicon wafer on top of SiO_2.
2. Multistep anodization on thin aluminum layers.
3. Barrier alumina layer removal, through gradual voltage reduction.

Nanopores of 80nm diameter and 1μm height (100:8 aspect ratio) were fabricated using this technique in layers of aluminum that were 2.4 μm thick.

Ultra-high aspect ratio ZnO nanowires were fabricated in the alumina nanopores using atomic layer deposition. This process demonstrated the high aspect ratio filling of the nanopores template using ALD, as well as the direct contact between Al MOS gate and the ZnO nanowires. Nanowires were fabricated with a diameter of 80 nm and 800 nm height (80:8 aspect ratio). The aspect ratio of the nanowires is somewhat less than that of the

nanopores, due to some loss in thickness of the nanowires during the release process to dissolve the alumina template. This process was also demonstrated over large areas and multiple devices on a silicon wafer.

The proof-of-concept ZnO Nanowire MOSFET pressure sensor was tested with mechanical stress applied to the nanowires gate of the MOSFET. The sensor showed a 110% response due to pressure, even with the expected piezoresistive response of the silicon device removed from the measurement.

There is still more work needed to fully understand and take advantage of the pressure sensor device. Even though ZnO ALD is widely used in nanotechnology, a deeper and more thorough film characterization is needed. Crystal structure of the ZnO ALD used in this work needs a more characterization. It is believed that the ZnO ALD was in the c-direction, yet it need to be confirmed by X-ray Diffraction techniques. It might be that the ZnO layer has a better potential if it is in other crystal structure.

It has demonstrated that the devices has different characteristics if it goes through a high temperature sintering process. The pressure sensor just went through a 4.5 hour low temperature (90°C) sintering process during the ZnO ALD. It was seemed that there was a higher contact resistance with the low temperature sintering process. Even though it did not affect the proof-of-concept of response of the ZnO nanowires, it is believed that a high temperature sintering process could improve the crystal structure to make it a single crystal and maybe make it a more sensitive pressure sensor.

Empty pores of about 1μm tall by 80 nm width were fabricated by the combination of the multistep anodization and barrier layer removal process. These pores could be filled by any other material through electroplating or chemical vapor deposition. ALD was

demonstrated that the pores were filled in a very conformal and uniform matter. There are common ALD materials that could be used to fill the pores with:

- Oxides
    - HfO_2, La_2O_3, TiO_2, ZrO_2, Ta_2O_5, In_2O_3, SnO_2, ITO, FeO_x, NiO2, MnO_x, Nb_2O_5, MgO, NiO, Er_2O_3
- Nitrades
    - WN, Hf_3N_4, AIN, TiN, TaN, NbN_x
- Metals
    - Ru, Pt, W, Ni, Co
- Sulphides
    - ZnS

ZnO is widely known piezoelectric material and it is used in different kind of applications [7]. Bending of the ZnO nanowires will produce a potential across them. This bending could not be only by making pressure on the top of the nanowire. It could be that the nanowires will bend by the flow of some gas material such as Oxygen or Ammonia. Therefore, a chemical or biosensor could be fabricated with the same optimization process described in this work.

The ZnO nanowire fabrication technique descripted in previous chapters was also attempted on a sapphire substrate with a buffer of GaN. The process was 100% compatible and the AAO template was completed filled with ZnO. Figure 5.1 shows a cross section of the self-assembly fabrication technique of a sapphire GaN device.

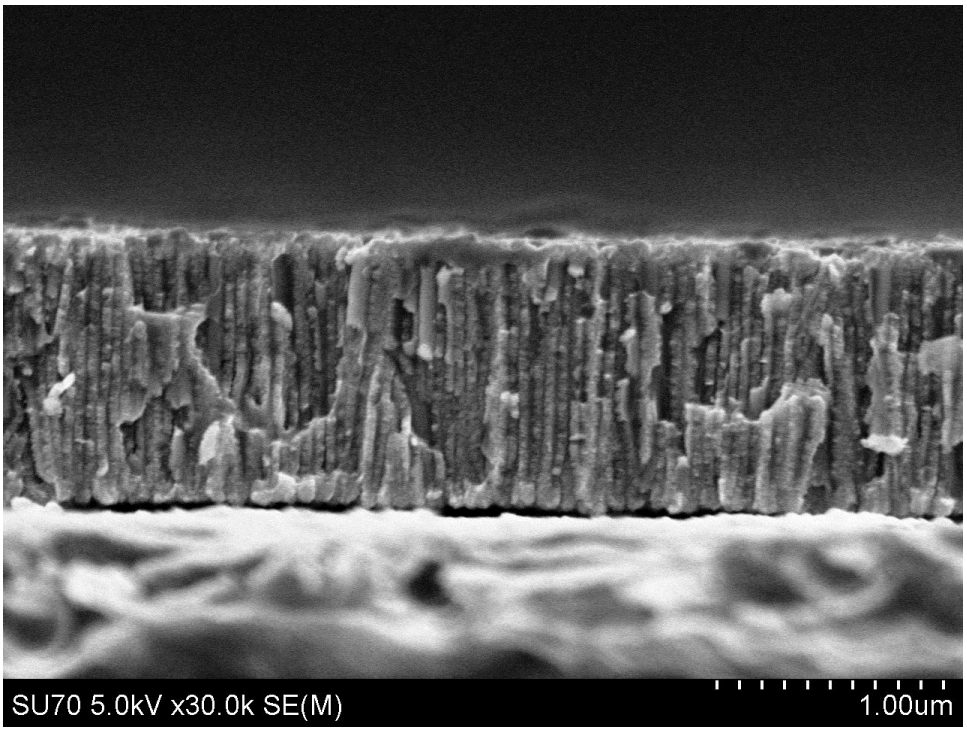


Figure 5.1: SEM cross section of an AAO template filled with ZnO on a sapphire substrate with a GaN device.

The ZnO nanowire pressure sensor could be more responsive if there is a layer of ZnO right underneath the ZnO nanowires. A sketch diagram of the concept of the idea is shown in Figure 5.2. That concept was attempted on a sapphire substrate with a GaN device and ZnO layer on top. The fabrication sequence was also compatible with this type of substrate/device. Figure 5.3 shows the AAO template with almost no Al residual at the bottom of the pores. This demonstrates that the idea of the concept of having a ZnO buffer layer could be possible in the future.

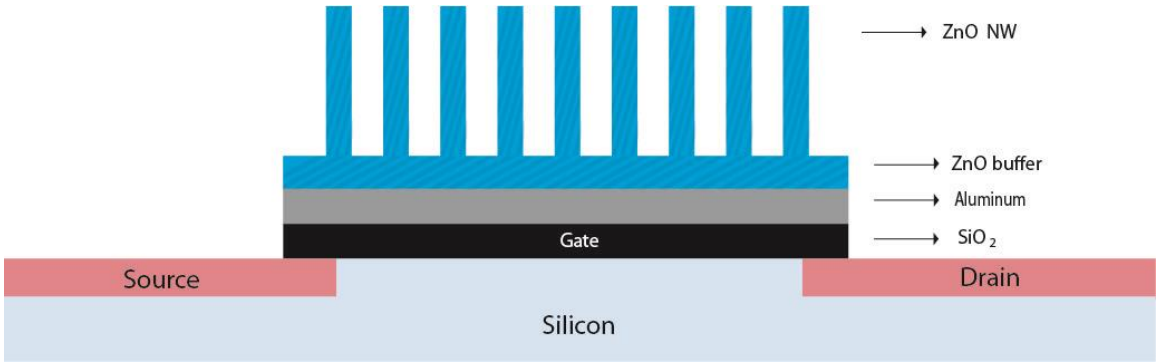


Figure 5.2: Device concept made of ZnO nanowires with a ZnO buffer on top of the gate of a MOSFET.

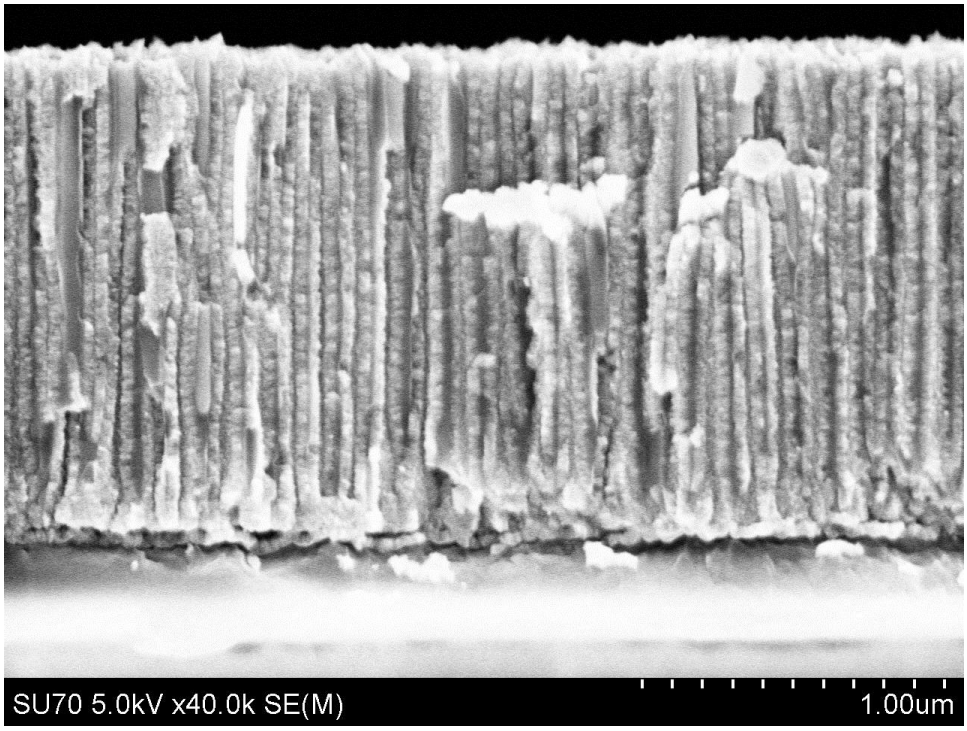


Figure 5.3: SEM cross section of an AAO template filled with ZnO on a sapphire substrate with a GaN device with a ZnO buffer layer.

The electrochemical self-assembly technique to fabricate highly ordered nanowires was demonstrated that is a low temperature process. That means that it could be compatible with a CMOS fabrication process. More work could be put into this area to actually fabricate a more complex device with a more complex digital architecture.

Appendixes

A. List of Abbreviations
B. Deckbuild code used for NMOS simulation

A. List of Abbreviations

ALD	Atomic Layer Deposition
AAO	Anodic Aluminum Oxide
CMOS	Complementary Metal-Oxide-Semiconductor
DEZ	Diethyzinc
DI	Deionized water
DI	Deionized (water)
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
Pb	Lead
PZT	Lead Zirconate Titanate
Ti	Titanium
VMC	Virginia Microelectronics Center
VLSI	Very Large System Integration
XRD	X-ray Diffraction
ZnO	Zinc Oxide
Zr	Zirconium

B. Simulation code used in Athena

```
go athena

# Grid Define

#
line x loc=0.00 spac=0.25
line x loc=5 spac=0.25

#
line y loc=0.00 spac=0.02
line y loc=1 spac=0.04
line y loc=2 spac=0.1
line y loc=3 spac=0.2
line y loc=5 spac=0.4

# Starting Wafer Specs
init silicon boron resistivity=5 orientation=100

# Mask Ox for NMOSFET (7800A)
diffus time=150 temp=1000 weto2
extract name="Ox Thickness" thickness material="SiO~2" mat.occno=1 x.val=4.9

#
deposit photoresist thick=1.00


#  Photoresist etch for N-Type Regions

 etch photoresist start x=1.5 y=3.00
 etch cont x=3.5 y=3.00
 etch cont x=3.5 y=-5.00
 etch done x=1.5 y=-5.00


etch oxide start x=1.5 y=3.00
 etch cont x=3.5 y=3.00
 etch cont x=3.5 y=-5.00
 etch done x=1.5 y=-5.00

#
etch photoresist all

# N-Type Doping Source and Drain
diffus time=30 temp=1100 nitro c.phosphor=1.0e20
```

```
#
etch oxide all

# Gate Oxidation
diffus time=190 temp=1000 dryo2
extract name="Ox Thickness" thickness material="SiO~2" mat.occno=1 x.val=4.9

# GATE Oxide Etch

 etch oxide start x=1.5 y=3.00
 etch cont x=3.5 y=3.00
 etch cont x=3.5 y=-5.00
 etch done x=1.5 y=-5.00


extract name="GateOxThickness" thickness material="SiO~2" mat.occno=1 x.val=5


#
deposit aluminum thick=0.10

# Metal etch
 etch aluminum start x=0 y=3.00
 etch cont x=0.75 y=3.00
 etch cont x=0.75 y=-5.00
 etch done x=0 y=-5.00

etch aluminum start x=3.75 y=3.00
 etch cont x=4.5 y=3.00
 etch cont x=4.5 y=-5.00
 etch done x=3.75 y=-5.00

# extract a curve of conductance versus bias.
extract start material="Oxide" mat.occno=1 \
        bias=0.0 bias.step=0.2 bias.stop=2 x.val=4.9
extract done name="sheet cond v bias" \
        curve(bias,1dn.conduct material="Silicon" mat.occno=1  region.occno=1)\
        outfile="extract.dat"

# extract the long chan Vt
extract name="n1dvt" 1dvt ntype vb=0.0 qss=1e10 x.val=4.9

#
extract name="NMOSVT" 1dvt ntype x.val=4.9

# extract final S/D Xj
```

```
extract name="nxj" xj silicon mat.occno=1 x.val=2.5 junc.occno=1

# extract the N++ regions sheet resistance
extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1 x.val=2.5
region.occno=1

# extract the surface conc under the channel.
extract name="chan surf conc" surf.conc impurity="Net Doping" \
        material="Silicon" mat.occno=1 x.val=4.9

#
struct mirror right

extract name="NMOS VT" 1dvt ntype    x.val=5


electrode name=gate x=5 y=0.2
electrode name=source x=2.5
electrode name=drain x=7.5
electrode name=substrate backside

structure outfile=Nmos1ex01_0.str

############## Vt Test : Returns Vt, Beta and Theta ################
go atlas

# set material models
models cvt srh print

contact name=gate aluminum
interface qf=3e10

method newton
solve init

# Bias the drain
solve vdrain=1

# Ramp the gate
log outf=Nmos1ex01_1.log master
solve vgate=-1 vstep=1 vfinal=3.0 name=gate
save outf=Nmos1ex01_1.str

# plot results
tonyplot  Nmos1ex01_1.log -set Nmos1ex01_1_log.set
```

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