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GaN heterojunction FET device Fabrication, Characterization and Modeling

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GaN heterojunction FET device Fabrication, Characterization and Modeling

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at Virginia Commonwealth University

by

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Table of Contents

List of Figures

R_{fdg} and R_{fgs} considered. (b) C_{dg}, C_{gs}, and C_{ds} . (c) g_m and τ. (d) Measured (×) and simulated (line) S parameters.

Figure 5.1 A schematic represents the difference result from quantum DD model and classic DD model.

Figure 5.2 A schematic on axis definition and nomenclatures used for modeling.

Figure 5.3 Flow chart of the numerical calculation procedure for self-consistent Schrödinger-Poisson equations.

Figure 5.4 (a) Calculated conduction band profile, electron distribution, and eigenenergy/wavefunction for the first three sub-bands in an AlGaN/GaN heterojunction. (b) Band structure for AlGaN/GaN HFET structure with and without an AlN spacer; electron density distributions is shown in the insert.

Figure 5.5 Conduction band profile with and without the electromechanical coupling in effect in an AlGaN/GaN heterojunction.

Figure 5.6 Carrier distribution for (a) different Al% in AlGaN/GaN HFETs structure, (b) different shallow donor concentration in AlGaN/GaN HFETs structure.

Figure 5.7 (a) Sheet carrier density dependence on AlGaN barrier thickness, with and without 1 nm AlN spacer. (b) Sheet carrier density dependence on AlN thickness in AlGaN/AlN/GaN HFETs structure; the electrical field distribution in AlGaN/AlN/GaN HFETs structure with 1nm AlN spacer is shown also.

Figure 5.8 The band diagram for an AlGaN/GaN HFETs structure with AlN spacer, when the Schottky gate is negatively biased at Vgs = -2.0V.

Figure 5.9 In the AlGaN/GaN HFETs structure with 1nm AlN spacer, (a) the dependence of sheet carrier density on the applied gate voltage, and(b) The calculated and measured capacitance

0.5V and -1.0V.

Figure 5.21 Device structures and dimensions used in the APSYS simulation.

Figure 5.22 The potential contour and field distribution along the the AlGaN/GaN interface for (a) conventional HFETs; (b) n+ cap recess gate HFETs; (c) HFETs with field plate under V_{DS} = 10V, V_{GS}=-5V bias.

List of Tables

ABSTRACT

GaN heterojunction FET device Fabrication, Characterization and Modeling

By Qian Fan, Ph.D

A dissertation submitted in partial satisfaction of the preliminary examination requirements for the degree of Doctor of Philosophy in Electrical and Computer Engineering at Virginia Commonwealth University

Director: Dr. Hadis Morkoç

This dissertation is focused on the research efforts to develop the growth, processing, and modeling technologies for GaN-based Heterojunction Field Effect Transistors (HFETs). The interest in investigating GaN HFETs is motivated by the advantageous material properties of nitride semiconductor such as large band gap, large breakdown voltage, and high saturation velocity, which make it very promising for the high power and microwave applications.

Although enormous progress has been made on GaN transistors in the past decades, the technologies for nitride transistors are still not mature, especially concerning the reliability and stability of the device. In order to improve the device performance, we first optimized the growth and fabrication procedures for the conventional AlGaN barrier HFET, on which high carrier mobility and sheet density were achieved. Second, the AlInN barrier HFET was successfully processed, with which we obtained improved I-V characteristics compared with conventional structure. The lattice-matched AlInN barrier is beneficial in the removal of strain, which leads to better carrier transport characteristics. Furthermore, new device structures have been examined, including recess-gate HFET with n+ GaN cap layer and gate-on-insulator HFET, among which the insertion of gate dielectrics helps to leverage both DC and microwave performances.

In order to depict the microwave behavior of the HFET, small signal modeling approaches were used to extract the extrinsic and intrinsic parameters of the device. An 18-element equivalent circuit model for GaN HFET has been proposed, from which various extraction methods have been tested. Combining the advantages from the cold-FET measurements and hot-FET optimizations, a hybrid extraction method has been developed, in which the parasitic capacitances were attained from the cold pinch-off measurements while the rest of the parameters from the optimization routine. Small simulation error can be achieved by this method over various bias conditions, demonstrating its capability for the circuit level design applications for GaN HFET.

Device physics modeling, on the other hand, can help us to reveal the underlying physics for the device to operate. With the development of quantum drift-diffusion modeling, the self-consistent solution to the Schrödinger-Poisson equations and carrier transport equations were fulfilled. Lots of useful information such as band diagram, potential profile, and carrier distribution can be retrieved. The calculated results were validated with experiments, especially on the AlInN layer structures after considering the influence from the parasitic Ga-rich layer on top of the spacer. Two dimensional cross-section simulation shows that the peak of electrical field locates at the gate edge towards the drain, and of different kinds of structures the device with gate field-plate was found to efficiently reduce the possibility of breakdown failure.

Chapter 1 Introduction

1.1 Background

Nitride-based compound semiconductors have already played a dominant role in optical-electronic device applications such as LEDs and LDs, covering the color spectrum ranging from green (530 nm) to UV (360 nm) due to the wide band gap span from 0.9 eV for InN, 3.4 eV for GaN and 6.2 eV for AlN[1]. On the other hand, the unique electrical properties of GaN material suggest it to be an ideal candidate for microwave power device applications too. The wide band gap leads to high breakdown voltage up to 10KV for GaN transistors[2]; strong polarization effects induce large sheet electron density reaching 5×10^{13} cm^{-2} for AlN/GaN heterojunction[45]; high electron saturation and overshot velocity reaches 10^7 cm/s[3], and good thermal conductivity can enable the transistor work in a harsh environment with temperatures over 500ºC[4]. The potential applications can cover various fields including wireless communication, auto-electronics, military radar, and aerospace etc. The basic material parameters for GaN and other semiconductors are listed in Table 1. 1.

	Si	**6H-SiC**	**GaAs**	**GaN**
Bandgap (eV)	1.11	2.9	1.43	3.42
Dielectric Constant	11.8	10	12.8	8.9
RT Electron Mobility (cm^2/Vs)	1300	600	8000	440
Breakdown Field (V/cm)	2.5×10^5	2.5×10^6	4×10^5	5×10^6
Thermal Conductivity (W/cmºC)	1.3	4.9	0.55	2.3
Saturation Velocity (cm/s)	1.0×10^7	2.0×10^7	2.0×10^7	2.5×10^7

Table 1. 1 The comparison in material properties of different semiconductors, taken from ref. 5

Lots of research has been carried out to push the advancing on the GaN transistors. Among all kinds of device structures, the heterojunction field effect transistor is by far the most well-developed and studied. Compared with conventional GaAs and InP HFET whose capability has almost been fully utilized by far, there is still substantial room for improving the device performance on GaN devices. For example, the best number on GaAs HFET was achieved with a power density of 1.4 W/mm at 8.0 GHz in 1980's[6]. The improvement in power density (1.6W/mm) can be reached with sacrificing the operation frequency range (2GHz)[7]. The larger electron saturation velocity of InP enables it operate at a higher frequency band (30GHz), with similar power density (1.45W/mm) compared with GaAs HFET[8]. While for GaN, after the first successful demonstration on HFET device in 1994[9], it has been experiencing a rapid progress. 9.4 W/mm power density has been reported on AlGaN/GaN HFET working at 10 GHz[10] in 2004. In late 2006, Toshiba announced that their GaN HFET prototypes were working at 6.0 GHz (C-band) with the highest recorded output power of 174W; and 81.3 W at 9.5 GHz (X-band), which has a six times higher power density than the conventional GaAs transistors. We can foresee that in near future an industrial supply chain for GaN HFET market embracing material epitaxy, device foundries, and system integration will be emerging.

Besides the great accomplishments that have been achieved, many difficulties and obstacles still exist. First on the growth side, due to the lack of the suitable native GaN substrate, most of the GaN device structures are grown on foreign substrate such as Sapphire, SiC, or Si. Due to the lattice mismatch between GaN and the substrate, large density of defects always reside within the heteroeptixial GaN wafers. How to effectively reduce the defects density of epi-layers is the primary goal that can fundamentally enhance device performances. For example, point defects in

GaN always have deep energy levels and act as electron/hole traps. The trapping and de-trapping action has a large time constant, which means it is a relatively slow compared with the swing of radio frequency (RF) input signal, and therefore could retard the speed of the transistors. Other defects like threading dislocations always behave as the vertical conduction path, which increases the leakage current at the operating bias conditions. The thermal issue of the GaN devices is also related to the defects. The edge and screw type dislocations as non-radiative centers can exaggerate the self-heating, leading to the current collapse problem.

Regarding the fabrication of GaN HFET, the processing procedures have already been standardized, but small and steady breakthroughs have been reported all along, including low resistive Ohmic contacts, low-damage plasma etching, recess gate fabrication, sub-micron T-shape gate, gate with field plate, surface passivation, flip-chip bonding and so on. The research on these processing methods aims at maximizing the output performance out of the device capacity and solving integrations issues such as thermal managements or signal coupling.

The device simulation for GaN HFET, on the other hand, is to predict the behavior by taking the insightful investigations into the device physics, so that it can help the device structure optimization and facilitate the circuit level design. However, the microwave performance, especially the large signal behavior of GaN HFET, can still not be precisely modeled. Influences such as large parasitic elements, self-heating or defects induced dispersion, current collapse and current lag cast a shadow of doubt onto the long-term device reliability, making the equivalent circuit extraction more difficult as well. Currently, the underlying cause that makes the modeling on GaN HFET differ from experiments is the incorporation of defects during high power operation. The establishment of the applicable device simulation methods still depends on the

further understanding to the material, especially on the electrical behavior of the defects and their influence to the carrier transport.

In this endeavor, I will present my study in this thesis on the various aspects of the GaN HFET, ranging from material growth to crystal characterizations; from device fabrication to semiconductor physical modeling.

1.2 Device Growth

The epitaxial growth of GaN material is often performed on SiC, Si, or Sapphire substrate, by molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), or metalorganic chemical vapor deposition (MOCVD) techniques. MBE system deposits the GaN layer at ultra-high vacuum, allowing precise control on beam fluxes and growth conditions. But the grow rate of MBE is slow, and due to the high vapor pressure of the precursor, the quality of GaN epi-layer usually is low. The HVPE system, on the other hand, has a very high GaN growth rate (more than 200 μm per hour). Therefore, it is often used to provide GaN bulk materials, but not capable of depositing nm scale device structures. Currently, MOCVD is the most widely used technique in GaN research because of its high growth rate (2~3 μm per hour), precise control on epi-taxy thickness and composition, high uniformity, and relatively easy maintenance.

In my study, the GaN HFET structures are grown on Sapphire substrate using Emcore D125 MOCVD system. The schematic of this system is illustrated in Figure 1. 1. Prior to the growth chamber, the group III and V precursors arrive via two separate pipelines, connected to the chamber through a specially designed injector to ensure the growth uniformity and correct composition.

Metalorganic (MO) compounds are used for the group III precursors. The metalorganic precursors for Ga, Al and In elements have high vapor pressure at room temperature to ensure

enough mass is transferred into the growth chamber. They also have a good thermal stability in resistance to the decomposition during the storage and transport. More importantly, they can decompose completely on pyrolysis without leaving any solid byproducts to contaminate the growing layer [11,12]. The parasitic gas phase reaction between some combinations of precursors like TMAl and NH_3, and the background impurities associated with precursors such as C and O need to be paid attention to at certain circumstances.

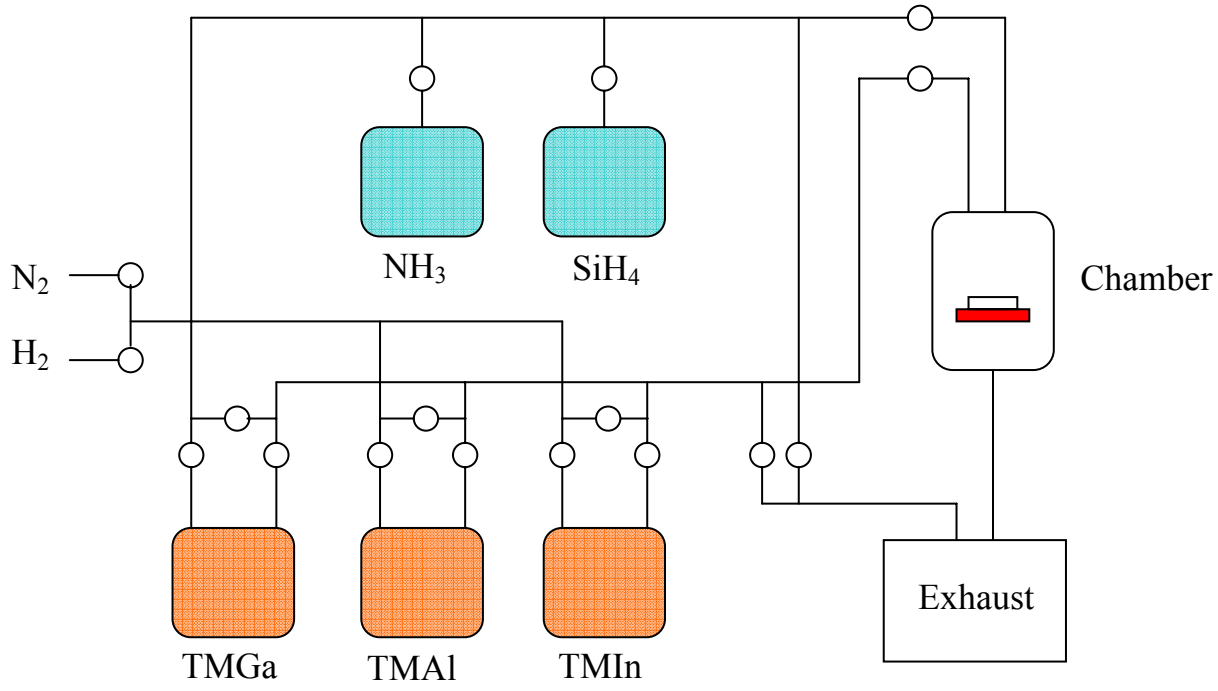


Figure 1. 1 A schematic illustration to the Emcore D125 MOCVD system used by this work.

The flow rate of each source is controlled by the mass flow controller (MFC). The amount of the source supply rate, in mol/min is determined by the mass flow rate, in sccm, of carrier gas into the source bubbler; the vapor pressure of the metalorganic source and the total pressure inside the bubbler. The relationship between these parameters is:

F (mol/min)= F(sccm) · P_{MO}/($P_{Bubbler}$ · 22400)

Equation 1. 1

By control over the carrier flow rate and the bubbler pressure, one can obtain correct composition of III-V alloys.

High purity NH_3 is used as the group III source for nitride growth. The stability of NH_3 requires a high temperature to decompose, but this would cause extra trouble to grow In alloys since the weak bond between In and N at high temperature. A V/III ratio typically larger than 1000 is used for GaN growth, in order to get enough supply on III source and suppress the N loss at high temperature. The basic reaction that describes GaN growth in MOCVD system can be simply written as:

$Ga(CH_3)_3+NH_3 = GaN+3CH_4$

Equation 1. 2

While the detailed reaction routes can be more complicated: after the MO sources and hydrides are injected to the reactor, the sources are mixed inside the reactor and transfer to the deposition area. The high temperature used in MOCVD system results in the decomposition of the group V sources. Other gas-phase pre-reaction will form the adduct mixtures, which if abundant could degrade the epi-layer quality[13]. The precursors are absorbed on the growth surface, and migrate to growth sites. The atoms incorporate into the growing film through surface reaction. Since the GaN growth reaction is thermodynamically driven by the change of free energy, the nucleation and atom diffusion are kinetic processes. Therefore, the growth temperature, related to the activation energy, is the main factor in determining the nucleation density. The byproducts of the reaction are mainly transported to the gas flow away from the deposition area, while partially absorbed by the surface. The main reaction routes for MOCVD grown GaN are illustrated in Figure 1. 2 according to ref. 11.

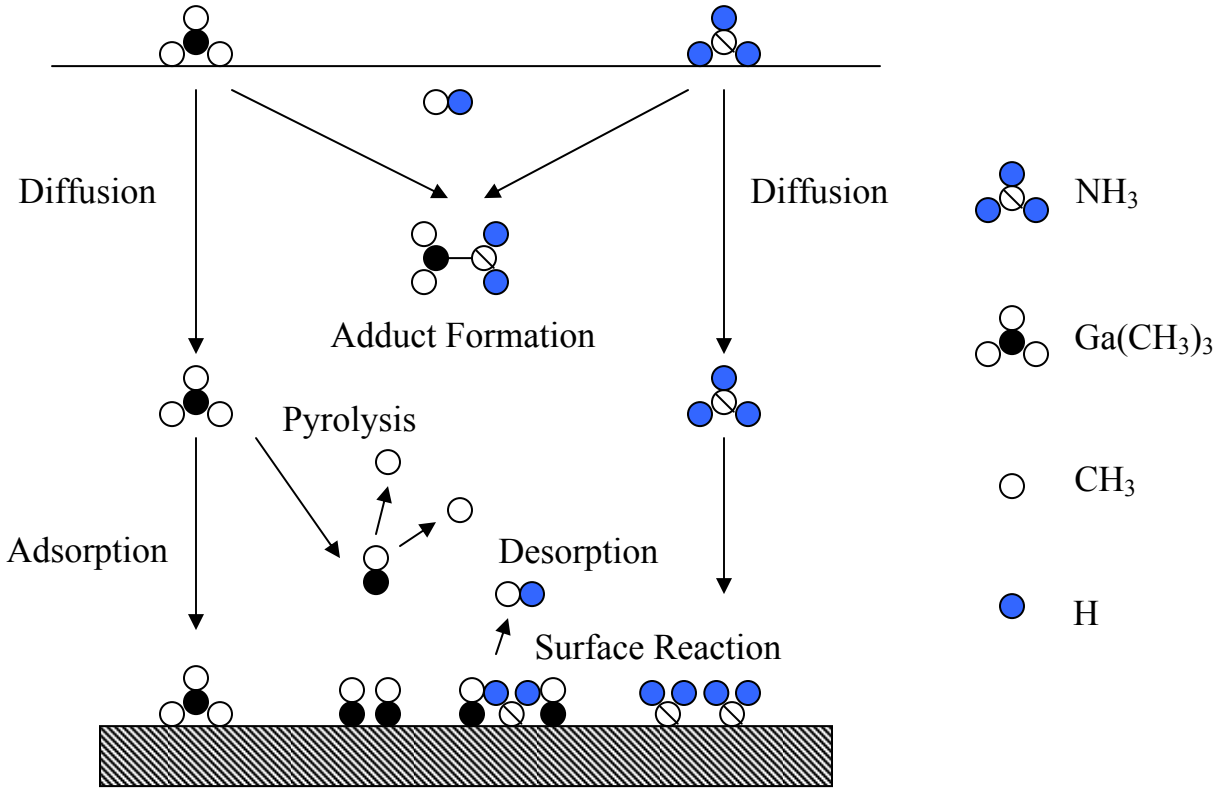


Figure 1. 2 The reaction routes for GaN MOCVD deposition, from ref. 11

The purified H_2 is flowing to the reactor as the carrier gas. N_2 is also used during the AlInN or InGaN growth to improve the In incorporation. Our MOCVD has a single two-inch wafer capacity. The SiC-coated graphite susceptor rotates up to 100 rpm during the growth to improve the uniformity of epi-layer. As well, the growth pressure is adjustable from 15 Torr to 300 Torr. The MOCVD heater consists of one inner and one outer filament for better thermal uniformity across the two inch holder. The filaments are controlled separately through a temperature feedback system. Si is the most effective n-type dopant for nitride materials, and trace amount Silane (SiH_4) is used as the dopant.

One primary issue associated with the growth of high quality GaN is the lack of suitable substrate. Despite the 14% lattice mismatch and 80% thermal expansion coefficient difference

between Sapphire (0001) basal plane and GaN, it is still the most common used substrate. Direct growth on Sapphire results in the nucleation of isolated GaN islands rather than the continuous layer. In order to achieve device-quality single crystalline film, buffer layer is always required prior to the high temperature epitaxial growth of GaN. Nakamura first demonstrated that a low temperature (LT) GaN thin film can serve as good buffer[14], which has been subsequently used by many other groups. At LT, normally in the range of 500~600 ^{o}C, the mobility of surface species decreases, which promotes a uniform dispersion of nuclei over the substrate. The thickness of buffer layer is around 20~50 nm, using low V/III ratio to increase the size of islands in the early stage. Afterwards, the LT buffer layer experiences a short annealing up to over 1,000°C. Then the epitaxial growth proceeds to micron meter thickness. A typical TEM cross-section image for this two-step grown GaN is shown in Figure 1. 3 (a).

Large density of dislocation type defects can be observed from the TEM images. The origin of the defects is the mismatch-induced strain at the GaN and Sapphire interface. The initial epitaxial GaN is distorted with elastic deformation if the layer thickness is less than the critical value. The distortion accumulates as the layer grows thicker, and finally results in the misfit dislocations in order to release the strain, seen in Figure 1. 3 (b)[15]. As the growth evolves, the growth mode transfers from the pseudomorphical two-dimensional mode into the three-dimensional one. The nucleation islands twist or tilt to each other to form a mosaic structure. Therefore, another type of dislocations--threading dislocations--are generated by such mosaic structure to accommodate the disorientation of GaN islands. These dislocations will propagate along the growth direction and rarely disappear. The dislocation density from this growth scheme can reach up to $10^{9} – 10^{10}$ cm^{-2}.

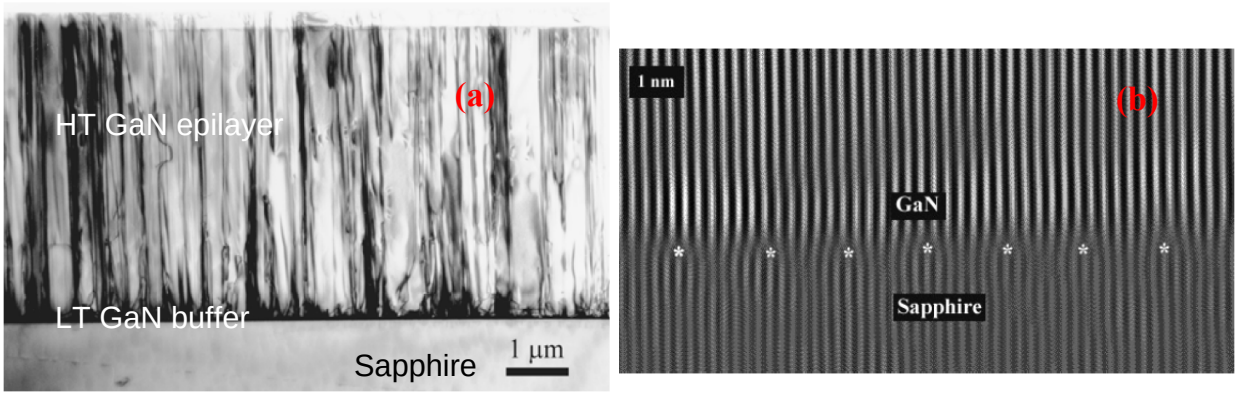


Figure 1. 3 (a) Cross-section TEM image for two-step grown GaN on Sapphire substrate. (b) Misfit dislocations at the GaN/Sapphire interface, from ref. 15.

Dislocations are the predominant type of defects in GaN layers that hamper the improvement of the devices' performance. Accounting for the reduction of dislocations, various efforts have been developed; epitaxial lateral overgrowth (ELO) technique is by far the most effective one. The basic idea of ELO is to pattern the as-grown GaN surface with a mask layer typically using SiO_2 or Si_3N_4 and then re-grow GaN on top of it. Due to the growth selectivity, the re-growth GaN will only continue from the open area (windows). By adjusting the growth parameters, the lateral growth rate out of the windows is enhanced and the surface quickly gets coalesced. Dislocations under the masks are blocked from propagation and the GaN layers over the masks would have ultra-low dislocation defect density. The schematic illustrating the ELO GaN on *c*-Sapphire is shown in Figure 1. 4. The dislocation density for ELO grown GaN is 10^7-10^8 cm^{-2}.

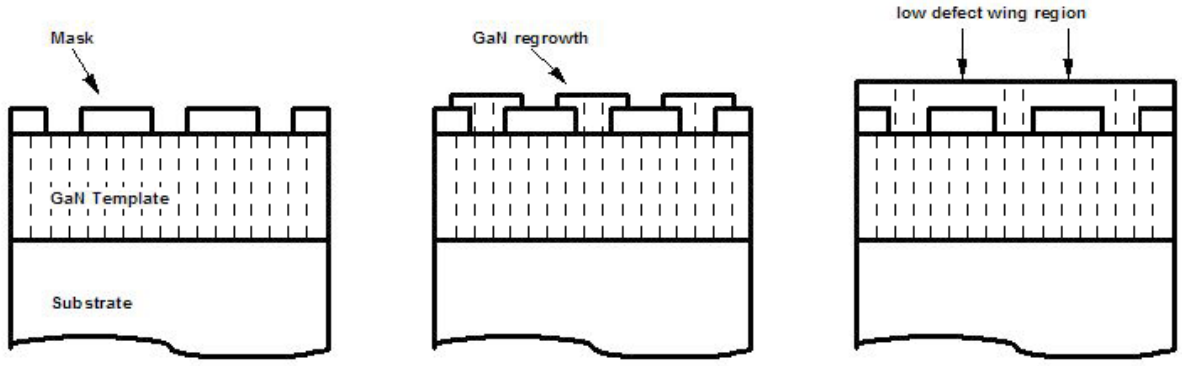


Figure 1. 4 The schematic shows the growth procedure of ELO GaN on *c*-Sapphire.

The ELO technique can effectively reduce the dislocation type defects compared with conventional two-step growth scheme and be more applicable for the LED/LD devices. However, neither method is suitable for HFET. Lateral conduction devices, like transistors, require insulating buffer beneath the channel to ensure the current pinch-off character. Otherwise if the electrons are not well-confined within the channel region, a large amount of microwave power could be dispersed through the parasitic conduction path and it will degrade the noise figure of the power amplifier. Within the LT GaN buffer, the concentration of oxygen shallow donor impurities is found to be as high as 10^{20} cm^{-3} due to the diffusion from the Sapphire substrates[16, 17] and generate a highly conductive layer. In contrast,, GaN directly grown on the SiC substrates without any special techniques is typically semi-insulating. ELO grown method also results the high Si or O incorporation into the GaN around the mask interface. Therefore, the very first task is to develop and optimize an appropriate growth scheme for GaN-on-Sapphire with semi-insulating buffer by MOCVD system.

1.3 Device Structures

The basic device structure of GaN HFET, along with the fabrication process workflow, is shown in Figure 1. 5. The techniques include lithography, dry etch, metal deposition, Ohmic contact formation, and insulator deposition. The fabrication process for GaN devices is quite different with that of Si due to the different physical properties of material. For example, owing to the inherent stability of GaN, no suitable wet etching methods are available for the compatible mesa isolation or gate recess. Also, low resistance Ohmic contact for GaN material can only be obtained after thermal annealing.

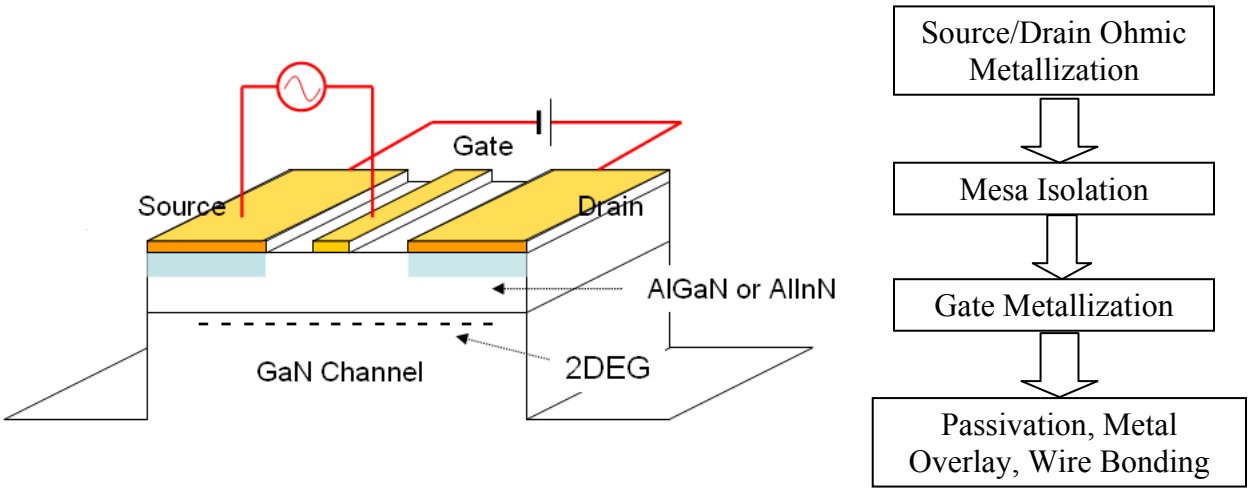


Figure 1. 5 The conventional GaN HFET structure and fabrication process work flow.

The process for HFET fabrication has been standardized in a large extent. However, there still exists a lot of room for improvements. For example, Ohmic contact resistance is critical for the performance of HFET. High contact resistance can not only degrade the transconductance of the device and lead to power consumption on the source/drain access area[18], but also retard the response of the device and lower the cut-off frequency[19]. But the wide band gap of nitride semiconductors makes the formation of Ohmic contact more difficult than that on the GaAs or Si.

Typical Ohmic metallization scheme for GaN material involves the Ti/Al multilayer and the annealing process. We need to optimize the metal thickness and anneal conditions to reduce the specific contact resistance.

The dry etching of GaN materials is another issue associated with the fabrication. Chlorine-based reactive ion etching (RIE) and inductive coupled plasma (ICP) etching are normally used to give a quick, well-controlled and repeatable anisotropic etch[20, 21]. Since the mesa isolation thickness needed is relatively small (~200 nm), the etching condition is controllable in favor of lowing the plasma induced surface damage. Also, new device structures, such as the recess gate transistor, require high etching selectivity between the GaN and the barrier. Different gas etchant combinations should be examined and optimized.

The device structure also determines the empirical equivalent circuit model that describes the microwave behavior. Empirical device modeling method in the context of parameter extraction is used for circuit level application. The circuit model usually describes the device via a two-port network and constructs analytical expressions. It has less the computational complexity compared with other physical modeling methods. The equivalent circuit overlapping on the basic HFET layer structures can be abstracted into the model shown in Figure 1. 6.

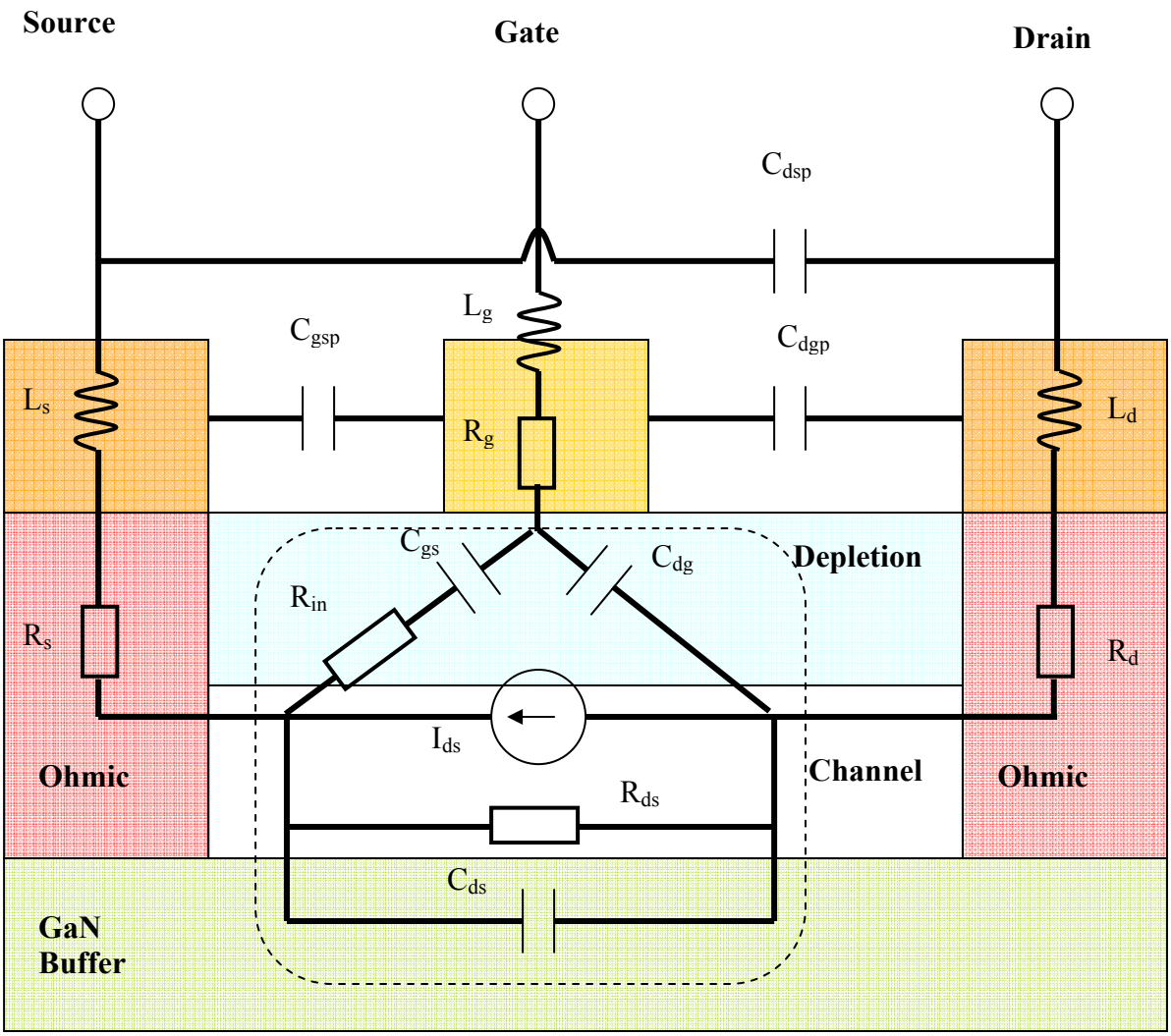


Figure 1. 6 One equivalent circuit model representing GaN HFET structure.

The circuit can usually be divided into two sub-parts: first, a nonlinear and bias-dependent intrinsic part corresponding to the inner device that excludes the contribution from the access regions as well as the stray capacitances, which is outlined with the dashed box; and second, a linear bias-independent extrinsic one corresponding to parasitic access elements. In the extrinsic part, C_{gsp}, C_{dgp} and C_{dsp} represents the parasitic capacitances introduced by the pad connection and probe contacts, and C_{gsi}, C_{dgi} and C_{dsi} account for the interelectrode capacitances.

Similarly, each discrete element in the intrinsic part also has its physical significance. For example, a gate-source capacitor represents the capacitance of the depletion region under the gate; a drain-source resistor represents the output resistance of the channel; the charging resistance R_i represents the retarded electron response to the input gate signal in the gate depletion region; and the delay time τ is the time it takes for the depletion region to respond to the change in the gate signal.

Relatively speaking, the empirical circuit models could be much more flexible, despite their somewhat black-box nature, to provide a better fit in large-signal situations, and interpolate some special effects such as self-heating, trap-assisted current collapse or current lag. For example, table-based modeling has been studied by many groups with great interest[22,23,24]. Instead of using linear circuit components, the equivalent-circuit is described as nonlinear transconductances and transcapacitances. Those components are symbolized as look-up tables obtained from measurement data. Another hotly pursued approach utilizes the neural network to map the nonlinearities of equivalent-circuit[25,26] and train the model through a certain algorithm from the measured data. All these methods, however, are based on the accurate elements extraction from small signal modeling. Therefore, I will focus on the small signal extraction in this work, trying to develop the routines applicable for GaN devices.

In short, fabrication process is a key step to maximize the output from GaN HFET, which needs to be optimized accordingly on different structures. The device structures also determine the equivalent circuit model that can offer the flexibility to describe the microwave behavior. When properly defined and extracted, the equivalent circuit modeling is very practical for circuit design purposes.

1.4 Device Physics

The device physics theory at non-equilibrium condition is often built up on the description of carrier transport mechanism. The drift-diffusion (DD) transport theory is by now the most widely used one for device physics simulation. The DD model is derived from the Bolzmann equations and the basic principles of irreversible thermodynamics. The electron and hole current densities in the semiconductor at certain applied potential are given by[27]:

$$J_n = q\mu_n n \cdot \nabla\varphi + qD_n \nabla n$$

Equation 1. 3

$$J_p = q\mu_p p \cdot \nabla\varphi - qD_p \nabla p$$

Equation 1. 4

where μ is mobility; n and p are carrier density; D is the diffusivity and related with temperature of carrier at thermal equilibrium (may not be equal the lattice temperature) conditions by:

$$D = \frac{k_B \mu}{q} T_{carrier}$$

Equation 1. 5

In the conventional DD model, it seldom incorporates the phenomena of quantum confinement caused by the heterojunctions. Classical carrier statistic is often utilized, which works well for large scale or narrow band semiconductor devices. However, in GaN HFET, large band discontinuities and strong polarization effect will cause substantial confinement to the carriers. Quantum corrections must be applied to DD model to improve the simulation accuracy.

One major difference between GaN and GaAs material is the polarization effect, which is very important to understand the unique behavior of GaN HFET. Polarization is found to be very strong in wurtzite structure crystals like GaN, AlN or InN, including both spontaneous and

piezoelectric components[28, 29]. In fact, polarization is the main reason for the formation of strong two dimensional electron gas (2DEG) at the GaN and AlGaN or AlInN heterojunction interface.

The naturally induced polarization or so called spontaneous polarization exists because the bond between the Ga and N atoms is not purely covalent. There is a displacement of the electron charge cloud towards one atom in the bond. It forms a dipolar pointing from Ga site to N site. Owing to the asymmetry of wurtzite crystal in *c*-axis, a net dipolar vector always exists along this direction. For the GaN layer grown in MOCVD system, it always introduces the Ga-face on the top surface. Therefore the spontaneous polarization within the nitride points from top surface to the bottom, as shown in Figure 1. 7(a). The lattice parameters and spontaneous polarization for GaN, AlN and InN are listed in Table 1. 2.

	GaN	AlN	InN
a_0 (A)	3.189	3.112	3.54
c_0 (A)	5.185	4.982	5.705
P_{sp} (C/cm^2)	0.029	0.081	0.032

Table 1. 2 The comparison in lattice constant and spontaneous polarization between GaN, AlN and InN

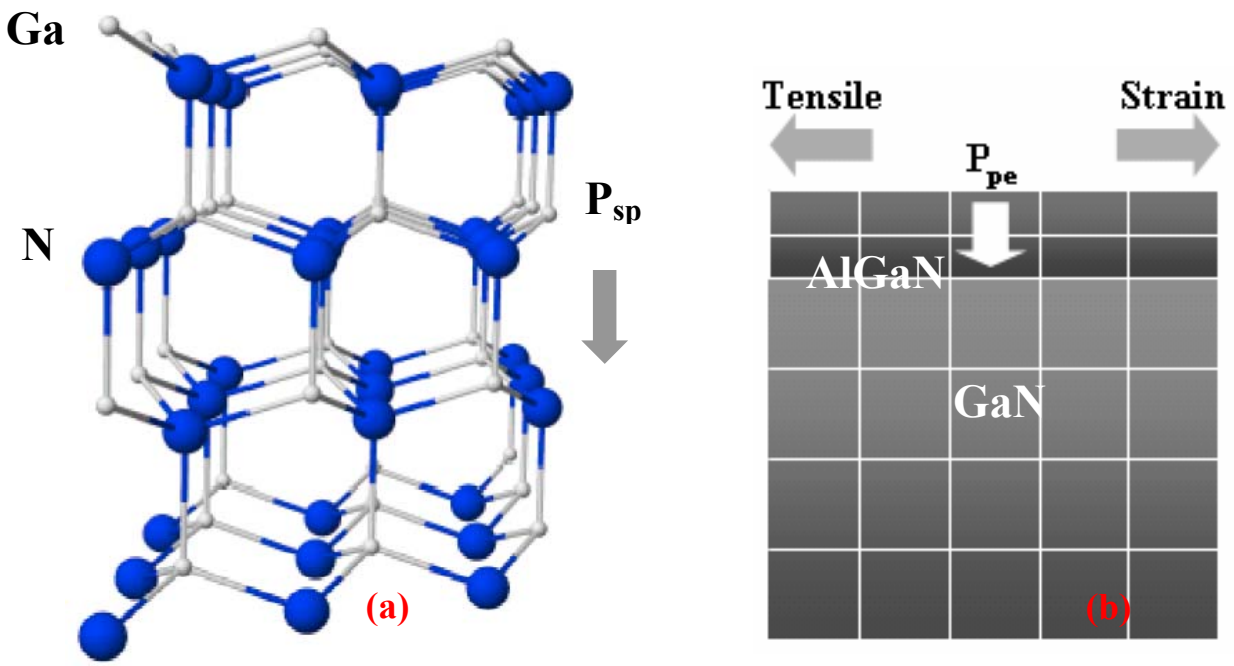


Figure 1. 7 Schematics to illustrate the origin of (a) spontaneous and (b) piezoelectric polarization in nitride semiconductor

Another type of polarization: piezoelectric polarization, is induced by strain between barrier and buffer. The Al-alloy barrier grown on the GaN experiences a strong tensile strain due to its smaller lattice constant. This lattice distortion alters the net dipolar vector at the interface and produces a large piezoelectric polarization correspondingly. As illustrated in Figure 1. 7 (b), the piezoelectric polarization in the strained AlGaN barrier also points from top surface toward the interface. The magnitude of piezoelectric polarization can be calculated by:

$$P_{pe} = 2\frac{a - a_0}{a_0}(e_{31} - \frac{C_{13}}{C_{33}}e_{33})$$

Equation 1. 6

where a and a_0 are the lattice constant of the GaN and the barrier, and the other parameters are listed below for different materials.

	GaN	AlN	InN
e_{31} (C/m^2)	-0.49	-0.6	-0.57
e_{33} (C/m^2)	0.73	1.46	0.97
C_{31} (GPa)	379	395	182
C_{13} (GPa)	70	120	121

Table 1. 3 The piezoelectric coefficients for GaN, AlN and InN

Therefore, both spontaneous and piezoelectric polarizations work together to attract electrons gathering at the heterointerface to form a high density electron sheet as illustrated in Figure 1. 8 (a). The density can go up to 10^{13} cm^{-2}, much higher than the traditional GaAs device structures at which the 2DEG is mainly confined due to the conduction band discontinuity. The existence of the strong polarization will cast a profound change on the band distribution in GaN HFET, as shown in Figure 1. 8 (b). The detailed calculation on the band diagram and carrier profile, by solving the Schrödinger and Poisson equations self-consistently, will be discussed in Chapter 4.

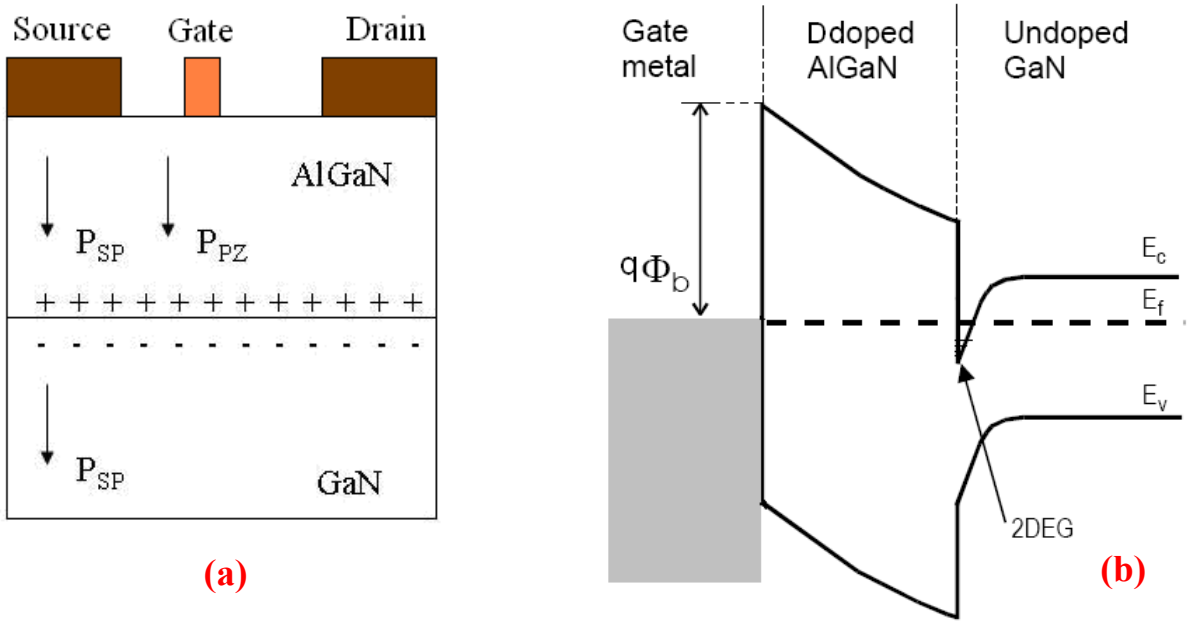


Figure 1. 8 Schematics to illustrate (a) the formation of 2DEG due to spontaneous and piezoelectric polarization; (b) the band diagram within a AlGaN/GaN HFET structure with gate metal.

By studying the theoretical device physics, the underline mechanisms that determine the device behavior can be revealed. The simulation can also provide us the preliminary guides in optimizing the device performances at certain configuration. The simulation should be based on drift-diffusion model with the correction from quantum physics, plus the special consideration on polarization effects in nitride semiconductor.

1.5 Dissertation synopsis

This dissertation will present the experiments and calculations done on the GaN HFET with AlGaN and AlInN barriers, covering the MOCVD growth, material characterization, device fabrication, empirical and physics based device modeling. The organization of this thesis is:

Chapter 1 - Introduction

An overview on GaN and related alloy material growth by MOCVD; device structure and circuit model; and device physics is introduced.

Chapter 2 – MOCVD growth

The detailed MOCVD growth scheme on semi-insulating AlN buffer, GaN template, AlGaN and AlInN barrier layers are described, followed by the layer characterizations obtained from X-ray diffraction (XRD), atomic force microscopy (AFM), and in-situ reflection measurements.

Chapter 3 –HFET Fabrication and Characterization

This chapter gives the device fabrication details, especially the optimizations performed on Ohmic contact and plasma dry etch. The measurements on device transport properties, DC characterizations, and microwave and capacitance/voltage results are presented. Experiments on two new device structures: recess gate HFET and metal-insulator-semiconductor (MIS) HFET are introduced.

Chapter 4 –Small Signal Modeling

The equivalent circuit modeling is studied to analyze the microwave performance of the HFET. A new 18-element equivalent circuit model is proposed. Different extraction methods covering cold- and hot-FET modeling schemes are reviewed. A hybrid extraction method is developed combining the virtue from the both methods. It provides high fitting accuracy to simulate the measured data.

Chapter 5 –Physics Modeling

Quantum DD modeling theory is implemented for GaN HFET, simulating carrier distributions, energy band diagram, potential profiles, and I-V characteristics, in one- and two-dimensionally. The solver provides self-consistent numerical solution to the Schrödinger, Poisson and current equations, using Newton iteration method. The simulation results are validated with experimental results, especially on the data measured from AlInN barrier structures.

Chapter 6 –Summary and Future Works

This chapter will summarize the key contributions of this dissertation and foresee the future work on the GaN transistor devices.

Chapter 2 MOCVD Growth

A typical layer structure for our GaN HFET device is shown in Figure 2. 1. It is grown on *c*-Sapphire substrate, with about 300 nm AlN first deposited as the semi-insulating buffer. About 3 μm un-doped GaN, its top acting as the 2DEG channel, is then grown on the buffer. Before the barrier growth, a thin AlN layer is deposited as the spacer to improve the mobility. The barrier we tested includes AlGaN and AlInN. Usually the barrier is divided into un-doped and Si-doped sub-layers. The doping concentration varies from 10^{17} to 10^{18} cm^{-3}, and the total thickness is in 20 ~ 40 nm. On the top of the barrier, an un-doped thin GaN about 2nm is placed to reduce surface leakage and improve the Ohmic contact. In this chapter, the growth detail for each layer will be presented.

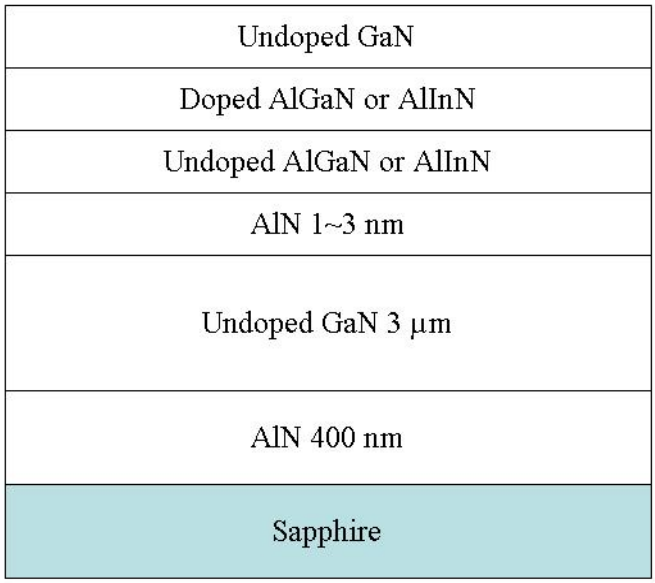


Figure 2. 1 The layer structures used in this work

2.1 GaN growth

2.1.1 Semi-insulating AlN buffer

Since the GaN layer is the electron channel for HFET devices, high crystal quality with less defects is important to suppress dispersion effects[30]. On the other hand, transistor devices also require none lateral conduction through the bulk, because the layers under the channel serve as the back barrier against which the gate can deplete the channel and perform the modulation. A conductive buffer will cause the capacitive coupling and result a large parasitic parameter that degrades the RF performance.

To achieve the semi-insulating buffer, different growth techniques have been reported. One method is the compensation. The residual donors in GaN have to be compensated by acceptor states from carbon impurities, or transition metals such as Cr or Fe[31, 32, 33]. However, it will leave high concentration of point defects or extended defects that are undesirable. An alternative approach is to use the AlN buffer. Because of the large band gap of AlN, it behaves as insulator in nature. Another advantage is its higher thermal conductivity. Furthermore, the AlN buffer introduces the compressive strain to the top GaN that could restrain the generation of cracks and reduce the dislocation density.

There are several challenges for high quality AlN buffer grown by MOCVD. First, due to the high binding energy between Al and N, the surface mobility of Al source atom is very small. The AlN growth is preferable in 3D mode, forming the islands of varying orientations with respect to the substrate. Most of the epitaxial AlN thin films on Sapphire were reported with large threading dislocation density and domain boundaries. Its typical dislocation density is about 10^{10}-10^{11} cm^{-2}. In order to enhance the surface migration of Al source, high growth

temperature is preferable[34]. Second, in the MOCVD system, the gas phase pre-reaction between ammonia and TMAl is considerably strong, which is the main cause for the low growth rate of AlN. Normally, lower chamber pressure is desired to suppress this parasitic reaction. If the "flow-modulation" growth method is applied, namely the III and V group sources are supplied alternatively into the reaction chamber, the step flow growth mode of AlN can be achieved easily[35].

In order to reduce the gas-phase pre-reaction between TMAl and ammonia, low chamber pressure (30 torr) and III group flow rate (7 sccm) are used along with high growth temperature at about 1030°C. Since the mobility of Al atoms on the surface is low, high temperature is recommended during growth. Also, the high nucleation temperature will improve the crystal quality of islands, and reduce the formation of screw-type dislocation. Figure 2. 2 shows the AlN buffer surface morphology evolution on Sapphire substrates. At the beginning stage, the grain-like islands are formed on the surface. With further growth, the islands evolve from a three-dimensional growth mode at first to finally form a continuous film covered with pin holes. The porous structures on AlN buffer could enhance the micro ELO growth effect for GaN epi-layer that followed [36].

The AlN buffer was examined by rocking curve XRD with a narrow full-width at half maximum (FWHM) about 80 arcsec on (002) direction, but 600 arcsec on (102) direction. This indicates that the AlN buffer layer has a very low density of screw-type threading dislocations, but high for the edge-type.

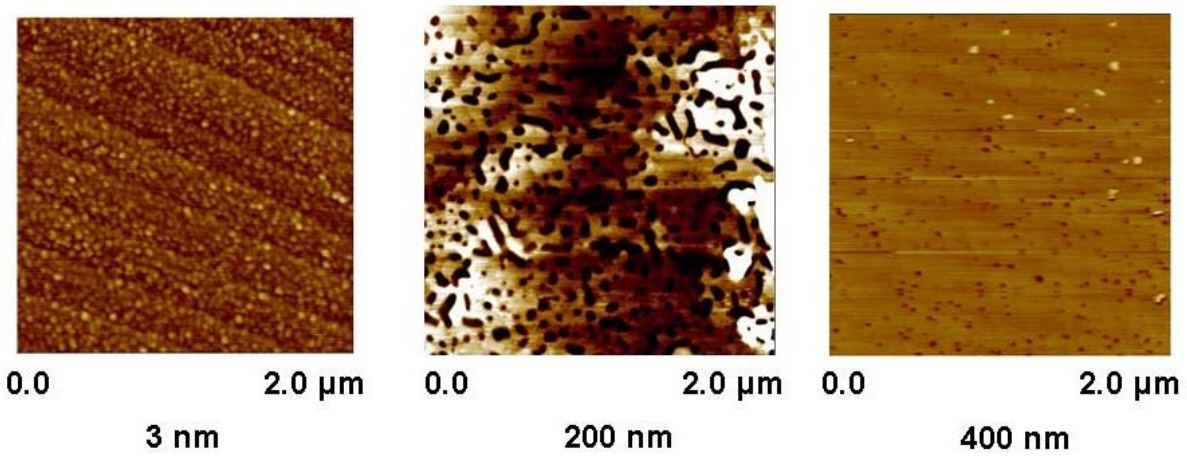


Figure 2. 2 Surface morphology evolution for AlN buffer layer on sapphire

2.1.2 GaN growth optimization

The conventional growth scheme for GaN on Sapphire consists of two steps: low-temperature (LT) buffer layer growth and high-temperature (HT) epi-layer growth. The purpose of the low temperature buffer layer, which contains various phase and disorder structures, is to optimize the transition between the Sapphire substrate and the GaN device layers. The high interfacial energy between GaN layer and Sapphire leads to 3D island growth. The annealing process is inevitable, which performs the thermal ramping under H_2 ambient to etch the as-deposited nucleation layer into isolated islands with (0 0 0 1) facet. Those nucleation sites enhance the lateral growth and suppress threading dislocations during the high temperature 2D growth mode that after.

The direct growth of GaN on AlN buffer similarly includes the mid-temperature nucleation stage and high-temperature epi-growth stage. The quality of GaN template is believed to be highly dependent on the nucleation growth conditions[37, 38]. In order to achieve the high

quality GaN template, the nucleation stage should be carefully controlled in terms of:

a. Temperature – About 900ºC-950ºC growth temperature is normally reported from different groups. Since the wetting of GaN on an AlN surface is much better than on a Sapphire, the nucleation temperature can be much higher than the LT GaN case.
b. Chamber pressure – High pressure over 100 torr is preferred, Associated with larger gallium diffusion rate, high pressure may facilitate the lateral expansion of large nuclei with lower density, and improve the epi-layer with fewer extended defects. Appropriate chamber pressure is picked subjected to the trade-off between less nuclei density and the less conductive GaN layer which need lower pressure instead.
c. V/III ratio – Moderate V/III ratio is needed, since the larger ratio in the initial growth stage causes a higher yellow luminescence in photoluminescence (PL) measurement; a increasing in FWHM in XRD measurement; and the decreasing in electron mobility. But too small ratio also will result in a large incorporation of shallow donor impurities that is undesired.

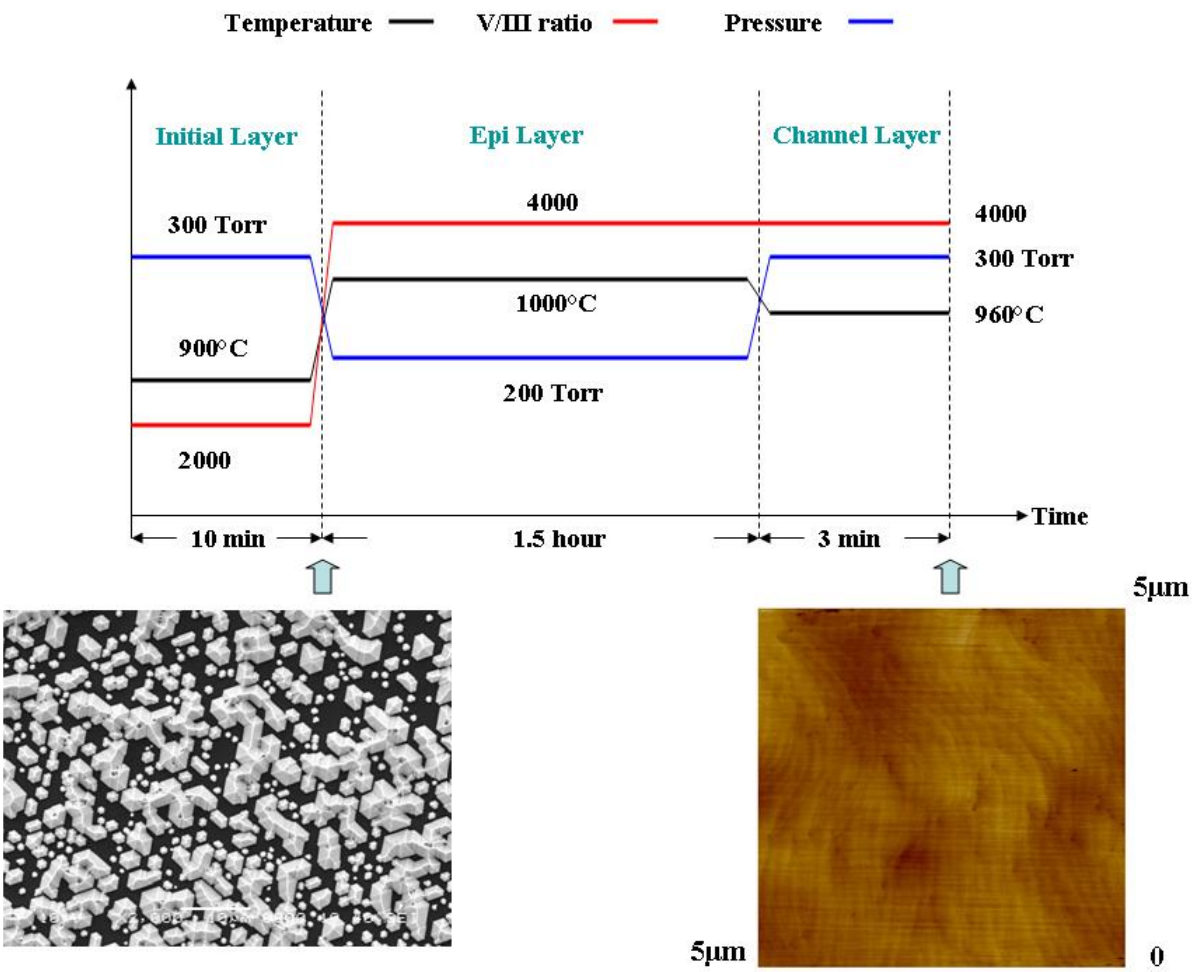


Figure 2. 3 Growth scheme for GaN layer in HFET structure.

As shown in Figure 2. 3, the initial layer and epi-layer have the thicknesses around 300 nm, 1.5 µm respectively. The initial seeding layer growth is critical in determining the GaN crystal quality. It is often grown at moderate temperature with high chamber pressure and slight low V/III ratio, under which conditions the nucleation density is reduced and lateral growth can be enhanced for the following epi-layer growth. We tested different growth conditions as shown in Table 2. 1. In terms of XRD, there is an obvious trend in reducing the FWHM, which relates to the reduction of edge type dislocations, with higher growth pressure and lower V/III ratio. The

best condition is determined as 300 Torr and 2000 V/III ratio, noting that a too-low ratio will result in a higher concentration of residual donors thus causing the buffer leakage. The SEM picture in Figure 2. 3 shows the surface morphology of seeding layer after the 10-minute.growth on the AlN buffer, from which we could tell the nucleation is randomly distributed in an obvious hexagonal shape and the growth mode is three-dimensional.

AlN buffer	GaN seeding layer		GaN epi-layer quality	
	Pressure	V/III ratio	XRD (002) arcmin	XRD (102) arcmin
400nm @30 Torr 1030 °C	76 torr	2000	4.3	16.7
	200 torr	2000	6.0	9.5
	200 torr	3000	5.3	7.4
	200 torr	4000	5.6	8.0
	300 torr	**2000**	**5.0**	**5.9**
	300 torr	1000	4.7	5.1

Table 2. 1. XRD characterized GaN template quality on different seeding layer growth conditions

The epi-growth stage is carried out normally at high temperature with large V/III ratio and high growth rate (~ 2μm/hour) that is similar to conventional ELO GaN. Different growth pressure has been tested at 30, 76 and 200 Torr. With lower chamber pressure, it is reported to increase the carbon impurity incorporation that has deep energy levels and makes GaN layer more resistive[39]. Our experiments on leakage current measurement comparing different growth pressures confirmed this trend, while the 200-Torr-grown sample still gives acceptable leakage current level.

A high quality GaN channel layer on the top of epi-layer serving as the 2DEG channel can effectively increase the carrier mobility[40]. Therefore, a 300 nm channel layer is grown on

the top at 300 torr pressure and 960°C. Higher chamber pressure helps to suppress the background impurity related to deep level defects. With the insertion of this channel layer, the 2DEG mobility for AlGaN/GaN heterojunction increases from 1200 cm^2/Vs upto 1500 cm^2/Vs, given the same barrier conditions.

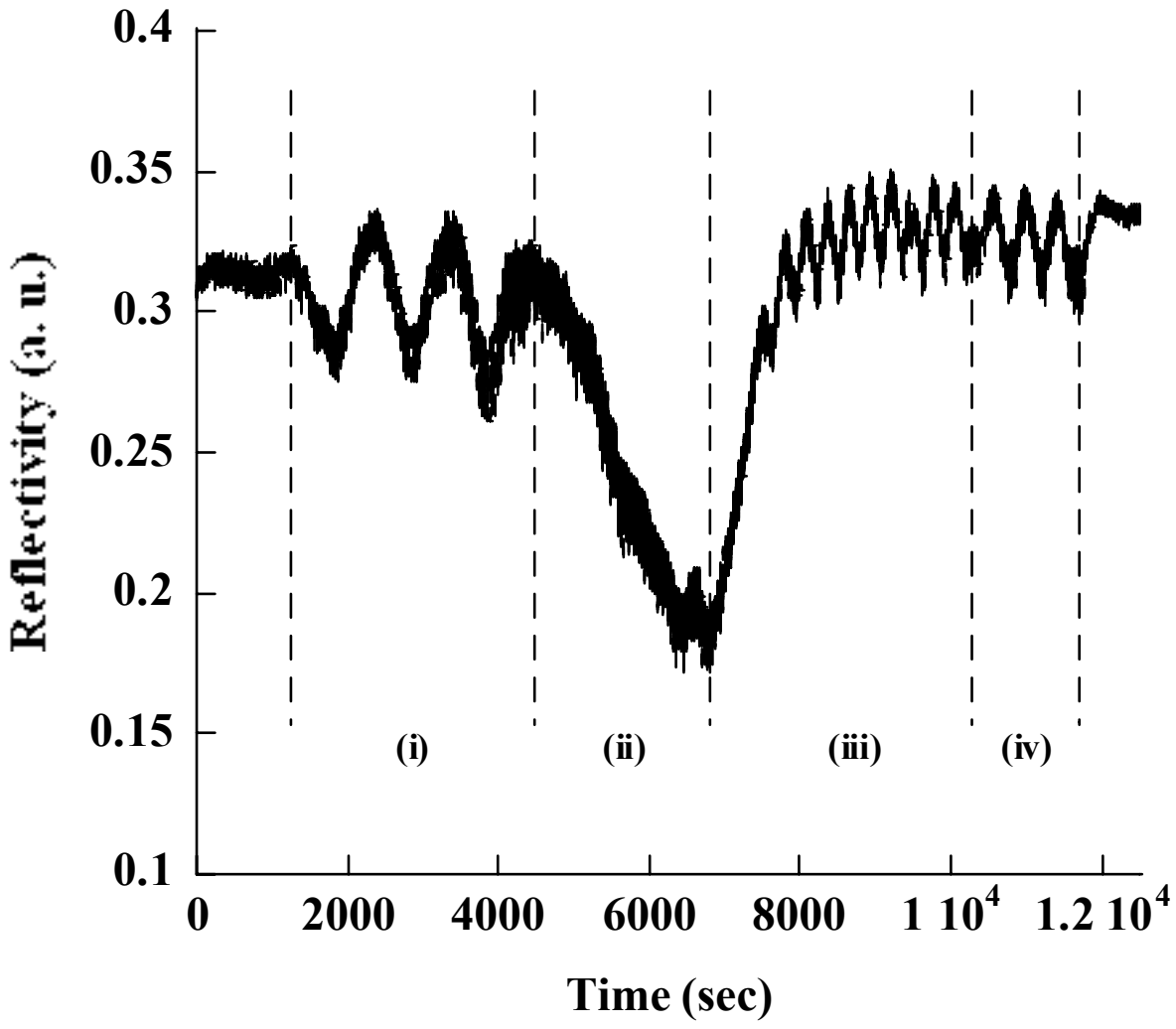


Figure 2. 4 The in-situ laser reflectivity measured during the HFET growth.

In-situ laser reflectance monitoring equipment has been utilized during our MOCVD GaN growth to record the surface morphological evolution. From the change of the reflectivity, we can obtain the qualitative measurement on surface roughness, and furthermore extract the information such as growth rate and alloy composition. A typical reflectivity data traced during the HFET growth is shown in Figure 2. 4. Each growth stage can be clearly distinguished. An immediate oscillation is seen at stage (i) representing the growth of AlN buffer, which has a small surface roughness. It followed by the GaN initial growth stage (ii) on top of AlN buffer, and the surface is roughened due to the nucleation. As the growth proceeded, the islands coalesce and result in the recovery of reflectance. Two-dimensional growth mode is achieved during the epi-layer growth stage (iii) and clear reflectance oscillation is observed. From the period of the oscillation, the growth rate is estimated close to 1.8 μm per hour. When the channel layer growth begins (iv), a transition in reflectance is observed and the growth rate at 300 torr reduces to 1.1 um per hour due to the increase of parasitic pre-reaction.

2.2 Barrier growth

2.2.1 Spacer growth

Prior to the barrier growth, a thin layer of spacer is deposited on the top of channel that usually employs an un-doped material with larger band gap, which tends to isolate the source of electrons away from the channel. For GaN devices, the insertion of an ultra-thin AlN spacer layer has been reported to increase the mobility of 2DEG[41.] The improvement in mobility is ascribed to the better confinement of 2DEG and thus the associated suppression of alloy scattering[42,43] and possibly scattering by defects/ionized donors in the barrier.

We found the spacer layer thickness is an influential parameter to change the electron transport characteristics of GaN heterojunction. It has been reported that the thicker AlN spacer can introduce higher density of 2DEG at the AlGaN/GaN structure due to the strong polarization of AlN material[43]. However, a contradictory result was reported in AlInN/GaN case[44], even though the barrier doping is kept at the same level. AlN thickness also affects the mobility of 2DEG dramatically. A high mobility window exists for 2DEG at ultra-thin AlN/GaN heterojunction[45], and the lower mobility with thick spacer is probably due to long range scattering originating from large-density defects in AlN. Our experiments indicate ~1 nm is the optimum AlN spacer thickness to achieve the best transport properties. Therefore, the growth rate of AlN spacer is critical in order to attain this very thin layer.

The growth conditions for AlN are 1020ºC, 30 torr chamber pressure, and V/III ratio around 800. The growth rate for the AlN at such conditions can be calibrated from the AlN/GaN superlattices (SLs) growth. As shown in Figure 2. 5, a 10-pair AlN/GaN SLs structure was measured by 2θ-ω XRD scan. In observing the sharp satellite peaks from the XRD of SLs, we can conclude the abrupt interface between GaN and AlN is achieved Here the clear satellite peak positions match with the simulation, which corresponds to the 2 nm/ 1.3 nm (AlN/GaN) pair thicknesses and growth rate is determined as 3 nm per minute. The AlN growth conditions were applied onto the HFET structures.

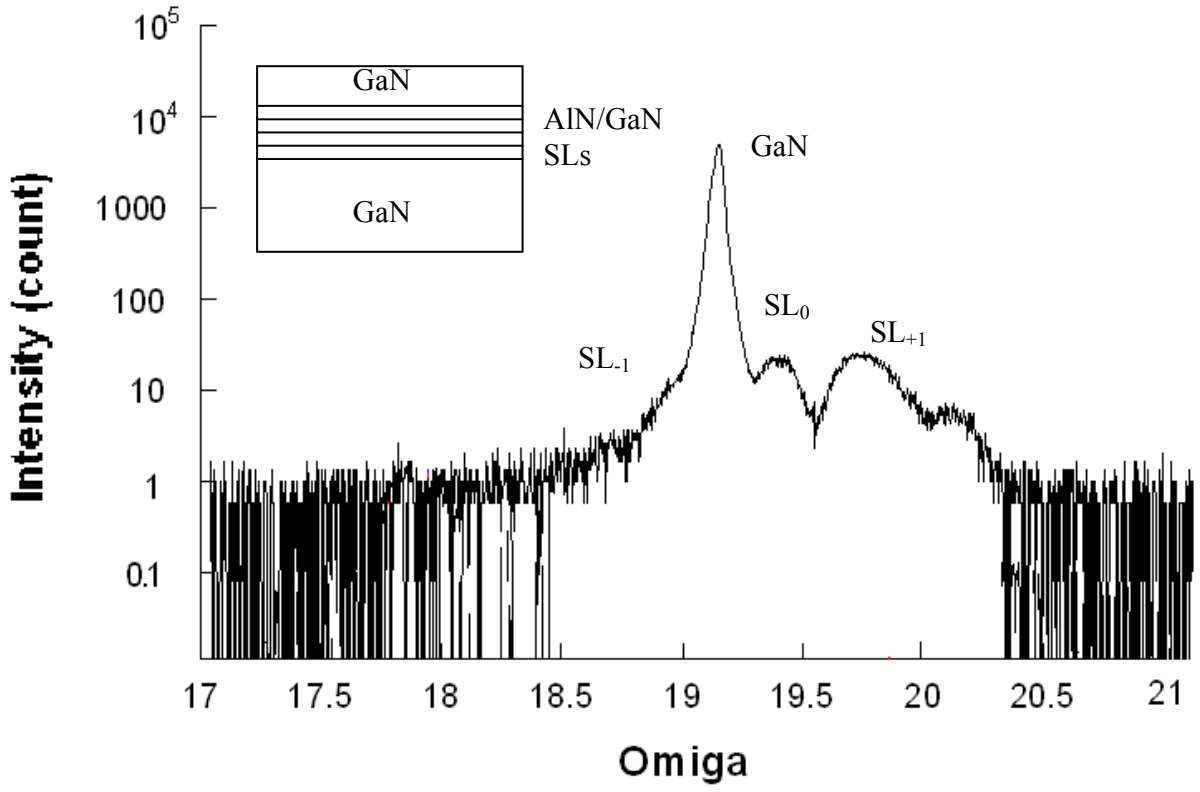


Figure 2. 5 XRD 2θ-ω scan of 10 pairs AlN/GaN SLs to determine AlN growth rate

2.2.2 AlGaN growth

The quality of AlGaN barrier layer also depends upon the beneath GaN layer. For example, the penetrating threading dislocation from the buffer layer can cause Al segregation around the dislocations up to 70% Al composition[46], and indubitably form the current leakage path. So the crystalline quality of AlGaN can be significantly improved if it is grown on high-quality GaN. Also, due to the lattice mismatch and different thermal expansion coefficients between GaN and AlGaN, more dislocations will be generated especially at large Al fractions situation even though it helps to induce more carriers in the GaN. It is also difficult to attain

good Ohmic contact on AlGaN due to the larger band gap. Therefore, the optimum Al composition is around 20~40 percent according to the literatures.

The thickness of the AlGaN barrier is another issue of concern. A thinner barrier can improve the transconductance of the device, but it can also increase the gate capacitance (C_{gs}) and make gate current easier to tunnel into the channel. Furthermore, both simulations and experiments have shown that the thin barrier can not induce sufficient high sheet carrier density and limit the saturation current that the device can achieve. On the other hand, a too-thick AlGaN will introduce serious cracking problem when its thickness exceeds a critical value[47], which originates from the tensile stress between AlGaN and GaN.

The growth conditions for high quality AlGaN by MOCVD is similar to that of AlN, with high growth temperature and low chamber pressure[48]. The accompanied gas-phase pre-reaction between Al-source and N-source needs to be suppressed by reducing ammonia flow and chamber pressure. Otherwise it can significantly deteriorate the group-III deposition efficiency and bring rough interface that reduces the mobility of the 2DEG. The barrier is grown under 30 Torr pressure with temperature around 1,000 ºC.

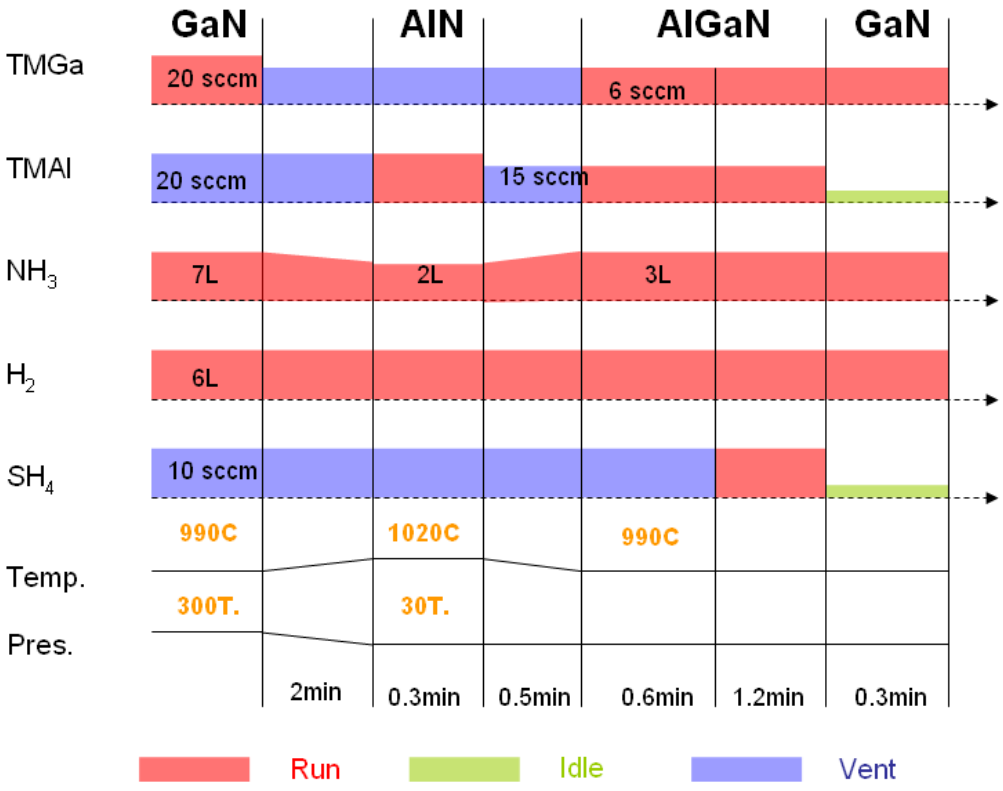


Figure 2. 6 Growth scheme for 30 nm $Al_{0.3}Ga_{0.7}N$ barrier.

The detailed growth scheme is illustrated in Figure 2. 6. In this figure, if the gas line is in "vent" status, the source flowing is bypassed into the exhaust right before get into the chamber. And the "idle" status means the gas flowing is blocked. In this configuration, the flow rate of TMAl and TMGa source ensure the appropriate Al concentration. The surface morphology measured by AFM is shown in Figure 2. 7. The dislocation density for the AlGaN barrier under these conditions is estimated to be around 10^9 cm^{-2}. The XRD ω-2θ scan shows clear peaks for the GaN template, AlGaN barrier and AlN buffer. The thickness of the AlGaN is about 30 nm calculated from the thickness fringes; the Al concentration is 27% from the AlGaN peak position. The top 20 nm barrier is normally doped with Si into middle 10^{17} cm^{-3} range.

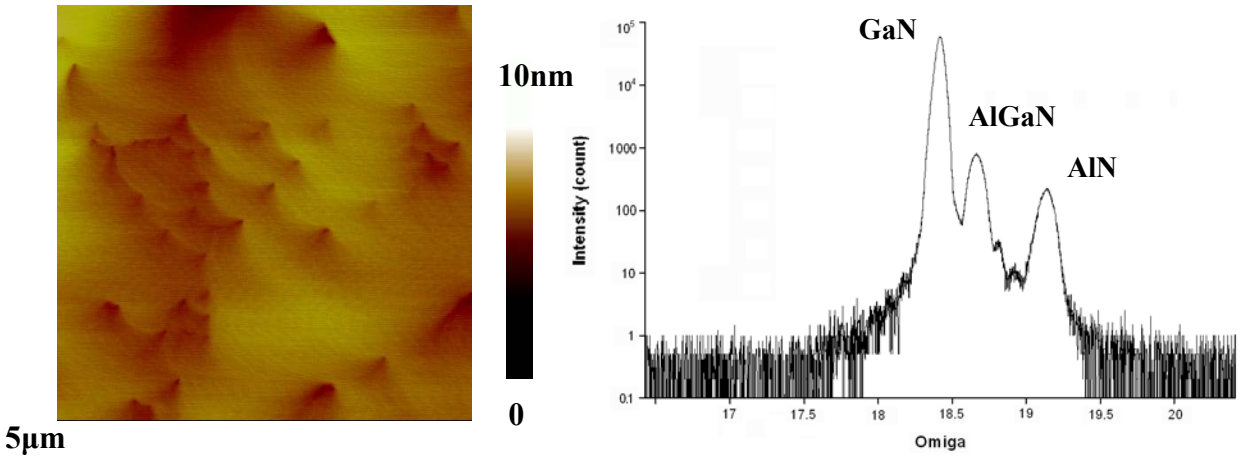


Figure 2. 7. The surface morphology and XRD ω-2θ for $Al_{0.27}Ga_{0.73}N$ barrier device.

2.2.3 AlInN growth

Indium-related ternary has been widely used for III-V HFETs, for example the GaAs p-HEMT. The advantage is to bring larger band gap discontinuity between the In-ternary channel and Al-ternary barrier producing higher carrier density. Also, InGaAs has a higher electron mobility and saturation velocity than the GaAs channel.

The same situation seems to be also applicable for nitride HFET. The incorporation of Indium is found to have a profound influence on electrical properties in the nitride semiconductor devices, especially for the LEDs. Due to the large ionic radii of Indium as compared to that of Al / Ga, the isoelectronic Indium atoms can occupy the vacancy sites along the dislocation core sites in the growing films[49]. The enhancement of optical and electrical properties is generally attributed to the reduction of non-zero *c*-component dislocations[50]. A thin InGaN layer is also reported to be placed beneath the GaN channel to form the back-barrier for HFET, in order to provide better confinement to 2DEG and suppress the buffer leakage[51].

Indium ternary can also be used in replacing the conventional AlGaN barrier, namely the AlInN barrier with large In composition. Considering the benefit from $Al_{0.82}In_{0.18}N$ matches the lattice of GaN, the barrier layer has much reduced strain compared with AlGaN and thus can reduce the possibility of dislocations generation. As well, lattice matching leaves no piezoelectric polarization but only spontaneous component. The device reliability is expected to be enhanced since less strain is present or even nonexistent. Even for AlGaN barrier, the addition of Indium with trace amount is reported to be beneficial. The threading dislocation density is lowered as Indium composition increases with a corresponding increase in lateral coherence length[52].

However, high quality Indium ternary alloys are relatively more difficult to grow in MOCVD than GaN or AlGaN materials. The high equilibrium pressure of N on InN requires the relatively low growth temperatures. The substrate temperature used ranges from 650 to 900°C as reported[53]. Indium ternary is also subjected to thermal instability. Phase separation is a serious problem for InGaN and AlInN growth, which may be caused by the large disparities between In and other group III materials, like the differences in atomic radii, equilibrium nitrogen pressure, surface diffusion barrier and so on.

The growth of Indium ternary alloys with correct concentration requires precise control over the temperature, since the high dependency between these two. Indium concentration goes down quickly with the increase of temperature. Also, carrier gas is another factor to be considered. N_2 combining with H_2 has been reported[54] to improve the Indium incorporation efficiency.

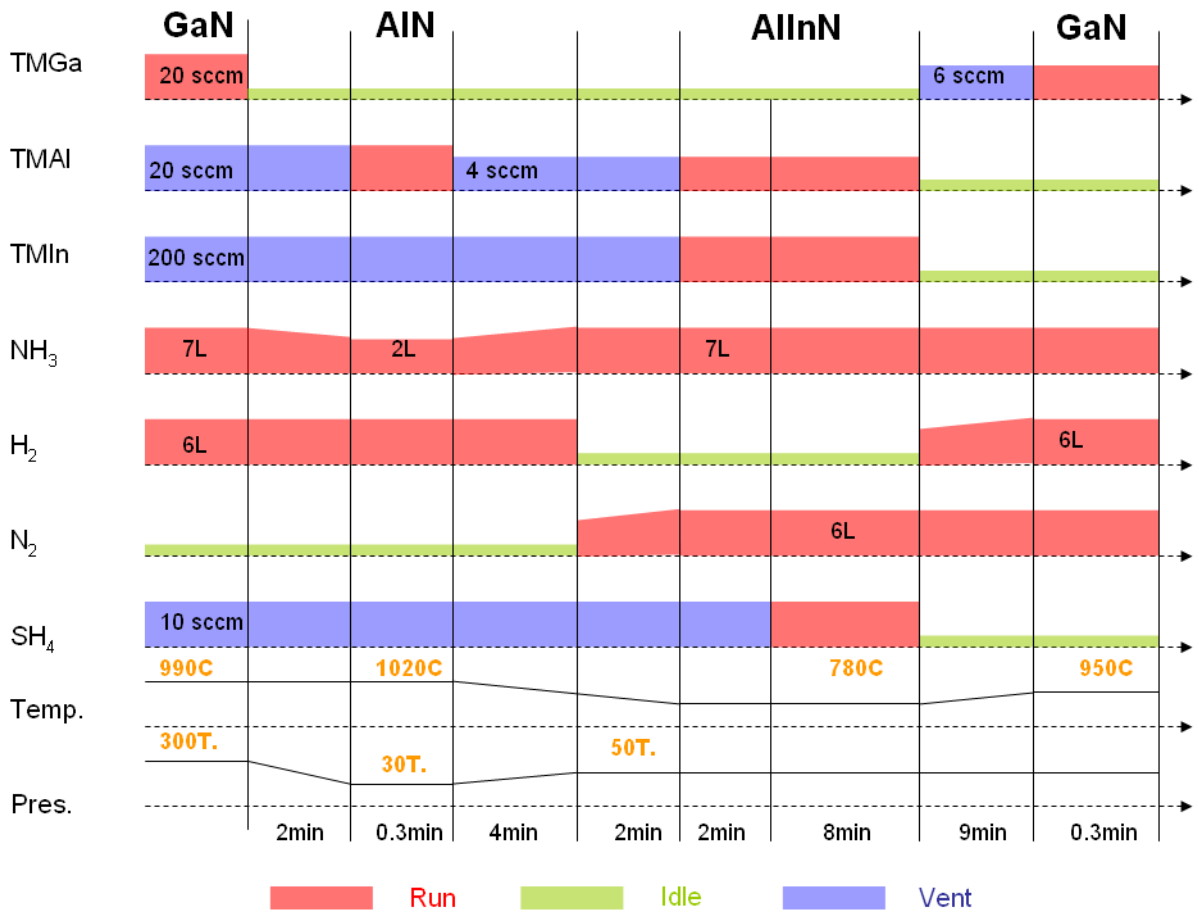


Figure 2. 8 Growth scheme for 20 nm $Al_{0.72}In_{0.18}N$ barrier.

Lattice-matched $Al_{0.82}In_{0.18}N$ barrier HFET structure was successfully grown with high carrier mobility being achieved. The growth scheme is shown in Figure 2. 8. After the spacer, H_2 is switched to N_2 as the carrier gas. Meanwhile the growth temperature ramp down from 1,000ºC to 780ºC, which takes about 6 minutes. The composition of Indium is mainly controlled by the changing the growth temperature, and found to be very sensitive to the temperature. For nearly lattice-matched AlInN barrier, the typical growth conditions are 50 torr, 780ºC, and 4,000 V/III ratio. Under these conditions, the growth rate of AlInN is around 120 nm/hour. As shown in Figure 2. 9, the surface of AlInN is very smooth, with RMS in 0.3~0.6 nm, but large amount of

defects still can be seen. From the XRD measurements, the composition and the thickness of AlInN can be estimated. In order to reduce the Indium composition variation across the wafer, fine tuning on the heaters (inner and outer one) power and high sample rotation speed are necessary.

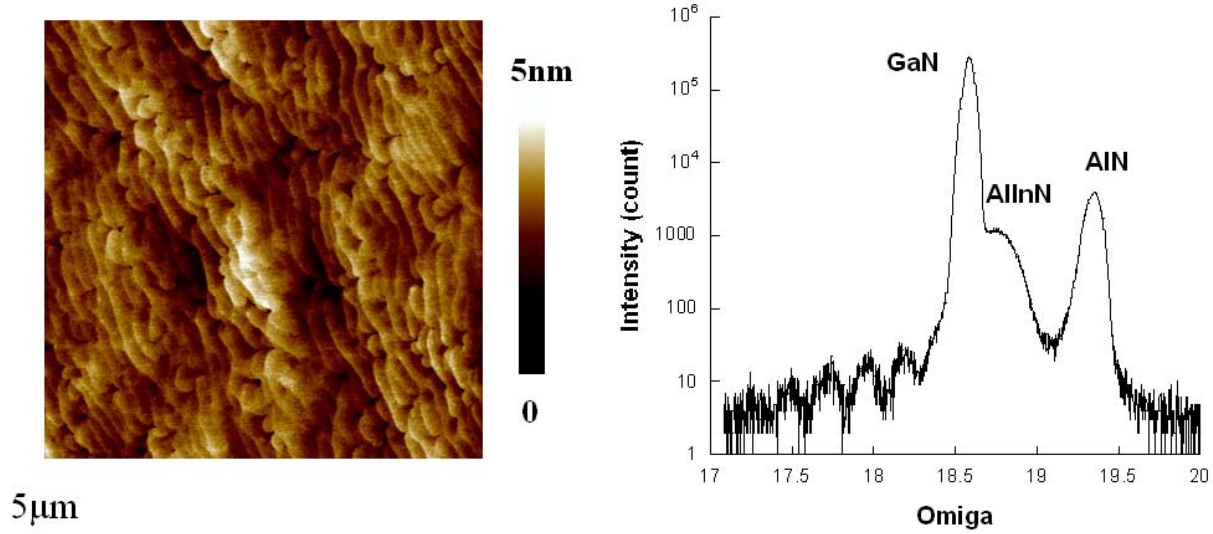


Figure 2. 9 The surface morphology and XRD ω-2θ for $Al_{0.82}In_{0.18}N$ barrier device

Chapter 3 HFET Fabrication and Characterization

3.1 Device Fabrication

3.1.1 Basic procedures

The fabrication procedures for GaN HFET normally involve three major steps, namely the source-drain Ohmic metal formation, device isolation, and gate pattern metal deposition. Within each step, either photolithography or electron-beam (e-beam) lithography method can be used to define the patterns.

Prior to the fabrication, the sample needs to be degreased by organic cleaning and surface-iron-removal by trace metal clean reagent. Photolithography is often used to define the source and drain liftoff pattern and the mesa etch pattern. Also, it is capable of making >1 μm gate length structure. For deep sub-micron gate length, the e-beam lithography method has to be utilized. The photoresist used by contact aligner is AZ-P4110, and the Polymethyl Methacrylate (PMMA) with 950K molecular weight is used for e-beam lithography. The photoresist is exposed under 436nm g-line UV light. E-beam lithography is performed in LEO-440 scanning electron microscope by direct writing, for which the pattern is designed in CAD-2000. After the exposure, we use Microposit MF™-CD-26 to develop the photolithography sample, and MIBK:IPA (1:3) mixed solution for the e-beam lithography sample. The detailed procedures are listed in Table 3. 1.

Sample cleaning	• Acetone, methanol, DI-water ultrasonic cleaning for 3 minutes each. • Clean in boiling aqua regia for 10 minutes, followed by DI-water rinse for 3 minutes. • De-hydration bake for 3 min in 160ºC oven.

Photoresist coating	• Spin AZ-P4110 photoresist for 40 seconds at 5000 rpm. • Soft bake for 10 minutes in 90ºC oven.
Exposure and developing	• Exposure in 436nm UV light for 90 seconds with power intensity of 6 mW/cm^{-2}. • Develop in MF-CD-26 for 40 seconds, rinse in DI water for 1 minute.
Metal deposition and lift off	• Deposit Ti/Al/Ni/Au metals with thickness of 30/1000/30/50 nm in the pressure of 10^{-6} Torr. • Soak the sample in acetone for 2 hours, apply ultrasonic appropriately for through metal lift-off. • Clean the sample in acetone, methanol, DI-water 3 minutes each, and dry it with N_2 blow.
Annealing	• 850ºC 1 minute in N_2 ambient for rapid thermal annealing.

(a)

Sample cleaning	• Acetone, methanol, DI-water ultrasonic cleaning for 3 minutes each. • De-hydration bake for 3 min in 160ºC oven.
Photo-resist coating	Same as that in table (a)
Alignment, exposure and developing	Same as that in table (a)
RIE etch	• Etch in ICP system for 5 minutes, with $BCl_3/Cl_2/Ar$ flow rate is 20/10/5 sccm; chamber pressure is 0.6 Pa, and RIE/ICP power is 80/15 W.

(b)

Sample cleaning	Same as that in table (b)
Photoresist coating	Same as that in table (a)
Alignment, exposure and developing	Same as that in table (a)
Metal deposition and lift off	• Deposit Ni/Au metals with thickness of 30/50 nm in the pressure of 10^{-6} Torr. • Lift-off is the same as what in table (a)

(c)

Sample cleaning	Same as that in table (b)
PMMA coating	• PMMA 950K spin for 40 second at 4000 rpm. • Soft bake for 40 minutes in 160ºC oven
Pattern writing and developing	• Write the pattern in SEM with pressure around 10^{-7} Torr, magnification is 1148, beam current is 10 pA. The mostly used line dose is 2.7 pC/cm, area dose is 260 nC/cm^2. • Develop the sample in MIBK:IPA (1:3) for 80 second, IPA for 20 second and rinse in DI water for 1 minute.
Metal deposition and lift off	Same as that in (c)

(d)

Table 3. 1 Summary for GaN HFET fabrication process: (a) Source/drain metal deposition; (b) Mesa isolation; (c) Gate defining and metal deposition (by photo-lithography); (d) Gate defining and metal deposition (by e-beam lithography)

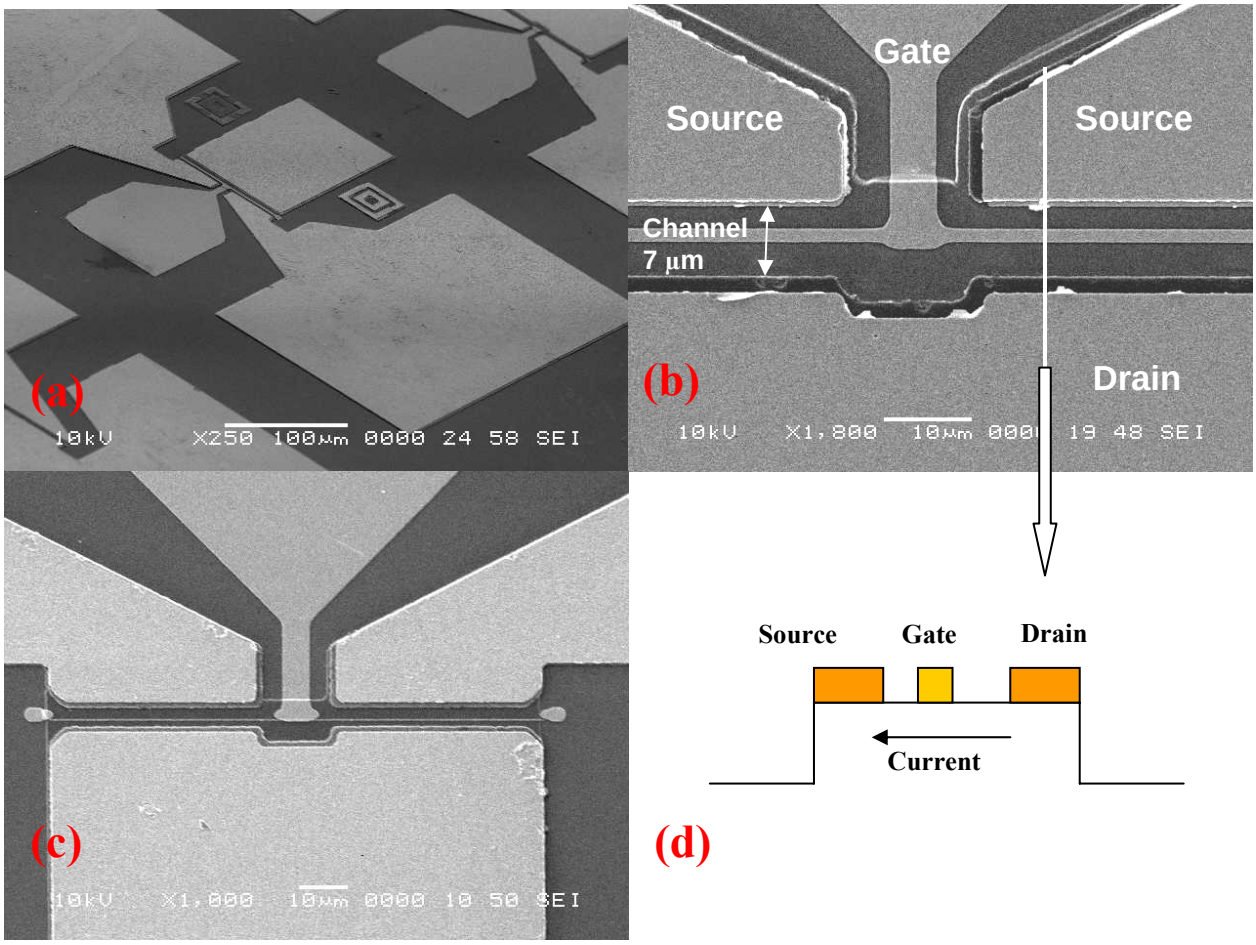


Figure 3. 1 SEM images for devices (a) HFET top view; (b) HFET fabricated by photo-lithography method, the channel length is 7 μm, gate length is 2μm; (b) HFET fabricated by E-beam lithography method, the channel length is 5μm, gate length is 200 nm; (d) schematic illustrate the cross section view of a HFET device.

Typical HFET devices after the fabrication are shown in Figure 3. 1. The Ohmic metal deposition scheme is Ti/Al/Ni/Au, in which Ti and Ni are e-beam evaporated and the rest metals are thermal evaporated, followed by rapid thermal annealing (RTA) in N_2 ambient for 1 minute. Mesa device isolation is performed in RIE/ICP etching system using $Cl_2/BCl_3/Ar$ plasma, and the typical etching rate is 30~50 nm/min. The gate definition process can utilize either photolithography or e-beam lithography with 100 nm gate length being achieved. The gate Schottky metal is Ni because of its large working function. The typical source-drain spacing varying from 5~ 8 μm, and gate width can be 40; 80 or 140 μm. The gate length defined by photo-lithography is around 1~2 μm, and 100-400 nm for the e-beam lithography.

3.1.2 Metallization and dry etch optimization

To effectively reduce the Ohmic contact resistance is very important for the improvement on the device DC and RF performance. The main mechanism of Ohmic contact formation on GaN is caused by the reaction between Ti and N and Ti-Al alloy formation[55, 56]. During our Ohmic contact optimization, two types of metallization scheme were tested: Ti/Al/Ti/Au and Ti/Al/Ni/Au, and different annealing temperature are examined respectively.

The reaction of Ti-N will generate N vacancies on the metal interface to GaN, which are known to be the shallow donor type defects. Therefore, the interfacial region becomes highly doped, which provides good tunneling path for the formation of Ohmic contact. Also the alloying between Ti-Al can decrease the resistivity in comparison with the metallization with only Ti. The role of Ni or 2nd Ti is the interlayer preventing the diffusion of Al into the top gold who serves as

the cap layer to avoid oxidization.

The method to determine the specific contact resistance of an Ohmic contact is the Transmission Line Modeling (TLM) method[57]. A linear array of contacts with various spacing is fabricated and the resistances between different contacts are measured. The specific contact resistance is calculated by the linear interpolation on those resistances. As shown in Figure 3. 2, TLM patterns are fabricated on 30 nm, 10^{17} cm^{-3} doped AlGaN barrier HFET samples. The conventional Ti/Al/Ti/Au (30/100/30/50 nm) rapidly thermal annealed (RTA) at 800ºC in N_2 ambient leads to typical contact resistance about 3.0 Ωmm, and specific contact resistance is around 5.4×10^{-5} Ωcm^2. Alternative Ti/Al/Ni/Au (25/125/30/50 nm) metallization scheme can improve the Ohmic contact property with contact resistance 1.2 Ωmm and specific contact resistance 2.0×10^{-5} Ωcm^2. Different anneal temperature was also examined from 780 ~ 900ºC, and the optimized temperature is confirmed to be 800ºC.

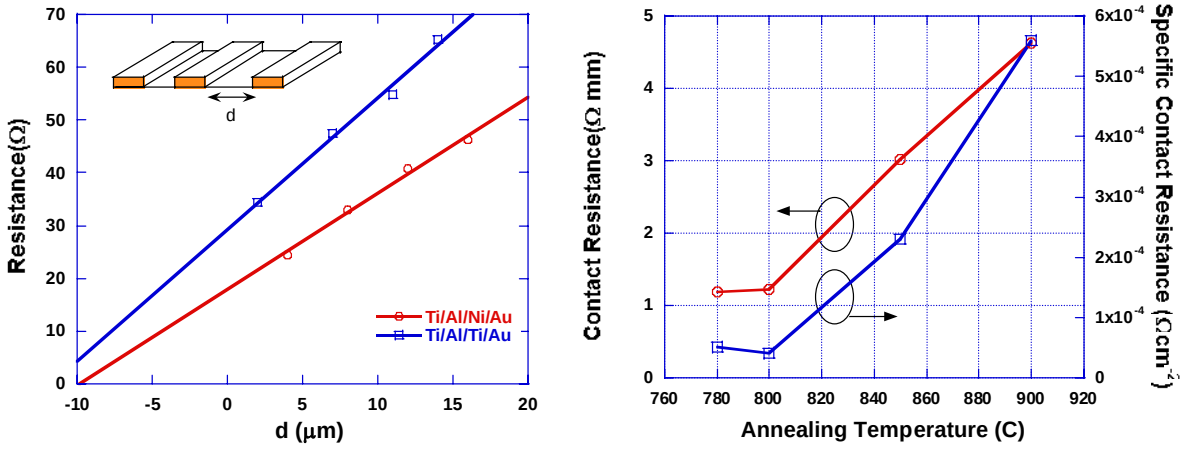


Figure 3. 2 Contact resistance measured in TLM configuration for different metallization schemes.

Most of etching processing for GaN devices is currently conducted by dry plasma etching.

Take RIE dry etch, for example, a typical etch system configuration is shown in Figure 3. 3. When applying the RF field between the gas showerhead and bottom electrode, the molecule of the etchant gas can be dissociated or ionized to form radicals, atoms, and ions during the collision. The active Chlorine-based radicals are accelerated and proceed onto the sample surface where they are absorbed and react.

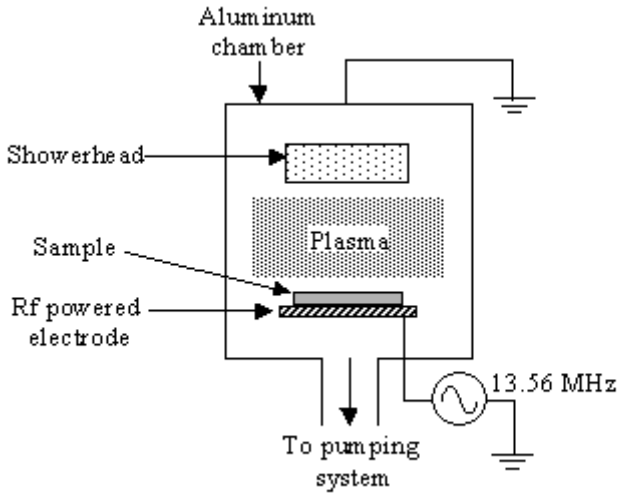


Figure 3. 3 The schematic for a RIE system for GaN dry etch.

Figure 3. 4 shows the relationships between the etch rate versus RIE power, chamber pressure, and gas flow rate. When the RF power increases, the etch rate increased from 10 to 60 nm/min while the surface roughness also increased from 0.4 to 1.4 nm. The degradation in surface smoothness is attributed to higher power levels, giving higher dissociation efficiency for the reactive radicals. Also high RF power will elevate the energy of ions and enhance the bombardment effect in dry etching.

On the other hand, the etch rate shows an almost linear decrease with chamber pressure. Both decrease[58] and increase[59] in etch rate as a function of pressure have been reported for

different dry etching systems. Much lower pressures may also reduce the reactive radical concentration which could lower the etch rate. But in the high-pressure regime, the mean-free path of the reactive ions is shorter due to collisions and therefore gives rise to the weaker bombardment effect. Also the sputtering desorption or re-deposition phenomena at high-pressure regime may also be the reason to the decrease of etch rate[60].

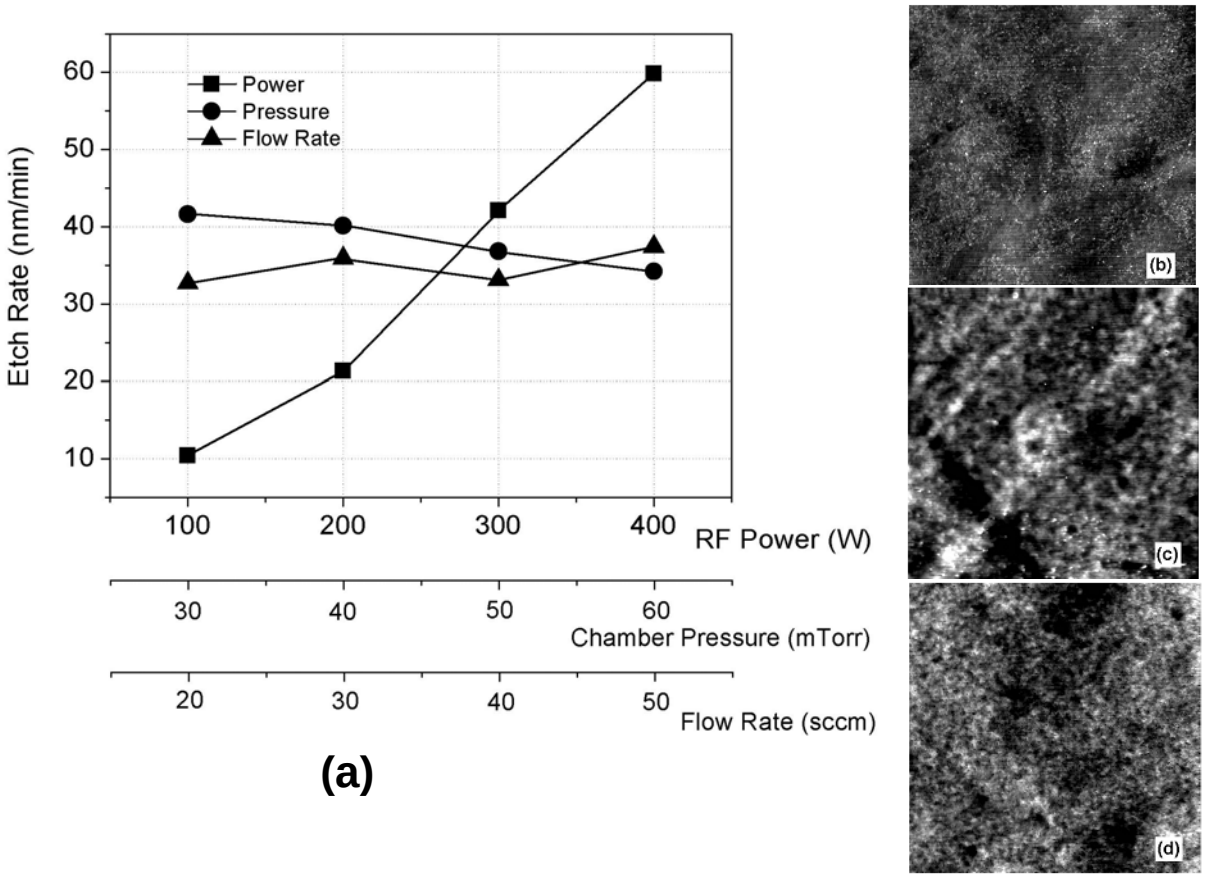


Figure 3. 4 (a) GaN dry etch rate in RIE system under different power, chamber pressure, and BCl_3 flow rate. (b), (c), (d) Surface morphology under 200, 300, and 400 W RIE etch power.

High-density plasma or energetic ion assisted etching were used to get a smooth etch surface and highly anisotropic sidewalls with high etch rates. But there are several disadvantages of dry etching, including the generation of ion-induced damage and difficulty in obtaining

smooth etched sidewalls. After dry etching, the surface potential always drops as measured from the scanning Kelvin probe microscopy (SKPM) measurements, which means the introduction in a large amount of surface states. Different surface treatments have been reported including N_2 plasma, thermal annealing, and KOH solution wet etch. From our observation, the leakage current of the Schottky contact can be reduced on some after-treated samples. KOH solution always provides the best treatment among all methods, for more detail please refer to ref. 61. In our new ICP system, the etchant is the combination of BCl_3, Cl_2 and Ar. The etch rate is controlled to be 50 nm/min, with a much smaller RF power to minimize the surface damage.

3.2 Device Characterization

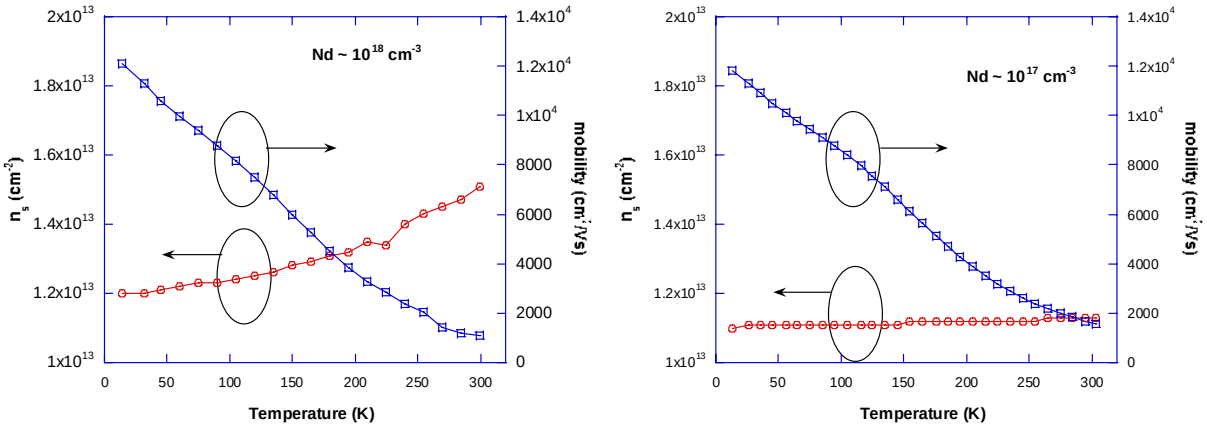
3.2.1 Transport properties

Prior to the device I-V measurements, the most important carrier transport properties of the GaN heterojunction, including temperature-dependent sheet carrier concentration and mobility, are examined by Hall measurements. The Van der Pauw pattern is defined on the rectangular shape samples (~8×8 mm^2), followed by Ohmic metal deposition and rapid thermal annealing. The samples are measured in the Lakeshore™ Hall Measurement System.

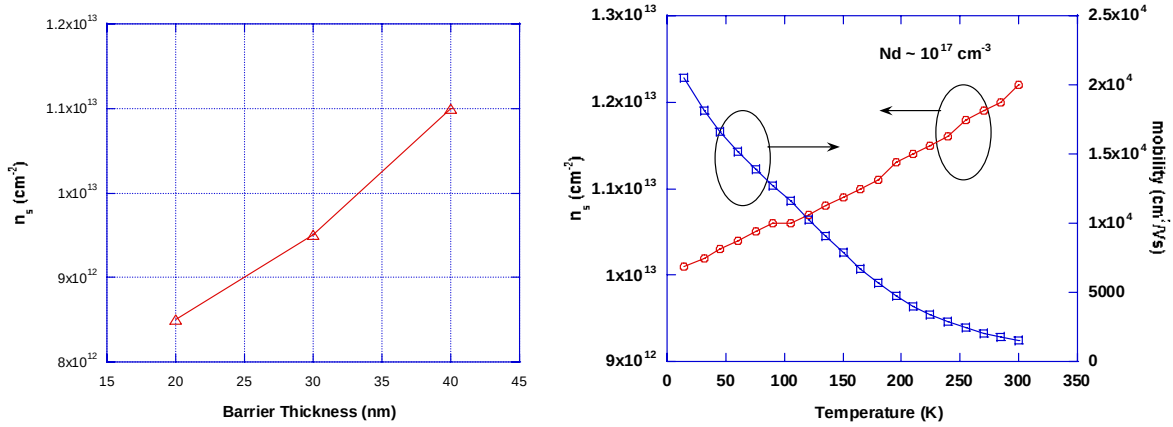
2DEG sheet carrier density and electron mobility under different barrier doping level and barrier thickness are shown in Figure 3. 5. Picture (a) is for 40 nm AlGaN barrier. With 10^{17} cm^{-3} level doping, the room temperature sheet carrier concentration approximates to 1.0~1.1×10^{13} cm^{-2} and mobility is 1400~1600 cm^2/Vs. While for higher doping concentration (10^{18} cm^{-3}) these numbers become 1.3~1.5×10^{13} cm^{-2} and 1000~1200 cm^2/Vs. Notice that the higher doping introduces certain parallel conduction, which does not contribute to the 2DEG at room temperature and is frozen out under low temperature. The 10^{17} cm^{-3} doping sample shows almost

no temperature dependency in sheet electron density, which means the conduction comes only from the degenerated electron population or 2DEG. It also indicates that there exists no parallel conduction path and furthermore proving the semi-insulating properties of buffer layer. Figure 3. 5 (b) shows the change of sheet carrier density with different AlGaN barrier thickness and an almost linearly relation is observed.

AlInN barrier with near lattice matched In% (19%) and 20 nm thickness was also characterized by Hall measurement as shown in Figure 3. 5 (c). The room temperature mobility is comparable with that of the AlGaN sample, while the low temperature (12K) one is improved to 21000 cm^2/Vs. With the same growth scheme on GaN buffer, we assumed this is due to the elimination on piezoelectric field and the reduction of the defects within the barrier.



(a)



(b) **(c)**

Figure 3. 5 (a) Temperature dependent sheet carrier density and mobility with different doping for 40 nm $Al_{0.3}Ga_{0.7}N$ barrier. (b) The relation between different barrier thickness and sheet carrier density for $Al_{0.3}Ga_{0.7}N$ barrier with 10^{17} cm^{-3} doping. (c) Temperature dependent sheet carrier density and mobility for 20 nm $Al_{0.81}In_{0.19}N$ barrier with 10^{18} cm^{-3} doping.

The logarithm plot on the temperature dependent 2DEG mobility on both AlInN and AlGaN barrier samples is shown in Figure 3. 6. By linearly fitting the mobility onto temperature regime, similar dependence coefficients are obtained for both samples. The mobility has a dependence of $T^{-0.17}$ at low temperature, and $T^{-2.41}$ at high temperature. We may infer from this coefficient that the piezoelectric scattering mechanism may be dominant in determining the low temperature mobility[62]. Since the GaN channel for both AlInN and AlGaN samples is grown at the same condition, so the ionized impurities scattering should be similar in both sets. The higher low temperature mobility for lattice-matched AlInN HFET indicates the reduction in the piezoelectric scattering effect. As for the room temperature mobility, from the coefficient we can infer it is limited by the polar optical phonon scattering mechanism.

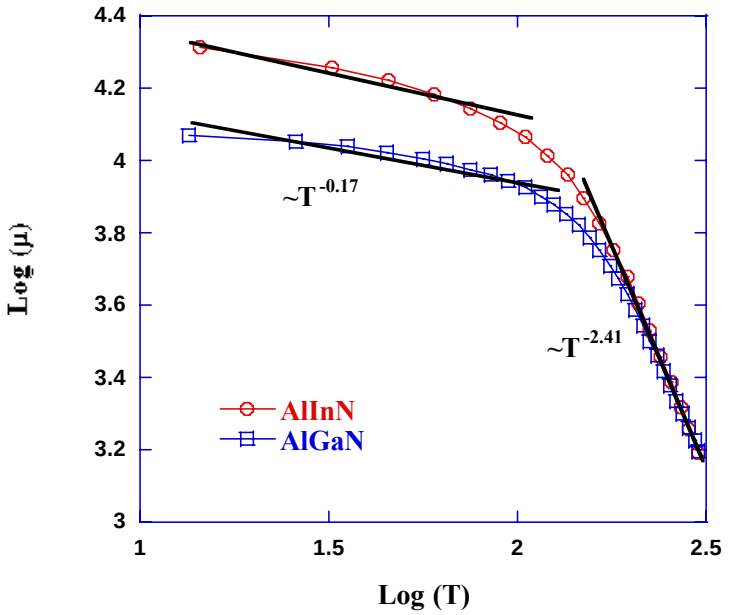


Figure 3. 6 The logarithm plot of carrier mobility vs. temperature for both AlInN and AlGaN barrier structure.

3.2.2 DC characterizations

The IV and CV characterizations of the HFET are measured using the Keithley parameter analyzer. For the typical AlGaN barrier HFET, I_{DS}-V_{DS}, gate leakage current, transconductance, and gate capacitance properties are shown in Figure 3. 7. Good channel pinch-off is observed at -3 ~ -4 V gate bias, and low knee voltage appears around 2 - 4 V. At the large drain bias case, an obvious current drop is always observed due to the rising of channel temperature by the self-heating effect. The gate leakage current is around μA range even without surface passivation. The maximum transconductance for a typical 40 μm gate width device is around 170~200 mS/mm reached when drain bias is 3~5 V. From the CV measurements, a sharp transition is observed and the threshold voltage is consistent with pinch-off voltage from IV measurements.

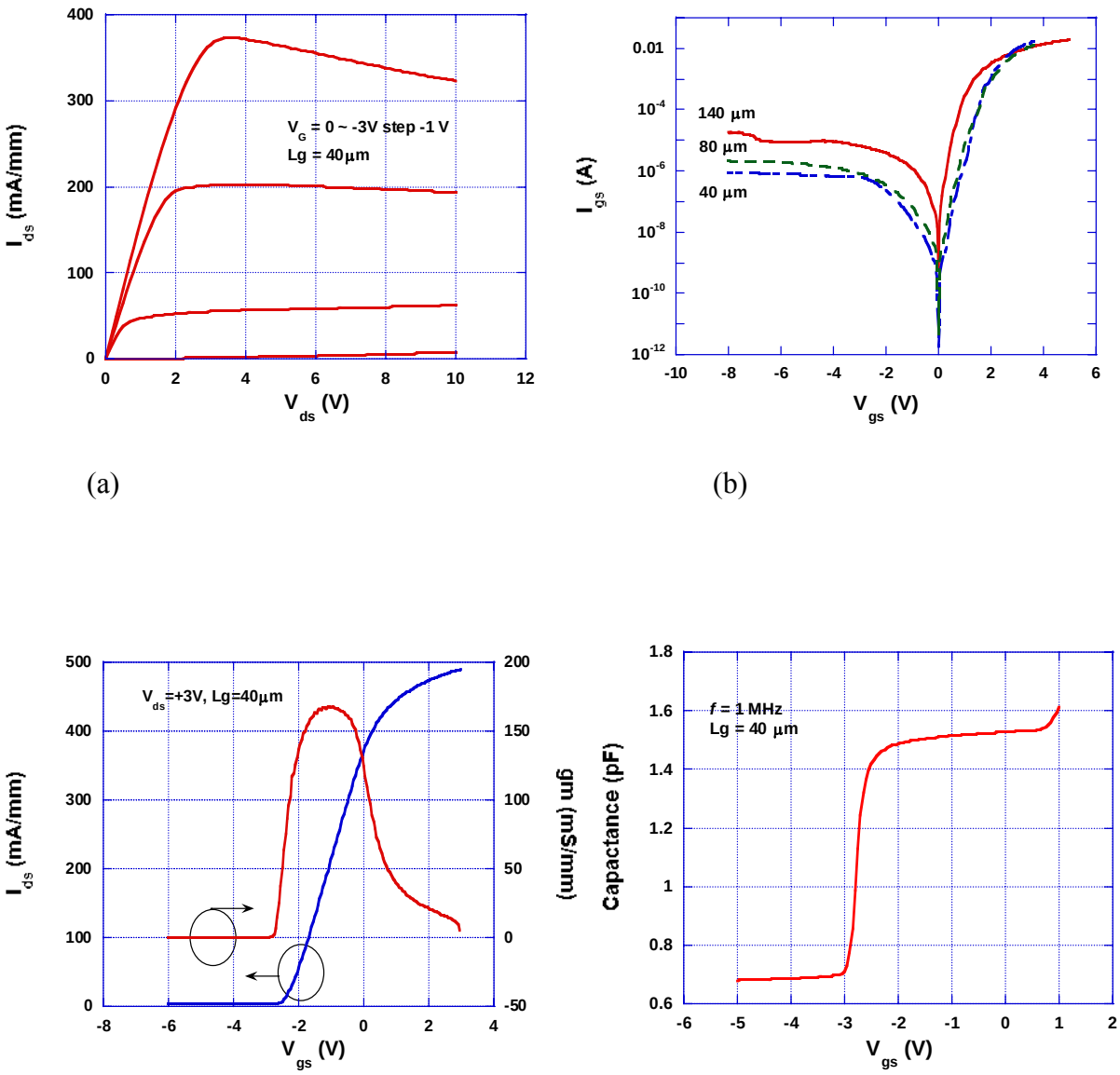


Figure 3. 7 IV characteristics of a 30 nm $Al_{0.3}Ga_{0.7}N$ barrier HFET (a) I_{DS} vs. V_{DS} (b) I_{GS} vs V_{GS} (leakage current) on different gate width (c) I_{DS} vs. V_{GS} and transconductance (at V_{DS} = 3V). (d) gate capacitance for 40 µm gate width device, measured at 1.0 MHz frequency.

Compared with AlGaN barrier HFET, the AlInN barrier device with In% = 18% has

higher saturation current since both n_s and mobility are improved. The transconductance reaches 260 mS/mm at 5V drain bias for 20 nm barrier sample, as seen in Figure 3. 8. Good current pinch-off can be obtained at -4 ~ -8V, depends on the thickness of the barrier. The gate leakage is similar to AlGaN case within μA range for 40 μm wide gate device.

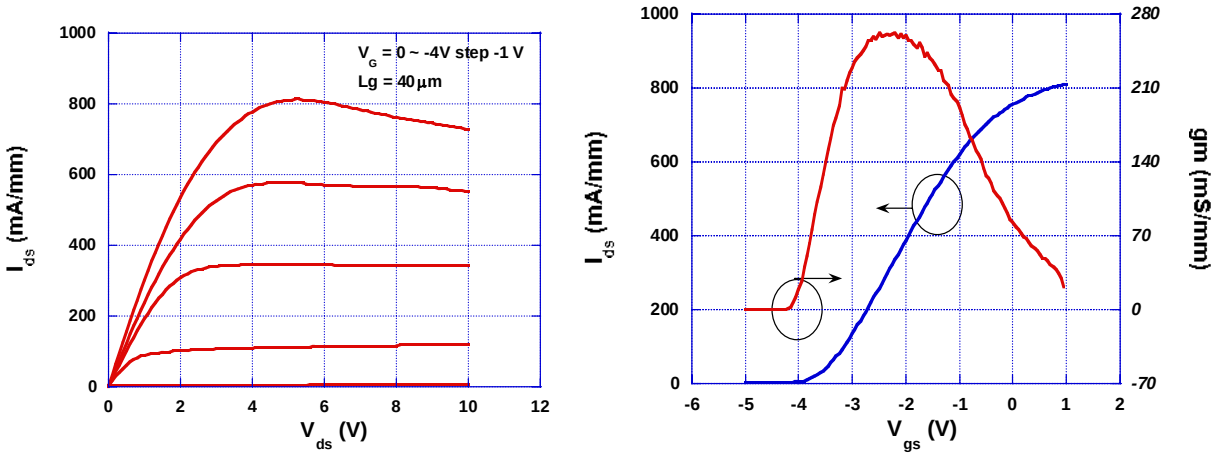


Figure 3. 8 IV characteristics for 20 nm $Al_{0.82}In_{0.18}N$ barrier HFET.

Drain current collapse can significantly affect the performance of nitride HFET. We also checked the DC current collapse for both AlGaN and AlInN HFETs. As shown in Figure 3. 9(a), drain current always collapse after turning off the visible light excitation, which makes us believe the light helps to generate extra free electrons from deep levels defects. The extent of current collapse varies from sample to sample, regardless if it has AlGaN or AlInN barrier. The collapse is observed even when gate is absent. On the gate-less structure, there is a significant reduction in current between two consecutive drain voltage sweeping up scan, as shown in Figure 3. 9(b). The drain current tends to have less reduction at high drain bias among the scans. It has been reported this instance is related to the trapping effect in the buffer layer, which was

interpreted in terms of deep traps formed under the high-resistivity GaN growth conditions[63, 64]. The collapse was not observed in the devices grown on conducting substrates in which case the traps are already filled by electrons from shallow donors[65].

We define the extent of current collapse by the maximum current drop percentage between two consecutive scans on a gate-less structure when light is OFF. The samples with high buffer growth pressure (200 Torr) always provide lower current collapse number compared with the low pressure (30 Torr) ones. This is because the low growth pressure facilitates the formation of deep level traps such as carbon impurity incorporation.

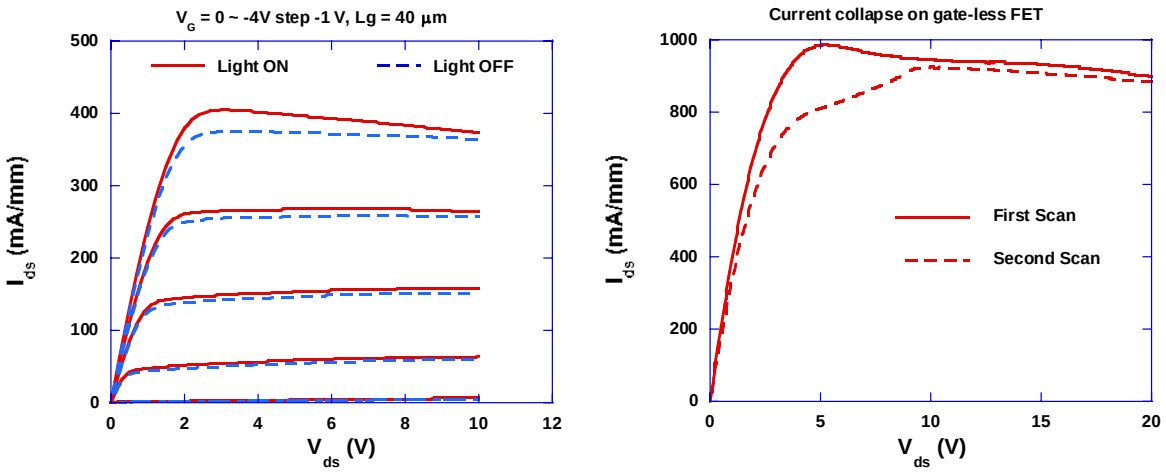


Figure 3. 9 DC Current collapse phenomena for (a) AlGaN FET, and(b) gate-less AlInN FET.

3.2.3 RF characterizations

The equipments used for RF measurements include HP 8510B network analyzer, HP 6629A DC power supply system, wafer prober, HP8514B S-parameters test set that goes from 45 MHz to 20 GHz and HP 33150A bias tees. The network analyzer measures the magnitude and the phase of the S-parameters. The S-parameters test set terminates the HFET device in the

required impedance. The bias tees consist of an inductor and a capacitor; the inductor keeps the AC signal from leaking into the DC power supply; and the capacitor keeps the DC power from interfering with the network analyzer. Figure 3. 10 shows a block diagram of the setup used in this measurement.

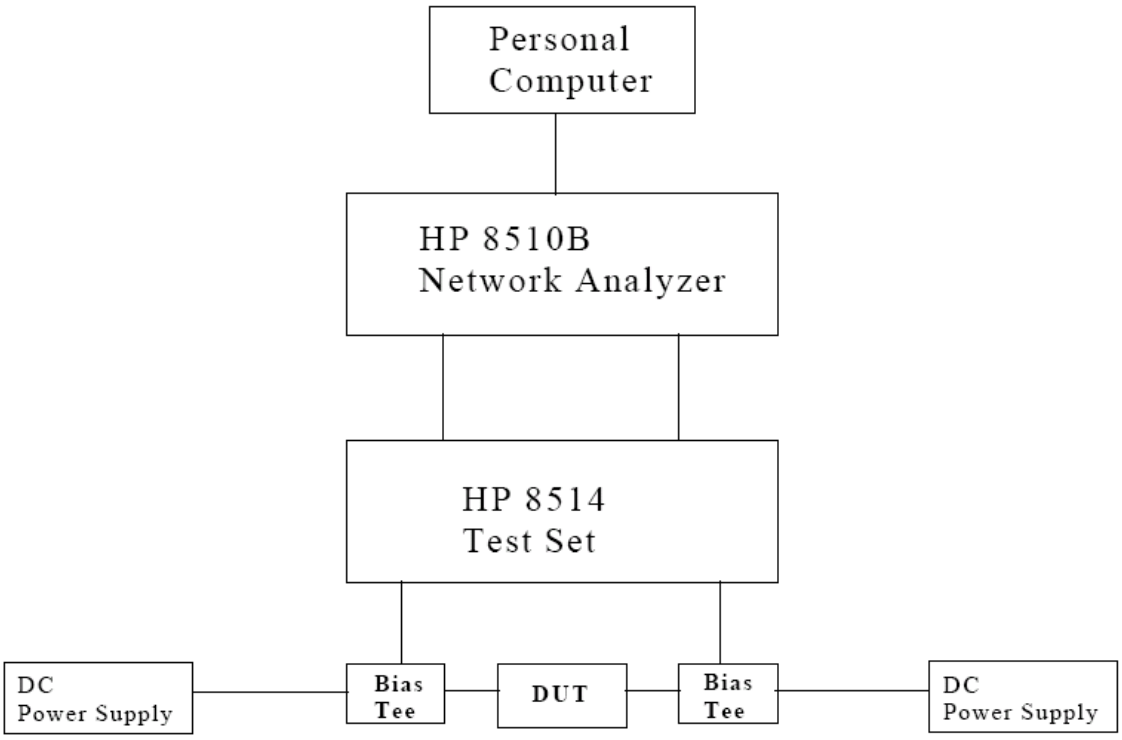


Figure 3. 10 Block diagram of the S-parameter measurement equipment

Before the measurements could be made, the probes had to be calibrated. There are two probes: one accesses the gate side of the device and the other accesses the drain side of the device. Calibration involves removing the parasitic effects of the probes, the cables, and the connectors in order to evaluate the only S-parameters of the device. A set of calibration standards exists. First, the response of the system to a "Short" is measured. This involves placing the probe on a strip of metallization; all the contacts are shorted. Next, the response of the probe to an

"Open" is measured, and for this, the probe is left in the air and is not contacting anything. The Load calibration involves placing the probe contacts on two 100 Ω resistors that are in parallel. Finally, the response of a "Load," which is a resistive 50 Ω transmission line is measured. These measurements are applied to an error correction term, which has been programmed into the network analyzer. In the Smith Chart display of the HP vector network analyzer, the Short is seen as a dot where the reflection coefficient Γ is, $\Gamma = -1$. Also, when the Open is measured, it is displayed a dot where $\Gamma = 1$. The Load used is the characteristic impedance of the line and it displays a dot at $\Gamma = 0$. Finally, for an independent verification, the calibration is verified with an inductor. This traces out a smooth curve of inductive reactance as the frequency is swept.

After the calibration, the device is properly biased and the S-parameters are measured with the frequency ranging from 2GHz to 20 GHz. Figure 3. 11 gives the typical S-parameters measured on L_g = 1 um, L_w = 40 um device,

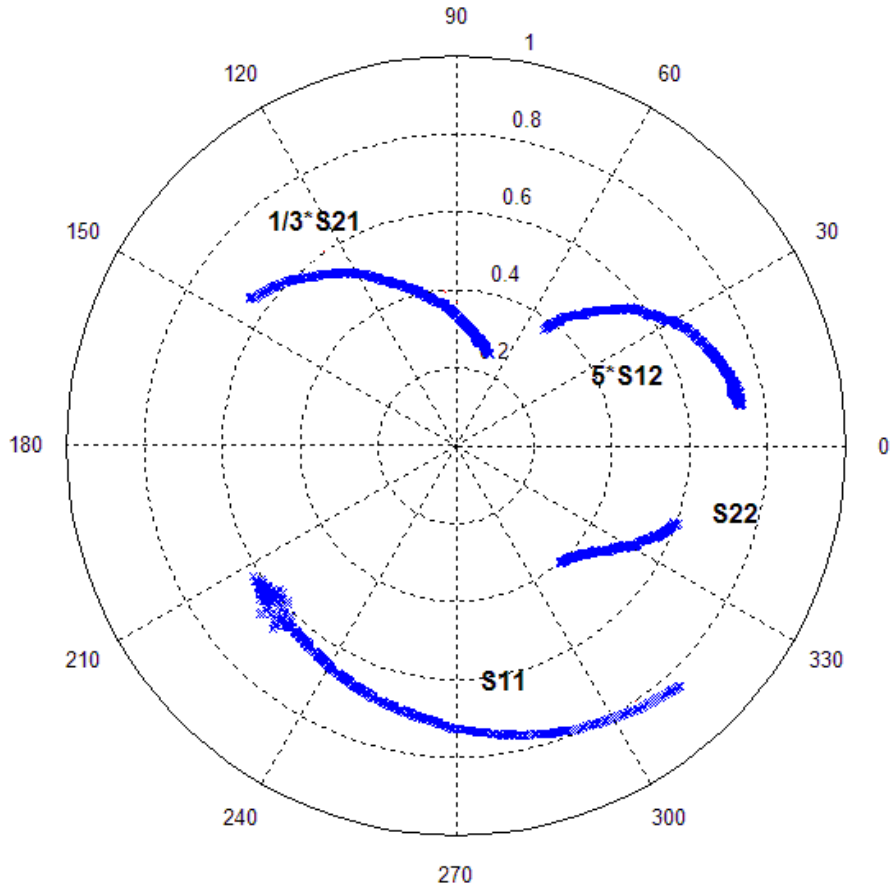


Figure 3. 11 Typical S-parameters for 1μm gate length, 40 um gate width device, frequency from 2G to 20GHz.

After converting S-parameters into H-parameters, we could extract the current cut-off frequency (f_T) as seen in Figure 3. 12. Three different gate width devices are compared. The e-beam lithography sample has 200 nm gate length (L_g) and 40 μm gate width, whose f_T reaches up to 21 GHz. From the relationship:

$$f_T = \frac{v_s}{2\pi L_g}$$

Equation 3. 1

the electron saturation velocity of the device is close to 10^7 cm/s.

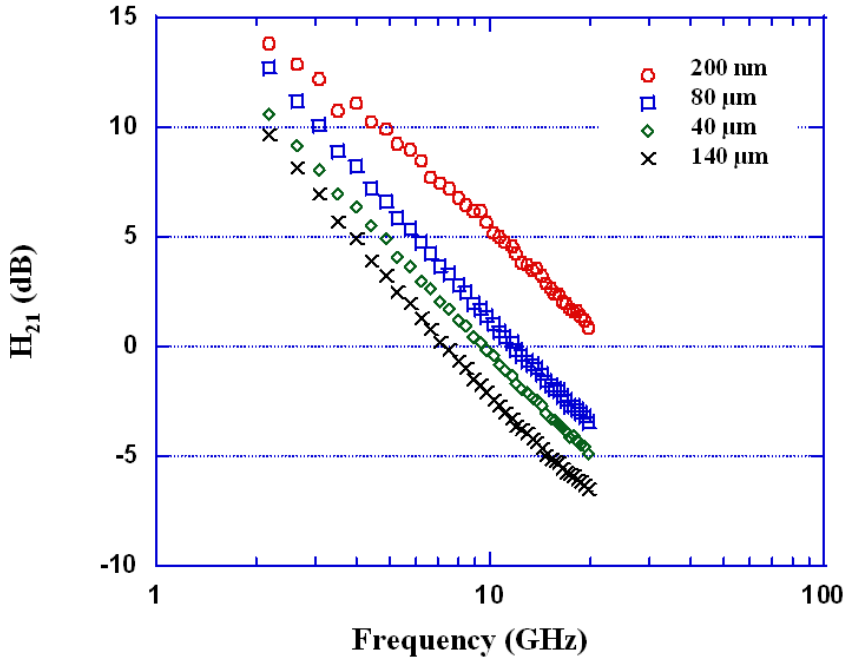


Figure 3. 12 Current gain (H_{21}) for HFETs fabricated by e-beam lithography and photolithography.

3.3 New Device Structures

3.3.1 Recess gate HFET

In the usual GaN HFET structure, the barrier is moderately doped and the surface donor states are believed to provide most of the electrons in 2DEG. However, the density of surface states can hardly to be monitored throughout the experiments. It also means the device performance is sensitive to the surface condition which hampers the improvement on the stability.

In order to eliminate the influence from surface states, we can either intentionally increase the barrier thickness, or put another heavily doped (n+) cap layer to provide enough electrons instead. The increasing in barrier thickness do provide more electrons from doping[45], but it also

gives less electron mobility due to the long range scattering effect. Also, the highly doped barrier introduces the problem of leakage current and parallel conduction. Therefore, the n+ cap layer plus the recess gate fabrication seems to be more applicable for HFET.

If looking at the GaAs devices, the effect of surface trapping effects in GaAs MESFETs was reduced to manageable level through the control on the recess gate geometry, proper dielectric passivation and modifications to the epitaxial layer doping profile[66, 67]. For HFET devices, by employing an n+ GaAs cap layer on the conventional heterojunction device structure, one can mitigate the impact of charging and discharging from surface states and reduce the dispersion effect. The gate recess fabrication technique must be applied in order to reduce the gate leakage and maximize the transconductance. The similar structure has been applied to GaN to improve the device performance with lower parasitic resistances and better breakdown characteristics [68, 69]. Additionally, the insertion of n_+ cap layer beneath the source and drain electrodes can effectively improve the Ohmic contact property. The typical device structure is shown in Figure 3. 13. To process the recess gate GaN HFET, plasma dry etch with enhanced selectivity is the key. Also sub-micron lithography method is preferred to define the gate.

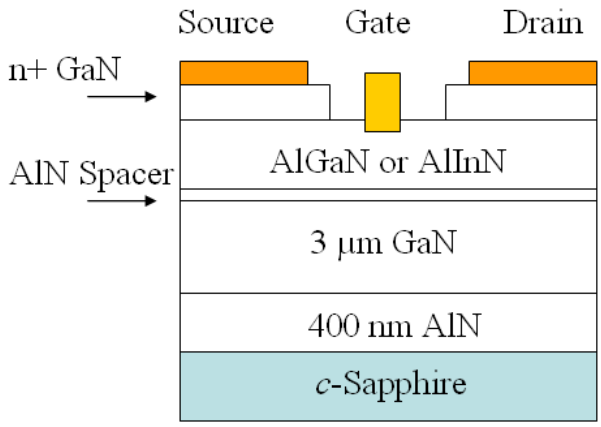


Figure 3. 13 The n+ cap HFET device structure with recess gate.

Figure 3. 14 shows the fabrication procedures for a recess gate HFET. There are two kinds of processing methods: selectively dry etch method and cap layer re-growth method. For the first one, etch has to be controlled precisely to stop at the cap/barrier interface. The traditional GaN ICP/RIE dry etch employs Chlorine-based plasma, which can hardly be used for recess gate fabrication because of its low etching selectivity between the cap and the barrier. An introduction of sulfide or oxygen into the gas etchant may improve the selectivity and the etch rate for Al-ternary in such case is usually slow. For the other method, after the growth of the conventional HFET, the patterned SiO_2 film covering the channel area is ex-situ deposited as the re-growth mask. Then the sample is loaded back into MOCVD for the n+ GaN cap layer re-growth. After that, the SiO_2 is removed and the regular fabrication procedures will be conducted on the re-growth sample. In the following, I will present the experimental results from both methods done on AlInN barrier devices.

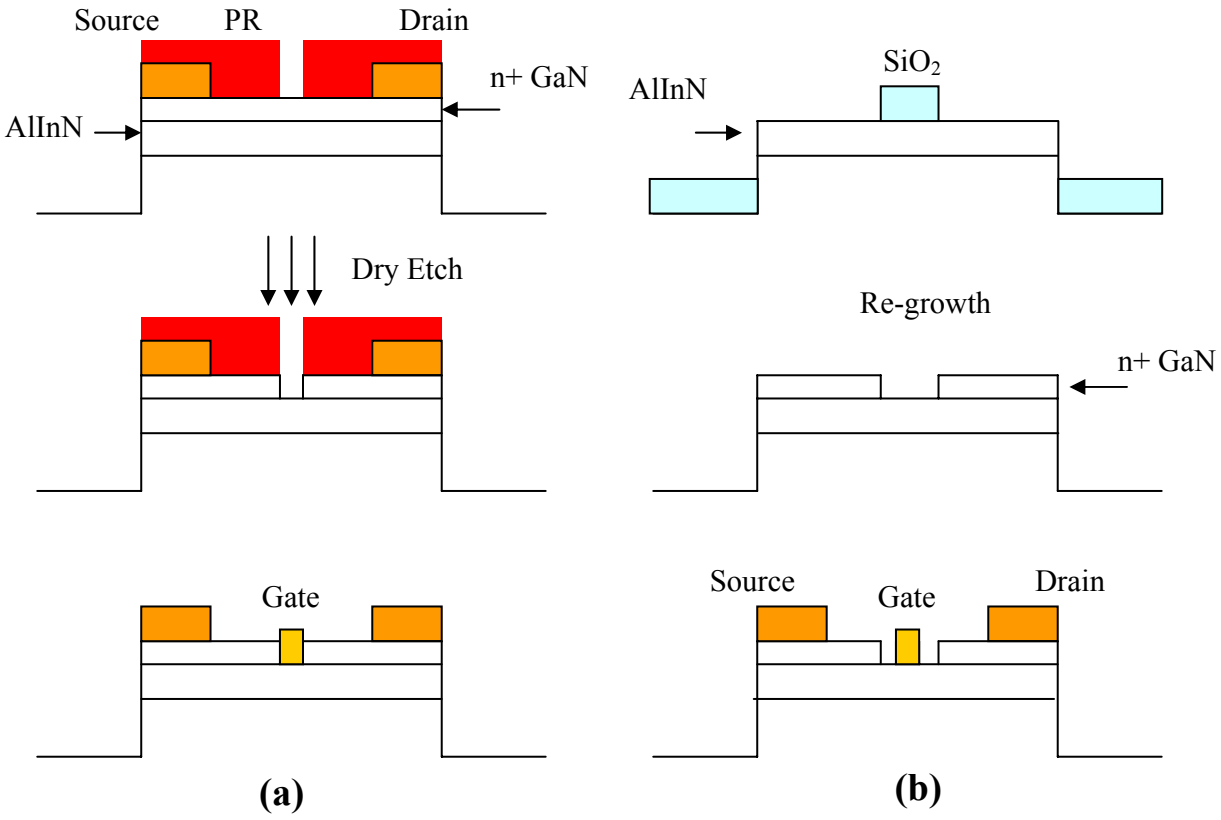


Figure 3. 14 The fabrication procedures for recess gate HFET, (a) selectively dry etch method; (b) n+ cap layer re-growth method.

(a) Selectively dry etch method

When growing the AlInN/AlN/GaN devices, I kept the 20 nm AlInN layer undoped followed by a 60 nm mid-10^{18} cm^{-3} doped GaN cap layer. Figure 3. 15 shows the temperature dependent mobility and sheet carrier density on this device structure. The sample gives the sheet carrier concentration about 1.2×10^{13} cm^{-2} at 10 K, which we believe only come from the carriers in channel.

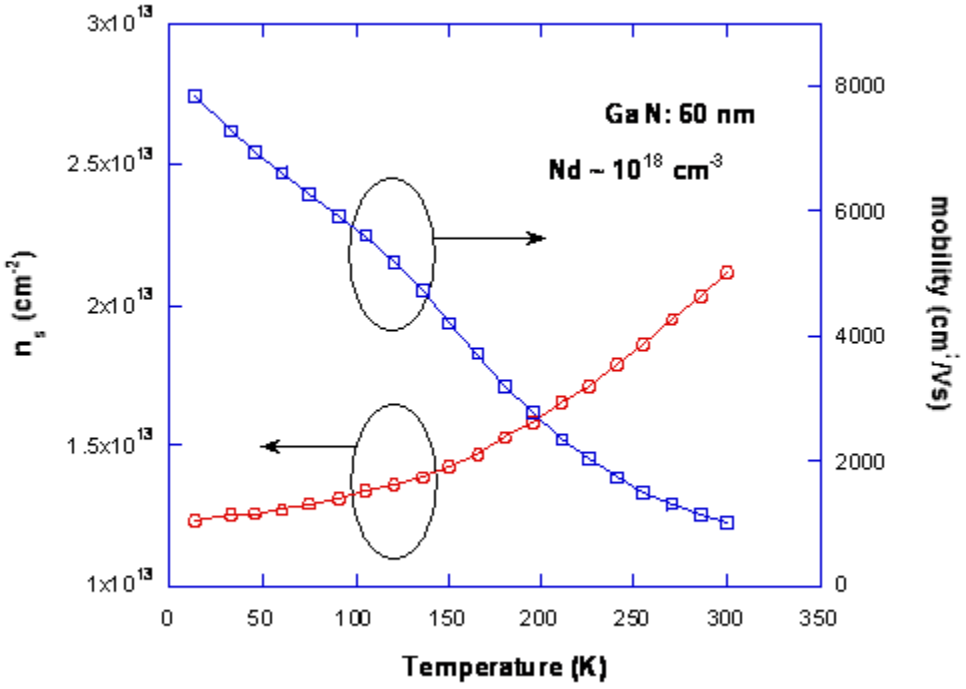


Figure 3. 15 Temperature dependent mobility and sheet carrier density from a 20 nm AlInN barrier structure with 60 nm n+GaN cap layer.

According to ref. 70, the measured total mobility and sheet carrier density for a semiconductor consist of two parallel conduction paths can be expressed as:

$$\mu n = \mu_1 n_1 + \mu_2 n_2$$
$$\mu^2 n = \mu_1^2 n_1 + \mu_2^2 n_2$$

Equation 3. 2

Here in the n+ cap structure, it assumes the 2DEG all comes from the ionized donor in cap layer, and part of the cap is still un-depleted. In Equation 3.2, one conduction path is 2DEG, and the other comes from the top un-depleted n+ GaN. At room temperature, as seen from Figure 3. 15, we take the overall μ and n to be 1000 cm^2/Vs and 2.1×10^{13} cm^{-2}. And 2DEG has μ_1 and n_1 equal to 1200 cm^2/Vs and 1.5×10^{13} cm^{-2} from the low temperature data. Then the calculated un-

depleted n+ cap is about 20 nm thick, and estimated to have doping level around 4.5×10^{18} cm^{-3}, which is consistent with the growth data.

It has been reported the adding of SF_6 into the BCl_3 plasma using the ICP etching system will improve the etch selectivity at GaN/AlGaN interface[71, 72]. A very thin AlF_x layer is believed to form when the etch-front reaches AlGaN barrier revealed from XPS[73]. Consequently, this layer provides protection to prevent further ion bombardment and plasma etching on AlGaN. The etching rate of AlGaN layer will be retarded and the etching selectivity between GaN and AlGaN materials can be enhanced. Various etch schemes are reported and usually the composition of SF6 is around 20% to reach the maximum etch selectivity ranging from 25 to 80, which is defined as the ratio between etch rate of GaN and AlGaN at this gas combination. Meanwhile, the post dry etch treatment (CF_4/O_2 plasma) may be useful to reduce gate leakage and increase breakdown voltage[74].

In our ICP/RIE dry etch system, I tried $BCl_3/Ar/SF_6$ mixture aiming at the high etch selectivity on n+ cap device structure. The etch rate under different SF_6 flowrate was tested on on a thick AlInN sample and a GaN sample respectively. As shown in Figure 3. 16 (a), it is obviously that the introduction of SF_6 will significantly reduce the etch rate for both material, more pronounce on AlInN. The selectivity plotted in Figure 3. 16(b) increases when more SF_6 involved while the GaN etch rate also experiences a fast drop. The roughness of AlInN surface after etch is plotted the same figure that varies from 0.5 to 1.7 nm. The optimized SF_6 flow rate I used here is 6 sccm, since it gives largest selectivity meanwhile does not deteriorate the etch rate on GaN layer too much as well.

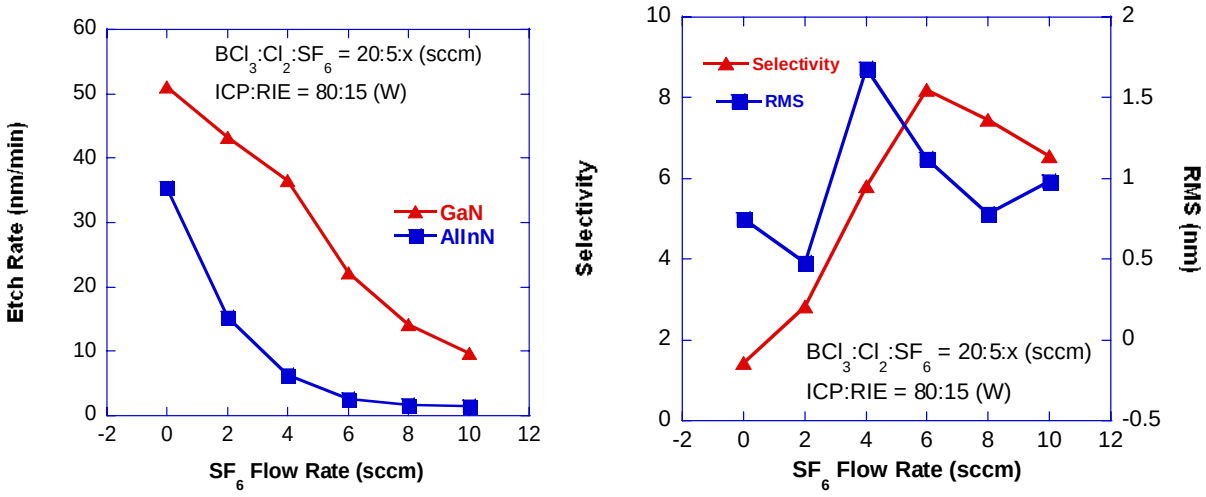


Figure 3. 16 The influence of SF_6 flow rate on (a) the etch rate of GaN and AlInN; (b) the selectivity, and stop layer surface roughness of a AlInN with n+ GaN cap.

The same receipt was applied on the AlInN sample with 60 nm n+ GaN cap layer shown in Figure 3. 15. The etching time was 3.5 min that is controlled to ensure the 60~70 nm etch depth. The surface morphology of the etching stop layer was confirmed from AFM measurement, as shown in Figure 3. 17.

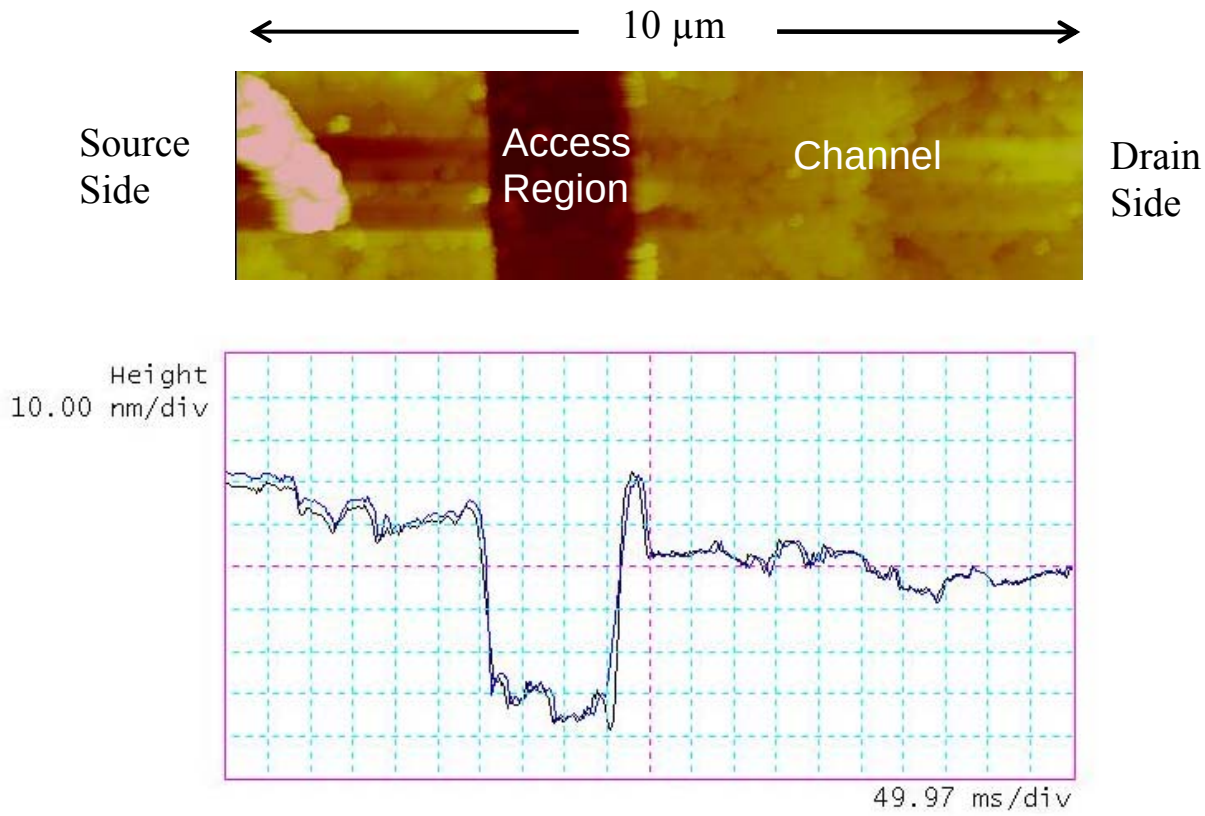


Figure 3. 17 Surface morphology channel after selectively dry etch.

After the dry etch, the gate metal was directly deposited and lifted off, without removing the photo-resist etch mask. The fabricated device has I-V characterization shown in Figure 3. 18. Compared with conventional HFET, the saturation current and transconductance are much lower, while the gate leakage is higher (See Figure 3. 20 (c)). The current pinch-off property is getting worse and channel breakdown phenomenon appears at lower bias. It has been reported the fluorine-based plasma can introduce strong immobile negative charges in the channel and effectively raising the potential of barrier. Normal-off enhance mode HFET has been fabricated by applying fluorine plasma treatment[75]. Therefore, we suspect that the adding of SF_6 during dry etch, although it can improve the selectivity of dry etch process, introduce extra defects in the

barrier that dramatically downgrade the performance of the device.

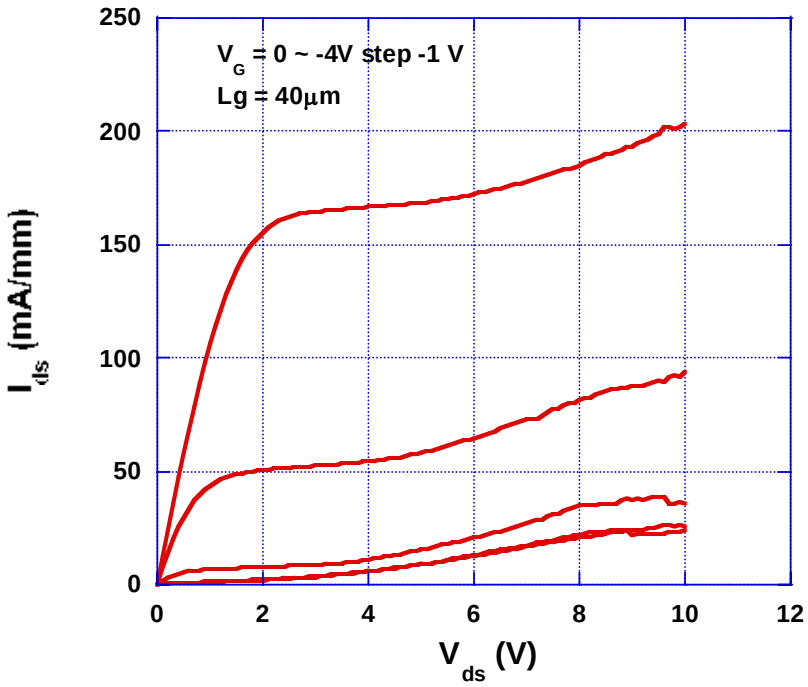


Figure 3. 18 I-V characterization for a $Al_{0.82}In_{0.18}N$ HFET sample with 60 nm n+ GaN cap, fabricated by selectively dry etch method.

(b) Cap layer re-growth method

In this method, the formation of the patterned SiO_2 mask is done on the conventional AlInN barrier structure with the following steps: (1) GaN dry etch to form the device mesa and alignment marks; (2) deposition of 100 nm SiO_2 layer by UHVCVD; (3) photo-lithography to open windows on source and drain region; (4) oxide dry etch in CF_4 plasma; (5) photo-resist cleaning for re-growth. The process details are shown in Figure 3. 19. During the oxide dry etch, RIE power is set to zero to reduce surface damage, and the etching time is prolonged to over-etch the oxide laterally. A 60 nm GaN cap layer is re-grown from the open source and drain window

with 10^{18} doping level. After re-growth, the source/drain and gate metallization are fabricated in the same way as the conventional HFET.

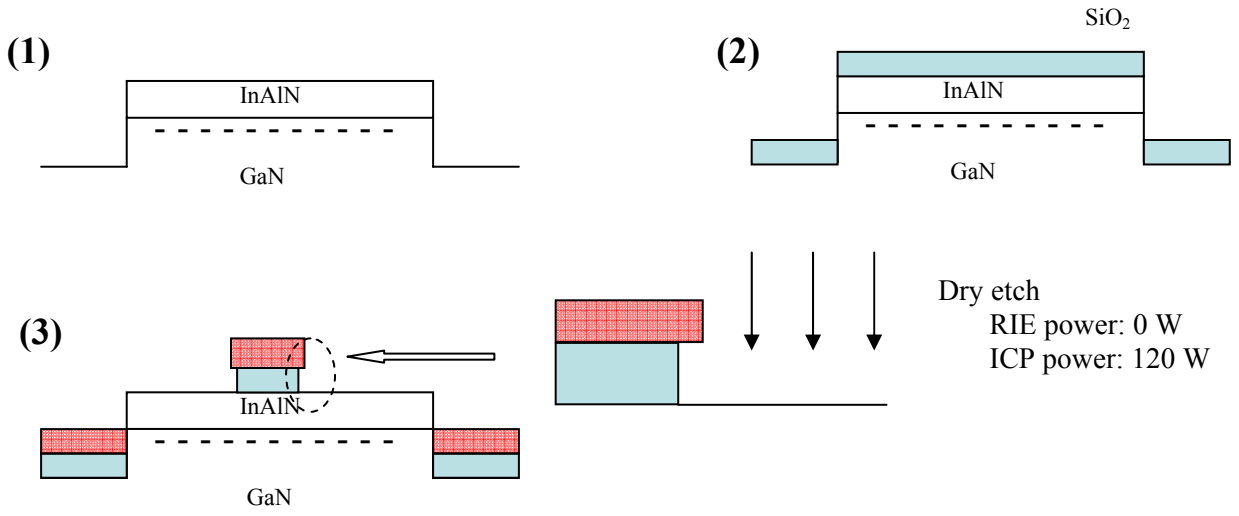


Figure 3. 19 Details on the formation of SiO_2 overgrowth mask: (1) mesa isolation, (2) SiO_2 deposition, (3) photo-lithography and plasma dry etch.

The DC I-V characteristics of the recess-gate HFET fabricated in this method are listed in Figure 3. 20. Both recess gate device (by re-growth method) and reference device (no n+ cap, barrier is doped to 10^{17} cm^{-3}) demonstrate good channel pinch-off. The saturation current of recess gate HFET is similar to the reference sample, however the saturation voltage is higher due to the extra access resistance under the source and drain pads. There is an obvious current kink observed on recess gate HFET, which we believed is introduced from the electron traps existing in the channel region[76, 77.] The transconductances of both devices at 5V drain bias are compared in Figure 3. 20 (b); both have peak value around 200 mS/mm. Also, the gate leakages are shown among all three types of devices with same device dimension. The conventional HFET give the lowest leakage current, which is below 10^{-3} mA for 40 μm wide gate. The dry etched method

leaves the largest gate leakage probably due to plasma-induced surface damages.

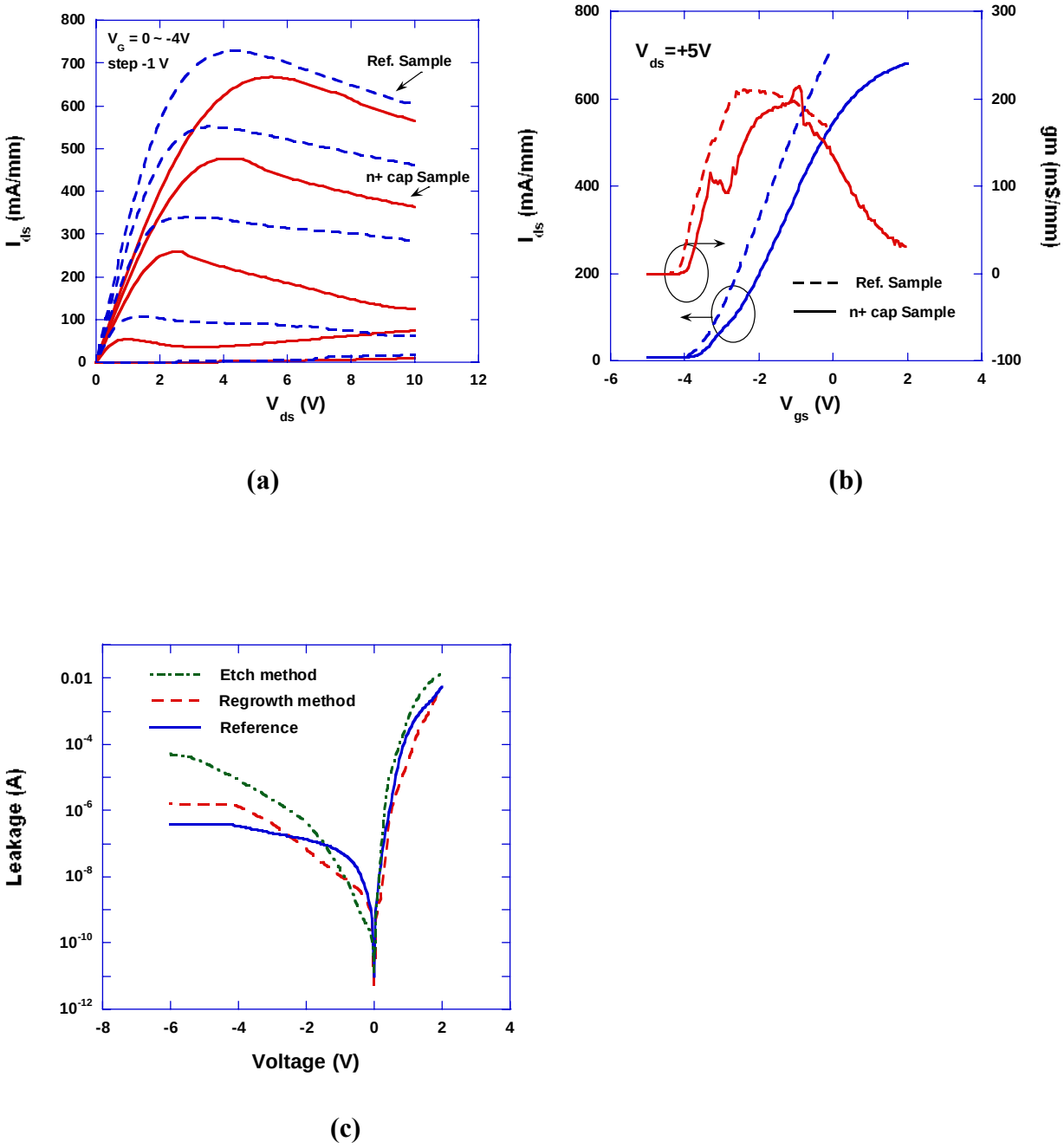


Figure 3. 20 The compare in IV characteristics between reference AlInN HFET and recess gate HFET (a) Ids – Vds of reference and recess gate samples by fabricated by re-growth method; (b) transconductances of

reference and recess gate samples by fabricated by re-growth method; (c) gate leakage current of reference and recess gate samples by fabricated by re-growth method and selectively dry etch method.

From the experiments done above, the recess gate fabrication procedures can easily introduce surface states or etch damages at the gate region. The identification of those defects needs to be further investigated by pulse measurements. The re-growth processing method brings less influence on devices structure, but no obvious improvements in DC characteristics are observed.

3.3.2 MIS HFET

It has been reported that the GaN metal-insulator-semiconductor HFET (MISHFET) can significantly decreased gate leakage current and increased breakdown voltage compared to the conventional structures. Different insulator materials such as SiO_2, Si_3N_4, Al_2O_3, ZrO_2, AlN and HfO_2 have been examined and discussed respectively in ref. 78, 79, 80. The insertion of dielectric layer under the gate would reduce the transconductance and the gate capacitance. On the other hand, some insulators can serve as surface passivation layers to reduce the density of surface states, leading to smaller current collapse effect[81, 82]. The RF performance of MISHFET is often reported to exceed that of normal AlGaN/GaN HFET[83, 84]. The state-of-the-art MISHFET has demonstrated current gain cut-off frequency (f_T) of 181 GHz and maximum oscillation frequency (f_{max}) of 186 GHz by using an ultra-thin Si_3N_4 gate dielectric layer[85]. The improvement of RF performance might be ascribed to the screening of the Coulomb scattering from the charged surface defects by the dielectric layer[86]. However, the question of which insulator is the best material still stands. High dielectric constant (κ) materials such as ZrO_2 and PZT have more potential by providing less gate capacitance and the ability to use thicker layers to further reduce leakage current. But the imperfection of the material quality due to different

crystalline structure and large lattice mismatch between the high-κ insulators and GaN, and the difficulty of integrating them into nitride device fabrication processes are the major obstacles to be overcome.

Hereby MISHFET devices on AlGaN/GaN structure were fabricated and characterized. Various gate dielectrics including SiO_2, Si_3N_4, ZrO_2 and Pb(Zr, Ti)O_3 (PZT) were tested, deposited by PECVD, MBE, and sputtering system respectively. For SiO_2 or Si_3N_4 gate dielectrics, their thicknesses are usually around 2~5 nm, which could be deposited at relatively low temperature after source/drain metallization. The short deposition time, low deposition temperature and low density plasma will not degrade the Ohmic contacts on the devices. On the other hand, the deposition of high-κ dielectric materials such as ZrO_2 and PZT requires active oxygen plasma source and much higher growth temperatures (~600 ºC), which can ruin the devices by quickly oxidizing the Ohmic contacts. To address this problem, we proposed and optimized the fabrication procedure shown in Figure 3. 21. Prior to the dielectric growth, a thick (~200 nm) amorphous SiO_2 layer was selectively deposited on the top of source and drain contacts by e-beam evaporation. This oxide layer can protect the metal contact during the insulator deposition. The 3 nm SiO_2 and Si_3N_4 were deposited by plasma enhanced chemical vapor deposition (PECVD) at 300ºC; the 2 nm ZrO_2 was grown by MBE; the 50 nm PZT was grown in RF magnetron sputtering system. The growth details can be found in ref. 87, 88, 89. Then, the samples were re-patterned so that the channel area was covered by photo resist, and dry etched in CF_4 plasma to remove the SiO_2 protection layer. After cleaning, at last gate pattern was defined and a Ni/Au (30/50 nm) gate was deposited.

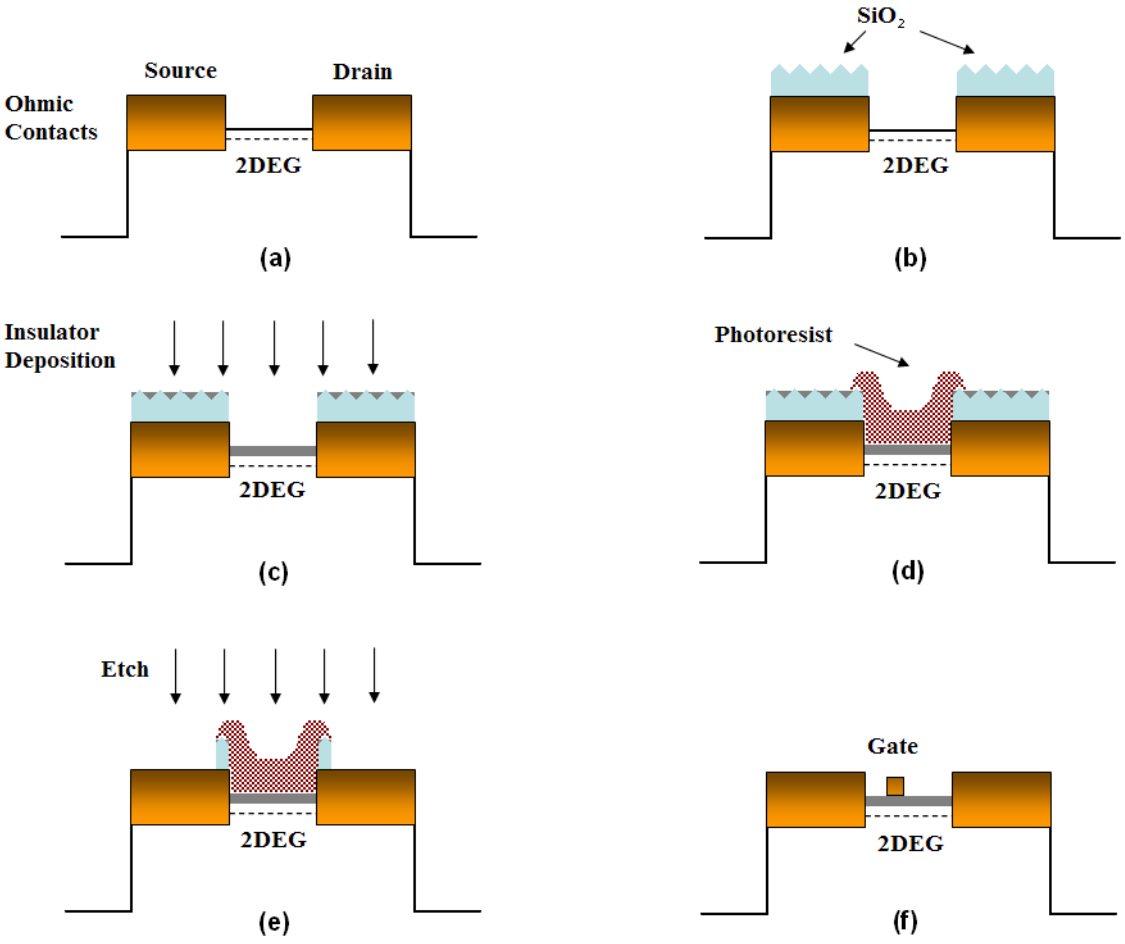
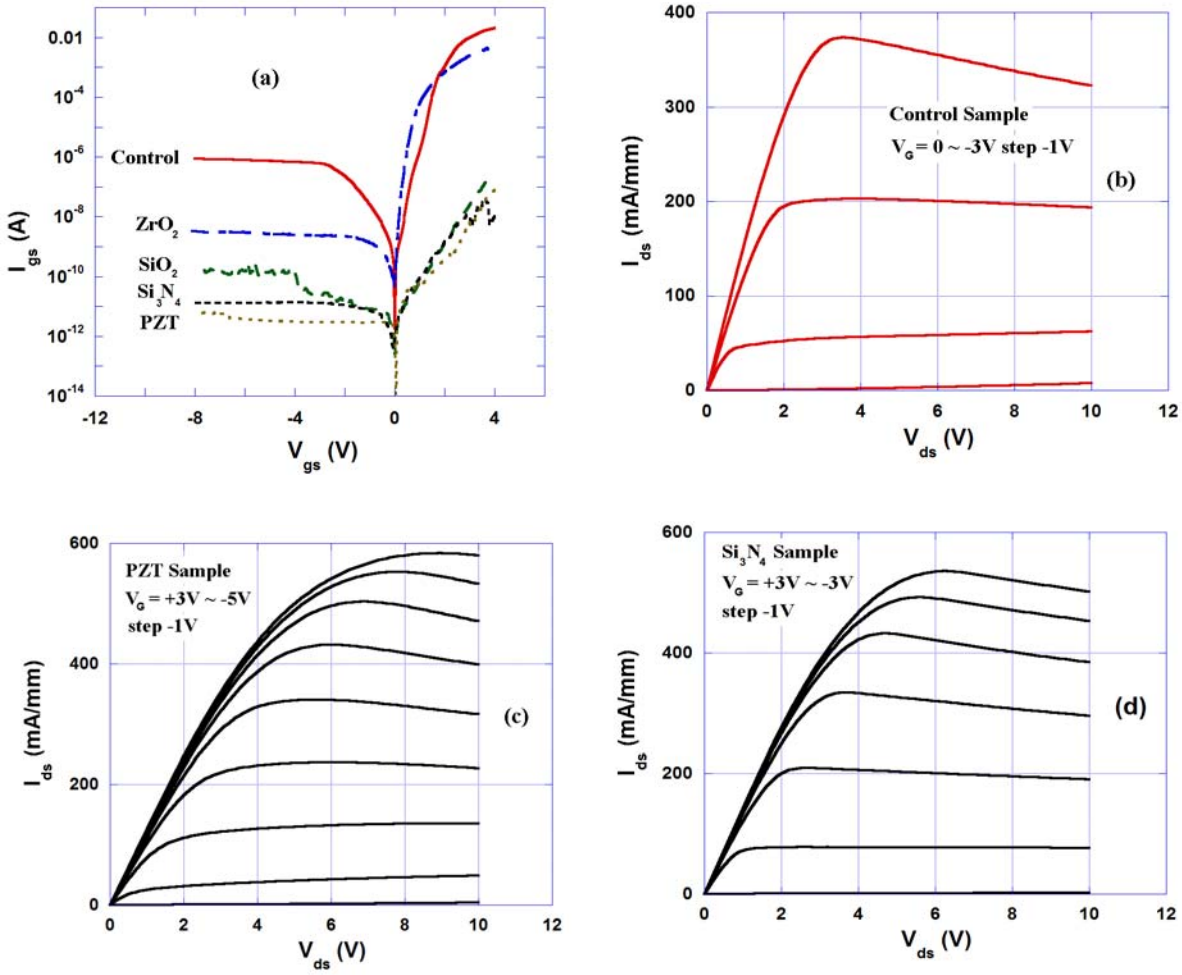


Figure 3. 21 Fabrication procedures for MISHFET.

As examined by the TLM measurements, the Ohmic contact property does not degrade after the insulator deposition – the average Ohmic contact resistance before and after this fabrication processes remained the same at about 3 Ω·mm. Therefore, it proved that the SiO_2 protection layer works effectively. Also, a test sample that followed these procedures but removed the gate dielectric before gate metallization showed the same saturation current and pinch-off voltage, compared with conventional fabricated HFET control sample, so the deposition of gate insulator does not damage the channel notably.

Figure 3. 22 shows the typical I-V and gate leakage current characteristics on all control

and MISHFET samples at room temperature. The data are all from devices with gate length/width of 2/40 μm and source-drain spacing of 6 μm. For the control sample, positive gate bias will induce significant leakage current that limits the input signal's dynamic range, while all MISHFETs shows orders of magnitude in decrease of leakage current. Si_3N_4 and PZT samples show similar leakage current range as low as 10 pA at -8 V gate bias, but it is worth mentioning that the uniformity of Si_3N_4 sample is better than PZT sample, showing a higher crystal quality achieved by the PECVD system.



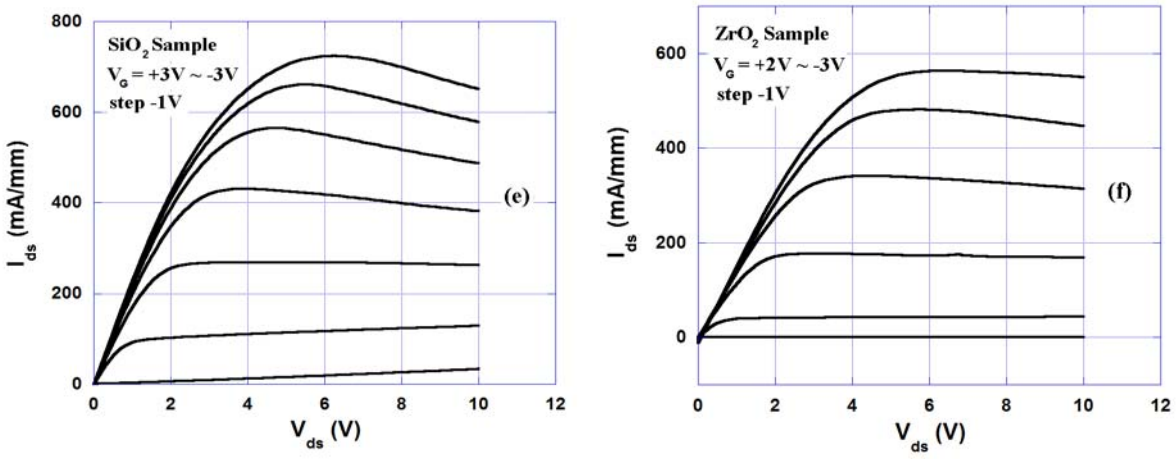


Figure 3. 22 Typical leakage current and IV characteristics on control and different MISHFET.

The reference sample shows good pinch-off and saturation properties. The reduction of the drain-source current is due to the self-heating. All MISHFETs can be applied up to +5 V gate bias without notable leakage current except the ZrO_2 sample. Under +3 V gate bias, the maximum current level can be enhanced, with the best reaching 700 mA/mm on the SiO_2 sample. Compared with the control sample, some of the MISHFETs also show higher saturation current at the zero bias, probably because of the passivation effect. No increase, except the PZT sample, in pinch-off voltage is observed for the MISHFET due to the use of very thin dielectrics layers. Under the fix drain bias (+3V), the dependence of drain-source current on the gate bias and the transconductance properties of all FETs are shown in Figure 3. 23. It is found that the thin Si_3N_4 and ZrO_2 gate dielectrics samples have a slightly reduction in transconductance, while the threshold voltage is unaffected as compared with control sample. The SiO_2 gate dielectric improves both the transconductance and the saturation current by around 10~15 %, probably caused by the effectively removing of surface states. On the other hand, transconductance drops

from 170 mS/mm to 120 mS/mm on PZT sample, which is considered as the result of the larger separation between the gate and the 2DEG channel with the presence of dielectrics. However, considering that the thickness of PZT is much larger than the other insulators, the decrease in transconductance is less significant due to the high- κ nature of PZT.

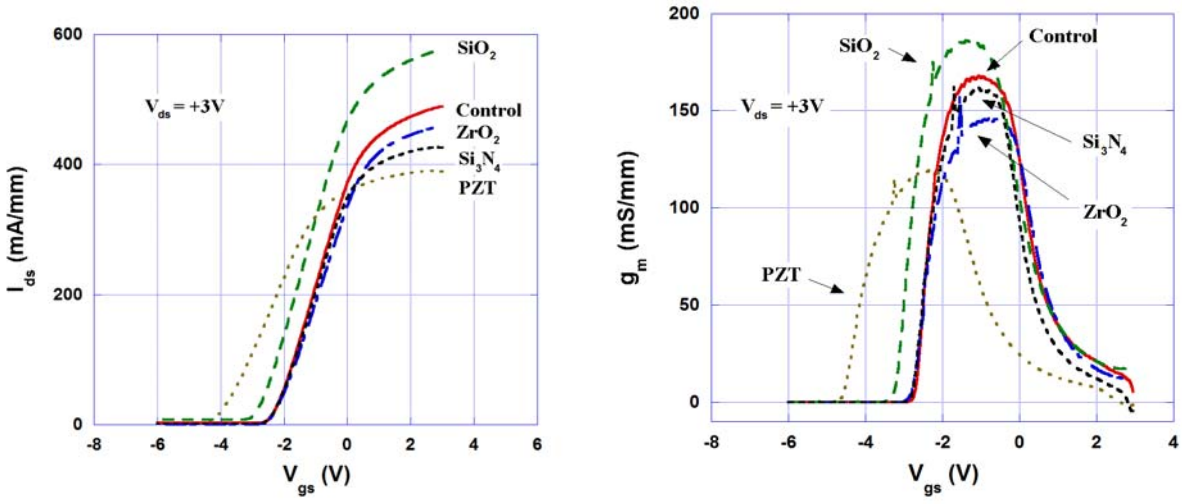


Figure 3. 23 Drain current and transconductance at V_{DS} = 3V on control and all MISHFETs

Figure 3. 24 (a) shows the C-V measurements at 1 MHz on control and MISHFET samples with the same dimension. A sharp transition could be observed at the threshold voltage consistent with the values obtained from I-V measurements. For MISHFET, at the 2DEG accumulation stage, the total capacitance can be expressed as:

$$C_{total}^{-1} = C_{FET}^{-1} + C_{insulator}^{-1}$$

Equation 3. 3

Under the zero gate bias condition, the thickness of insulators and the total capacitance are related by:

$$\frac{C_{HFET}}{C_{MISHFET}} = 1 + \frac{d_{Insulator}}{d_{AlGaN}} \cdot \frac{\varepsilon_{AlGaN}}{\varepsilon_{Insulator}}$$

Equation 3. 4

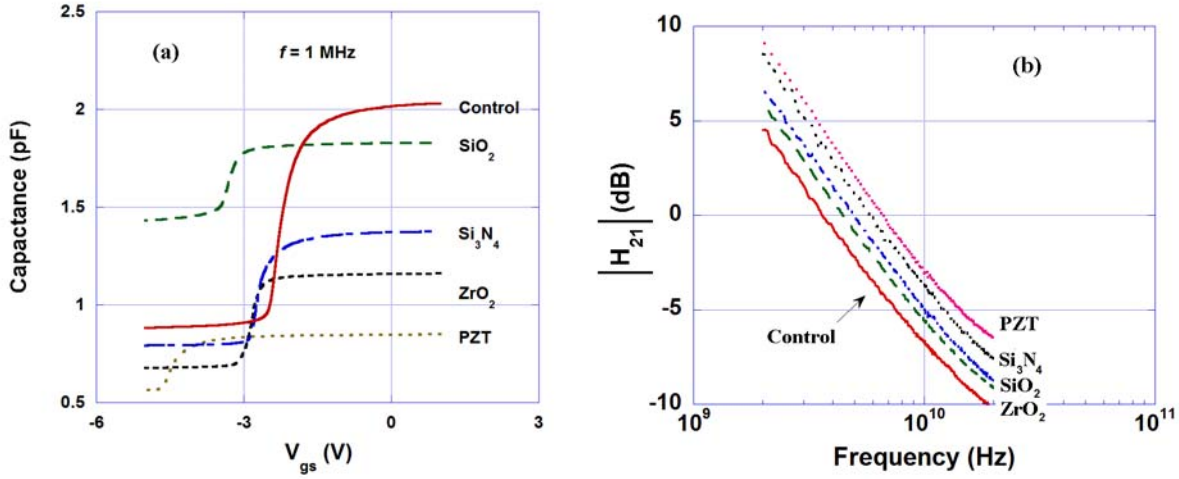


Figure 3. 24 (a) C-V measurements at 1 MHz; (b) current cut-off frequency obtained from RF S-parameter measured at 2GHz ~ 20 GHz.

Given the values of dielectric constants, the thickness of each gate insulator can be calculated, and we assume the constant for PZT to be 200[90]. The calculated SiO_2 and Si_3N_4 thicknesses agrees with experimental data, while the calculated PZT and ZrO_2 thicknesses are much larger. This may be accounted by the reduction of the actual dielectric constant, due to the different crystallization conditions of those high- κ materials on GaN.

The on-wafer RF measurements were also performed to determine the cut-off frequency (f_T) of those MISHFETs. The drain bias was set around 6~7 V and gate bias used 2~3 V on different samples. As seen from Figure 3. 24 (b), f_T of all MISHFETs are enhanced with the highest one achieved by PZT sample. Notice that the transconductance of PZT sample is lower, therefore the gate capacitance of it needs to be even smaller to increase f_T, which is consistently observed from C-V data shown in Figure 3. 24 (a).

Chapter 4 Small Signal Modeling

4.1 Equivalent circuit for GaN HFET

Modeling to the HFET is essential from the engineering point of view, not only because it can provide an accurate prediction on the circuit performance under the operating conditions, but also it facilitates the design and integration routines in conjunction with microwave applications such as amplifiers, mixers, oscillators or filters that are widely used in burgeoning communication systems. In general, the various modeling methods fall into two categories: physical and empirical models. The traditional empirical device modeling methods are based on the equivalent-circuit description to the transistors, and the determination of the each discrete circuit elements.

The transistor is first properly DC biased so that the device is working at a quiescent point (Q-point) at which the V_{DS} determines the saturated output current, and V_{GS} is well away from the pinch-off value that determines the depletion width and channel resistances. If the input signal is small, then it will not affect the Q-point of the device. A small input voltage will produce approximately a linear response in the drain-source current. As well, the equivalent circuit has linear response in the frequency domain without higher orders of harmonics. The output of the device has same frequency components as the input signal, only the phase and amplitude of the signal might be different.

Standard small signal extraction methods have been well-established for GaAs HFETs or SiC MESFETs[91, 92]. Basically, the equivalent circuit can be divided into the intrinsic part, for which the value of each element is a function of bias, and the extrinsic part that has no dependence on the bias instead. Usually each element is obtained by fitting the scattering

parameters measured directly from the device. The determination of the equivalent circuit always requires accurate S-parameter measurements, so that the extracted values can have physical significance. The basic procedure is to conduct "cold" measurements under channel pinch-off bias conditions (V_{DS} = 0V, $V_{GS} \leq 0$), at which the intrinsic circuit part can be simplified, to extract the bias-independent extrinsic parameters such as parasitic resistances or capacitances.

Similar extraction methods have been tested on GaN HFET[93, 94]. The circuit model is often more complicated than others because of the unique behavior from GaN devices such as the gate leakage current, self-heating, or defect-induced dispersion effects[95, 96]. The most comprehensive model for GaN HFET was proposed by Jamdal and Kompa [97] and consists of 22 distributed elements, which is reliable, general, and applicable for large signal construction, as shown in Figure 4. 1. As a three-terminal device, the extrinsic circuit for the HFET must include three parasitic resistances and inductances associated with each contact and wire connection. In principle, these elements should be as small as possible, although for wide band gap semiconductor, the obtaining on good Ohmic contact is still a technical difficulty.

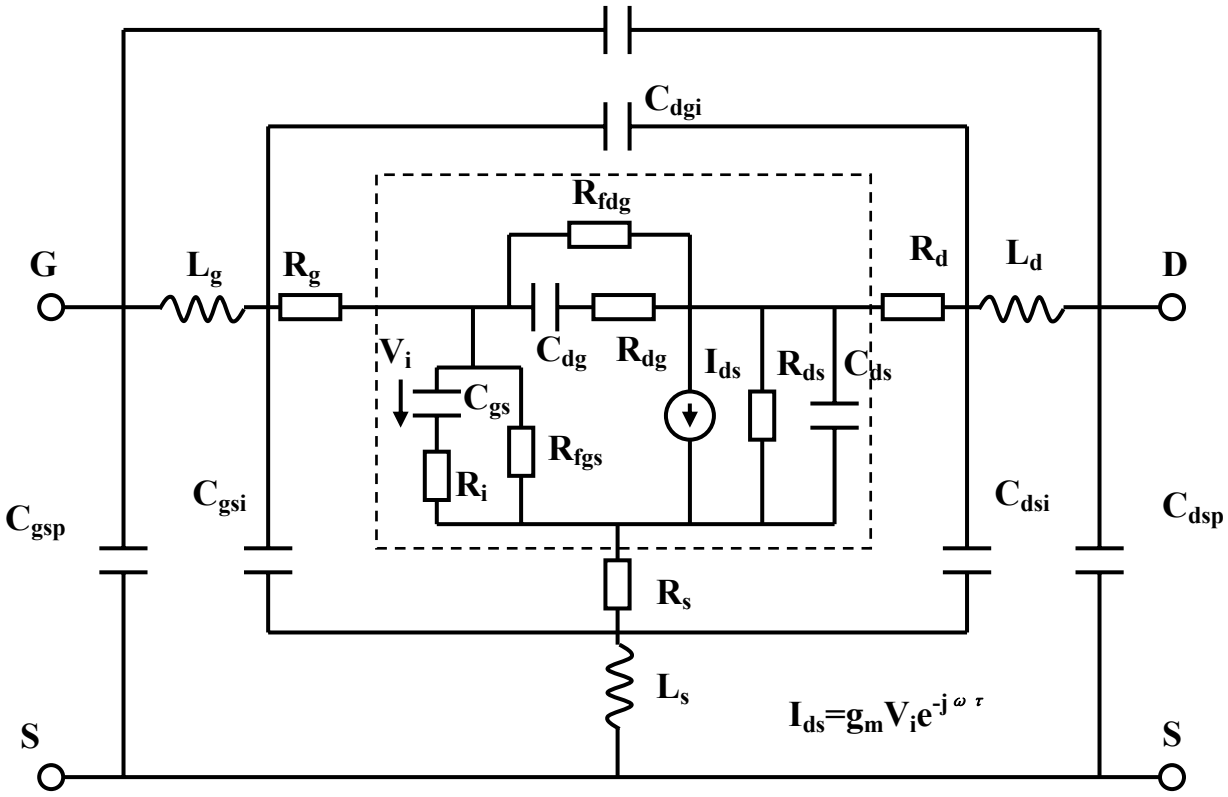


Figure 4. 1 A 22-element equivalent circuit model for GaN HFET from ref. 97.

Regarding the extrinsic capacitances, C_{gsp}, C_{dgp} and C_{dsp} represent the parasitic capacitances introduced by the pad connection and probe contacts, and C_{gsi}, C_{dgi} and C_{dsi} account for the interelectrode capacitances. They are all considered in ref. 97, while the de-embedding procedure (an optimization-based routine) requires the initial values estimated from empirical assumptions. To reduce the complexity of the modeling procedure, the inter-electrode capacitances are often neglected by many reports[98, 99], since these values are always relatively small. In our effort, we propose an equivalent circuit for the GaN HFET shown in Figure 4. 2, in which the C_{dgp} is also neglected in favor of the extraction simplicity.

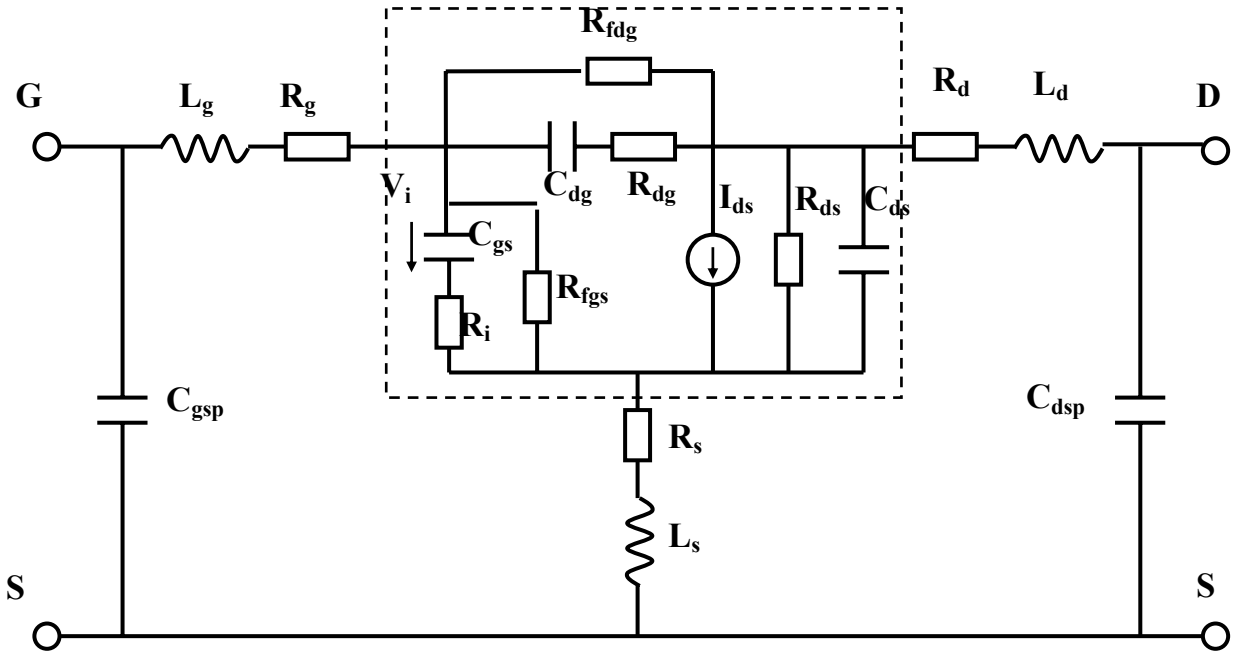


Figure 4. 2 The proposed 18-elements small signal equivalent circuit for GaN HFET, within the dashed box is the intrinsic part.

For the intrinsic circuit part in this model, the consistency between GaN HFET and GaAs or SiC power transistors is obvious. The traditional model often consists of 8 elements with explicit physical significance. But for GaN HFET, the scenario is little more complicated. The differential resistances introduced in ref. 99, R_{fdg} and R_{fgs}, are necessary for characterizing the current conduction through the gate diode. Reference 98 even considered the possible existence of time delays in the output conductance element (R_{ds}). The adding of more elements into the intrinsic circuit, however, will give an over-determined system of equations. Hereby we choose a 10-element intrinsic circuit model similar to ref. 97, which is believed to have enough accuracy and applicable for large signal analysis as well.

4.2 Circuit parameters extraction methodology

The key for the small signal de-embedding methodology is the determination of extrinsic circuit elements, because it is easier for the intrinsic part with the analytical expressions available. Once the extrinsic elements are successfully extracted, by fitting through the *y*-parameters of a two terminal network, one can easily extract the value of intrinsic elements. Taken the equivalent circuit proposed in Figure 4. 2 for example, the *y*-matrix of the intrinsic part can be written as:

$$y_{\text{int}} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} \left(j\omega C_{gs} \left\| R_i^{-1}\right.\right) + \left(j\omega C_{dg} \left\| R_{gd}^{-1}\right.\right) + R_{fdg}^{-1} + R_{fgs}^{-1} & -\left(j\omega C_{gd} \left\| R_{dg}^{-1}\right.\right) - R_{fdg}^{-1} \\ \dfrac{g_m e^{-j\omega\tau}}{1 + j\omega C_{gs} R_i} - \left(j\omega C_{dg} \left\| R_{dg}^{-1}\right.\right) - R_{fdg}^{-1} & R_{ds}^{-1} + R_{fdg}^{-1} + j\omega C_{ds} + \left(j\omega C_{gd} \left\| R_{dg}^{-1}\right.\right) \end{bmatrix}$$

with $A \| B = \dfrac{A \cdot B}{A + B}$

Equation 4. 1

At low frequencies (in the megahertz range), the capacitance terms in y_{11} and y_{12} of Equation 4. 1 approach zero so that R_{fgs} and R_{fdg} can be easily determined at this condition:

$$R_{fdg}^{-1} = g_{fdg} \approx -\text{Re}(y_{12}) \text{ and } R_{fgs}^{-1} = g_{fgs} \approx \text{Re}(y_{12} + y_{11})$$

Equation 4. 2

Then the real and imaginary parts of Equation 4. 1 can be equated to obtain the rest 8 intrinsic elements:

$$C_{dg} = -\frac{\text{Im}(y_{12})}{\omega}\left[1 + \left(\frac{\text{Re}(y_{12}) + R_{fdg}^{-1}}{\text{Im}(y_{12})}\right)^2\right]$$

Equation 4. 3

$$R_{dg} = \frac{\mathrm{Re}\left(y_{12}\right) + R_{fdg}^{-1}}{\omega C_{dg}\,\mathrm{Im}\left(y_{12}\right)}$$

Equation 4. 4

$$C_{gs} = \frac{\mathrm{Im}\left(y_{11}\right) + \mathrm{Im}\left(y_{12}\right)}{\omega}\left\{\left[1 + \frac{\left[\mathrm{Re}\left(y_{11}\right) + \mathrm{Re}\left(y_{12}\right) - R_{gfs}^{-1}\right]^2}{\left[\mathrm{Im}\left(y_{11}\right) + \mathrm{Im}\left(y_{12}\right)\right]^2}\right]\right\}$$

Equation 4. 5

$$R_i = \frac{\mathrm{Re}\left(y_{11}\right) + \mathrm{Re}\left(y_{12}\right) - R_{fgs}^{-1}}{\omega C_{gs}\left[\mathrm{Im}\left(y_{11}\right) + \mathrm{Im}\left(y_{12}\right)\right]}$$

Equation 4. 6

$$g_m = \sqrt{\left\{\left[\mathrm{Re}\left(y_{21}\right) - \mathrm{Re}\left(y_{12}\right)\right]^2 + \left[\mathrm{Im}\left(y_{21}\right) - \mathrm{Im}\left(y_{12}\right)\right]^2\right\}\left(1 + \omega^2 C_{gs}^2 R_i^2\right)}$$

Equation 4. 7

$$\tau = \omega^{-1}\arcsin\left[\frac{\mathrm{Im}\left(y_{12}\right) - \mathrm{Im}\left(y_{21}\right) - \omega C_{gs} R_i\left[\mathrm{Re}\left(y_{21}\right) - \mathrm{Re}\left(y_{12}\right)\right]}{g_m}\right]$$

Equation 4. 8

$$C_{ds} = \left[\frac{\mathrm{Im}\left(y_{22}\right) + \mathrm{Im}\left(y_{12}\right)}{\omega}\right]$$

Equation 4. 9

$$R_{ds}^{-1} = \mathrm{Re}\left(y_{22}\right) + \mathrm{Re}\left(y_{12}\right)$$

Equation 4. 10

Therefore, the problem is reduced to the determination for the intrinsic *y* parameters, which depends on the extraction of extrinsic parameters. To ensure one can get unique and

representative solution set, namely the extrinsic elements are bias-independent and intrinsic elements are frequency independent, many types of measurements are made to attain as much confidence as possible.

The extrinsic elements could be determined through either measurement-based methods or optimization-based methods. The former is more prevalent and utilizes the *S*-parameter measurement measured in the cold conditions, or in another word, under 0V drain-source bias conditions. In the following sections we will examine many different extraction methods applying to our AlGaN/GaN devices.

4.3 Cold-FET methods

The cold-FET methods that determine the parasitics always include two sets of measurements conducted at different frequency ranges. In the low frequency range, the influence from the inductances can be neglected. Meanwhile, the device is biased under a pinched-off condition (V_{DS} = 0, V_{GS} <<0), so very small current is conducting through the device. Therefore, the channel conductivity is negligible and the *S*-parameters measure exhibit capacitive properties. At the high frequency range, the impedance of the circuit is dominated by the inductances. Also the device is biased under a strongly forward gate bias condition (V_{DS} = 0, V_{GS} >>0), in order to reduce the channel depletion capacitance to a large extent. Thus the parasitic resistances and inductances are easily calculated. The following are the detailed experimenting methodologies.

4.3.1 Determination of extrinsic capacitances

Under the pinch-off cold-FET conditions, the equivalent circuit for the circuit model in Figure 4. 2 can be reduced as shown in the inset to Figure 4. 3 if considering only the imaginary part of the *y*-parameters[92]. For our AlGaN barrier HFET sample, the device is biased under V_{DS}

= 0 V, V_{GS} = -7 V, and the RF measurements are performed in the frequencies ranging from 150 MHz to 1.0 GHz.

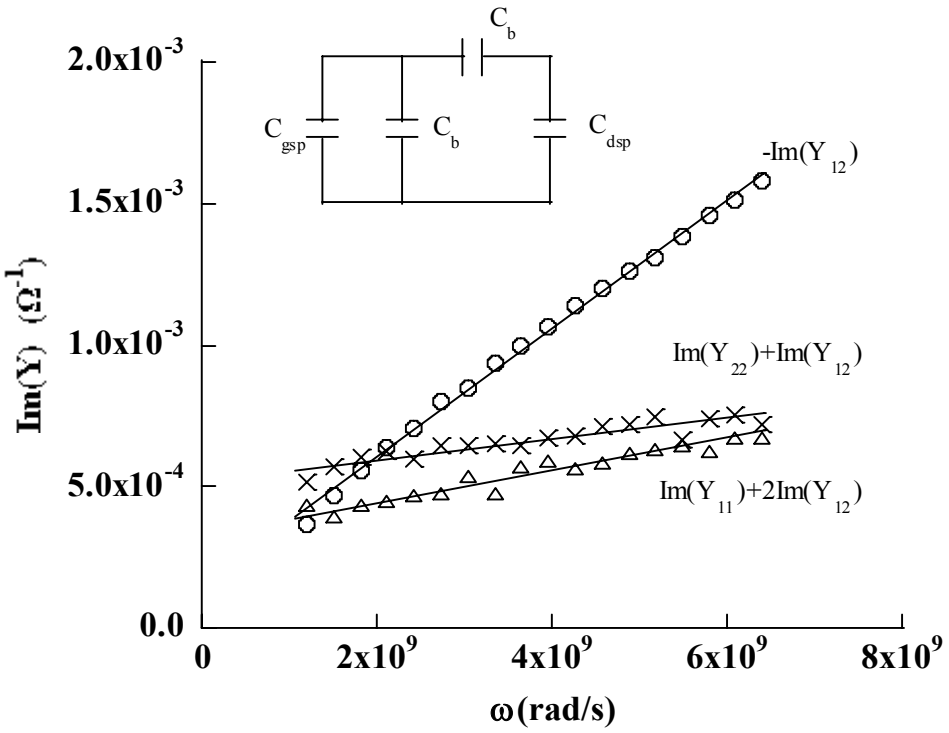


Figure 4. 3 Reduced equivalent circuit for pinch-off Cold-FET condition, and the parasitic pad capacitances determined by linear regression at V_{DS} = 0 V, V_{GS} = -7 V, frequencies from 150 MHz to 1.0 GHz.

With the assumption that the gate depletion region is symmetric at the pinch-off condition, it quickly leads to the following relationships:

$$\mathrm{Im}(Y_{11}) = \omega(C_{gsp} + 2 \cdot C_b)$$

Equation 4. 11

$$\mathrm{Im}(Y_{12}) = -\omega C_b$$

Equation 4. 12

$$\mathrm{Im}(Y_{22}) = \omega(C_{dsp} + C_b)$$

Equation 4. 13

Here C_b is the residual coupling capacitance between the gate and the source and drain regions.

By linearly fitting the imaginary part of the *y*-parameters over this frequency range, shown in Figure 4. 3 for a typical device, we can extract the pad capacitances as: C_{gsp} = 0.069 pF; C_{dsp} = 0.062 pF.

Pad capacitances extracted from a typical device under different bias conditions are also tested and listed in Table 4. 1. Higher applied biases result in stable, settled values of these parasitics. As suggested also in ref. 100, high gate bias is desired to suppress differential resistance and obtain the accurate parasitics. But high gate bias may also introduce surface state-assisted tunneling current flow and subsequent gate breakdown problems, which, as we observed, fail to produce reliable capacitances value on some devices.

Gate Bias (V)	C_{gsp} (pF)	C_{dsp} (pF)
-5	0.095	0.102
-6	0.081	0.054
-7	0.069	0.062
-8	0.063	0.061
-9	0.067	0.057

Table 4. 1 The extracted pad capacitances under different pinch-off bias.

4.3.2 Determination of extrinsic resistances and inductances

The inductances and resistances are determined under strong forward gate biased cold

condition, at which the *z*-parameters for the remaining circuits with parasitic capacitances removed should exhibit inductive properties[92]. However, it has been pointed out by many groups that this bias condition may not be applicable to the inductance extraction on the GaN HFET[101]. The forward gate bias conditions for GaN devices may easily cause damages to the channel, and the results that after could differ from the ones under the normal operating conditions. The more prevalent methods for GaN HFET in extracting these inductances and resistances are often conducted at zero or small negative gate bias conditions[97] (V_{DS} = 0, V_{GS} ~0). After removing the measured pad capacitances, the corresponding equivalent circuit is shown in Figure 4. 4.

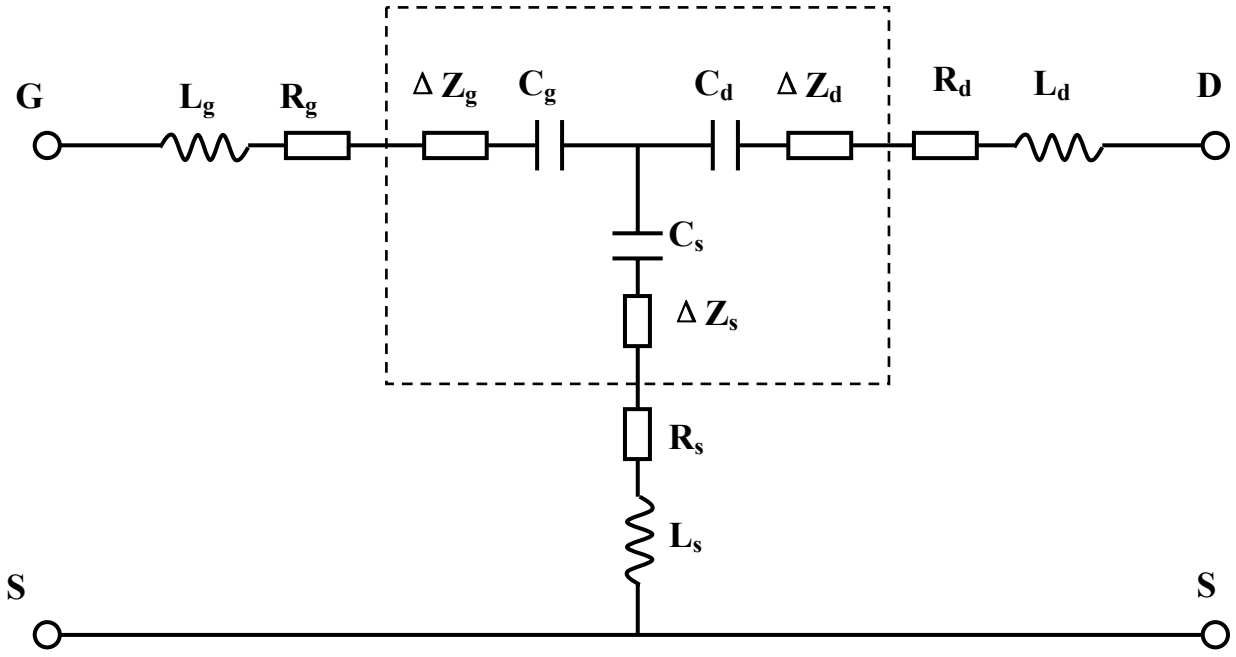


Figure 4. 4 Reduced equivalent circuit for the determination of parasitic inductances and resistances at V_{DS} = 0, V_{GS} ~0 bias condition, after removing the pad capacitances.

Here the residual intrinsic impedance terms (ΔZ_i) in Figure 4. 4 are always treated as channel resistances. The applicable *z*-parameters can be expressed in terms of parasitic resistances and inductances:

$$z_{11} = R_g + R_s + j\omega(L_g + L_s) + \frac{1}{j\omega}(C_g^{-1} + C_s^{-1}) + \delta Z_g$$

Equation 4. 14

$$z_{22} = R_d + R_s + j\omega(L_d + L_s) + \frac{1}{j\omega}(C_d^{-1} + C_s^{-1}) + \delta Z_d$$

Equation 4. 15

$$z_{12} = z_{21} = R_s + j\omega L_s + \frac{1}{j\omega C_s} + \delta Z_s$$

Equation 4. 16

In this manner, the residual terms show no influence on the imaginary part of the *z*-parameters, from which the parasitic inductances are determined by linearly fitting $\mathrm{Im}(\omega Z_{ij})$ over ω^2:

$$\mathrm{Im}(\omega z_{11}) = \omega^2(L_g + L_s) - \left(\frac{1}{C_g} + \frac{1}{C_s}\right)$$

Equation 4. 17

$$\mathrm{Im}(\omega z_{22}) = \omega^2(L_d + L_s) - \left(\frac{1}{C_d} + \frac{1}{C_s}\right)$$

Equation 4. 18

$$\mathrm{Im}(\omega z_{12}) = \omega^2 L_s - \frac{1}{C_s}$$

Equation 4. 19

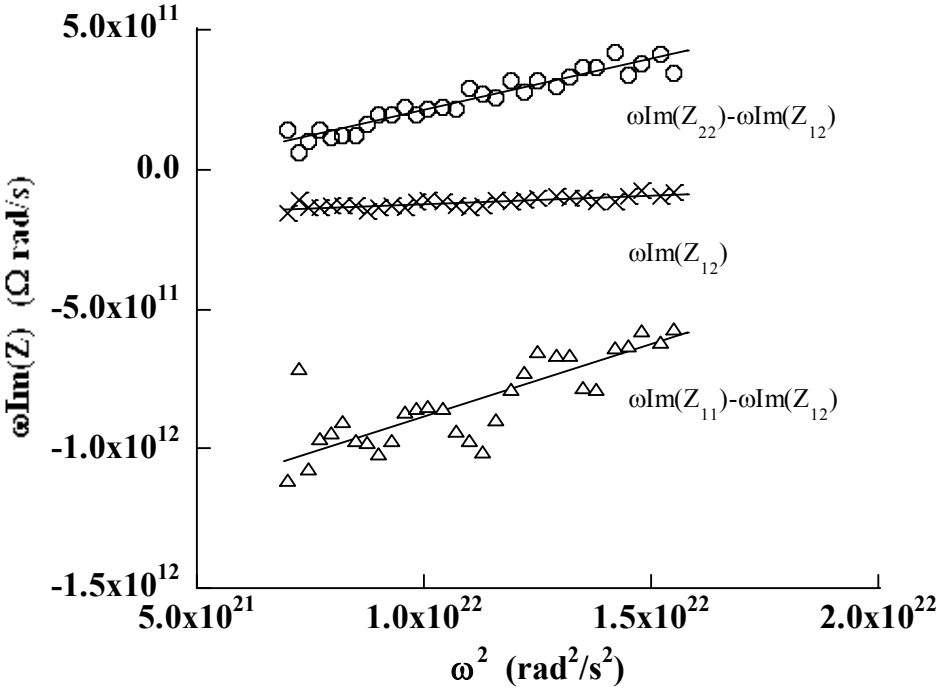


Figure 4. 5 Parasitic inductances determined from cold measurement at V_{DS} = 0 V, V_{GS} = 0 V, at frequencies from 10 GHz to 20 GHz.

On the devices from which we extracted pad capacitances, we calculated parasitic inductances from *z*-parameters measured at V_{DS} = 0 V, V_{GS} = 0 V conditions. The data were collected over the high frequency range from 10 GHz to 20 GHz to minimize the error from residual capacitive terms. Figure 4. 5 shows the linear fit of $\omega\mathrm{Im}(Z)$ vs. ω^2, and the parasitic inductances are determined as L_s = 6.82pH, L_d = 36.99pH, L_g = 52.19pH.

The extraction of parasitic resistances, on the other hand, depends on ΔZ_i which is expressed in various ways in different reports. For example, from zero to low negative gate bias range described in ref. 97, it follows:

$$\mathrm{Re}(Z_{11}) = R_s + R_g$$

Equation 4. 20

$$\mathrm{Re}(Z_{12}) = R_s + R_{ch}/2$$

Equation 4. 21

$$\mathrm{Re}(Z_{22}) = R_s + R_d + R_{ch}$$

Equation 4. 22

In order to determine four unknowns out of three equations, various bias points need to be measured to interpolate R_s+R_d. But we could not obtain reliable consistency in the extracted resistances under multiple bias conditions, which was beautifully done in ref. 93. Hereby, we neglected the channel resistance at zero gate bias condition, as suggested in ref. 97, making the determination of parasitic resistances much easier. Here we extract the parasitic resistances by multiplying with ω to further eliminate the influence from the residual terms.

$$\omega(R_g + R_s) = \omega\,\mathrm{Re}(z_{11})$$

Equation 4. 23

$$\omega(R_d + R_s) = \omega\,\mathrm{Re}(z_{22})$$

Equation 4. 24

$$\omega R_s = \omega\,\mathrm{Re}(z_{12})$$

Equation 4. 25

As seen in Figure 4. 6, we can linearly fit the data and obtain the parasitic resistances from the slope, the corresponding results are: R_s = 4.45Ω, R_d = 5.47Ω, R_g = 3.69Ω.

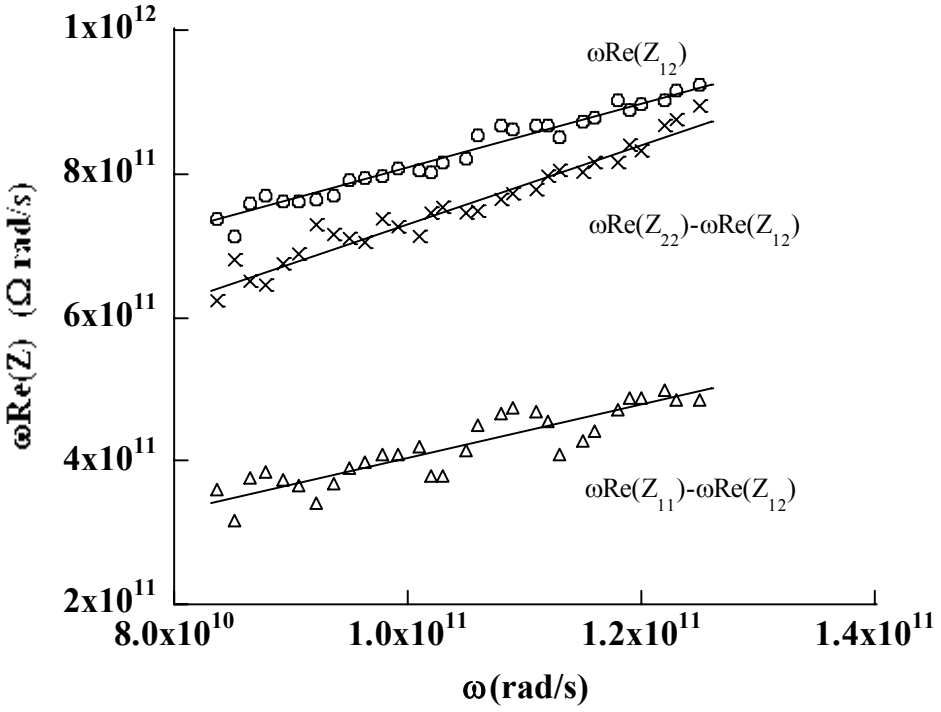


Figure 4. 6 Parasitic resistances determined for the same device under the same bias condition.

From Figure 4. 6, the curve fittings for gate parasitics show larger variation compared with that of source and drain. They are also more sensitive to the frequency range where the fitting is done, similar to what was observed in 102. This cold measurement method gives more accuracy and confidence on source and drain parasitic resistances and inductances than those of the gate.

4.3.3 Fitting on the intrinsic parameters

Once the extrinsic parameters are predetermined, the intrinsic parameters can be calculated by Equation 4. 2 to Equation 4. 10. Similarly some equations are multiplied by ω to make the linear fitting easier. The differential resistances are determined in the frequency 200

MHz to 1 GHz. Some of the parameter fittings are shown in Figure 4. 7.

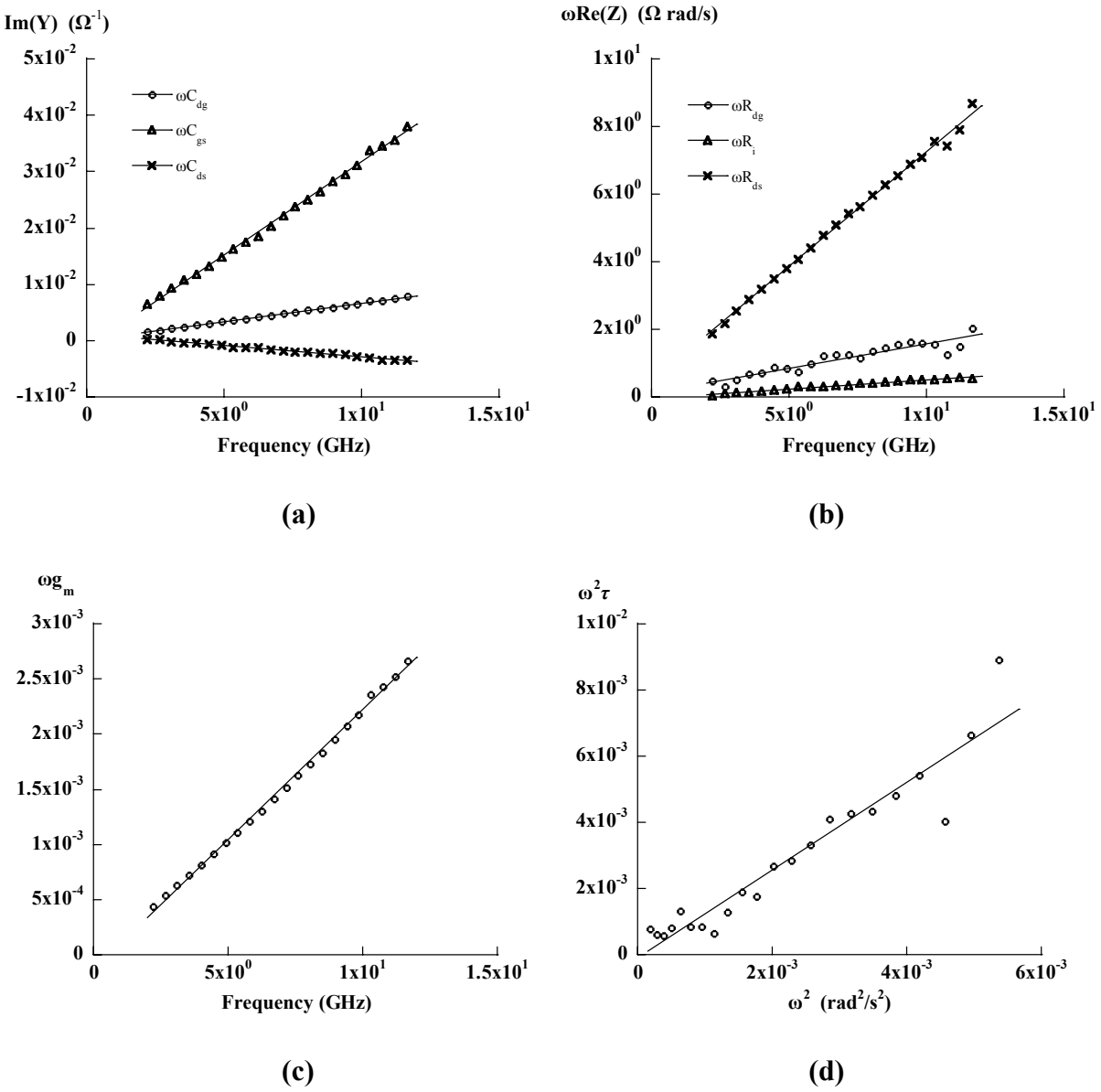


Figure 4. 7 The linear fittings on the intrinsic parameters (a) C_{dg}, C_{gs} and C_{ds}; (b) R_{dg}, R_i and R_{ds}; (c) gm; (d) τ.

The calculated intrinsic parameters for the same device are listed in Table 4. 2, where ΔS refers to the average error between calculated and measured S-parameters over the whole frequency range. The bias condition for intrinsic parameters extraction is V_{DS} = 4 V, V_{GS} = -3 V. For some parameters, such as C_{ds}, the slope of the linear fitting is negative then the value is set to

be zero.

R_s (Ω)	4.45	L_s (pH)	6.82
R_d (Ω)	5.47	L_d (pH)	36.99
R_g (Ω)	3.69	L_g (pH)	52.19
C_{gsp}(fF)	69.0	R_{fgs} (kΩ)	0.91
C_{dsp}(fF)	62.0	R_{fdg} (kΩ)	6.84
C_{gs} (fF)	571.06	R_i (Ω)	8.62
C_{ds} (fF)	0.00	R_{ds} (Ω)	153.33
C_{dg} (fF)	76.44	R_{dg} (Ω)	23.02
g_m (mS)	41.57	ΔS	9.82%
τ (ps)	1.38		

Table 4. 2 The extracted extrinsic parameters from cold-FET measurements, and intrinsic parameters from determined S-parameters measured at V_{DS} = 4 V, V_{GS} = -3 V.

4.4 Hot-FET methods

The determination of parasitic circuit elements, as we can see, is fundamental in the whole de-embedding procedure. Instead of cold-FET measurements, there are many other optimization-based extraction methods that attempt to find out the parasitic parameters only at the biased conditions (hot-FET methods), because of speculations on the dependence of the parasitics on bias[103]. Especially for the access resistances, they have been reported to be more critical in GaN HFET than in other material systems[101]. Also, the relatively slow trapping and thus the associated dispersion effects could substantially be affected by the bias conditions according to pulsed I-V measurements, and in turn trapping can also affect the effective bias

conditions. Therefore, it stands to reason that these values are bias-dependent. Hereby we will examine two hot-FET extraction methods proposed by Manohar et al. and Shirakawa et al. in ref. 104 and 105. The first method is analytic-based, while the second is optimization-based.

4.4.1 Analytical method

The analytical expressions can be derived if the circuit model contains less components and simpler. One of such method was developed in ref. 104 for SiC MESFETs. The equivalent circuit used by this method is shown in Figure 4. 8.

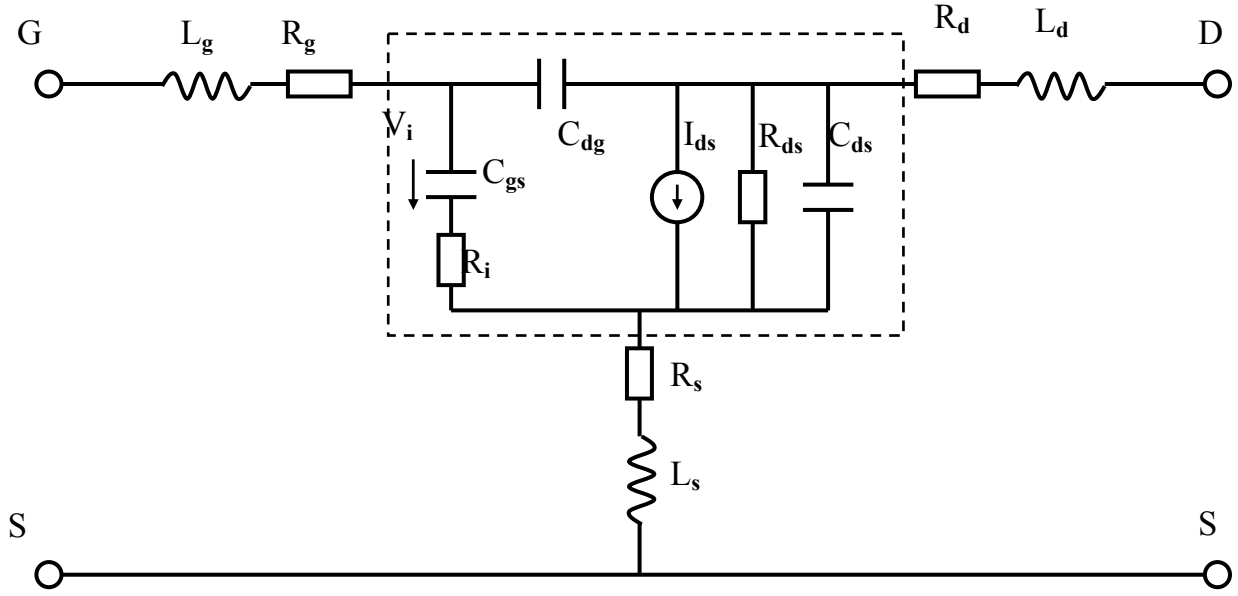


Figure 4. 8 Circuit model after parasitic capacitances de-embedded for analytical extraction method proposed in 104.

Assuming the pad capacitances are known and de-embedded, the parasitic resistances and inductances can then be correlated with the *z*- parameters of the rest circuit. Taking the source pad for example, it has the following relationship:

$$\frac{\mathrm{Im}(z_{12})}{\omega} = \frac{C_{gd}}{g_m} X_1 + L_S$$

Equation 4. 26

$$\mathrm{Re}(z_{12}) = \frac{C_{gd}}{g_m} X_2 + R_S$$

Equation 4. 27

with

$$X_1 = \sin(\omega\tau)[\mathrm{Im}(z_{21}) - \mathrm{Im}(z_{12})] + \cos(\omega\tau)[\mathrm{Re}(z_{12}) - \mathrm{Re}(z_{21})]$$

Equation 4. 28

$$X_2 = \omega\cos(\omega\tau)[\mathrm{Im}(z_{21}) - \mathrm{Im}(z_{12})] - \omega\sin(\omega\tau)[\mathrm{Re}(z_{12}) - \mathrm{Re}(z_{21})]$$

Equation 4. 29

Therefore by linearly fitting $\mathrm{Im}(z_{12})/\omega$ on X_1 and $\mathrm{Re}(z_{12})$ on X_2, the source R_s and L_s can be extracted by extrapolation. Once R_s and L_s are determined, the rest of the parasitic resistances and inductances can be extracted in a similar manner by fitting the real and imaginary part of the following equations:

$$\frac{z_{12} - Z_s}{z_{11} - Z_s - Z_g} = -\frac{y_{12}}{y_{22}}$$

Equation 4. 30

$$\frac{z_{12} - Z_s}{z_{22} - Z_s - Z_d} = -\frac{y_{12}}{y_{11}}$$

Equation 4. 31

Noting that the validity of Equation 4. 26 and Equation 4. 27 is based on the assumption

that $(\omega R_i C_{gs})^2 \sim 0$, the linear regression is better to be done under 5 GHz frequency. The transition time τ is initially set to be 1ps, and updated at each iteration. For example, the linear regression in determining the source resistance is illustrated in Figure 4. 9, from the data measured on the same device and conditions.

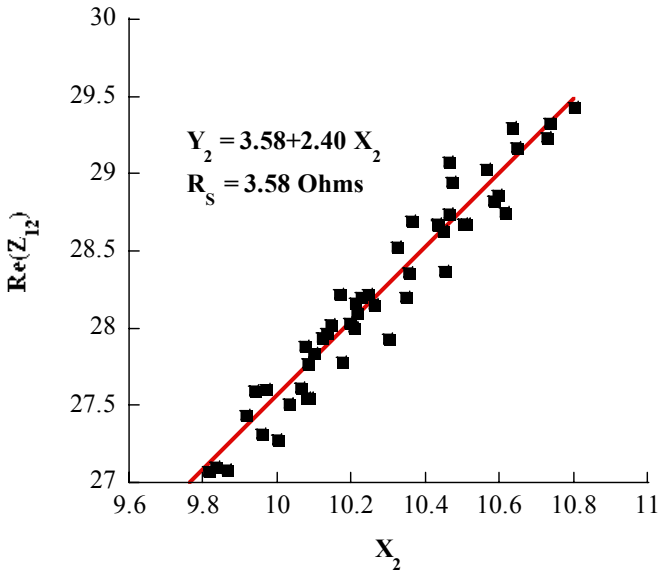


Figure 4. 9 The illustration of analytical method to determine source parasitic resistance.

The rest extrinsic parameters are fitted in the similar ways. After the de-embedding of extrinsic part, the intrinsic parameters are calculated consequently and listed in Table 4. 3. Here, some of the extracted parasitic resistances and inductances are comparable with the results from cold measurements. However, the parasitic inductances exhibit large variations and fit errors, from our observations. The calculated inductances vary significantly when different frequency ranges are used. Sometimes the parasitics obtained by this method are negative without any physical representations, even though careful calibrations and measurements were conducted.

Besides the possible reason that the pad parasitics may change at hot-FET conditions compared with cold-FET, the omission of the gate differential resistances (R_{fdg} and R_{fgs}) , especially when they are in the few kΩ range, may bring considerable error on to the analytical expressions Equation 4. 26 and Equation 4. 27.

R_s (Ω)	3.58	L_s (pH)	85.54
R_d (Ω)	6.12	L_d (pH)	216.72
R_g (Ω)	0.00	L_g (pH)	112.65
C_{gsp}(fF)	69.0		
C_{dsp}(fF)	62.0		
C_{gs} (fF)	415.90	R_i (Ω)	11.07
C_{ds} (fF)	0.98	R_{ds} (Ω)	215.33
C_{dg} (fF)	71.23		
g_m (mS)	28.84	ΔS	14.8%
τ (ps)	0.89		

Table 4. 3 The calculated circuit parameters with analytical method, directly from hot-FET measurements data.

4.4.2 Optimization method

Shirakawa *et al.* have proposed a simple small signal equivalent circuit model for the conventional GaAs HFET, same as what is shown in Figure 4. 8, along with a pure optimization method to extract extrinsic and intrinsic parameters simultaneously. Our optimization routine is based on their algorithm with some modifications so that it can work on the more complicated the equivalent circuit shown in Figure 4. 2.

Differential resistances, R_{fdg} and R_{fgs} should not be omitted for GaN HFET as in the Shirakawa model. However, the incorporation with extra elements will present some challenges in the complexity of the optimization as we will see later.

Still the pad parasitic capacitances, C_{gsp} and C_{dsp}, are considered using the value from cold measurements. After de-embedding the parasitic capacitances, the *z*-parameters for the total remaining circuit and intrinsic part are related by:

$$z_{\text{int}} = z_{total} - z_{ext} = \begin{bmatrix} z_{11} - (R_g + R_s) - j\omega(L_g + L_s) & z_{12} - R_s - j\omega L_s \\ z_{21} - R_s - j\omega L_s & z_{22} - (R_d + R_s) - j\omega(L_d + L_s) \end{bmatrix}$$

Equation 4. 32

where z_{ij} represents the *z*-parameter of the total device with the pad capacitances removed.

The basic idea of the optimization procedure is to express all of the intrinsic elements as functions of ω and an extrinsic vector, z_{ext} (R_d, R_g, R_s, L_d, L_g, L_s). By assuming that all intrinsic elements are frequency independent, through minimizing their variance over frequency we will obtain the optimized value for both the extrinsic and intrinsic parameters.

Given a specific value on z_{ext}, the intrinsic *z* or *y* parameters can be determined from the measured data. From Equation 4. 2 to Equation 4. 10, every the intrinsic parameters can be calculated except R_{fdg} and R_{fgs} , which are determined at low frequency range. Since the number of intrinsic parameters is 10, it is actually impossible to express all 10 variables solely as a function of single ω in light of the fact that there are only 4 measured pieces of data, including real and imaginary parts, at each frequency point. Our solution is to find expressions for each of the intrinsic circuit elements in terms of the intrinsic *y*-parameters at multiple frequency points. In another words, we chose a proper $\Delta\omega$ so that at each frequency ω, all elements are determined from both $y(\omega)$ and $y(\omega+\Delta\omega)$. Taking the R_{fgs}, R_i, C_{gs} sub-circuit as an example, the feedback

resistances and its corresponding RC sub-circuit will follow:

$$C_{gs} \cdot R_i = \frac{\mathrm{Re}[Y_1(\omega + \Delta\omega) - Y_1(\omega)]}{(\omega + \Delta\omega)\,\mathrm{Im}[Y_1(\omega + \Delta\omega)] - \omega\,\mathrm{Im}[Y_1(\omega)]}$$

Equation 4. 33

Moreover we can find out:

$$R_{fgs}^{-1} = \mathrm{Re}[Y_1(\omega)] - \omega \cdot \mathrm{Im}[Y_1(\omega)] \cdot (C_{gs} \cdot R_i)$$

Equation 4. 34

$$\omega C_{gs} = \mathrm{Im}[Y_1(\omega)] \cdot [1 + (\omega \cdot C_{gs} \cdot R_i)^2]$$

Equation 4. 35

where $Y_1 = y_{11,\mathrm{int}} + y_{12,\mathrm{int}}$. Similarly, the R_{fdg}, R_{dg}, C_{dg} sub-circuit follows:

$$C_{dg} \cdot R_{dg} = \frac{\mathrm{Re}[Y_2(\omega + \Delta\omega) - Y_2(\omega)]}{(\omega + \Delta\omega)\,\mathrm{Im}[Y_2(\omega + \Delta\omega)] - \omega\,\mathrm{Im}[Y_2(\omega)]}$$

Equation 4. 36

$$R_{fdg}^{-1} = \mathrm{Re}[Y_2(\omega)] - \omega \cdot \mathrm{Im}[Y_2(\omega)] \cdot (C_{dg} \cdot R_{dg})$$

Equation 4. 37

$$\omega C_{dg} = \mathrm{Im}[Y_2(\omega)] \cdot [1 + (\omega \cdot C_{dg} \cdot R_{dg})^2]$$

Equation 4. 38

where $Y_2 = -y_{12,\mathrm{int}}$. When programming, we also smoothed the calculated values by averaging them within several adjacent data points in order to reduce the scatter caused by the error from the measurement. The rest four intrinsic elements will be:

$$R_{ds}^{-1} = \mathrm{Re}(y_{22,\mathrm{int}} + y_{12,\mathrm{int}})$$

Equation 4. 39

$$\omega C_{ds} = \mathrm{Im}(y_{22,\mathrm{int}} + y_{12,\mathrm{int}})$$

Equation 4. 40

$$g_m = \left|(y_{21,\mathrm{int}} - y_{12,\mathrm{int}}) \cdot [1 + j\omega \cdot (C_{gs} \cdot R_i)]\right|$$

Equation 4. 41

$$\omega\tau = -\tan^{-1} \frac{\mathrm{Im}\{(y_{21,\mathrm{int}} - y_{12,\mathrm{int}}) \cdot [1 + j\omega \cdot (C_{gs} \cdot R_i)]\}}{\mathrm{Re}\{(y_{21,\mathrm{int}} - y_{12,\mathrm{int}}) \cdot [1 + j\omega \cdot (C_{gs} \cdot R_i)]\}}$$

Equation 4. 42

To minimizing the variance of each parameter over frequency, we first define the variance as:

$$\varepsilon_i = \sqrt{\frac{\sum_{k=1}^{N} [f_i(\omega_k, Z_{ext}) - \overline{f_i(\omega, Z_{ext})}]^2}{N-1}} \qquad (i = 1,2,\cdots 10)$$

Equation 4. 43

Here f_i represents the analytical expressions of each intrinsic parameter obtained from Equation 4. 33 through Equation 4. 42. We define a global weighted scalar as the objective function for the optimization routine:

$$\varepsilon = \sum_{i=1}^{10} W_i \varepsilon_i$$

Equation 4. 44

The weighting factors are selected from the normalization of minimum variance according to the optimization procedure performed on each intrinsic parameter. Or, if $\Re(\cdot)$ denotes the optimization routine, its output will give both the minimized variance and

corresponding optimized extrinsic vector:

$$\Re(f_i, \varepsilon_i, z_{ext}^{initial}) \rightarrow [\hat{\varepsilon}_i, \quad z_{ext}^{optimized}]$$

Equation 4. 45

Then W_i is defined as:

$$W_i = \frac{1}{\hat{\varepsilon}_i}$$

Equation 4. 46

To avoid non-physical convergence, we also strengthen the optimization routine by imposing the following inequality constraints:

$$[R_d, R_g, \cdots, L_s] \geq 0 \qquad and \qquad [\overline{f_1}, \overline{f_2}, \cdots, \overline{f_{10}}] \geq 0$$

Equation 4. 47

In a short summary, our hybrid extraction method firstly removes the contributions from the pad capacitances, achieved via a cold pinch-off measurement. In order to find the weighting factors, the routine is run to minimize the variance for each intrinsic element individually. Then the weighted average is set to be the objective function, and the routine is run again to obtain the globally optimized extrinsic vector. Finally, the calculated S-parameters are evaluated with measured data. The flow chart demonstrating this extraction procedure is shown in Figure 4. 10.

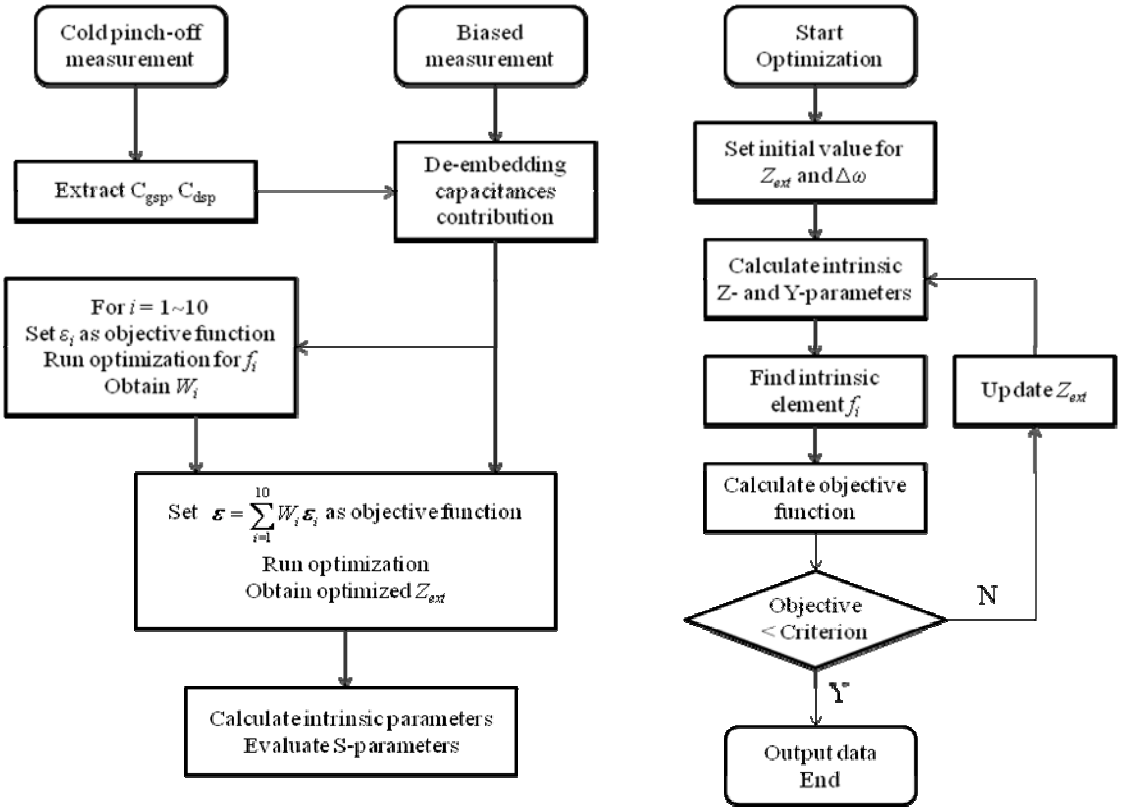


Figure 4. 10 Working flow for the extraction procedure

A sequential quadratic programming (SQP) algorithm, which is a generalization of Newton's method[106], is utilized in solving this constrained optimization problem. The objective function and the constraints are replaced with quadratic and linear approximation respectively. The convergence properties of the algorithm can be improved by using line search with penalty parameters recommended in ref. 107. Noting that it is a gradient-based method, the convergence of the program relies on the continuity of the objective function. Therefore the measurements should be carefully conducted to avoid noise or movements of the reference planes.

For the same device as measured in cold measurements, we still take the pad capacitances as: C_{gsp} = 0.069 pF; C_{dsp} = 0.062 pF. In Figure 4. 11 we demonstrate the intrinsic parameters

obtained from the optimization routine, using the measured data taken at V_{DS} = 4V, V_{GS} = -3V in the frequency range from 2 GHz to 20 GHz.

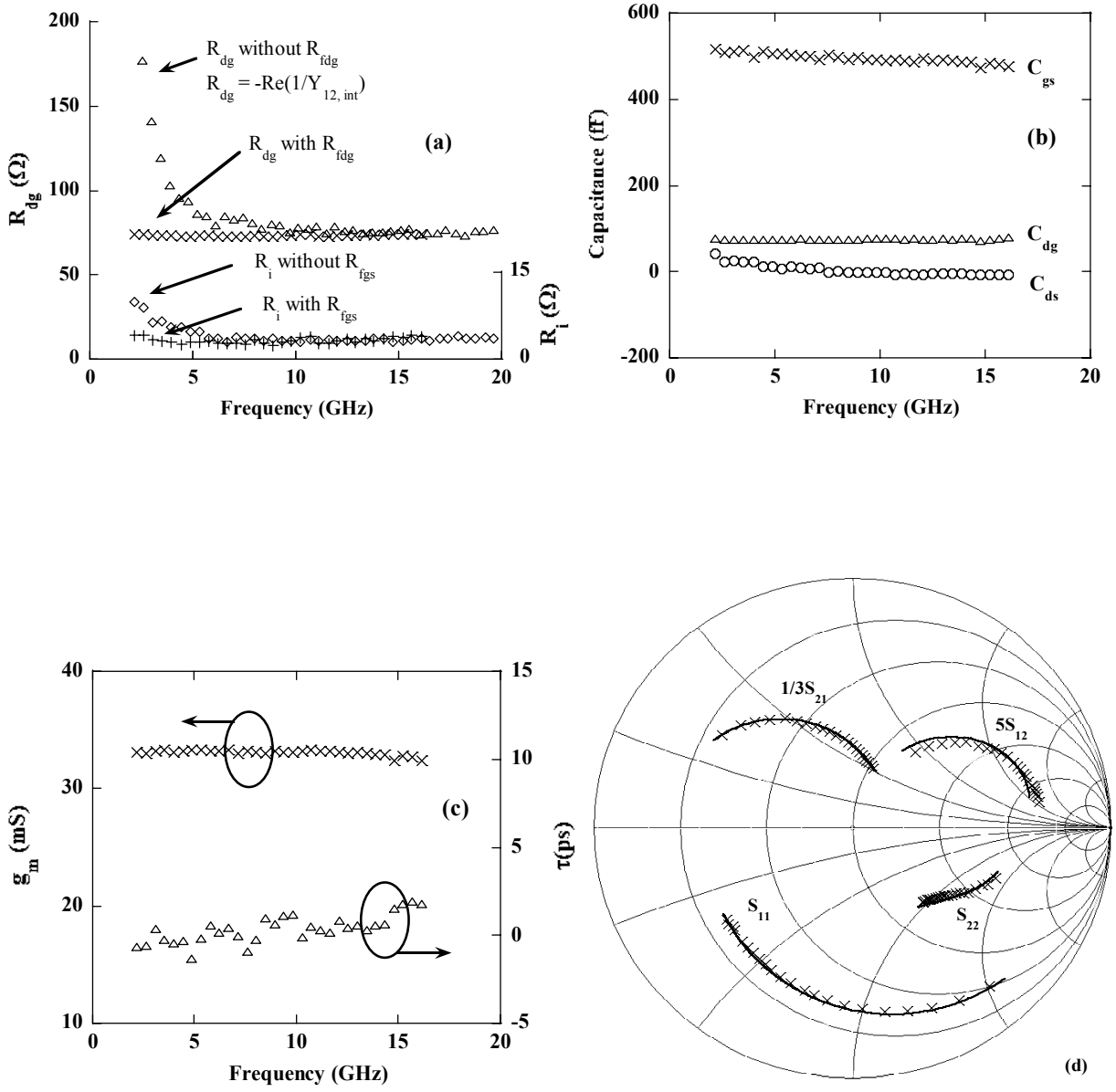


Figure 4. 11 Optimized intrinsic elements from the data measured at V_{DS} = 4 V, V_{GS} = -3 V, and frequencies from 2 GHz to 20 GHz. (a) R_i and R_{dg}, with and without the differential resistances R_{fdg} and R_{fgs} considered. (b) C_{dg}, C_{gs}, and C_{ds} . (c) g_m and τ. (d) Measured (×) and simulated (line) S parameters.

The calculated intrinsic parameters have shown good frequency invariance properties. In order to demonstrate the importance of the differential resistance values, we also optimized and simulated a simplified intrinsic circuit model without the differential resistances. Neglecting them imparts a profound effect onto R_{dg} and R_i at lower frequencies as shown in Figure 4. 11 (a). A good agreement is achieved between measured and simulated S-parameters with only a 3.86% average error in this frequency range at such a bias condition. The calculated intrinsic and extrinsic parameters are listed in Table 4. 4.

R_s (Ω)	2.80	L_s (pH)	81.55
R_d (Ω)	3.94	L_d (pH)	180.91
R_g (Ω)	0.00	L_g (pH)	13.61
C_{gsp}(fF)	69.0	R_{fgs} (kΩ)	0.93
C_{dsp}(fF)	62.0	R_{fdg} (kΩ)	22.96
C_{gs} (fF)	489.26	R_i (Ω)	3.30
C_{ds} (fF)	0.00	R_{ds} (Ω)	197.17
C_{dg} (fF)	76.56	R_{dg} (Ω)	72.72
g_m (mS)	32.92	ΔS	3.86%
τ (ps)	0.51		

Table 4. 4 The extracted extrinsic and intrinsic parameters optimized from the hot-FET measurements data, same conditions as the cold-FET.

As seen above, the equivalent circuit for a GaN HFET is more complicated than the conventional models for GaAs or SiC devices. The involvement of the gate differential resistances is necessary, which under the reverse bias conditions represent leakage current paths

of the gate Schottky diode. Due to the defects and dislocations in the crystal and assistance from surface states or traps, the leakage current term is always non-negligible. Especially at low frequencies where the value of ωC is small, the differential resistance term will be predominant in total conductance. Although the increase in the number of circuit elements brings extra complexity in hot-FET extraction, the intrinsic parameters can still be calculated via the strengthened optimization routine.

By analyzing and comparing different small signal modeling methods, we could examine the validity and consistency of the results. In our GaN HFET device, the parasitic resistances extracted under different techniques are consistent, while the parasitic inductances show large variation. Basically, the inductances calculated from hot-FET models are always larger than that from cold-FET measurements. This difference may reflect the change of the pad parasitic at hot conditions compared with cold conditions. Also for GaN HFET, more profound material defects related reasons may be also involved since the frequency range used for extrinsic subtractions between hot and cold methods are different. The error generated in cold measurements could propagate, affecting the accuracy of the intrinsic parameters obtained thereafter.

From a mathematical point of view, the optimization-based extraction routine will undoubtedly produce the smallest error at one certain condition, compared to the other techniques. However, it is more meaningful to evaluate the validity of this method at various bias conditions. Thus we verified its stability first by testing whether the results depended on the initial values at each bias condition. By selecting all zeroes, random numbers, and results from the cold measurement as the initial values for z_{ext}, we found that at each bias, the routine led to the same results regardless of the initial values chosen. Second, 15 different bias conditions were tested for one device as shown in Table 5. The overall simulation error is seen as approximately

5%. In contrary, this number rises up to more than 10% for the corresponding bias points using the constant extrinsic parameters from cold measurements. In favor of the large signal device nonlinearity analysis, it is usually convenient to assume the extrinsic parameters to be constant. If one were to do so by taking the mean value of the extrinsic parameters over all bias points as the set of bias-independent extrinsic parameters, the error will increase, remaining below 9% for every bias condition.

V_{GS} (V) / V_{DS} (V)	-2.5	-3.0	-3.5
3.0	8.21, 0.93, 3.32 4.47%	8.34, 3.26, 4.19 6.71%	0.00, 8.73, 2.64 4.00%
4.0	2.72, 11.67, 3.95 5.47%	2.80, 3.94, 0.00 3.86%	3.43, 7.78, 1.13 5.73%
5.0	4.36, 6.32, 2.19 4.32%	0.00, 4.45, 3.58 5.32%	0.00, 4.83, 3.58 5.39%
6.0	0.00, 14.67, 3.63 5.42%	2.14, 6.65, 1.05 5.46%	2.20, 9.09, 2.50 5.34%
7.0	0.00, 4.19, 0.00 2.64%	0.00, 11.24, 2.44 5.76%	0.00, 0.00, 2.89 4.50%
	R_s , R_d , R_g (Ω) ΔS	R_s , R_d , R_g (Ω) ΔS	R_s , R_d , R_g (Ω) ΔS

Average: $R_s = 2.28\ \Omega$, $R_d = 6.52\ \Omega$, , $R_g = 2.47\Omega$

Table 4. 5 The parasitic resistances and calculated S-parameters simulation error for different bias conditions, from optimization method.

In conclusion, when simulating the *S*-parameters of the GaN HFET, our hybrid extraction

method provides a high accuracy with an overall error of approximately 5% without any initial-value dependence compared with traditional cold measurement methods. The extracted extrinsic parameters show a notable dependency on applied biases. We believe that the cold measurement method may not be able to generate accurate enough parasitic parameters especially on inductances that can be used for intrinsic parameter extraction at operation voltages. As such, our hybrid optimization routine can give more reliable extrinsic and intrinsic values for the small signal equivalent circuit for GaN HFET.

Chapter 5 Physics Modeling

The physics model which the most of the simulation tools are now based on is the drift-diffusion (DD) model. The basic theories include semiconductor carrier statistics, Poisson equation, and carrier transport mechanism.

First, let's look at the Poisson equation, which is derived from the Gauss's law for electricity:

$$\nabla \cdot \vec{D} = \rho$$

Equation 5. 1

Where D is the electric displacement, ρ is the free charge density. Furthermore, the displacement is related with electric field and polarization field:

$$\vec{D} = \varepsilon \vec{F} + \vec{P}$$

Equation 5. 2

Since the electric field is the derivative of potential field, so finally we obtain the Poisson equation as:

$$\nabla(\varepsilon \nabla \varphi) + \nabla \cdot \vec{P} = \rho$$

Equation 5. 3

Here we should pay much attention to the polarization field, which is not zero across a GaN heterojunction. It causes profound change to the charge and potential distribution.

The way to calculate the carrier population is one of the major differences between classical drift-diffusion model and quantum corrected drift-diffusion model. The traditional DD model utilizes the classic carrier statistics, which allow carriers momentum to be any direction. For example, the electron density within the non-degenerated semiconductor is:

$$n = N_C \exp(\frac{E_F - E_C}{kT})$$

Equation 5. 4

However, in the heterojunction devices, the potential wells or barriers are presented at the interfaces due to the discontinuity of energy bands. The movement of carriers is confined by the heterojunctions. Thus the classical carrier statistics are not accurate anymore within those regions. Take two-dimensional heterojunction structures for example, the carriers are confined on discrete energy sub-bands, and the density of state for each sub-band is a constant:

$$\rho_{2D} = \frac{m^*}{\pi\hbar^2}$$

Equation 5. 5

The density of state theory gives the electron distribution function as:

$$n = \sum_m \int_{E_m}^{\infty} \rho_{2D} f(E) |\psi_m|^2 dE$$

Equation 5. 6

Here the ψ_m is the wave function of the mth sub-band, and f is the distribution function, which usually takes Fermi-Dirac distribution. Therefore, Schrondinger equation has to be solved to obtain correct carrier distribution. With the quantum correction, the calculated carrier distribution can be quite different from the classical method, seeing Figure 5. 1 as an example for Si MOSFET.

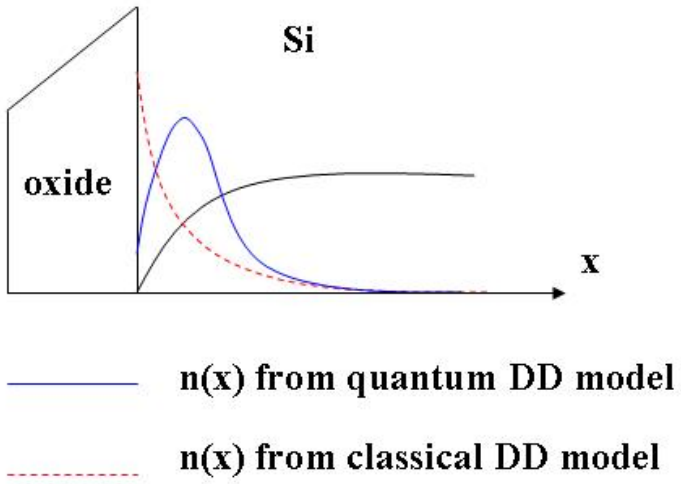


Figure 5. 1 A schematic that represents the different results from quantum DD model and classic DD model.

When the external field is applied onto the device, DD model expresses the current density as a sum of two components: The drift component which is driven by the field and the diffusion component caused by the gradient of the carrier concentration. Here for HFET, we consider only electrons.

$$j_n = nq\mu\nabla\varphi + qD\nabla n$$

Equation 5. 7

In the non-equilibrium case, the Fermi level inside the semiconductor is not a constant anymore, and quasi-Fermi level is introduced to describe the carrier population displaced from equilibrium. Furthermore, the current density is considered as proportional to the gradient of the quasi-Fermi level:

$$j_n = nq\mu\nabla E_{Fn}$$

Equation 5. 8

Another important expression is the current continuity equation, which defines the change of current within the semiconductor to be related with the carrier recombination rate U:

$$\nabla \cdot j_n = qU$$

$$\nabla \cdot j_p = -qU$$

Equation 5. 9

There are several kind of recombination mechanisms, such as the electron-hole Shockley-Read-Hall (SRH) recombination, Auger recombination, direct radiative recombination, which are of important in the modeling of solid-state lighting devices such as LEDs and LDs. However, here we assume that there exists no recombination in HFET at the working conditions. Thus the current density across the entire device is a constant.

It is difficult to give a general optimum solution out of the equations above, since in most circumstances it depends on the device details. Based on a specified device structure and the information we are interested in, one can make several assumptions on HFET device and draw some general conclusions on the methodology.

5.1 Methodology to solve the quantum DD model

The quantum DD model based on the Boltzmann transport equation and quantum effects describes the movement of carriers at the non-equilibrium state within a semiconductor. It needs to handle the following relationships:

1. Poisson equation
2. Schrödinger equation and carrier statistics
3. Current equations

4. Continuity equations

Unfortunately, most of those equations are non-linear set, and it is impossible to give a direct and neat solution. The most popular methods are iteration-based Gummel algorithm[108] and Newton-Raphson algorithm[109]. In this work, I will use the Newton method, which is best known for its fastest converging performance.

Since the variables are correlated with each other in those equations, it's important first to choose the minimum set of unknowns as the independent variables of Newton method. One choice is to select potential and quasi-Fermi levels: (φ, E_{fn}, E_{fp}). Then I can define the residual errors for each independent variable as:

$$\begin{cases} E_1 = \varphi - \varphi^* \\ E_2 = E_{fn} - E_{fn}^* \\ E_3 = E_{fp} - E_{fp}^* \end{cases}$$

Equation 5. 10

Here (φ^*, E_{fn}^*, E_{fp}^*) are estimation values calculated from current iteration. According to the Newton method, giving a initial value on (φ^0, E_{fn}^0, E_{fp}^0), the next iteration could be expressed as:

$$\begin{pmatrix} \varphi^1 \\ E_{fn}^1 \\ E_{fp}^2 \end{pmatrix} = \begin{pmatrix} \varphi^0 \\ E_{fn}^0 \\ E_{fp}^0 \end{pmatrix} - J^{-1} \cdot \begin{pmatrix} E_1^0 \\ E_2^0 \\ E_3^0 \end{pmatrix}$$

Equation 5. 11

In this relation, J denotes for the Jacobian matrix of the residual errors:

$$J = \begin{bmatrix} \frac{\partial E_1}{\partial \varphi} & \frac{\partial E_1}{\partial E_{fn}} & \frac{\partial E_1}{\partial E_{fp}} \\ \frac{\partial E_2}{\partial \varphi} & \frac{\partial E_2}{\partial E_{fn}} & \frac{\partial E_2}{\partial E_{fp}} \\ \frac{\partial E_3}{\partial \varphi} & \frac{\partial E_3}{\partial E_{fn}} & \frac{\partial E_3}{\partial E_{fp}} \end{bmatrix} = \begin{bmatrix} 1-\frac{\partial \varphi^*}{\partial \varphi} & -\frac{\partial \varphi^*}{\partial E_{fn}} & -\frac{\partial \varphi^*}{\partial E_{fp}} \\ -\frac{\partial E_{fn}^*}{\partial \varphi} & 1-\frac{\partial E_{fn}^*}{\partial E_{fn}} & -\frac{\partial E_{fn}^*}{\partial E_{fp}} \\ -\frac{\partial E_{fp}^*}{\partial \varphi} & -\frac{\partial E_{fp}^*}{\partial E_{fn}} & 1-\frac{\partial E_{fp}^*}{\partial E_{fp}} \end{bmatrix}$$

Equation 5. 12

The speed of convergence for Newton method is at least quadratic at the neighborhood of roots. In most cases, the algorithm can convergence within 20-30 iterations, to get enough small residual error, which in another words means to reach the solution of (φ, E_{fn}, E_{fp}).

For the estimations value (φ^*, E_{fn}^*, E_{fp}^*), first I assume no hole is taken into account in as carrier within the HFET device. Therefore variable E_{fp} and E_{fp}^* are neglected. Referring to Equation 5. 1 to Equation 5. 6, the estimated potential φ^* is calculated from (φ, E_{fn}) as:

$$\begin{cases} -\frac{\hbar^2}{2}\nabla\left(\frac{\nabla\psi}{m}\right) + E_c \cdot \psi = E_m \psi \\ n = \rho_{2D} k_B T \sum \ln\left[1+\exp\left(\frac{E_{fn}-E_m}{k_B T}\right)\right] \cdot |\psi|^2 \\ \nabla(\varepsilon \nabla \varphi^*) + \nabla \cdot \vec{P} = q(N_D^+ - n) \end{cases}$$

Equation 5. 13

The Schrödinger equation is based on single electron approximation within the semiconductor. The wave functions ψ and discrete energy levels should be obtained, and feed into the second equation for carrier statistics (n) calculation. Then the estimation φ^* is solved from the Poisson equation. Furthermore, the derivatives of φ^* are computed in stack:

$$\begin{cases} \dfrac{\partial \varphi^*}{\partial \varphi} = \dfrac{\partial \varphi^*}{\partial n}\dfrac{\partial n}{\partial \psi}\dfrac{\partial \psi}{\partial \varphi} \\ \dfrac{\partial \varphi^*}{\partial E_{fn}} = \dfrac{\partial \varphi^*}{\partial n}\dfrac{\partial n}{\partial E_{fn}} \end{cases}$$

Equation 5. 14

Another variable E_{fn}* is calculated from current equations by combining Equation 5. 8 and Equation 5. 9, assuming no recombination in the HFET:

$$\nabla(n \cdot \mu \cdot \nabla E_{Fn}^*) = 0$$

Equation 5. 15

And the derivatives of E_{Fn}* can be calculated similarly.

In short, given an initial value on (φ, E_{fn}), the algorithm first computes the wave function from the Schrödinger equation solver. Then the carrier distribution n is determined within the quantum confined region. The estimated potential and Fermi level are obtained by solving the Poisson equation and the current equation. This estimation values are feed into Newton module to calculate the Jacobian matrix and update (φ, E_{fn}), and loop back for next iteration until exit criteria meets. However, almost all above equations are high order partial differential equations (PDEs) with only numerical solution, which makes the determination on the Jacobian matrix complicate. Another difficulty lies in the tremendous computational efforts. In case of a two dimensional device modeling with N^2 grid points, the size of Jacobian matrix reaches $2N^2 \times 2N^2$. Without fast computing method, the matrix operation is too time-consuming to afford.

Unlike LEDs or RTDs, GaN HFET is a lateral conduction device. The materials along the plane perpendicular to the growth direction have homogeneous property giving no confinements to carriers. Also, the lateral device geometries are much larger than the dimensions of vertical layer structures. Therefore, usually the distributions of carriers and conduction band along *c*-GaN

direction are of interest than the other directions.

An important assumption is the Fermi level along *c*-GaN is a constant, even with the presence of the gate and applied bias. This implies that the vertical conduction is negligible. This assumption is based on the fact that the gate is usually reversely biased, and the vertical current flowing from gate is much smaller compared with the lateral conduction from source to drain.

To unify the nomenclatures in one-dimensional and two-dimensional simulations, the basic layer structure and the axis directions are shown in Figure 5. 2.

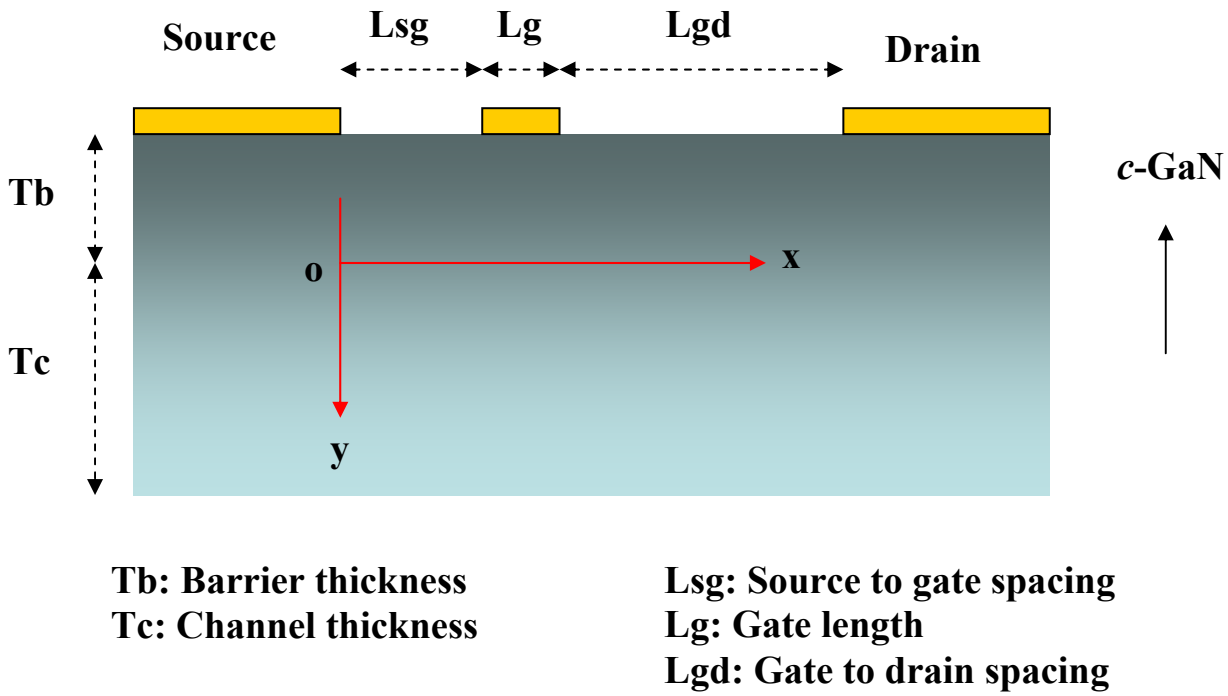


Figure 5. 2 A schematic showing the axis definitions and nomenclatures used for modeling.

In the following sections, I will first focus on the 1D solution along *c*-GaN. It can give us plenty of useful information such as the device band diagram and carrier distribution. Besides, it also paves the way for the 2D device simulations to investigate the cross-section profile around the channel.

5.2 One-dimensional modeling

5.2.1 Self-consistent solution to Schrödinger-Poisson equations

The one-dimensional Schrödinger equation across the heterojunction can be written as[110, 111]:

$$-\frac{\hbar^2}{2}\frac{d}{dy}[\frac{1}{m_e(y)}\frac{d}{dy}]\psi_m(y)+E_C(y)\psi_m(y)=E_m\psi_m(y)$$

Equation 5. 16

where $m_e(y)$ is the electron effective mass, it is position dependent; E_m is the eigenenergy for m^{th} subband; ψ_m is the wavefunction corresponds to this eigenenergy; y is opposite to c-GaN direction; and E_C is the energy band that incorporates with conduction band discontinuity and static potential φ by:

$$E_C(y)=-q\varphi(y)+\Delta E_C$$

Equation 5. 17

Here ΔE_C is the conduction band discontinuity at the interface. The Schrödinger equation in Equation 5. 16 can be also expressed as:

$$H\psi=E_m\psi$$

Equation 5. 18

where H is the Hamiltonian operator. In single electron approximation, electron energy is admissible on stationary eigenvalue E_m. After mesh $x_i \subset (1, N)\Delta x$, and the discretatization on H matrix would be:

$$H = \begin{bmatrix} \frac{\hbar}{2\Delta x^2}(\frac{1}{m_2}+\frac{1}{m_1}) - Ec_2 & \frac{-\hbar}{m_2 2\Delta x^2} & 0 & \cdots & 0 & 0 \\ \frac{-\hbar}{m_2 2\Delta x^2} & \frac{\hbar}{2\Delta x^2}(\frac{1}{m_3}+\frac{1}{m_2}) - Ec_3 & \frac{-\hbar}{m_3 2\Delta x^2} & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & \frac{-\hbar}{m_{N-3} 2\Delta x^2} & \frac{\hbar}{2\Delta x^2}(\frac{1}{m_{N-2}}+\frac{1}{m_{N-3}}) - Ec_{N-2} & \frac{-\hbar}{m_{N-2} 2\Delta x^2} \\ 0 & 0 & \cdots & 0 & \frac{-\hbar}{m_{N-2} 2\Delta x^2} & \frac{\hbar}{2\Delta x^2}(\frac{1}{m_{N-1}}+\frac{1}{m_{N-2}}) - Ec_{N-1} \end{bmatrix}$$

Equation 5. 19

Therefore, the problem of solving the descret energy spectrum E_m and wave function would become the determination of eigenvalue/eigenvector of H matrix. Note that the size of H matrix is (N-2)×(N-2).

Once the wave functions are obtained, the carrier distribution can be calculated from Equation 5. 6. Applying the Fermi-Dirac distribution, the expression will become:

$$n(y) = \frac{m_e}{\pi\hbar^2}\sum_m \int_{E_m}^{\infty} \frac{|\psi_m(y)|^2}{1+\exp(\frac{E-E_{Fn}}{k_B T})} dE = \frac{m_e k_B T}{\pi\hbar^2}\sum_m \ln[1+\exp(\frac{E_{Fn}-E_m}{k_B T})]\cdot|\psi_m(y)|^2$$

Equation 5. 20

If we consider both ionized shallow and deep donors as the source of charges within the semiconductor, then the one-dimensional Poisson equation is written as:

$$\frac{d}{dy}[\frac{1}{\varepsilon(y)}\frac{d\varphi(y)}{dy}] + \frac{dP(y)}{dy} = q[\sum N_D^+ - n(y)]$$

Equation 5. 21

where ε is the dielectric of each layer, $n(y)$ is the electrons from previous equation. Similar to

Schrödinger equation, 1D Poisson equation has a matrix form expression and the solving is equivalent to the matrix inversion operation. The polarization charge term *dP(y)/dy* become a delta function, with nonzero values only at the interface. Similar to Equation 5. 21, the Poisson equation after discretization also has a linear algebra expression. Basically to solve it is equivalent to solve the linear system equation $\boldsymbol{A}x=b$.

Since we assume the Fermi level is a constant across each layer, usually it is fixed at the zero level in 1D simulation. Therefore, potential is the only variable to be calculated, and the Jacobian matrix reduces to one term $\partial\varphi*/\partial\varphi$. Equation 5. 14 is used to compute the Jacobian matrix. Take $\partial\psi/\partial\varphi$ for example, once the Green matrix of the Schrödinger equation is determined, this derivative can be expressed as:

$$\frac{\partial\psi_m}{\partial\varphi} = -q(H - E_m \cdot I)^{-1} \cdot \varphi$$

Equation 5. 22

here **I** is identity matrix; φ needs to be expand into diagonal matrix. With grid size *N*, all matrixes are *N*×*N* square one.

The basic flow chart of the numerical calculation procedure is shown in Figure 5. 3. Starting with a trial value on potential, the Schrödinger equation is first solved to obtain the wave functions and eigen-energy levels. Then, the carrier distribution *n* and sheet density n_s can be calculated as the input to the Poisson equation. The newly estimated potential $\varphi*$ is then compared with the starting value. If the error between the two is within a predefined criterion, one then ends the iteration. Otherwise φ is updated by compute the Jacobian matrix out of each equation.

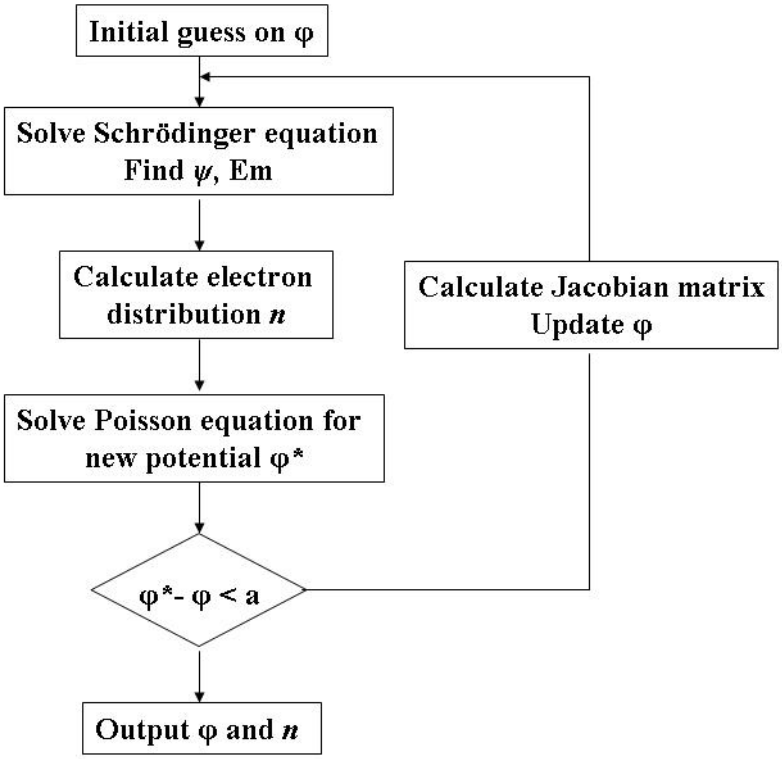


Figure 5. 3 Flow chart of the numerical calculation procedure for Self-consistent Schrödinger-Poisson equations.

5.2.2 Other considerations

Several more treatments that are related to the unique properties of GaN material can applied to the modeling, provide us better understanding to the device performance.

1. Strain induced band gap shrink

For AlGaN/GaN heterojunction, the uniaxial strain existed at the interface will cause the conduction and valence band edge shift. Therefore the conduction band gap is slightly smaller than the caused by. The reduction of conduction band discontinuity is given by:

$$\Delta E = a_{33}\varepsilon_{\perp} + 2a_{31}\varepsilon_{\text{II}}$$

Equation 5. 23

Where $\varepsilon_{\text{Ц}} = \frac{a - a_c}{a_c}$, and $\varepsilon_{\perp} = -2\frac{C_{13}}{C_{33}}\varepsilon_{\text{Ц}}$. The deformation potential for wurtzite semiconductors can be found in 112. In general, the band gap of tensile strained AlN or AlGaN shrinks that lowers energy barrier and reduces sheet carrier concentration consequently.

2. Electromechanical coupling effect

During the calculation of piezoelectrical polarization, it is assumed that this kind of polarization is induced by strain due to the lattice mismatch between AlGaN barrier and GaN buffer. However, since the presence of strong electrical field at the interface, the effect of electric field induced strain that causes the change of piezoelectricity in AlGaN, which is often referred to as the electromechanical coupling, should be considered.

According to the Hooke's law, the displacement that used in the uncoupled case must be replaced with the coupled pair. The coupled formulation is based on the linear piezoelectric constitutive equations for stress and electric displacement[113]:

$$\sigma_{ij} = C_{ijkl}\varepsilon_{kl} - e_{kij}F_k$$
$$Di = e_{ijk}\varepsilon_{jk} - \kappa_{ij}F_j + P_i^S$$

Equation 5. 24

where σ_{ij} is the stress tensor, C_{ijkl} is the fourth rank elastic stiffness tensor, ε_{kl} is the strain tensor, e_{ijk} is the third ranked piezoelectric coefficient tensor, κ_{ij} is the second rank permittivity tensor, D_i is the electric displacement, F_k is the electric field, and P_i^S is the spontaneous polarization. The indices i, j,k, and l run over the Cartesian coordinates 1, 2, and 3 (x, y, and z). Einstein's rule of summation over repeated indices is implied. The symmetry of the wurtzite crystal structure of

GaN and AlGaN reduces the number of independent elastic and piezoelectric moduli. In the devices considered here, the crystals are grown with the *c* axis normal to the surface in the *z* direction, we make the common assumption that the thick GaN layer is unstrained, and the biaxial strain of the thin AlGaN layer satisfies $\varepsilon_{xx} = \varepsilon_{yy} = \left(a_{GaN} - a_{AlGaN}\right)/a_{AlGaN}$, where a_{GaN} and a_{AlGaN} are the *c*-plane lattice constants of each material constituting the heterojunction. The absence of stress along the growth direction (*z*-direction), in the barrier AlGaN layer, allows us to express the strain along the growth direction as[114]:

$$e_z = -2\frac{C_{13}}{C_{33}}\varepsilon_{xx} + \frac{e_{33}}{C_{33}}E_z^{AlGaN}$$

Equation 5. 25

where E_z AlGaN is the *z*-directed electric field in the barrier AlGaN layer and we have expressed the elastic and piezoelectric moduli in matrix notation[115]. The equivalent sheet charge density due to PE polarization in AlGaN is given by ref. 114

$$P_{PE}^{AlGaN} = 2\varepsilon_{xx}(e_{31} - \frac{C_{13}}{C_{33}}e_{33}) + \frac{e_{33}^2}{C_{33}}F_Z^{AlGaN}$$

Equation 5. 26

The electric field on both side of interface satisfies the conservation on electric displacement, while the field on the channel side can be deduced from the Poisson equation by neglecting the impurity and hole concentration as follows:

$$\int_{z=d+}^{\infty} dF(z) = \int_{z=d+}^{\infty} \frac{q}{\kappa^{GaN}}[q(z) - n(z) + \sum_i N_{Di}^{+} - \sum_i N_{Ai}^{-}]dz \approx -\frac{q}{\kappa^{GaN}}\int_{z=0}^{\infty} n(z)dz = -\frac{\sigma_{2DEG}}{\kappa^{GaN}}$$

with $F(\infty) - F(d_+) = 0 - F(d_+) = -F_Z^{GaN} = -\frac{\sigma_{2DEG}}{\kappa^{GaN}}$ or $\sigma_{2DEG} = \kappa^{GaN}F_Z^{GaN}$

Equation 5. 27

where κ is used as the permittivity of material, instead of the usual ε to avoid confusion with strain, and σ_{2DEG} is the two-dimensional electron gas charge density. Therefore, it will have:

$$\sigma_{2DEG} - \kappa^{AlGaN} F_Z^{AlGaN} = P^{AlGaN} - P^{GaN} = P_{PE}^{AlGaN} - \Delta P_{SP}$$

Equation 5. 28

where $\Delta P_{SP} = P_{SP}^{GaN} - P_{SP}^{AlGaN}$ represents the differential spontaneous polarization between the AlGaN barrier and GaN channel. Put the modified term of AlGaN piezoelectric polarization into Equation 5. 28, then we could get the electrical field at AlGaN side:

$$F_Z^{AlGaN} = \frac{1}{\kappa^{AlGaN} + e_{33}^2 / C_{33}} [\sigma_{2DEG} + \Delta P_{SP} - 2\varepsilon_{xx}(e_{31} - \frac{C_{13}}{C_{33}} e_{33})]$$

Equation 5. 29

Furthermore, the piezoelectric polarization in AlGaN can be rewritten as:

$$P_{PE}^{AlGaN} = 2\varepsilon_{xx}(e_{31} - \frac{C_{13}}{C_{33}} e_{33})(1-\alpha) + \alpha(\sigma_{2DEG} + \Delta P_{SP})$$

Equation 5. 30

where $\alpha = \frac{e_{33}^2 / C_{33}}{\kappa^{AlGaN} + e_{33}^2 / C_{33}}$ and represents the electromechanical coupling. Setting $\alpha = 0$ brings us back to the polarization charge with no coupling which can be obtained from Hooke's law and piezoelectric polarization in an uncoupled case.

3. Surface donor states

The solving for any differential equations requires the determination on boundary condition. On the top surface without Schottky gate, the value of surface potential served as the

boundary conditions for Poisson equation is important yet hard to specify. The Fermi level at the GaN surface is often found to be pinned due to the existence of surface donor states[116]. At the surface, the total number of surface states could be enormously large because of the dangling bond of the semiconductor atoms, as was noted in the venerable Si case many decades ago[117]. More interestingly it is surface states that is often believed to be the main source of electrons in the 2DEG at the channel[118, 119]. For a conventional AlGaN/GaN structure, the barrier is mid- or even un-doped. The intrinsic or the intended doping level is within $10^{16} \sim 10^{18}$ cm^{-3}. However, the 2DEG density is commonly around 10^{13} cm^{-2}. Even all of the donors are fully ionized, it can not provide enough electrons into the 2DEG. Therefore, the determination of surface potential depends on the population of ionized surface states, and furthermore relates to the carrier density of the system.

Very first consideration for any equilibrium system to satisfy is the conservation of the charges. Similar to that proposed in reference[120], we can take a simplifying treatment as follows: neglecting the hole and acceptor concentrations in the semiconductor and considering only the donor states, the charge neutrality condition is expressed as:

$$n_{sf}^{+} + N_D^{+} d = n_s$$

Equation 5. 31

with ns is the sheet electron density. We assume the density of ionized surface donor states n_{sf}^{+} follows the Fermi-Dirac distribution, and there is a single surface states energy level E_{sd}. Then it follows

$$n_{sf}^{+} = \frac{n_{sf}}{1 + g \exp(\frac{E_F - E_{sd}}{kT})}$$

Equation 5. 32

The degeneracy factor g is 2 and surface donor state's energy level is approximately 1.2 eV below the conduction band according to Scanning Kelvin Probe Microscopy measurement. Given a certain surface potential boundary value, carrier distribution and sheet density can be calculated. Furthermore, this value should satisfy Equation 5. 31 and Equation 5. 32 and update iteratively. The density of total surface donor state n_{sf} can be assumed to be up to 10^{15} cm^{-2}, and the calculation shows that E_F at the surface is often pinned to the energy level of surface donor.

If a Schottky gate is present, then the surface states will be depleted and the potential at the surface will be fixed by the barrier height and applied voltage. Thus the potential boundary value is easy to be determined.

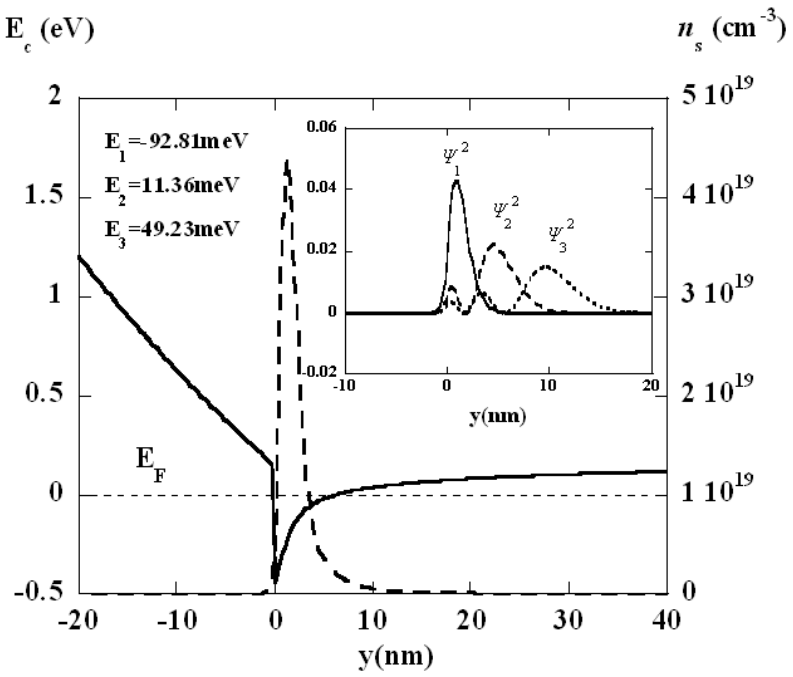
5.3 One-dimensional modeling results

5.3.1 Band diagram and carrier distribution

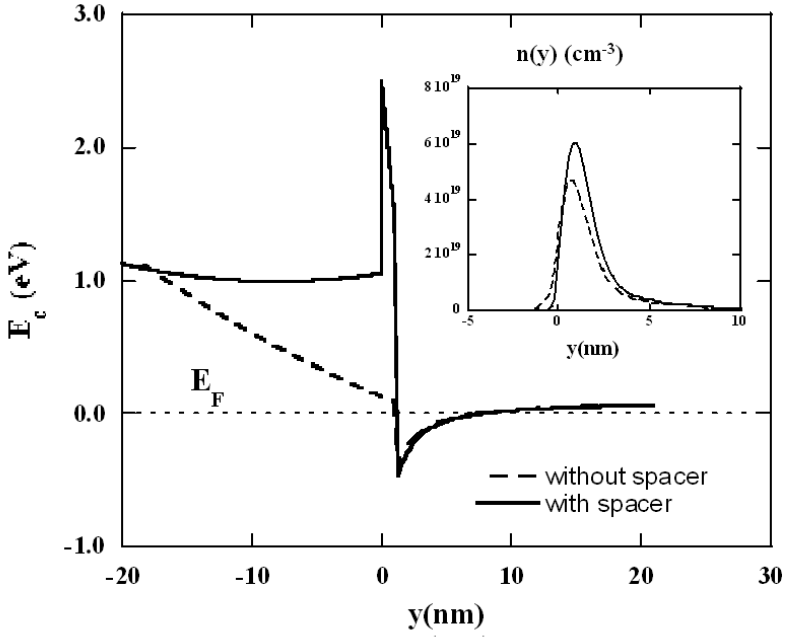
The ionized donor states at the AlGaN surface have been reported to reach 10^{13} $cm^{-2}eV^{-1}$ with distributed in energy within 1~1.8eV below the conduction band[121]. During the simulation, the surface state density was assumed to be extremely large up to 10^{15} cm^{-2}, with single donor energy level locate at 1.2eV to make sufficient number of electrons are available from this source alone for the system to reach equilibrium. Additionally assumed shallow and deep donors in the barrier layer have concentrations of 8×10^{17} cm^{-3} and 5×10^{17} cm^{-3}, and the ionization energy levels are 30 meV and 1.0 eV below the conduction band respectively. Both AlGaN and AlInN barrier structures are investigated, with the 25% and 82% Al mole fraction in each case. The

barrier thickness is 20 nm. The spontaneous and piezoelectric polarizations are calculated as introduced in Chapter 1.4, for which the detailed steps could also be found in 122, 123. For lattice matched $Al_{0.82}In_{0.18}N$ barrier, neither piezoelectric polarization nor conduction band reduction exists since the varnish of the strain.

For the solving of Schrödinger equation, the *y*-range of wavefunction into the bulk GaN is 100 nm, and the first 10 energy eigen-states are considered. For AlGaN barrier structure, the room temperature total sheet electron density is approximately 1×10^{13} cm^{-2}. The band diagram and electron distribution are shown in Figure 5. 4 (a). The eigen-energies and the wave functions of first three sub-bands are also shown. As can be seen, the most of the 2DEG is confined within a 5 nm channel under the interface. The ground energy state level (~100 meV) is consistent with the experiments results from Shubnikov-de Haas (SdH) measurements[124, 125]. The conduction band edge diagram and electron distribution for an AlGaN/GaN system with an AlN spacer layer is shown in Figure 5. 4 (b). Compared with the normal AlGaN/GaN heterojunction with the same Al mole fraction and doping concentration, the AlN spacer provides a better confinement with smaller proportion of the electron wavefunction spilling into the barrier. The total sheet carrier concentration increase from 1.1×10^{13} cm^{-2} to 1.3×10^{13} cm^{-2}.


E_c (eV)
n_s (cm^-3)
E_1=-92.81meV
E_2=11.36meV
E_3=49.23meV
E_F
y(nm)
ψ_1^2
ψ_2^2
ψ_3^2

(a)


n(y) (cm^-3)
E_c (eV)
E_F
y(nm)
without spacer
with spacer

(b)

Figure 5. 4 (a) Calculated conduction band profile, electron distribution, and eigenenergy for the first three subbands in an AlGaN/GaN heterojunction, wavefunctions are shown in the insert (b) Band structure for AlGaN/GaN HFET structure with and without an AlN spacer; electron density distributions are shown in the insert.

Taking the electromechanical coupling effect into account, the change of band diagram is small, as shown in Figure 5. 5. Also, the total sheet carrier concentration changes only from 1.19×10^{13} cm^{-2} to 1.17×10^{13} cm^{-2}. This is due to the small built-in electrical field in the barrier layer (F_Z^{AlGaN}) in the absence of Schottky metal and applied voltage on the surface.

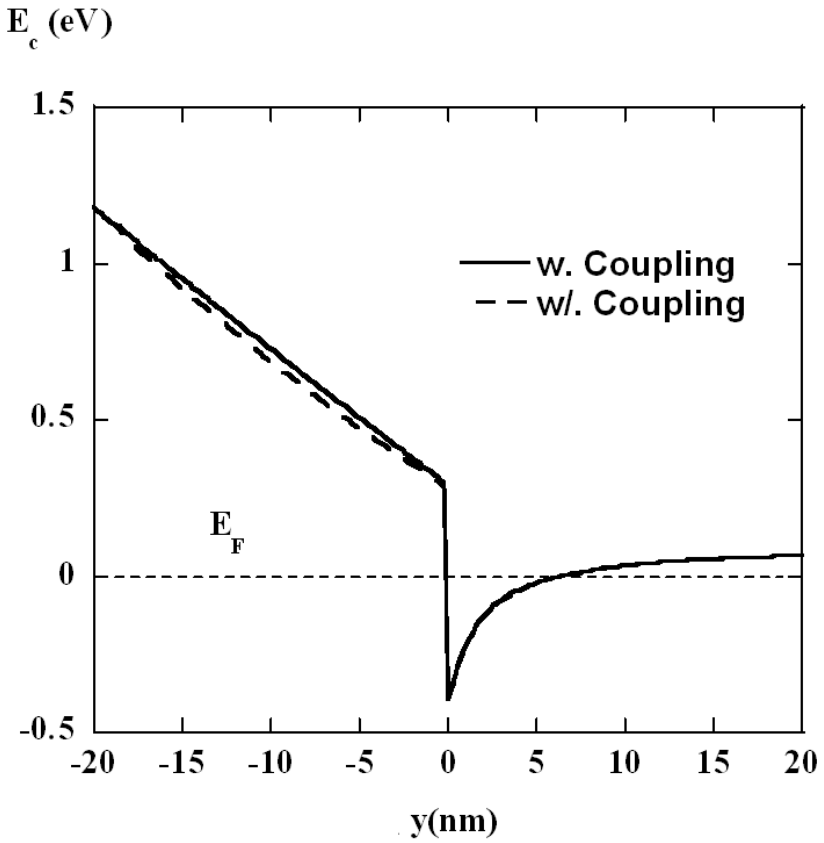
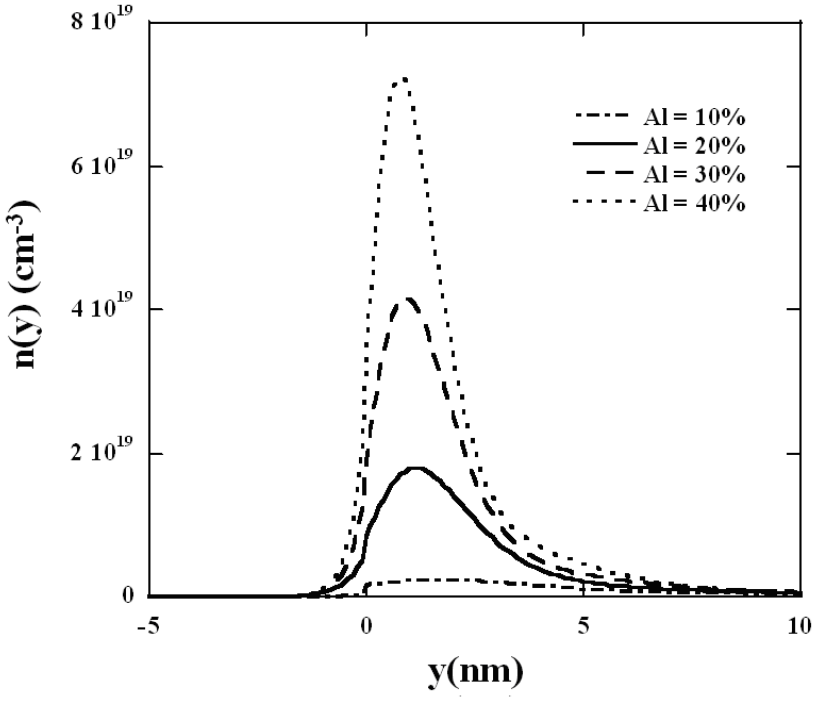
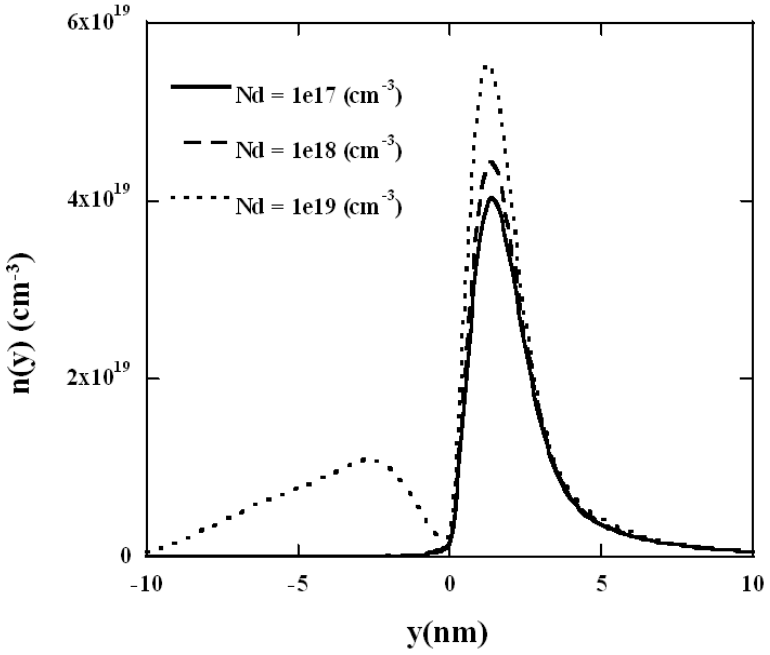


Figure 5. 5 Conduction band profile with and without the electromechanical coupling in an AlGaN/GaN heterojunction.

The electron distribution in the AlGaN/GaN HFET structure with 10, 20, 30, and 40% Al mole fractions is shown in Figure 5. 6 (a). Increasing the Al content induces a larger polarization charge at the AlGaN/GaN interface and consequently a higher channel electron concentration at equilibrium. The distribution of electrons in the channel with varying doping (10^{17} cm^{-3} ~ 10^{19} cm^{-3}) in the barrier is shown in Figure 5. 6 (b). Increasing the doping in the barrier supplies more electrons to the channel and thus increases the total sheet density. However, it comes with side-effects such as the decreased mobility and the increase of gate leakage current[126].



(a)

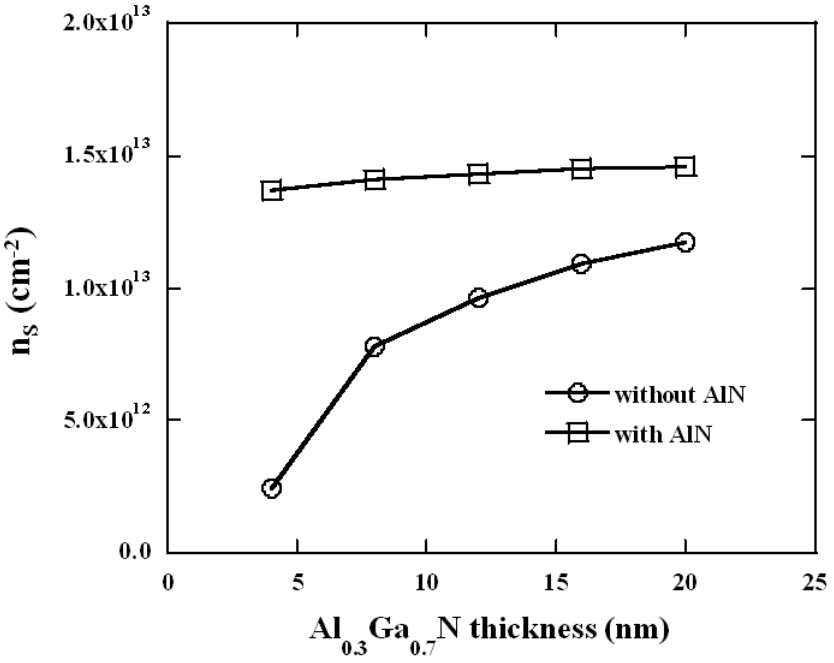


(b)

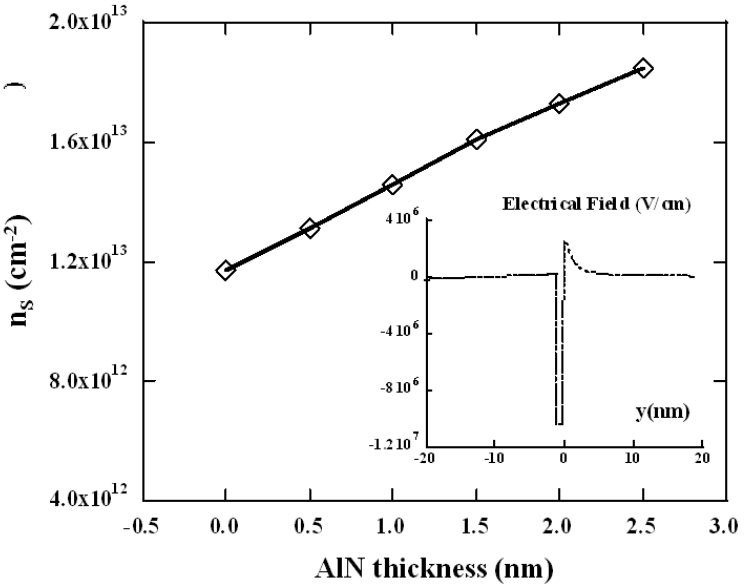
Figure 5. 6 Carrier distribution for (a) different Al% and, (b) different shallow donor concentrations in the AlGaN/GaN HFET structure.

Experiments have been reported in which the thickness of the AlGaN barrier in the HFET structures has been shown to have a significant influence on the channel carrier density and device performance[43,127], especially regarding the reliability[128]. The associated interpretation assumes the source of electrons to be the surface states. The calculated total sheet carrier concentration n_s as a function of the AlGaN barrier thickness is shown in Figure 5. 7 (a), for both with and without 1 nm AlN spacer layer cases. The increase of n_s with thicker barrier is because when the AlGaN thickness increases, the potential well at the interface becomes deeper. The build-in electrical field on the channel side is stronger, which is proportional to the 2DEG sheet density. In addition, insertion of an AlN barrier increases the piezoelectric-induced polarization

(the spontaneous polarization is not influenced in net). Moreover, with the help of AlN spacer, n_s has a weakened dependence on the barrier thickness. The calculated data are in good agreement with those reported in ref. 43. The reason of this phenomenon is that the large band gap discontinuity between AlN and GaN serves to "buffer" the change in potential energy caused by the variation of barrier thickness, thus lessens the impact on the potential well profile in the channel.



(a)



(b)

Figure 5. 7 (a) Sheet carrier density dependence on AlGaN barrier thickness, with and without 1 nm AlN spacer. (b) Sheet carrier density dependence on AlN thickness in AlGaN/AlN/GaN HFET structure, the electrical field distribution in AlGaN/AlN/GaN HFET structure with 1nm AlN spacer is shown also.

Because of the strong polarization induced large lattice mismatch between AlN and GaN, and the associated compositional gradient at the interface insertion of the AlN spacer layer increases the sheet electron density. Very high carrier density (5×10^{13} cm^{-2}) and strong internal electrical fields (10^9 V/m) at the AlN/GaN interface have been observed or calculated [45, 129, 130]. The dependence of sheet density and AlN spacer thickness for AlGaN/GaN HFET structures is plotted in Figure 5. 7 (b). The electrical field distribution for 1nm AlN spacer case is also plotted in the figure. While the AlN spacer layer helps to improve the low field transport properties by providing higher electron concentration and mobility, and lower leakage current, the strong built-in electrical field may cause breakdown to occur in the spacer and therefore reduce the long term

reliability of the device. Experimental data involving a large number of HFETs with and without the AlN layers seem to unequivocally indicate that the presence of AlN causes more rapid degradation[131] in terms of the leakage current and output power under RF stress.

By far the theoretical calculation is all focused on the AlGaN barrier device structure. From the Hall measurements seen in Chapter 3.2.1, the calculated results are consistent with the experiments, especially the total sheet carrier density and its dependence on barrier thickness. For AlInN barrier case, the calculation is similar to AlGaN structure, while the total sheet carrier density is much larger reaching $2\sim3\times10^{13}$ cm^{-2} range due to the larger band gap and stronger polarization. However, the experimental results do not match with the calculations for AlInN device. More details will be discussed in Chapter 5.5.

5.4.2 Electrical characteristics

If considering the real device structure with the presence of Schottky gate, the applied negatively gate voltage will deplete the barrier and lower the n_s. We assume the Schottky barrier height ϕ_B keeps constant of 1eV. The Figure 5. 8 gives the detailed band diagram at -2.0 V gate bias condition. The conduction band of barrier is lifted up and the potential well is shallower, which lead to less sheet carrier density. As bias keep on increasing to pinch-off voltage, the conduction band in the channel turns to be more flat the potential well can no longer concentrate 2DEG.

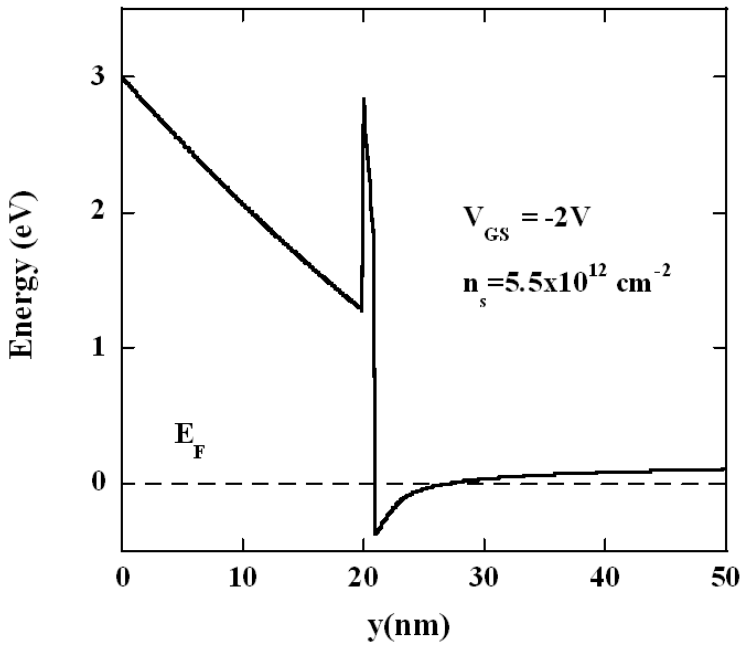


Figure 5. 8 The band diagram for an AlGaN/GaN HFET structure with AlN spacer, when the Schottky gate is negatively biased for -2.0V.

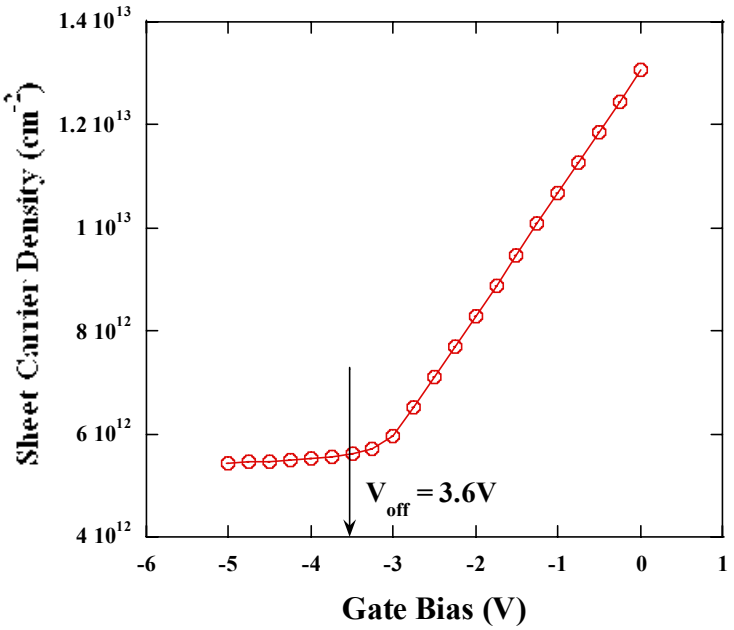
In Figure 5. 9 (a) we show the calculated sheet carrier density on the applied gate voltage. The n_s almost linearly decreased on the gate bias before the channel is pinched off. The pinch-off voltage, which in the figure corresponds to the onset of invariance of n_s, for AlGaN/GaN structure with 1nm AlN spacer is around 3.6 V. It is necessary to mention, although not shown in the figure, that without considering the coupling effect, the pinch-off voltage increase about 4%. With this dependence, one can easily calculate the CV characteristics of gate:

$$C(V) = \frac{qdn_s}{dV}$$

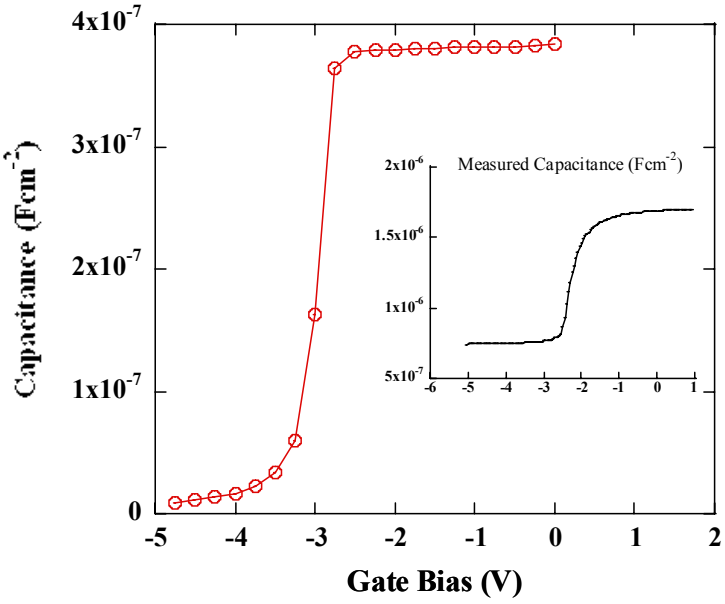
Equation 5. 33

and it is plotted in Figure 5. 9 (b). The measured CV data is also shown in the same figure, which is about 4~6 times larger than the theoretical predication. It may be caused by the error of

effective area, also the measured the capacitance represents the total charges within all layers include traps and defect states while in our calculations we considered only free carriers.



(a)



(b)

Figure 5. 9 In the AlGaN/GaN HFET structure with 1nm AlN spacer, (a) the dependence of sheet carrier density on the applied gate voltage. (b) The calculated and measured capacitance on applied gate voltage.

Once the pinch off voltage is determined, the IV characteristics for a HFET can be expressed as[110]:

$$I_D = \frac{1}{1+\mu V_D / v_s L} \cdot \frac{\mu Z}{L} \cdot \frac{\varepsilon}{d}[(V_G + |V_{off}|)V_D - \frac{V_D^2}{2}]$$

Equation 5. 34

Here the gate length L=1 μm, low field electron mobility μ=1000 cm^2/Vs, saturation velocity v_s=10^{5}m/s. Shown in Figure 5. 10, the maximum source-drain current reaches 680 mA/mm saturated at 2V, which will increase if neglect the coupling effect. But the actual device's DC characteristics, as seen from Chapter 3.2.2, can hardly get close to this level due to

the influences from the Ohmic contact resistance, leakage current, self-heating, etc.

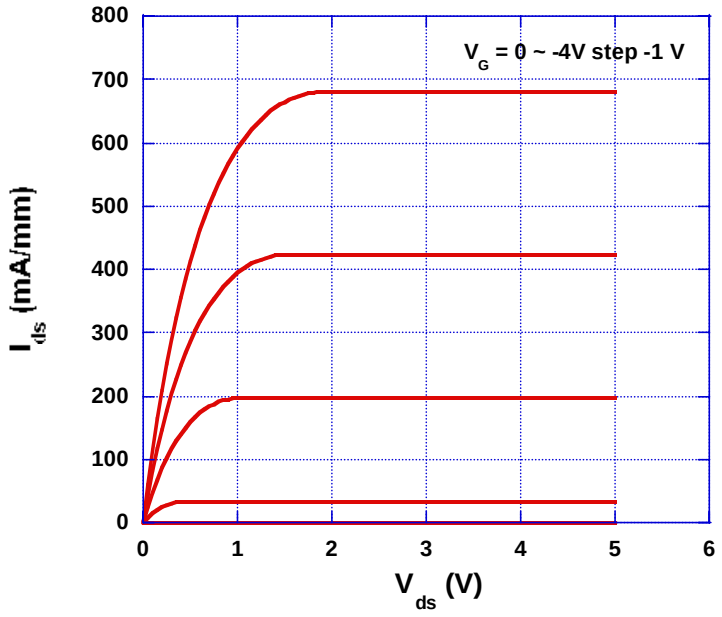


Figure 5. 10 Ideal I-V characteristics for AlGaN/GaN HFET with 1nm AlN spacer.

As an important process accounting for the current dispersion, some preliminary studies on self-heating is presented here as well. The self-heating effect at large drain bias will increase the channel temperature due to the power that dissipated inside the device. It can decrease the carrier mobility and saturation velocities by increasing the electron phonon scattering[132, 133]. As a result, the transconductance and output current will be reduced. In general, the self-heating plays a dominant role at low frequency range account for current dispersion. While at relatively higher frequencies, the dispersion is mainly caused by trapping effect from defects. Relatively slow process the dispersion effect is, though, compared with the microwave input signal, it still significantly affect the device's RF performance by producing the inter-modulations harmonics

in the amplifier application for example[134, 135].

In order to quantify the current dispersion due to the self-heating, basic electrothermal calculation has been applied to Equation 5. 34. Since the self-heating is caused by power dissipated within the device, people often utilize a thermal sub-circuit to characterize[136] the relation between temperature and power. For FET devices, the thermal sub-circuit is shown in Figure 5. 11. The thermal resistance R_{th} denotes for the temperature rising per power applied, whose unit is K/W. The thermal capacitance C_{th} describes the time response of temperature on the given input wave from. Then the static channel temperature would be:

$$T = R_{th} P + T_0$$

Equation 5. 35

Here T_0 is the environment temperature, P is the DC component of power signal $p(t)$.

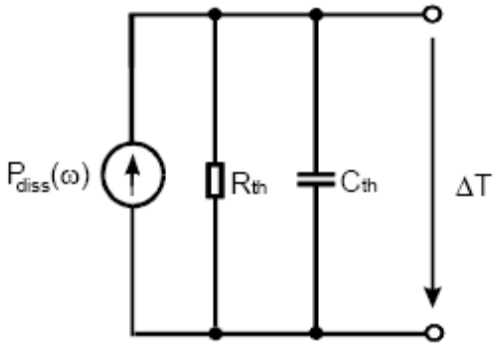


Figure 5. 11 The electrothermal sub-circuit account for self-heating effect.

Thermal resistance has been reported to be related with the substrate for GaN HFET, device dimension and geometry. It can be measured by pulse measurements so that the self-heating effect is eliminated. Typical values for R_{th} on different substrate and device size are listed in Table 5. 1.

R_{th} (K/W)	Reference	Material/Substrate	Gate Dimension
70	137	AlGaN/GaN on Si	0.5 μm ×150 μm
250	136	GaAs pHEMT	4×0.15 μm ×50 μm
45.7	140	AlGaN/GaN on SiC	0.35 μm ×250 μm
123	138	GaAs MESFET	6×0.5 μm ×300 μm
135	139	AlGaN/GaN on Sapphire	2×0.8 μm ×94 μm

Table 5. 1 Comparison of thermal resistance on different device structures.

Many methods have been proposed to describe the change of current on channel temperature. Except Monte Carlo simulation[133], large signal models usually use analytical expression to incorporate the temperature dependent terms into drain current[140]. Other methods include transient thermal model[137] and Laplace heat spread model[141, 139]. Here, I use the following expression to separate the self-heating part from isothermal model from ref.142:

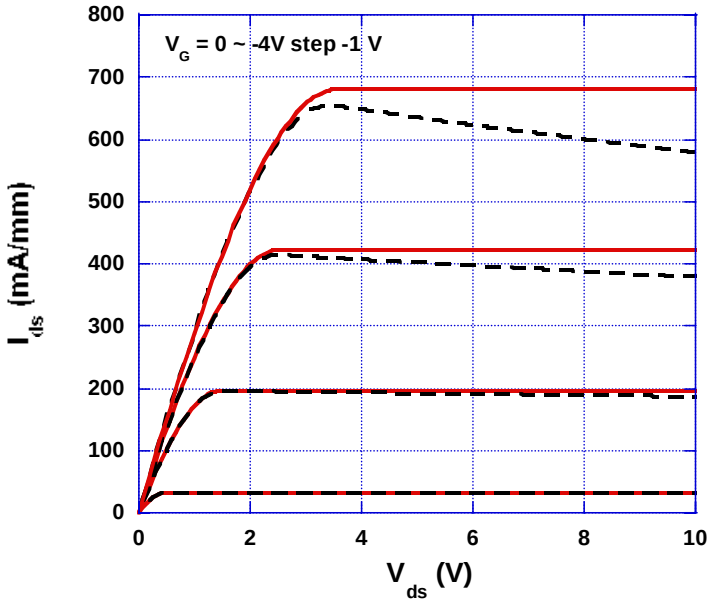
$$I_{DS}(t) = I_{DSO}(t, T_o)[1 - \delta \cdot p(t) * h_{th}(t)]$$

Equation 5. 36

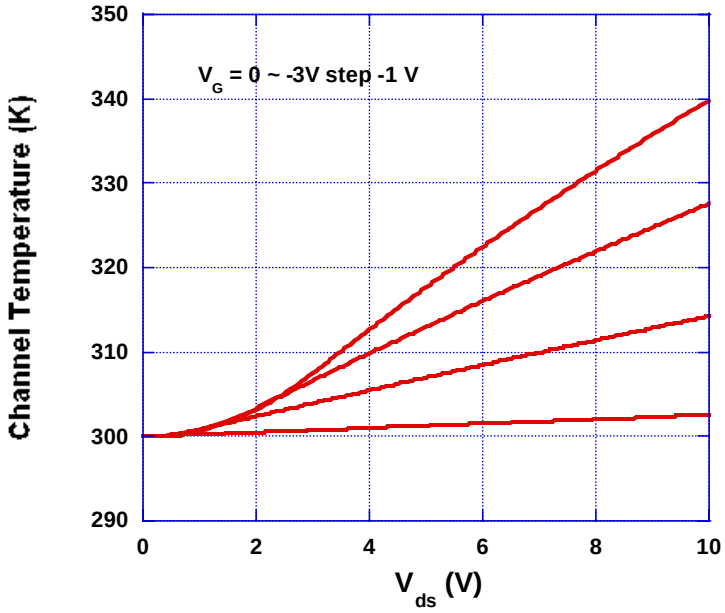
here * denotes for convolution, T_0 is the environment temperature, I_{DSO} is the isothermal current, and $h_{th}(t)$ is the impulse response of the electrothermal sub-circuit.

For I-V characteristics, we assume the source and drain contact resistivity is 1.2 Ωmm, obtained from the TLM measurements states in Chapter 3.1.2. Environment temperature T_0 = 300K. Using $\delta = 0.2\ W^{-1}$ as 142 indicated, R_{th} = 70 K/W, and I_{DSO} is the current model from Equation 5. 34. The calculated I-V characteristics are shown in Figure 5. 12 (a) as the dashed line. After considering the self-heating effect, the apparent collapse on I_{DS} is clearly observed, which is consistent with the measurement data. Figure 5. 12 (b) gives the channel temperature at the corresponding DC conditions. The highest temperature can reach 340 K at about 6W/mm output

power level.



(a)



(b)

Figure 5. 12 For AlGaN/GaN HFET with 1nm AlN spacer, (a) the calculated IV characterization considering accessing resistances (solid line) and self-heating (dash); (b) channel temperature at different bias conditions.

5.4.2 AlInN HFET structures

Similar to AlGaN HFET, lattice matched AlInN barrier structure were modeled. The larger conduction band discontinuity (0.84 eV) between barrier and GaN, along with stronger spontaneous polarization (0.036 C/m^2) will induce higher sheet electron density. The calculated band diagram for 20 nm AlInN barrier structure with 1 nm AlN spacer is shown in Figure 5. 13, along with the carrier distribution. The barrier is doped to 8×10^{17} cm^{-3}, and surface states are still considered as the main resource for the 2DEG.

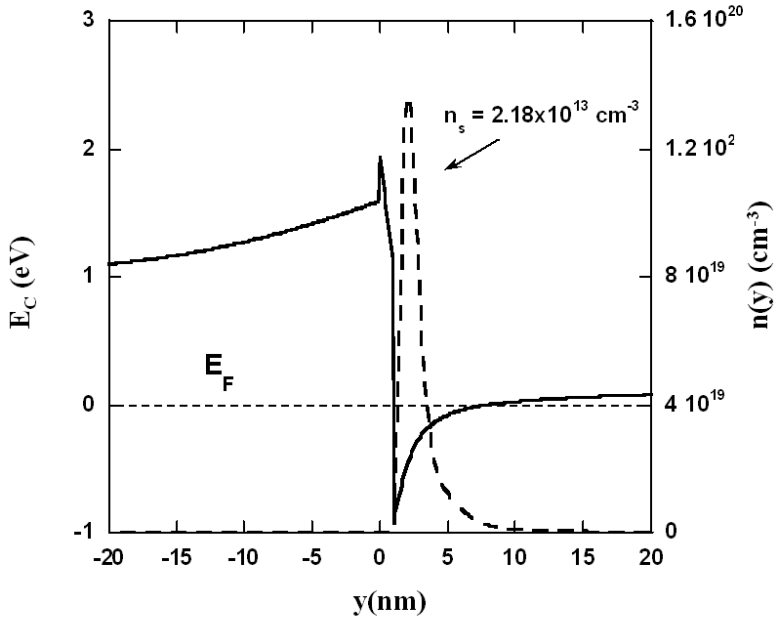
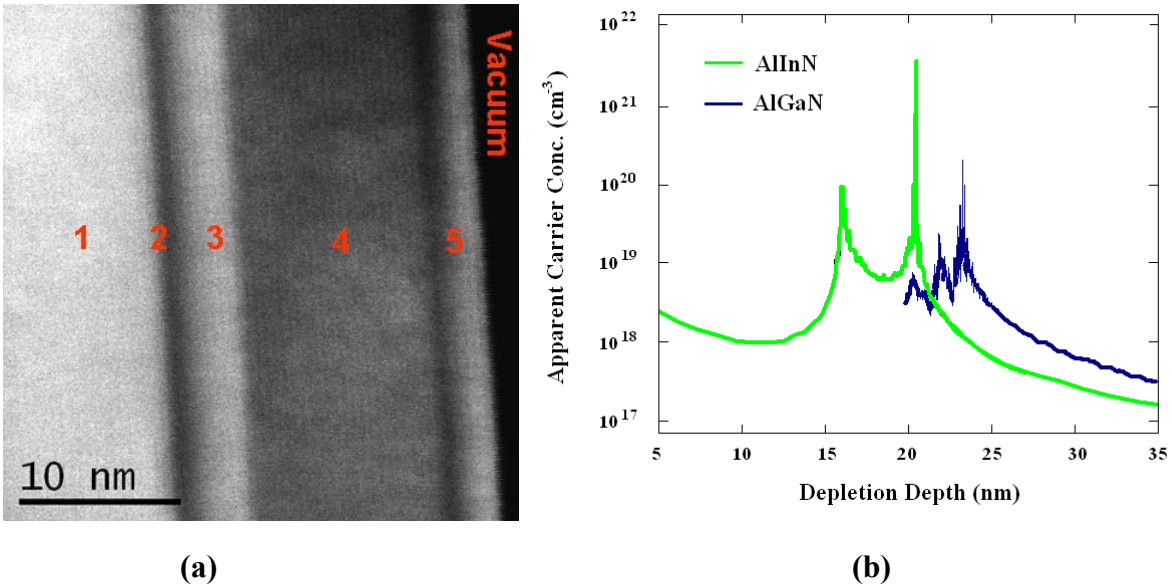


Figure 5. 13 The calculated conduction band diagram and electron distribution for 20 nm AlInN/GaN HFET structure with 1 nm AlN spacer. The total sheet density is 2.56×10^{13} cm^{-2}.

From this Figure, we could see the sheet electron density in AlInN barrier device is much larger than the AlGaN case. The 2DEG has a wider distribution with a channel depth around 10 nm below the interface. AlN still helps to confine the electron within the channel and the first two energy sub-bands are both filled. However, refer to the measured carrier transport properties shown in Chapter 3.2.1, the actual 2DEG density is much smaller than our anticipated value that is nearly twice more. It is possible some structural difference from the ideal situation may exist and therefore alter the distribution of carriers, which need to be confirmed by other means.

In order to reveal the cause for this difference, annular dark-field STEM images were taken on the cross section of an AlInN barrier structure as shown in Figure 5. 14 (a). An extra layer is clearly observed on the top of the AlN spacer. As confirmed by EDX measurements, it is a Ga- rich region with thickness around 4 nm. The formation of this Ga- rich layer is believed to be due to the interruption of growth between the AlN and AlInN layer needed for ramping down the temperature and switching the carrier gas from H_2 to N_2, during which time the GaN inadvertently appears to have been deposited from the residual TMG source within the system. This Ga- rich layer which has a smaller band gap in the barrier can easily trap a high concentration of electrons to form a second channel. The electron profile extracted from CV measurements shows a double-peak distribution in the AlInN sample, while no clear second peak is observed in the AlGaN sample for which the barrier growth interruption period is much shorter.



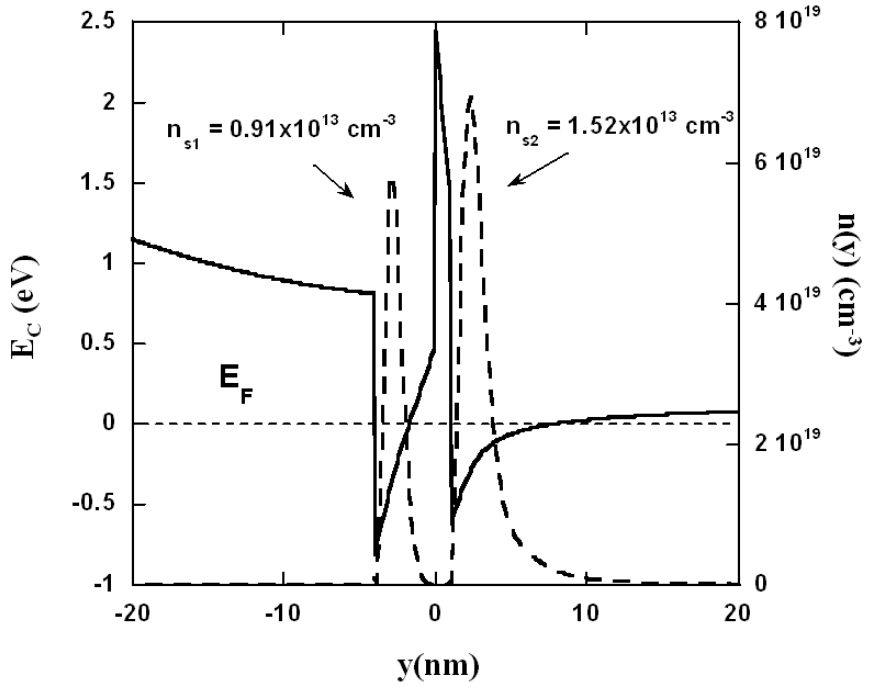
(a) **(b)**

Figure 5. 14. (a). Cross section annular dark-field STEM image for AlInN barrier HFET structure. Each numbered layer is 1) GaN template; 2) AlN spacer; 3) Ga- rich layer; 4) AlInN barrier; 5) GaN cap layer. (b) Carrier profile for AlGaN and AlInN samples calculated from CV measurements.

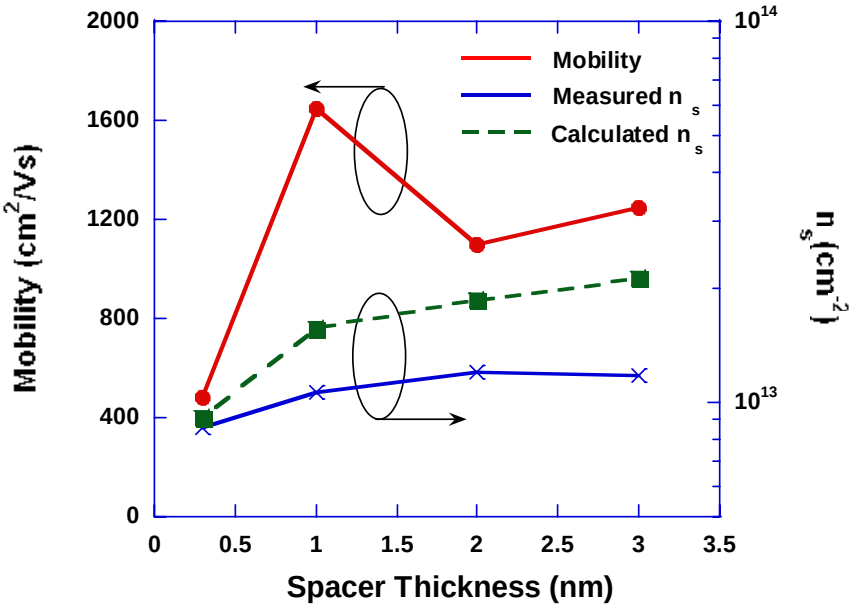
The simulations we performed show that the sheet electron density within the top parallel channel can reach up to 9×10^{12} cm^{-2}, assuming the top channel consists of 4 nm un-doped GaN. The 2DEG density within the real channel is much reduced, as shown in Figure 5. 15 (a). Both channels will contribute to the measured conductivity in the way described by Equation 3.2. It is quite possible the electrons in the top channel have relatively lower mobility, therefore the overall carrier density and mobility are mainly determined by those of the real channel.

In our experiments, we also investigated the influence of the spacer thickness on the carrier transport properties for AlInN barrier cases. As shown in Figure 5. 15 (b), a very thin AlN spacer (0.3 nm) can hardly help to confine 2DEG and thus a relatively lower mobility results. Maximum mobility is obtained when spacer thickness is around 1 nm. The total 2DEG sheet density for various AlN thicknesses is measured at low temperatures, in an effort to exclude the

influence from any non-degenerate parallel channels. The calculated sheet carrier density (determined by n_{s2}) is also plotted in the same figure, which increases with the thicker spacer layer similar to what was reported on AlGaN barrier cases[43, 143]. The experimental carrier density data increases when AlN spacer changes from 0.3 nm to 1 nm, while it hovers around 1.1 ~ 1.2×10^{13} cm^{-2} with >1 nm spacer. As to what may be responsible for the lack of a clear upward trend, it might be possible that it is caused by the Ga- incorporation during the AlN spacer growth, so that the actual barrier height and polarizations for spacer is smaller. Second, although the critical thickness for AlN grown on GaN is not explicitly known with reported figures varying from atomic mono-layer range to a few nm as reported[144, 145], it is true that the spacer quickly relaxes due to the relatively large lattice mismatch. The partial relaxation of the spacer will introduce compressive strain in the AlInN barrier lattice matched to GaN, and the reduction in total polarization then can also cause the lower sheet electron density.



(a)



(b)

Figure 5. 15 (a). Simulated conduction band diagram and carrier distribution for AlInN barrier structure with 4 nm Ga- rich layer on the top of spacer. (b) Measured 2DEG mobility (room temperature) and sheet density (12K) of AlInN samples with 0.3, 1, 2 and 3 nm spacer. The calculated n_{s2} at same structure condition is also plotted in dashed line.

5.5 Two-dimensional modeling

The basic theories for 2D quantum DD modeling have been introduced in Chapter 5.2. Compared with 1D simulation, the self-consistent solution involves more partial differential equations that dramatically boost the complexity of the problem. For simplicity, I made the following treatments and assumptions:

(1) Solve sliced 1D Schrödinger equation

Within the HFET, since the carrier has only confinement along growth direction, it is

reasonable to assume the quantum effects from lateral direction (x) is negligible. Also the dimension of devices over x direction is much larger than the layer thickness. The mesh size Δx is often limited by the Debye length:

$$L_D = \sqrt{\frac{\varepsilon k_B T}{q^2 N_D}}$$

Equation 5. 37

For GaN channel, if background doping is around 10^{16} cm^{-3}, then Debye length is about 120 nm. In my simulation, I choose Δx = 100 nm, and it is large enough to allow us describe the movement of carrier by classic transport theory.

Therefore, the electron density is computed by solving the vertically sliced 1D Schrödinger equation. So the solver developed in the 1D modeling procedure can be re-used.

(2) Assume the electron quasi-Fermi level E_{fn} is x-dependent only

The current conduction within the HFET, as we can imagine, is mainly in lateral direction through the 2DEG channel formed at the hetero-interface. The injection current from the gate into the channel, or the leak current component, is usually very small as seen from the experiments. Therefore at a given x grid point, I assume the E_{fn} is a constant along the y direction.

This assumption helps to shrink the number of unknown E_{fn} variables. Furthermore, it reduces the current equation to one dimensional case. If we denote quasi-Fermi level as $E_{fn}(x)$, then the current density should become a constant unless we take the recombination or the carrier emission/capture process into account:

$$j_n = n_S q\mu \frac{dE_{fn}}{dx} = q\mu \int n(x,y)dy \cdot \frac{dE_{fn}}{dx}$$

Equation 5. 38

Here n_s is the electron sheet density at position x.

(3) Constant carrier mobility

For long channel devices, the electric field within the channel is low so that the carrier mobility is considered as constant. With the increase of field, carrier drift velocity will saturate and is no longer proportional to the electric field. The empirical relationship between velocity and field is:

$$v = \frac{dE_{fn}}{dx} \cdot \frac{\mu}{1 + \mu / v_S \cdot dE_{fn} / dx}$$

Equation 5. 39

Here v_s is the saturation velocity of electron. However, the including of velocity/field dependency into my model will sacrifice the linearity between current density j_n and field dE_{fn}/dx and increase a lot more complexity into the Newton iteration. Therefore, I use constant carrier mobility in the modeling.

(4) Preset potential boundary conditions

In the 2D modeling, Poisson equation become x and y correlated as:

$$\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} = \frac{q}{\varepsilon}(N_D^+ - n)$$

Equation 5. 40

In a given area, to solve a PDE, we need to specify the boundary conditions, or the value of potential along the surrounding border. It is straight forward to define potential at source side as zero and drain side as V_{ds}:

$$\varphi(x=0)=0$$
$$\varphi(x=L_{sd})=V_{ds}$$

Equation 5. 41

The potential at top surface and bottom boundary is hard to determine. Here, I assume there are no surface states or bulk defects to trap charges and alter the potential distribution. Therefore, the potential at these three regions: source to gate (top surface); gate to drain (top surface), and source to drain (bottom boundary) are linearly distributed[146]; see Figure 5. 16 for detail.

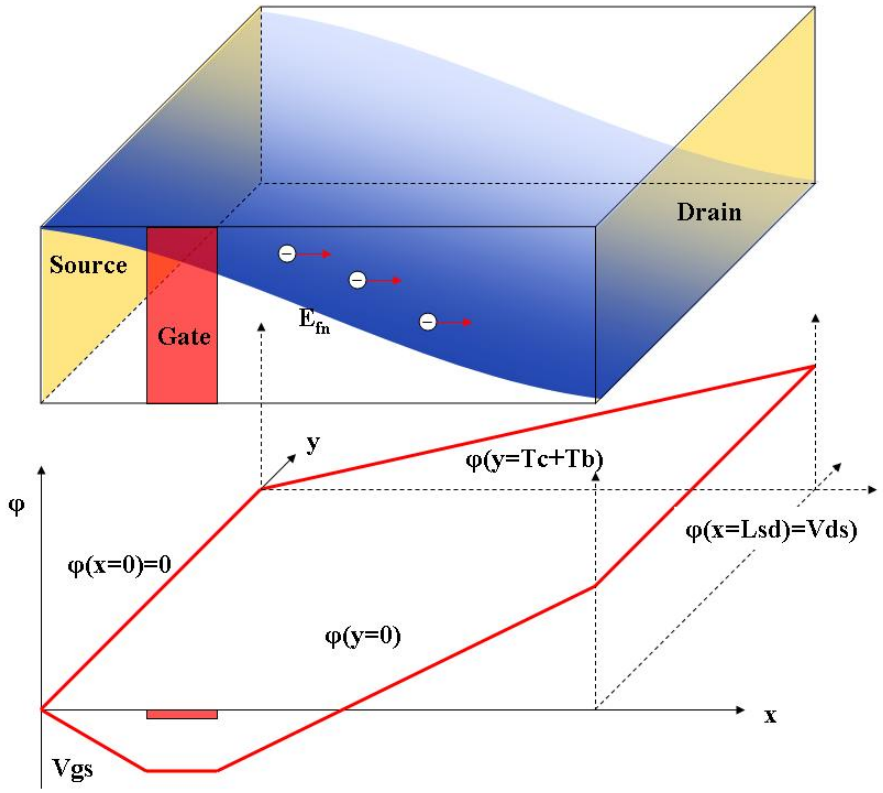


Figure 5. 16 Illustration for the potential boundary conditions.

Some device parameters used for modeling are listed in Table 5. 2

Parameter	Value	Parameter	Value

Lsg	2.0 μm	$Al_xGa_{1-x}N$	x = 30%
Lg	1.0 μm	N_D (barrier)	10^{18} cm^{-3}
Lgd	7.0 μm	N_D (bulk)	10^{16} cm^{-3}
Tb	20 nm	Polarization	$8 \cdot 10^{12}$ cm^{-2}
Tc	50 nm	μ	1000 cm^2/Vs

Table 5. 2 Some parameters used for 2D modeling.

In this model, only Poisson equation is a PDE. Here I use rectangle grids over the cross-section of channel region, with constant mesh size Δx = 100 nm, Δy = 0.5 nm. After discretization, at a given grid point ($x=i\Delta x$, $y=j\Delta y$), the Poisson equation can be rewritten as:

$$\varepsilon(i,j)\times\frac{\varphi(i+1,j)-\varphi(i,j)}{\Delta x^2}-\varepsilon(i-1,j)\times\frac{\varphi(i,j)-\varphi(i-1,j)}{\Delta x^2}+$$
$$\varepsilon(i,j)\times\frac{\varphi(i,j+1)-\varphi(i,j)}{\Delta y^2}-\varepsilon(i,j-1)\times\frac{\varphi(i,j)-\varphi(1,j-1)}{\Delta y^2}=q[N_D^+(i,j)-n(i,j)]$$

Equation 5. 42

The number of the unknown potential variables is (10 μm / 0.1 μm)×(70 nm / 0.5 nm) =14,000; and that number for E_{fn} is 100. Therefore, the size of the Jacobian matrix for Newton iteration algorithm is 14,100×14,100 = 198,810,000. In computer memory, if each data is float point with double precision, the size for one matrix storage would reach 1 Gbyte! It is obvious that the demands for both data storage capacity and computation time on linear algebra operations are very heavy. Without proper fast algorithm, the cost for computation effort is unaffordable.

Fortunately, in most cases, the majority population of the matrix is zero or it is so-called sparse matrix. There are numerous fast algorithms along with optimized data structure to implement the linear algebra operations for sparse matrix.

Generally speaking, the large scale sparse matrix is compressed per row (or column). The linked table structure is used to storage the position of non-zero elements and value. To efficiently condense the table and enable fast search, I employed some random hash functions to better distribute the data, and a rehash technique was provided for quick data indexing[147]. With the optimized data structure, the space occupied by the matrix is very small. The size for Jacobian matrix is usually less than 100K compared with original 1G. A co-coding on Matlab and C++ is implemented so that many functions can be utilized directly from Matlab. The function I take to solve linear system equation $\mathbf{A}x=b$ is Generalized Minimal Residual Method (GMRES). This method approximates the solution by the vector in a Krylov subspace with minimum residuals, and the Arnoldi iteration is used to find this vector[148]. For more detail, please refer to the help documentation for Matlab from Mathworks.

5.6 Two-dimensional modeling results

5.6.1 Cross-section profile

In this section, I will present the simulation results for the cross-section profiles of a basic AlGaN/GaN HFET structure with device geometry listed in Table 5. 2. Assume all the donors are fully ionized, and the Schottky gate has a barrier height of 1.0 eV.

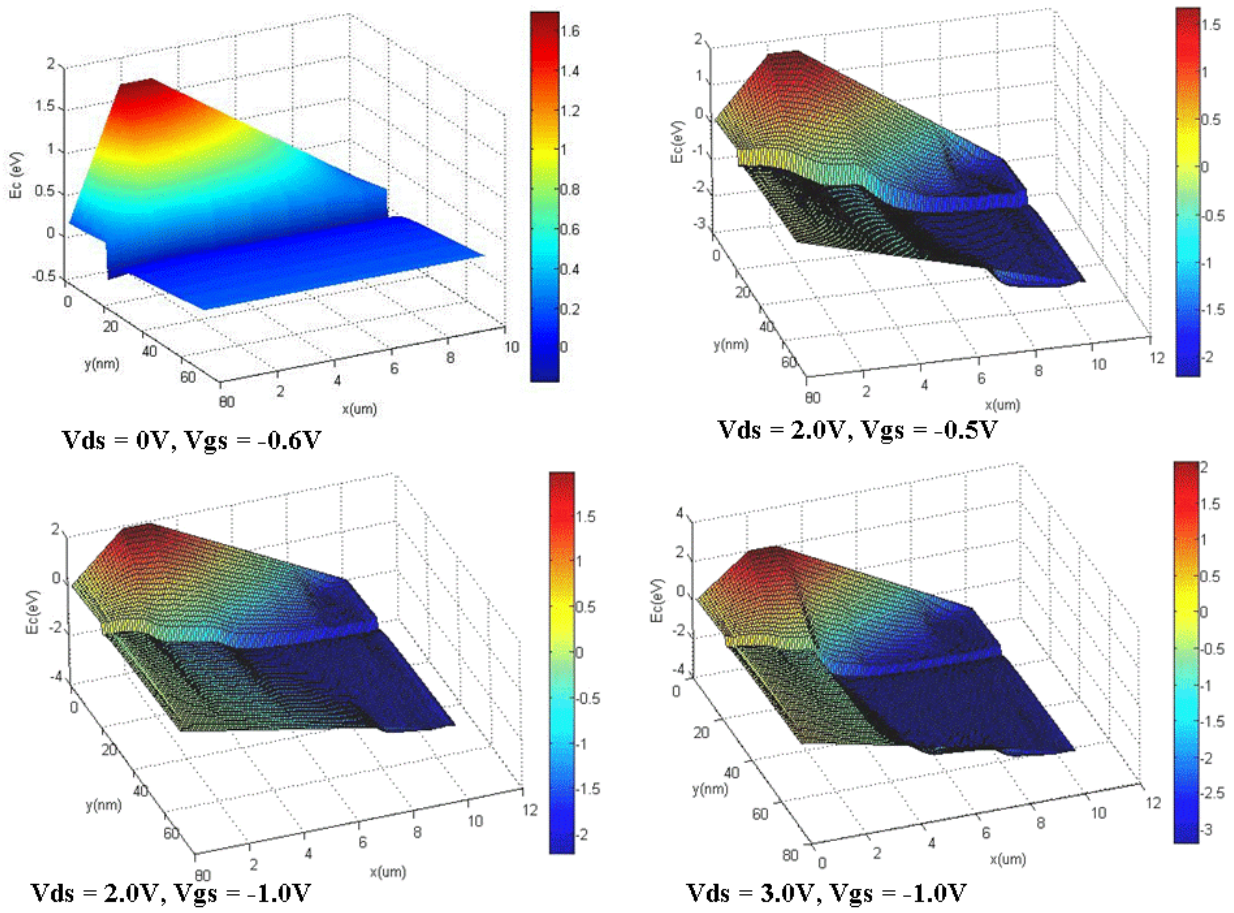


Figure 5. 17 Conduction band distribution at different bias condition.

Figure 5. 17 shows the two-dimensional electron conduction band profile throughout the AlGaN/GaN heterojunction, with different bias conditions. If no source to drain bias is applied, the slice on the conduction band profile is identical to what was obtained from 1D simulation. Once the drain bias is on, 2DEG channel is lifted at the source side to guide the movement of electrons. With the increase of gate pinch voltage, the channel under the gate is raised to hold the carriers travelling from source to drain. The need for high resistivity bulk GaN is also inferred in these pictures. If extra carriers exist in the bulk, it could generate considerable parallel current since the slope of conduction band there is still large.

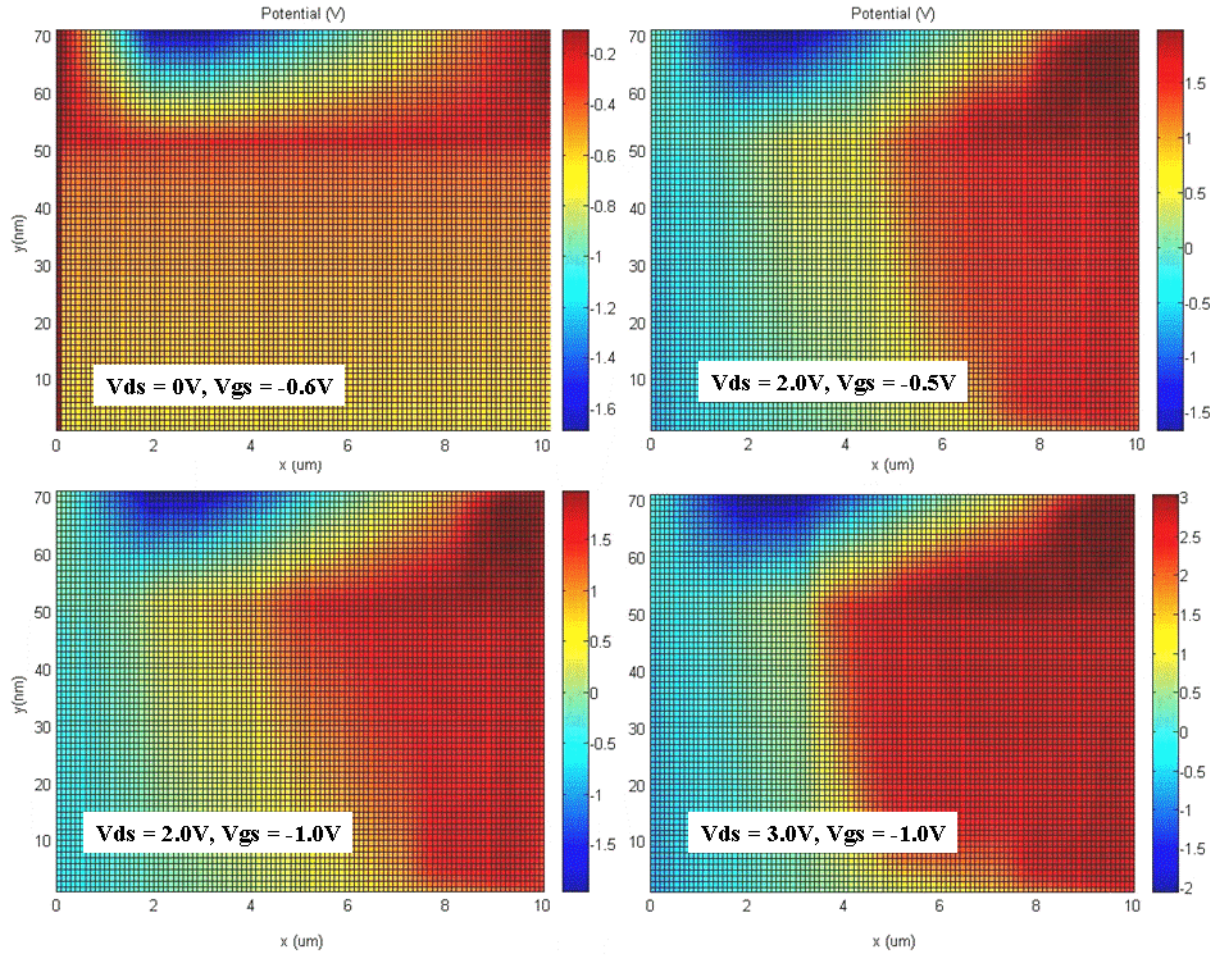


Figure 5. 18 Cross-section potential distribution at different bias condition.

Figure 5. 18 is the cross-section potential profile for the HFET at the same bias conditions. The 2DEG channel tends to stay at the constant potential, while the increase on gate pinch off voltage will break this uniformity. The higher the gate voltage, the deeper the depletion region will be. The increase on drain voltage would also enhance the gradient of potential change near the gate edge. It is clear from in Figure 5. 18 that the electrical field always has a maximum value near the gate edge. The increase of gate or drain bias will push this maximum field position close to the gate, where the breakdown is believed to occur if enough high voltage is applied[149].

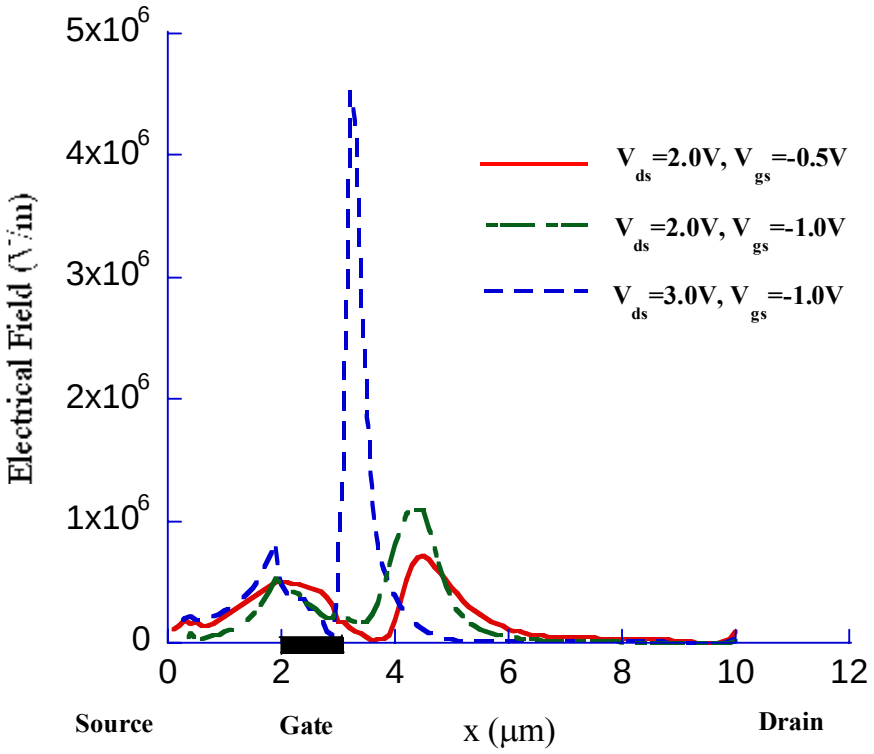


Figure 5. 19 Electrical field in the channel with different bias conditions.

Large gate or drain bias input caused the simulation program failure without approaching reliable convergence. The calculated Jacobian matrix is close to singular, so its inversion is ill-conditioned. Also, from Figure 5. 20, where the calculated IV characterization is plotted, we can see the current shows no saturation tendency. The non-linearity of carrier velocity over electrical field at large bias conditions should be considered to provide better accuracy.

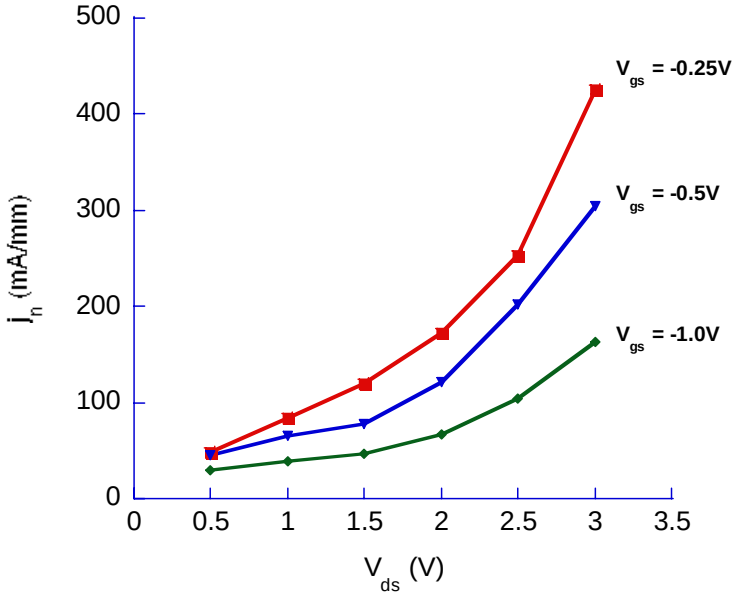


Figure 5. 20 Simulated IV characteristics, drain bias from 0.5 V to 3.0 V, gate bias is -0.25V, -0.5V and -1.0V.

5.6.2 Results from other simulation software

If we look into the commercial two- or three-dimensional device simulators, some industrial CAD software [150, 151] and university-developed applications [152, 153, 154] have been successfully employed for Si-device applications. In contrast to the silicon devices, where both process and device level simulation tools form a continuous virtual workbench from material analysis to chip design, III-V simulation mainly is still focused on device physics.

APSYS from Crosslight Inc is a general purpose 2D finite element analysis and modeling software especially designed for compound semiconductor devices (with silicon as the special case) in simulating their electronic and optoelectronic performances. The energy band structure is calculated by solving Schrödinger equation using 8-band **k.p** model within a high precision finite differences grid. For GaN devices, polarization charges are incorporated during the

simulation. The kernel of APSYS simulator also solves the non-equilibrium drift-diffusion equations. The tunneling current transport mechanism through the quantum well and barrier is also modeled. Three different carrier recombination mechanisms have been implemented, namely direct-, SRH- and Auger-recombination, which can be used for LED and LD device simulations.

For a specified semiconductor, we must first build up the micro files to specify the material properties such as mobility, saturation velocity, electron affinity, refractive index, and thermal conductivity. For example, the mobility model for GaN we used here is doping and field dependent:

$$\mu_n(N) = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + (N / N_r)^{\alpha}}$$

Equation 5. 43

$$\mu_n(F) = \frac{\mu_0}{1 + \mu_0 F / v_{sat}}$$

Equation 5. 44

Where v_{sat} is the saturation velocity, N_r is the reference doping concentration, μ_0, μ_d, a are predefined parameters. The polarization that induces sheet carriers has to be treated as the bonded interface charge existing at the bottom of barrier. Some of the parameters used are listed below:

Parameter	Value	Comment
ε	9.5	Dielectric constant
χ	4.07	Affinity
v_{sat}	1.91×10^7 cm/s	Electron saturation velocity

α	0.66	Used in Equation 5.34
$\mu_{\min}$	$295\times(300/T)^{1.5}$ cm^2/Vs	Minimum mobility
$\mu_{\max}$	$1461\times(300/T)^{1.5}$ cm^2/Vs	Maximum mobility
N_r	10^{17} cm^{-3}	Reference density
A_n	10^{-32} s	Electron Auger coefficient
τ	10^{-10} s	Electron life time
P_{SP}	8×10^{12} cm^{-2}	Spontaneous polarization
P_{PZ}	4×10^{12} cm^{-2}	Piezoelectric polarization

Table 5. 3 Some parameters defined in the micro file of APSYS for the HFET simulation.

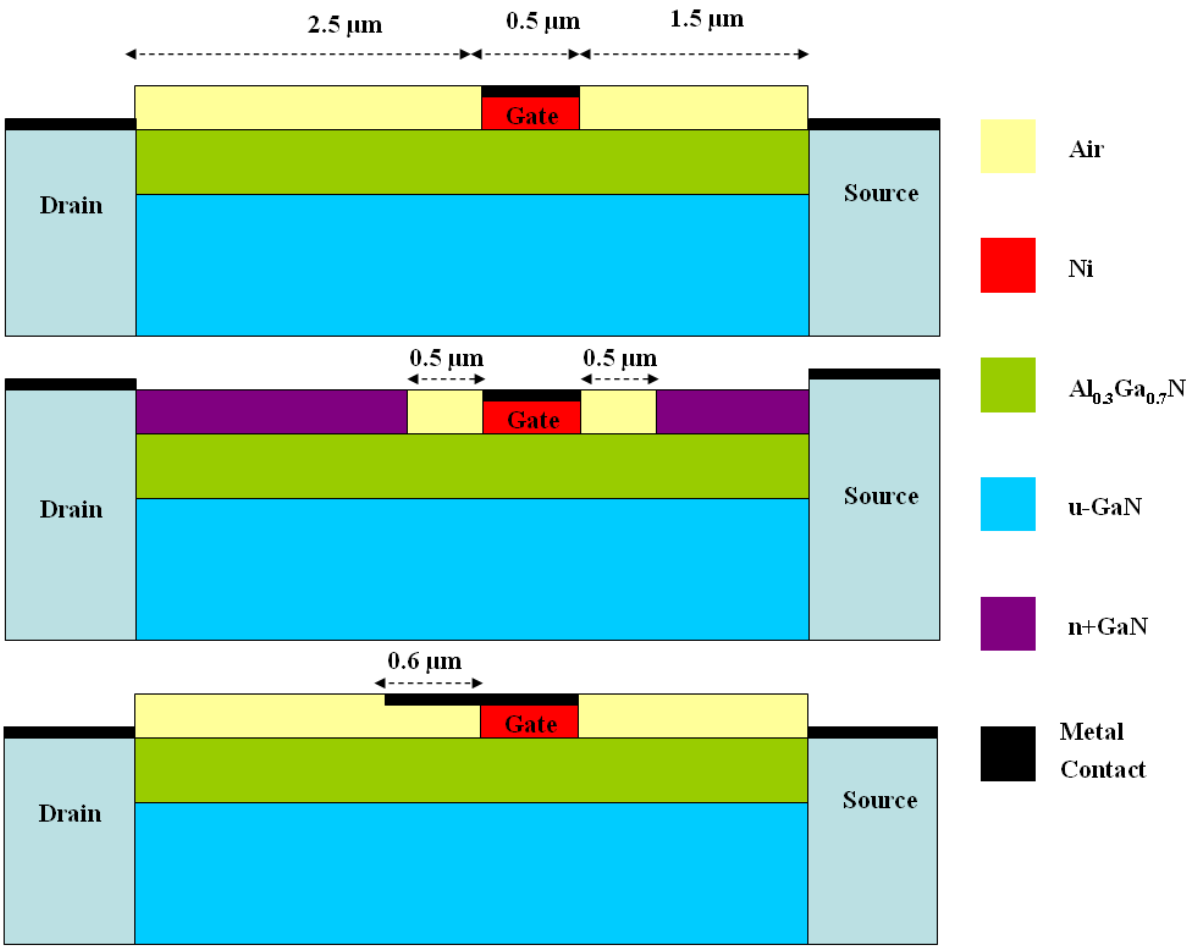
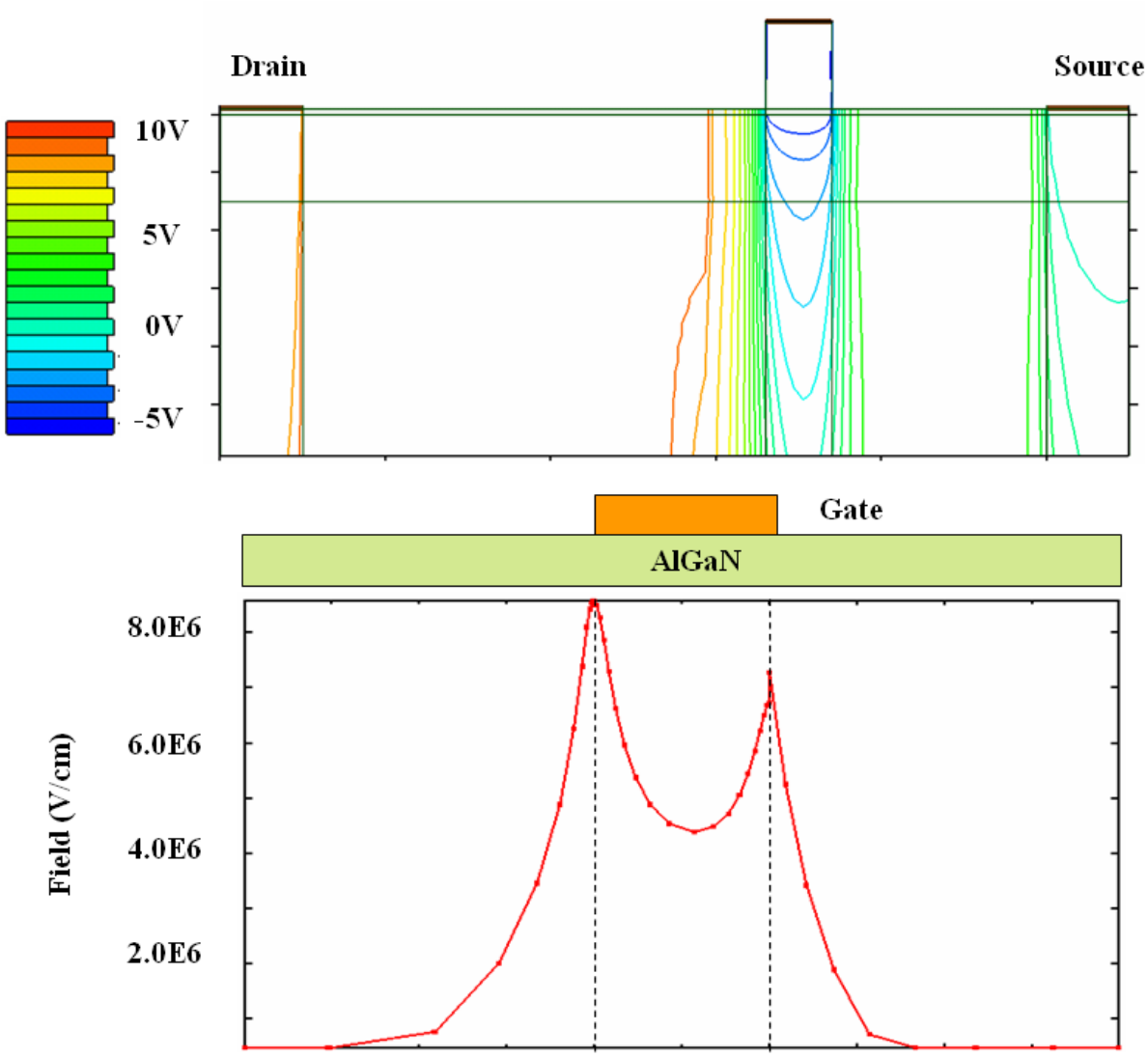
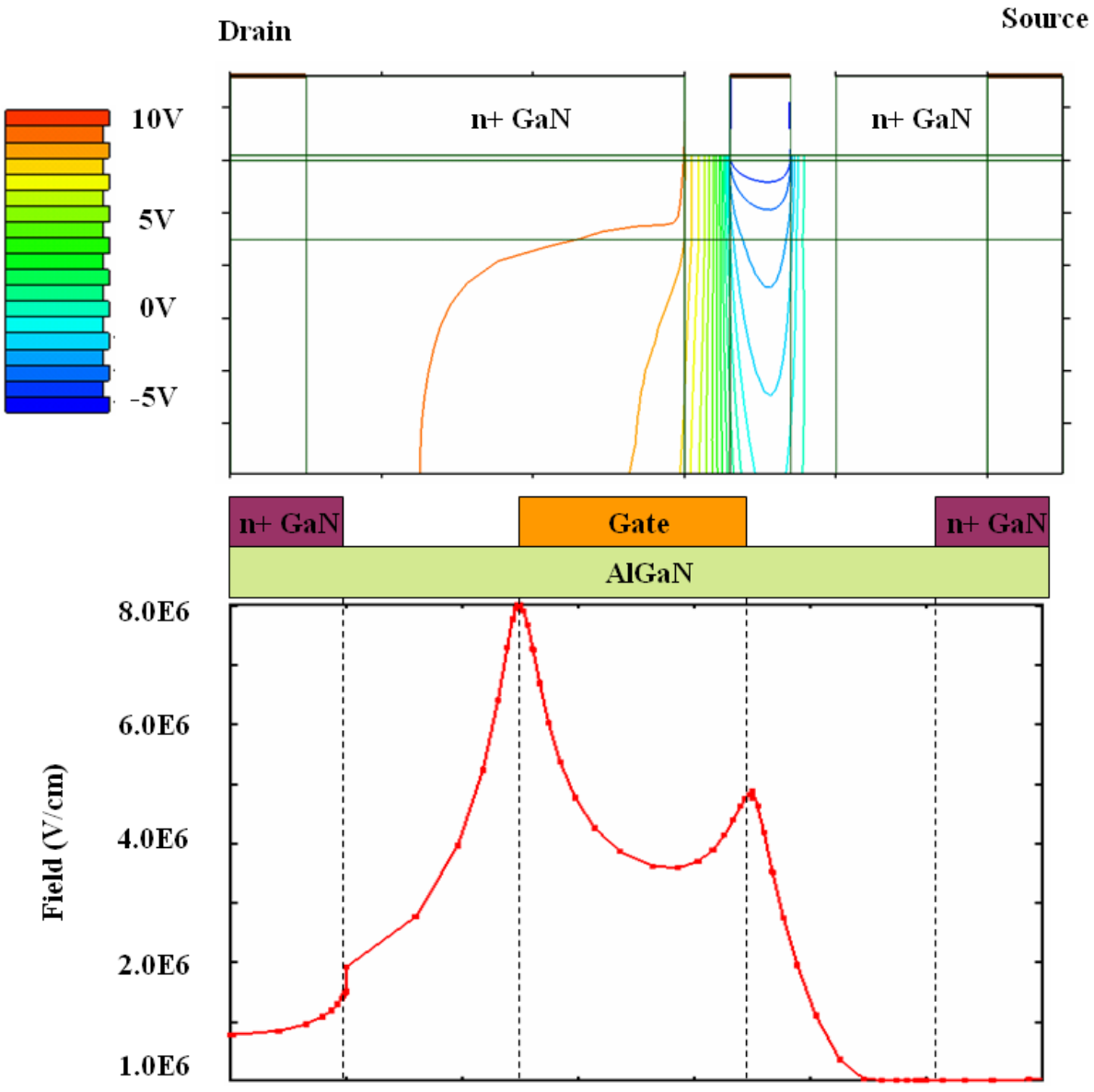


Figure 5. 21 Device structures and dimensions used in the APSYS simulation.

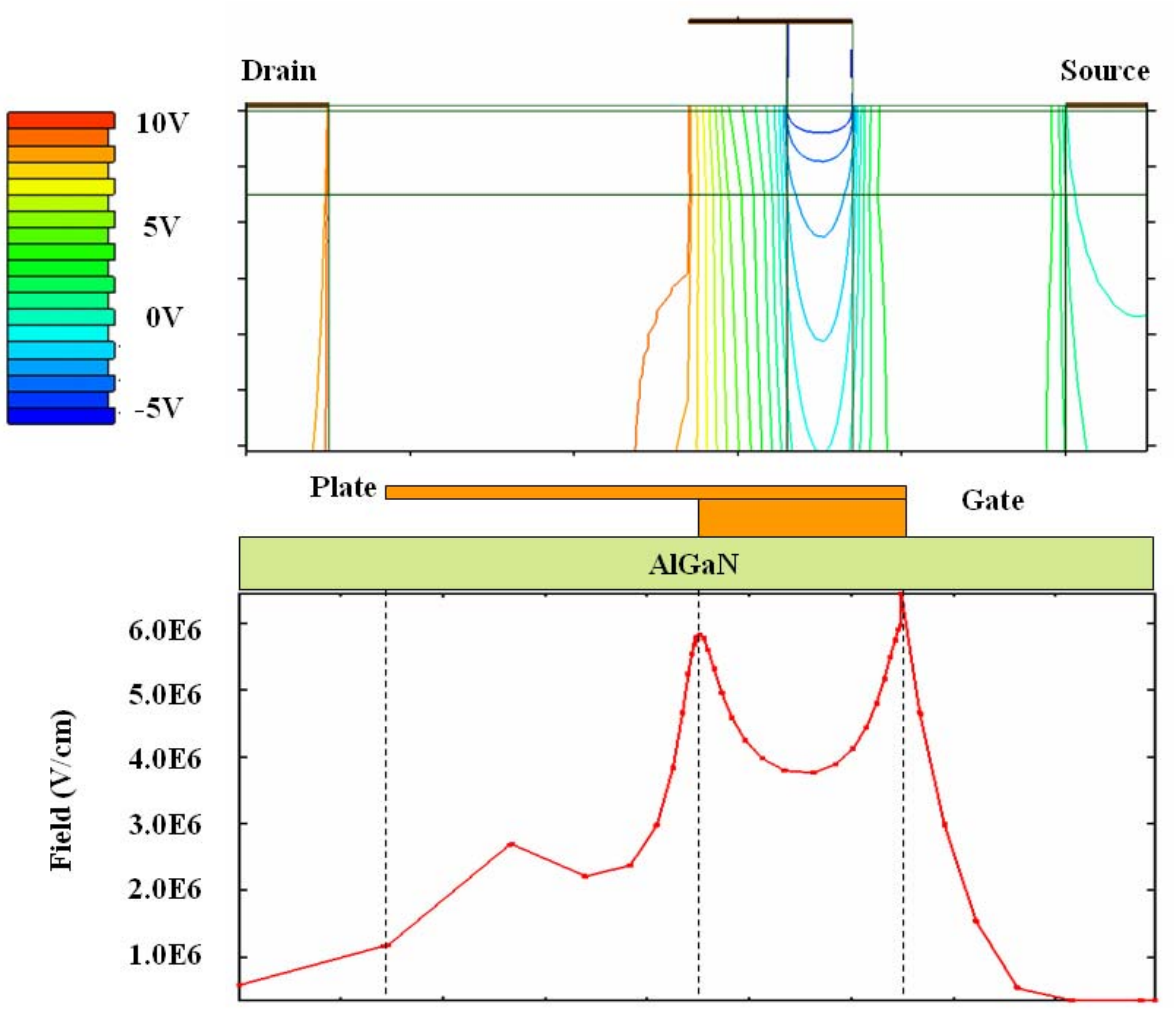
Three different kind of device structures are simulated based on AlGaN/GaN structure: conventional HFET, HFET with field plat and recess gate HFET. The cross-section device geometries are illustrated in Figure 5. 21. The AlGaN barrier thickness is 25 nm and the gate length is 0.5µm, and channel length is 4.5µm. For the n+ cap recess gate HFET, the barrier is un-doped and the n+ GaN is 30 nm thick with 10^{18} cm^{-3} doping. For the field plate HFET, the plate is extended to the drain side with the length of 0.6µm. All devices are biased under V_{DS} = 10V, V_{GS}=-5V. The simulated potential and field distribution for each device are shown in Figure 5. 22.


Drain
Source
10V
5V
0V
-5V
Gate
AlGaN
8.0E6
6.0E6
4.0E6
2.0E6
Field (V/cm)

(a)


Drain
Source
10V
5V
0V
-5V
n+ GaN
n+ GaN
n+ GaN
Gate
n+ GaN
AlGaN
8.0E6
6.0E6
4.0E6
2.0E6
1.0E6
Field (V/cm)

(b)



(c)

Figure 5. 22 The potential contour and field distribution along the AlGaN/GaN interface for (a) conventional HFET; (b) n+ cap recess gate HFET; (c) HFET with field plate under V_{DS} = 10V, V_{GS}=-5V bias.

It can be observed from the potential contour figures that, due to the existence of 2DEG, the electrical field distribution is very concentrated near the gate edge. For the conventional HFET structure, the maximum field exists at the gate edge toward the drain side reaching 8.5×10^6 V/cm, which stress the material to a considerable extent and easily cause break down to fail the device. The recess gate device structure doesn't show much help in reducing this field,

while the field at the gate-source side reduces a little. The HFET with field plate structure, as seen from the simulation results, efficiently helps to dispense the contour line near the gate edge. The maximum field at the 2DEG channel decreases to 6.0×10^6 V/cm, which is about 29% lower than the conventional structure.

Chapter 6 Conclusions

6.1 Summaries

The GaN HFET device growth, fabrication, characterization, and modeling have been investigated extensively in this work. The process development and optimization for both AlGaN and AlInN barrier devices have been experimented to achieve low defect density, high carrier mobility and large output power. Regarding the device characterization and modeling, both equivalent circuit analysis and quantum drift-diffusion modeling are studied. The simulations based can provide us plenty of useful information especially for the microwave application and device structure optimization.

To exploit the potential of GaN and related alloy on device application, high quality epitaxial film is a must. The device operation poses strict requirements on insulate buffer layer, making many prevalent growth techniques like epitaxial lateral overgrowth inapplicable for HFET. Here, we utilize semi-insulating AlN layer on Sapphire substrate as the buffer, and optimize the growth for the GaN layer on top of it. In summary, the growth of GaN involves three steps, namely the nucleation, the epi-growth and the channel growth. It is beneficial to use the growth conditions at the nucleation stage that favor the formation of large, isolated GaN islands so that the density of edge-type dislocations are lowered. The next step is carried out with high growth rate to reduce the background doping preventing the formation of parallel conduction path. The top 300 nm GaN layer that serves as the electron channel is grown at high pressure to reduce the incorporation on deep level impurities and enhance the mobility of 2DEG. Very thin AlN spacer has been verified to better confine the carriers, reducing the alloy scattering and improve the mobility. The spacer thickness is critical and the optimum number is about 1 nm. For barrier

layer, AlGaN is deposited at high temperature, for which the Al composition is controlled mainly by V/III ratio. On the other hand, the AlInN growth requires precisely control on temperature to achieve the exact Indium composition and the lattice-matched $Al_{0.82}In_{0.18}N$ barrier structure was successfully grown.

High carrier transport performance has been observed on both kinds of barrier structures, generally with the mobility of 1,200 cm^2/Vs @ 300K and 10,000 cm^2/Vs @ 12K for AlGaN barrier; and 1,500 cm^2/Vs @ 300K and 20,000 cm^2/Vs @ 12K for AlInN barrier respectively. The total sheet carrier density is around $1\sim2\times10^{13}$ cm^{-2}, depending on the doping, composition and barrier thickness. The HFET devices, which are fabricated using the optimized processes, have achieved the good DC to RF performances. The AlInN device has larger saturation current up to 800 mA/mm and higher transconductance about 220 mS/mm. We believe the reliability of AlInN HFET is superior since the reduction of the stress within the barrier. The RF performance of both type of devices are similar, with the highest cut-off frequency around 20 GHz.

Furthermore, new device structures have been experimented including recess-gate HFET and MISHFET with various gate insulators. The recess-gate device is caped with n+ doped GaN. Two different process techniques have been tested: selectively dry etch method and the SiO_2 masked re-growth method. However, the DC characteristics of recess-gate device didn't show much advantage over the conventional one. The MISHFET structures, on the other hand, have the improved the DC and RF characteristics. With the help of SiO_2, Si_3N_4, ZrO_2 and PZT gate insulators, gate leakage current was significantly reduced, enabling the device to work under enhanced mode. The improvement on RF performance of MIS structure, we believed is due to the passivation to block the surface states, especially with the high dielectric constant dielectrics.

Device behaviors are thoroughly simulated. This research was carried out on circuit level category and device physics category. Various small signal device models have been well established for Si and GaAs transistors, but not quite applicable for GaN HFET yet due to the high contact resistances and defect related dispersion effects. An 18-element equivalent model was proposed in this work, and the circuit parameters were extracted by various means including cold-FET measurements and hot-FET calculations. A hybrid extraction method has been developed combining the parasitic capacitances extracted from cold pinch-off measurements, and the rest of the parameters obtained from the optimization procedure based on the working-bias measurement data. The average S-parameter simulation error is around 5% over the frequency range from 2GHz to 20GHz. This method was also validated with the initial value independence and the multi-bias measurements. Therefore, we believe it is more suitable for the GaN HFET small signal modeling.

The quantum drift-diffusion modeling of HFET, on the other hand, was based on band structure of GaN material and description of current transport mechanism. A solver to give self-consistent solution of Schrödinger-Poisson equations has been developed. The influences from interface polarizations, surface donor states and electromechanical coupling effects have been included during the modeling. The one-dimensional study on different heterojunction strucutres is verified via experiments, especially on AlInN HFET. Furthermore, basic IV and CV characteristics can be calculated, considering the recess resistance and self-heating effects. Two-dimensional simulation was also developed, fulfilling numerical calculation on partial differential Schrödinger-Poisson equations, drift-diffusion current, and current continuity equations. Visualizing the potential and field distribution cross-sectional profiles over the device channel region can be drawn from this modeling. We also compared various device structures

including the conventional, the recess-gate, and the field-plate HFET using APSYS software. It shows that field-plate structure is more promising in effectively dispensing the highly concentrated field around the gate edge that may fail the device by breakdown.

6.2 Future works

The improvement on the reliability of GaN HFET is the foremost important task for the realization of commercial application, which requires efforts on both process side and design side. With the availability the free-standing GaN bulk materials, the research trend is moving toward to the homo-epitaxy GaN growth on those substrate, which undoubtedly could provide much better GaN layer for HFET. Therefore, the improvement of the device performances relies mainly on the quality of different barrier layers or novel device structures.

The lattice-matched AlInN barrier is a good candidate in obtaining higher standard of device reliability, as stated in our research. However, the existence of Ga-rich layer on the top of spacer will separate the 2DEG into two channels and significantly lower the sheet carrier density. The formation of this extra layer is probably caused by the parasitic deposition of GaN during the long temperature-ramping down. In order to eliminate this parasitic layer, modifications to our current growth scheme are needed. On the other hand, the incorporation of Indium into the device structures is another efficient way to improve the device performance. The InGaN channel device structures is one of the candidates to provide higher sheet electron concentration and better 2DEG confinement[155]. The typical room temperature mobility of $In_{0.04}Ga_{0.96}N$ channel heterojunction was found to be around 800~1100 cm^2/Vs, still having much room to improve. The effort may need to focus on the reduction of interface roughness[156] and in-plane localization effect due to the Indium segregation[157]. The trace amount incorporation of Indium into the spacer or barrier layer might be also a help, as often used in GaAs devices. The main advantage of the

In-doping is to improve the spacer/barrier crystalline quality and interfacial abruptness of the heterojunction. Also the In-doping growth scheme avoids the drastic change in temperature and carrier gas, which help to maintain the optimized growth conditions on the known structures.

As for the device process, it has been reported that the field plate structure can help to enhance the output power density, the breakdown voltage and power adding efficiency, as confirmed also from our simulations. We need to set-up the fabrication procedures for the field plate device structures, which may involve optimization on the e-beam lithography. Furthermore, a more systematic study on the recess-gate HFET devices is needed. The selective dry etch conditions that we tested so far deteriorate the I-V characterization, and further optimization can be exerted on different plasma combination, reduced etch power, and post etch treatments including KOH, HCl solutions or N_2 plasma .

In order to provide precise description on DC to RF range behavior of the device, the large signal modeling for GaN HFET is the only way. If the amplitude of input signal is increased considerably, it will shift the quiescent operating point of the transistor and the output drain current no longer changes linearly. Many changes on nowadays large signal modeling methods have to be implemented for GaN devices accounting for the dispersion effects. As for the drift diffusion modeling on GaN devices, some simplifications and assumptions I currently build can be substituted to incorporate better descriptions on the carrier transport behavior and on the charged defects. Besides, implementation on the fast parallel computing algorithm is also important for more precise simulation.

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