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Electron – phonon interaction in multiple channel GaN based HFETs: Heat management optimization

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Electron – phonon interaction in multiple channel GaN based HFETs: Heat management optimization

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at Virginia Commonwealth University.

by

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Dedicated to all those diverse people from many different nations
that helps me along my journey.

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Abstract

ELECTRON - PHONON INTERACTION IN MULTIPLE CHANNEL GaN BASED HFETS: HEAT MANAGEMENT OPTIMIZATION

By Romualdo Alejandro Ferreyra Dr.

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at Virginia Commonwealth University.

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Director: Hadis Morkoç Ph.D.
Founders Professor, Dep. of Electrical and Computer Engineering

New power applications for managing increasingly higher power levels require that more heat be removed from the power transistor channel. Conventional treatments for heat dissipation do not take into account the conversion of excess electron energy into longitudinal optical (LO) phonons, whose associated heat is stored in the channel unless such LO phonons decay into longitudinal acoustic (LA) phonons via a Ridley path. A two dimensional electron gas (2DEG) density of $\sim 5\times10^{12}cm^{-2}$ in the channel results in a strong plasmon–LO phonon coupling (resonance) and a minimum LO phonon lifetime is experimentally observed, implying fast heat removal from the channel. Therefore, it is desirable to shift the resonance condition to higher 2DEG densities, and thereby higher power levels. The more convenient way to attain the latter is by widening the 2DEG density profile via heterostructure engineering, i.e. by using multiple channel heterostructures. A single channel heterostructure (GaN/AlN/AlGaN), a basic heterostructure used to obtain a 2DEG, exhibits a resonance condition at low 2DEG densities ($\sim 0.65\times10^{12}$ cm^{-2}). Successful widening of the 2DEG density

profile was predicted by simulation results for two types of multiple (Al)GaN channel heterostructures, i.e. coupled channel GaN/AlN/GaN/AlN/AlGaN and dual channel GaN/AlGaN/AlN/AlGaN. Because of a reduction of carrier confinement, it is experimentally observed that control of the channel is moderate in the case of dual channel heterostructures. On the other hand, carrier confinement provides a better control of the channel in coupled channel heterostructures. Furthermore, unlike in a dual channel heterostructure, alloy scattering does not affect carrier transport properties, which results in a higher cut-off frequency. It was found experimentally that the coupled channel heterostructure successfully reaches resonance condition at a 2DEG density that is 23% higher than in a single channel heterostructure. Multiple channel heterostructures therefore provide a convenient way to shift the plasmon-LO phonon resonance to higher 2DEG densities. However, in our grown heterostructures, high power levels under optimal channel working conditions and minimum heat accumulation, all desirable benefits for the development of high power transistors, were only observed in coupled channel heterostructures.

Chapter 1. Introduction

Traditional applications in the range of RF, microwave, and millimeter frequencies for telecommunication systems, wireless infrastructure (base stations), and high performance military electronics compel devices with incessant demand for superior performance; low noise figure (NF), reasonable gain at frequencies exceeding 100 GHz, and management of increased power levels. In order to satisfy applications requirements, in the last three decades, a good deal of effort was invested in the development of new device architectures and in the search for new semiconductors. Because of limitations in the realm of Si for high frequencies applications and because of the lack of gate quality dielectrics in other semiconductor families, heterostructure field effect transistors (HFET) and no metal-oxide-semiconductor field-effect transistors (MOSFET) are used for high performance transistors.

Initial FETs implemented in non-conventional Si technology, were of the metal-semiconductor (MESFET) type. MESFETs are based on semiconductors with high quality surfaces like GaAs, InP, and SiC. Later on, modulation-doped FETs (MODFET) emerged as an option to overcome MESFETs limitations; because of the doping levels requirements and proximity of the gate with respect to the conducting channel in short channel devices for high speed applications. Early MODFETs were based on GaAs and then on SiGe and InP. When based on GaN, MODFET are usually called HFETs (in Europe and Asia are also mistakenly known as high electron mobility transistors (HEMTs)) and for the compound semiconductors they are usually based on i.e. AlGaN, InAlN, and GaN. HFETs exhibit relative large low-field mobility, large maximum electron velocities (at high critical electric fields), and large electron concentrations, which are required characteristics for high-performance FETs.

AlGaAs/InGaAs-based pseudomorphic MODFET characterized by low noise, high gain, and reasonable high power handling capabilities at high frequencies used to dominate the radio frequency (RF) marketplace. However, because GaAs-MODFETs power output is relatively low, high radio frequency power levels used to be only achieved by means of power combining schemes which increase not only hardware/infrastructure complexity, but also costs. GaN-based HFET resolved these issues by providing high power at high frequencies. Electrical properties, large bandgap (3.42 V), large dielectric breakdown electric field (3-5 × 10^6 Vcm^{-1}), and good electron transport properties (~1400 cm^2 V^{-1} S^{-1} experimental at 300K), specially at room temperature, are the relevant characteristics of GaN which make of GaN a suitable semiconductor material for high frequency, high power, and high temperature applications. Record power densities levels (see Table 1.1), unthinkable some years ago, were already achieved thanks to the development of GaN technology. From Table 1.1 we can see that the highest power density (PD) levels are attained when HFET on SiC substrates. And which is consistent with the thermal conductivity of the material, 4.5 Wcm K^{-1}, the highest among the substrates used for RF power transistors. Therefore, using substrates with high thermal conductivity and assuming heat sink attached to the substrate has a thermal resistant zero (ideal case), heat removal from the device is limited by the heat transfer along the path from the FET channel through the device structure down to the substrate. In a HFET the active part, the main component, is the channel where a two dimensional electron gas (2DEG) is formed. See Figure 3.6 for a description of GaN-HFET and location of the 2DEG.

At high electric field conditions, under which power transistors perform most of the time, electron gain energy; increases its temperature and start to transfer energy to the lattice (hot electron). Effects of hot electrons are more prominent underneath and at the drain side of the gate where the electric field is more intense (see Figure 3.6). And at high power working conditions occur heat accumulation aggravated by the built-up of phonon (a unit of

vibrational energy that arises from oscillating atoms within a crystal) which generate a non-equilibrium distribution, in this case, of longitudinal optical (LO) phonons (hot phonons) inside of the 2DEG channel.

Table 1.1. Semiconductor materials used for power transistors. Cutoff frequency (f_T), power gain (Gain), power-added efficiency (PAE), and power dissipation (PD) performed by GaN-based HFETs

Material	E_{crit}	$k(300K)$	f_T	Gain	PAE	PD
	$MVcm^{-1}$	$Wcm^{-1}K^{-1}$	GHz	dB	%	Wmm^{-1}
GaAs[1]	0.4	0.46	3.8	12	50	0.4
Si[2]	0.3	1.5	14	7	30	3
GaN[3]	3.3	>1.5	10	3	40	9.4
SiC[4]	3	4.5	10	9	44	16.7

Hot phonons persist in the 2DEG channel until they decay into acoustic phonons (APs), removing the heat from the 2DEG channel. 2DEG in a GaN system is formed by mobile electrons provided, mainly, by the ohmic contacts. Therefore, hot electron and hot phonon effects are not screened by impurity scattering in GaN 2DEG channel.

One of the most important carrier-phonon scattering mechanisms in semiconductors is the carrier-electric polarization field, due to the relative displacement of positive and negative ions. In polar semiconductors and in particular in low-defect polar GaN material system, carrier scattering is governed by the polar-optical-phonon (POP) scattering mechanism and it is referred to as the Fröhlich interaction. Because of the Fröhlich interaction, emission and absorption of LO phonons by hot electrons perform the most relevant role in terms of heat generation at high electric fields.

On other hand, it was observed, experimentally, a carrier density dependence of hot phonon lifetime [5]–[10]. Phonon lifetime minimum occurs when the frequency, ω_p, of longitudinal oscillation of the free electron gas (plasmon) in the channel match LO phonon frequency (resonance). Strong resonance happens at a 2DEG density of 0.8-1.1 × 10^{13} cm^2, equivalent to ~1x10^{19} cm^3. Where 2D and 3D densities are related by a "form factor," correlated with the way in which the channel widens the carrier density profile. Channel widening depends on the heterostructure in which it is formed.

Because in bulk GaN resonance happens around ~1x10^{19} cm^3 and in order to achieve higher power levels under resonance conditions, the heterostructure should wide the carrier density profile in such a way that 3D carrier density maximum is ~1×10^{19} cm^3 and 2DEG density is as high as possible. Then, hot phonons emitted by hot electrons decay very fast and therefore a minimum of TO and LA phonons are launched. Due to that LA phonons are in charge of the heat removal from the channel, under resonance working conditions, minimum dissipation and fast decay of the heat conditions are attained. Efficient heat management will let device work at higher power levels. And owing to the hot phonon fast decay, hot phonon effects are expected to be the lowest, increasing device reliability.

This thesis aims to evaluate heterostructure designs that may drive to ***plasmon - hot phonon resonance conditions toward higher carrier densities and to estimate the reduction on heat dissipation under resonance conditions***

Chapter 2. Motivation

Heat removal from a power transistor junction has been a complication since early days of solid state power electronics. Usually, heat management on a power transistor is characterized by the thermal figure of merit, maximum junction temperature. Maximum junction temperature is defined as the highest temperature at a semiconductor electronic device still is functional. A number of factors i.e. temperature effects, p-n junction leakage, thermionic leakage, and carrier mobility just to mention a few, limit the high-temperature operation of semiconductor electronic devices.

Regarding temperature effects, more precisely, when the intrinsic carrier concentration defined as

$$n_i \propto T^{3/2} e^{\left(-\mathrm{E_g}/k\mathrm{T}\right)},$$

where E_g is the band gap energy, k is the Boltzmann constant and T the absolute temperature, becomes equal to typical doping level (either intentional or unintentional), 1×10^{15} cm^{-3} at 267°C for Si, 3.9×10^{7} cm^{-3} at 427°C for 4H-SiC [11] , and 1×10^{12} cm^{-3} at 700°C for GaN[12] (where the donor concentration of an unintentionally doped GaN and 4H-SiC layers is 1×10^{16} cm^{-3} at room temperature) the development of mesoplasmas has been observed [13].

Mesoplasma creates current filaments that have very high current density, leading to destructive failure in semiconductors[11]. This phenomenon is less likely in SiC and even much less likely in GaN, mainly, because $Eg_{Si} < Eg_{SiC} < Eg_{GaN}$. Then for unintentionally doped semiconductors, intrinsic carrier concentration determined by the thermal generation of electron-holes pairs across the energy band gap imposes a fundamental limit to the junction temperature.

With a maximum junction temperature of 150°C [14], the performance of power transistors based on Si technology rely strongly on high performance cooling systems. The advent of III-Nitride semiconductors brought relief to this stringent condition, extending the maximum junction temperature up to 300°C [15]. However, new power applications, inquire for managing of constantly increasing higher power levels.

In a simplistic one dimensional (1D) heat diffusion model, where the only variable is the temperature, yet conceptually correct. The temperature differential between ambient temperature and device temperature can be written as

$$\Delta T = T_{\mathrm{j}} - T_{\mathrm{ca}} = \left(\frac{W}{\kappa A} + \Theta_{\mathrm{ca}}\right) P\mathrm{D},$$

where ΔT is the temperature difference between the maximum junction temperature T_{j} and the case temperature T_{ca}, W is the distance from the junction to the case, κ is the thermal conductivity of the semiconductor material, A is the area of heat source (assumed to be spatially uniform to allow the use of 1D model), Θ_{ca} is the thermal resistance of the case to the ambient, and finally $P\mathrm{D}$ is the dissipated electrical power, which is represented, for instance, by the subtraction of RF power-out from DC power-in in a radio frequency circuit (see Figure 2.1).

In a one-dimensional problem where the temperature is the only variable, the difference between the device and the ambient temperature under steady-state conditions is determined by the product of the total device to ambient thermal resistivity and the total power that must be dissipated by the device. The very simplistic of Figure 2.1 and even more complex heat flow removal models for power devices do not take into account, properly, the fundamental process through which heat is removed from semiconductor channel.

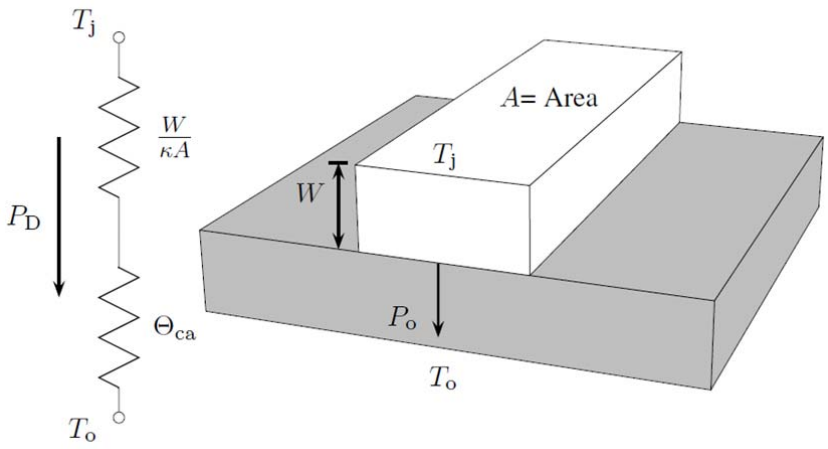


Figure 2.1 One dimensional heat model. White area, A,is the heat source. Gray part represents the device case, heat sink.

Selection of materials for power devices usually is determined by the thermal conductivity parameter, κ . Thermal conductivity is a diffusion process, in which the heat flow, $Q = \kappa \frac{dT}{dx}$, is driven by gradient of temperature. κ is majorly constituted by two components. One owing the phonon conduction (lattice), κ_L , and the second, κ_e , due to the free-carrier (electron) conduction. Contribution of κ_e to the total thermal conductivity is quite small, specially, at high temperatures (>300K). Then, electron contribution to the heat conduction can be discharged in our case, because we are interested in the conduction mechanism at high temperatures. And the total thermal conductivity can be taken as κ_L , that is, $\kappa \approx \kappa_L$. The lattice contribution to the heat conductivity is realized by diffusion and scattering of phonons (such as phonon-to-phonon, phonon-to-defects, phonon-to-carriers, boundaries, and surfaces). At high temperature, phonon-to-phonon is the dominant scattering process, resulting in a reduction of the mean free path of the phonon. And a monotonically drop of κ as 1/T is observed as the temperature increases. Thermal conductivity values at room temperature for GaAs, Si, GaN, and SiC can be found in Table 1.1. Observing at the thermal conductivity, κ , column we can see that SiC and GaN are best suitable for heat conduction.

Low values of κ fosters heat accumulation in the channel with side effects; reduction of carrier mobility and carrier velocity. What, fortunately, prevent thermal-runaway. Heat source temperature is determined by Joule effect, i.e. input DC power minus RF power extracted. Joule effect manifests itself as heat owing to the relaxation of the electron kinetic energy. Relaxation is dominant by electron-lattice inelastic scattering mechanisms. Then Joule heating results in phonon (LO-phonon) emission, and may lead to sensible heating[16]. The higher the device efficiency the lower the heat needs to be removed from the channel.

The described above is the conventional manner to consider heat dissipation. In which, the heat transfer from the heat source to the lattice is dissipated via longitudinal acoustic phonons without taking into account the conversion of hot electron energy excess into LO phonons.

The aforementioned conversion is the genesis of the heat generation in GaN-based HFET. Generation that if could be suppressed an improved heat management can be attained. And that is the topic of this thesis.

The organization of this thesis is as follow. In the chapter Background is introduced all basic concepts; hot electron, hot phonon, phonons in GaN, plasmon, their interaction and their relation with the generation and transport of heat. Also, a description of the different ways in which a carrier density profile may be widened is exhibited.

In the chapter Review a description of the standard HFET is presented. And a revision of HFET performance reported in the literature is given. The aim here is to show that in standard HFET, in the context of plasmon-hot phonon resonance, optimal working condition occur at low power levels.

Then preluding the experimental work, the methods and approach utilized for the design, simulation, and growth of the heterostructures and the fabrication and characterization of the devices are exposed in the chapter Methods and approach.

Following results on the performance of implemented heterostructures are presented in the chapter Experimental results. Conclusions from the work carried out are presented in the chapter Conclusions. Ending the thesis, guide lines for further investigation are provided in the chapter Future work.

Chapter 3. Background

GaN and related nitrides being direct and large band gap materials led themselves to a variety of electronic and optoelectronic applications. Advantages associated with a large band gap include relatively high breakdown voltages, ability to sustain large electric fields, low noise generation, and high temperature and high power operation. Reasonable low-field mobility, large satellite energy separation, and high phonon frequency are among the other attributes. A high thermal conductivity, large electrical breakdown fields, and resistance to hostile environments also support the III-Nitrides as a true material of choice for device applications. In this work we make focus on power applications therefore high current level at high electric field. In other words, the related with high field transport is the indicated physics and is the topic of the next section.

3.1 High Field Transport in nitrides

Ensemble Monte Carlo simulations have been the popular tool to theoretically investigate the steady-state electron transport in nitrides. In particular, the steady-state velocity-field characteristics have been determined for AlN ([17], [18]), GaN ([17], [19]–[23]), and InN ([24], [25]). These reports show that the drift velocity initially increases with the applied electric field to reach a maximum and decreases with further increase in the field strength. The intervalley electron transfer plays a dominant role at high electric fields leading to a strongly inverted electron distribution and to a large negative differential resistance (NDR). Not that credible experimental confirmation of intervalley scattering is still pending. The reduction in the drift velocities was attributed to transfer of electrons from the high-mobility Γ-valley to the low-mobility satellite X-valley. The onset electric field and peak drift velocities, however, show some disparity among the reported calculations due to the variety of the degree of approximation and used physical constants of the materials. A typical velocity-field characteristic for bulk III-nitrides at room temperature is shown in Figure 3.1 along with the well-studied GaAs data used to test the author's Monte Carlo model. For the doping concentration being set to 10^{17} cm^{-3}, InN has the highest steady-state peak drift velocity; 4.2×10^{7} cm/s at an electric field of 65 kV/cm. In the case of GaN and AlN, steady-state peak drift velocities are rather low and occur at larger electric fields; 2.9×10^{7} cm/s at 140 kV/cm for GaN and 1.7×10^{7} cm/s at 450 kV/cm for AlN.

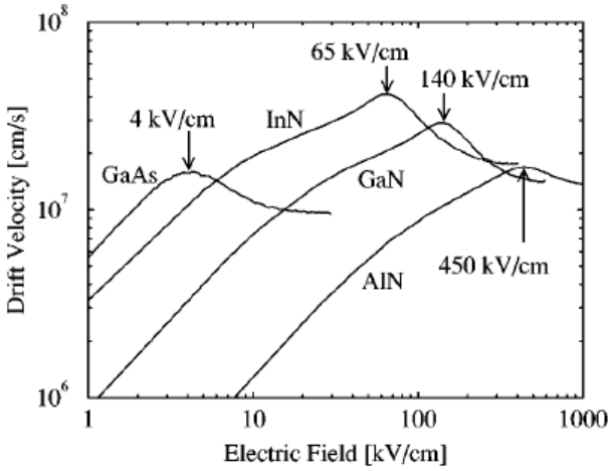


Figure 3.1 The velocity–field characteristics associated with wurtzite GaN, InN, AlN, and zincblende GaAs. In all cases, the temperature was set to 300K and the doping concentration was set to 10^{17} cm^{-3}. The critical fields at which the peak drift velocity is achieved for each velocity–field characteristic are clearly marked: 140 kV/cm for GaN, 65 kV/cm for InN, 450 kV/cm for AlN, and 4 kV/cm for GaAs. After [26].

Another interesting aspect of electron transport in III-nitrides is its transient behavior, which is relevant to short channel devices with dimensions smaller than 0.2 μm where a significant overshoot is expected to occur in the electron velocity over the steady state drift velocity. Transient electron transport and velocity overshoot in both wurtzite and zincblende GaN, InN, and AlN were studied theoretically by a number of groups. Foutz et al. [26] employed both Monte Carlo simulations and one dimensional energy-momentum balance techniques. They used a three-valley model for the conduction band by taking the main scattering mechanisms, such as ionized impurity, polar optical phonon, acoustic phonon through deformation potential and piezoelectric, and intervalley scatterings into account.

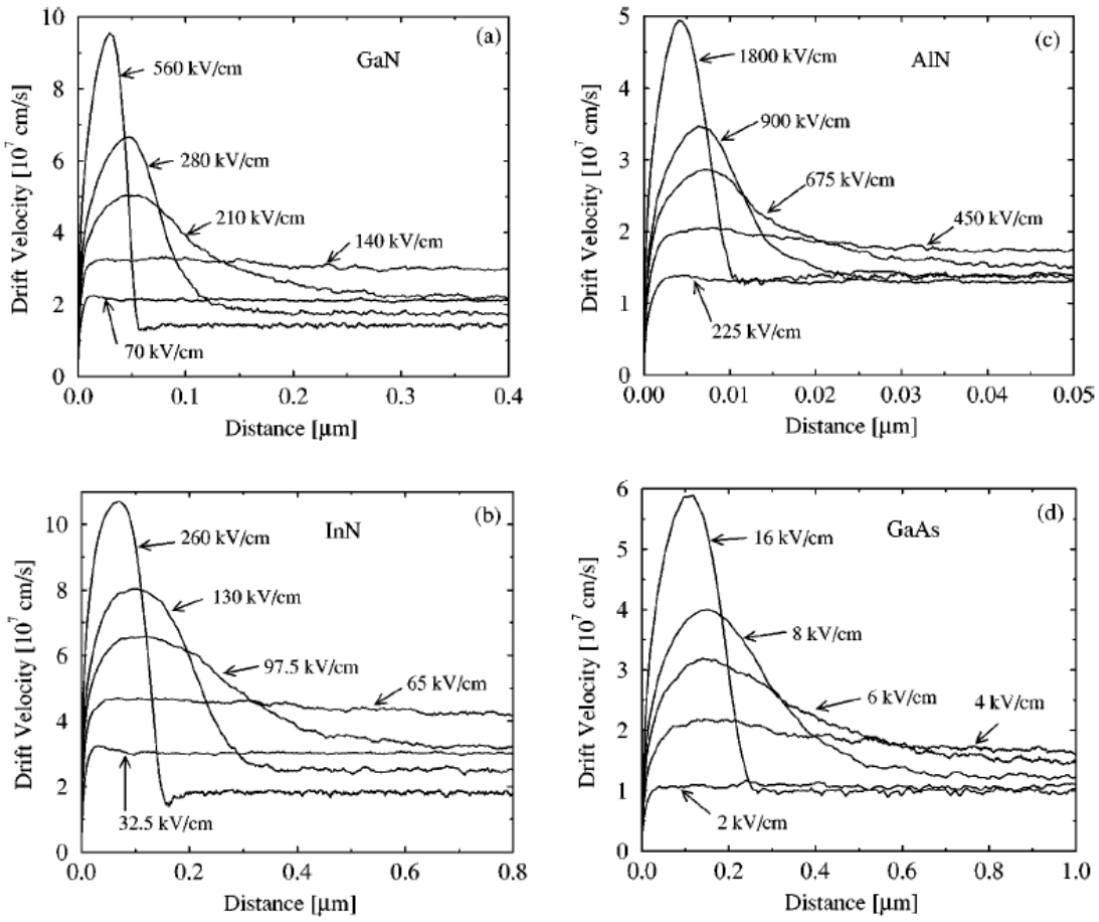


Figure 3.2 The average electron velocity as a function of the displacement for various applied fields for the cases of (a) GaN, (b) InN, (c) AlN, and (d) GaAs. In all cases, we have assumed an initial zero-field electron distribution, a crystal temperature of 300 K, and a doping concentration of 10^{17} cm^{-3}. After [26].

In particular, they examined how electrons, initially in equilibrium, respond to the instant application of a constant electric field. Figure 3.2 shows the average velocity of the electrons in AlN, GaN, and InN as a function of distance. According to their calculation, electron velocity overshoot only occurs when the electric field exceeds a certain critical value unique to each material and it lasts over a certain distance dependent on applied field. These critical fields are points where the highest steady-state peak drift velocities are achieved and being reported as 65 kV/cm, 140 kV/cm, and 450 kV/cm with corresponding peak velocities of

2.9×10^7 cm/s, 1.7×10^7 cm/s, and 1.6×10^7 cm/s for InN, GaN, and AlN, respectively. Among them InN exhibits the highest peak overshoot velocity on the order of 10^8 cm/s at 260 kV/cm and the longest overshoot relaxation distance on the order of 0.8 μm at 65 kV/cm. To optimize the device performance by only minimizing the transit time over a given distance is prevented by a tradeoff between the peak overshoot velocity and distance taken to achieve steady state. The upper bound for the cutoff frequency of InN and GaN based HFETs benefits from larger applied fields and accompanying large velocity overshoot when the gate length is less than 0.3 μm in GaN and 0.6 μm in InN based devices. However, all measured cutoff frequencies are gate length dependent and well below these expectations indicating that devices operate in the steady-state regime and other effects, such as real-space transfer, should also be considered. On the other hand, there is some controversy in the reports related to the onset of velocity overshoot in nitride semiconductors. For example, Rodrigues et al. [27] reported overshoot onsets at 10 kV/cm in InN, 20 kV/cm in GaN, and 60 kV/cm in AlN by using a theoretical model based on a nonlinear quantum kinetic theory, which compares the relation between the carriers' relaxation rate of momentum and energy. Experimental investigations of the transient transport in III-Nitrides are very limited and few results are reported by using different techniques. Wraback et al. [28] employed a femtosecond time-resolved electro-absorption technique to study the transient electron velocity overshoot for transport in the AlGaN/GaN heterojunction p-i-n photodiode structures. It has been reported that electron velocity overshoot can be observable at electric fields as low as 105 kV/cm. The velocity overshoot increases with electric fields up to ~320 kV/cm with a peak velocity of 7.25×10^7 cm/s relaxing within the first 0.2 ps after photoexcitation. The increase in electron transit time across the device and the decrease in peak velocity overshoot with increasing field beyond 320 kV/cm are attributed to a negative differential resistivity region of the steady-state velocity-field characteristic in this high field range. Collazo et al. [29] used

another experimental technique based on the measurement of the energy distribution of electrons which were extracted into vacuum through a semi-transparent Au electrode, after their transport through intrinsic AlN heteroepitaxial films using an electron spectrometer. They observed electron velocity overshoot as high as five times the saturation velocity and a transient length of less than 80 nm at the field of 510 kV/cm. In order to design an electronic device that is expected to operate at high power and high frequency, one could consider harnessing velocity overshoot in III-Nitrides semiconductor heterojunctions. However, the strong coupling between hot electrons and LO phonons appear to limit the velocity attainable by electrons, being dependent on the LO phonon decay time. A systematic investigation of InN, GaN, AlN and their alloys as a function of various parameters in dynamics mode would be very beneficial for development of higher performance, next generation electronic and optoelectronic devices.

Because the gate length of the HFETs investigated in this thesis are around 1μm, we do not expect observe ballistic conduction. Furthermore, in all cases applied electric field is lower than 50 KV/cm which means drift electron velocity is well below the saturation. And we are safe considering that drift velocity increase with the applied electric field.

3.2 Hot electrons

The electron transport in semiconductors, including nitrides, can be considered at low and high electric field conditions. **(*i*)** At sufficiently low electric fields, the energy gained by the electrons from the applied electric field is small compared to the thermal energy of electrons, and therefore, the energy distribution of electrons is unaffected by such a low electric field. Since the scattering rates determining the electron mobility depend on the electron distribution function, electron mobility remains independent of the applied electric field, and Ohm's law is obeyed. **(*ii*)** When the electric field is increased to a point where the energy

gained by electrons from the external field is no longer negligible compared to the thermal energy of the electron, the electron distribution function changes significantly from its equilibrium value. These electrons become hot electrons characterized by an electron temperature larger than the lattice temperature.

When the electron transport is caused by an electric field, electrons are continuously supplied with energy from the source of the electric field at a rate $J \times$ E (where J is current density and E is the electric field). It would appear that the total energy of the electron system should increase indefinitely. Actually, this not happens as the gain of energy is balanced by transfer of energy to the lattice atoms via collisions. Electron are scattered by the lattice by emitting or absorbing a phonon. The lattice absorbs energy from the electron when phonon is emitted and it delivers energy to the electron when a phonon is absorbed. In the absence of electric field the absorption and emission processes are balanced and there is not transfer of energy from the electron system to the lattice system or vice versa. It means in fact that the temperature, thermodynamic coefficient determining transfer of energy from one system to another, of the electron (value of temperature in the electron distribution function) and the lattice system (temperature in the phonon occupation number) are identical.

Under the presence of an external electric field, the energy of the electron system start to increase and electrons start to emit more phonons than they absorb. In other words, there is a net transfer of energy from the electron system to the lattice system. This mean the temperature of the electron system, T_e, is larger than the lattice temperature, T_L. And energy transfer rate increases as the difference between T_e and T_L augment. This situation keeps until a new equilibrium is reached. The latter is set when the difference between the electron and the lattice temperature is such that the rate of gain of energy of the electron from the electric source is balance by the rate of loss of energy to the lattice atoms.

3.3 Hot phonons

From the preceding discussion, when $T_e > T_L$ hot electron lose energy to the lattice creating a large non-equilibrium population of phonons, hot phonons, in the semiconductor so that the probability a free carrier absorb a phonon is increased. The latter leads to a reduction in the net probability of emission of a phonon and therefore reduces the energy loss rate from carriers to the lattice. This effect is present in bulk as well as in 2D systems like a 2DEG.

3.4 Phonons in GaN

III-nitrides and in particular GaN and they alloys can present either both zinc-blend or wurtzite crystal structures. However, attainable GaN under normal growth conditions by MBE and MOCVD is the wurtzite crystal structure. Therefore, from now on we focus only in wurtzite structure. Wurtzite crystal structure with a number of atoms per unit cell *s*=4 exhibit a C_{6v}^4 symmetry (belongs to the hexagonal crystal system) and according group theory the total number of vibrational modes in wurtzite is 12 (see Table 3.1).

Table 3.1. Phonon modes in a crystal with wurtzite symmetry such as AlN, GaN, and InN. *s* stands for number of atoms per unit cell.

Mode type	Set	Number of modes
LA	A_1	1
TA	E_1	2
Total acoustic modes		3
LO	A_1, B_1, E_1	4-1
TO	$A_1, B_1, E_1, 2E_2$	2*s*-1
All optical modes		3*s*-3
All modes		12

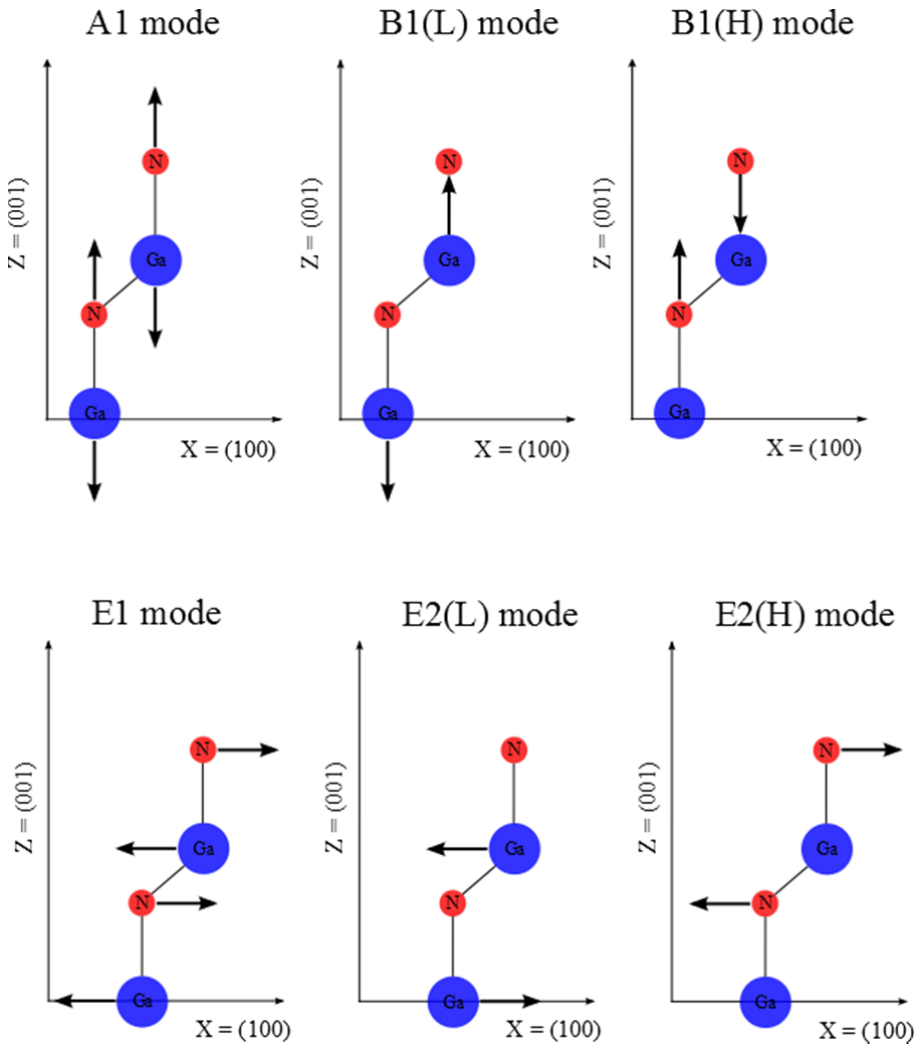


Figure 3.3 Phonon normal modes at the Γ point (zone-center). Z=(001) and X=(100) represent the optical polarization directions for zone-center phonons.

For hexagonal structures group theory predicts eight sets of phonons normal modes at the Γ point, namely $2A_1 + 2E_1 + 2B_1 + 2E_2$. Among them, one set of A_1 and E_1 modes are acoustic (LA+2TA) and the remaining six, $A_1 + E_1 + 2B_1 + 2E_2$, are optical modes (3LO + 6TO) (see Table 3.1). A_1 and B_1 modes give atomic displacement along the *c*-axis and E_1 and E_2, gives atomic displacement perpendicular to *c*-axis, on the basal plane. Because of their polar nature, the A_1 and E_1 modes split into longitudinal optical modes (A_1-LO and E_1-LO) meaning

beating along the *c*-axis, and transverse optical modes (A_1-TO and E_1-TO), meaning beating along the basal plane. A description of the atomic vibrations in wurtzite GaN for the zone-center phonons (Γ point) are displayed in Figure 3.3.

Calculated phonon dispersion curves and phonon density of states or hexagonal bulk GaN are show in Figure 3.4.

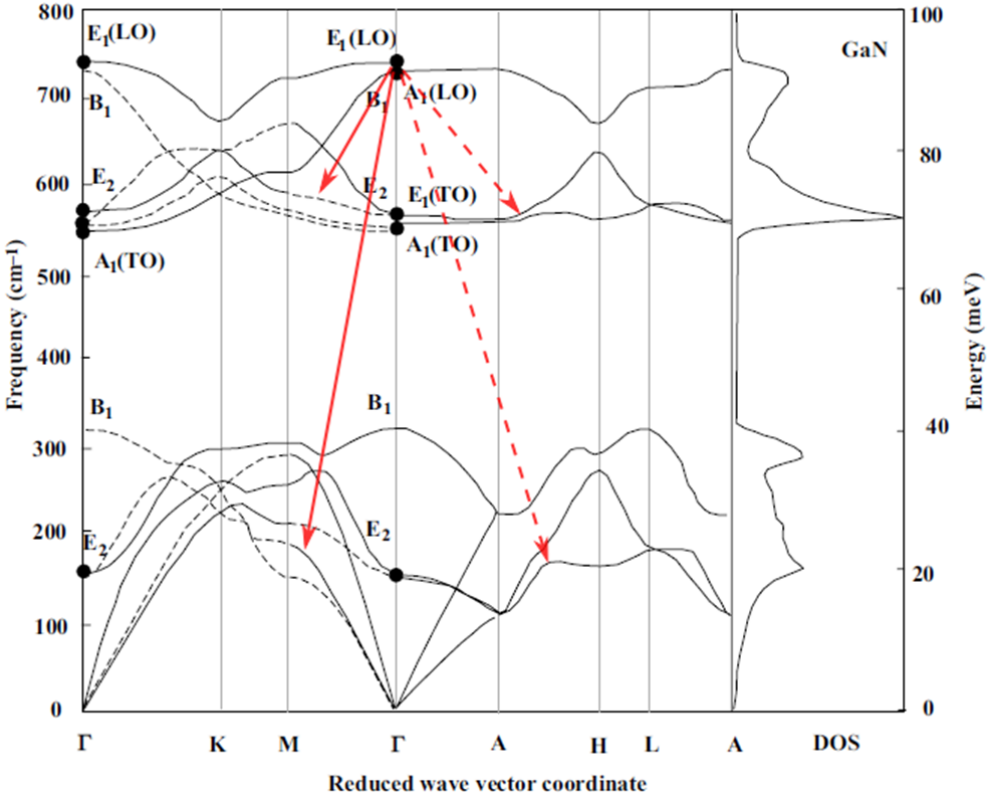


Figure 3.4 Phonon dispersion curves for GaN. Normal modes are indicated along the zone-center. Also, indicate with arrows are the dominant decay paths – Ridley path [30].

Infrared reflection and Raman spectroscopy are very useful techniques to derive zone-center and some zone-boundary phonon modes in nitrides. The A_1 and E_1 modes are each split into longitudinal optic (LO) and transverse optic (TO) components, giving a total of six Raman peaks. These A_1 and E_1 branches are both active for Raman and infrared techniques, while the

E_2 branches are Raman-active only and B_1 branches are inactive. Table 3.2 gives a list of experimental as well as calculated values for the zone-center optical-phonon wave numbers of AlN, GaN, and InN. A1(LO) and E1(LO) are very close each other in energy with a value of ~92meV. And their effects are the most relevant from the point of view of transport properties at high electric field in polar semiconductors such as III-nitrides.

Table 3.2. Optical phonon frequencies of wurtzite AlN, GaN, and InN at the center of the Brillouin zone in the units of cm^{-1}.

Symmetry	**AlN (cm^{-1})**	**GaN (cm^{-1})**	**InN (cm^{-1})**
A_1 – TO	613.64[30], 607.3[31], 609[32], 610[33], 609[34], 612[35], 601[36]	531.0[37], 531.4[38], 533.54[39], 531.2[40], 531.7[41], 540[42]	440[43], 446[44], 440[45], 480[46], 445[47], 440[47]
E_1 – TO	671.41[30], 666.5[31], 668[32], 669.6[33], 668[34] 679[35], 650[36]	558.0[37], 558.4[48], 559.99[39], 558.2[41], 568[42], 558.4[49]	477.9[50], 476[46], 472[47], 472[47]
A_1 – LO	883.6[51], 891.80[30], 884.5[31], 891[52], 895[32], 888[33]	736.5[41], 748[42], 735[53], 733[54], 737[55]	585.4[56], 592[43], 590[44], 590[45], 580[46], 588[47]
E_1 – LO	919.09[30], 911[32], 912.6[33], 911[34]	739.9 [40], 742[41], 757[42], 743[53], 740[54], 745[55]	570[46]
E_2 – (low) / E_2^1	247.8[51], 249.57[30], 249[31], 246[32], 248[33], 246[34], 247[35], 228[36]	144.1[41], 142[42], 144[53], 144[54], 146[36]	89[44], 88[45], 87[46], 104[47]
E_2 – (high)/ E_2^2	653.6[51], 658.51[30], 653.6[31], 659[31], 655[32], 656.6[33], 655[34], 672[35], 638[36]	566.6[37], 567.6[48], 567.5[38], 568.28[39], 567.0[41], 576[42], 566.9[49]	490.1[56], 491[43], 491[44], 491.1[50], 490[45], 488[46], 483[47]
B_1 – (low)	636[35], 534[36]	337[42], 526[35], 335[36]	192[44], 200[46], 270[47]
B_1 – (high)	645[35], 703[36]	713[42], 584[35], 697[36]	540[46], 530[47]

[51] *Seeded grown of AlN boules on PVT grown c-plane AlN;* [30] *bulk wurtzite AlN crystals grown by PVT method;* [31] *0.8-μm-thick AlN layer under a biaxial tensile stress of 0.6 GPa*

grown on Si(111) by MBE; [52] *Freestanding bulk AlN grown by sublimation sandwich technique on SiC seed;* [32] *AlN bulk crystal grown by PVT technique;* [33] *Self-nucleated AlN single crystal with facets;* [34] *bulk AlN grown by PVT technique;* [35] *Calculated using first-principle total energy;* [36] *Calculated using pseudopotential LDA;* [37] *Non-polar (* $1\bar{1}00$*) bulk GaN grown by Ammonothermal method;* [48] *c-plan bulk GaN grown by HVPE;* [38] *m-plane GaN substrate grown by HVPE;* [39] *Nonpolar a-plane GaN grown on r-plane sapphire substrate;* [40] *Strain-free frequencies in a high-quality bulk GaN;* [41] *50 μm thick hexagonal crystal of GaN grown on 6H-SiC by HVPE;* [42] *ab initio calculation using a pseudopotential-plane-wave method;* [49] *Bulk-like GaN grown by HVPE and with removed substrate by laser liftoff;* [53] *Raman scattering on bulk GaN;* [55] *Raman study on high-quality freestanding GaN templates grown by HVPE;* [56] *Strain-free values obtained by Raman measurements on a freestanding InN film grown by MBE;* [43] *Raman measurements on wurtzite InN film deposited on sapphire substrate by MOVPE;* [44] *Raman measurements on hexagonal InN thin films grown by MOVPE;* [50] *Strain-free value obtained by Rama measurement on InN films grown on sapphire by MBE;* [45] *Hexagonal InN thin film grown on (0001) GaN;* [46] *Raman study on InN grown on sapphire and calculation based on the pairwise interatomic potentials and rigid-ion Coulomb interaction;* [47] *Raman study on polycrystalline and faceted platelets of InN and calculation using FP-LMTO LDA.*

3.5 Polar phonon in GaN

One of the most important carrier-phonon scattering mechanisms in semiconductors is the carrier-electric polarization field, due to the relative displacement of positive and negative ions. In polar semiconductors and in particular in low-defect polar GaN material system, carrier scattering is governed by the polar-optical-phonon (POP) scattering mechanism. And it is referred to as the Fröhlich interaction. The Hamiltonian for the interaction is given by:

$$H_{Fr} = \sum_{\boldsymbol{q}} (iC_{\mathrm{F}}/\boldsymbol{q}) \left\{ a_q^{\dagger}\, e^{\mathrm{i}\mathbf{q}\cdot\mathbf{r}-\omega_{\mathrm{LO}}t} - a_q\ e^{-\mathrm{i}\mathbf{q}\cdot\mathbf{r}-\omega_{\mathrm{LO}}t} \right\}$$

where $a_q^{\dagger}$and a_q are the phonon creation and annihilation operators, respectively, ω_{LO} is the LO phonon frequency, $\boldsymbol{q}$ is the wave vector, and t is the variable time. The coefficient C_{F} is given by

$$C_{\mathrm{F}} = e\left[\frac{2\pi\hbar\omega_{\mathrm{LO}}}{NV}(\varepsilon_{\infty}^{-1} - \varepsilon_{0}^{-1})\right]^{1/2}$$

N is the number of unit cells, V is the volume, ε_∞ and ε_0 are the high- and the low-frequency dielectric constants [57]. Because of the Fröhlich interaction, emission and absorption of LO phonons by hot electrons perform the most relevant role in terms of heat generation at high electric fields.

3.6 Hot phonon decay

While the harmonic approximation of the displacement of the ions from their equilibrium position may be used to describe phonon dispersion, non-parabolic terms (cubic or higher order terms containing product of three or more displacements) in the crystal potential for ionically bonded atoms are required in order to describe the decay of phonon modes into other phonons. The leading term in the anharmonic interaction is the cubic term. Interaction Hamiltonian for the cubic term of the anharmonic interaction may be written as

$$H_3 = \sum_{r,i,j,k,\alpha,\beta,\gamma} M_\alpha^{1/2}\omega_\alpha\, M_\beta^{1/2}\omega_\beta 2\Gamma_{ijk}(\alpha,\beta,\gamma)u_{i\alpha}u_{j\alpha}u_{k\alpha}$$

where M is the oscillator mass, ω is the oscillator angular frequency, $\Gamma_{ijk}(\alpha,\beta,\gamma)$ is the third-order anharmonicity coefficient (optical-mode analogue of the type of Grüneisen constant). The subscripts $i, j,$ and k refer to spatial directions and α, β, and γ refer to the type of phonon mode. u is the relative displacement of the ions in each mode and is given by

$$u = \sum_q \left(\frac{\hbar}{2NM\omega}\right)^{\frac{1}{2}} \left(\boldsymbol{e}_{\boldsymbol{q}}^* a_q^\dagger e^{\mathrm{i}\mathbf{q}\cdot\mathbf{r}} + \boldsymbol{e}_{\boldsymbol{q}}\, a_q e^{-\mathrm{i}\mathbf{q}\cdot\mathbf{r}}\right)$$

where $\boldsymbol{e}_{\boldsymbol{q}}$ is a unit polarization vector.

Anharmonic effects, i.e. phonon decay, in wurtzite structures occurs via Ridley three-phonon (LO, transversal optic (TO), longitudinal acoustic (LA), and transversal acoustic (TA)) decay path, LO → TO + LA which competes with the LO → TO + TA path. However, owing to wurtzite crystal symmetry considerations, it is expected that Ridley path LO → TO + LA dominates. For the case of the Ridley path, phonon modes in H_3 are identified as LO with the subscript γ, TO mode with α, and LA mode with β [58].

It is known that the lifetime of TO phonon is shorter than that of LO phonon mode [59] and that additionally electron-TO scattering rate is two order of magnitude lower than the electron-LO phonon scattering [60] due to TO weak coupling with carrier. Then, once the LO phonon has decayed via the Ridley mechanism, we can disregard the effect of the daughter TO mode. Owing to the polar nature of GaN, electron-LO-phonon interaction is strong therefore the more probable heat dissipation path, according Ridley [58] and the mentioned above, is hot electron → LO → LA(TA), then to the heat sink. LA (TA) is related with the thermal conductivity of the lattice. And which is approximately equal to the total thermal conductivity at high temperatures. That is to say, reported high temperature thermal conductivity values for materials and in particular for material for power electronics applications (see Table 1.1) are a measure of how efficient is the propagation of LA through the crystal structure. In GaN it is well known that the LO-LA(TA) is the limiting conversion process. Because, the direct hot electron – LA (TA) path is a very less probable one. Therefore, the LO-LA conversion is the limiting factor; the ultimate process needs to be optimized to remove heat from higher power devices. See Figure 3.5.

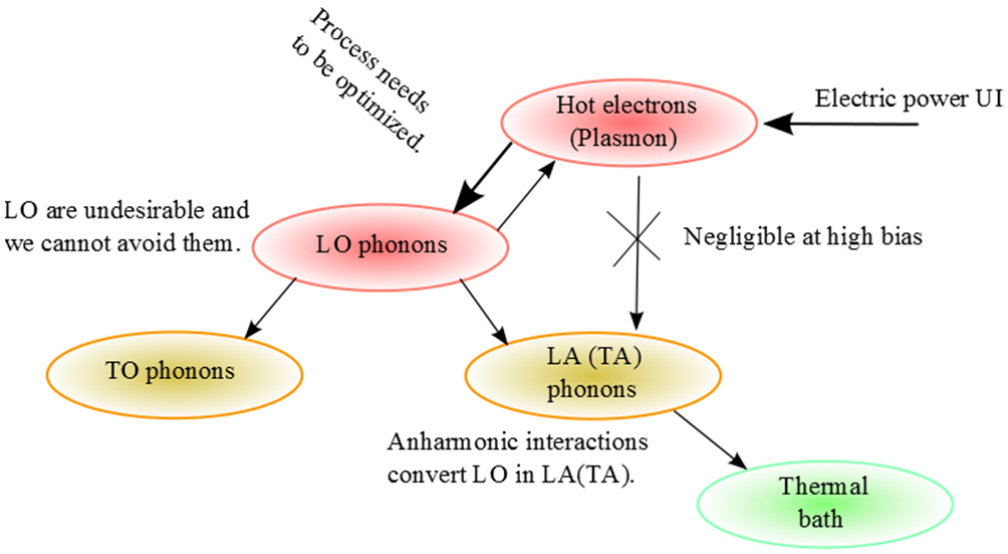


Figure 3.5 Electron energy excess - conversion path. Hot electrons generate hot phonons (LO), LO phonons are converted into TO and LA(TA) phonons via Ridley channel [5]

3.7 Phonon generation in HFETs

The hot electron – LO conversion is a bidirectional process. And manipulation of the physics of the device should incline in favor of the direct path, hot electron → hot phonon (big bold arrow, see Figure 3.5) and not vice versa. As indicated in Figure 3.6, in FETs and in particular in HFETs, the hottest zone (transparent red area), is in between drain side of the gate and drain. Where, the electric field is stronger than in any other region of the device. Because of the GaN pyroelectric nature, hot spots would induce dynamic polarization, affecting device performance. In particular, gate-drain region is subject to high electric fields and current densities (red spot in Figure 3.6). That linked with local defects and pyro-and piezoelectric effects, owing to the different thermal expansion coefficient of the layers and additional strain induced by the dissimilarities between gate metal and semiconductor would result in device performance limitation and shorter lifetime.

Generation of hot electron and subsequent emission of hot phonon is expected in aforementioned region. In other words, in GaN HFETs heat is generated by high electric field. And the diffusion of the heat (white arrow) is assisted by the decay of the hot phonons (LO) into LA phonons. Therefore, heat removal away from the channel, in GaN, is crucial not only for good device performance, but also for device reliability.

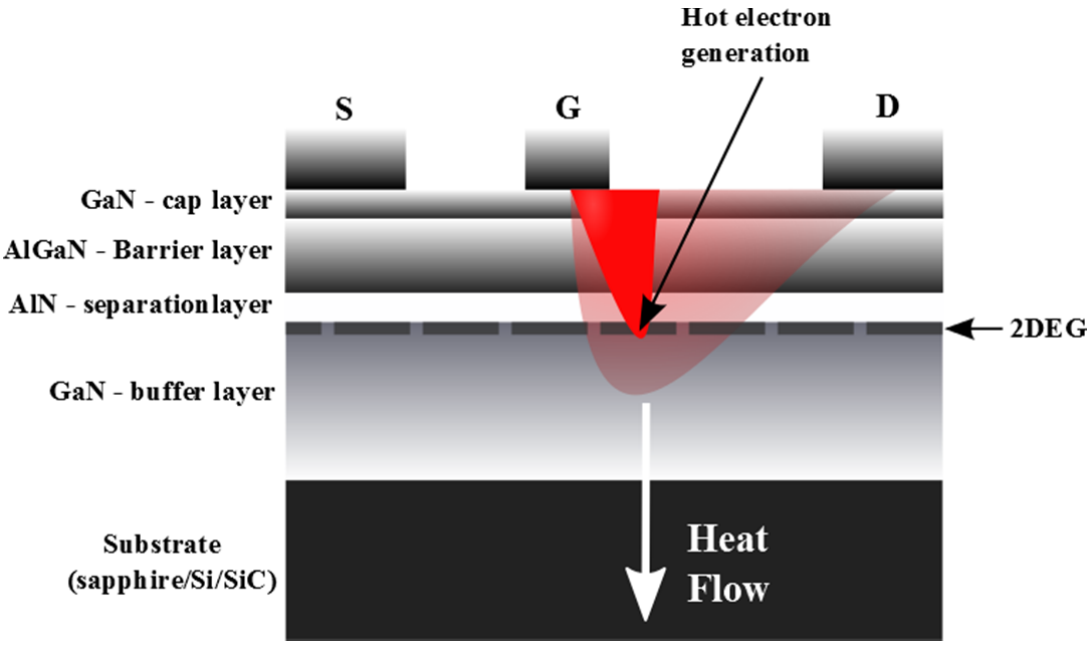


Figure 3.6 Schematic of a standard GaN-based HFET. Layers desciption are at the left figure. G stands for gate, S for source, and D for drain. The location of the 2DEG is indicated at the right. The red spot dicates the region subject to high electric fields. The hot-electron generation place is pointed. The hot zone of the HFET (transparent red colored) expand parallel to the channel and perpendicular to the channel, down to the substrate. Also, the desirable heat flow direction is indicated (white arrow).

3.8 Geometric aspect of phonon generation

In wurtzitic III-nitride, as it was mentioned already, there are 12 phonon modes in total. Three times the number of atoms per unit cell, and which is four. From those 12, 9 modes are optical phonons and the remaining three are acoustic phonons. Electrons interact more strongly with A1(LO) and E1(LO) phonons which energy levels are close each other and is around 92meV in GaN. E1(LO) couples parallel to the channel direction in a HFET base on heterostructures grown on basal *c*-plane and A1(LO) couples along the direction perpendicular to the channel (see Figure 3.7).

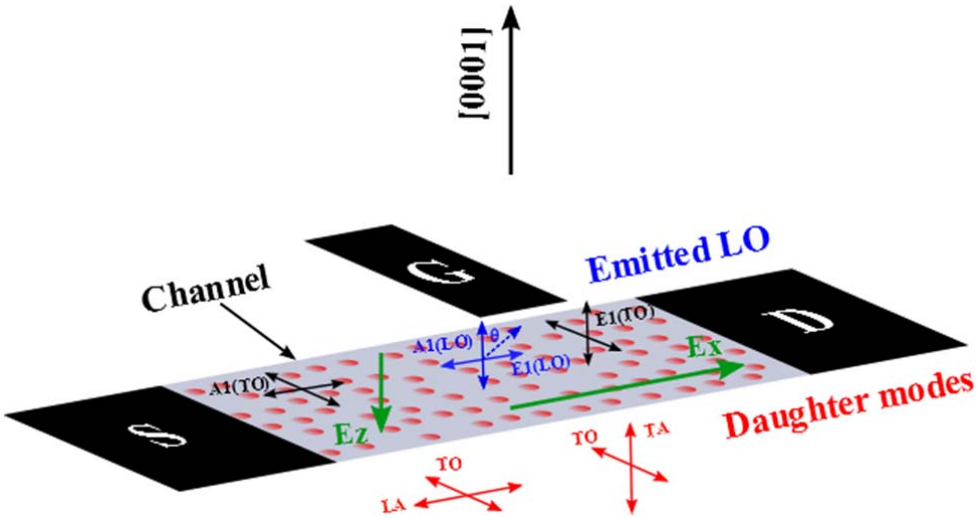


Figure 3.7 Schematic representation of the phonons in a HFET built-up on a heterostructure grown along *c*-plane direction, [0001]. Small arrows indicate the phonon atomic displacement.

Electron flow along the channel parallel to the applied electric field (Ex), therefore, it is expected that electrons interact mainly with E1(LO) phonons. In case electrons are available, also, to flow perpendicular to the *c*-plane (because scattering process or leakage current from the gate and through the barrier), interaction of electrons with the A1(LO) phonons should also be taken into account.

In general emission of both A1(LO) and E1(LO) take place and the angular frequency dependence of the resultant zone-center LO phonon is given by

$$\omega_{\mathrm{LO}}(\theta) = \left[\left(\omega_{\mathrm{LO}}^{\mathrm{A1}}\right)^2 \cos^2\theta + \left(\omega_{\mathrm{LO}}^{\mathrm{E1}}\right)^2 \sin^2\theta\right]^{1/2}$$

where θ is the angle formed between *c*-axis and the resulting phonon wave vector, $\omega_{\mathrm{LO}}^{\mathrm{A1}}$ and $\omega_{\mathrm{LO}}^{\mathrm{E1}}$ are the A1 and E1 LO phonon frequency, respectively. Depending on the current direction, hot electrons may primarily relax through A1(LO) ($\theta = 0°$) or E1(LO) ($\theta = 90°$) emission. Assuming transport occurs in *c*-plane only hot electrons loss energy by emission of E1(LO) phonons should be considered. However, from an energetic point of view, LO energy in all cases is ~ 92 meV. In steady state, electron energy gained from the electric field is balance by electron energy loss via LO phonon emission, so the electrons propagate at a saturated velocity.

3.9 Power dissipated by hot phonons

The probability that a phonon state with energy $\hbar\omega$ is excited at a temperature, T_{ph}, is known as its occupation number. Phonons are bosons and their phonon occupation number, $N_{\mathrm{ph}}(\hbar\omega)$, is given by the Bose-Einstein distribution function:

$$N_{\mathrm{ph}}(\hbar\omega) = \frac{1}{e^{\left(\hbar\omega/k_B T_{\mathrm{ph}}\right)} - 1},$$

where k_B is the Boltzmann constant.

Under energy conservation considerations, which means that the energy supplied by the electric source is equal to the dissipated energy, the energy given off by an electron is given by the following formula

$$P_{\mathrm{d}} = \frac{\hbar\omega}{\tau_{\mathrm{sp}}} N_{\mathrm{ph}}\left(1 + N_{\mathrm{ph}}\right)p_{-} - \frac{\hbar\omega}{\tau_{\mathrm{abs}}} N_{\mathrm{ph}} p_{+} \tag{1}$$

where the average times τ_{sp} and τ_{abs} correspond to the spontaneous emission and absorption of LO phonon by a hot electron, respectively. And p_{-} and p_{+} are the probabilities a hot electron be ready to emit or absorb an LO phonon, respectively, and are given by:

$$p_{\mp} = \frac{1}{n_{2D}} \int D(\mathrm{E}) f(\mathrm{E})[1 - f(\mathrm{E} \mp \hbar\omega_{\mathrm{LO}})]\,\mathrm{dE}$$

where E is the electron energy, $f(\mathrm{E})$ is the Fermi function, $D(\mathrm{E})$ is the 2D density of states , and n_{2D} is the 2DEG density [61].

3.10 Plasmon

The dielectric behavior of semiconductors with high electron concentrations is determined by collective excitations of the free carriers. If u is the homogeneous displacement of the electron gas relative to the ion cores, then equation of motion (without considering any mechanical restoring force) is given by

$$n_{3D}\, m\, \frac{d^2u}{d^2t} + \gamma \frac{du}{dt} = -n_{3D} e\, \mathrm{E} \tag{2}$$

where e is the elemental charge, n_{3D} is the bulk electron concentration, m the electron mass, E applied electric field, and γ is the damping constant. The damping constant and the conductivity, σ, are related by $\sigma = \frac{J}{\mathrm{E}} = \frac{{n_{3D}}^2\, e^2}{\gamma}$.

Replacing the latter into the equation of motion (2) we have

$$n_{3D}\, m\, \frac{d^2u}{d^2t} + {n_{3D}}^2\, e^2 \frac{du}{dt} = -n_{3D} e\ \mathrm{E}$$

Then Fourier-transformed equation is

$$\left(-n_{3D}\, m\, \omega^2 - i\, \frac{n^2\, e^2}{\sigma(\omega)}\omega\right) u(\omega) = -n_{3D}\, e\ \mathrm{E}(\omega)$$

Writing $u(\omega)$ as a function of the polarization, $P(\omega) = -e\, n_{3D}\, u(\omega)$, and replacing it in the latter expression we have then the dielectric function

$$\varepsilon(\omega) = 1 - \frac{\omega_{\mathrm{p}}^2}{\omega^2 + i\, \frac{\omega_{\mathrm{p}}^2 \varepsilon_0}{\sigma(\omega)}\omega}$$

with $\omega_{\mathrm{p}}^2 = \frac{n_{3D}\, e^2}{m\, \varepsilon_0}$ (in a 2DEG system $\omega_{\mathrm{p}}^2 \propto \sqrt{\frac{n_{2\mathrm{D}}\, e^2 4\pi}{m^* \varepsilon}}$ where $n_{2\mathrm{D}}$ is 2DEG density, m^* is the electron effective mass, and ε is the dielectric contact of the material). Assuming weak damping, ω_p is just the frequency at which $\varepsilon(\omega) = 0$. Thus, ω_p denotes the frequency of the longitudinal oscillation of the free electron gas. These oscillations are called plasmon. On the other hand there is no transverse oscillation because of the lack of restoring force. As we can see from its expression, ω_{p} increases with the square root of the electron density. It is worth to mention at this point that in semiconductors beside the plasma oscillation of free electrons, also display plasma oscillations of valence electrons[62]. In this work when we talk about plasmon, we mean oscillation of free electrons.

3.11 Plasmon-hot-phonon resonance

RF, microwave, and millimeter wave systems for telecommunication and power switching electronics claim for electronic devices capable to work at higher frequency and higher power levels [63]. HFET based on GaN is covering this demand in both telecommunication and power electronics. Nowadays, GaN HFETs are a commercial reality and several vendors are supplying the high power switching [64] and high power at frequency [65] markets.

However, long term reliability at high power is still an issue even for HFET based on GaN for which crystal perfection has not been achieved yet. On the other hand, generated heat in the channel (non-equilibrium (hot) longitudinal optical phonons) fosters additional electron scattering, degrading device performance comprising the reliability and stability of the HFET.

Then, it is desirable to find optimal working conditions for the HFET at which higher power handling at higher frequencies (cut-off frequency) and lower degradation (reliability) can be all achieved, simultaneously. The latter can be attained under plasmon–hot phonon resonance conditions where HFET work at optimal conditions, because plasmon-assisted ultrafast decay of hot phonons.

Experimental data obtained from both Fluctuation technique and Raman techniques show an empirical $1/n$ dependence of the hot phonon lifetime, where n is the volumetric carrier density. Such a model suggest a plasmon-assisted decay of the LO phonons into acoustic phonons. As plasmon energy exceeds the acoustic phonon energy ($n\sim 10^{17}-10^{18}$ cm^{-3}) plasmon-LO phonon coupling becomes more pronounced. A further increase of the carrier density ($n\sim 10^{19}$ cm^{-3}) results in a plasmon energy comparable to that of the LO phonon energy. At this point plasmon–LO phonon coupling is the strongest (minimum hot phonon lifetime) and reversing the course for higher carrier densities. In other words, for a $n\sim 10^{19}$ cm^{-3} we have plasmon-LO phonon resonance.

In HFET with a 2DEG density of $\sim 10^{13}$ cm^{-2} and considering the 2DEG is confined in a triangular quantum well with effective width at Fermi level of 5nm, we see that volumetric electron (3DEG) densities in the order of $\sim 10^{19}$ $\mathrm{cm}^{-3}$and higher are achievable in the channel of a GaN-based HFET. Figure 3.8 a) shows the energy levels of LO phonons, acoustic phonons and plasmon energy as function of the 3DEG density. Figure 3.8 b) exhibits experimental data on hot phonon lifetime dependence on 2DEG and equivalent 3DEG density. At this moment, it is worth to mention that there is not satisfactory theoretical treatment of plasmon-LO phonon interaction as indicated in Ref [66]. And that the "plasmon–LO phonon resonance" model is sustained by experimental data as the shown in Figure 3.8 b). Also, signature of the plasmon-hot phonon resonance in HFET was found in a variety of experimental results. Resonance signature in hot phonon lifetime, reliability, and signal delay in single InAlN/AlN/GaN channel HFET were summarized in Ref. [5], resonance signature in electron drift velocity was studied in Ref. [6]. And resonance signature in fast decay of hot phonons in InAlN/AlN/AlGaN/GaN multiple channels was studies in Ref. [7]. Also, resonance signature in hot-phonon lifetime in single AlGaN/GaN channel and in ultrafast decay of hot phonons and hot electron drift velocity in multiple AlGaN/GaN channels were studied in Ref. [8] and Refs. [9], [10], respectively. Since drain current is proportional to carrier drift velocity and carrier density, higher power implies higher voltage and higher current levels. At higher voltage then higher electric field the electron drift velocity, because of the LO phonons, increase slowly and toward carrier velocity saturation [67]–[69]. Hence, in order to increase HFET power delivery, it is more feasible to achieve higher power levels by increasing the carrier density in the channel. Electronic devices working at high power conditions, always comes with heat dissipation issues. Built up heat in the channel is dissipated, mainly, by the conversion hot LO phonons into acoustic phonons which transfer the heat out of the channel.

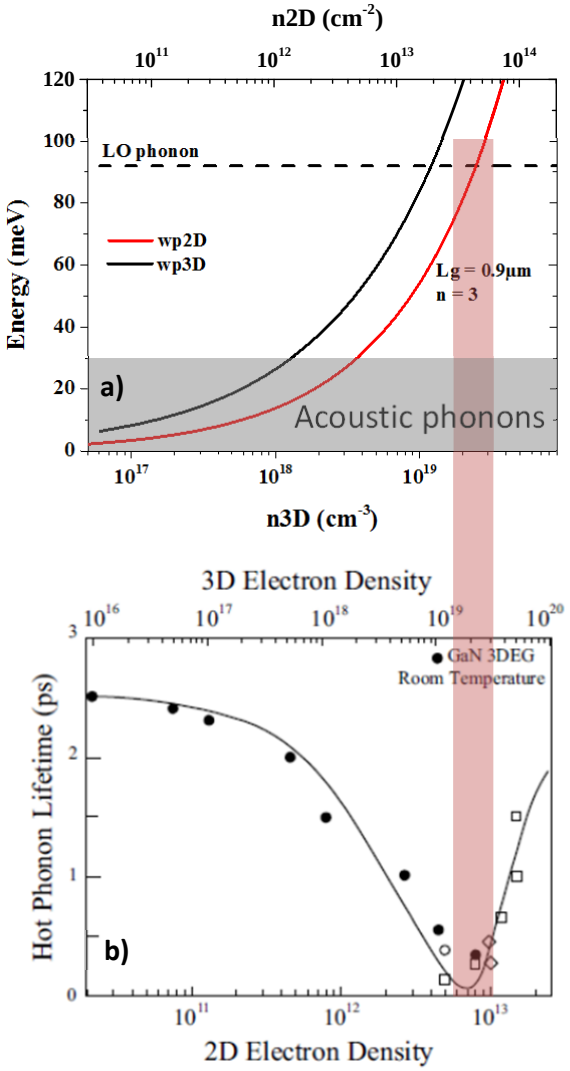


Figure 3.8 Idealization of the LO phonon, acoustic phonon, and plasmon energies as a function of the electron concentration in GaN a) and b) Measured low-field hot phonon lifetime for bulk (closed circles) and various GaN-based channels (open circles). After [61]. In a) red line indicate the plasmon energy for a for a heterostructure field-effect transistor with a gate length (Lg) of 0.9µm, n indicates the plasmon wave vector order.

The rate of the aforementioned conversion is a limiting from the point of view of power dissipation. Therefore, the faster the hot phonon decay the lesser the hot phonon effects and consequently a better frequency performance of the channel [70]. Then, for power application, it is desirable to attain plasmon-hot phonon resonance at higher 2DEG. The latter can be attained by widening the electron density profile.

3.12 Widening the carrier density profile

With strongest plasmon-hot phonon interplay, resonance, at a 2DEG density of 0.8-1.1 x 10^{13} cm^2, equivalent to a 3DEG ~1x10^{19} cm^3, 2D and 3D densities are related by a "form factor," correlated with the way in which the channel widens the carrier density profile. Channel widening at moderate electric fields depends, mainly, on the heterostructure in which it is formed. Because in bulk GaN resonance happens around ~1x10^{19} cm^3 and in order to achieve higher power levels, the heterostructure should wide the carrier density profile in such a way that 3D carrier density maximum is ~1x10^{19} cm^3 and 2DEG density is as high as possible.

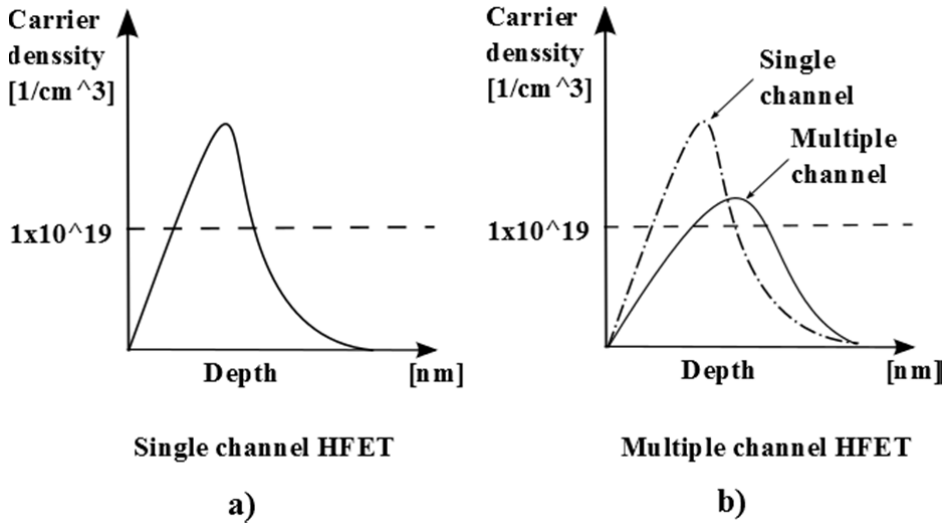


Figure 3.9 3DEG density profiles a) in a standard heterostructure (single channel (SC)) and b) a qualitative comparison between single and multiple channel heterostrucutre (coupled channel (CC) or dual channel (DC)) on the widening of 3DEG density profile.

In Figure 3.9 a) is presented a representation of the electron density profile of a standard HFET (here called single channel (SC)). In order to bring plasmon–LO phonon resonance condition in the SC, we to deplete the channel.

Channel depletion can be done in different ways. One is by applying very high electric fields. Doing so, electron will gain energy increasing its temperature. As a result the 3DEG density is reduced and resonance is achieved. Unfortunately, this is not a practical way to widening the 3DEG density profile because the necessary electron temperature is too high (>400K) that the channel would be destroyed before to occur resonance conditions. Other option is by depleting the channel via gate-source voltage. This option even safe, is not convenient because usually requires an almost complete depletion of the channel. It means that the resonance condition would be attained under very low power conditions. And it is what happens, as discussed in the section 4.2 Single channel HFET performance: literature review.

As it was already reported, a convenient realizable approach to reach the mentioned resonance at higher 2DEG is by designing HFET structures based on multiple channels [9], [71] e.g. dual channel (DC) and coupled channel (CC) (see Figure 5.1). When DC and CC structures widen the carrier density profile, as it was already pointed out in Ref.[7], [9], the plasmon-hot LO phonon resonance occurs at higher 2DEG. And the wider the part of 3DEG profile close to 10^{19} cm^{-3} level, at which plasmon–hot phonon resonance happens in GaN bulk system[67], [72], the higher 2DEG density in the channel under resonance condition. Thus resonance takes place at higher power working conditions. It is desirable to attain resonance conditions at V_{GS}=0V. Case in which gate leakage current is expected to be minimum with additional benefit of an efficient use Al content of the barrier layer which is directly related with the carrier density in the channel. In summary, at resonance condition it is expected phonon side effects to be minimized, a better use of the heterostructure and minimum heat dissipation from the channel. However, a better understanding of the conditions at which resonance occur is lacking. So far, there is no reported plasmon-phonon resonance at values of $V_{GS} \approx 0V$.

Chapter 4. Review

In this Chapter we present a brief description of the heterostructure on which SC HFET are usually based. The role that each layer plays in the heterostructure is mentioned. Later on a revision of the reported values of gate-source voltage (V_{GS}) under which cut-of frequency happens in standard HFETs as well as other electrical parameter that characterizes the performance of the SC heterostructure are presented.

4.1 Single channel (Standard) HFET: A brief description

Description of a generic standard HFET based on GaN is exhibit in Figure 4.1. The HFET topology presented is a well-established one and is used by the industry. Following a brief explanation of the component layers of a HFET as well as their main purpose are given.

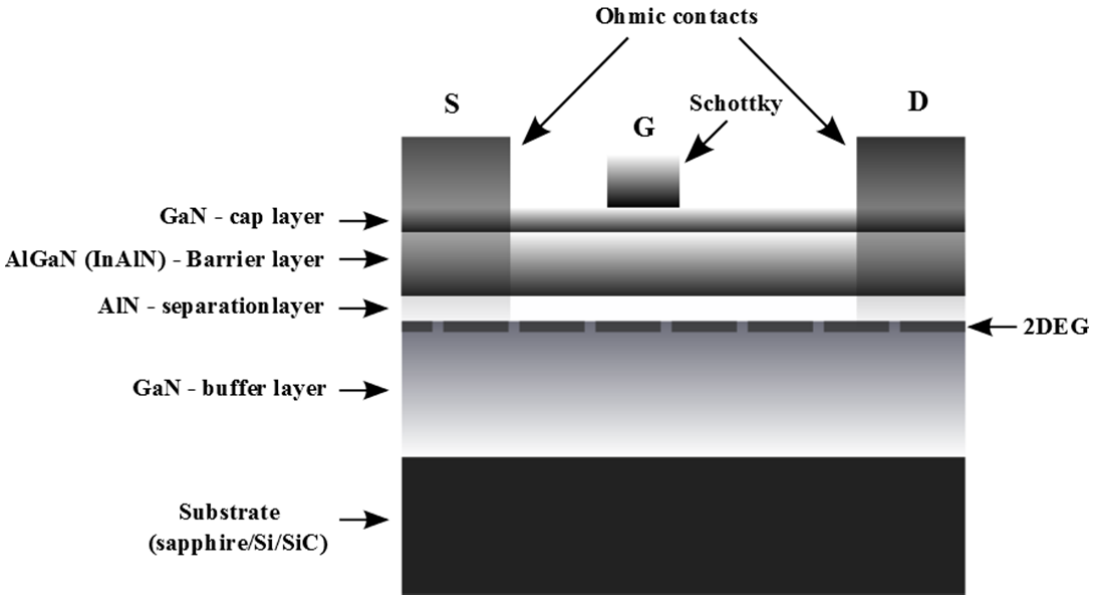


Figure 4.1 Schematic description of a standard (single channel (SC)) GaN-based HFE. Layers desciption at the left of the figure indicate the diferent layers which form a standard HFET. G stands for gate, S for source, and D for drain. The location of the 2DEG is indicated at the right of the figure.

Substrate: basically three different materials are used for device based on III-nitride, sapphire, Si, and SiC. Sapphire is used in low power application, mainly, optoelectronics. Owing to their thermal properties Si and SiC are the election in power switching electronics and in RF power application, respectively. Also, it should be mentioned the existence of GaN substrates but they prohibitive.

Buffer layer: ideally insulating GaN. However, owing to the imperfection GaN has semi-insulating character with a background carrier density of 10^{16} cm^{-3} in good quality material. At the edge of buffer layer (adjacent to the separation layer) is where the formation of the channel occur. Therefore, the last nanometers of the buffer layer should be of high quality. That means, free of imperfections. Also, its end surface should be electrically smooth.

Separation layer: a thin AlN interlayer at the buffer/barrier interface. It suppresses the penetration of the electron wave function into the barrier layer and effectively reduces alloy scattering. From the point of view of the transport parameters, an optimized thickness value of 1nm for the AlN layer is found and for which either both the carrier mobility and the sheet resistance of the channel are optimum.

Barrier layer: the mission of this layer is twofold. It provides polarization induced charge to the 2DEG and at the same time serves as Schottky-gate barrier. Induced charge is controlled, mainly, by the Al content in the barrier. Also, and at lower degree, induce charge density can be controlled with the barrier thickness. The higher the Al content and the thicker the barrier layer the higher the induced charge density. Of course, first theoretical and practical issues limit the maximum achievable charge density. As material for the barrier, AlGaN and InAlN were proposed for HFET applications.

For AlGaN/GaN the general trend is, the higher the Al composition and the thicker the barrier layer the higher the polarization induced charge. At Al content higher than 37% or barrier thicker than 10nm induced charge starts to saturate. The highest sheet carrier density, either both calculated and measured, is $2\times10^{13}cm^{-2}$ for an Al composition of 37% in a barrier layer 30nm thick. For higher Al content the barrier stats to relax diminishing the piezoelectric component of the polarization induce charge.

InAlN barrier layers were proposed as an alternative to AlGaN barriers. Having the possibility to growth lattice match on GaN, InAlN barrier reduce stress related issues. And because of the band discontinuity with GaN provide higher polarization induced charge than AlGaN counterpart, even though only the spontaneous component of the polarization is present for InAlN barrier lattice matched. In the practice InAlN-GaN lattice matched is achieved for an Al composition of ~18% with a sheet carrier concentration of around $1.2\times10^{13}cm^{-2}$. And which would be promising from the point of view of the power level a HFET could handle. However, as pointed in the Chapter Experimental results, InAlN barrier layers degrade easily, even after few hours under electrical stress.

Cap layer: improve Schottky barrier and facilitates ohmic (drain/source) contacts. Also, protects AlGaN from oxidation (Al oxidation). Inclusion of a GaN layer of a few nanometers (usually 2nm) on top of the barrier layer increases the peak barrier height owing to the strong polarization effect in nitrides. Higher peak barrier results in a reduction in the gate leakage current when compared with HFET without cap layer. However, the suppressed leakage current mechanism is unclear.

Ohmic contacts: source and drain contacts are of fundamental importance for GaN-HFETs because they provide most of the electron to 2DEG. Ohmic contacts are formed by deposing a sequence of metal layers, usually, Ti/Al/Ni/Au. In aforementioned scheme, Ti is the

responsible to form the ohmic contact itself via TiN_x phase formation which provides residual nitrogen vacancies that act as donors in GaN.

Schottky contacts: formed by bilayer Ni/Au directly deposit on top of the cap layer. Resulting layer denominated gate is expected to have the control of the charge in the channel. Lateral tunneling (from gate to cap surface) at the drain edge of the gate creates an extension of the gate what is usually referenced as "virtual gate". Virtual gate degrade the HFET cutoff frequency performance.

4.2 Single channel HFET performance: literature review

Table 4.1 summarizes characteristics of high performance HFET together with the transport parameter of the heterostructure they are base on, single channel in all cases. All heterostructures perform carrier density larger than $1\times10^{13}cm^{-2}$ and according what we discussed in the section "Widening the carrier density profile" it should be necessary to deplete the channel in order to get resonance condition and in fact it is what happens. As explained in section 5.6.2, in this work we are going to use the cutoff frequency (f_T) as "sensing probe" to infer HFET bias condition at which minimum lifetime of hot phonon occur (plasmon-hot phonon resonance). Note that here we do not emphasis the absolute value of f_T but the bias condition at which f_T is attaned. Then plotting the gate-source for which cutoff frequency is found, V_{GSfT}, over the threshold voltage, $V_{Th,}$ versus pristine carrier density, n_s, we demostratet that standard channels need to be depleted around 50% or more in order to reach plamon –hot phonon resonance conditions (see Figure 4.2). This means, assuming V_{DS} voltage fix, that in reported high performance HFET resonace conditions take place at 50% of the maximum power level the HFET can handle which is not optimum.

Table 4.1. Reported cutoff frequequency values for high performance HFET.

				V_{GSfT} - V_{GSfT} for f_T and f_{max}				V_{GSfT} - V_{GSfT} for g_m				
n_s	μ	Sheet Resistance	V_{Th}	V_{GSfT}	V_{DSfT}	f_T	f_{max}	V_{GSgm}	V_{DSgm}	g_m	Ref.	Year
$\times 10^{13}$ [cm^{-2}]	[$cm^2 \cdot V^{-1} \cdot s^{-1}$]	[Ω/■]	[V]	[V]	[V]	[GHz]	[GHz]	[V]	[V]	[mS/mm]		
2.74	759	-	-3.3	-2.4	6	64	106	-2	6	363	[73]	2014
1.8	1770	195	-4	-3.3	5.6	230	300	-3.75	5.6	770	[74]	2013
1.64	1766	215	-5.25	-3.7	2.5	317	49	-3.7	2.5	680	[75]	2013
1.17	2000	314	-2.8	-2.1	5	100	206	-2	5	440	[76]	2012
1.92	1240	262	-4.25	-2.9	2.75	370	30	-3	3	650	[77]	2012
1.5	1670	250	-2.7	-1.7	3.5	245	-	-1.3	5	467	[78]	2011
2.4	1300	200	-9	-5.3	4	205	-	-5.3	4	575	[79]	2011
1.4	1500	290	-3.25	-2	20	19	50	-3	10	374	[80]	2011
1.56	1000	-	-3	-1.5	7	14.32	16.22	-2	7	169	[81]	2011
1.89	1790	183	-3.5	-2.6	4	52	110	-2.6	4	460	[82]	2011
2.15	1250	235	-6	-3.2	5	52	102	-4	10	400	[83]	2011
1.6	1330	290	-4.7	-4.1	4	46	125	-4	6	473	[84]	2011
1.9	1.300	260	-5.5	-4.0	4.8	55	210	-4	6	487	[84]	2011
2.2	1250	-	-4.5	-3	10	50	40	-2.8	4	300	[85]	2011

Continued Table 4.1

				V_{GSfT} - V_{GSfT} for f_T and f_{max}				V_{GSfT} - V_{GSfT} for g_m				
n_s	μ	Sheet Resistance	V_{Th}	V_{GSfT}	V_{DSfT}	f_T	f_{max}	V_{GSgm}	V_{DSgm}	g_m	Ref.	Year
$\times 10^{13}$ [cm^{-2}]	[$cm^2 \cdot V^{-1} \cdot s^{-1}$]	[Ω/■]	[V]	[V]	[V]	[GHz]	[GHz]	[V]	[V]	[mS/mm]		
1.5	1900	227	-4.8	-3.7	4.7	220	60	-4	6	548	[86]	2011
1.8	1790	190	-4.8	-3.7	4.7	153	54	-4	6	548	[86]	2011
1.1	1635	310	-2.5	-1.6	4.5	210	-	-17.5	5	540	[87]	2011
1.7	1369	260	-3.5	-2.4	4.5	195	-	-2.6	5	595	[87]	2011
2.3	1400	-	-7	-5.6	6	205	220	-5.5	4	462	[88]	2011
1.65	1581	228	-4.2	-2.9	4	300	-	-3	4	525	[89]	2011
2.15	1250	23	-2.5	-1.6	4	85	103	-1.4	5	600	[90]	2011
1.3	731	-	-5	-2.5	10	21	42	-2.3	8	138	[91]	2010
2.39	1079	244.3	-5.8	-4.5	10	104	96	-4.75	10	432	[92]	2010
3	1050	-	-4.	-3	14	54	58	1	5	187	[93]	2010
3	1050	-	-6.8	-4.5	10	61	70	1	6	222	[93]	2010
1.95	1060	380	-5.5	4.2	4	143	176	-4.34	4	415	[94]	2010
2.4	1300	200	-5	-4.25	5	144	137	-4	4	480	[95]	2010

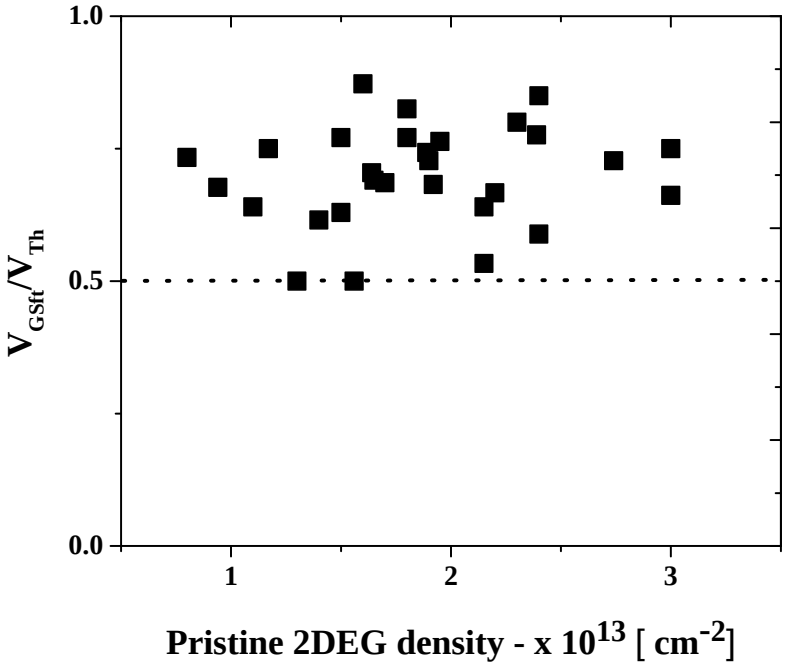


Figure 4.2 Gate-source voltage at maximum cut-off frequency (V_{GSft}) relative to (V_{Th}). Reported *f*T values for standard high performance HFET are obtained for V_{GSft}/V_{Th} equal or higher than 0.5.

Chapter 5. Methods and approach

Following a brief description of the methods used for the study of the plasmon–hot phonon resonance is presented. First, multiple channel heterostructures, coupled channel and dual channel, are introduced. Also a description of the multiple channel heterostructures is presented taken as base the single channel heterostructure already described in section 4.1. Next, simulation results on mentioned heterostructures are reported. Simulations aim to share some light on how multiple channel heterostructures widen the carrier density profile. Here, distribution and shape of the electron density profile are our main concern. Continuing with our presentation, the growth process based on metal organic vapor chemical deposition (MOCVD) technique employed to grow the multiple channel heterostructures is described.

Following, the device fabrication process is presented. Electrical tools and techniques to characterize the heterostructures and devices are detailed. Finally, the approach followed to grow and characterized the heterostructures and fabricate and characterized HFET devices is described.

5.1 Multiple channel heterostructures

Heterostructures studied in this work, namely, single channel (SC), dual channel (DC), and coupled channel (CC) are presented in Figure 5.1. A qualitative description of a single channel heterostructure was given in subsection 4.1. The main difference between SC and DC and CC is the insertion of an extra channel ((Al)GaN) layer and separation layers between the barrier layer (second layer from top) and the buffer layer (3µm GaN) of a SC heterostructure. By inserting extra channels of varied composition and thickness it is expected to control, to some extent, the carrier density profile as it is demonstrated in subsection 5.2.

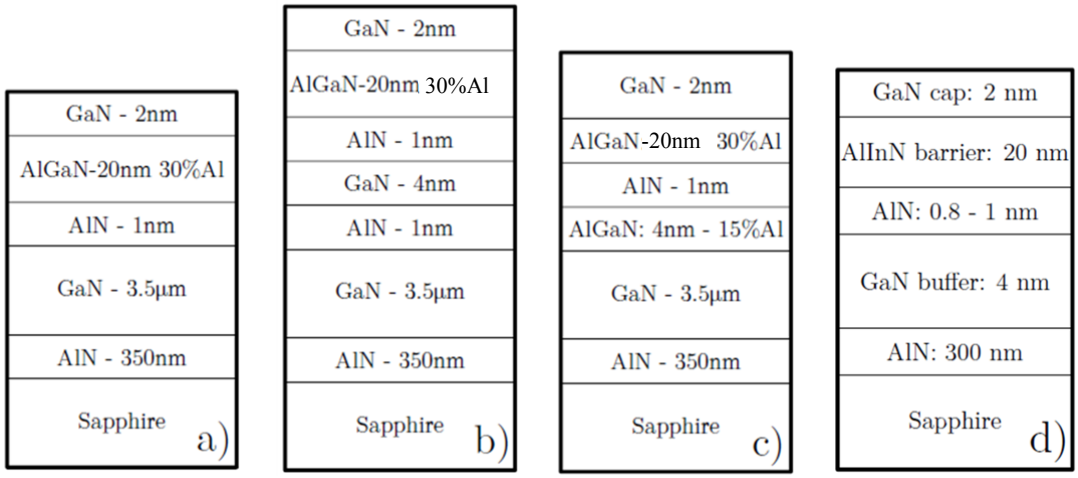


Figure 5.1 HFET structures with AlGaN barrier layers a) single channel (SC), b) coupled channel (CC), and c) dual channel. d) single channel HFET with InAlN barrier layer. The latter, optimized AlInN/AlN/GaN heterostructure.

5.2 Simulation

Single and multiple channel heterostructures design, namely, coupled (CC) and dual (DC) were model and simulated via technology computer –aided design (TCAD) tool – ATLAS by SILVACO. Self-consistent coupled Schrodinger Poisson Mode was used in all simulations. This model self-consistently solves Poisson's equation (for potential) and Schrodinger's equation (for bound state energies and carrier wave functions). III-nitride material and model parameters were the ones provided by the Blaze simulator, which simulates devices fabricated using advanced materials and includes a library of binary, ternary and quaternary semiconductors, i.e. III-nitrides. Blaze has built-in models for graded and abrupt heterojunctions, and simulates binary structures such as MESFETS, HFETs and HBTs.

Piezoelectric polarization (strain induced) and total spontaneous polarization in our simulations are calculated automatically. Therefore, insertion of delta doping to simulate interface charge is not necessary. Also the degree of polarization can be controlled by a factor which value goes between 0 and 1. In our simulation a value of 1 was used in all simulations. No unintentional doping was added to the heterostructure modeling since the purpose of the simulation is to evaluate the effect of the heterostructure design on the widening of the carrier density profile and not HFET performance. A working and tested simulation file for a single channel heterostructure is displayed in APPENDIX C. Simulation results are plotted in such a way that x-axis represents depth perpendicular to the heterostructure from the top (left side) to the bottom (right side). Right y-axis indicates the conduction band (CB) and link y-axis the carrier density profile (n_s).

5.2.1 Coupled Channel HFET

For coupled channel heterostructure the effect of the GaN channel thickness and AlN separation layer thickness were studied. In Figure 5.2 the effects of GaN channel layer thichness is exhibited. As expected the thicker the GaN layer the large the separation between channels. Intresting to note is that for thickness lower than 4nm, the coupled channels combine in one and from the point of view of carrier profile the heterostructure behaves as a single channel heterosstucture. Then, thickness equal or larger than 4nm should be implemented in order to be in the presence of coupled channels.

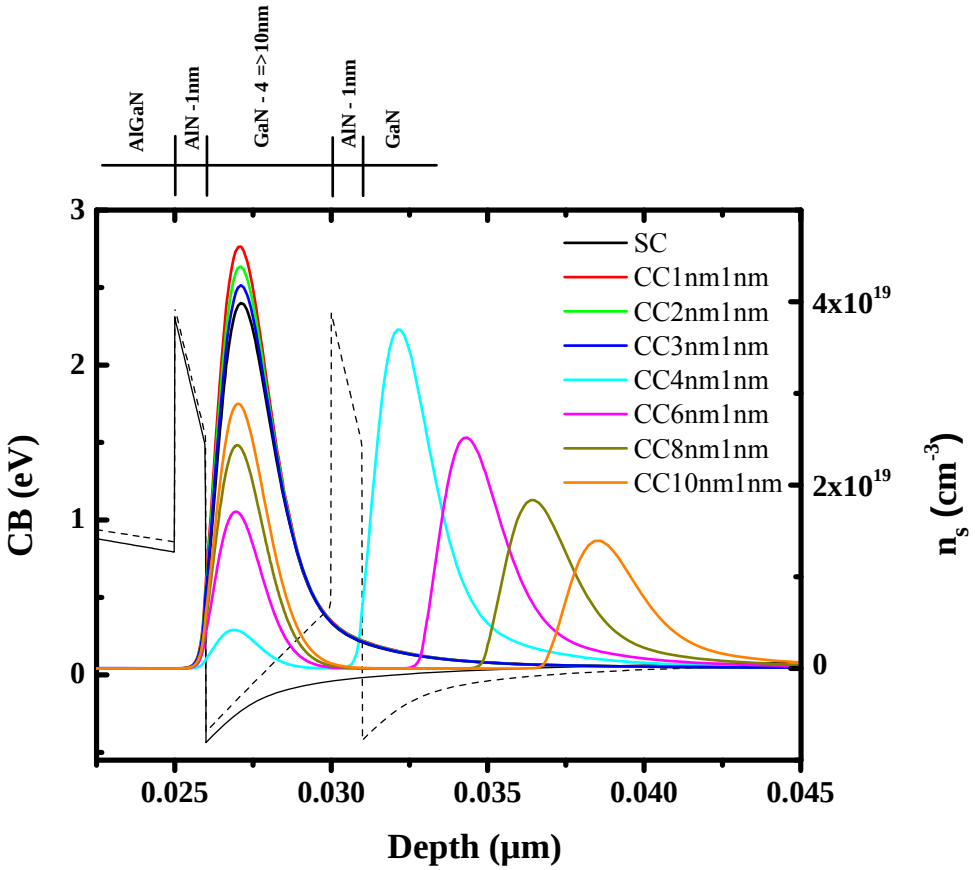


Figure 5.2 Coupled channel heterostructure. GaN channel layer thickness effects on carrier density profile. Left axis indicates conduction band (CB), right axis carrier density (n_s). Thin continuous line is the CB for single channel (SC) heterostructure and dashed line for couple channel heterostructure for a GaN layer 4nm thick and a separation layer 1nm.

Results on the effect of the thickness of the separation layer on the carrier density profile are presented in Figure 5.3 and Figure 5.4. It is clear from Figure 5.3 that separation layer thicker than 1nm concentrate carrier in the botton channel. Resulting carrier profile resmbles pretty much the same than for a a single channel structure.

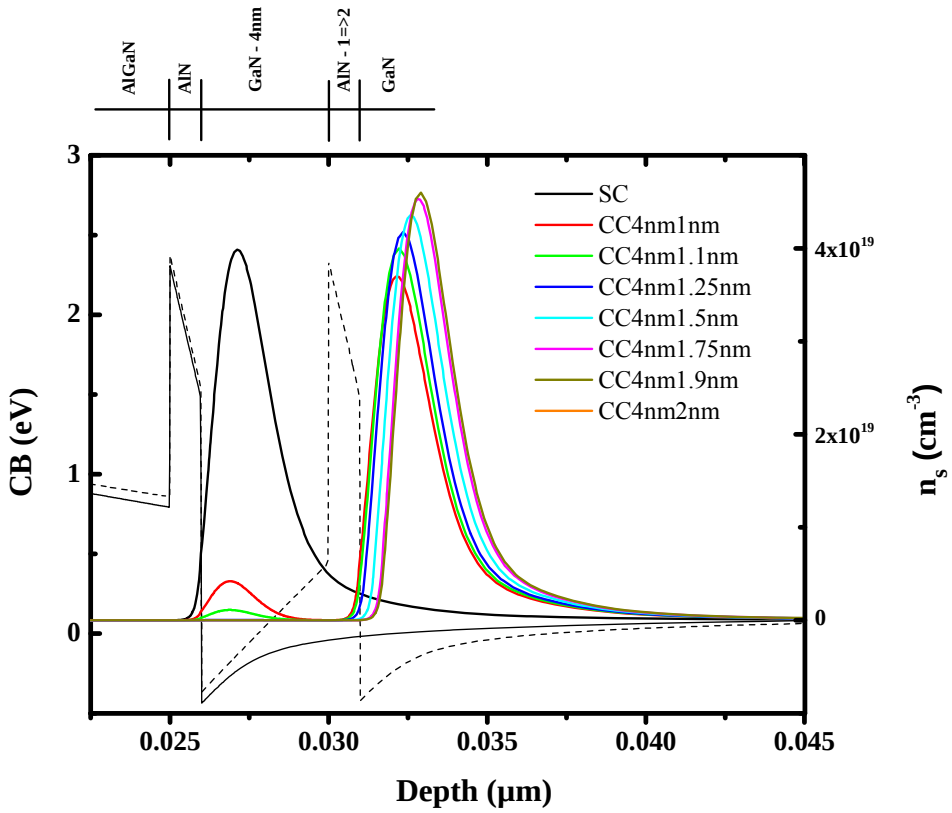


Figure 5.3 Coupled channel heterostructure. AlN separation layer thickness (1≤2nm) effect on carrier density profile. Left axis indicates conduction band (CB), right axis carrier density (n_s). Thin continuous line is the CB for single channel (SC) heterostructure and dashed line for couple channel heterostructure for a GaN layer 4nm thick and a separation layer 1nm.

More interesting results are obtained when AlN separation layer is thinner than 1nm. Reduction of separation layer has the effect of redistribute carriers among channels (see Figure 5.4). As AlN layer thickness goes from 0 to 1nm the carrier profile changes of

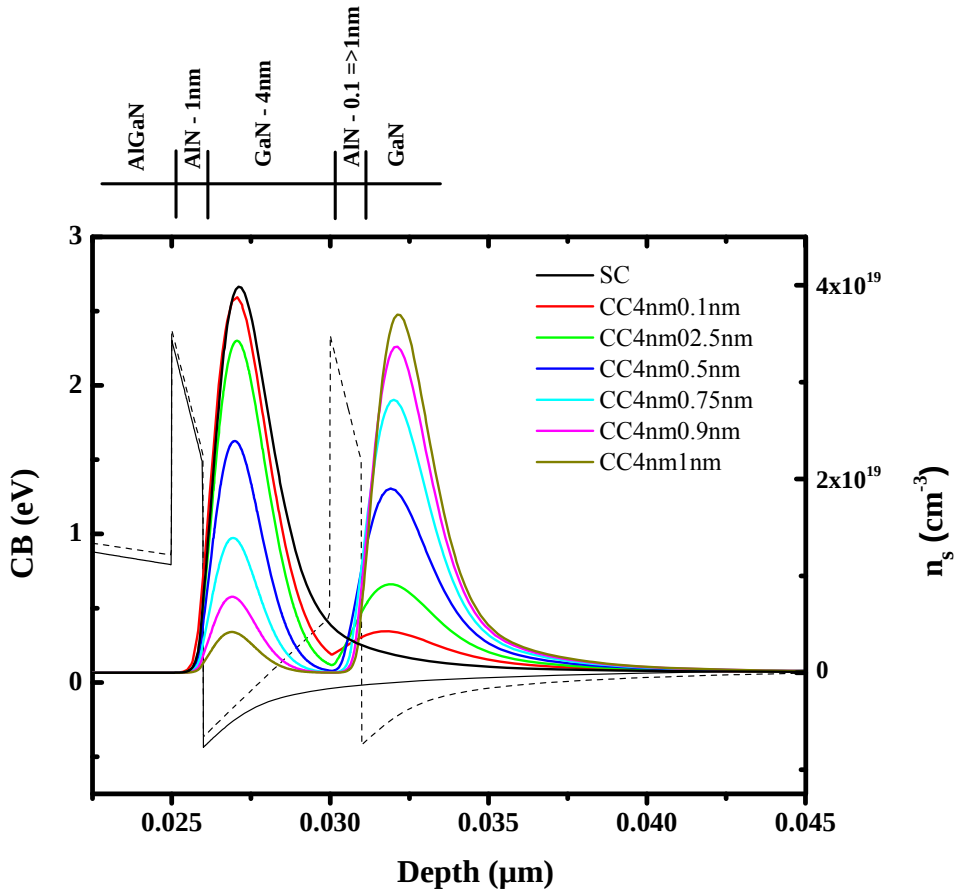


Figure 5.4 Coupled channel heterostructure. AlN separation layer thickness (≤1nm) effect on carrier density profile. Left axis indicates conduction band (CB), right axis carrier density (n_s). Thin continuous line is the CB for single channel (SC) heterostructure and dashed line for couple channel heterostructure for a GaN layer 4nm thick and a separation layer 1nm.

character. From single peak like in the top channel, splits into two peaks one in each GaN channel and for AlN 1nm thick carrier are concentarted mostly in the botton channel. Notice that for a AlN 0.5nm thick a balanced distribution of the carriers among the channel is achieved and what is desirable. Also, the effect of the separation layer composition was evaluated via simulation (see Figure 5.5). The effect of the separation layer composition is similar to the AlN separation layer for thickness lower than 1nm. For decreasing Al content in

the separation layer the carrier distribution changes from a crrier profile mostly concentrated in the botton channel to a profile that acumulates carrier in the top channel. For intermediate Al concentration (50%, not show here) ist is expected a balanced distribution of the carrier among the channels. Balanced distribution of carrier is desirable because plasmon-hot phonon resonance is expected to be atained at higher carrier densities, therefore, higher power levels.

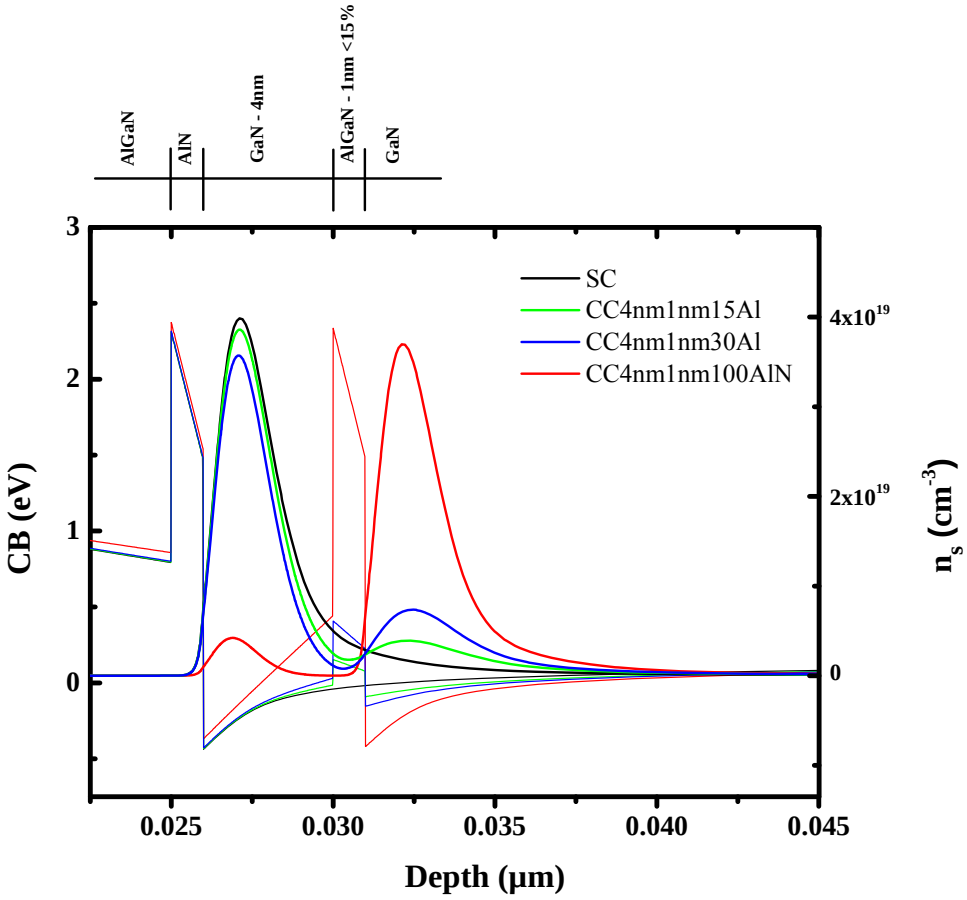


Figure 5.5 Coupled channel heterostructure. Separation layer composition effect on carrier density profile. Left axis indicates conduction band (CB), right axis carrier density (n_s). Black thin continuous line is the CB for single channel (SC) heterostructure and red continuous line for couple channel heterostructure for a GaN layer 4nm thick and AlN separation layer 1nm thick.

5.2.2 Dual Channel HFET

In the case of dual channel heterostructures, the effect of both the Al content in the AlGaN channel and the channel thickness were simulated. Heterostructures with AlGaN channels 4nm thick and 10, 15, and 20% Al content were simulated, results are shown in Figure 5.6. First observation is that the carrier density profile is compact.

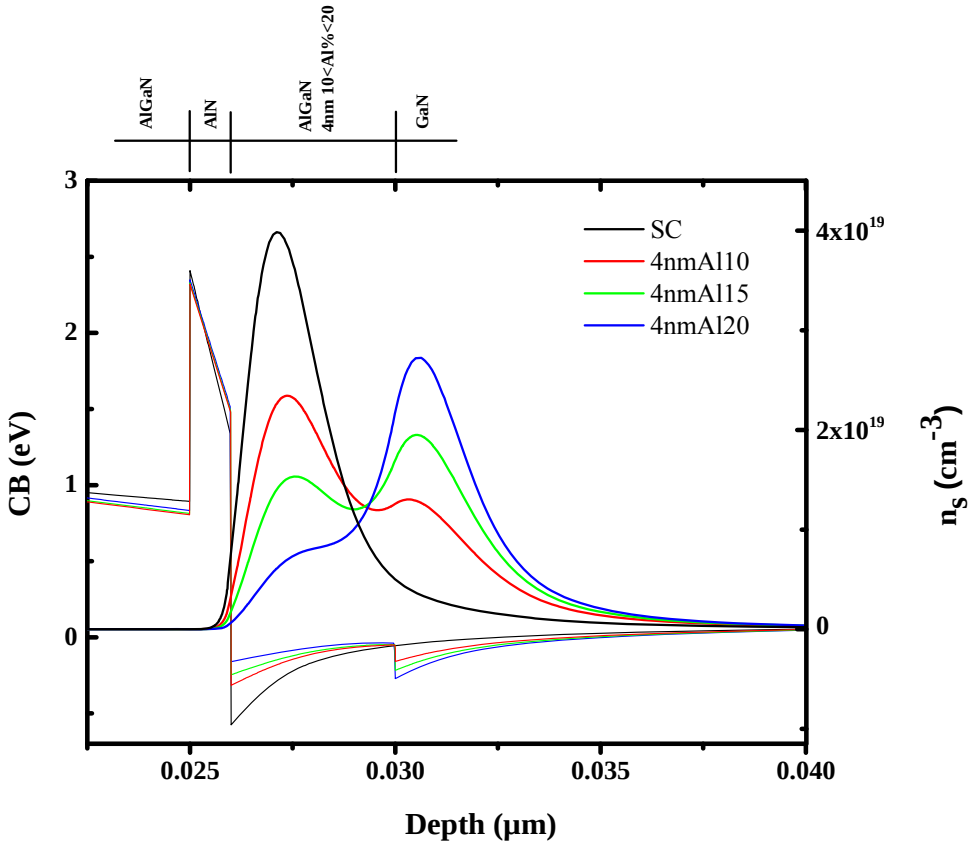


Figure 5.6 Dual channel heterostructure. Effect of the Al content in the AlGaN channel in the carrier distribution. Left axis indicates conduction band (CB), right axis carrier density (n_s). Thin black line is the electron density profile for single channel (SC) heterostructure.

Channel with low Al content behaves pretty much like single channel. However, as Al content is increased the carriers concentrate more in the channel located in the buffer layer

(bottom channel). The latter can be seen as beneficial from the point of view of a possible reduction of the alloy scattering at low electric field. However, a 15% Al content result in a better profile for a plasmon-hot phonon resonance at higher carrier densities at higher applied electric fields. Figure 5.7 shows simulation results for an AlGaN channel with 20%Al content and 2, 3, and 4nm thick. The AlGaN channel thickness seems to be not as effective as the channel Al content in widening the carrier profile. Even though, the carrier profile can be widen a peak like prevails. Thicker AlGaN channel concentrate carrier in the buffer side which could be beneficial from the point of view of transport properties of the channel. However, the carrier profile resembles a single channel profile.

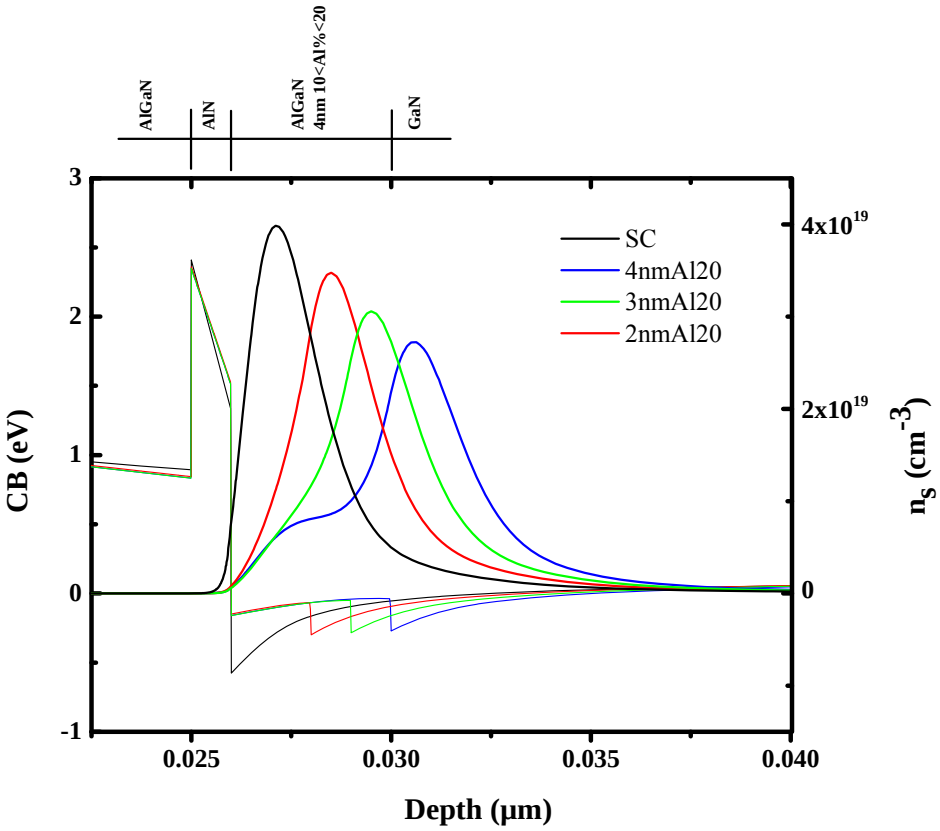


Figure 5.7 Dual channel heterostructure. Effect of the AlGaN channel thickness on the carrier profile. Left axis indicates conduction band (CB), right axis carrier density (n_s). Thin black line is the electron density profile for single channel (SC) heterostructure.

5.3 **Heterostructure Growth**

Heterostructures were gown on 2" *c*-plane sapphire substrate utilizing a vertical low pressure metal-organic chemical vapor deposition (MOCVD) system in which trimethylgallium (TMG), trimethylaluminium (TMAl), and NH_3 was used as Ga, Al, and N precursors, respectively, and Hydrogen was used as carrier gas. Following, a description of the heterostructure growth process is presented. Low temperature AlN nucleation layer with thickness of about 20nm grown at growth temperature about 900°C was followed by a 330nm thick AlN at high substrate temperature (1050°C) and pressure of 30Torr and V/III ratio of ≈7. Growth of GaN was performed in 2 step process. First, a 1μm thick layer at 76 Torr was grown to introduce a carbon compensated layer which acts as a semi-insulating buffer. Then, 2.5 μm of GaN at 200 Torr was grown to improve crystal quality which is an important factor in high mobility heterostructures. On top of the buffer layer, a 1nm thick AlN was deposited, separation layer, this layer helps to improve electron transport properties. Thereafter, a 20nm thick $Al_{0.3}Ga_{0.7}N$ barrier layer was grown followed by a 2nm of GaN cap layer to protect the barrier from oxidation. All the last three stages were grown at chamber pressure of 76Torr and a V/III ratio of 910 at same substrate temperature as that for the underlying GaN buffer layer. In case of coupled-channel structure an additional 1 nm separation layer followed by 4nm layer was deposited on top of the original spacer layer (see shown Figure 5.1 b)). For dual channel structure, an additional $Al_{0.15}Ga_{0.85}N$ layers was grown on top of GaN buffer layer (see Figure 5.1 c)).

5.4 Thermal conductivity in heterostructures

In order to evaluate the thermal conductivity as seem from the channel and especially from the top channel in multichannel heterostructures i.e. dual and coupled channel where heat flow could be impeded by subsequent layer, we calculate the effective thermal conductance between two points A and B using the series model as displayed in Figure 5.8. The figure shows an array of three layers, AlN/GaN/AlN, that essentially may be the path through which the heat generated in the channel of single channel heterostructure need to go to reach the substrate (see Figure 5.9 a)). The same concept applies to dual and couple channel.

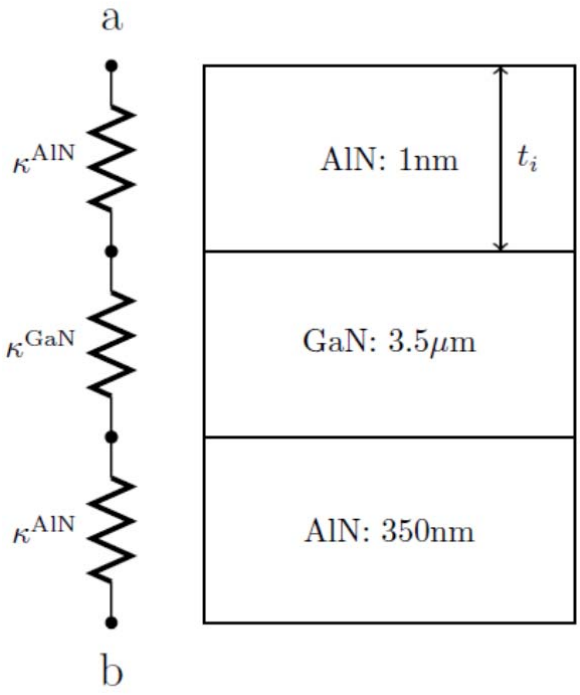


Figure 5.8 Thermal conductance series model to calculate the effective thermal conductance from a to b. Shown in the figure is the case for single channel heterostructure

The series model for the effective thermal conductance between point a - b is given by [96]

$$\kappa_{\text{eff series}}^{\text{ab}} = \frac{\sum_{i=1}^{N} t_i}{\sum_{i=1}^{N} \left({}^{t_i}/_{\kappa^i} \right)}$$

where t_i is the thickness of the $i-$sima layer, κ^i the thermal conductance of the $i-$sima layer, and N runs from 1 to total number of layers. The thermal conductance for binaries materials at a temperature, $\mathrm{T_L}$, can be calculated by the power law

$$\kappa(\mathrm{T_L}) = \kappa_{300} \left(\frac{\mathrm{T_L}}{300\mathrm{K}} \right)^{\alpha}$$

where κ_{300} is the thermal conductance at room temperature (300K) and α is a fitting parameter. In the case of ternary alloy materials, $\mathrm{A}_{1-x}\,\mathrm{B}_x\,\mathrm{C}$, the thermal conductance of the material, $\kappa_{300}^{\mathrm{ABC}}$, varies between the values of $\kappa_{300}^{\mathrm{AC}}$ and $\kappa_{300}^{\mathrm{BC}}$. $\kappa_{300}^{\mathrm{ABC}}$ can be calculated via harmonic mean ($\frac{1}{H} = \frac{1}{n} \frac{1}{\sum_{i=1}^{n} a_i}$, H is the harmonic mean of n real values, a_i) model of the conductance at 300K and which given by

$$\kappa_{300}^{\mathrm{ABC}} = \left(\frac{x}{\kappa_{300}^{\mathrm{AC}}} + \frac{(1-x)}{\kappa_{300}^{\mathrm{BC}}} + \frac{(1-x)x}{C_\kappa} \right)^{-1}$$

where C_κ is an additional bowing factor introduced in order to account for the drastic reduction of the thermal conductivity with the increasing alloy compositions.

Exponent is linearly interpolated as

$$\alpha^{\mathrm{ABC}} = (1-x)\alpha^{\mathrm{AC}} + x\alpha^{\mathrm{BC}}$$

where α^{AC} and α^{BC} are the fitting parameter for the binary alloy $\mathrm{A}_{1-x}\,\mathrm{B}_x$ and $\mathrm{B}_{1-x}\mathrm{C}_x$, respectively.

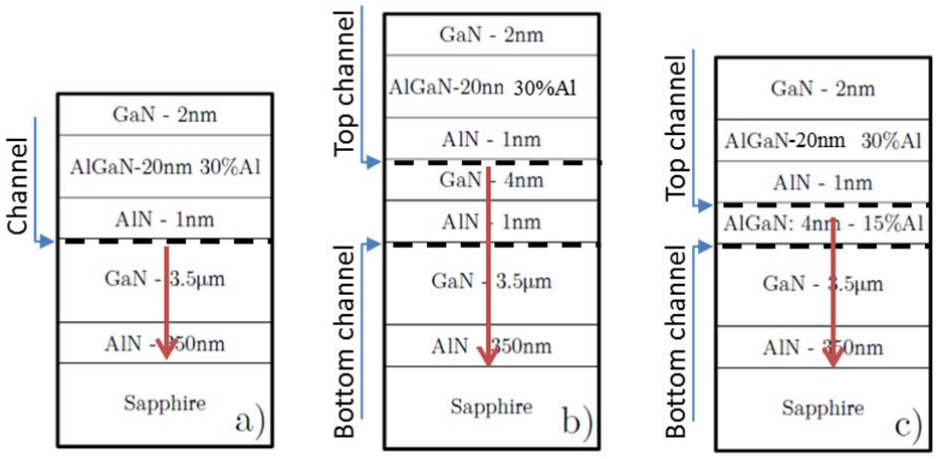


Figure 5.9 HFET structures a) single channel (SC), b) coupled channel (CC), and c) dual channel (DC). Red arrows indicate calculated thermal conductivity, start positioned at the top channel, end points the substrate.

Then the thermal conductivity for ternary alloys materials at a temperature, T_L, can be calculated by the power law

$$\kappa^{ABC}(T_L) = \kappa_{300}^{ABC}\left(\frac{T_L}{300K}\right)^{\alpha^{ABC}}$$

In our calculations we use the following values of thermal conductivity, power constant, and bowing factor, $\kappa_{300}^{AlN} = 3.5\ W/cm\ K$, $\alpha^{AlN} = -1.7$, $\kappa_{300}^{GaN} = 2.2\ W/cm\ K$, $\alpha^{GaN} = -1.2$, $C_\kappa = 0.031\ W/cm\ K$ (for AlGaN alloys). AlN, GaN and AlGaN thermal conductivities as a function of the temperature for 1%Al, 15%Al, and 99.9%Al, are shown in Figure 5.10 a), c), and e), respectively. As expected in all cases, the thermal conductivity decreases as the temperature increases. As the Al composition goes from zero to 100% the thermal conductivity of AlGaN changes from the value for GaN to the thermal conductance value for AlN. As observed in Figure 5.10 b), d), and d) the change in the thermal conductance from (top) channel to the substrate in single and multiple channel heterostructures is insubstantial.

However, the effect of Al content is notorious in dual channel heterostructures, especially, for 15Al% (see Figure 5.10 d). Nevertheless, the difference in the thermal conductance between the dual channel heterostructure and coupled channel which is very close to the single channel conductivity is ≈ 2%. Variation on the thermal conductance as a function of the Al content in AlGaN at 300K is displayed in Figure 5.11 a). AlGaN thermal conductivity exhibits a minimum (plateau like) with a value of $\approx 0.25\ \mathrm{W/cm\,K}$ for 15%Al content. It is worth to evaluate the effect of Al% in AlGaN in the dual channel thermal conductance and which shown in Figure 5.11 b). We are interested in 10 < Al% < 20 range of Al content for which the AlGaN contribute more efficiently to the widening of the 2DEG profile. For this range of Al content the variation in the thermal conductivity of AlGaN is ≈1%.

In summary, the higher the temperature and the larger the Al content (< 50%) in AlGaN channel the lower the conductivity. For 1<AlGaN layer thickness < 5nm and 0< Al% < 50 the change in thermal conductivity is lower than 2%. Therefore, it is expected as shown in Figure 5.10 b), d), and d) that the thermal conductivity in the single and multiple channel be govern by the thermal conductivity and thickness of GaN buffer layer (3.5μm thick GaN layer, see Figure 5.9 a), b), and c)).

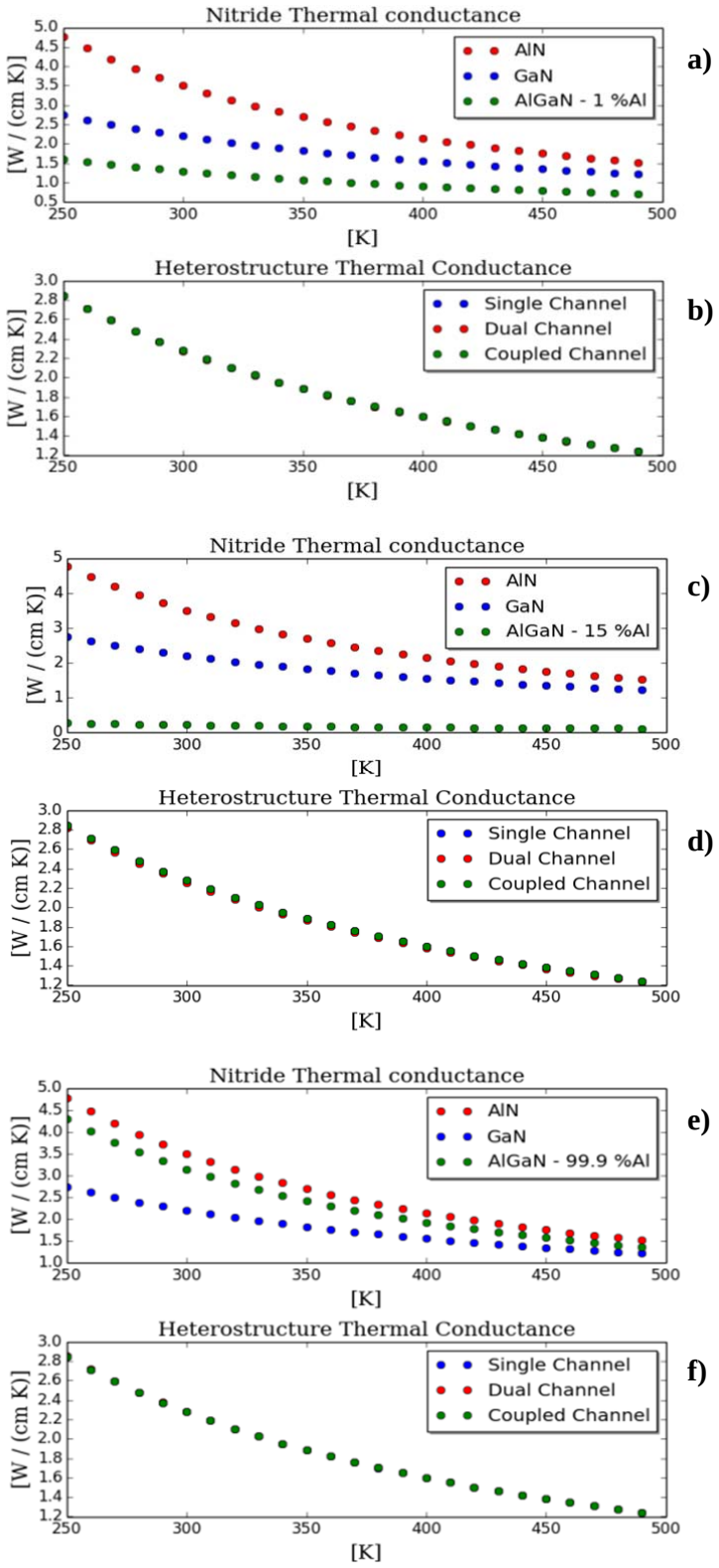


Figure 5.10 Thermal conductance as a function of the temperature for AlN, GaN and AlGaN for 1%Al, 15%Al, and 99.9%Al are shown in a), c), and e), respectively. b), d), and f) thermal conductance from (top) channel to substrate for single-dual and couple channel heterostructures.

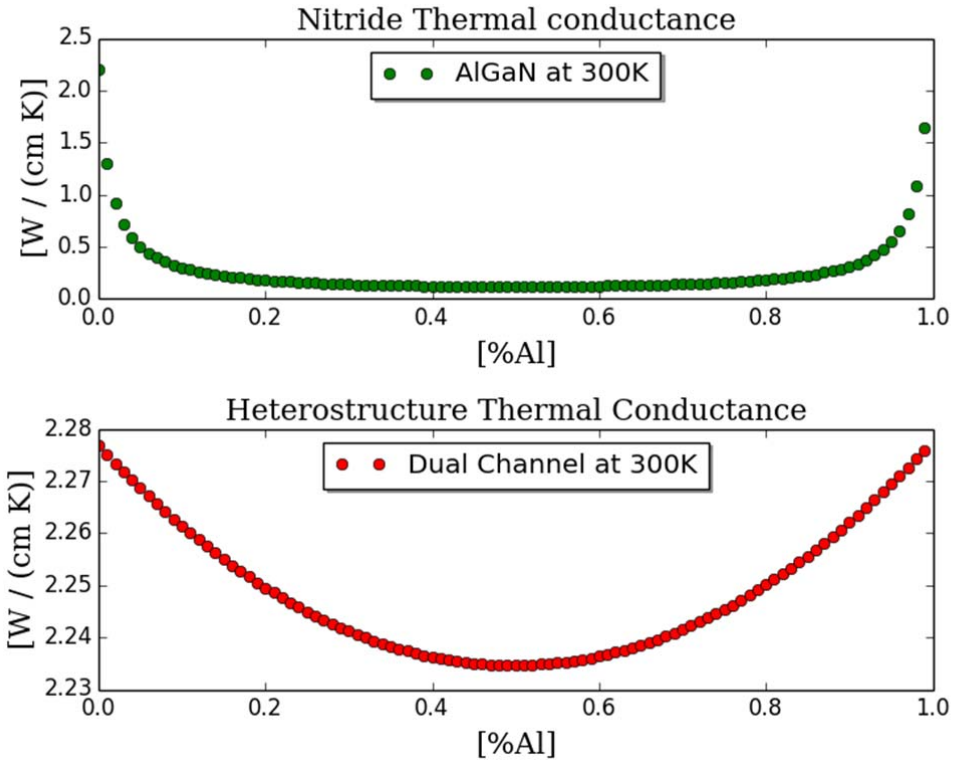


Figure 5.11 a) Thermal conductance variation for a 4nm thick AlGaN layer as function of Al content, b) Change in the thermal conductance of dual channel heterosturucture (Figure 5.9 c)) as a function of the Al content in the AlGaN channel.

5.5 Device fabrication

After heterostructures are grown, ohmic contacts Ti/Al/Ni/Au (30nm/100nm/40nm/75nm) are deposited via E-beam and thermal evaporation. Then MESA etch by dry etching (Cl_2 reaction). Next, ohmic contacts are annealed under nitrogen atmosphere at 800-940°C for 20-60s. Finally, Schottky contacts Ni/Au (300nm/75nm) are deposited. A picture of fabricated devices is shown in Figure 5.12. Devices are compound of two (gate (G), source 1 (S1), drain (D), and G, source 2 (S2), and D) HFETs with common drain and gate. The gate length is 1-2μm, channel width is 90 μm. Source – gate separation is 1-1.5μm, and gate-drain separation 2-4μm. The recipes used to carrier out the photolithography process are in the APPENDIX B. The recipe for photolithography process for MESA etching results in undercut photoresist profiles, which allows a better access to the HFET channel. The photolithography process for metal contact deposition produce overcut profiles ideal to obtain acute and clean metal profiles.

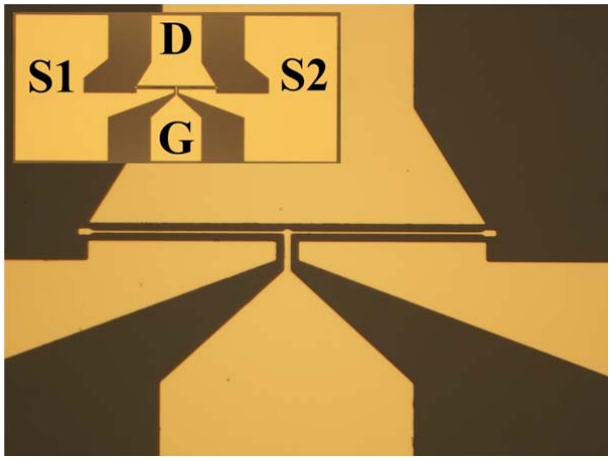


Figure 5.12 Optical image (top view) of fabricated devices composed by two HFETs. Indicated in the insert are gate (G), drain (D), source 1 (S1), and source 2 (S2).

5.6 Electrical characterization

5.6.1 Heterostructures

The entry level electrical characterization of the heterostructures is accomplished via Hall measurements-Van der Paw configuration at room temperature. Hall measurements results are decisive for further sample processing. This technique provides the carrier nature (holes – electrons) and its density (including parallel conduction if any). It should be pointed out that HFETs based on GaN/AlGaN or GaN/InAlN heterostructures such as the ones shown in Figure 5.1 exhibit always *n*-channels. In all studied cases mobility was around $1x10^3$ cm^2 $V^{-1}S^{-1}$ or higher and 2DEG density higher than 1.2 $x10^{13}$ cm^{-2}. Samples with lower carrier mobility and/or carrier density are discharged from the study.

5.6.2 Devices

Direct current voltage-current characteristics either both input, gate-source voltage (V_{GS})-gate current (I_{GS}) and output, drain-source voltage (V_{DS}) - drain current (I_D), as well as transconductance (Gm) were measured and used to evaluate the DC performance of the devices. Devices with I_{GS} <100 μ mm^{-1}, Gm >100 mS mm^{-1}, and I_D > 350 mA mm^{-1} were selected. High I_D is mandatory for high power applications. Gm is capital for power amplifier gain. While a low I_{GS} (leakage current) level is important to reduce I_{GS} side effects (i.e. drain current lag and poor device reliability), it is also relevant for a meaningful low noise frequency characterization of the device.

Capacitance-voltage (C-V) measurements were accomplished with a RLC meter. From the C-V measurements, apparent carrier concentration profile, *n* (cm^{-3}) normal to the growth direction versus depth (nm), were calculated by using the equations:

$$n = \frac{2}{qK_s\epsilon_o A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV}}$$

$$\text{depth} = \frac{K_s\epsilon_o A}{C}$$

n vs depth curves were used to judge the widening of the carrier concentration. Standard heterostructure exhibits, usually, a narrow peak. While multiple channel HFETs, usually, present one or two peaks. And in general the carrier concentration profile is wider than that for a standard structure. Knowledge of the carrier density profile is important in terms of evaluation of the effectiveness of the heterostructure on widening the 3DEG density profile. It worth to mention that results from C-V profile should be taken "qualitatively" since this method has several limitation. Among which Debye length is the most important in the definition of the carrier density profile (see APPENDIX A).

Measurement of **s-parameters** is carried out with a vector network analyzer in the range of frequencies 2-20GHz. Cut-off frequency, f_T, defined as extrapolation of $|h_{21}|^2$ to zero dB. And h_{21} short circuit current again, is calculated from s-parameters as

$$h_{21} = (i_2/i_2)|_{v_2=0} = \frac{-2s_{21}}{(1-s_{21})(1+s_{22})+s_{21}s_{21}}.$$

Gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) at which f_T is achieved are recorded for further analysis. Studied devices exhibit a f_T in the range 10-14 GHz. This technique is crucial to evaluate the bias point at which plasmon-hot phonon resonance in gated HFETs is attained. Since no other technique is applicable. s-parameters together with a HFET small-signal equivalent electrical circuit Figure 5.13 help to find out extrinsic and intrinsic parameters by extraction techniques. Then it is possible to reconstruct the intrinsic equivalent

circuit. Of principal interest are gate-source capacitance (C_{gs}), and gate drain capacitance (C_{gd}). Which are related with the intrinsic cut-off frequency in the following manner

$$f_{T,int} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{v_{sat}}{2\pi L_g}$$

where g_m is the small signal transconductance, v_{sat} the saturation velocity, and L_g the gate width.

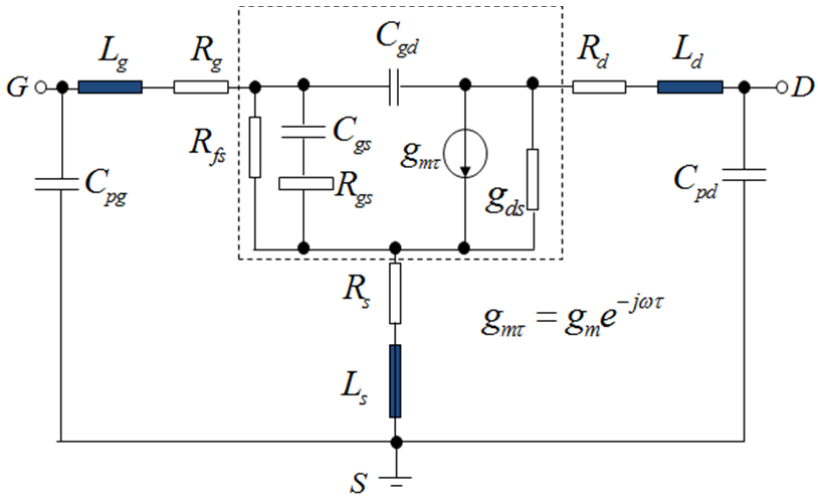


Figure 5.13 HFET equivalent small signal circuit.

Extrinsic parameters are useful in finding out a better approximation to the real conditions, electric field in the channel, at which cut-off frequency occurs. That is to say, bias conditions at which phonon effects are minimized. From the measurements of the f_T, intrinsic transient time, τ_{int}, is calculated. Under high electric field but lower than critical electric field (E_{cri}), shorter τ_{int} implies higher saturation carrier velocity,v_{sat}, therefore, shorter hot-phonon lifetime. τ_{int}, is calculated as follow, the total transient time is $\tau_{Total} = \tau_{int} + \tau_D + \tau_{RC} = (2\pi f_T)^{-1}$, where τ_D is the drain time constant and τ_{RC} is the charging delay time constant. From the τ_{Total} versus channel voltage, $V_{ch} = V_{DS} - I_D (R_S - R_D)$, and τ_{Total} versus $1/ I_D$ characteristics

we obtained $\tau_{int} + \tau_{RC}$ and $\tau int + \tau_D$, extrapolating τ_{Total} , respectively, for V_{ch} and $1/ I_D$ tending to zero.

In order to evaluate the **reliability of the devices**, a series of stress at four different bias points were carried out. The bias points are: (1) on-state-low-field stress ($V_{GS} = 0$ V, $V_{DS} = 7$ V), (2) reverse-gate-bias stress ($V_{GS} = -20$ V, $V_{DS} = 0$ V), (3) off-state-high-field stress ($V_{GS} = -10$ V, $V_{DS} = 20$ V), and (4) on-state-high-field stress ($V_{GS} = 0$ V, $V_{DS} = 20$ V). Mentioned electrical stress tests are realized, also, at high temperature, up to 200°C.

Low frequency noise (LFN) characterization of the devices before and after stress them is accomplished with the help of a phase noise measurement system. See Figure 5.14. Characteristic noise signal from HFET are built up, usually, by a superposition of $1/f$–like noise, generation-recombination (G-R) noise, and white noise. The latter, frequency independent is related with the device temperature and impose a minimum detectable noise level. In practice this level is set by either both the device under test (DUT) or the set up used to measure the noise. In this case our Test set has a noise level well below -180 dB V/Hz, which corresponds to a power density of -167dBm/Hz at an input impedance of 50 Ω. The thermal noise power density is -174dBm/Hz, which is about 7dB lower compared to the noise floor of the Test set.

G-R noise in semiconductors is related with the generation and recombination of carries. G-R results in a fluctuation in the number of carriers contributing to the current transport. G-R power spectrum density (PSD), Lorentzian in nature, is given by the McWhorter's number fluctuation as follow:

$$S_N(f) = \overline{4\Delta N^2}\frac{\tau}{1 + (2\pi f)^2\tau^2}$$

where τ is the trap time constant and f belongs to the noise frequency spectrum.

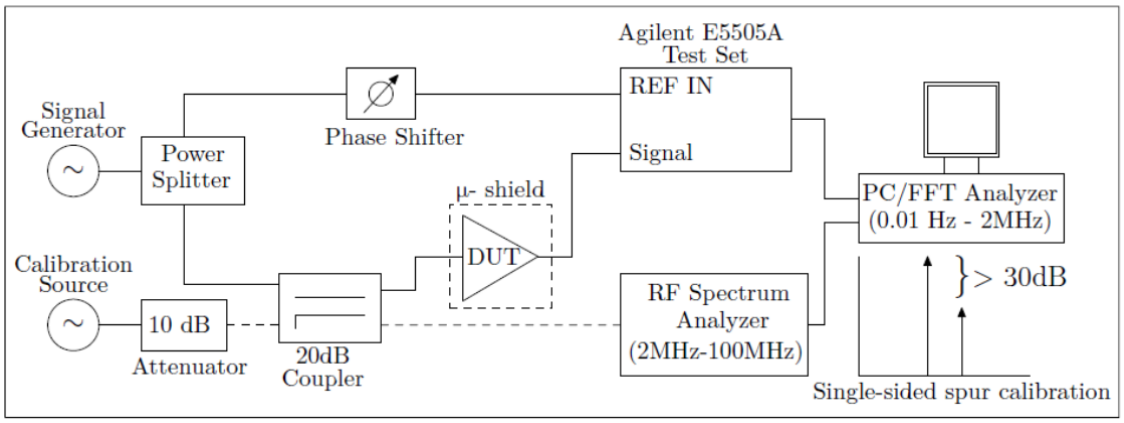


Figure 5.14 Block diagram shows the Agilent E5505A residual phase-noise measurement setup with the single-sided spur calibration technique. Calibration source and 10 dB attenuator attenuator are only used for calibration purpose. DUT stands for device under test.

When a large number of trap (number fluctuation) are presented, G-R noise exhibit $1/f$ –like noise provided trap time constant are distributed as follow:

$$g(\tau) = \frac{1}{\ln\left(\frac{\tau_2}{\tau_1}\right)\tau} \qquad \tau_1 < \tau < \tau_2, \qquad g(\tau) = 0 \quad \text{otherwise.}$$

Because G-R noise is relevant within a few kT from the Fermi energy level and owing to the pining of Fermi energy level in nitrides, G-R noise in nitrides is mostly due to the deep traps. Traps closer to the conduction or valence band will stay most of the time either empty or filled. PSD general expression for $1/f$ –like noise is proportional to $1/f^{\gamma}$, with $0.3<\gamma<1.3$. γ is found from the phenomenological relation between $1/f$ and the inverse of the total number of charge carriers, N, in the channel in homogeneous samples. This relation is called Hooge and is given by:

$$\frac{S_I(f)}{I} = \frac{\alpha_H}{Nf} = \frac{\gamma}{Af}$$

where $S_I(f)$ is the current spectral density, α_H is the dimensionless Hooge's parameter, N is the number of electrons scattered by A lattice nodes.

Fluctuation in current may be caused by either both mobility fluctuation and number carrier fluctuation. Carrier fluctuation can be described by McWhorter's number fluctuation, while mobility fluctuation can be described by Hooge phenomenological formulation. Both fluctuations may exhibit $1/f$ –like PSD. Therefore, sometimes it is not possible to discerner between carrier or mobility fluctuations. And extra measurements (e.g. pulse measurements, high temperature measurements) and or stress the device are necessary in order to elucidate the nature of noise. Difference in LFN levels is an indication of the degradation of the device after being stressed. It is expected, for example, that when the stress takes place under plasmon-hot phonon resonance conditions, the device be minimally degraded because the effect of hot phonon is minimized. In order to corroborate result from the stress/measurements usually an ensemble of the devices on the same sample is studied, and a representative value is taken for every single measured variable.

5.7 Approach

Owing to the lack of a theory may take into account all factors, which could intervene in the plasmon-phonon resonance bias point, there is so far, no other direct option than the experimental one. In other words, growth the heterostructures, fabricate devices on them and find the bias points at which cut-off frequency occurs. If the bias point does not approach to V_{GS} =0V at high V_{DS} voltages, the growth, fabrication and testing processes need to be repeated until some satisfactory result is attained. After an evaluation of the obtained results, new directions on the heterostructure design are taken, if necessary. Of course, all experiment work is sustained by a theoretical background. And this work is not the exception. Theory is appealed as required. In order to understand the electron-phonon physics in the heterostructures and then guide the design of the heterostructures. Also, TCAD simulations

are carried out to evaluate the electron wave function profile, carrier density, and electric field distribution among other parameters.

The heterostructure design optimization process starts with the growth of the heterostructure on sapphire substrate (for low cost, SiC or even better GaN substrates would be ideal, but they are prohibitive) by MOCVD technique; see Figure 5.16 for the explanation of the optimization process. Two innovative heterostructures for the implementation of HFET, namely, coupled channel and dual channel are object of the optimization process. Also, and as reference, standard heterostructures named single channel are growth (see Figure 5.1 a)). The latter are used for device performance reference. Following heterostructure growth, substrates are cut as indicated in Figure 5.15. The Figure 5.15 also shows the relative position of the HFET's gate with respect to the *c*-sapphire substrate *m*-plane. Gates are aligned parallel to the substrate *m*-plane, because it is believed that defect density in the perpendicular direction to the *m*-plane, where sit the HFET channel, is lower.

Small samples of 5x5 mm^2 are used to characterize heterostructure transport properties via Hall measurements in the Van der Paw configuration. Mobility higher than $1x10^3$ cm^2v^{-1} s^{-1} and carrier density higher than $1x10^{13}$ cm^{-2} are used as sample selection rule. In the case the sample does not satisfied the mentioned condition no further sample processing is carried out. After Hall measurement, remaining pieces of wafer are processed in the following way. Remaining piece of pie shape used for Hall measurement is used to fabricate of TLM devices (see Figure 5.15). These devices help in the optimization of ohmic contact rapid thermal annealing (RTA) process. The optimization is realized by finding best combination of annealing temperature and annealing time under a nitrogen atmosphere. As a feedback, I-V characteristic curves of the TLM patterns are used to calculate electrical properties of the ohmic contacts.

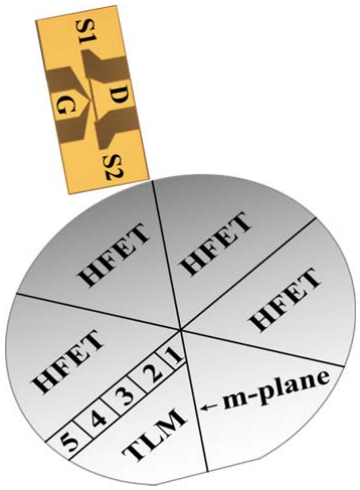


Figure 5.15 Substrate cutting details. Pieces 1-5 are dedicated to Hall measurements. Pie shape indicated as TLM is destinated to the fabrication of TLM devices. Remaining pie-shapes are used for the fabrication of HFET devices.

The lower the specific contact resistance, $\rho_{c,}$ the better the ohmic contact. Values of $\rho_{c,} \approx 1x10^{-6}$ Ω cm^2 are considered good and the annealing conditions are accepted. Once implemented the ohmic contacts, gateless HFETs are DC characterized. Obtained I-V curves are used as reference to discriminate the metal gate effect on the 2DEG density, unintentional depletion.

Continuing with the fabrication process, gates are deposited by E-Beam evaporation. Then first, direct current characterization results of the HFETs are used to screen devices. Only are chosen for further studies those devices that exhibit good drain current, I_D (>600 mm A^{-1}) and transconductance, Gm, $\geq$ 100 $mSmm^{-1}$. Also C-V measurements are taken on fat FET in order to calculate the 2DEG density profile. This measurement is important in terms of the evaluation of the 2DEG profile widening that multichannel structure may cause if compared with the 2DEG profile of a standard structure.

Selected devices are RF characterized. The RF performance is evaluated via s-parameters. Which are used for the calculation of the cut-off frequency. Scanning in V_{GS} and V_{DS} is executed to find out the bias conditions at which f_T occurs. f_T is an indicator of when minimum effect of hot phonons happens. And is a crucial parameter for the performance, in terms of plasmon-hot phonon interaction in the heterostructure. To find out if the f_T is influenced by the carrier velocity frequency values are, in conjunction with the bias points, further processed in order to find out the internal transient time. The latter is related with the carrier saturation velocity, $V_{sat} = Lg/\tau_{int}$. If V_{sat} occurs at high electric field but lower than critical electric field, E_{cri}. It means that the possible difference in V_{sat} among samples is due to mobility. Increase of mobility is related, at the same time, with a reduction of the hot phonon lifetime. Otherwise, the relation between τ_{int} and hot phonon is no trivial, because the carriers begin to populate higher valleys and a new effective transient time, τ_{eff}, need to be defined. This new τ_{eff} does not relate directly mobility with the hot phonon lifetime.

If the bias point at which f_T occurs, approaches to V_{GS} = 0V, a whole evaluation of the device performance is carried out. And decisions on fine tuning of the heterostructure design are taken. Otherwise, heterostructure efficiency in widening the 2DEG density profile and possible reasons on why V_{GS} does not approach to 0V are analyzed. And new decisions on heterostructure designs are taken.

The whole optimization process, of course, is an iterative one. And values of V_{GS} approaching to 0V are expected to be achieved cycle after cycle. Iteration, always, starts from growth process. See Figure 5.16 for a description of the entire flow process.

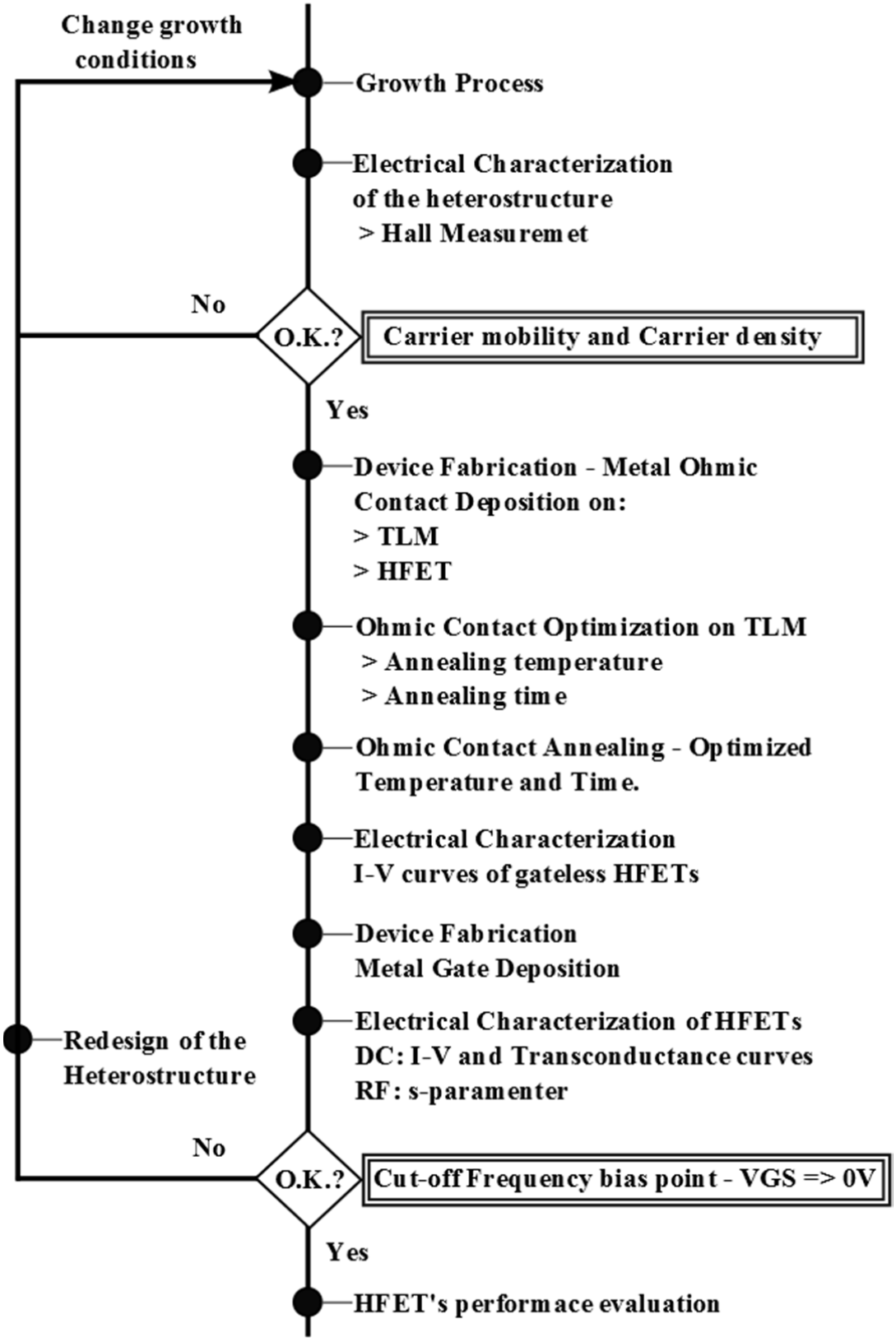


Figure 5.16 Heterostructure design optimization process flow.

Chapter 6. Experimental results

GaN-based heterostructure field effect transistors exhibit remarkable performance in the high frequency and high power applications [63]. The reliability of GaN-based power devices is still focus of intense research in order to improve their performance and extend their lifetime, since the devices still suffer from some degradation mechanisms such as mechanical stress due to high electric field, strain, electrical defects and hot electron/hot phonon effects. For instance, the drain current collapse (gate lag) is attributed to the charge traps located in the buffer layer, barrier region or the surface states mostly residing on the drain side of the gate [97]–[100].

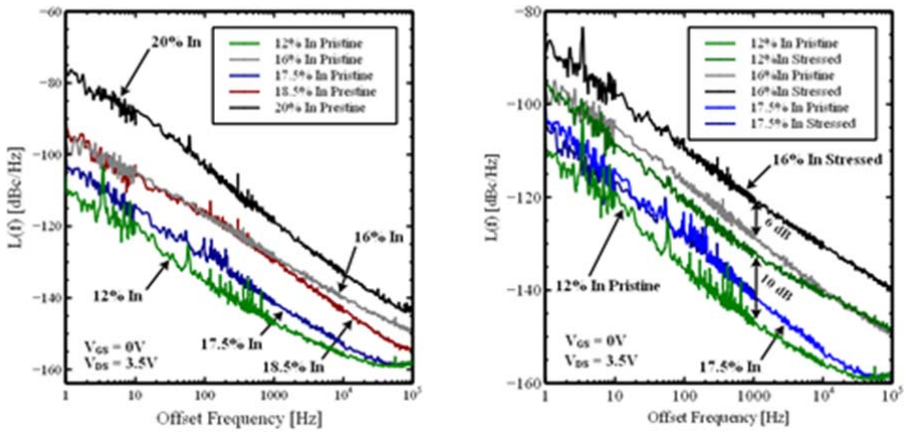
For high power application, as mentioned earlier, channel capable to conduct high current densities are desirable. In this vein first devised theoretically [101] and then implemented [102], InAlN/GaN heterostructures offer a mean to supply the increasing power demand. Increase of power handling with conventional AlGaN barrier layer, mainly, means increase Al%. This approach has a limitation and this is that for Al% higher than ~37% Al in AlGaN barriers layers on GaN start to relax. And the piezoelectric component of the polarization induced charge begins to be diminished. Increasing barrier layer thickness do not make any substantial increase in the induced charge with the side effect of degrading the DC and RF performance of the HFET i.e. pinch-off voltage, Vpo, and f_T.

6.1 Single channel HFET – InAlN barrier layers

InAlN barrier layers induce higher charge levels in the channel (~ 0.9 A/mm, see Figure 6.2 curve corresponding to a 17.5%In) as compared with AlGaN barrier layers (0.6 A/mm for 25%Al, not shown here). Therefore, InAlN/GaN HFETs are, a priori, capable to handle higher power level.

Replacing the AlGaN with an InAlN barrier layer, due to its lattice-matched growth possibility, larger band-gap leads to higher current densities compared to the counterparts with AlGaN barriers [101], [103], [104]. Even though there are an increasing number of studies on structures with InAlN barriers delving into the lattice parameter effect, i.e. the impact of Indium composition [104]–[106], the study of In-composition effect on reliability was missing. Hot phonon and hot electron/phonon effects in InAlN/AlN/GaN HFET were reported in Refs. [107] and [108]. The study on off-state electrical stress in InAlN/AlN/GaN HFETs with varying In compositions [109] is presented here. Optimized InAlN/GaN heterostructure designs like the shown in Figure 5.1 d) were studied. We monitored low-frequency noise (LFN) for the HFETs with InAlN barriers with In compositions varying from 12% to 20% to investigate the impact of electrical off-state stress (V_{GS} = -10 V, V_{DS} = 0 V, and I_D = 0 A - Inverse-Piezoelectric stress) in the context of inverse piezoelectric effect.

Figure 6.1 a) exhibits the resulting curves of LFN measurements before stress. Mostly, the noise characteristic of the samples follows 1/f type. However, in some of the LFN curves slight features were observed deviating from 1/f, indicating generation recombination noise. Because these features are contemplated (for 18.5% and 20% In) pre and post-stress conditions, it is feasible to attribute them to the GaN buffer, in which case it can be concluded that there was no additional trap generation under the above mentioned stress conditions. Figure 6.1 b) shows pre- and post-stress LFN curves for the lattice matched condition (17% In) and for the ones with the In compositions below the lattice matched condition (12% and 15%). We observed that LFN spectra for the HFETs with the In compositions higher than the lattice matched conditions (18.5% and 20%) remained almost the same (no shown in the Figure 6.1 b)).



a) b)

Figure 6.1 a) LFN measurement on pristine samples. Distinct features can be observed for 15%, 18.5%, and 20% In, indicating generation-recombination noise. b) pre and post-stress LFN curves for 12%, 15%, and 17% In composition. HFETs with 18.5%, and 20% In compositions (not shown) showed no change in noise power after stress process. In the case of 12% and 15% In, the lower the In composition the larger the noise power.

However, the noise level increased 6 dB and 10 dB for the HFETs with 15% and 12% In compositions in their barriers, respectively. This effect may be caused by the tensile stress from which the barrier layers suffer for lower Indium compositions [110].

Figure 6.2 presents I_D-V_{DS} characteristics before and after stress for V_{GS} = 0V. For higher In composition the I_{Dmax} increases as expected because of the higher electron density accumulated in the GaN channel. For 17% In composition, electron density is mostly due to the spontaneous polarization. For In composition higher than 17%, the piezoelectric effect due to the compressive strain reduces the two-dimensional electron density. While for lower In compositions, piezoelectric effect contributes positively to the increase of the density of electrons, which in turn increases the I_{Dmax}.. For HFETs with lower In compositions (12% and 15%) an appreciable degradation due to the off-state stress is noticed. Even though, for lattice matched HFETs (17% In) the stress effect in LFN spectra variation is not severe, it is notorious if compared with the results from AlGaN/GaN HFET (not shown here) under

similar stress condition. In AlGaN/GaN HFET change in noise power, due to stress is not discernible, even after dozen hour under stress.

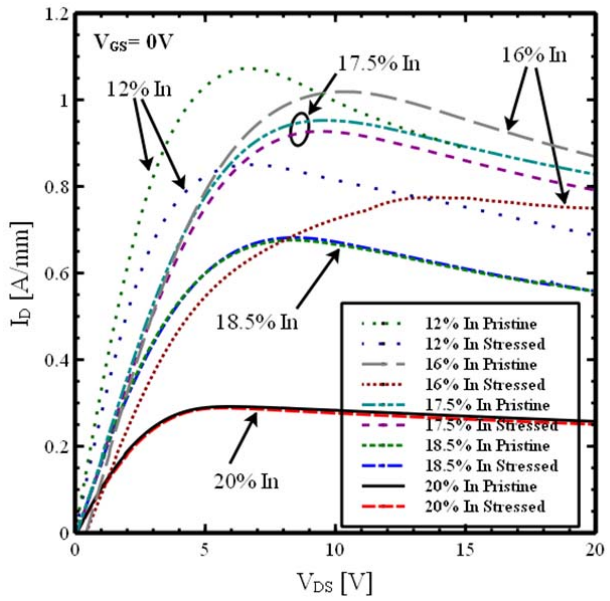


Figure 6.2 ID -VDS characteristics before and after stress for VGS = 0V. A substantial difference between characteristic curves can be observed for HFETs with 12% and 15% In composition in the barriers of the devices.

On the other hand, even for lattice match (InAlN-GaN) In composition, InAlN barrier layer degrade easily. Even after, a couple hour of stress, notable increase in the LFN level is observed. In spite of InAlN/AlN/GaN heterostructures have attractive electrical characteristics from the point of view of the reliability which is of uppermost importance for power devices InAlN barrier layers are not reliable enough yet. Reason may be varied, from the barrier layer growth quality, to hot electron/phonon effects at high carrier densities and /or high electric field effects.

As an introduction to the next step in the developing of HFET for power applications, it is worth to mention that the minimum degradation in InAlN/GaN HFETs as monitored by LFN in Ref. [107] was found at a 2DEG density of ~0.92x10^{13} cm^{-2} (coincident with the 2DEG density at which also f_T is found in this type of heterostructures [111]), while the 2DEG density at V_{GS} = 0V is 2.3 x10^{13} cm^{-2}. That means we need to deplete the channel in more than 50% of the carrier in order to achieve, from the point of view of the reliability, optimal working conditions. The latter is not fruitful from the point of view of a good utilization of the heterostructure. In this regard, a more efficient HFET power handle capabilities need to be found without scarify its reliability.

6.2 Multiple channel HFET – (Al)GaN barrier layers

AlGaN/GaN HFET, even though, has some reliability issues are preferable for power applications. And they are chosen by the industry. 2DEG densities as high as 2x10^{13} cm^{-2} for AlGaN/GaN HFET with barrier layer with 37% Al and 30nm thick were predicted [112]. In practice, however, a carrier density of 1.0 x10^{13} cm^{-2} and 1x10^{3} cm^{2} /V s are routinely attained for barrier layer with 25%Al. Beside the lower polarization induced carrier in the channel compared with InAlN barrier case, HFETs based on AlGaN barrier layers also need to be depleted ≈ 50% in order to accomplish cut-off frequency (see section 4.2). As a result HFET based on AlGaN/GaN heterostructures, as in the case of HFET with InAlN barrier layers, exhibit a reliable working point at low carrier densities. And then, once again, the HFET has a poor power handling. In this case, we come across with the mismatched situation. That is to say, on the one hand we have minimum degradation at low 2DEG. While for high power applications we need higher 2DEG densities at high V_{DS} voltages. And the ideal condition

would be to have minimum degradation (plasmon-hot phonon resonance) at high carrier densities.

Originally proposed by Prof. Arvydas Matulionis and then by Prof. Hadis Morkoç, the idea to shift plasmon-hot phonon resonance point to a higher 2DEG densities via multiple channels heterostructures was established. In this respect, first experimental work consisted in the implementation of coupled channel (CC) heterostructures [71].

6.2.1 Coupled channel HFET

Coupled channel heterostructures like shown in Figure 5.1 b) were first studied and their performance compared with the one from single channel (SC) heterostructure, Figure 5.1 a). In this first approach, we compare electronic transport performance in HFETs based on single channel (SC) GaN/$Al_{0.30}Ga_{0.70}$N/AlN/GaN (2nm/20nm/1nm/3.5µm) and coupled channels (CC) GaN/$Al_{0.28}Ga_{0.72}$N/AlN/GaN/AlN/GaN (2nm/20nm/1nm/4nm/1nm/3.5µm) structures.

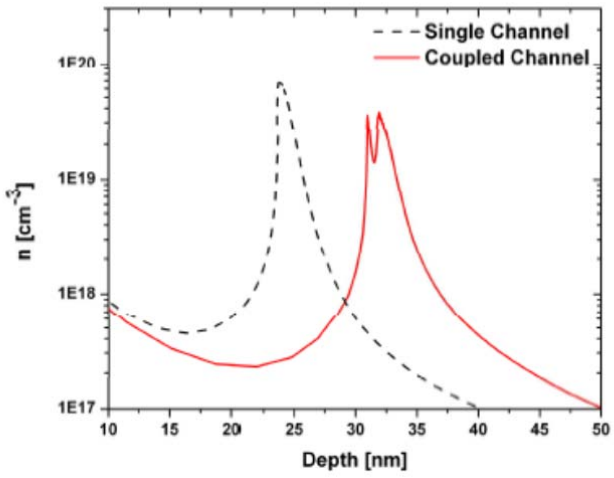


Figure 6.3 Apparent carrier density, n, as a function of the depth along the direction perpendicular to the heterostructure.

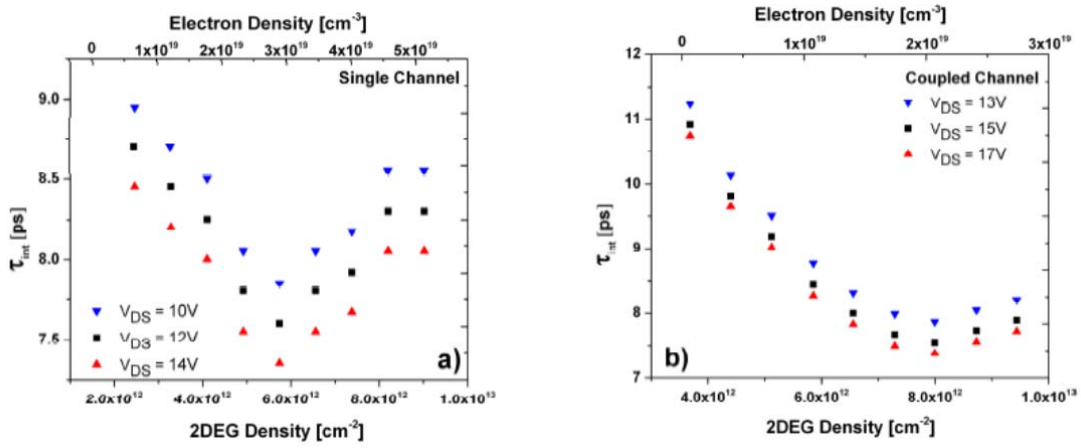


Figure 6.4 Intrinsic transit time vs of 2DEG density under different V_{DS}, for a) SC and b) CC HFETs. Minimum Intrinsic transit time occur at ~5.85×10^{12} cm^{-2} and ~8×10^{12} cm^{-2} for SC and CC, respectively.

Apparent carrier density (n) profiles versus depth, deduced from C-V measurements (not shown here), are shown in Figure 6.3. From the apparent carrier density profiles we can see that the CC heterostructure successfully widens the 2DEG density profile if we compare it with the one from SC channel heterostructure. The two structures have similar current gain cut-off frequencies (11.6 GHz for SC and 14 GHz for CC for ~1μm gate length), however, the maximum drain current, I_{Dmax}, is nearly doubled in the CC HFET (0.64 A mm^{-1} compared to 0.36 Amm^{-1} in SC). HFETs exhibit maximum transconductance (Gm_{max}) at a bias point close to where maximum f_T occurs: V_{GS} =-2.25 V and V_{DS} =12 V and V_{GS} = -2 V and V_{DS}= 15 V for SC and CC HFETs, respectively. Since threshold voltage (V_{th}) is ~ -3.75 V for both SC and CC structures, devices are able to work at high frequencies with a high Gm delivering higher I_D. This is in contrast with device performance reported by others where f_T is attained at V_{GS} closer to V_{th} and therefore with lower I_D/I_{Dmax} ratios and low Gm. From the Hall measurement SC presents an electron mobility (μ) 1.1×10^3 cm^2 V^{-1} s^{-1} and n = 1.2×10^{13} cm^{-2}, while CC performs μ= 1.4×10^3 cm^2V^{-1} s^{-1} and n= 1.3×10^{13} cm^{-2} giving a higher product μ × n, which is consistent with the higher I_{Dmax}.

In order to shed light on the reason of the difference in electron mobility, we conducted Moll's transit time analysis, as explain in section 5.6.2. Results of the mentioned analysis are shown in Figure 6.4. The difference in electron mobility can be explained as follow. The strong hot electron-hot phonon scattering decreases electron velocities [68], [69], [113] and additionally keeps heat trapped in the channel [68], [114] unless the hot phonons can decay into propagating (acoustic) modes and exit the channel [111]. The existence of a minimum in the intrinsic transit time (see Figure 6.4), or a maximum in the electron velocity which in this case corresponds to a maximum in mobility, at a particular 2DEG density can be understood in terms of the hot plasmon-hot phonon resonance. At resonance, hot phonon lifetime is the shortest. The hot phonon lifetime appears to be dependent on the power applied to and the electron density in GaN 2DEGs, and also is understood in terms of the interaction between hot phonons and plasmon [115], [116]. In the regime where the plasmon-hot phonon effect is prominent (at high electric field in the channel), we expect the electron velocity to increase as the hot phonon lifetime decreases. What means that intrinsic transit time decreases as observed in Figure 6.4 a) and less pronounced in Figure 6.4 b).

The hot phonon lifetime is a non-monotonic function of 2DEG and applied power [117], that exhibits a minimum for a 2DEG density near ~ 6.5×10^{12} cm^{-2} [16] or equivalently a bulk electron density of ~ 1×10^{19} cm^{-3}. The SC structures exhibit minimum in the intrinsic transit time at a 2DEG density of ~5.85×10^{12} cm^{-2}, which is close to 6.5×10^{12} cm^{-2}, the optimum [118] 2DEG density (at which hot plasmon-hot phonon resonance occurs). In contrast, minimum in the intrinsic transit time for CC occurs at a 2DEG density of ~8×10^{12} cm^{-2} at which the mobility is even higher compared with the one for SC structure. This happens, because the hot electrons in CC are spread over a larger volume, they have a lower (full width at half maximum (FWHM)) bulk electron density ~2×10^{19} cm^{-3} compared with ~3×10^{19} cm^{-3} of SC (see Figure 6.3). And as pointed out in Ref. [7], the plasma frequency decreases and the

plasmon-hot phonon resonance is observed at higher 2DEG densities. Based on the higher mobility and lower FWHM bulk electron density obtained for CC, it is believed that a 2DEG density ~8×10^{12} cm^{-2} is closer to the 2DEG density at which plasmon-hot phonon resonance happens in CC structure.

As the saturation drain current, I_{Dsat}, is attained at electric fields (~40KV/cm) lower than the critical electric field, E_{cr}, (~150KV/cm for GaN) the higher f_T in CC HFETs can be attributed, mainly, to a higher μ, which is in agreement with the Hall measurements. A higher μ in CC HFET is attributed to a shorter hot phonon lifetime.

Even though, CC heterostructures reach resonance conditions at higher carrier densities the channel need to be depleted, as a $V_{GS} < 0V$ need to be applied to attain resonance conditions. A better situation could be if we tune the 2DEG density profile in order to achieve the resonance at as closer to $V_{GS} = 0V$. This is extra beneficial. First, an efficient use of the heterostructure is achieved. Second, because the gate is at 0V the barrier layer is subject to lower electric fields, reducing leakage current either both because of the surface states or because of the barrier layer.

6.2.2 Dual channel HFET

In an attempt to shift resonance bias point even closer to $V_{GS}=0V$, another series of devices were fabricated on fresh grown similar heterostructures and additionally a new heterostructure design was implemented, dual channel (DC) heterostructure, see Figure 5.1 b). The idea behind different heterostructure designs is, observe how the heterostructures widen the 2DEG density profile and evaluate possible shift in plasmon-hot phonon resonance.

Apparent carrier density profiles for the new series of samples are shown in Figure 6.5 and their characteristics are displayed in Table 6.1. The following discussion spins around the HFET universal relationship (the concept of "universal relationship" was first introduced by Prof. Arvydas Matulionis) between the initial electron density and the optimal gate bias toward higher carrier densities.

Table 6.1. 2DEG density and apparent carrier density profile parameters.

Sample	V_{GS} at f_T	2DEG	2DEG width at $10^{19}cm^{-3}$	2DEG Δ-height from x 10^{19} cm^{-3}
	V	x 10^{13} cm^{-2}	nm	nm
SC	-1	1.23	2.15	5
CC1	-2.5	1.55	3.1	3.6
CC2	-1.25	1.3	3.1	3
DC1	-1.5	1.3	2.3	5.3
DC2	-3	1.5	2.95	15.7

HFET based on multiple channels heterostructures are expected to shift the HFET universal relation toward higher carrier densities. Therefore, HFET higher power operation points at optimum electron densities. And best HFET performance (higher cut-off frequency, low degradation, and phase noise level), because plasmon-assisted ultrafast decay of hot phonons. Optimum electron density in the active part of the channel, tuned by the optimal gate bias, is $\approx 1x10^{13}$ cm^{-2} for standard AlGaN/GaN HFETs. As shown Figure 6.6, multiple AlGaN/GaN channel structures, when widen the 2DEG density profile (see Figure 6.5), can shift the HFET universal relation curve toward higher 2DEG densities, from $\sim 1\times10^{13}$ cm^{-2} for standard HFET structure to $\sim 1.15\times10^{13}$ cm^{-2} for multiple channel HFET structures. Among proposed multiple

channel structures, coupled channel and dual channel, coupled channel heterostructures seem to be more suited to widen the 2DEG density profile. Increasing the optimal electron sheet density without the deleterious effect caused by inefficient hot phonon decay observed in HFET standard design.

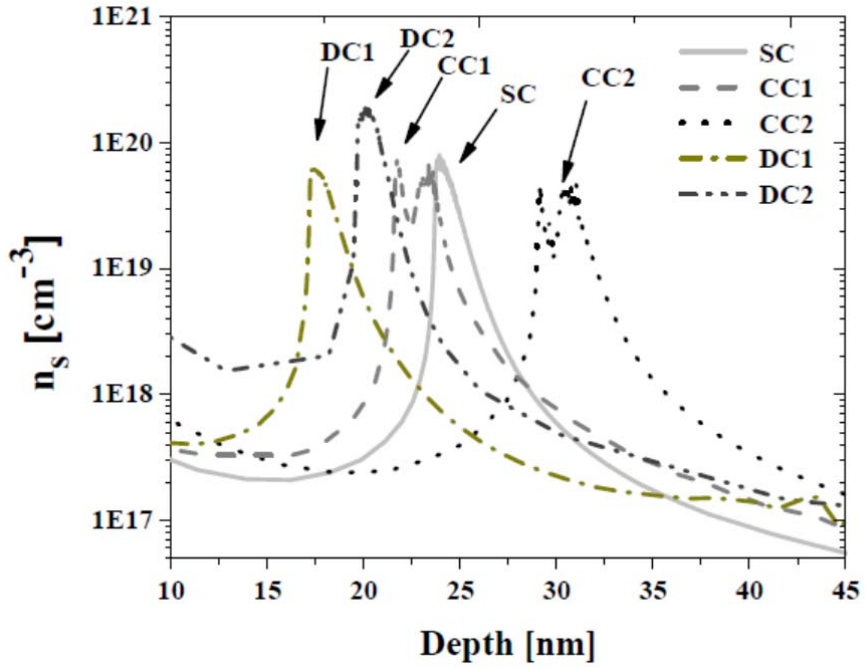


Figure 6.5 Apparent carrier density, n_s, as a function of the depth along the direction perpendicular to the heterostructure.

In the regime where the plasmon-hot phonon effect is prominent, (at high electric field in the channel), electron velocity increases as plasmon-assisted ultrafast decay of hot phonons is more pronounced. This means a decreasing carrier intrinsic transit time. Hence, HFET bias conditions for f_T are the same at which plasmon-hot phonon resonance occurs. Notice here we are interesting in the conditions at which f_T is achieved, in particular V_{GS}, and not in the absolute value of f_T which depends on scaling down of the transistor and on parasitic elements. On the other hand, optimal gate bias depends, mainly, on the initial 2DEG density

[119]. In Figure 6.7 dots on N_s curves (integrated apparent carrier density curves normalized with respect to initial electron density) indicate the value of V_{GS} at which f_T is achieved.

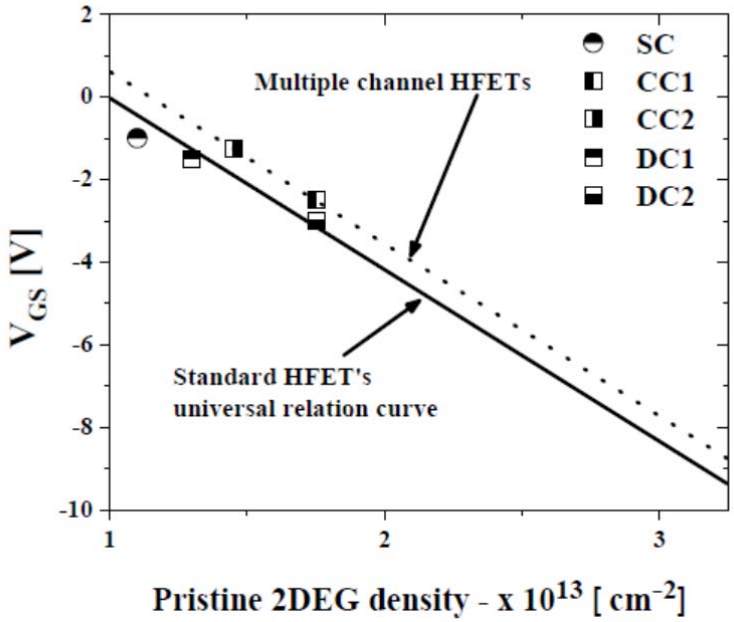


Figure 6.6 Universal optimum gate voltage - pristine 2DEG density relationship for standards HFETs (—) and for coupled channels (---). SC stands for single channel, DC dual channel, and CC for coupled channel.

The first observation we should make is the following. When the multichannel structure fails in broadening the 2DEG profile, the optimal gate bias may lead to a lower 2DEG density than the one for a SC. This is the case for the dual channel heterostructures DC1 and DC2, in which both exhibit higher 2DEG Δ-height (see Table 6.1). That is, a great contribution to the 2DEG density is over 10^{19} cm^{-3} level (see Figure 6.5). On the other hand, CC1 and CC2 widen successfully the 2DEG profile demonstrating optimal gate bias at higher N_S. In the latter case, 2DEG width and 2DEG Δ-height for both samples are comparable. However, N_S is a little be lower for CC1 due to the higher initial 2DEG of CC1 compared with the of CC2 (see Table 6.1).

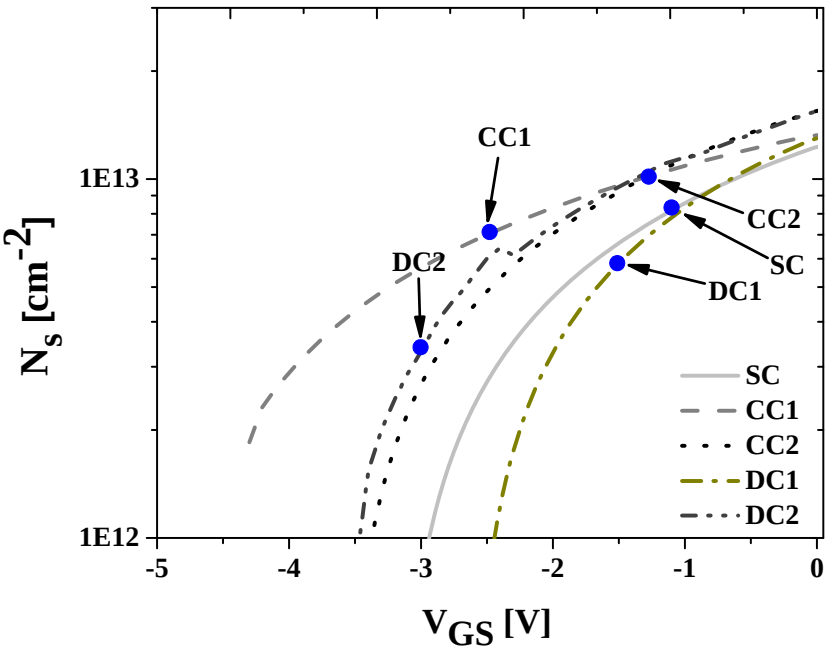


Figure 6.7 Normalized integrated apparent carrier density (Ns) vs.V_{GS}. Dots indicate HFET working conditions at which cut-off frequency occurs.

For comparable 2DEG densities, the larger the 2DEG Δ-height the more negative (closer to pinch-off) is the optimal gate bias. The mentioned can be observed between CC1 and DC2 and between CC2 and DC1. Whose 2DEG density and 2DEG width are comparable. Exception is the sample DC1 for which 2DEG is smaller but it is compensated by a larger 2DEG Δ-height. In other words, in order to attain optimal gate bias closer to $V_{GS} = 0V$, what is important, ultimately, is that the area of 2DEG profile above 10^{19} cm^{-3} level needs to be as small as possible. Therefore, the channel needs to be depleted less to achieve resonance conditions. It is the case of SC when compared with DC1 and DC2 and the case of CC2 when compared with CC1. In this last point a more formal analysis of the 2DEG profile should be done. The analysis should take into account the effect of V_{DS} (in fact the applied electric field) bias in reshaping of 2DEG density profile. Here, for the sake of simplicity, we assume the profile does not change much under V_{DS} bias in first approximation. Therefore, 2DEG density

profiles obtained from C-V measurements are valid under V_{DS} bias. The universal optimum gate voltage - pristine 2DEG density relationship for standard heterostructure (SC) is given by the following $V_g = \frac{(n_g - n_s) \times e}{C_g}$, where n_g, is the active 2DEG density in the part of the channel controlled by the gate bias, V_g, C_g is the effective gate capacitance, n_s is the initial 2DEG density, and e is the electron charge. Figure 6.6 displays V_g for standard structures (solid line) with $n_g = 1 \times 10^{13}$ cm^{-2} and $C_g = 3.8 \times 10^{-7}$ F cm^{-2}. By using the expression for V_g and n_g as fitting parameter to fit points CC1 and CC2 taken $C_g = 3.8 \times 10^{-7}$ F cm^{-2}, we get $n_g = 1.15 \times 10^{13}$ cm^{-2}. It means optimal gate bias for CC structures occurs at higher active 2DEG density (1.15×10^{13} cm^{-2}) compared with that of SC (1×10^{13} cm^{-2}). Namely, CC structures shift optimal gate bias closer to V_{GS}=0 V for the same 2DEG density. That means, CC structures possess 2DEG density profile for which more carriers take part of the plasmon-hot phonon resonance. Clearly, optimal gate bias points for DC1 and DC2 lay on the standard HFET's universal relation curve. This is consistent with the fact that these structures do not widen the 2DEG profile substantially (DC1) or its profile concentrates a good deal of carrier above 10^{19} cm^{-3} level (DC2). On the contrary, CC structures separate from standard universal relation curve to higher 2DEG at constant V_{GS} or similarly, lower absolute values of V_{GS} at constant 2DEG. The latter is exemplified by comparing DC1 and CC2 in the case of constant V_{GS} and comparing DC2 and CC1 in the case of constant 2DEG density (see Figure 6.6). In both cases CC structures successfully shift the optimal gate bias point to higher active 2DEG densities. The most interesting of the cases is when the CC structure a constant V_{GS} shifts active 2DEG density to higher levels. And therefore, higher power working conditions. Additionally, a more efficient use of the structure is attained. The key point is that CC structures widen the 2DEG profile, reshaping it in such a way the channel needs to be depleted less than in the case of DC ones to achieve plasmon-hot phonon resonance. Of course, It is desirable to reach

resonance conditions at V_{GS} = 0V, case in which HFET would delivers maximum power without the deleterious effect caused by inefficient hot-phonon decay observed in HFET standard design and as an extra benefit lower gate leakage currents are expected.

6.3 Estimation of heat dissipation

From the point of view of energy efficiency and heat removal from the heterostructure it is instructive to do an estimation of the hot electron given energy to the lattice. In the following analysis we assume that the hot phonon energy is 100% converted into acoustic phonon (LA) energy. Hence, LO phonon excess energy is transported to the heat sink. In this section our approach to calculate hot phonon dissipated power is a slightly different to the one presented in section 3.9. While the Eq. 1(1)111 is theoretically correct the one presented here is more practical and instructive one. Assuming hot phonon life time constant, the hot phonon dissipated power is proportional to the excess occupancy of the hot phonon modes. Such proportionality is described by $P_d = \frac{\hbar\omega_{\mathrm{LO}}}{\tau^*_{\mathrm{LO}}}\ (N^*_{\mathrm{LO}} - N_0)$ where τ^*_{LO} its effective lifetime, N^*_{LO} is the equivalent occupancy of the LO phonon states. In the case of dominant phonon, here because of the electron –LO-phonon interaction and strong phonon effect, a direct relationship between noise temperature, T_n, (that can be experimentally measured) and hot phonon temperature can be found. Under the condition of dominant electron-LO-phonon scattering T_n is just a few per cent higher than the electron temperature, T_e [120]–[122]. In a 2DEG hot electron and hot phonon are under intense interaction. Then at a high density of electrons, the hot phonon temperature, T_{LO}, is just few per cent lower than the hot phonon temperature [113], [120]. As a result, in GaN based channel with high 2DEG density we have $T_n \approx T_e \approx T_{LO}$. Thus, N^*_{LO}, can be estimated, after Bose-Einstein distribution with $T_{LO} \approx T_e$ assumed, as

$$P_{\mathrm{d}} \approx \frac{\hbar\omega_{\mathrm{LO}}}{\tau^{*}_{\mathrm{LO}}}\left(\frac{1}{e^{\frac{\hbar\omega_{\mathrm{LO}}}{k_B T_{\mathrm{n}}}}-1}-\frac{1}{e^{\frac{\hbar\omega_{\mathrm{LO}}}{k_B T_{\mathrm{L}}}}-1}\right) \tag{3}$$

where $\hbar\omega_{\mathrm{LO}}$ is the energy of the hot electrons emitted phonon, T_n in the noise temperature, T_L is the ambient temperature, and k_B, is the Boltzmann constant.

Correctness of Eq. (3) was checked by Monte Carlo simulation [123], [124]. Our estimation of power dissipation is focus in dual channel ($In_{0.82}Al_{18}N/AlN/Al_{0.1}Ga_{0.9}N$ /GaN) which is contrasted with its single channel counterpart ($In_{0.82}Al_{18}N/AlN$ /GaN). From experimental data displayed in Figure 6.8 a) we obtain the hot electron temperature for a fix resonance 2DEG density, here we chose $\approx 1.15 \times 10^{13}\mathrm{cm}^{-2}$. We found hot electron temperature of $\approx 350\mathrm{K}$ and $\approx 2300\mathrm{K}$ for dual a single channel, respectively. Then we these value of temperatures we enter in Figure 6.8 b) as indicated by arrows. Doing so, we get for both cases constant hot phonon lifetime of $\approx 60\mathrm{fs}$. Then inserting phonon lifetime and temperature in the Eq. (3) we have power dissipation per electron of $410\mathrm{nW/e}$ and 3.8nW/e for single and dual channel respectively. It means that the single channel dissipates ≈ 108 times more power per electron than the dual channel does before to achieve optimal work conditions. Two order of magnitude in the dissipate power is a remarkable difference.

To contrast latter result, we found phonon dissipated power from Figure 6.8 c) in which dissipated power and excess noise temperature are experimentally and directly correlated.

A dissipated power of $100\mathrm{nW/e}$ and $0.25\mathrm{nW/e}$ are found for dual and single channel with a power ratio of 400. Once again dissipated power in single channel is two order of magnitude higher compared with dual channel. The difference in absolute values might be due to experimental, extrapolation and calculation errors. In concrete, we have that electron dissipated power is two order of magnitude higher in a single channel than in dual channel for a 2DEG density of $\approx 1.15 \times 10^{13}\mathrm{cm}^{-2}$. A reduction of hot electron dissipated power is desirable especially at high current level when a large total amount of heat is expected to be

dissipated by the device compromising not only electron transport performance but also device reliability.

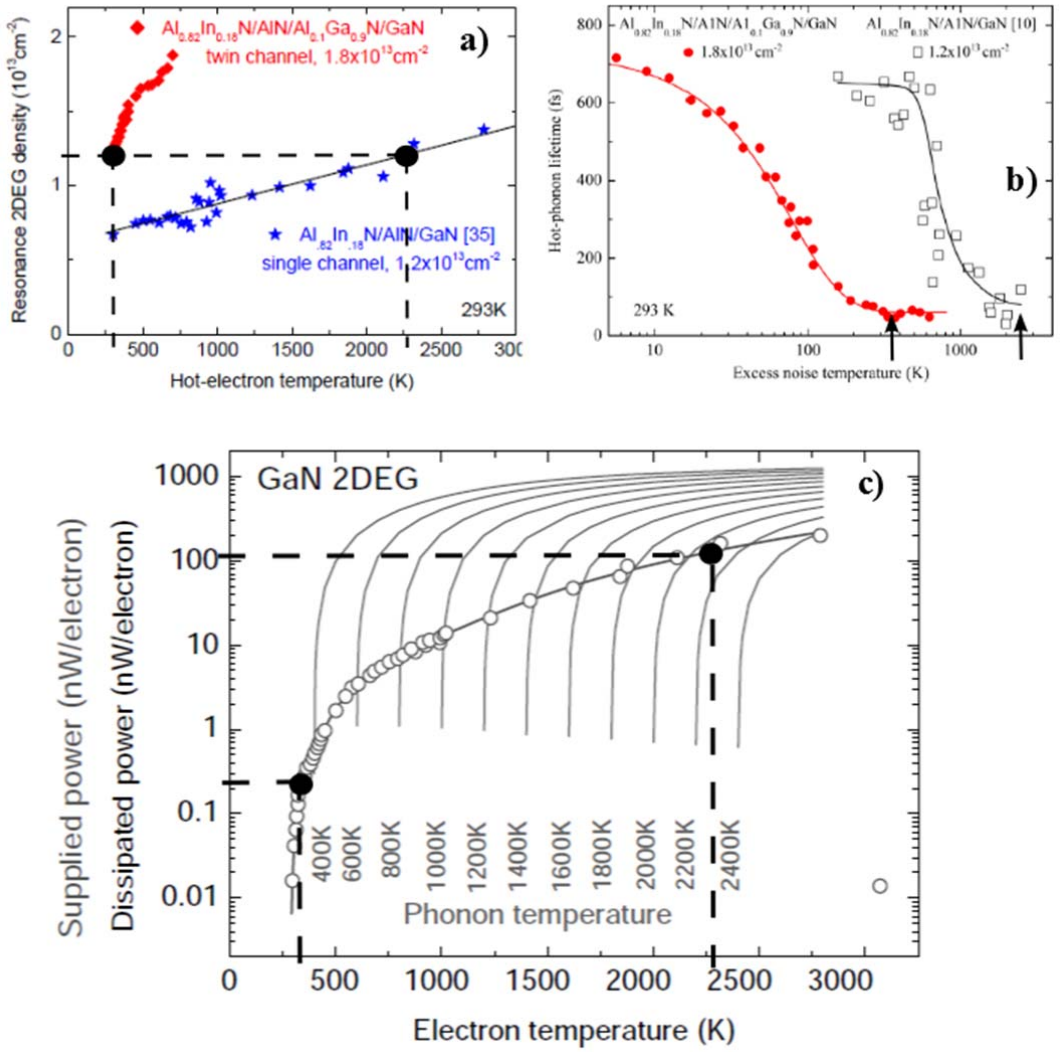


Figure 6.8 2DEG density at resonance conditions in a dual channel heterostructure. a) dependence of resonance 2DEG on hot-electron temperature: single channel (start), and dual channel (diamonds) [66]. b) hot phonon lifetime as a function of the excess noise temperature in the single channel (squares) and in the dual channel (circles) [7]. In a) and b) curves guide the eye. c) Solid lines indicate power dissipated by hot phonons at a number of phonon temperature. Symbols and curve display experimental electron temperature as a function of supplied power. Intersection of the curves gives hot phonon temperature for a given hot electron temperature [119].

Chapter 7. Conclusions

The concept of hot electron, hot phonon, plasmon and the interaction among them was presented. Plasmon-hot phonon resonance model under which phonon fast decay is observed was introduced. A logical path for the understanding of electron power dissipation by emission of hot phonon under high electric field was delineated.

The fact that the resonance depend on the carrier density profile open the door to imaginative heterostructure designs such as the ones show here, dual- and coupled-channel heterostructures. As discussed in the section dealing with heterostructure simulations 5.2, dual channel is attractive design from the point of view of 2DEG density profile widening and coupled channel design from the point of view of transport properties as assessed from experimental results. However, under inadequate design parameters i.e. layer thicknesses and compositions, either both dual and channel heterostructures may behave as a single channel heterostructure from the point of view of the 2DEG profile widening.

Capacitance –voltage profile confirm 2DEG density widening in either both dual and coupled channel heterostructures. However, in the case of our dual channel heterostructures widening is not very notorious, fact that is reflected in the bias point for the resonance condition.

Single channel heterostructure concentrate carrier profile shifting resonance point to lower carrier concentrations, delivering higher power under non optimum working conditions therefore under high electron power dissipation conditions. The 2DEG in dual channel heterostructure is subject to alloy scattering which is not desirable, especially, at low electric fields. At high electric field it was observed that carrier experience real transfer space (RTS) effect which in principle might look like something negative. Nevertheless, at high electric field the 2DEG profile widens toward the GaN part of the channel where better transport conditions are expected. Nonetheless, we lose channel confinement in consequence control of

the channel. Also from simulations and from experimental data (in the case of DC) it is observed a single channel performance like if the layer thickness and compositions are not the adequate and all potential advantages of the multiple channel heterostructures are lost. On the other hand, in coupled channel heterostructures carrier confinement is best but the carrier profile is not as uniform as it is in dual channels. In reality this structure exhibit two channel in parallel in which carrier distribution should be balanced in order to optimize the widening of the 2DEG density profile. It was demonstrated that in couple channel resonance condition can be effectively shift toward higher resonance 2DEG.

Dual and coupled channels successfully widen the 2DEG density profile. However, because of a reduction of the carrier confinement the control of the channel is moderate in the case of dual channel heterostructures. On the other hand, in coupled channel heterostructures carrier confinement is better providing a better control of the channel. Furthermore, unlike in a dual channel heterostructure, alloy scattering does not affect carrier transport properties, resulting in a higher cut-off frequency. It was found that coupled channel heterostructure successfully reaches resonance conditions at a 2DEG density 23% higher than that in single channel heterostructure.

Calculation based on conventional thermal model show that separation layer (AlN) and AlGaN layer (channel) reduce thermal conduction for top channel in just 2%. Therefore, we can say that in all cases the thermal conductance of the heterostructures is comparable and it is limited mainly by the GaN thermal conductance of the buffer layer and not by the multichannel heterostructure design. Simple calculation based on the assumption that the hot electron dissipated power is fully converted into hot phonon power and the later converted only into acoustic phonon power (we assume that the TO mode shared energy is negligible), the power dissipated by an electron in a single channel heterostructure ($\sim 400 \mathrm{nW/e}$) is 100

times higher than the power dissipated per electron in a dual channel heterostructure ($\sim 4\mathrm{nW/e}$) for the same 2DEG density $\sim 1.15 \times 10^{13}\mathrm{cm}^{-2}$. Similar calculations for a carrier density of $\sim 1.4 \times 10^{13}\mathrm{cm}^{-2}$ result in a ratio of 50. Promising ratios still need to be proven in HFET where the electric field in the channel under working condition is not uniform and heat up the 2DEG changing the 2DEG density profile.

Chapter 8. Future work

In order to evaluate if such mentioned electron dissipated power ratio keep in HFET at high power working conditions, the channel temperature need to be measured, task which is not trivial. So, methods to estimate the channel temperature need to be applied. Such as methods are based on many considerations and many measurements need to be taken before to arrive to some useful result. Instead, a convenient qualitative approach as the following can be implemented.

The main idea is to evaluate the temperature ramping of a well-defined and isolated piece of chip (see Figure 8.2). It could a block of our fabrication process. A block consists of 26 HFETs distributed in an array of 4 columns by 7 rows with a total area of 3×3 mm^2. All devices of the block should be connected in order to avoid excessive temperature gradient. By applying power the temperature of the piece of chip will increase reaching a steady state.

Figure 8.1 HFET design block 3×3 mm^2.

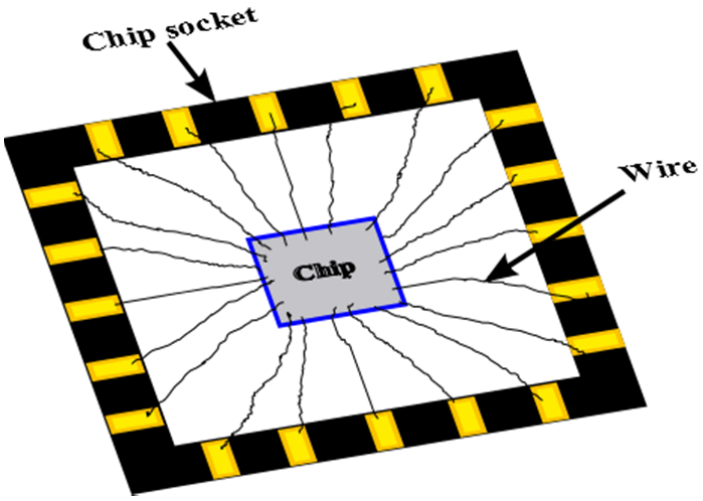


Figure 8.2 Chip bonded to a socket.Wires suspend the chip. With this arrangenemt heat transfer from the chip to the surroundings is minimized.

It is this temperature at steady state we should keep track of. Assuming, dissipated heat due to the ohmic contacts is the same in single, dual, and couple channel HFETs the difference in final temperatures for the same drain current level should be owing to the hot electro dissipated power. If we set the drain current level at the one at which plasmon-hot phonon resonance occurs in dual- or coupled channel, the temperature of the single channel-chip should be higher than the one for dual- or coupled channel chip.

Two feasible methods to measure the chip temperature are: thermocouple and infrared gun. The thermocouple compared with the piece of chip should smaller in size. And it should be mechanically attached to the chip. On the other hand, infrared gun need to be well aligned with the chip and have enough resolution to detect small variations in temperature.

Other option is to evaluate the temperature on HFET capable to handle higher power levels for instance Finger HFET design such as the one shown in Figure 8.3 or versions with 10 or more fingers. Such design might dissipate enough heat to detect the temperature variations

and under real working condition the effect of hot phonon dissipated power could be evaluated by measuring the temperature increment of the isolated piece of substrate (chip).

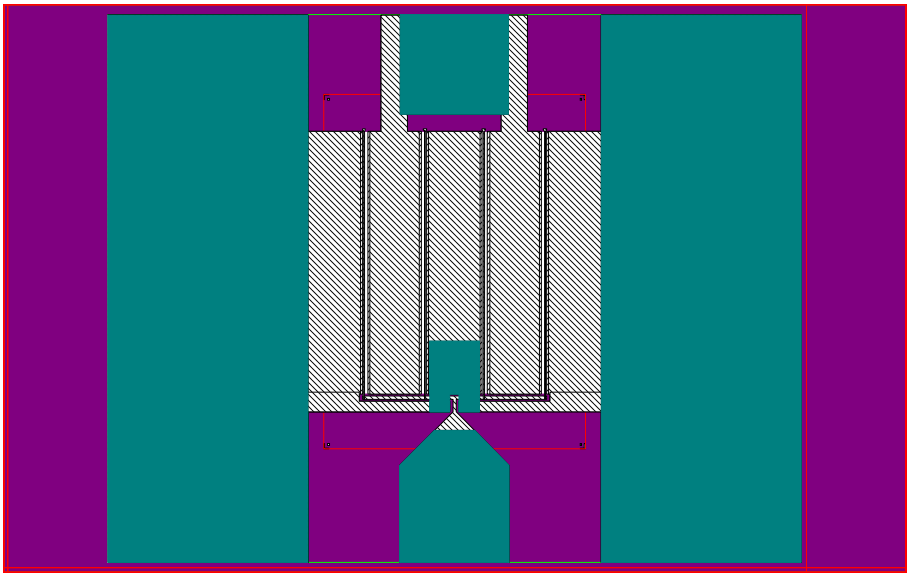


Figure 8.3 Multi-Finger HFET design for power application. The design consists of 4 fingers.

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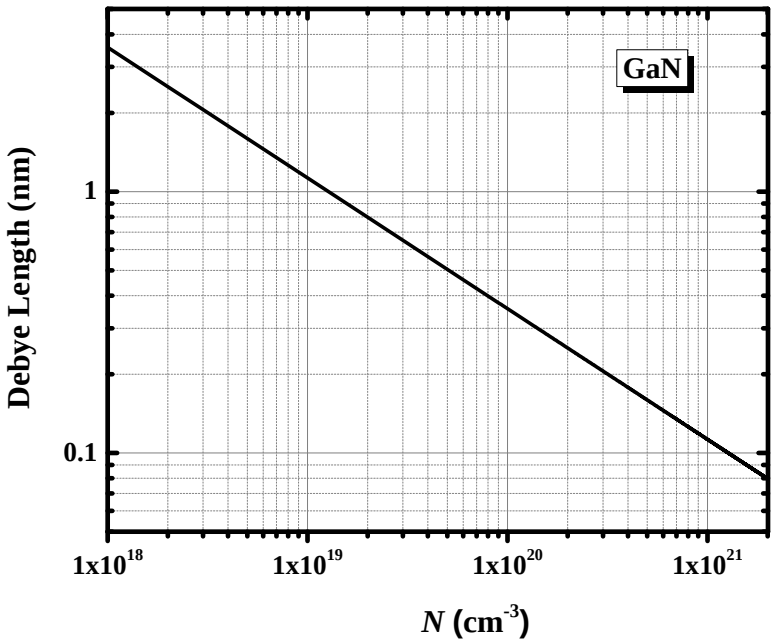
APPENDIX A

Debye Length

Debye length, L_D, is a characteristic length for semiconductors and is given by

$$L_D = \sqrt{\frac{\varepsilon_r \varepsilon_o k\mathrm{T}}{q^2 N}},$$

where ε_o is the vacuum dielectric constant, ε_r the relative dielectric constant of the semiconductor, k the Boltzmann constant, T the absolute temperature, q , the elemental electric charge and $N$the charge density. Debye length gives an idea of the limit of the potential change in response to an abrupt change in the doping profile. Figure A1 exhibits the Debye length characteristic for GaN as a function of carrier density, *N*. For carrier densities ≈ $1E^{20}$ cm^{-3}, what is expected for the peak of a 2DEG profile in a GaN-based HFET, Debye length is in the order of few Åmstrongs.



A1 Debye length in GaN at room temperature as a function of the carrier (electrons) density, *N*.

APPENDIX B

Photolithography

Photolithography Process for MESA etching

SPR3012

1. Cleaning — Acetone/methanol (under ultrasound)/ DI water
2. Spin Coating — 1000rpm/3 sec, 3000rpm/30sec, 6000rpm/3 sec
3. Softbake — 80 sec @ 100^{o}C
4. Exposure — 2.38min @ 6.5 W/cm^2 (90mJ/cm^2 / i-Line)
5. Postbake — 80 sec @ 110^{o}C
6. Development — 60 sec - MF CD-26 @ RT, DI water rinse/1min, N_2 blow dry

SPR955 0.9µm

1. Cleaning — Acetone/methanol (under ultrasound)/ DI water
2. Spin Coating — 1000rpm/3 sec, 3000rpm/30sec, 6000rpm/3 sec
3. Softbake — 140 sec @ 100^{o}C
4. Exposure — 2.38min @ 6.5 W/cm^2 (165mJ/cm^2 / i-Line)
5. Postbake — 80 sec @ 110^{o}C
6. Development — 60 sec - MF CD-26 @ RT, DI water rinse/1min, N_2 blow dry

Photolithography Process for Metal contact deposition

SPR955 0.9µm

1. Cleaning — Acetone/methanol (under ultrasound)/ DI water
2. Spin Coating — 1000rpm/3 sec, 3000rpm/90sec, 6000rpm/3 sec
3. Soak in Developer — 60 sec - MF CD-26 @ RT, DI rinse 1min, N_2 blow dry
4. Exposure — 2.38min - 6.5 W/cm^2 (to remove sample edges)
5. Softbake — 140 sec @ 70^{o}C
6. Exposure — 2.38min - 6.5 W/cm^2 (165mJ/cm^2 / i-Line)
7. Postbake — 80 sec @ 110^{o}C
8. Development — 11 sec - MF CD-26 @ RT, DI water rinse/1min, N_2 blow dry

APPENDIX C

Atlas – SILVACO - Setting to simulate a single channel GaN-HFET

```
#=============================================================================#
#     GaN HFET simulation
#
#      AlN/GaN/AlGaN/GaN - Single Channel HFET
#
#     By Romualdo Alejandro Ferreyra    January 2014
#
#=============================================================================#
#         Start
#_____________________________
go atlas
#         Constants definition
#_____________________________
set GateLength = 90
#         Structute Specification
#=============================================================================#
# mesh definition
#_____________________
mesh width=$GateLength
# x plane meshing
x.m l=0.0       s=0.25
x.m l=0.5       s=0.125
x.m l=1.5       s=0.125
x.m l=2.5       s=0.125
x.m l=4.5       s=0.25
x.m l=5         s=0.25
# y plane meshing
y.m l=0         s=0.249
y.m l=0.498     s=0.0001
y.m l=0.499     s=0.0001
y.m l=0.5       s=0.0001
y.m l=0.520     s=0.00001
y.m l=0.521     s=0.00002
y.m l=0.6       s=0.005
y.m l=0.7       s=0.1
y.m l=1.0       s=0.2
y.m l=2.0       s=0.5
y.m l=3.5       s=0.05
y.m l=3.850     s=1
```

```
#       Regions definition
#_____________________________
region num=1 x.min=0 x.max=5 y.min=0.0  y.max=0.498          mat=  nitride insulator
region num=2 x.min=0 x.max=5 y.min=0.498 y.max=0.499        mat= GaN
polar calc.strain polar.scale=1
region num=3 x.min=0 x.max=5 y.min=0.499 y.max=0.5          mat= GaN
polar calc.strain polar.scale=1
region num=4 x.min=0 x.max=5 y.min=0.5   y.max=0.520        mat= AlGaN x.comp=0.3
polar calc.strain polar.scale=1
region num=5 x.min=0 x.max=5 y.min=0.520 y.max=0.521        mat= AlN
polar calc.strain polar.scale=1
region num=6 x.min=0 x.max=5 y.min=0.521 y.max=3.5          mat= GaN
polar calc.strain polar.scale=1
region num=7 x.min=0 x.max=5 y.min=3.5   y.max=3.85         mat= AlN  substrate
polar calc.strain polar.scale=1
#       Electrodes definition
#_____________________________
elec num=1 name=source x.min=0   x.max=0.5 y.min=0.498  y.max=0.6
elec num=2 name=drain   x.min=4.5 x.max=5   y.min=0.498  y.max=0.6
elec num=3 name=gate    x.min=1.5 x.max=2.5 y.min=0       y.max=0.498
elec num=4 substrate
#       Material Models Specifications
#=============================================================================#
#       Models definition
#_____________________________
model n.schrodinger p.schrodinger fixed.fermi
#       Contact definitions
#_____________________________
contact name=gate     work=5
contact name=source work=3.93
contact name=drain    work=3.93
#       Numerical Method Selection
#=============================================================================#
#       Method definition
#_____________________________
method carriers=0
#       Solution Specification
#=============================================================================#
#       Outputs
#_____________________________
output con.band val.band charge  polar.charge band.par
#       Solve
#_____________________________
solve init
save outf=GaN_HFET_SC.str
#       Stop
#_____________________________
quit
```

Vita

Romualdo Alejandro Ferreyra was born on May 10, 1977, in Ciudad Autonoma de Buenos Aires, Argentina. He graduated from Escuela Provincial de Educación Técnica N°1, Santa Rosa, La Pampa, Argentina, 1995. He received his Engineer degree in Electronics from Universidad Nacional del Sur, Bahía Blanca, Argentina in 2005. A Diplom-Ingenieur in Electrical Engineering from RWTH AACHEN, Aachen, NRW, Germany. And a Doctorate in Engineering from Universidad Nacional del Sur in 2010.