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DC, MICROWAVE, AND NOISE PROPERTIES OF GAN BASED HETEROJUNCTION FIELD EFFECT TRANSISTORS AND THEIR RELIABILITY ISSUES

Congyong Zhu
Virginia Commonwealth University

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RELIABILITY ISSUES

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by

CONGYONG ZHU
Master of Philosophy, The University of Hong Kong, 2008
Bachelor of Science, Wuhan University, 2006

Director: MORKOÇ, HADIS
FOUNDER PROFESSOR OF ELECTRICAL AND COMPUTER ENGINEERING

Committee in charge

PROF. MORKOÇ, HADIS

PROF. ATKINSON, GARY

PROF. BASKI, ALISON

PROF. ÖZGÜR, ÜMIT

PROF. RESHCHIKOV, MICHAEL

Virginia Commonwealth University
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FIGURE 58 PHASE NOISE RESULTS OF $IN_{0.185}AL_{0.815}N$/GAN HFETS BEFORE AND AFTER 30 HOURS SEMI-ON STRESS AT V_{GS}=-5*V* AND V_{DS} =20*V* AT DIFFERENT EXTERNAL BASE PLATE TEMPERATURES: (A) ROOM TEMPERATURE; (B) 100 ^{O}C; (C) 150 ^{O}C. THE RESULTS WERE OBTAINED AT V_{GS} =0V AND V_{DS}=6*V*. 95

Abstract

DC, MICROWAVE, AND NOISE PROPERTIES OF GAN BASED HETEROJUNCTION FIELD EFFECT TRANSISTORS AND THEIR RELIABILITY ISSUES

By

Congyong ZHU

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Major Director: MORKOÇ, HADIS
Founder Professor Department of Electrical and Computer Engineering

AlGaN/GaN and InAlN/GaN-based heterojunction field effect transistors (HFETs) have demonstrated great high power and high frequency performance. Although AlGaN/GaN HFETs are commercially available, there still remain issues regarding long-term reliability, particularly degradation and ultimately device failure due to the gate-drain region where the electric field peaks. One of the proposed degradation mechanisms is the inverse-piezoelectric effect that results from the vertical electric field and increases the tensile strain. Other proposed mechanisms include hot-electron-induced trap generation, impurity

diffusion, surface oxidation, and hot-electron/phonon effects. To investigate the degradation mechanism and its impact on DC, microwave, and noise performance, comprehensive stress experiments were conducted in both un-passivated and passivated AlGaN/GaN HFETs. It was found that degradation of AlGaN/GaN HFETs under reverse-gate-bias stress is dominated by inverse-piezoelectric effect and/or hot-electron injection due to gate leakage. Degradation under on-state-high-field stress is dominated by hot-electron/phonon effects, especially at high drain bias. Both effects are induced by the high electric field present during stress, where the inverse-piezoelectric effect only relates to the vertical electric field and the hot-electron effect relates to the total electric field.

InAlN/GaN-based HFETs are expected to have even better performance as power amplifiers due to the large 2DEG density at the InAlN/GaN interface and better lattice-matching. Electrical stress experiments were therefore conducted on InAlN/GaN HFETs with indium compositions ranging from 15.7% to 20.0%. Devices with indium composition of 18.5% were found to give the best compromise between reliability and device performance. For indium compositions of 15.7% and 17.5%, the HFET devices degraded very fast (25 h) under on-state-high-field stress, while the HFET devices with 20.0% indium composition showed very small drain. It was also demonstrated that hot-electron/phonon effects are the major degradation mechanism for InAlN/GaN HFETs due to a large 2DEG density under on-state operations, whereas the inverse-piezoelectric effect is very small due to the small strain for the near lattice-matched InAlN barrier. Compared

to lattice-matched InAlN/GaN HFETs, AlGaN/GaN HFETs have much larger strain in the barrier and about half of the drain current level; however, the hot electron/hot phonon effects are still important, especially at high drain bias.

CHAPTER 1 Introduction

GaN-based heterojunction field effect transistors (HFETs) are receiving a great deal of attention owing to their high performance in high-frequency/high-power applications[1]. Both AlGaN/GaN and InAlN/GaN HFETs show supreme device performance. AlGaN/GaN based HFETs on SiC substrate with 60 nm gate lengths have achieved maximum oscillation frequency (f_{max}) of 300 GHz[2], which followed by the implementation of several techniques to improve the device performance, such as low-damage gate-recess technology, scaled device geometry, and recessed source/drain ohmic contacts to simultaneously enable minimum short-channel effects and low parasitic resistances. Also an on resistance R_{ON} = 1.1~1.2 $\Omega \cdot mm$ and drain current of ~0.9A/mm at $V_{GS} = 0V$ were achieved for the devices with the same gate length of 60 nm. The first remarkable $In_{0.14}Al_{0.86}N$/GaN HFETs with high current gain cutoff frequency (f_T) of 102 GHz was achieved on high resistivity (111) Si substrate for 0.1-μm gate length devices and 9 nm barrier thickness[3]. A high drain current of ~1.3 A/mm was demonstrated at V_{GS}=0V with an extrinsic transconductance of 330 mS/mm. Continuous-wave power measurements in class-A operation at 10 GHz with V_{DS}=15V demonstrated a 19-dB linear gain, a maximum output power density of 2.5 W/mm with an ~23% power-added efficiency (PAE), and a 9-dB large-signal gain. The use of lower indium composition further increased the drain current to ~2.0 A/mm for 10nm thick $In_{0.12}Al_{0.88}N$/GaN HFETs. By reducing the gate length further down to 55 nm, an f_T of 205 GHz and drain current of 2.3

A/mm at V_{GS}=0V were achieved for 10 nm thick $In_{0.14}Al_{0.86}N$ barrier. Active scaling of the gate length to ~30 nm for 4.5 nm thick $In_{0.17}Al_{0.83}N$ barrier HFETs improved f_T to 245 GHz with the simultaneous application of oxygen plasma treatment on the surface to reduce the gate extension[4]. The highest f_T of 370 GHz was demonstrated on 7.5 nm thick $In_{0.17}Al_{0.83}N$ barrier HFETs. This high value was attributed to the regrown ohmic contacts which can reduce the parasitic effects.

The AlGaN/GaN HFETs are already commercially available for high power RF amplification applications, and InAlN/GaN HFETs are in the process of commercialization. Despite the impressive performance recorded, these devices are saddled with long term reliability. The degradation of the HFETs devices are usually characterized by surface trap generation[5] and hot-electron degradation[6], [7], pits and crack formation at the gate edge[8]. A common method for testing HFETs device reliability is to apply high electric field to the device with or without drain current. Researchers are focusing on the influence of electrical stress on the dc performance such as, change of threshold voltage, change of drain and gate current, and trap information, etc. The location of the failure has been exclusively ascribed to the gate edge close to the gate-drain access region where the electric field is the highest. A popular proposed mechanism for the degradation is the so-called inverse-piezoelectric effect [9] based on the hypothesis that mechanical strain produced by the high gate-drain voltage may aggravate the tensil strain caused by the lattice mismatch between AlGaN barrier and GaN layer, where the proposed degradation mechanism indicated the existence of a critical gate-drain voltage,

beyond which the HFETs device started to degrade abruptly. However, permanent degradation was found even for stress below critical voltage with sufficiently long stress time for reverse-gate-bias stress, supporting the hypothesis that permanent degradation is due to a defect percolation process[10]. Other proposed degradation mechanisms include hot-electron induced trap generation [6], impurity diffusion during the early stage of degradation[11], oxidation of device surface[12], and hot-electron/phonon effects[13], [14]. Although active researches are being done, there is no consensus on the underlying degradation mechanisms for AlGaN/GaN based HFETs.

The interest of using InAlN/GaN HFETs is due to the large two-dimensional electron gas (2DEG) in the heterostructure induced by the large polarization charge at the InAlN/GaN interface. More importantly, the InAlN layer can be grown lattice-matched to the underlying GaN layer for an indium composition around 17%~18%[15], under which indium compositions the 2DEG density are much larger than that induced by commonly used $Al_{0.25}Ga_{0.75}N$/GaN HFETs. The 2DEG density will increase monotonically with decreasing the indium composition due to the piezoelectric polarization charge, which varies between 0.90×10^{13} to $1.64\times10^{13}\,cm^{-2}$ for an indium composition between 20% and 12%[16], respectively. The 2DEG density for InAlN/GaN HFETs can be almost doubled to that of AlGaN/GaN HFETs, of which a 2DEG density of around $0.76\times10^{13}\,cm^{-2}$ can be achieved for a commonly used aluminum composition of 25% [17]. Device performance reported by several groups indicates large current density[18] and large output power density[19]. The specialty for InAlN/GaN HFETs is that the InAlN barrier layer can be

grown lattice-matched to the GaN substrate. This will certainly avoid the inverse-piezoelectric effect[20], which is proposed to be the degradation mechanism for AlGaN/GaN HFETs due to the strain caused by lattice-mismatch. However, the much larger current density in InAlN/GaN HFETs will impose a critical issue due to the stronger hot-electron, hot phonon (non-equilibrium optical phonon)[13], and self-heating (excess acoustic phonon) effects.

CHAPTER 2 Characterization techniques

2.1 Temperature-dependent gate lag measurement

Gate lag is a delayed response of the drain current with respect to the gate voltage variation. A typical usage of gate lag for testing trap information in GaN based HFETs is to bias the drain terminal at a static voltage and pulse the gate bias from under pinch-off voltage to zero gate bias while monitoring the transient drain current versus time. Under reverse gate bias, electrons can tunnel through the gate contact and be captured by electron traps in the AlGaN barrier around the gate area. When the reverse gate bias is removed, the trapped electrons are energetically unstable and thus start to emit at a certain rate depending on the time constant of the traps which is temperature-dependent. Since the 2DEG density is reduced by those trapped electron in the barrier, a transient behavior of the drain current would be expected when the barrier traps start to emit electrons at a certain time-constant after the removal of the reverse gate bias. The emission rate of the associated trap can be expressed as

$$e(T)=\frac{1}{\tau(T)}=\sqrt{\frac{3}{2\pi}}\frac{m^{*}k^{2}}{\pi\hbar^{3}}\sigma T^{2}\exp\left(-\frac{E_{A}}{kT}\right)$$

Equation 1

where τ is the time constant of the trap, E_A is the activation energy, σ is the capture cross section, k is the Boltzmann constant, $\hbar$ is the reduced Planck's constant, and m^* is the electron effective mass. By measuring the gate-lag at different temperatures, a series of emission rates can be recorded under corresponding temperatures, and the activation

energy and cross-section of the trap(s) can be obtained by using Arrhenius plot[21] based on Equation 1.

2.2 Flicker noise

The noise spectra of HFETs may consist of superimposed 1/f noise (or 1/f-like noise), generation-recombination (G-R) noise, and white noise, which is illustrated in Figure 1.The white noise is frequency-independent and relates to the device temperature. G-R noise in semiconductors originates from traps that randomly capture and emit carriers, thereby causing fluctuations in the number of carriers available for current transport. The power spectrum density (PSD) of the fluctuation for the G-R noise can be expressed as[22]

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+(2\pi f)^2\tau^2}$$

Equation 2

Here, τ is the time constant of the trap, and *f* is the frequency in the noise spectrum, the shape of which is called a Lorentzian. G-R noise is only significant when the Fermi level is close, within a few *kT*, to the trap energy level. If the Fermi-level is far above or below the trap level, the trap will be filled or empty most of the time. Thus few transitions will occur that can produce noise.

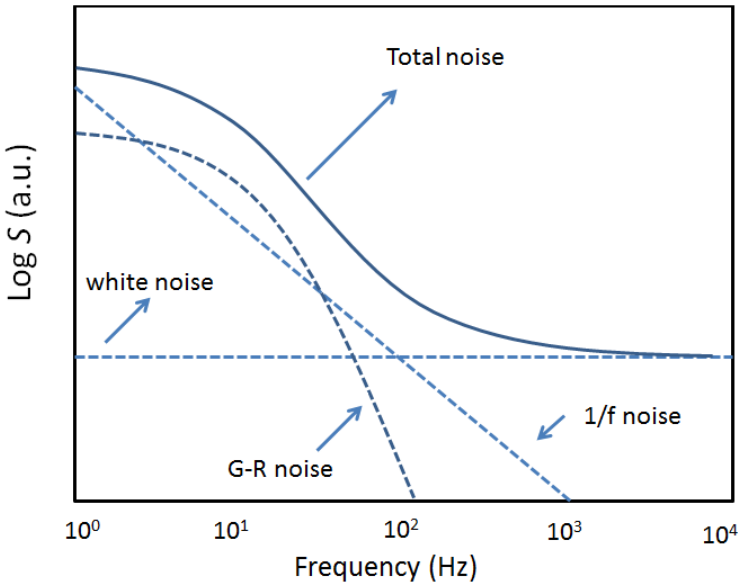

Figure 1 The noise power spectrum density (PSD) of low-frequency noise and white noise plotted vs. frequency. The PSD may consist of 1/f noise or generation-recombination (G-R) noise.[23]

$1/f$ noise, also called flicker noise, is the common name for fluctuations with a PSD proportional to $1/f^{\gamma}$ with γ close to 1, usually in the range of 0.7 ~ 1.3. There are essentially two physical mechanisms behind any fluctuations in the current: fluctuations in the mobility or fluctuations in the number of carriers. G-R noise from a large number of traps (number fluctuations) can produce $1/f$ noise if the time constants of the traps are distributed as[23]

$$g(\tau) = \frac{1}{\ln(\tau_2/\tau_1)\tau} \quad \text{for } \tau_1 < \tau < \tau_2$$

$$g(\tau) = 0 \quad \text{otherwise}$$

Equation 3

Superposition of the above continuous traps will form a $1/f$ shape spectrum, which is graphically illustrated in Figure 2. The fluctuations due to the mobility is described by Hooge with the following empirical formula for the resistance fluctuations[24]

$$\frac{S_R}{R^2} = \frac{\alpha_H}{fN}$$

Equation 4

The dimensionless parameter α_H, referred as the Hooge parameter, relates to the quality of the crystal and devices. Although the underlying mechanism(s) is still not clear, noise is a sensitive diagnostic tool for testing quality and reliability of electronic devices[25].

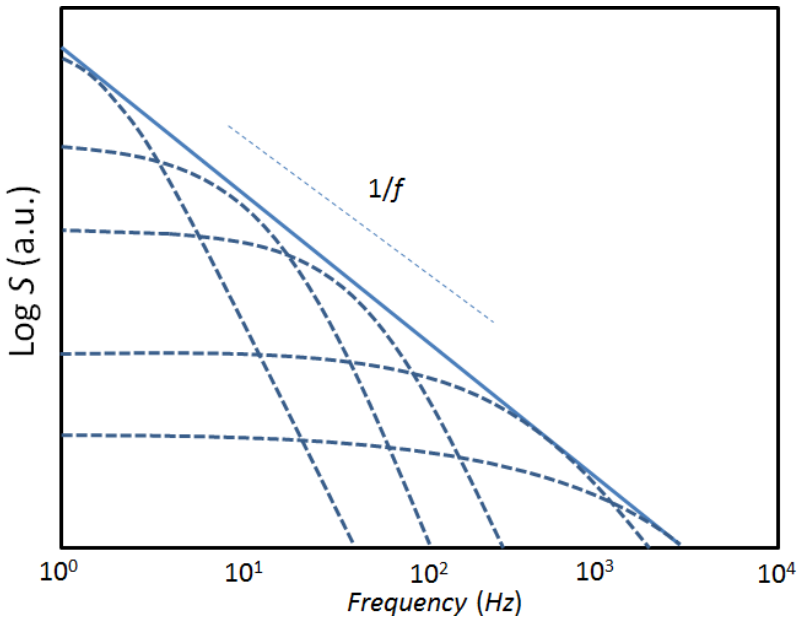

Figure 2 Superposition of 5 Lorentzians giving a total spectrum that approximately exhibits a 1/f dependence[23].

2.3 Microwave approach

The microwave properties involved in this thesis are focusing on the measurement of small-signal *s*-parameters of GaN based HFETs by HP8510C vector network analyzer in the frequency range of 2-20 GHz. The current-gain cutoff frequency (f_T) is determined by

$$h_{21} = (i_2/i_1)|_{v_2=0} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22})+s_{21}s_{12}}$$

Equation 5

Extrapolation of $|h_{21}|^2$ versus frequency to 0 dB leads to f_T , where the s-parameters are defined as,

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Equation 6

where the parameters a_1 and b_1 represent the incident and reflected power at the input port of the device under test with their amplitude and phase information. Similarly, a_2 and b_2 represent the incident and reflected power at the output port of the device under test with their amplitude and phase information. Models for small-signal equivalent circuit were built for GaN based HFETs, and the circuit is demonstrated in Figure 3. All the shown components are assumed to be frequency-independent in the small signal analysis, in addition to bias and input stimulus independent. As can be seen the circuit are separated into intrinsic and extrinsic parts. In the strict sense, the intrinsic part (within the dashed box) is nonlinear, bias dependent, and corresponds to the inner device that excludes the contribution from access regions as well as the stray capacitances. The extrinsic part

(outside the dashed box) can be assumed linear and bias independent corresponding to parasitic access elements. The small-signal *s*-parameters under different frequency and bias conditions can be used to extract the parameters in the equivalent circuits by following certain procedures. Firstly, the pad capacitance can be extracted under a pinched-off "cold-FET" condition (V_{DS}=0*V*, V_{GS} <<0*V*) at low frequencies (in the megahertz range) so that the influence of inductances can be minimized. Then the parasitic inductance and resistances are extracted under cold-FET conditions with large forward gate bias (V_{DS}=0*V*, V_{GS} >>0V) in order to reduce the depletion capacitance. After determining the extrinsic parasitic elements, the intrinsic circuit elements can be extracted from *s*-parameters measured under working bias conditions, and the corresponding methods are described in Ref.[26]. Because

$$f_{T,\mathrm{int}} = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{g_m}{2\pi C_{gs}} = \frac{v_{sat}}{2\pi L_g}$$

Equation 7

the small-signal gate-source capacitance (C_{GS}), gate-drain capacitance (C_{GD}), and transconductance (g_m) will be extracted only. The C_{GS} and C_{GD} parameters are defined as[27], [28]:

$$C_{GS} = \left[\frac{\partial Q}{\partial V_{GS}}\right]_{V_{GD}=const.} = C_{GS}^{depl} + C_{FS}$$

Equation 8

$$C_{GD} = \left[\frac{\partial Q}{\partial V_{GD}}\right]_{V_{GS}=const.} = C_{GD}^{depl} + C_{FD}$$

Equation 9

where Q is the space charge underneath the gate area, C_{GS}^{depl} is the capacitance component from the depletion region under the gate on the source side, C_{GD}^{depl} is the capacitance component from the depletion region under the gate on the drain side, C_{FS} and C_{FD} are the corresponding fringing capacitance contributions.

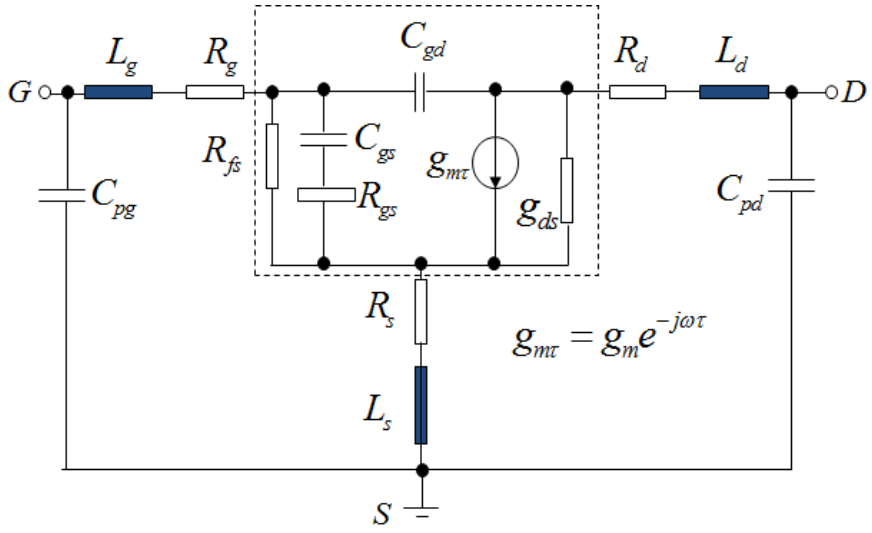

Figure 3 Small-signal equivalent circuit used for the small-signal parameter extraction[26].

2.4 Measuring of channel resistance, source and drain resistance

In HFETs structures, the channel resistance can be modulated by the gate voltage, and the channel resistance can be related to the gate voltage and threshold voltage (in GaN HFETs, the threshold voltage is the pinch-off voltage) as:

$$R_{ch} \propto \frac{1}{V_{GS} - V_{TH}}$$

Equation 10

where R_{ch} is the channel resistance under the gate as schematically demonstrated in **Figure 4**. The source resistance Rs and drain resistance Rd can be assumed to be constant when biasing the HFETs in the linear region where the drain bias is small. By varying the gate bias, the channel resistance changes while the source and drain resistance remained unchanged. By plotting the total drain-source resistance versus $\frac{1}{V_{GS} - V_{TH}}$, the sum of source and drain resistance can be determined. The channel resistance under a specific gate bias can be determined as well afterwards.

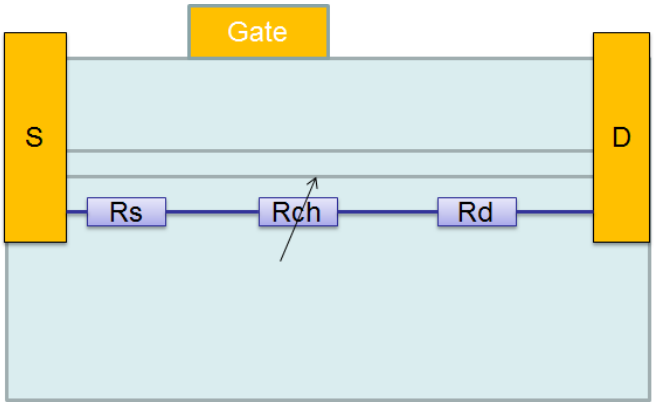

Figure 4 Schematic of HFETs showing the principles of measuring the channel resistance Rch, the sum of source and drain resistance (Rs+Rd)

CHAPTER 3 Degradation of un-passivated AlGaN/GaN HFETs

3.1 Degradation performance at room temperature

The AlGaN/GaN HFET structures were grown by metalorganic chemical vapor deposition (MOCVD) on *c*-plane sapphire substrates. The structures are comprised of a 2-µm-thick undoped GaN layer followed by a 1nm-thick AlN spacer, and a 20 nm-thick unintentionally doped $Al_xGa_{1-x}N$ (x=0.25) barrier. The source and drain contacts were formed using standard photolithography and Ti/Al/Ni/Au (30/100/40/50 nm-thick) metal stacks annealed at 800 ^oC. Mesa isolation was performed in a SAMCO inductively coupled plasma (ICP) system using a Cl-based chemistry. Gate electrodes were formed by deposition of Ni/Au (30/50 nm-thick) metal stack. The gate length, the gate width, and the source-drain spacing are L_G=2.0 µm, W_G=90 µm, and L_{SD}= 7 µm, respectively. The schematic diagram for the devices is illustrated in Figure 5, and the band structures under the gate featuring the on-state and off-state of this HFET device are presented in Figure 6. The I-V family and transconductance (g_m) for a typical pristine device is plotted in Figure 7, where we can clearly see that the pinch-off voltage is around -3.5*V*.

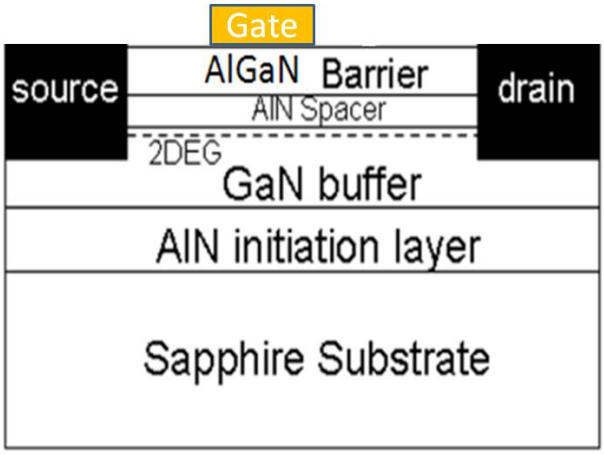

Figure 5 Schematic diagram of AlGaN/GaN HFET structure used for electrical stress experiments.

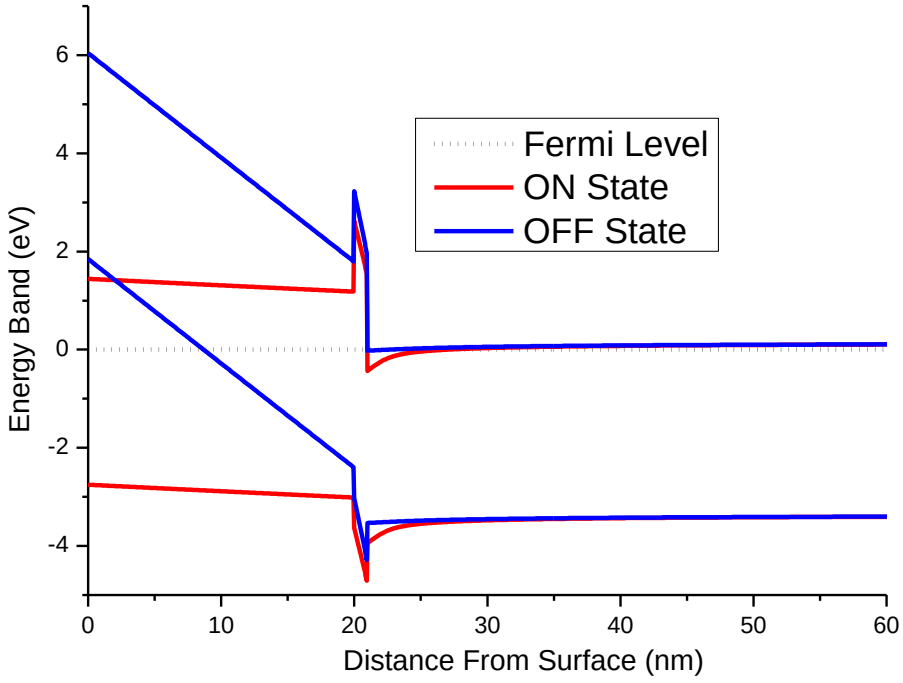

Figure 6 Band structure of an AlGaN/AlN/GaN HFET device under on-state (V_{GS}=0V) and off-state (V_{GS}=-4V), respectively.

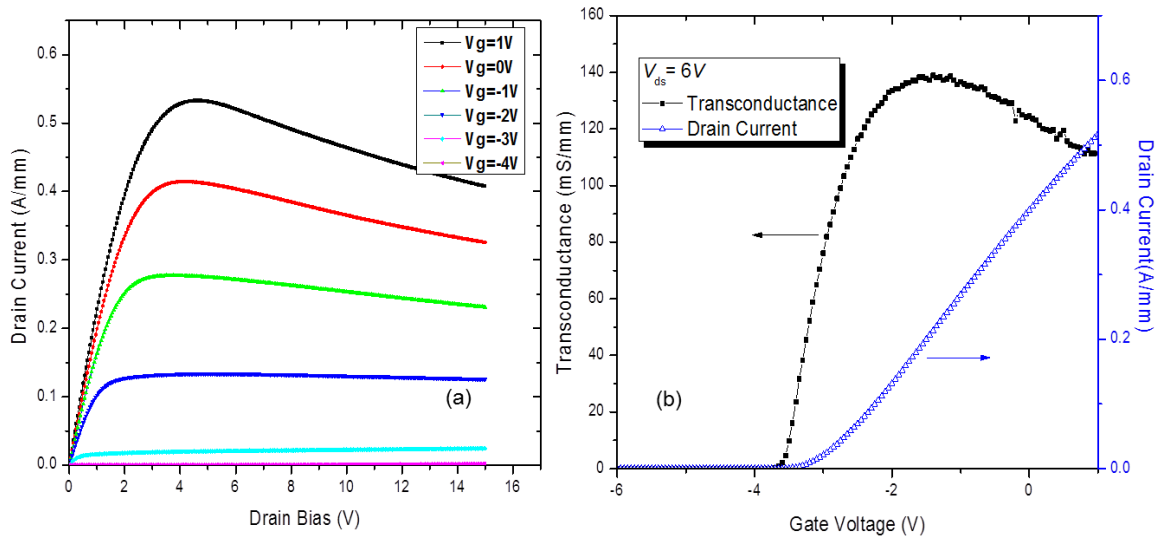

Figure 7 (a) I-V family and (b) transconductance (g_m) measured at V_{DS}=6V for a pristine device.

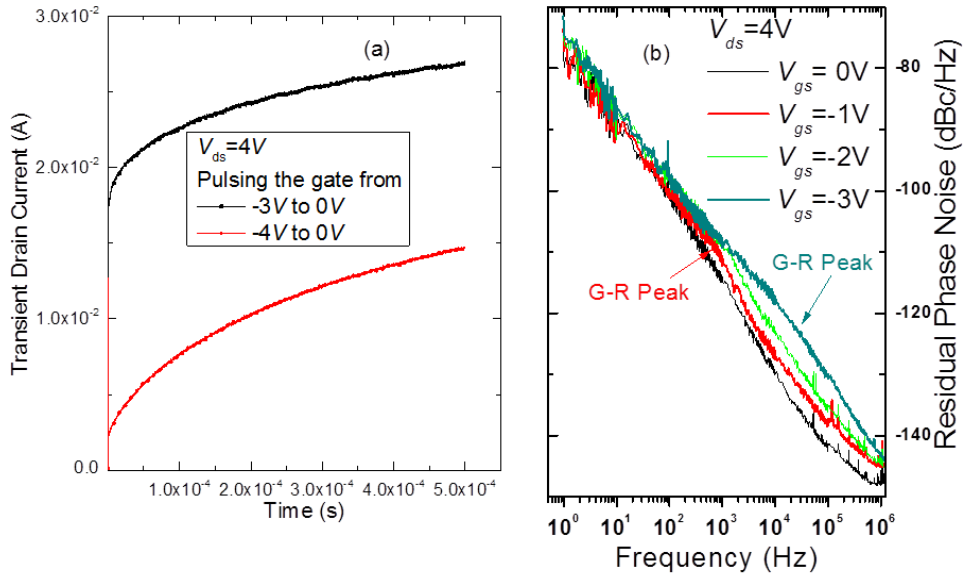

Figure 8 (a) Gate-lag measured at V_{DS}=4V and pulsing the gate bias from -3V, -4V to 0V, respectively, and (b) noise spectra measured at V_{DS}=4V and various gate biases.

Figure 8 shows the gate lag and noise spectra. As we can clearly see, the drain transient current shows gradual increase with time, which clearly indicated lagging effect with

larger reverse gate bias inducing larger lagging effect. Correspondingly, a G-R peak appears in the noise spectra and this G-R peak has a larger intensity and shifts to higher frequency with further reverse gate bias. The possible reason might be the electric field induced by the gate voltage lowers the barrier of the traps, which makes the capture and emit process more frequent. Since the barrier of the traps is lowered by the electric field (Poole-Frenkel effect [29]), the activation energy as well as the time-constant of the trap will decrease, which is the reason why the G-R peak shifts towards higher frequency.

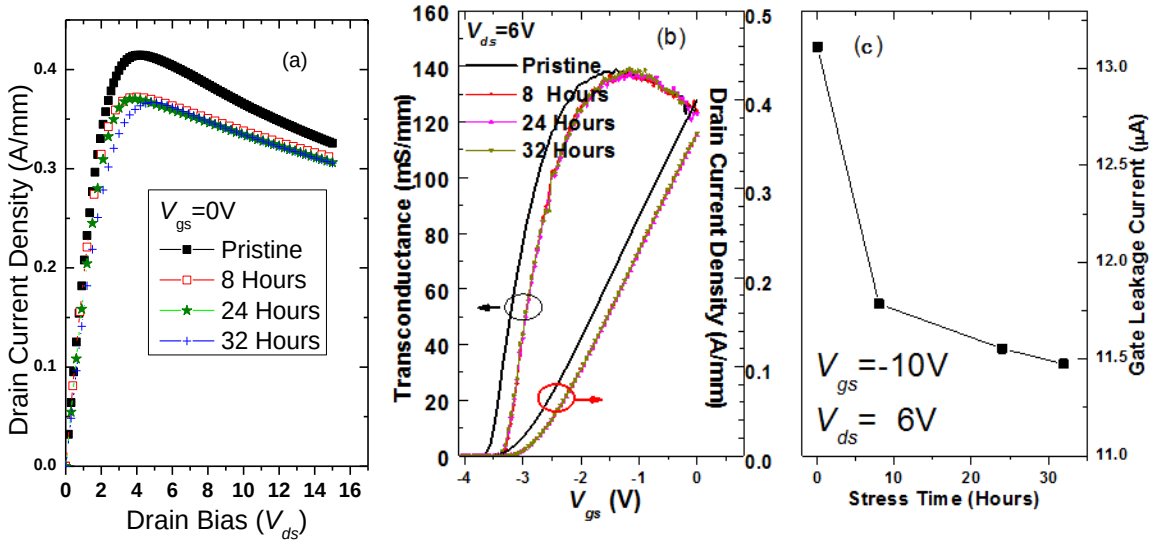

Figure 9 The electrical properties of the HFET change upon on-state-high-field stress up to 32 hours. (a) The drain current gradually decreases after stress; (b) The pinch-off voltage have a positive shift after the first 8 hours stress; (c) The gate leakage current at V_{GS}= -10V & V_{DS}=6V becomes small after each stress.

Upon electrical stress under the on-state-high-field condition (V_{GS}=0V, V_{DS}=20V), the device performances show a series changes as demonstrated in Figure 9, characterizing by a decrease of drain current, positive shift of the pinch-off voltage, and reduction of gate leakage current. Aside from that, the devices show larger gate lag and smaller noise after

stress as demonstrated in Figure 10. The reduction of the drain current was consistent with the positive shift of the pinch-off voltage; especially most of both changes occurred in the first 8 hour stress. Thus, we can conclude that the reduction of the drain current in the first 8 hours primarily comes from the positive shift of pinch-off voltage, which can be due to electrons getting trapped and/or negatively charged traps being generated underneath the gate[30]. These trapped electrons and/or negatively charged traps are most likely more stable or equivalently having a longer time-constant than the pre-existing traps, which makes the lagging effect larger as demonstrated in Figure 10(a). The trapped electrons reduce the positive charges associated with the surface shallow donors, thus the gate-drain electric field is reduced, lowering the electron injection from the gate and reducing the gate leakage current[31]–[33]. Additionally, this reduces the trapping or de-trapping of electrons by surface donor-like states, which may be the reason for the near disappearance of the G-R peak and reduction of the noise as demonstrated in Figure 10(b). The activation energy of the pre-existing traps is extracted to be 0.20±0.02 e*V* via the temperature-dependent gate-lag measurements as demonstrated in Figure 11. Please be reminded that the activation energy was extracted under a drain bias of 6*V*, so the zero-field activation energy will be larger.

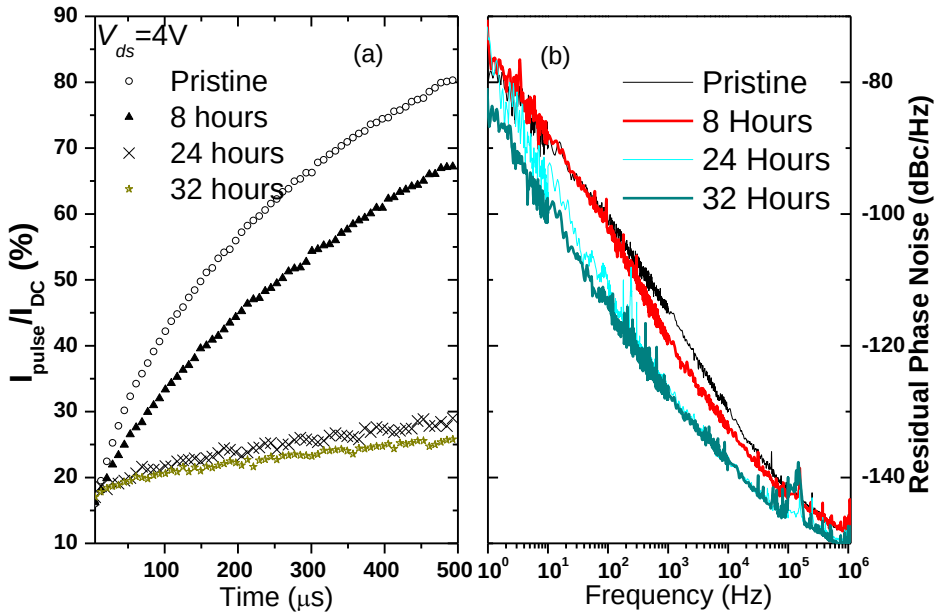

Figure 10 (a) Gate lag normalized to dc values measured at pulsing V_{GS} from -4 to 0V and (b) noise spectra measured at V_{GS}=0V and V_{DS}=4V for different stress times.

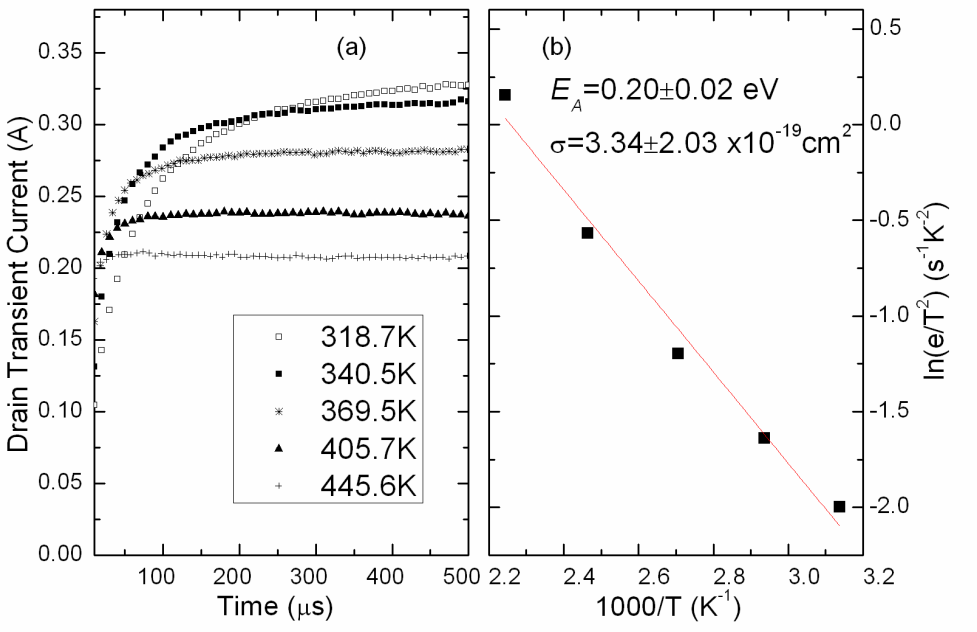

Figure 11 (a) Gate lag measured at different temperatures at V_{DS}=4V and pulsing V_{GS} from -4 to 0V on a pristine device. (b) The resulting Arrhenius plot from which an activation energy of 0.20±0.02 eV has been extracted.

3.2 Effect of temperature on the AlGaN/GaN degradation

AlGaN/GaN HFETs were also subjected to on-state-high-field (V_{GS}=0V & V_{DS}=20V) stress under different temperatures to investigate the effect of temperature on the device degradation. As we can see from Figure 12, degradations in terms of gate lag are characterized by an increased lagging effect for all stress conditions. For room-temperature stressed devices, the gate-lag mostly happened at shorter time scale. While for stressed devices at higher external base plate temperatures, the gate-lag becomes almost flat, which means the time-constant for the associated traps must be very long, thus the transient currents need very long time to recover. This assertion is also consistent with the noise results as demonstrated in Figure 13. The noise spectra decreased for devices stressed at room temperature, which is the same as demonstrated before Figure 10(b). For devices stressed at higher temperatures, the noise decrease about 20 dBc/Hz for "relaxed" condition (A relaxed condition means the device is not under operation for more than 1 day), which is about 10 dBc/Hz more than that decreased in devices stressed at room temperature. The results imply that a significant amount of long time-constant traps must be created in devices stressed at higher external base plate temperatures, and these long time-constant traps are more stable thus they make the pre-existing short time-constant traps not accessible to electrons. In this way, the contribution from these pre-existing short time-constant traps was diminished which explained why such a large decrease of noise occurred in devices stressed at high temperatures. The generated long time-constant traps in devices stressed at high temperatures must have time-constant much longer than 1 second (corresponding to frequencies smaller than 1 Hz in noise spectrum), which is

outside the frequency range of the spectrum (1 Hz to 10^6 Hz), thus they didn't show in the noise spectrum. As we mentioned above, the noise data for the stressed devices shown in Figure 13(b) and (c) are for devices in relaxed condition, which means the stressed device are not under any operation for more than 1 day prior to the noise measurement. When biases were applied to the gate or drain terminal, a large transient behavior occurred for devices stressed at external base plate temperatures of 100 ^{o}C and 150 ^{o}C. The transient phenomena for devices stressed at 150 ^{o}C are demonstrated in Figure 14.

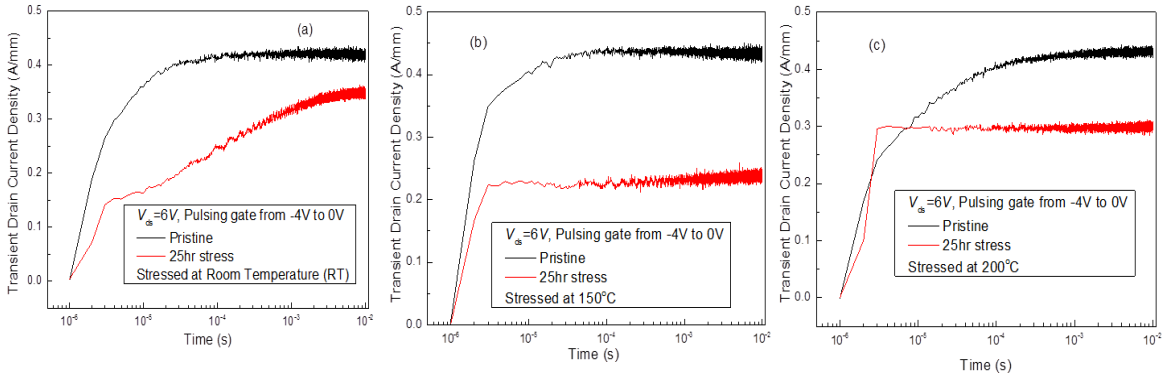

Figure 12 Gate Lag measurement of $Al_{0.25}Ga_{0.75}N$/GaN HFETs stressed at V_{GS}=0V and V_{DS}=20V at external base plate temperature of (a) room temperature; (b) base plate temperature of 150 ^{o}C; (c) base plate temperature of 200 ^{o}C. The drain bias for the gate lag measurement was fixed at V_{DS}=6V, and the gate bias was pulse from V_{GS} =-4V to V_{GS} =0V with a duty cycle of 1%.

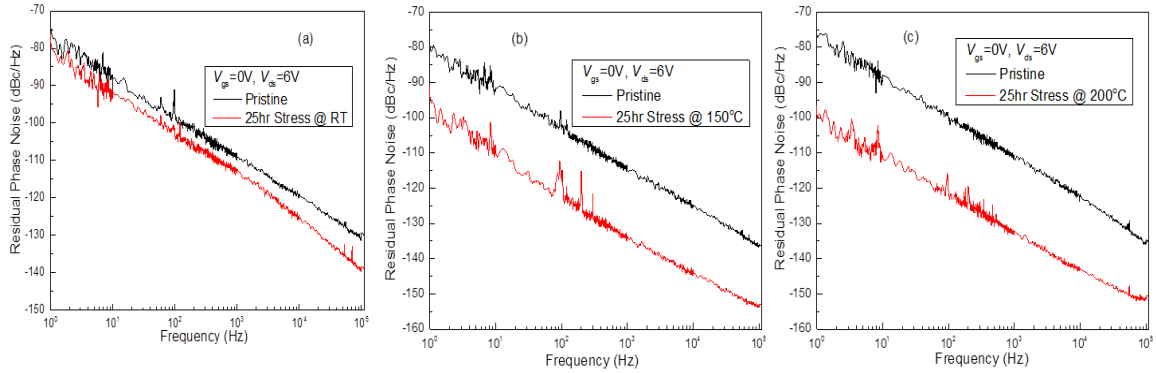

Figure 13 Noise spectra for pristine AlGaN/GaN HFETs and devices stressed under on-state-high-field stress (V_{GS} =0V & V_{DS} =20V) at an external base temperature of (a) room temperature; (b) 150 ^{o}C; (c) 200 ^{o}C. The measurements were for relaxed devices under the measurement bias condition of V_{GS} =0V & V_{DS} =6V.

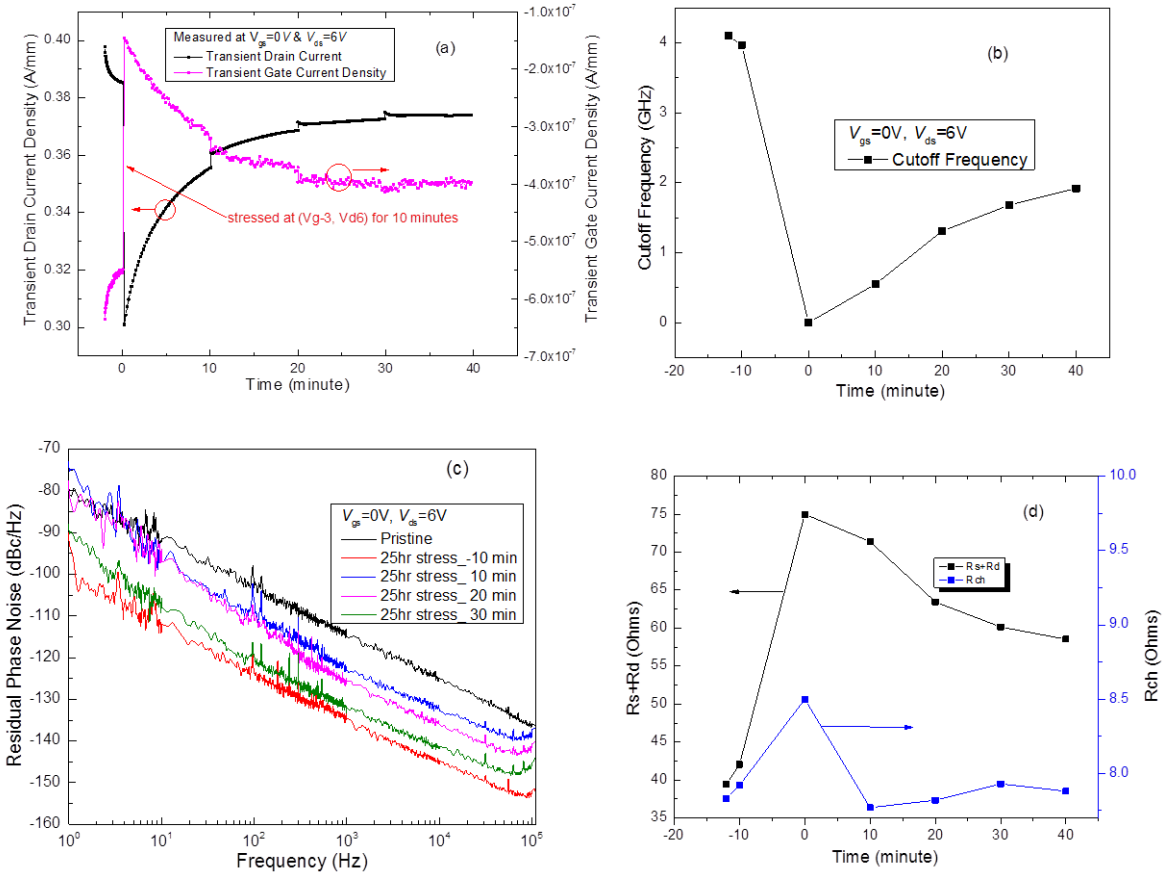

Figure 14 Transient effects for an AlGaN/GaN HFET device stressed under on-state-high-field stress at 150 ^{o}C. After stress, the device was biased under V_{GS} = -3V & V_{DS} = 6V for 10 minutes, and the time was set to zero when this bias condition was removed. For convenience purpose, we call this process as "temporary stress". Various measurements started immediately after the removal of this bias condition. (a)The drain current for a measurement bias condition of V_{GS} =0V & V_{DS} =6V. The drain current increased from 0.30 A/mm to almost 0.38 A/mm in 40 minutes after the temporary stress. (b) Transient behavior of cutoff frequency before and after this temporary stress. (c) Transient noise behavior before and after temporary stress. (d) Transient behavior of channel resistance (R_{ch}) and sum of source and drain resistance (R_s+R_d) before and after temporary stress.

Figure 14 (a) demonstrates that the drain current decreased by about 30% after temporal stress under the bias condition of V_{GS} = -3V & V_{DS} = 6V for 10 minutes, and the drain current almost recovered after 40 minutes. Figure 14(b) shows the transient behavior of

current gain cutoff frequency (f_T) measured at V_{GS} =0V & V_{DS} =6V before and after temporal stress, where we can see that the cutoff frequency recovered to only half of the value of a relaxed device, which was different from the fully recovered drain current for the same time period. The noise data presented in Figure 14(c) is also consistent with the phenomena of drain current and cutoff frequency. For stressed devices under relaxed condition, the noise is very low, of which the noise increased ~15dBc/Hz at 10 minutes after the temporal stress. The noise gradually decreased or recovered to the relaxed condition after the removal of the temporal stress. The change of channel resistance (R_{ch}) and the sum of source and drain resistance (R_s+R_d) were also monitored during this transient process, and the results are plotted in Figure 14(d), which clearly shows that most of the change of drain current came from the change of the R_s+R_d, especially when the relaxing time is larger than 10 minutes. Since the drain access region is where the electric field is largest, the impacted area is most likely located at the drain access region close to the gate edge, where electrons getting trapped in the drain access region close to the gate and they deplete electrons in the channel and caused the increase of the drain access resistance (R_d). The drain current got larger during the recovery process as demonstrated in Figure 14(a), thus de-trapping of electrons must occur during the recovery process. Since the noise spectrum is only sensitive to short time-constant traps, active de-trapping of electrons must exist for short time-constant traps, although de-trapping from long time-constant traps may also contribute. Since devices stressed at higher external base plate temperature showed 20 dBc/Hz lower noise at relaxed condition than that of pristine devices, long time-constant traps should be generated around the gate during the stress.

The existence of these long time-constant or more stable traps are necessary so that they prevent electrons from accessing the short time-constant traps, which can be the reason why we see the long recovery process. The short time-constant traps formed the so-call virtual gate or gate extension[34], which extended from the physical metal gate making the effective gate length longer and deteriorate the current gain cutoff frequency f_T. All these results are consistent with the slow transients observed elsewhere [35], and the possible reason should be due to surface effect induced by the electrical field and high temperature. It has been found out that these surface effects can be largely removed by SiN_x passivation[35], which can provide a more stable surface and hence better HFET performance. Thus it is imperative that a proper surface preparation technique should be introduced to provide a stable surface and device performance, especially if the devices are intended to be operated under high bias and high temperatures.

Chapter 4 Passivation and Surface Pre-treatment

4.1 Motivation for passivation

The purpose of using SiN_x passivation is to remove the surface states as well as associated electrons, and further prevent the electrons getting trapped in the access regions on the surface. Since the electrons are removed from the surface, the 2DEG density in the channel will increase and the drain current density will increase. More importantly, the gate extension caused by the surface states will be reduced, making an effective gate length close to the actual physical dimension of the metal gate, thus an increased f_T. The detailed passivation procures were as follow: The un-passivated devices were cleaned by standard solvent cleaning procedure, and they were loaded into the loading chamber of plasma enhanced chemical vapor deposition (PECVD) system. Then a 100nm SiNx film was deposited onto the HFETs wafer at a substrate temperature of 270 ^{o}C, which is the highest achievable temperature for our PECVD system. Then ICP dry-etching with fluorine based recipe was used to open the window to the Ohmic contact pads and gate pads. Figure 15 showed a cross section view of a HFET structure with SiNx passivation on the surface, where the whole metal gate and access are covered by SiNx. Since electrical stress at temperatures of 150 ^{o}C and 200 ^{o}C caused a large trapping effect around the gate at the drain access region, oxidized surface layer is suspected to be the reason[36]. Chemical pre-treatment using mild acid or base solution before the deposition of SiNx layer can be used to remove the surface oxide layer and achieve better interface properties between the SiNx layer and the HFETs surface layer [37] [38]. Thus, surface pre-treatment procedure using hydrochloric acid (HCl) or ammonium sulfide ($(NH_4)_2S_x$) solution was adopted

trying to ensure a cleaner surface before passivation, and the correspondingly results are compared to passivation without surface pre-treatment. To avoid etching of Ohmic contact and gate metal by HCl and $(NH_4)_2S_x$, the following conditions are used. For HCl, a 33% solution was mixed with de-ionized water at 1:3 ratios to treat the wafer for 60 seconds before loading wafer to PECVD chamber. For $(NH_4)_2S_x$, a 20% solution was mixed with de-ionized water at 1:3 ratios to treat the wafer for 10 minutes at room temperature. Then the wafers were blown dry and immediately loaded into the PECVD vacuum chamber for subsequent SiNx deposition.

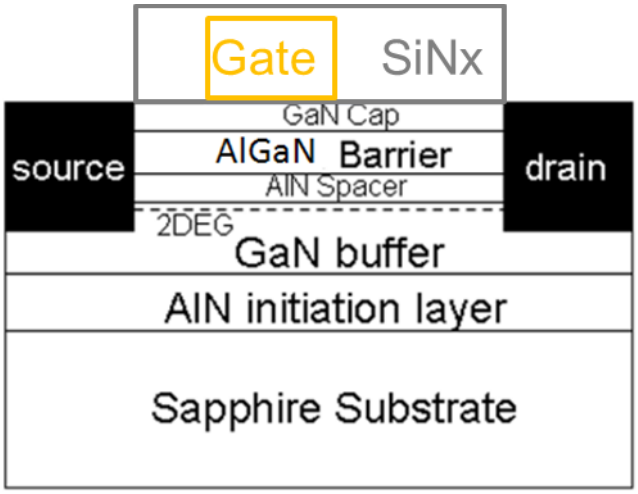

Figure 15 A cross section vie of the HFETs structure with the devices passivated by SiNx. The whole wafer is covered by SiNx to protect electrons getting trapped on the surface. The Ohmic contacts and gate pads were exposed by ICP etching with fluorine based chemistry so that electrical measurements can be conducted.

4.2 Effect of passivation and surface pre-treatment

To demonstrate the effect of passivation, the current collapse phenomena were showed in un-passivated devices for comparison. As demonstrated in Figure 16(a) for un-passivated devices, a large current collapse was observed after repeated drain current measurement, and most of the current reduction is observed to be close to the large gate bias condition (large drain current), which means that the major electron trapping sites occurred at the drain access region[39], which is the location where the electric field is the highest and it's exposed to air. A test wafer with $Al_{0.25}Ga_{0.75}N$/GaN HFETs was cut into three pieces to test the effect of passivation as well as surface pre-treatment. All procedures for the three pieces are exactly the same except whether they have pre-treatment and what type of pre-treatment was used.

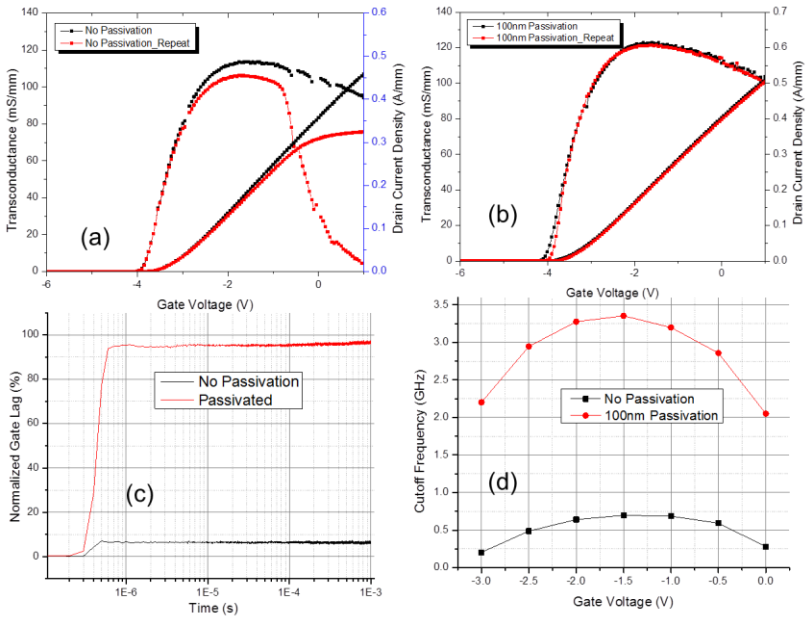

Figure 16 The effect of passivation on the device performance; (a) Measurements of drain current and transfer characteristics at V_{DS} =6V. The measurement was repeated immediately after each other; (b) Repeated measurements of drain current and transfer characteristics at V_{DS} =6V for passivated devices without any surface pre-treatment; (c)Gate Lag measured before and after passivation without surface pre-treatment; (d) f_T measured at V_{DS} =6V before and after passivation without surface pre-treatment.

Piece A was deposited with 100nm thick SiNx by PECVD without any surface pre-treatment. Upon passivation without pre-treatment, the current collapse was greatly reduced as demonstrated in Figure 16(b). By comparing the drain current for the same bias condition, we find out that a ~10% increase in drain current was observed after passivation. The ratio of pulse drain current to DC drain current has increased tremendously to an amount of almost 100%. These improvements were also consistent with the increase of the f_T, which means the surface-states induced gate-extension was reduced after passivation. The results showed that SiNx can effectively passivate the surface and prevent electron trapping on the surface at the drain access region, although some gate lag still exist after passivation. Piece B was pre-treated with $(NH_4)_2S_x$ solution for 10 minutes at room temperature and then deposited with 100 nm SiNx by PECVD, and the corresponding measurement results are demonstrated in Figure 17. The results are quite similar to Piece A with even larger gate-lag as demonstrated in Figure 17(c). Piece C was pre-treated with diluted HCl solution at room temperature for 60 seconds, and the measured results are demonstrated in Figure 18. The results are similar to what has been demonstrated in Figure 16 and Figure 17. However, as demonstrated in Figure 18(c), the ratio of pulse drain current to the dc drain current is larger than 100%, which means there is no gate lag for HCl treated wafers. The reason why the ratio is larger than 100% is because the self-heating is very small under pulse measurement. Since the gate-lag is the parameter that directly relates to the surface states if assume electron traps in the barrier are the same for all three pieces from the same wafer, we can argue that the HCl pre-treated piece gave the

best performance in terms of ability to remove surface traps. Thus, this pre-treatment method is used as a standard procedure prior to SiNx deposition.

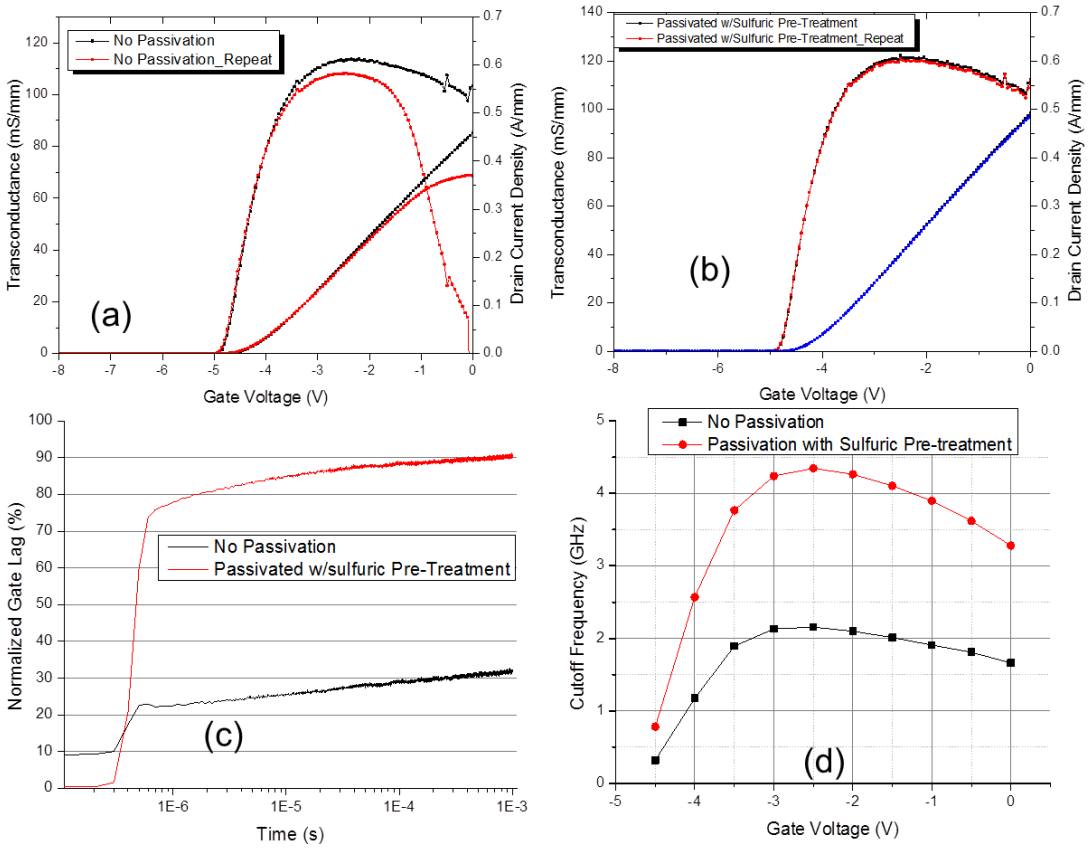

Figure 17 The effect of passivation with $(NH_4)_2S_x$ solution pre-treatment on the device performance; (a) Measurements of drain current and transfer characteristics at V_{DS} = 6*V*. The measurement was repeated immediately after the first measurement; (b) Repeated measurements of drain current and transfer characteristics at V_{DS} =6*V* for passivated devices with $(NH_4)_2S_x$ pre-treatment; (c)Gate Lag measured before and after passivation with $(NH_4)_2S_x$ pre-treatment; (d) f_T measured at V_{DS} =6V before and after passivation with $(NH_4)_2S_x$ pre-treatment.

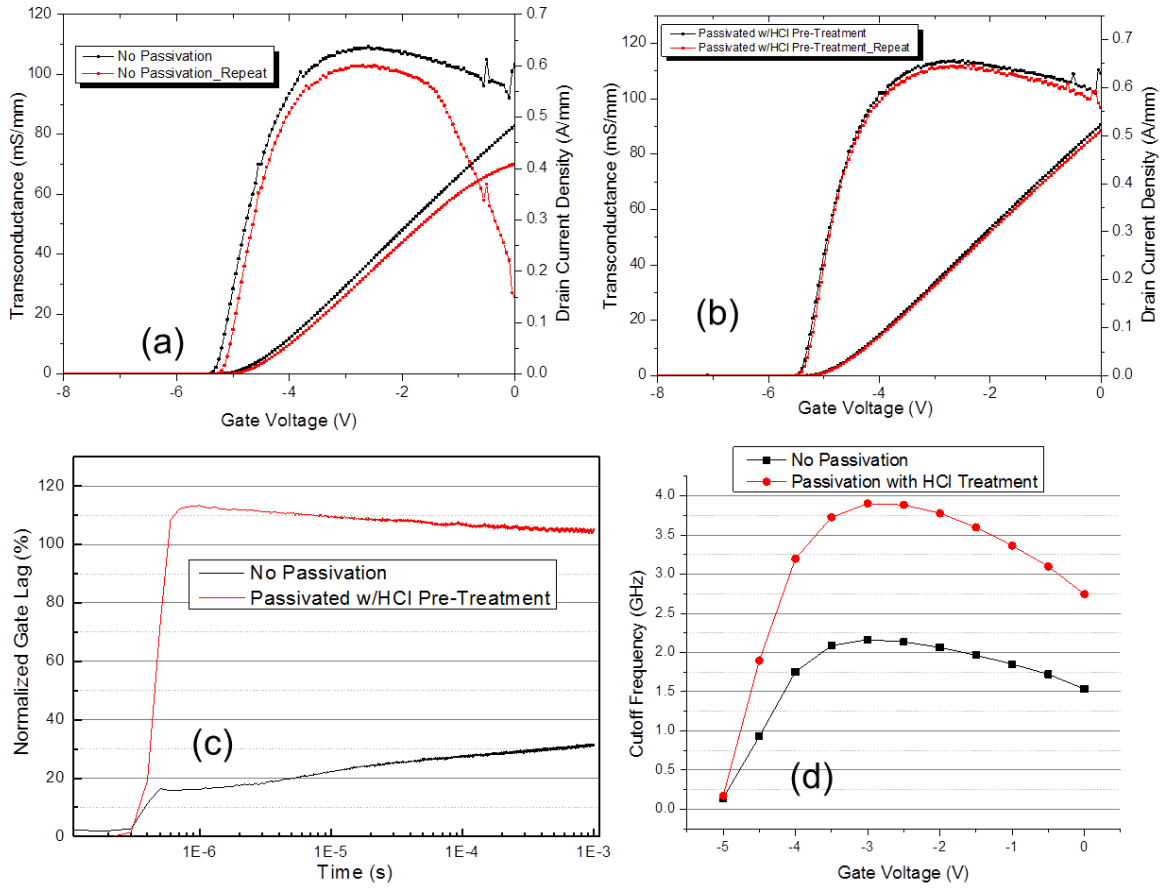

Figure 18 The effect of passivation with HCl solution pre-treatment on the device performance; (a) Measurements of drain current and transfer characteristics at V_{DS} =6*V*. The measurement was repeated immediately after each other; (b) Repeated measurements of drain current and transfer characteristics at V_{DS} =6*V* for passivated devices with HCl pre-treatment; (c)Gate Lag measured before and after passivation with HCl pre-treatment; (d) f_T measured at V_{DS} =6*V* before and after passivation with HCl pre-treatment.

4.3 Mechanism for HCl treatment

The mechanism of ammonium sulfide treatment on GaAs substrate is to remove the surface oxidized layer while temporarily passivated the surface with a sulfide layer[40]. The question now is that will the mechanism for HCl treatment on GaN surface the same as that of ammonium sulfide on GaAs? Suppose that HCl treatment leaves Cl ions on the surface working as a temporal passivation layer, then the drain current after HCl treatment but before passivation should be smaller than that of without HCl treatment because Cl ions are most likely to be negatively charged due to their strong negativity. However, a larger drain current density was observed immediately after HCl treatment but before passivation as demonstrated in Figure 19(a) and (b). Thus, HCl removed all surface states; most likely those associated with oxide layer, but Cl ions most likely didn't remain on the surface acting as a temporary passivation layer. If some of them did remain on the surface and were negatively charge, the number of remained Cl ions should be smaller than those surface electrons removed by HCl solution because the drain current became larger after HCl treatment. This conclusion is consistent with Figure 19(c) which shows the gate lag results before and after HCl treatment. As we can see, more gate lag was observed after HCl treatment, which means that more electrons were trapped on the surface after HCl treatment upon applied reverse gate bias. This may be because the HCl treatment exposed all trapping site on the surface thus causing more lagging effect. If the Cl ions stayed at the surface after HCl treatment and they were stable on the surface, then the amount of surface trapping sites will be smaller. Then the gate lag effect should be smaller, which is not the case.

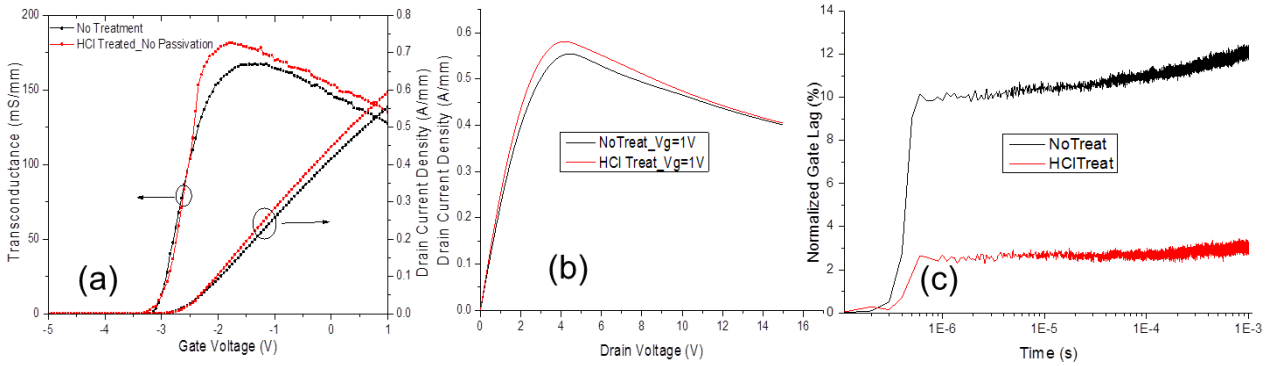

Figure 19 Effect of HCl solution treatment on AlGaN/GaN HFET devices without subsequent SiNx passivation. The devices performance was measured immediately after HCl treatment while the devices are not passivated. (a) Transfer characteristic measured at V_{DS} =6*V*; (b) Drain current measurement at V_{GS} =0*V*; (c) Gate lag measured at V_{DS} =6*V* while pulsing the gate from -4*V* to 0V.

Chapter 5 Simulation of AlGaN/GaN HFETs

5.1 Silvaco Atlas Simulation Software

In order to design devices with desired device performance, the cheapest and fastest way is to run simulation tools if it can accurately predict the device performance prior to the lengthy and expensive fabrications. However, precise material parameters as well as models should be used or established to achieve the best match between experimental and simulation results. In this chapter, a successful simulation of I-V family curve as well as transfer characteristic of an AlGaN/GaN HFETs will be demonstrated with proper material parameters, polarization field, and surface trap densities, layer mobility, as well as models by using commercially available simulation software Silvaco Atlas. The bandgap of $Al_xGa_{1-x}N$ at room temperature is calculated by[41]:

$$E_g(x) = 6.13x + 3.42(1-x) - x(1-x) \text{ eV}$$

Equation 11

and the dielectric constant is given by

$$\varepsilon_r(x) = 10.4 - 0.3x$$

Equation 12

The band alignment was chosen to be that the conduction band discontinuity will have a 70% of the whole bandgap discontinuity, and the work function of the Ni/Al Schottky contact was chosen to be 5.2 eV. The material parameters that were used for the simulation are listed in Table 1.

Table 1 Material parameters of GaN and $Al_{0.25}Ga_{0.75}N$ for Silvaco Atlas simulation.

Parameter	Description	Unit	GaN	$Al_{0.25}Ga_{0.75}N$
E_g	Band gap at 300K	e*V*	3.42	3.91
ΔE_c	Conduction Band offset between AlGaN and GaN	Fraction of E_g	0.7	0.7
μ_n	Low field electron mobility for 2DEG in GaN, or AlGaN	cm^2/Vs	1600	100
ε_r	Relative permittivity		8.9	8.96
Nc	Conduction band effective density of states at 300K	cm^{-3}	3.23×10^{18}	2.23×10^{18}
Nv	Valence band effective density of states at 300K	cm^{-3}	4.62×10^{18}	1.57×10^{18}
$\upsilon_{sat,n}$	Electron saturation velocity	cm/s	1.3×10^{7}	1×10^{4}
K_{300}	Thermal conductivity at 300K	W/K·cm	1.3	0.031
Alpha	Power factor for temperature dependent thermal conductivity		-0.43	-0.43

5.2 Device Structure and Determination of Variable Parameters

The device structure used for the Silvaco Atlas simulation is presented in Figure 20(a). All structure parameters, for example the barrier thickness and the mobility of the channel as well as the buffer electron mobility, are variables that can be adjusted to fit the experimental results, mainly the I-V family curve and transfer characteristics. The buffer unintentional doping was decided from C-V measurement from a Schottky diode on the same wafer, and the result is demonstrated in Figure 20(b). The C-V measurements were conducted at 1 MHz frequency. The polarization charges at each interface or surface were calculated according to the results in [41] . The surface donor states can be simulated as traps with certain ionization energy or can be simply mimicked as a surface doping, which can equivalently gave correct simulation if proper surface doping concentration is given.

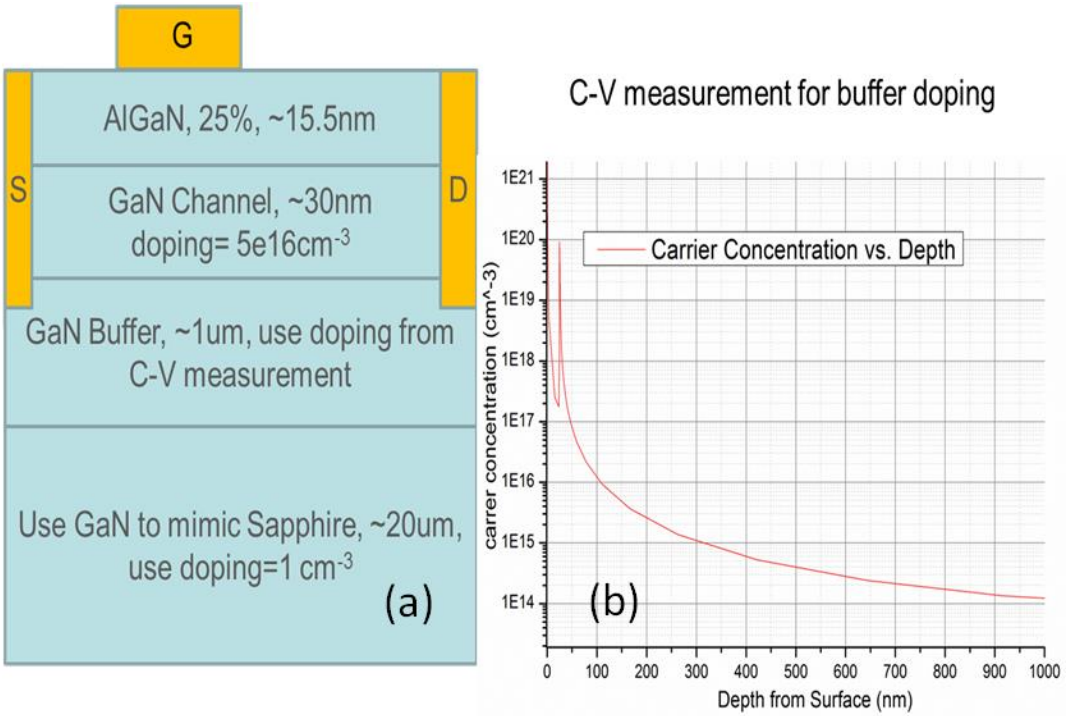

Figure 20 (a)Device structure used for Silvaco Atlas simulation; (b) Carrier concentration calculated from C-V measurement on a Schottky diode structure.

A 1600 cm^2/Vs mobility was used for the channel 2DEG electrons, however, the electron mobility in the buffer is unknown, which strongly depends on the buffer quality. A method to determine the buffer electron mobility is to simulated the buffer leakage and make sure that the simulated buffer leakage is smaller than the measured drain leakage (The drain leakage is composed of buffer leakage and gate leakage, thus the measured drain leakage is an upper limit of the buffer leakage). Although the exact buffer mobility cannot be precisely determined, the upper limit can be estimated using this method and the results are demonstrated in Figure 21. An upper limit of 2 cm^2/Vs was determined for the average buffer mobility from this method.

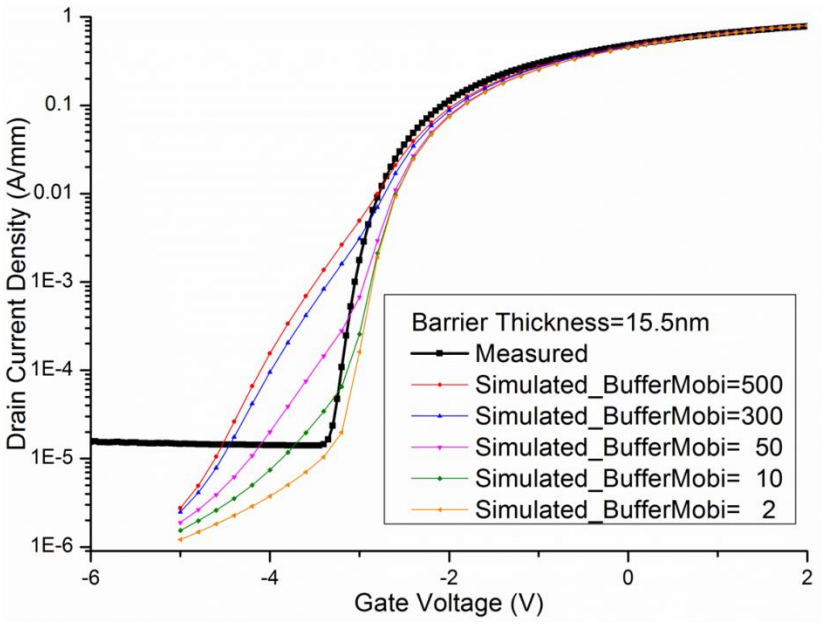

Figure 21 Simulated drain current vs. gate voltage by varying the buffer electron mobility, and the results are compared to measured results. In order to make sure that the drain leakage is smaller than the measured results, a buffer electron mobility of equal or smaller than 2 cm^2/Vs should be used.

Considering that electron mobility for electrons close to the 2DEG channel should be very high, then electrons in the lower end of the buffer have to have negative mobility in order to maintain an average buffer mobility of 2 cm^2/Vs, which means that the determined average electron mobility of 2 cm^2/Vs is too small and thus not practical. If a more reasonable electron mobility in GaN buffer (for example ~250 cm^2/Vs [42]) is used while maintaining the buffer leakage, the electron density in the buffer has to be decreased. Please be reminded that the mobile electrons that contribute to the current conduction in the buffer were assumed to come from doping in the simulation, where in reality they come from multiple donor traps. Donor traps with energy levels ranging from ~0.25 eV to ~0.70 eV [43] were reported in bulk GaN grown by hydride vapor-phase epitaxy (HVPE), which can be used as a reference for GaN buffer layer grown by MOCVD. The C-V measurements used to extract the free carrier concentration in the buffer were conducted under 1 MHz. Considering the case that 1) the emission rates of the deep traps are larger or comparable to the measurement frequency of 1 MHz, then the deep donor density will count towards the free carrier concentration as calculated in Figure 20(b), but at the same time 2) these traps may be deep enough that they may not be ionized under normal device operation. The key factor to ensuring these two conditions met at the same time is the cross section of the trap state. The ionization of the traps depends on the energy level only, while the emission rate also depends on the cross section of the traps. If a suitable emission rate is introduced, then it's possible to meet both assumptions. If these two assumptions can indeed be met, then the free carrier concentration calculated from C-V measurement is

overestimated, which is quite normal when traps with different energy levels are involved[44]. The situation might be even more complicated by carrier compensation from acceptor states from unavoidable carbon doping in MOCVD growth system. By assuming a more practical electron mobility of ~250 cm^2/Vs [42] in the buffer, the deep donor density has to be ~$3\times10^{15}cm^{-3}$ to match the drain leakage current if assuming an energy level of ~0.9 e*V* in MOCVD grown GaN buffer layer [42], and the simulation results are presented in Figure 22. In order to match the experimental result, a deep donor level which contributed to the free carrier concentration in C-V measurement while didn't contribute to carrier transport under device operation has to be incorporated with density of $3\times10^{15}cm^{-3}$. However, this hypothesis needs to be further verified by frequency-dependent as well as temperature-dependent C-V measurements so that an accurate determination of the trap information and carrier concentration in the buffer layer can be achieved.

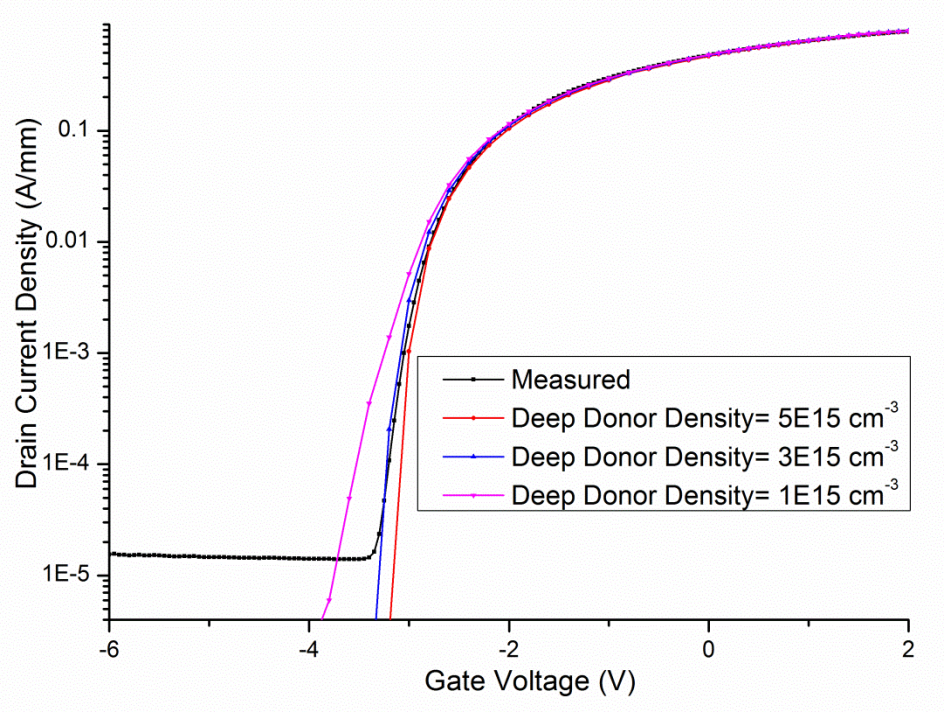

Figure 22 Silvaco Atlas simulation of drain leakage current by assuming electron mobility of 250 cm^2/Vs in the buffer. The deep donor was assumed to contrite to the free carrier concentration calculated from C-V measurement, while they will not contribute to the free carrier concentration under device operation.

To make the simulation process simple, we will still use the superficial electron mobility of 2 cm^2/Vs in the GaN buffer layer to determine other material parameters, such as barrier thickness and surface doping density. The barrier thickness is varied to ensure a pinch-off voltage that exactly fit the measured one, and a barrier thickness of 16.5 nm was adopted as demonstrated in Figure 23. And the surface doping density of 0.45×10^{20} cm^{-3} was used to ensure a proper drain current density at various gate voltages as presented in Figure 24. After proper adjustment for various parameters, the best fit to a representative device was demonstrated in Figure 25. The mismatch of the results at lower drain voltages might be due to the current collapse which was generally ascribed to be traps located in the GaN

buffer[45]. Additional trapping effect in the buffer layer should be included to better fit the measured results; however, our simulation procedure should work perfectly for a device without this trapping effect.

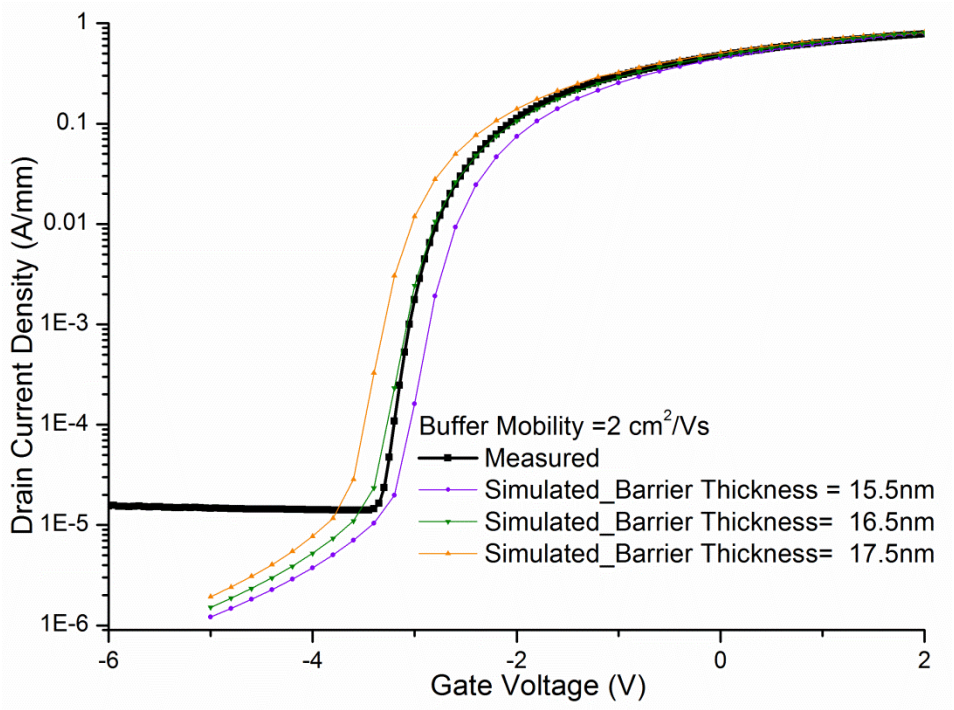

Figure 23 Determination of barrier thickness to ensure a correct threshold voltage.

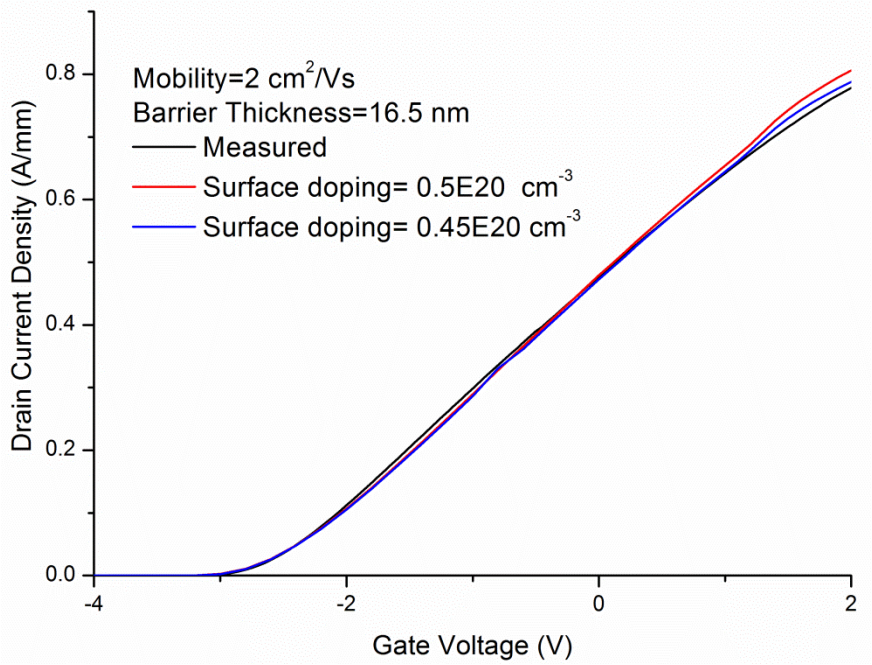

Figure 24 Determination of surface doping to ensure a proper drain current density at various gate voltages.

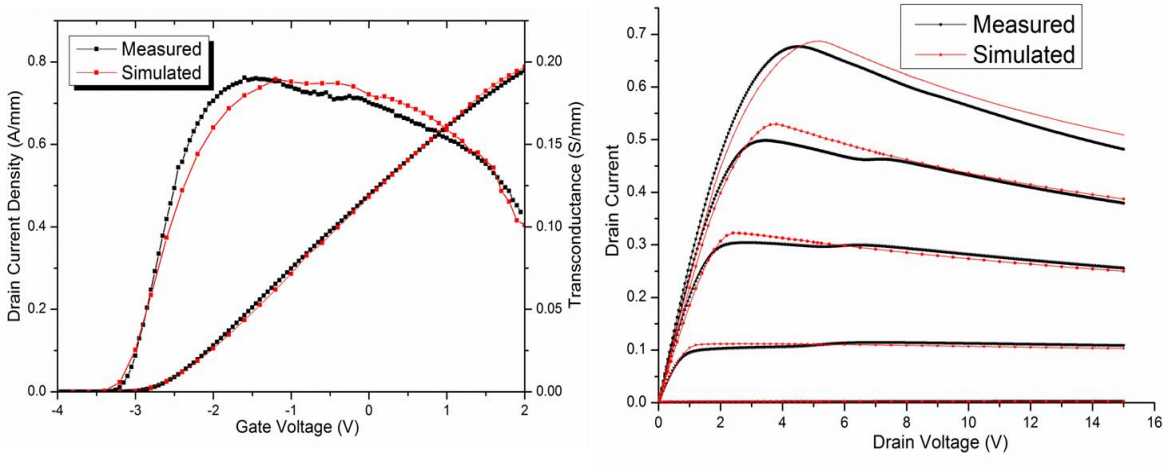

Figure 25 Comparison of simulated and measured results after adjusting various variables for (a) transfer characteristics and (b) I-V family curves.

5.3 Vertical electric field under different bias conditions

A popular theory explaining the degradation of AlGaN/GaN HFETs is the so-called inverse piezoelectric effect [9], which is based on the hypothesis that mechanical strain produced by the high reverse gate-drain voltage induced vertical electric field may aggravate the tensile strain already present owing to the lattice mismatch between the AlGaN barrier and the GaN layer. Since piezoelectric tensor elements such as d_{11} and d_{22} are zero in GaN and AlN, lateral electric field in the HFETs will not be able to result in normal strain (material expansion/contraction)[46]. In this scenario, beyond a critical gate-drain voltage that corresponds to the critical elastic energy of the AlGaN, the HFET devices begin to degrade abruptly. And lateral electric field was observed to be less relevant for the device degradation. To examine that whether the degradation is exclusively due to the vertical electric field, electric field distribution (both lateral and vertical electric field) was simulated for different bias conditions. Since the electric field is largest at the gate edge at the drain side, the electric field distribution is probed along the line as showed in Figure 26(a). As demonstrated in Figure 26(b), the vertical electric field is the largest on the surface, and will gradually decrease while approaching the GaN buffer. A position was chosen along the dashed line in Figure 26(a) at 5 nm from the surface, and the vertical electric field at that specific position was plotted at various bias points in Figure 27. As we can see, for the same gate-drain bias, the vertical electric field increases much faster for reverse gate bias conditions than that of on-state-high-field bias conditions, and the former is about 10% more than that of the latter case. Thus, if the degradation of HFETs is only

related to the vertical electric field, then reverse-gate-bias stress condition should degrade the devices faster than on-state-high-field stress conditions for the same gate-drain biases.

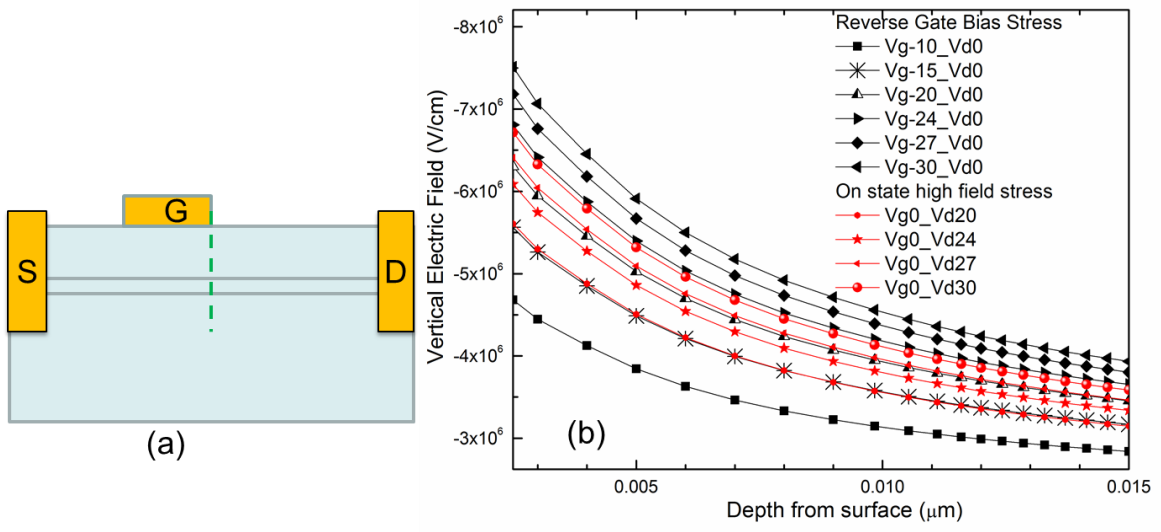

Figure 26 (a) Electric field is probed along the dashed line. (b) Simulation results of vertical electric field for a 2 um gate length HFET device under various bias conditions along the dashed line in figure on the left. For the same gate-drain voltage, the simulated results for the reverse-gate-bias and on-state-high-field bias conditions are presented.

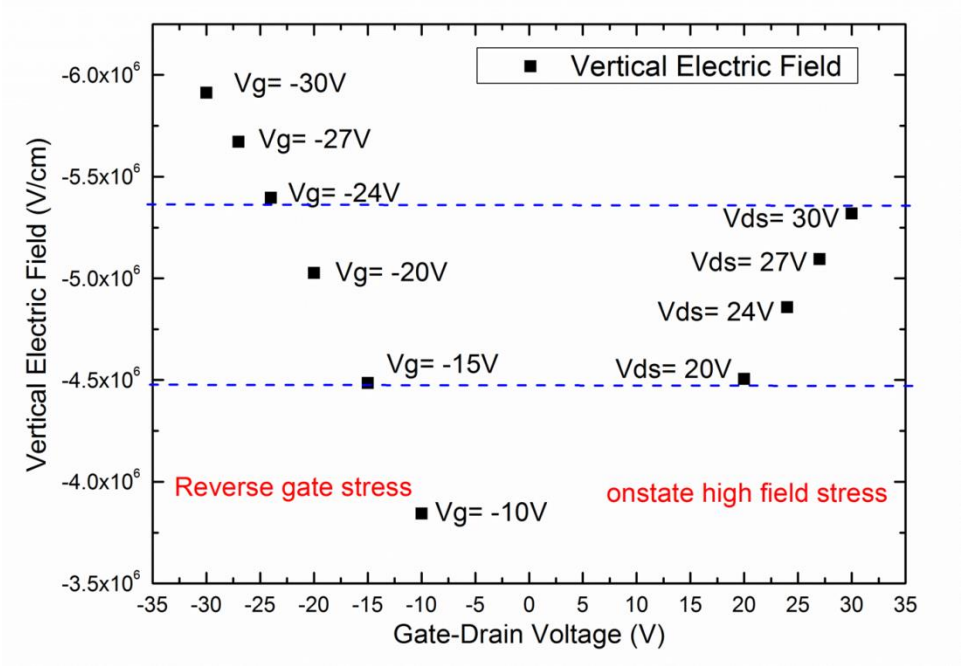

Figure 27 Vertical electric field at 5 nm from the surface at the drain side of the gate edge for various bias points. The ones at the left side are for reverse gate bias stresses at different reverse gate biases. The ones on the right are for on-state-high-field stress at different drain biases.

CHAPTER 6 Degradation of SiNx passivated AlGaN/GaN HFETs

6.1 Introduction to various degradation mechanisms

A popular theory explaining the degradation of AlGaN/GaN HFETs is the so-called inverse piezoelectric effect[9], which is based on the hypothesis that mechanical strain produced by the high reverse gate-drain voltage induced vertical electric field may aggravate the tensile strain already present owing to the lattice mismatch between the AlGaN barrier and the GaN layer. Since piezoelectric tensor elements such as d_{11} and d_{22} are zero in GaN and AlN, lateral electric field in the HFETs believes not be able to result in normal strain (material expansion/contraction)[46]. In this scenario, beyond a critical gate-drain voltage that corresponds to the critical elastic energy of the AlGaN barrier, the HFET devices begin to degrade abruptly. However, permanent degradation was also found to occur even for stresses below that particular critical voltage with sufficiently long stress time for reverse-gate-bias stress, supporting the hypothesis that permanent degradation is due to a defect percolation process[10] at least for reverse-gate-bias stress, where the degradation was characterized by the increase of the gate leakage current. The increase of the gate leakage current was ascribed to the generation of defects in the AlGaN barrier through the inverse piezoelectric effect or large electric field. Other proposed degradation mechanisms include hot-electron-induced trap generation[6], impurity diffusion along the dislocation lines during the early stages of degradation[11], oxidation of the device surface[12], and hot-electron/phonon effects[13], [14]. The proposed degradation mechanism of hot-electron effect was supported by the experimental results that non-Arrhenius degradation of AlGaN/GaN HFETs grown on bulk GaN substrate were

demonstrated[47], where stressing the AlGaN/GaN HFETs at higher temperatures caused lesser degradation compared to stressing AlGaN/GaN HFETs at room temperature. The realization of the importance of hot-phonon effect on the device degradation originates from the careful investigation of the heat transfer from hot-electrons to the heat sink. Hot electrons dissipate heat to longitudinal acoustic (LA) phonons effectively in materials such as Si and GaAs; however, it is not the case for GaN due to the strong electron-phonon coupling. In GaN, the hot-electron has to transfer energy to hot-phonons (LO optical phonon), and then from hot-phonons to LA phonon. And the overall conversion process is going to be limited by the slowest process in the chain. The overall conversion process is schematically demonstrated in Figure 28.

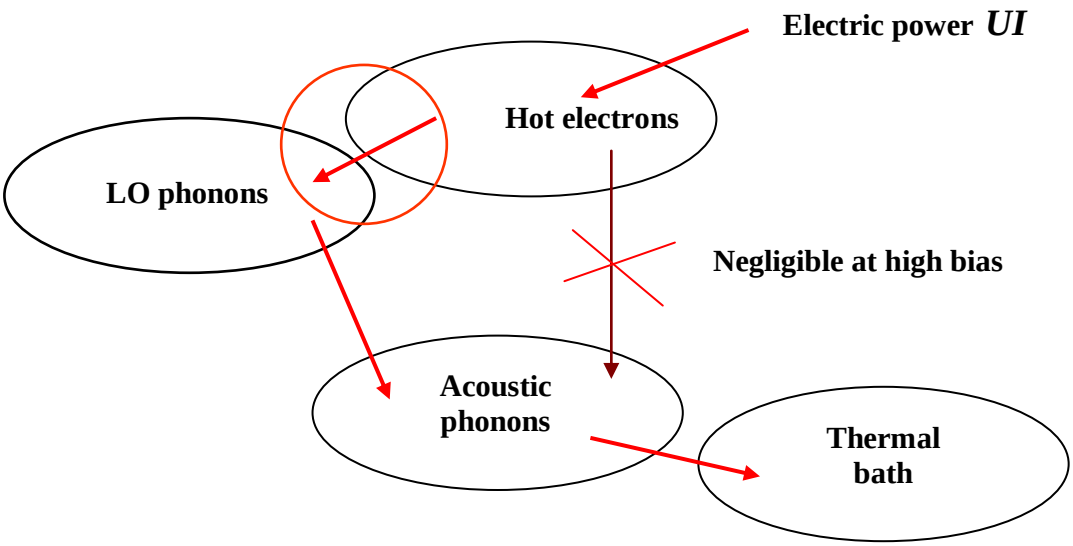

Figure 28 Schematic of the dissipation of heat in GaN at high fields. The only means of transferring energy out of the hot electron/hot phonon subsystem is through the hot phonon decay into acoustic modes. Note that if the hot electron and hot phonon temperatures were equal, no energy would be dissipated.[48]

The non-equilibrium population of hot-phonon originate from the fact that the time associated with the emission of LO phonons is much shorter than the time associated with the decay of LO phonons into LA phonons that have large group velocity, which cause the buildup of low-group velocity LO phonons and cause the buildup of heat locally. The buildup of the local heat can cause defects to form, particularly when some defects are already present. Experiments have demonstrated that degradation rate of InAlN/GaN HFETs has a strong dependence on the decay rate of hot phonons to LA phonons or equivalently the lifetime of the hot phonons[13]. When the lifetime of the hot phonons is small or the hot-phonon can efficiently decay to propagating LA phonons, the degradation rate is small, vice versa. The lifetime of hot-phonons can be tuned by the 3-dimensional (3D) electron density in GaN, and minimum lifetime occurs at a certain 3D carrier density which is set by the plasmon frequency matching that of the LO phonon in GaN[49]. By tuning the 3D electron density in the GaN channel while maintaining the 2DEG density at the hetero-interface through the insertion of a 10% Al composition AlGaN extra channel layer, the LO phonon lifetime can be decreased[50]. This $Al_{0.1}Ga_{0.9}N$/GaN double channel layer can effectively spread the 2DEG profile making the 3D electron density closer to that corresponding to the minimum LO phonon lifetime.

Although many mechanisms were proposed to be responsible for the degradation of AlGaN/GaN HFETs, it should be noticed that the impact of the same mechanism may change under different stress bias conditions. For example, hot electron effect should be directly proportional to the amount of electrons in the channel as well as the energy of the

hot electrons, thus hot electrons should be more important when the channel current is high and the accelerating electric field is high during the stress. Hot-phonon/longitudinal polar optical phonons come from the interaction of hot-electron with the lattice, thus generally speaking hot phonon effect should be strong only when hot-electron effect is strong (Hot-phonon lifetime was demonstrated to be dependent on the 2DEG density in the channel, however, if the hot-electron effect is small, the hot-phonon effect should be small as well). For bias conditions where there is little channel current, the hot-phonon effect should be small as well. For inverse piezoelectric effect, the degradation should be only relates to the vertical electric field presented in the devices, thus devices should degrade faster for reverse-gate-bias stress than that of on-state-high-field stress for the same gate-drain bias during the stresses if only consider degradation caused by inverse-piezoelectric effect. Meneghesso *et. al.* [51] demonstrated that for reverse-gate-bias stress, the degradation in terms of gate leakage has a strong dependence on the stress time and applied gate biases, while the degradation was ascribed to be the hot-electron effect for on-state-high-field stress. However in their results, the degradation rates had a non-monotonic dependence on the gate voltage level, where the maximum degradation rate located at V_{GS}= -0.5*V*. Since the bell shaped degradation had strong correlation to the dependence of the electroluminescence signal on the gate voltage, the degradation mechanism was ascribed to hot electron effect because the electroluminescence signal is generated by hot electrons[52]. However, bell shaped degradation rate was also reported in InAlN/GaN HFETs with the smallest degradation at a certain gate bias which is different to that reported in Ref. [51], and the degradation is ascribed to be hot-phonon effect[13]. In this

chapter we will investigate the degradation phenomena in SiNx passivated AlGaN/GaN HFETs at both on-state-high-field stress conditions (V_{GS}=0V and V_{DS}=20 to 30V) and reverse-gate-bias stress conditions (V_{GS}=-20V to -30V and V_{DS}=0V) to examine the dependence of degradation on different bias conditions as well as propose possible degradation mechanisms.

6.2 Device performance of pristine passivated AlGaN/GaN HFET devices and stress bias conditions

Figure 29 shows a representative 2 μm gate length device from a SiNx passivated $Al_{0.25}Ga_{0.75}N$/GaN with HCl pre-treatment. As we can see, the device performance was improved substantially after SiNx passivation in terms of DC drain current, f_T, and phase noise. The increase of dc drain current is due to the removal of the electrons from the surface states, avoiding the depletion of the 2DEG electrons by the surface electrons. The f_T increased to almost 5GHz, which means a huge reduction of the "virtual gate" or gate extension. The phase noise reached a small value of -100dBc/Hz at 1Hz, which is about the same level as that of high-temperature-on-state-stressed un-passivated AlGaN/GaN HFETs under relaxed condition as showed in Figure 13(c). Overall, the improvement of the device performance is quite substantial after passivation, and we can conclude that maintaining a good surface property is crucial to obtain a small phase noise because the phase noise decreased by 20 dBc/Hz after passivation.

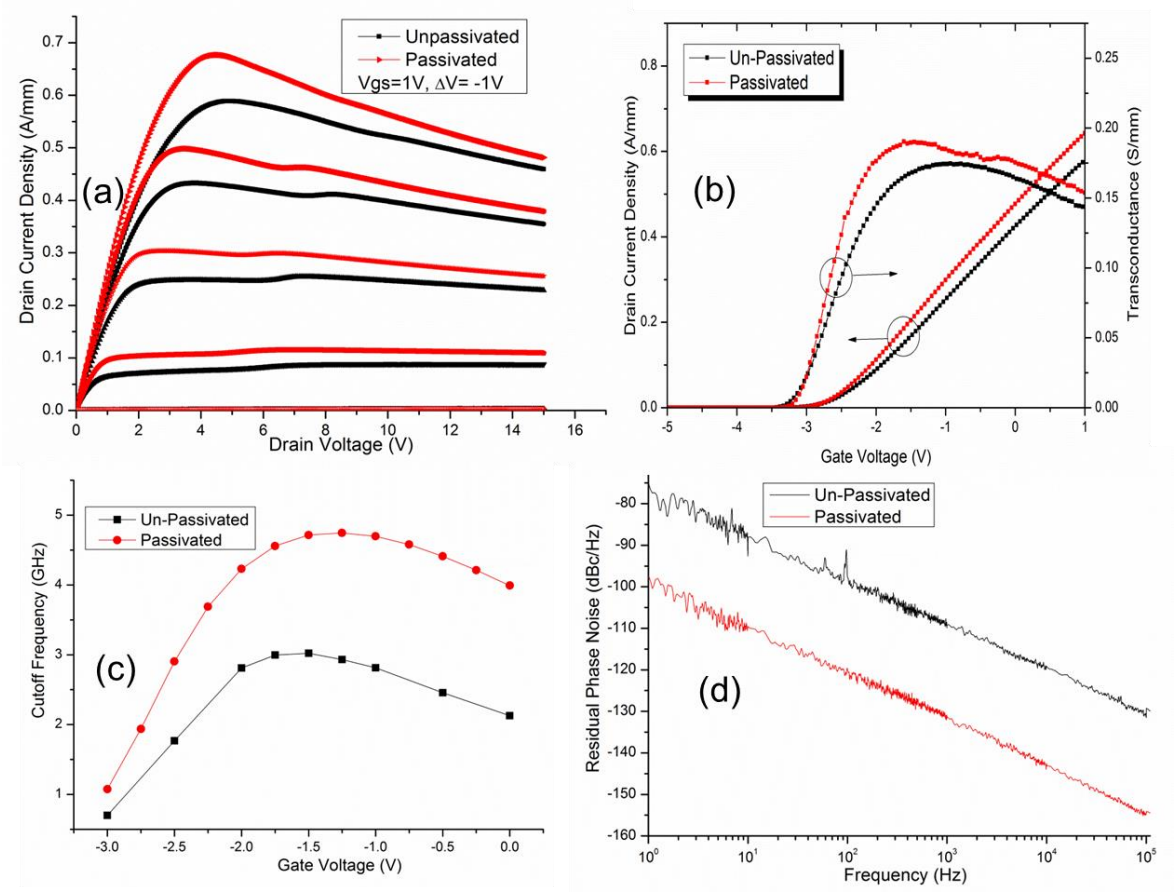

Figure 29 Electrical performance of a representative $Al_{0.25}Ga_{0.75}N$/GaN HFET device before and after SiNx passivation with HCl pre-treatment. (a) IV family curve measured from V_{GS}=+1*V* to -4*V* with step size of -1*V*; (b) transfer characteristic measured at V_{DS}=6*V*; (c) current gain cutoff frequency (f_T) measured at V_{DS}=6*V*; (d) phase noise measured at V_{GS}=0*V* and V_{DS}=6*V*;

Two sets of stress conditions were used to test degradation of HFETs. The on-state-high-field stress conditions were V_{GS}=0, and V_{DS}=20, 24, 27, or 30*V*. The reverse-gate-bias stress conditions were V_{GS} = -10, -15, -20, -24, -27 or -30*V* and V_{DS} =0*V*. Devices were stressed for 10 hours in air at external base plate temperatures up to 150 °C. An ensemble of HFETs devices on the same wafer was chosen for each stress condition, and all showed similar behavior after stress. Therefore, results from representative devices are presented

here. The phase noise spectra were measured at a bias condition of V_{GS} =0V & V_{DS} =6V before and after stress.

6.3 Degradation under on-state-high-field and reverse-gate-bias stress

Figure 30 shows the phase noise spectra for devices stressed under on-state-high-field at different drain biases. The noise spectrum for the pristine device is representative of typical *1/f* noise that we observe. As can be clearly noted, the devices stressed under the on-state-high-field stress with V_{GS} = 0*V* and V_{DS} =20*V* started to exhibit an increase in phase noise (no noticeable change was observed for smaller drain biases) and the noise level increased further consistently for higher stress drain biases of V_{DS} = 24*V*, 27*V*, and 30*V*. The change occurred in the form of a frequency independent increase of 1/f noise plus a generation—recombination (G-R) peak in the frequency range of 10^3 to 10^5 Hz. The appearance of the G-R peak can be attributed to the generation of traps after stress[23]. The drain current also showed significant degradation as the drain bias for the on-state-high-field stress was increased (see inset of Figure 30). After stressed at V_{DS} =0*V* and V_{DS} =30*V*, the drain current at bias condition of V_{GS} =1*V* and V_{DS} =4*V* decreased to nearly 50% of that of pristine device under the same bias condition.

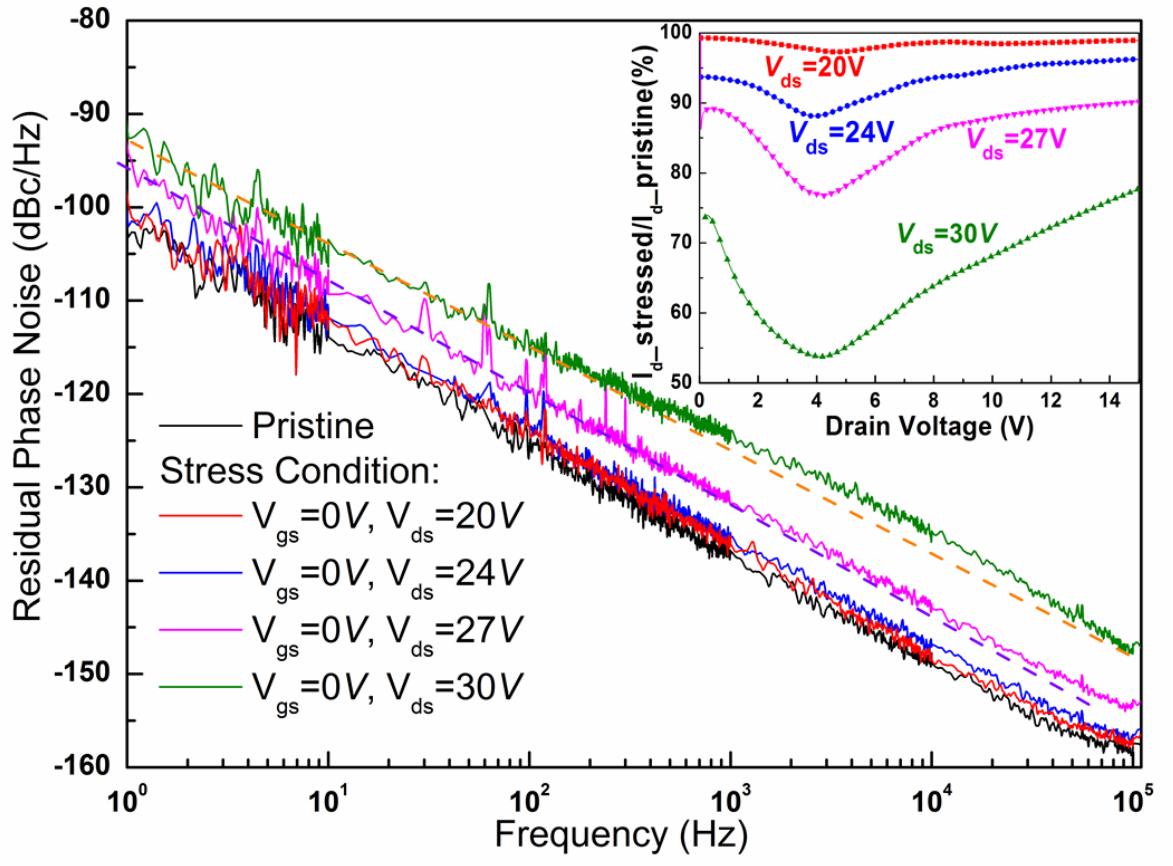

Figure 30 Phase noise spectra measured at V_{GS} =0*V* and V_{DS} =6*V* for pristine devices and devices stressed under on-state-high-field at various drain biases. The inset shows the degradation of drain current after on-state-high-field stress characterized by the ratio of drain current for stressed devices to that in pristine devices (The drain currents were measured under V_{GS} =1*V* at various drain biases). The dashed lines are used as guides for the 1/f noise and to reveal the G-R peaks in the high frequency range.

The phase noise spectra after reverse-gate-bias stress are shown in Figure 31. For devices stressed under reverse-gate-biases of V_{GS} = -10*V* and -15*V*, the noise spectra as well as drain current (not shown) did not indicate any change. However, when the reverse gate bias was increased to V_{GS} = -20*V*, a weak G-R type peak appeared near 10^3 Hz after stress. The intensity and width of this G-R peak increased for devices stressed at larger $|V_{GS}|$, *i.e.* higher vertical electric field. For sufficiently large $|V_{GS}|$, *i.e.* $V_{GS} = -30V$, we suggest the

presence of several G-R peaks corresponding to different time-constants superimposed on each other which leads to frequency-independent increase of 1/f noise.

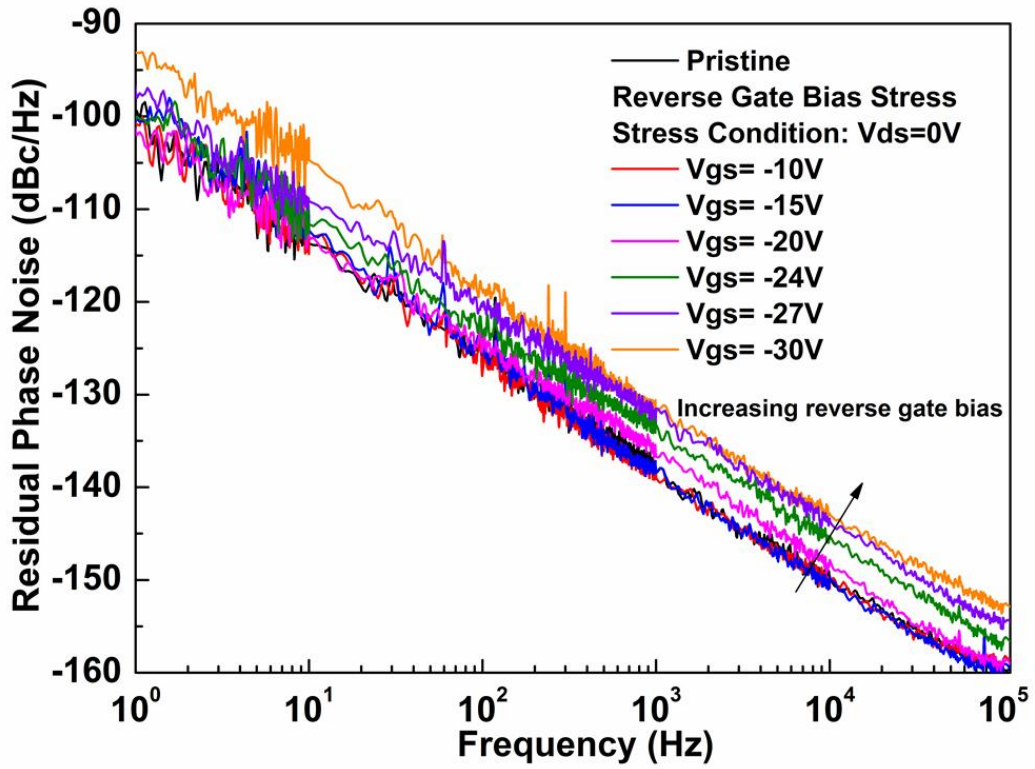

Figure 31 Phase noise spectra measured at V_{GS} =0V and V_{DS} =6V for pristine devices and devices stressed under different reverse-gate-biases.

The above results are consistent with other reports which suggest that the degradation was induced by the applied electric field [53], [54], for both on-state-high-field and reverse-gate-bias stress conditions. Electric field simulations using Silvaco Atlas with field dependent mobility model showed that vertical electric field at the gate edge of the drain side induced by reverse-gate-bias stress is ~10% higher than that induced by on-state-high-field stress for the same applied gate-drain voltage as already demonstrated in Figure 27. However, this does not necessarily mean that the reverse-gate-bias stress will inevitably

cause higher degradation rate than on-state-high-field stress. For the same gate-drain voltages applied during the reverse-gate-bias and on-state-high-field stress, the role of the applied bias can be significantly different in terms of voltage induced lateral electric field. For the case of on-state-high-field stress, the high source-drain voltage can induce a huge amount of hot electrons in the channel by the large lateral electric field, while the effect of hot-electrons in reverse-gate-bias stress should be much smaller due to the small gate leakage current. Interaction of the huge amount of hot electrons in the channel with the lattice induces self-heating (equilibrium excess acoustic phonons) and hot phonon (non-equilibrium optical phonon) effects[14], [55]. Comparing the noise spectra in Figure 30 and Figure 31, we can clearly see that the degradation behavior is quite different. The degradation under the reverse-gate-bias stress is characterized by a gradual increase of trap(s) intensities, while the on-state-high-field stress is characterized by a nearly frequency-independent increase of phase noise. Thus, the degradation mechanism(s) associated with the on-state-high-field stress is not simply due to the high electric field, but to the lateral electric field induced hot-electron, hot phonon and self-heating effects in aggregate as demonstrated in the degradation of InAlN/GaN based HFETs[14] . And further evidence comes from the gate leakage current ratios of stressed to pristine devices under these two different stress types as demonstrated in Figure 32, where larger gate leakage current ratios correspond to larger gate-drain stress voltages for each stress type. For reverse-gate-bias stress under $|V_{GS}|$=10 and 15*V*, the gate-leakage currents showed a small (2-4 times) increase, with no corresponding G-R peak in Figure 31. For reverse-gate-

bias stress under $|V_{GS}| \geq$ 20V, the gate leakage current showed a large (50-200 times) increases and a G-R peak emerged in the noise spectra. The increase of gate leakage current for reverse-gate-bias stress under $|V_{GS}| \geq$ 20V should be due to the trap generation in the AlGaN barrier which can form a conductive path [10]. In retrospect, the increasing amount of accelerated gate leakage electrons under higher stress electric field may further promote the trap generation in the barrier. For on-state-high-field stress, the gate leakage currents increase gradually from ~2 to ~30 times for V_{DS} from 20*V* to 30*V*. If the increase of the gate leakage current and noise after on-state-high-field stress is as well due to the trap generation in the barrier, then on-state-high-field stress should generate much lower concentration of traps in the barrier, and therefore, a small increase of noise, which is not the case as shown in Figure 30. Thus, factor(s) other than trap generation in AlGaN/GaN barrier due to vertical electric field should be in play.

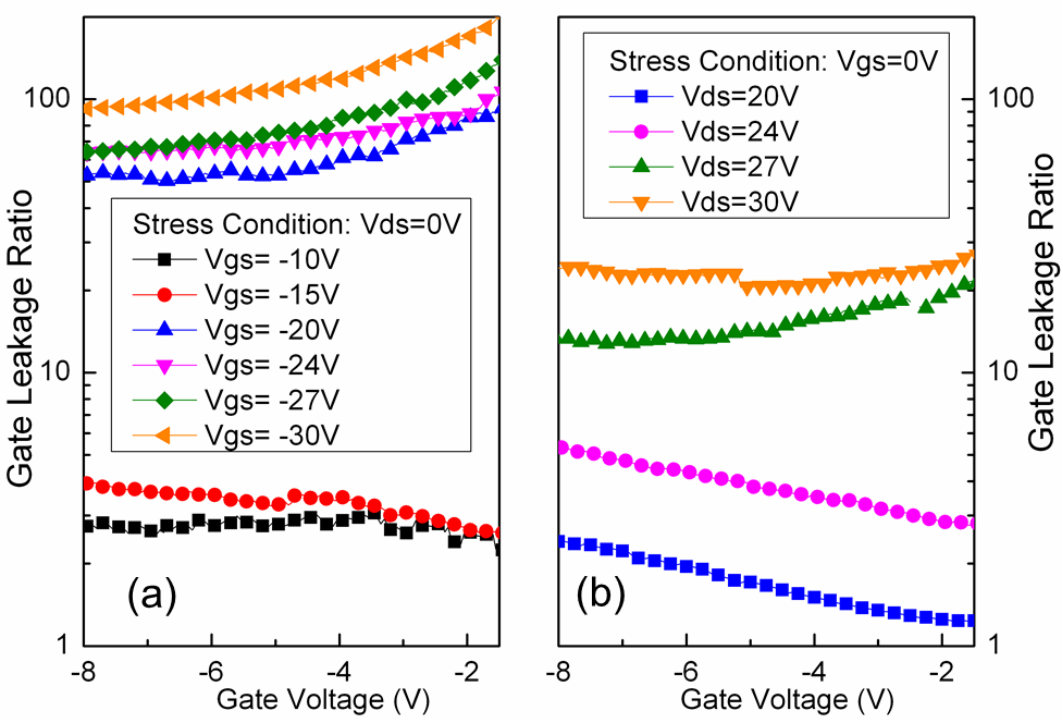

Figure 32 Gate leakage current ratios of stressed devices to pristine devices for (a) reverse-gate-bias stress and (b) on-state-high-field stress.

The effects of the base plate temperatures on the device degradation for the on-state-high-field stress were investigated and the results are plotted in Figure 33(a). A G-R peak emerges at between ~10^3 – 10^4 Hz for the on-state-high-field stress with V_{DS} =20V at 100 ^oC and its intensity increases further for a higher stress temperature of 150 ^oC. The effects of the base plate temperature on the device degradation for the reverse-gate-bias stress were also examined and the G-R peak intensity was also observed to increase with temperature as shown in Figure 33(b). Using a thermal resistance of approximately 27.3 $^oC\cdot$mm/W[56], the temperature of devices stressed at V_{GS} =0V & V_{DS}=20V and at 150 ^oC base plate temperature is about 40 ^oC higher than that of devices stressed at V_{GS} =0V & V_{DS}=30V and at room temperature. However, a much larger degradation in terms of phase

noise was observed for devices stressed at V_{GS} =0V & V_{DS}=30V at room temperature, which means the heat (equilibrium excess acoustic phonons) is excluded as the key factor causing the nearly frequency-independent increase of the noise when large drain bias was applied during the on-state-high-field stress. Thus, the degradation should be mainly due to the non-equilibrium hot-electron and hot phonon (non-equilibrium optical phonon) effects[13], [14]. It should be noted that the equilibrium excess acoustic phonons (temperature) increased the number of traps for both on-state-high-field and reverse-gate-bias stress as demonstrated in Figure 33. This may be a result of higher temperature causing stronger lattice vibration, and hence promoting atomic displacements, which inevitably will cause more defects, and thus increase the G-R peak intensity.

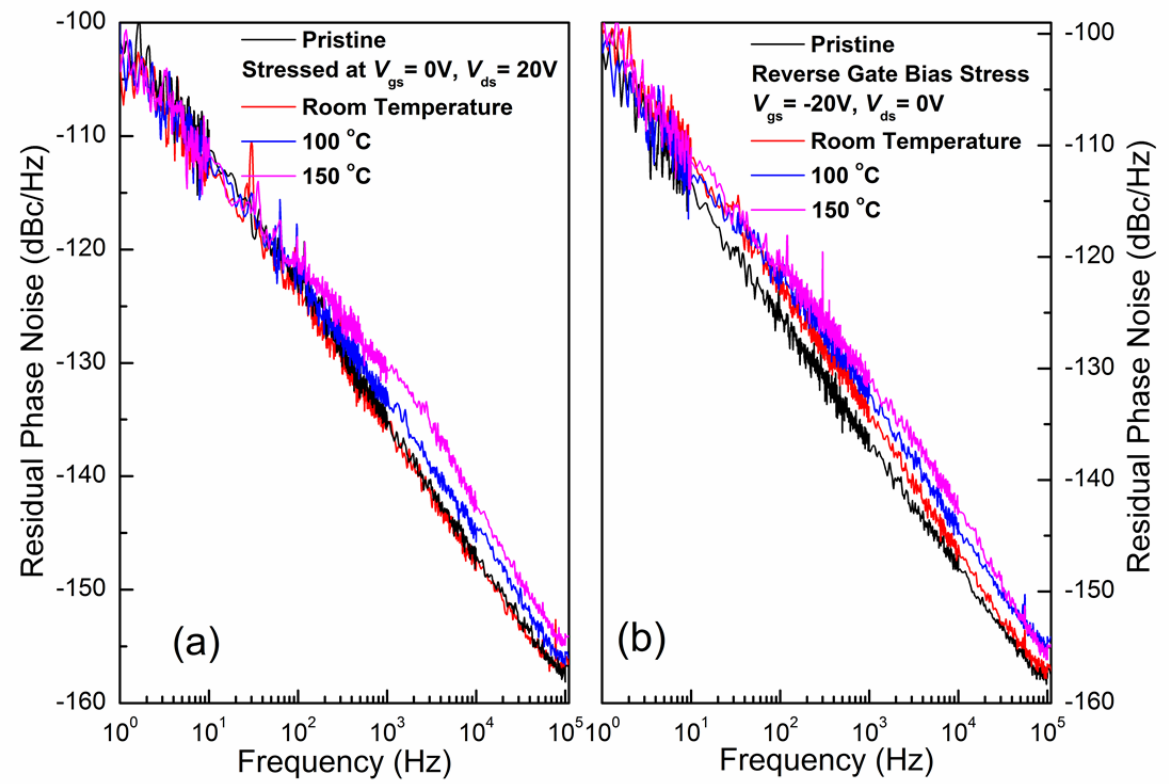

Figure 33 (a) Phase noise spectra measured at V_{GS} =0V and V_{DS}=6V for pristine devices and devices stressed under on-state-high-field at V_{GS} =0V & V_{DS}=20V at room temperature, 100 °C and 150 °C; (b) phase noise spectra measured at V_{GS} =0V and V_{DS}=6V for pristine devices and devices stressed under reverse-gate-bias at V_{GS} = -20V & V_{DS}=0V at room temperature, 100 °C and 150 °C.

The hot-electron and hot-phonon effects can be further examined by varying the drain-source voltage during the on-state-high-field stress. Gate-voltage dependent current measurements in the linear operation region of HFETs were conducted to extract the channel resistance R_{ch} as well as the sum of source and drain resistances (R_s+R_d). For the case of on-state-high-field stress at V_{DS}=30V, more than 90% of the increase of source-drain resistance after stress was shown to be due to the increase of R_{ch}, *i.e.* due to the channel degradation. This correlates well with the findings from phase noise

measurements, where the spectra after stress were characterized by a frequency independent increase of noise with a small G-R peak. It should be noted that the drain current did not show any recovery after weeks in ambient environment, and current collapse was not observed during repeated current measurements. Thus, it can be concluded that a permanent degradation has occurred instead of temporary trapping unless the trapped electrons have very long time-constants, in which case the process can be equivalently regarded as permanent defect/trap generation. A frequency independent increase of noise can be due to mobility fluctuation or number fluctuations from continuous trap spectrum (such as the case of reverse-gate-bias-stress at V_{GS} = -30*V*), or both processes acting together [23]. The drain current and phase noise degradation observed in aggregate as mentioned above suggests that the frequency independent increase of noise should most likely be ascribed to the mobility fluctuations due to the channel degradation, similar to what has been reported in InAlN/GaN HFETs[14]. Similar results were also demonstrated that the permanent degradation of drain current occurs only with the combination of the following two factors: 1) high junction temperature and 2) high electric field [57]. Although no in-depth explanation was given why these two factors are needed, it is consistent with our proposed degradation mechanism of hot-electron and hot-phonon effects.

In conclusion, we showed that the degradation is strongly correlated with both the applied electric field and external base plate temperature. The external base plate temperature was shown to promote trap generation for both the reverse-gate-bias and on-state-high-field

stress, while the role of electric field is different for the two stress conditions. Simulation of electric field intensity across the device together with experimental results suggest that the hot-electron/hot-phonon effects induced by the accelerating lateral electric field are dominant in device degradation under on-state-high-field stress, while degradation under reverse-gate-bias stress is purely due to the high electric field in conjunction with increased gate leakage.

CHAPTER 7 InAlN/GaN based HFETs

7.1 Introduction

Due to the large sheet carrier concentration in the channel, thus the large channel current, InAlN/GaN based HFETs are strong candidate for next generation high-power and high-frequency amplifiers [1][15]. Devices performance reported by different groups have demonstrated 2.3 A/mm current density [18], current gain cutoff frequency (f_T) of 300 GHz [58] and 2.9 W/mm output power density at 18 GHz [19]. The motivation to develop InAlN/GaN based HFETs is because large polarization charge can be induced at the InAlN/GaN interface while InAlN can be grown lattice matched to GaN at indium composition of around 17.5%. Although there is no polarization charge induced by piezoelectric effect for a lattice-matched heterostructure, the large spontaneous polarization charge can induce a sheet carrier concentration of about $(1.5\pm0.1)\times10^{13}$ cm^{-2}, which is much larger than that induced by $Al_{0.25}Ga_{0.75}N$/GaN HFETs which a $\sim0.8\times10^{13}$ cm^{-2} sheet carrier concentration will be induced [41]. Even larger sheet carrier concentration can be induced if using a larger Al composition in AlGaN/GaN HFETs; however, a large Al composition means a large lattice-mismatch between AlGaN and GaN, which will pose a serious reliability problem. And it's also more difficult to have good ohmic contact on high Al composition AlGaN layer.

Theoretically, lattice match condition occurs at an indium composition of around 17%~18%[41], where precise value for the indium composition is difficult to determine.

Gačević *et al.* [59] reported an indium fluctuation of around ±1.2% for a 60 nm thick InAlN layers with nominal indium composition of 17% grown by plasma-assisted molecular beam epitaxy, where the composition fluctuation was assessed by electron energy loss spectroscopy with sub-nanometric spatial resolution. Lorenz *et al.*[60] used Rutherford Backscattering/Channeling (RBS/C) and XRD to investigate the strain state of 100nm MOCVD grown InAlN/GaN structures with different indium composition on sapphire substrate, and a 17.1(9)% indium composition has been determined to be the lattice-match condition. While in reference [61], InAlN layers grown under high growth rates are separated into bi-layer structures with two different indium compositions except for samples with indium composition at 18%. Although the lattice-match composition is 17% according to Vegards' law, the practical value is yet quite clear especially if different substrates are used. In this section, we will examine the reliability of the InAlN/GaN HFETs by electrical stress for indium compositions around the nominal lattice match condition of 17%~18%.

7.2 Lattice-match condition for InAlN/GaN HFETs: Reliability Perspective

Four InAlN/GaN wafers with indium composition of 15.7% (device A), 17.5% (device B), 18.5% (device C) and 20.0% (device D) were grown under the following procedures: The $In_xAl_{1-x}N$/GaN HFET structures were grown by metalorganic chemical vapor deposition (MOCVD) on *c*-plane sapphire substrates. The structures are comprised of a 2-μm-thick undoped GaN layer followed by a 1nm-thick AlN spacer, a 20nm-thick unintentionally doped $In_xAl_{1-x}N$ (x=15.7%, 17.5%, 18.5%, 20.0%) barrier, and a 2 nm-thick GaN cap layer. The source and drain contacts were formed using standard photolithography and Ti/Al/Ni/Au (30/100/40/50 nm-thick) metal stacks annealed at 800°C. Mesa isolation was performed in a SAMCO inductively coupled plasma (ICP) system using a Cl-based chemistry. Gate electrodes were formed by deposition of Ni/Au (30/50 nm-thick). The gate length, the gate width, and the source-drain spacing are L_G=2.0 μm, W_G=90 μm, and L_{SD}= 7 μm, respectively. The performances for the four devices are listed in Table 2. The band structures for a theoretical lattice-matched 17% InAlN/GaN HFETs with AlN spacer layer is presented in Figure 34. Noted that the much larger pinch-off voltage (-8V compared to ~ -4V in $Al_{0.25}Ga_{0.75}N$/GaN HFETs) due to the large positive polarization charge at the hetero-interface.

Table 2 Device performances for representative pristine devices under the on-state-high-field stress. The $f_{T,\,max}$ is the maximum current gain cutoff frequencies measured at V_{DS}=6*V* and various gate biases.

InAlN/GaN	$I_{D,max}$(A/mm)	I_{Pulse}/I_{DC} at 1ms (%)	Noise at 1 Hz (dBc/Hz)	$f_{T,max}$ (GHz)
A (15.7%)	0.95	105%	-100	5.5
B (17.5%)	0.91	80%	-82	0.75

C (18.5%)	0.63	70%	-81	2.5
D (20.0%)	0.42	4%	-78	1.6

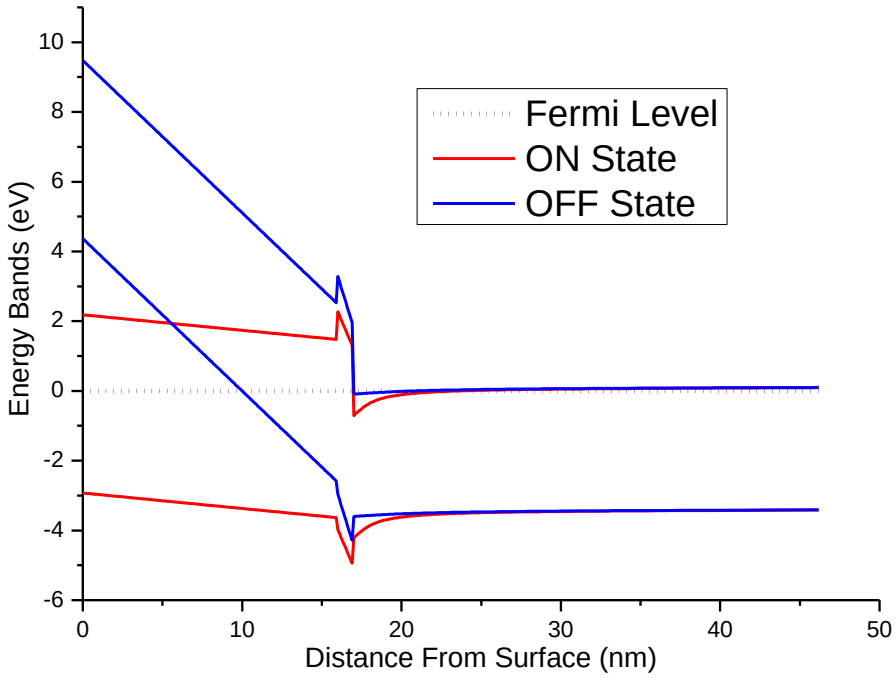

Figure 34 Band structure of an $In_{0.17}Al_{0.83}N$/AlN/GaN HFET device under on-state (V_{GS}=0V) and off-state (V_{GS}=-8V), respectively. Note that the pinch-off voltage is much larger than we presented in Figure 6 for AlGaN/GaN HFETs.

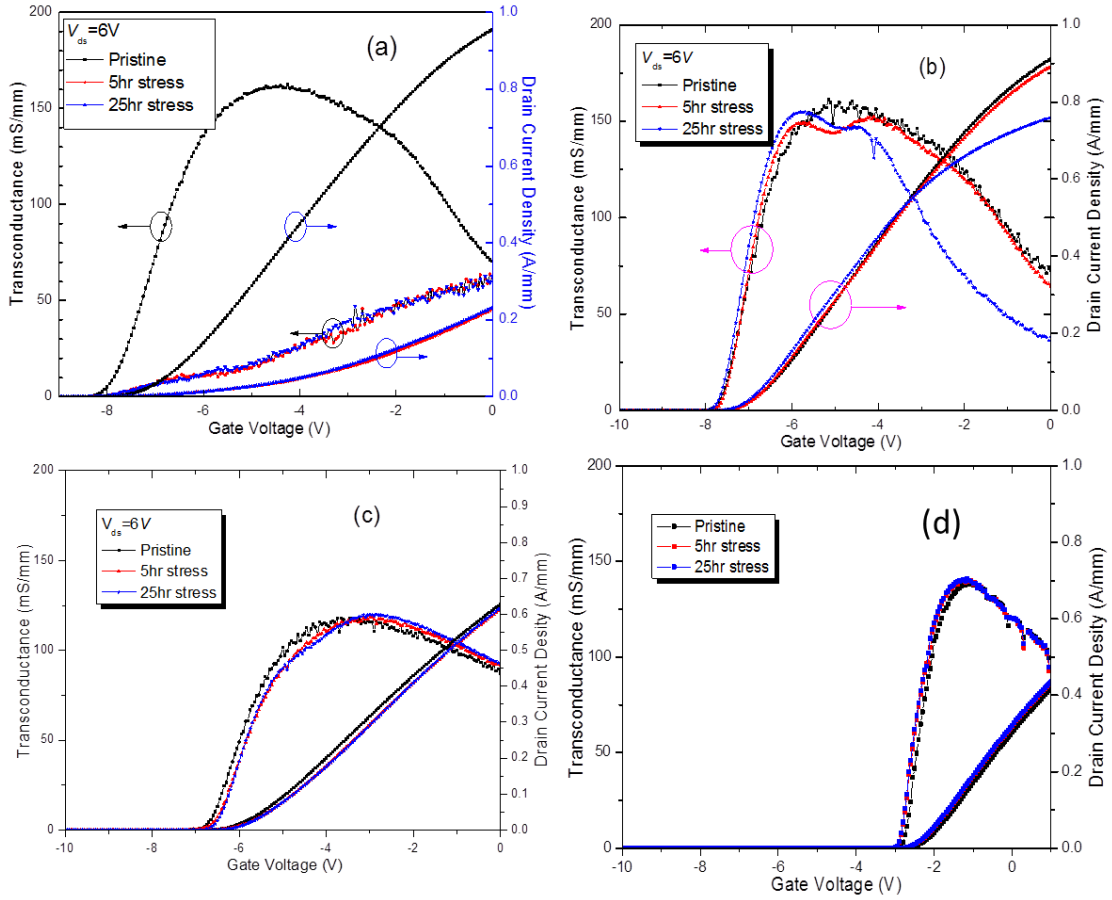

Figure 35 Transconductance (g_m) and drain current measured under V_{DS}=6*V* at various gate biases for pristine, 5 hr & 25hr stressed devices for InAlN/GaN HFETs at an indium composition of (a) 15.7%; (b)17.5%; (c) 18.5%; (d) 20.0%. The electrical stress condition was V_{GS} =0*V* & V_{DS}=20*V*.

Figure 35 shows the transconductance and drain current for each of the four InAlN/GaN devices with different indium compositions under pristine, 5hr, and 25hr stressed conditions. The devices are stressed under bias condition of V_{GS} =0*V* & V_{DS}=20*V*. For pristine devices, devices A, B, C, and D have a pinch-off voltage around -8.2*V*, -8*V*, -7*V*, and -3*V*, respectively. And the drain currents at V_{GS} =0*V* & V_{DS} =6*V* are ~0.95 *A*/*mm*, ~0.9 *A*/*mm*, ~0.62 *A*/*mm*, and ~0.42 *A*/*mm*, respectively, for devices A, B, C, and D. The magnitude of the drain currents are consistent with the 2DEG density in the channel as we

stated before, where a smaller indium composition will induce a higher 2DEG density due to the piezoelectric charge caused by the lattice-mismatch. Upon 5hr stress, the device A showed a very large degradation of drain current, where the drain current decreased to ~30% of a pristine device as demonstrated in Figure 35(a). A further 20hr stress didn't change much of the drain current and transconductance. For device B, the drain current showed little change after 5hr stress, and reduced to ~83% of a pristine device with another 20hr stress as demonstrated in Figure 35(b). The degradation of the transconductance for this device B after 25hr stress mostly happened at high gate bias or open channel condition, which indicates that the degradation most likely happened at the gate-drain access region probably due to electron trapping[39]. The electrical performance of device C and D are much more stable and shows little change of both drain current and transconductance after stress.

The results for the current-gain cutoff frequency f_T are presented in Figure 36 for the four devices. Device A showed the highest f_T for a pristine condition, but showed severe f_T degradation after 5hr stress, which is consistent with the drain current degradation. While for device B, the f_T first showed a drastically increase after 5 hr stress, and decreased after further 20hr stress. And the decrease of f_T mostly happened at the open-channel gate bias conditions, which is consistent with the drain current degradation. More interestingly, the f_T showed continuous increase with the stress time for device C. Device D showed very small f_T for pristine devices, and it became even smaller after stress.

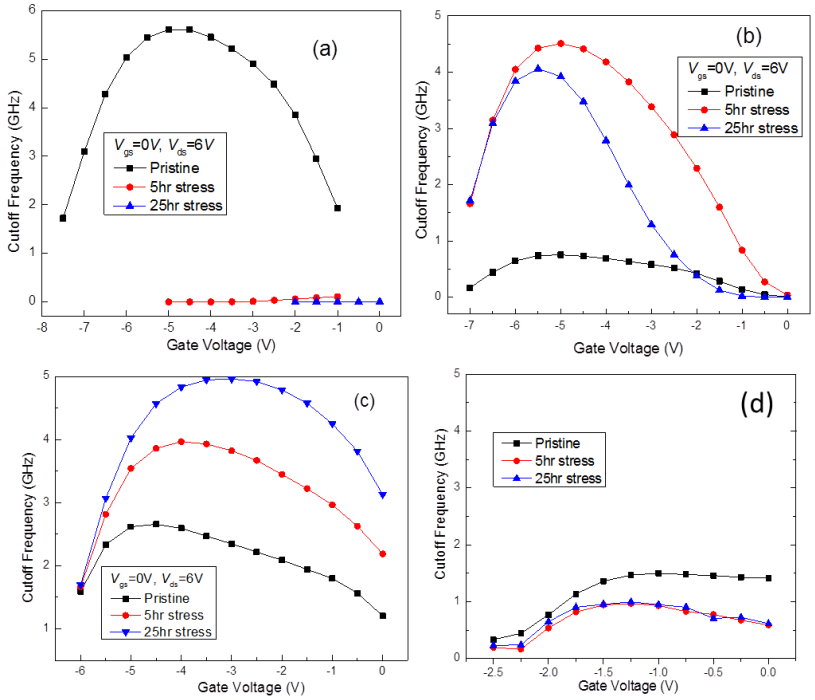

Figure 36 Current-gain cutoff frequency (f_T) measured at V_{DS} =6*V* and various gate biases for pristine, 5 hr & 25hr stressed devices for InAlN/GaN HFETs at indium composition of (a) 15.7%; (b)17.5%; (c) 18.5%; (d)20.0%.

The corresponding noise spectra are presented in Figure 37. The noise of device A showed continuous increase, which is consistent with the continuous degradation of DC and microwave performance. Device B first showed a large decrease of noise, and then an increase, although the final noise level is still lower than that of the pristine condition. Device C showed continuous decrease of noise, and the noise level didn't change much for device D. As we can see, the drain current shows universal decrease after stress. While the change of noise level, either increase or decrease, are in the same pattern as that of the change of cutoff frequencies f_T as well as the gate lag as demonstrated in Figure 38, except for device D whose electrical properties doesn't change much after stress. The decrease of the noise for device B and C are similar to that of AlGaN/GaN HFETs stressed at room

temperature, where the reduction of the noise is ascribed to the change of shallow donor-like traps. In order to elucidate the underlying mechanism, extraction of small-signal circuit parameters were used for device C.

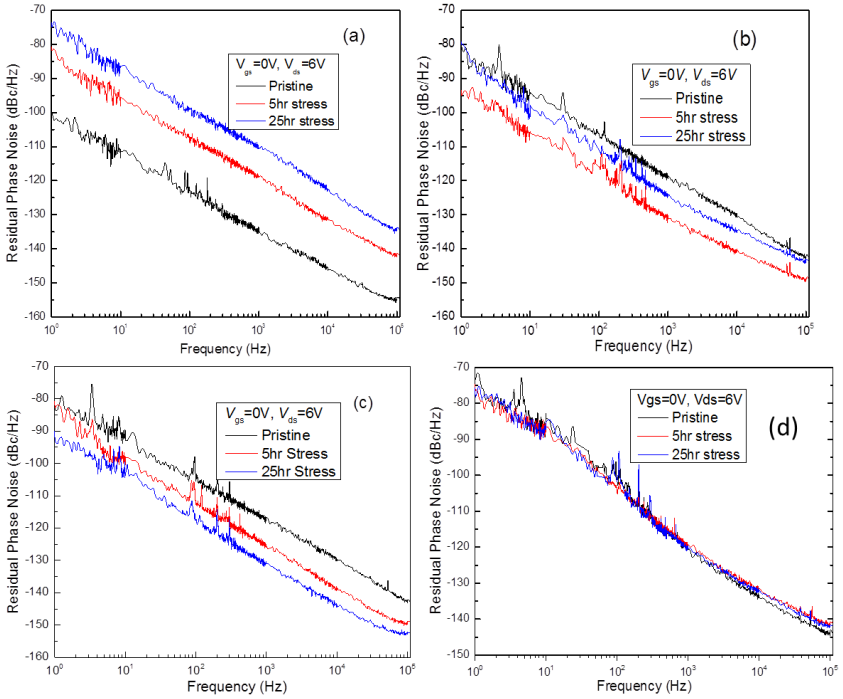

Figure 37 Noise spectra measured at V_{GS} = 0V & V_{DS} = 6V for pristine, 5 hr & 25hr stressed devices for InAlN/GaN HFETs at an indium composition of (a) 15.7%; (b)17.5%; (c) 18.5%; (d)20.0%.

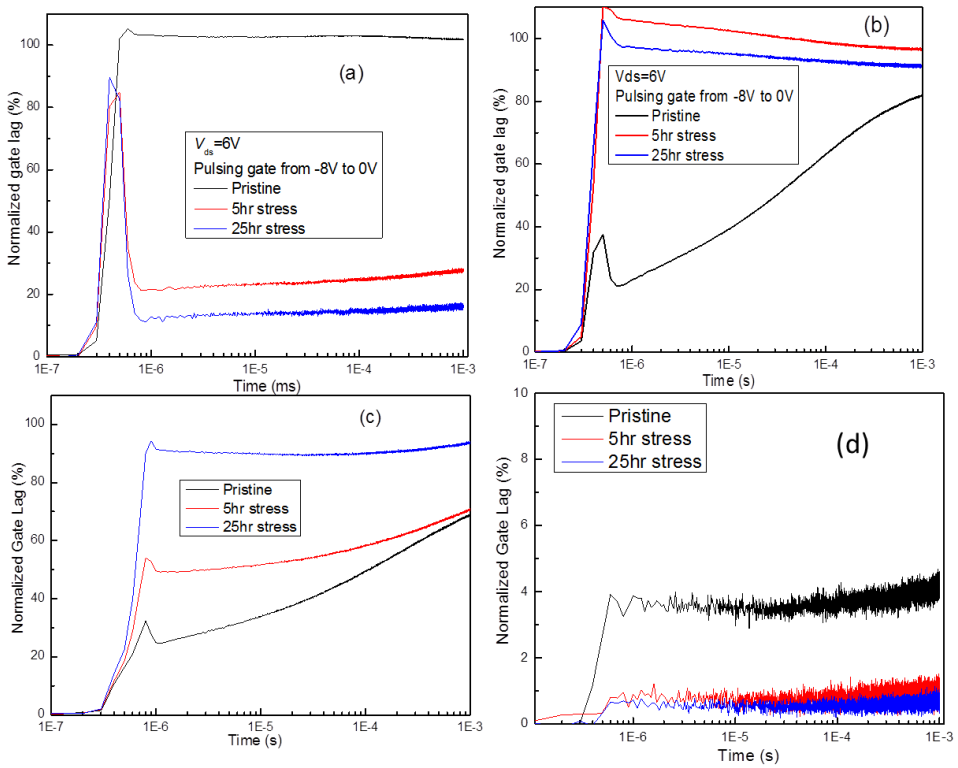

Figure 38 Gate lag measured under V_{DS}=6V, and pulse V_{GS} from -8V to 0V for pristine, 5 hr & 25hr stressed devices for (a) Device A, 15.7% indium; (b) Device B, 17.5% indium; (c) Device C, 18.5% indium; (d)Device D, 20.0% indium. The transient drain current is normalized to its corresponding dc value and presented in the form of percentage. A higher percentage means a smaller lagging effect.

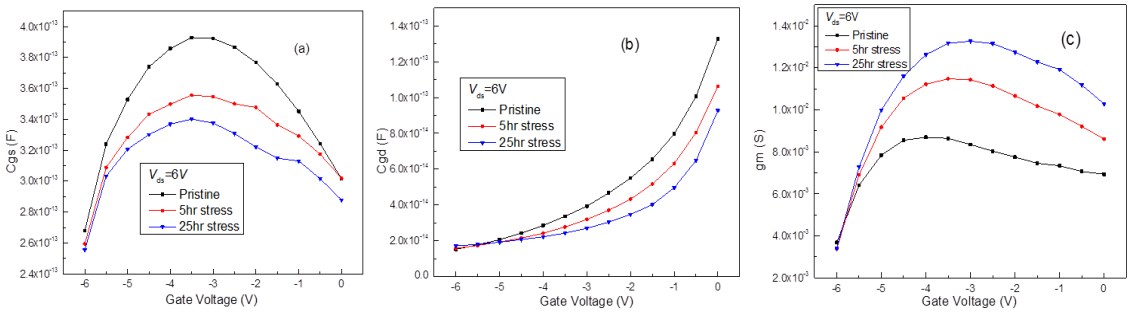

Figure 39 The extracted small-signal parameters at V_{GS} =0V & V_{DS}=6V for a typical device C. (a) gate-source capacitance C_{GS}; (b) gate-drain capacitance C_{GD}; and (c) microwave transconductance g_m extrapolated to zero frequency.

The f_T showed continuous increase with the stress time, almost doubling after the 25hr stress as shown in Figure 36(c). Considering the gate length (L_G) of the HFET devices is 2

μm, a product of $f_T \cdot L_G >= 10 GHz \cdot \mu m$ is reached after stress, which means that the stressed device C showed very good microwave properties. The results of the extracted small-signal parameters are presented in Figure 39. As can be inferred from Equation 7, the increase of f_T after each stress can be attributed to the increase of small-signal transconductance, g_m, and reduction of C_{GS} and C_{GD}. The decrease of C_{GS} and C_{GD} can be ascribed to the reduction of the gate extension or the so-called "virtual gate"[34], where a reduced gate extension reduced the volume of the depletion region underneath the gate and hence reduced the space charge Q in Equation 8, and Equation 9, which reduced both C_{GS} and C_{GD}. When the virtual gate diminished completely, the effective gate length became the physical gate length. The gate extension or "virtual gate" can be as long as the physical metal gate length as has been reported [62]. Thus, a doubled f_T after stress is quite reasonable. The increase of g_m after stress (Figure 39) can be due to the increase of the effective velocity of electrons in the 2DEG [28] as well as a shortened travel distance for the electrons due to the diminishing of the gate extension, which again was due to surface effect.

Table 3 DC and pulse performance of InAlN/GaN HFET devices with different indium composition before and after 25hr on-state-high-field stress.

InAlN/GaN	$I_{D,max}$(A/mm) Pristine	$I_{D,max}$(A/mm) 25hr stressed	I_{Pulse}/I_{DC} at 1ms (%) pristine	I_{Pulse}/I_{DC} at 1ms (%) 25hr stressed
A (15.7%)	0.95	0.30	105	15
B (17.5%)	0.91	0.75	80	90
C (18.5%)	0.63	0.62	70	95

D (20.0%)	0.42	0.50	4	0.8

Table 4 Microwave and noise performance of InAlN/GaN HFET devices with different indium composition before and after 25hr on-state-high-field stress.

InAlN/GaN	$f_{T,max}$ (GHz) Pristine	$f_{T,max}$ (GHz) 25hr stress	Noise at 1 Hz (dBc/Hz) pristine	Noise at 1 Hz (dBc/Hz) 25hr stress
A (15.7%)	5.5	0.1	-100	-75
B (17.5%)	0.75	4.0	-82	-84
C (18.5%)	2.5	5.0	-81	-92
D (20.0%)	1.6	0.8	-78	-78

By comparing the degradation performance of four InAlN/GaN HFETs with different but close to the theoretical lattice-match indium compositions as demonstrated in Table 3and Table 4, we can see that the devices with indium composition of 18.5% and 20.0% are stable in terms of stability of drain current. Putting aside the $In_{0.2}Al_{0.8}N$/GaN HFETs due to the much lower drain current, the ones with 18.5% indium composition are the most stable HFETs. Although its microwave and noise properties changes tremendously, it has been demonstrated that the change most likely is a surface effect, which can be removed by proper surface treatment, like surface passivation. Regarding devices with 17.5% indium composition, the initial improvement in terms of noise and microwave performance should also come from the diminishing of the gate extension, while further degradation causes serious drain current, cutoff frequency f_T, and noise performance degradation. Thus, the

reliability of the devices with 17.5% indium composition is not as stable as devices with 18.5% indium composition. The devices with 15.7% indium composition are the least stable one, which have severe degradation just after 5hr electrical stress. Thus, further study should be conducted to investigate the underlying mechanism(s) contributing to the degradations. Although devices with 20.0% indium composition showed good reliability in terms of drain current, the drain current are much smaller than other indium compositions because the small 2DEG density in the channel. Thus this composition is not quite useful for the purpose of high power amplifier. Although $In_{0.185}Al_{0.815}N$/GaN HFETs showed smaller drain current compared to InAlN/GaN HFETs with 15.7% and 17.5% indium composition, it demonstrated much better reliability, which is vital important for semiconductor devices. And it can be concluded that the real lattice-match indium composition in terms of device reliability should be 18.5%.

7.3 Degradation study of $In_{0.157}Al_{0.843}N$/GaN HFETs under four bias point stresses

Results from our lab have shown that hot-phonon effects can be a very important degradation mechanism in InAlN/GaN based HFETs due to its much larger 2DEG density in the channel[13], [63]. However, other effects contributing to the degradation of AlGaN/GaN HFETs might also be in play in InAlN/GaN HFETs, especially when different operation bias conditions are used. A four bias point stress has previously been used to investigate the degradation contributions from different effects in AlGaN/GaN HFETs[64]. The situation in InAlN/GaN HFETs can be quite different from AlGaN/GaN HFETs because the InAlN can be grown lattice-matched to GaN, which potentially makes the inverse piezoelectric effect not important. More importantly, the large 2DEG density at the InAlN/GaN interface can cause much stronger hot-electron, hot phonon (non-equilibrium optical phonon), and self-heating (excess acoustic phonon) effects, especially because the hot-phonon lifetime is larger in InAlN/GaN HFETs than that in AlGaN/GaN HFETs due to the much larger 2D and 3D electron density (In InAlN/GaN case, the 3D density is larger than the minimum point and is more far away from the minimum point than AlGaN/GaN HFETs)[48].

Due to varying field strengths and electron concentrations involved, different degradation mechanism(s) can be expected for different bias points as demonstrated in Figure 40. For the case of $V_{GS} = 0V$ and biasing the drain contact with voltage just enough for saturating

the drain current, only self-heating effect should be expected. While for the case of V_{DS} =0V and large reverse gate bias, the inverse piezoelectric effect caused by high vertical electric field should dominate if the gate leakage current is small. For the case of on-state-high-field stress (V_{GS}=0V and drain bias is large (i.e. ≥20V)), then a combination of hot-phonon, hot-electron and self-heating effects should prevail. For off-state-high-field stress, where the channel is in the pinch-off condition while the drain bias is still high, the contributing mechanisms in this case should be hot electron and inverse-piezoelectric effect. In order to demonstrate the impact of the above mentioned mechanisms on the device degradation, electrical stresses under four different bias points were conducted with special focus on the hot-phonon, hot electron, self-heating, and inverse piezoelectric effects to discern various effects on the electrical and phase noise performance of InAlN/GaN based HFETs. An attempt was made to distinguish the major degradation mechanisms in InAlN/GaN HFETs at various indium compositions.

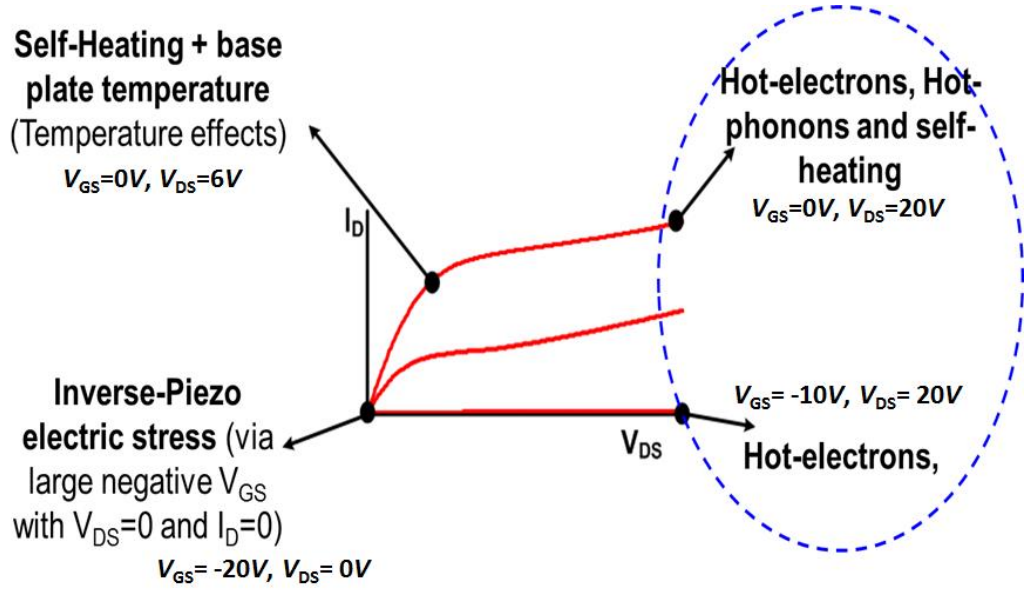

Figure 40 Degradation mechanisms that may dominate under different bias conditions.

One extreme we chosen is InAlN/GaN HFETs with 15.7% indium composition, where the devices degraded very fast as already demonstrated in Figure 35(a). The $In_{0.157}Al_{0.843}N$/AlN/GaN HFET structures were grown by metalorganic chemical vapor deposition on *c*-sapphire substrates covered with 250 nm-thick AlN initiation layers. The structures are comprised of a 2-μm-thick undoped GaN layer followed by a 1-nm-thick AlN spacer, a 20-nm-thick nominally undoped $In_xAl_{1-x}N$ (x=0.157) barrier, and a 2-nm-thick GaN cap layer. The source and drain contacts were formed using standard photolithography with Ti/Al/Ni/Au (30/100/40/50 nm) metal stacks annealed at 800 ^oC. Mesa isolation was performed using a SAMCO inductively coupled plasma system with Cl-based chemistry. Gate electrodes were formed by deposition of Pt/Au (30/50 nm). The gate length, the gate width, and the source-drain spacing are L_G= 2.0 μm, W_G= 90 μm, and L_{SD} = 7 μm, respectively. Since these devices didn't show much surface effect, the degradation was conducted for un-passivated devices.

The four bias points employed were (*i*) on-state-low-field stress (V_{GS} = 0 *V*, V_{DS} = 6 *V*), (*ii*) reverse-gate-bias stress (V_{GS} = -20 *V*, V_{DS} = 0 *V*), (*iii*) off-state-high-field stress (V_{GS} = -10 *V*, V_{DS} = 20 *V*), and (*iv*) on-state-high-field stress (V_{GS} = 0 *V*, V_{DS} = 20 *V*). An ensemble of the HFET devices on the same wafer has been studied, and the results from a representative device for each bias point are presented here. Each stress test started with an initial 5 hour stress, and then followed by another 20 hour stress. The dc transfer

characteristics and phase noise were measured before and one day after each stress test. If there were any shifts of pinch-off voltage (V_{th}) after stress, the transfer characteristics were adjusted by an amount equaling the shift of V_{th} as it was done in Ref [11]. The gate bias during off-state-high-field stress was chosen to be smaller than the pinch-off voltage (V_{th} ~ -8*V*) to ensure that the channel is fully depleted in case of slight variations in the pinch-off voltage during electrical stress. The noise-spectra-density (NSD) of HFETs can be expressed as [65]

$$\mathrm{NSD} = \frac{A}{f^{\gamma}} + \frac{\sum_i B_i \tau_i}{1 + (2\pi f)^2 \tau_i^2}$$

Equation 13

where τ_i and B_i are the time constant and trap concentration, respectively, of traps located at different discrete energy levels, and γ is a constant which nearly equals 1. The constant *A* characterizes either the mobility fluctuations or number fluctuations from continuous trap spectrum, or both processes acting together [23].

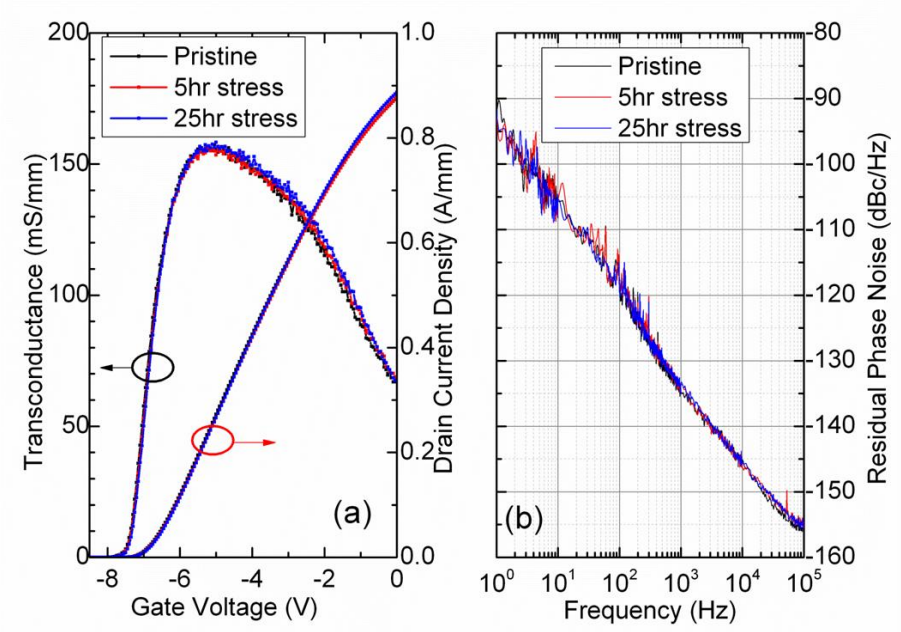

Figure 41 Effect of on-state-low-field stress on (a) I-V and transconductance measured at V_{DS}=6 *V*; (b) phase noise measured at V_{GS}=0 *V* and V_{DS}=6 *V*.

The results for the on-state-low-field stress are demonstrated in Figure 41(a) and (b), where the NSD shows a $1/f^{\gamma}$ shape. The extracted Hooge parameters were on the order of 10^{-4}, which were comparable to AlGaN/GaN based HFETs[66]. The change in NSD was not discernible even after 25 hours of stress, and the drain current shows little change as well. The effects due to the reverse-gate-bias stress are illustrated in Figure 42(a) and (b). The drain current showed little change for the first 5 hour stress and a ~5% change after 25 hour stress (Figure 42(a)). A double peak feature appeared in the g_m plot after 5 hours of stress and became more apparent after the 25 hour stress. This effect is very similar to the kink effect usually ascribed to hot-electron injection into donor-like traps followed by subsequent field-assisted de-trapping under high electric field[45]. Thus, most likely the hot electrons generated traps in the barrier layer around the gate since only the gate area

was affected under corresponding stress condition. The influence was also observed in the noise measurement as demonstrated in Figure 42 (b), where the G–R peak below 1 kHz in the pristine devices diminished after the 25 hour stress. A plausible explanation can be as follows: deep traps were generated during the stress around the gate area, they rendered the pre-existing shallow donor-like traps inaccessible for electrons and caused the observed reduction of the G–R peak intensity in NSD below 1 kHz [67]. The created deep traps should be temporarily stable or equivalently have a very large time constant, thus they would not be reflected in the NSD spectrum which covers from 1 Hz to 100 kHz. For frequencies not influenced by this G–R peak, *i.e.* above 1 kHz, the NSD remained the same, which meant that the *A* parameter in Equation 13 does not change under the reverse-gate-bias stress condition.

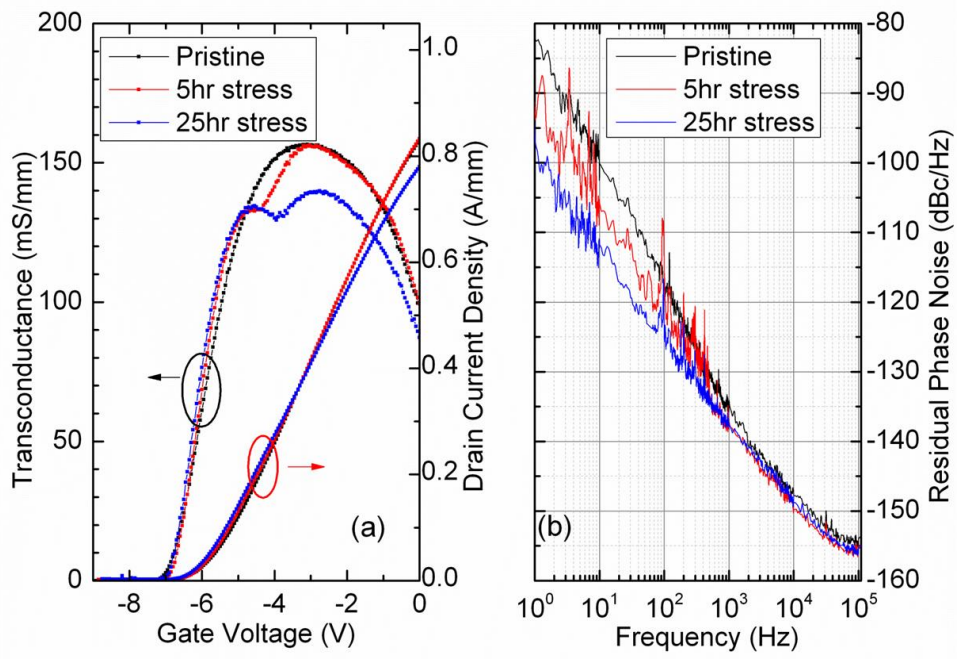

Figure 42 Effect of reverse-gate-bias stress on (a) I-V and transconductance measured at V_{DS}=6 *V*; (b) phase noise measured at V_{GS}=0 *V*, V_{DS}=6 *V*.

In contrast to the above two stress conditions, the off-state-high-field stress exhibited a noticeable reduction in the drain current and an increase in NSD (Figure 43 (a) and (b)). And the most damaging stress condition is the on-state-high-field stress as demonstrated in Figure 44(a) and (b), where the drain current permanently decreased to ~25% of the original value and the NSD increased by about 25-30 dBc/Hz after the 25 hour stress. One common feature for these two stress condition is that the g_m degradation is most pronounced near the g_m peak rather than at V_{GS} bias points closer to zero volt, thus the major degradation is associated with the decrease of channel conductivity instead of the increase in the drain access resistance R_d caused by the electron trapping in the gate–drain access region[39]. This assertion is consistent with the change of channel resistance R_{ch} and drain access resistance R_d after stress, where the increase of R_{ch} takes around 70% of the total increase of source-drain resistance (The method for the resistance measurement is described in Ref. [68]).

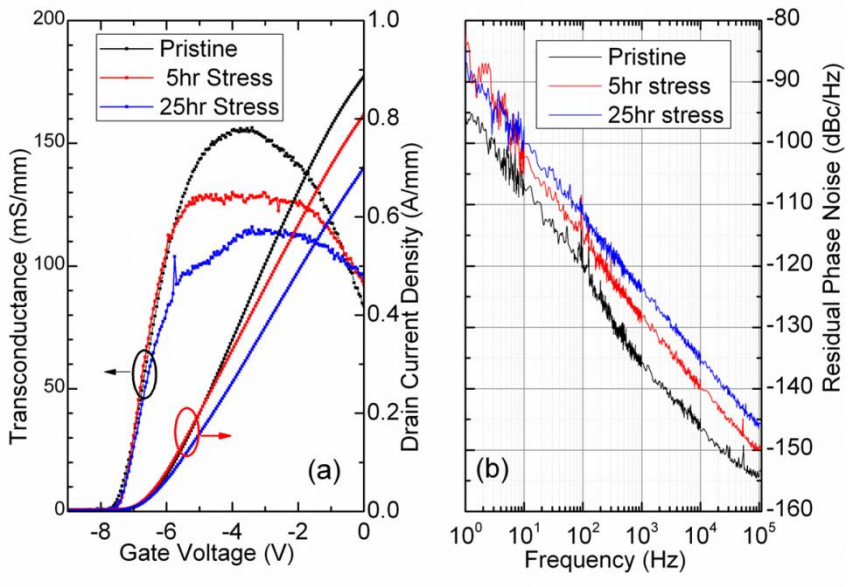

Figure 43 Effect of off-state-high-field stress on (a) I-V and transconductance measured at V_{DS}=6 *V*; (b) phase noise measured at V_{GS}=0 *V*, V_{DS}=6 *V*.

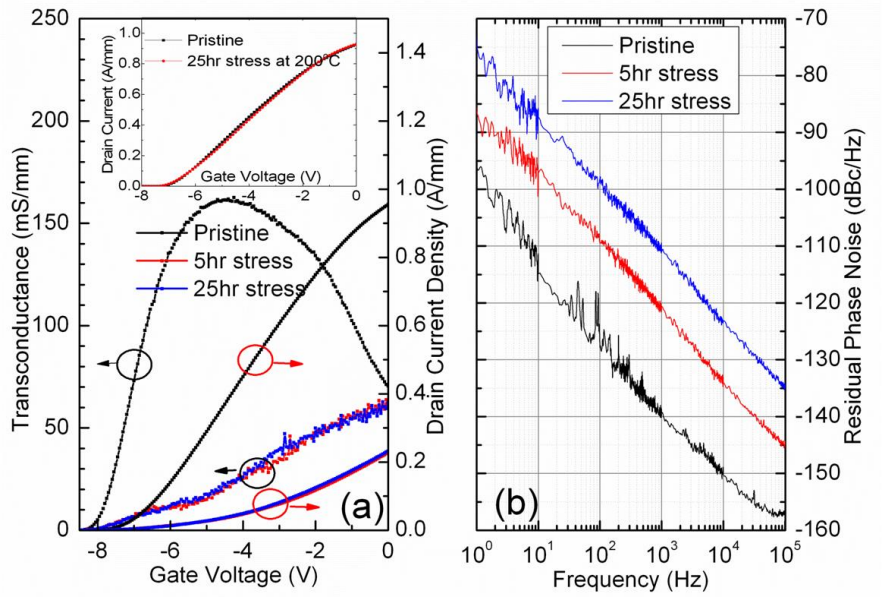

Figure 44 Effect of on-state-high-field stress on (a) I-V and transconductance measured at V_{DS}=6 *V* (The inset shows the drain current density before and after 25hr on-state-low-field stress at 200 °C); (b) phase noise measured at V_{GS}=0 *V*, V_{DS}=6 *V*.

The results of Figure 41(a) and (b) demonstrate that the electrical properties of the devices show no change after the on-state-low-field stress. Consequently, the channel self-heating effect due to the drain current at moderate drain bias is not likely to cause any degradation in the channel. The excess acoustic phonon temperature under the on-state-high-field stress is expected to be around 219 ^{o}C higher than that under the on-state-low-field stress if we assume a thermal resistance of around 27.3 ^{o}C·mm/W [56]. In order to isolate the effect due to excess acoustic phonons from the on-state-high-field stress, an ensemble of pristine devices were stressed under on-state-low-field stress at 200^{o}C to test the heating effect only. No permanent degradation of drain current was observed (inset of Figure 44(a)), which is consistent with the known good thermal reliability of InAlN/GaN based HFETs [69]. Thus, the large degradation under on-state-high-field stress cannot be attributed to the self-heating effect caused by the excess acoustic phonons. The reverse-gate-bias stress and the associated piezoelectric effect can cause damage to the barrier layer and change the drain current by depleting the 2DEG in the channel[46]. However, the change in the drain current predominantly results from a shift of the pinch-off voltage in our experiments. Indeed, Figure 42(a) demonstrates a very small change in the drain current after correcting for the pinch-off voltage. Thus, the degradation is limited to the barrier layer, and moreover, most probably near the surface area far away from the channel, which can have only an indirect influence on the channel properties. This assertion is plausible since the remote ionized impurity scattering will cause minor effect on the mobility of the 2DEG for a typical barrier thickness of 20 nm [70], particularly at room temperature and above. This

is also confirmed by the NSD results since the *A* parameter shows no change after the reverse gate bias stress as discussed above.

The channel degradation induced by the off-state-high-field stress is evidenced through the drain current and the NSD. The degradation is possibly caused by the electrons leaking along the channel through the depleted high-field area. Due to the high source–drain voltage, these electrons are hot and can cause direct damage in the channel, *i.e.* through the generation of trap states in the channel. This in turn causes a reduction of channel conductivity and increase of the NSD. This is also consistent with the high degradation rate for the on-state-high-field stress considering the large amount of the hot-electrons in the channel compared to that of the off-state-high-field stress condition. Also the large amount of hot-electrons in the channel will induce high density of hot phonons and the resultant strong hot-phonon effect [13][63], which can speeds up the degradation. The increase of the *A* parameter in the NSD exclusively correlated with the reduction of the drain current as demonstrated by the on-state-high-field and off-state-high-field stress, thus the increase of noise should directly relates to the increase of R_{ch} caused by channel degradation and/or increase of R_d by electron trapping in the gate-drain access region. Considering the *A* parameter in NSD did not change after the reverse-gate-bias stress, the increase of noise under the off-state-high-field stress and the on-state-high-field stress most likely comes from the increase of R_{ch} due to the channel degradation instead of the increase of R_d caused by electron trapping in the gate-drain access region. Although passivation could reduce surface trapping at the gate-drain access region and therefore alleviate the increase in R_d, it

would not impact the conclusions presented here as reliability was found to be limited mainly by channel degradation.

In conclusion, electric stress for $In_{0.157}Al_{0.843}N$/AlN/GaN HFETs at four different bias conditions has been conducted to probe various degradation mechanisms and their impact on the phase noise performance. The location and nature of the degradation have been correlated with the observed *I*-*V* and NSD data. Data in aggregate are consistent with the assertion that the dominant degradation is due to the hot-phonon and hot-electron effects, where the primary degradation location is in the channel. The channel deterioration is shown to decrease the channel conductivity and cause almost frequency-independent increase of the NSD.

7.4 Degradation study of $In_{0.185}Al_{0.815}N$/GaN HFETs under four bias point stresses

As already demonstrated above, the most deteriorate degradation condition for $In_{0.157}Al_{0.843}N$ /GaN HFETs is on-state-high-field stress, which was ascribed to be the hot-electron/phonon effects. Now the question is what might be the major degradation mechanism for the stable $In_{0.185}Al_{0.815}N$/GaN HFETs. Similarly, we can employ four bias point stresses to find out the major degradation bias conditions. The $In_{0.185}Al_{0.815}N$/GaN HFET structures were grown by metalorganic chemical vapor deposition on *c*-sapphire substrates covered with 250 nm-thick AlN initiation layers. The structures are comprised of a 2-μm-thick undoped GaN layer followed by a 1-nm-thick AlN spacer, a 25-nm-thick nominally undoped $In_xAl_{1-x}N$ (x=0.185) barrier, and a 2-nm-thick GaN cap layer. Because the surface effect was so large in this wafer, we used SiNx passivation trying to improve the device performance. The device performance before and after SiNx passivation is demonstrated in Figure 45. Although the gate-lag and f_T showed some improvement after SiNx passivation, the improvement was not substantial. And there still existed a huge amount of gate lag for the passivated device. Although large amount of surface states still exist, we can actually use surface states as a signature for the degradation of device performance after stress which will be demonstrated soon.

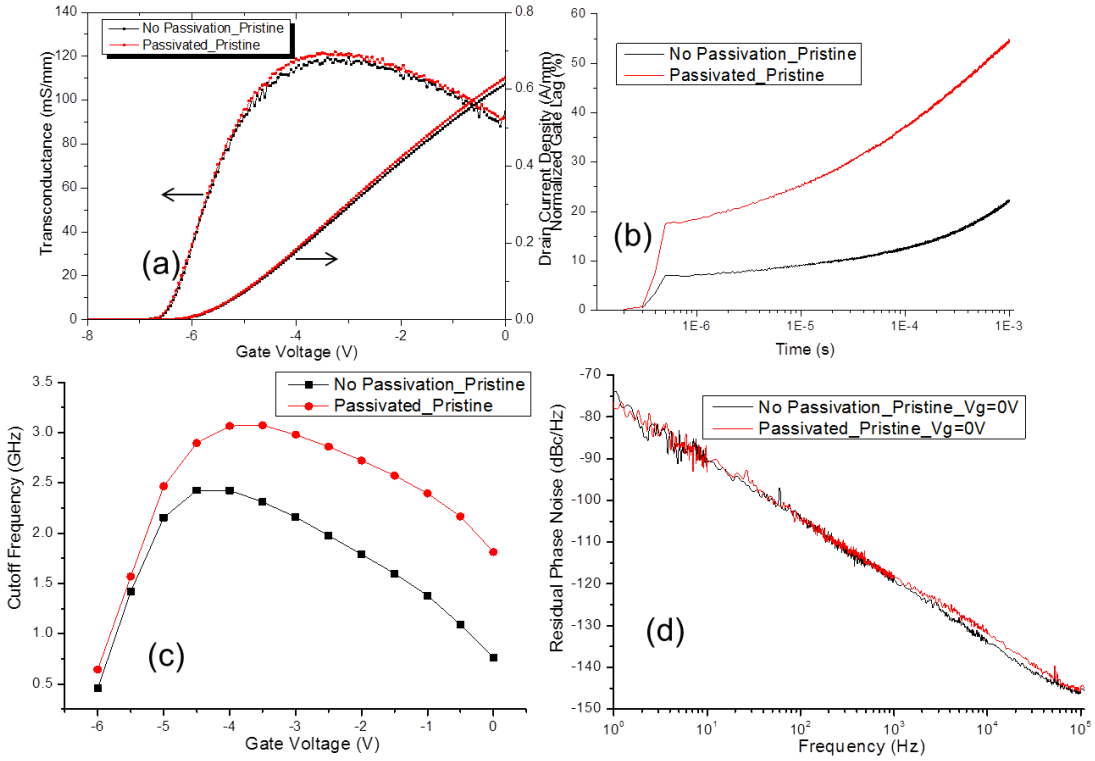

Figure 45 Device performance for $In_{0.185}Al_{0.815}N$/GaN HFETs before and after SiNx passivation. (a) Drain current and transfer characteristic measured at V_{DS}=6*V*; (b) gate lag measured at V_{DS} = 6V and pulse the gate from -8*V* to 0V; (c) current gain cutoff-frequency (f_T) measured at V_{DS} =6V; (d) phase noise measured at V_{GS} =0*V* and V_{DS} =6*V*.

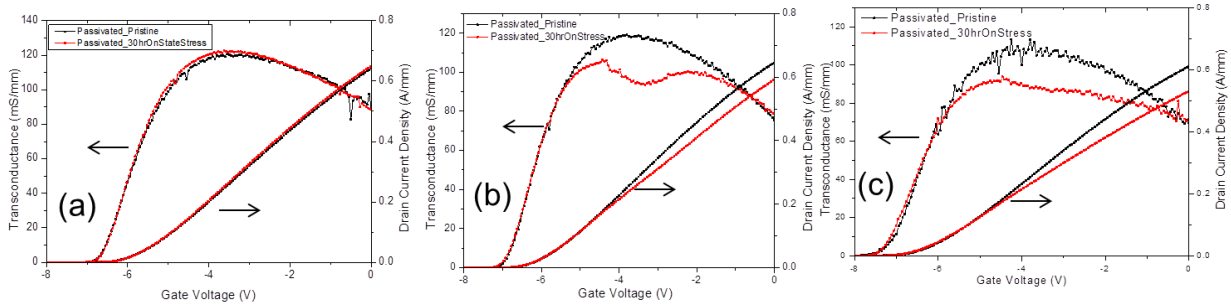

Figure 46 Drain current and transfer characteristic of $In_{0.185}Al_{0.815}N$ /GaN HFETs before and after 30 hours on-state-high-field stress. The stress conditions are (a) V_{GS} =0*V* and V_{DS} =20V; (b) V_{GS} =0*V* and V_{DS} =25V; (c) V_{GS} =0*V* and V_{DS} =30V.

The on-state-high-field stress conditions are V_{GS}=0*V* and V_{DS}=20, 25, or 30*V*, respectively, for 30 hours at room temperature. The drain current and transfer characteristic before and

after stress are demonstrated in Figure 46. As we can see for stress condition of V_{GS}=0V and V_{DS}=20V, the drain current didn't show any degradation. HFET devices started to degrade for stress at V_{GS}=0V and V_{DS}=25V, and the degradation further increased for stress at V_{GS}=0V and V_{DS}=30V. The degradation of transconductance was the largest at V_{GS}= -4V (corresponds to the peak of the transconductance), which implied that the degradation most likely came from the channel conductance degradation[39]. The behavior of the drain current degradation at higher drain bias stresses is consistent with the gate lag results as demonstrated in Figure 47. The gate lag showed improvement when stressed at V_{GS}=0V and V_{DS}=20V, however, the gate lag degraded when stressed at V_{GS}=0V and V_{DS}=25V or 30V. Thus, the devices suffered from performance degradation under on-state-high-field stress with higher drain biases. These results are also consistent with the change of f_T as demonstrated in Figure 48. The f_T firstly increased after stressed at V_{GS}=0V and V_{DS}=20V, which was due to the diminishing of the gate extension or virtual gate. The f_T increased as well for devices stressed at V_{GS}=0V and V_{DS}=25V, but the increase was smaller than that of stressed at V_{GS}=0V and V_{DS}=20V. The f_T decreased for devices stressed at V_{GS}=0V and V_{DS}=30V, which clearly showed that the RF performance of HFETs degraded after stressed at V_{GS}=0V and V_{DS}=30V for 30 hours. These results are consistent with the noise spectra as well, where the phase noise initially showed decrease after stressed at V_{GS}=0V and V_{DS}=20V, and the decrease of phase noise was smaller for devices stressed at V_{GS}=0V and V_{DS}=25V or 30V.

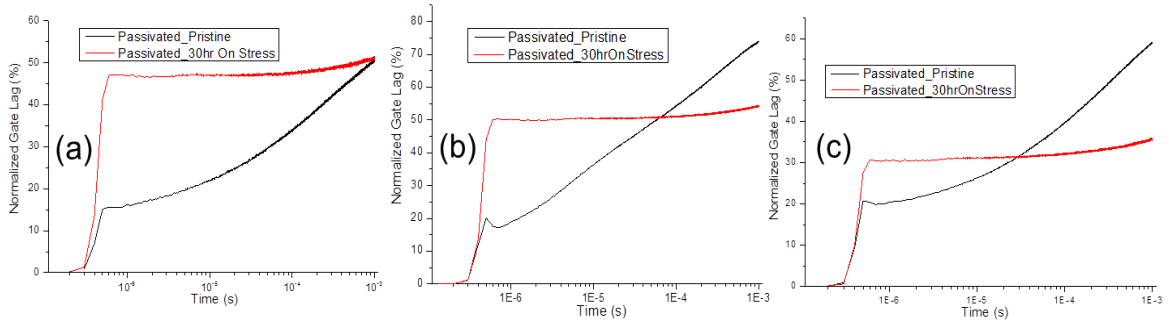

Figure 47 Gate Lag results of $In_{0.185}Al_{0.815}N$ /GaN HFETs before and after 30 hours on-state-high-field stress. The stress conditions were (a) V_{GS}=0V and V_{DS}=20V; (b) V_{GS}=0V and V_{DS}=25V; (c) V_{GS}=0V and V_{DS}=30V. The gate lag was measured at V_{DS}=6V and pulsed V_{GS} from -8V to 0V with 1% duty cycle.

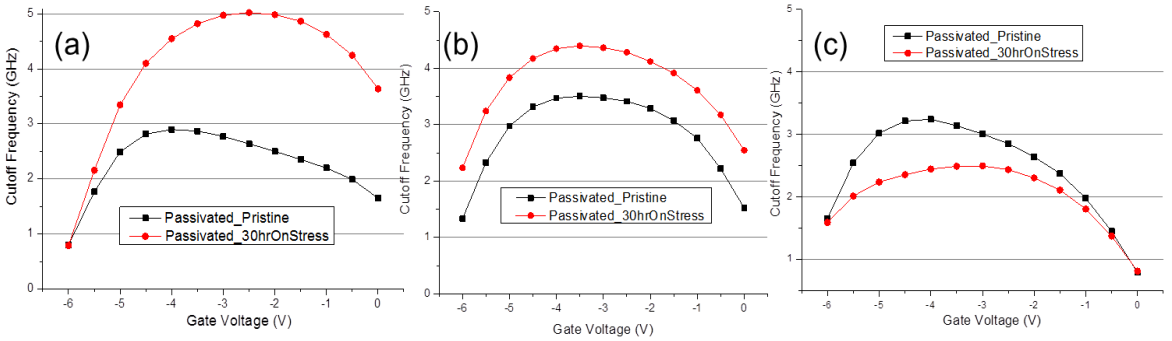

Figure 48 Current gain cutoff frequency (f_T) for $In_{0.185}Al_{0.815}N$ /GaN HFETs before and after 30 hours on-state-high-field stress. The stress conditions were (a) V_{GS}=0V and V_{DS}=20V; (b) V_{GS}=0V and V_{DS}=25V; (c) V_{GS}=0V and V_{DS}=30V. The results were obtained at V_{DS}=6V.

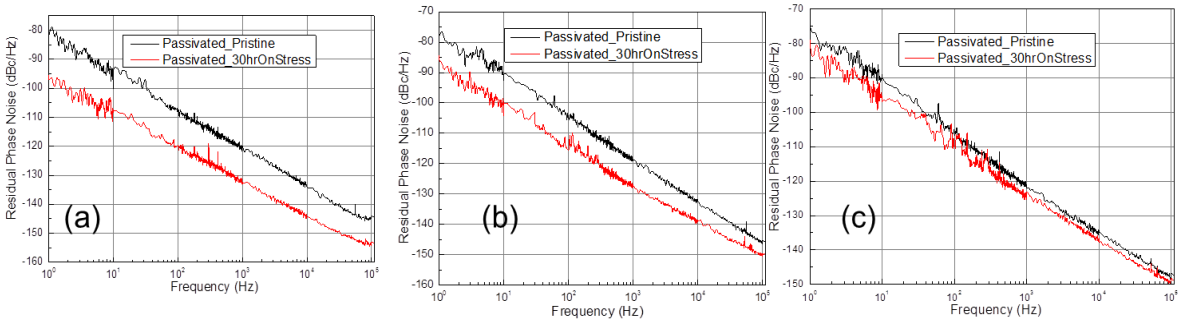

Figure 49 Phase noise spectra for $In_{0.185}Al_{0.815}N$ /GaN HFETs before and after 30 hours on-state-high-field stress. The stress conditions were (a) V_{GS}=0V and V_{DS}=20V; (b) V_{GS}=0V and V_{DS}=25V; (c) V_{GS}=0V and V_{DS}=30V. The results were obtained at V_{GS}=0V and V_{DS}=6V.

There were two phenomena remained unexplained: 1) what makes the RF and noise properties improved for devices stressed at V_{GS}=0V and V_{DS}=20V; 2) Why the performance degraded, especially why the drain current decreased , for devices stressed at V_{GS}=0V and V_{DS}=30V. In order to demonstrate that the above mentioned phenomena were not due to the large electric field presented during the stress, nominally identical pristine devices were stressed at V_{GS} = -20, -25, or -30V and V_{DS} =0V (reverse-gate-bias stress conditions) for 30 hours, and the results were presented in Figure 50, Figure 51, Figure 52, and Figure 53. After reverse gate bias stress with V_{GS} down to -30V, the drain current didn't show any degradation as demonstrated in Figure 50, although the gate lag increased for all three reverse-gate-bias stress conditions (Figure 51). The f_T also decreased slightly for all three stress conditions, which were different from that under on-state-high-field stress conditions where some of the f_T increased after stress. The above phenomena were also consistent with the noise results in Figure 53. For reverse-gate-bias-stress at V_{GS} = -20V and V_{DS} =0V, the phase noise didn't show any change, while the phase noise showed slightly increase for reverse-gate-bias-stress at V_{GS} = -25V or -30V and V_{DS} =0V. As we already demonstrated in Silvaco Atlas simulation in Figure 27, reverse-gate-bias stress conditions induces ~10% more vertical electric field than that of on-state-high-field stress conditions for the same applied gate-drain biases. Here we observed no drain current degradation under reverse-gate-bias stress, while drain current degradation were indeed observed for the same applied gate-drain biases under on-state-high-field stresses. Thus, the degradation of $In_{0.185}Al_{0.815}N$/GaN HFETs under on-state-high-field stress conditions had nothing to do with the vertical electric field during the stress. Thus, the inverse piezoelectric effect

proposed for the degradation of AlGaN/GaN HFETs should have very small effect in lattice-matched InAlN/GaN HFETs, especially compared to on-state-high-field stress.

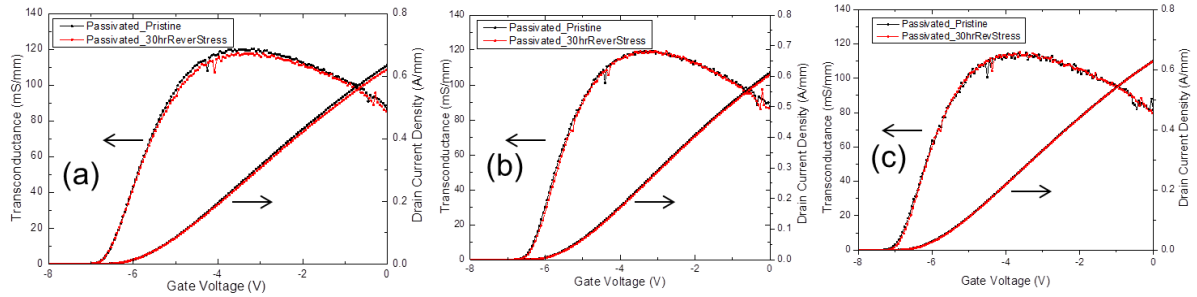

Figure 50 Drain current and transfer characteristic of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress. The stress conditions were (a) V_{GS}= -20V and V_{DS}=0V; (b) V_{GS}= -25V and V_{DS}=0V; (c) V_{GS}= -30V and V_{DS}=0V. The results were obtained at V_{DS}=6V.

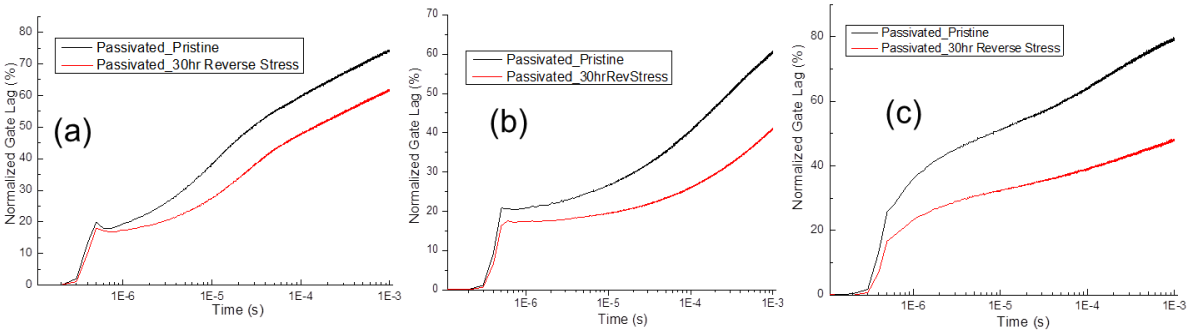

Figure 51 Gate Lag results of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress. The stress conditions are (a) V_{GS}= -20V and V_{DS}=0V; (b) V_{GS}= -25V and V_{DS}=0V; (c) V_{GS}= -30V and V_{DS}=0V. The results were obtained at V_{DS}=6V and pulsing V_{GS} from -8V to 0V.

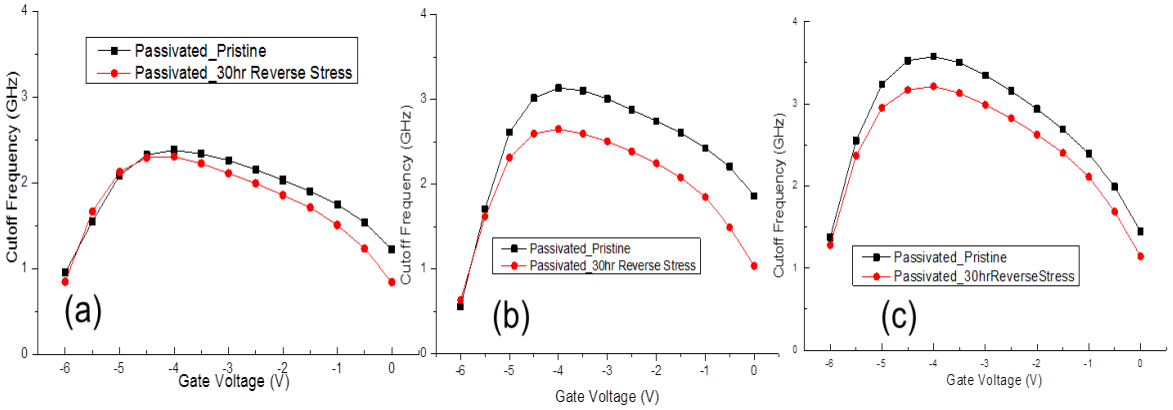

Figure 52 Current gain cutoff frequency (f_T) results of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress. The stress conditions were (a) V_{GS}= -20V and V_{DS}=0V; (b) V_{GS}= -25V and V_{DS}=0V; (c) V_{GS}= -30V and V_{DS}=0V. The results were obtained at V_{GS}= 0V and V_{DS}=6V.

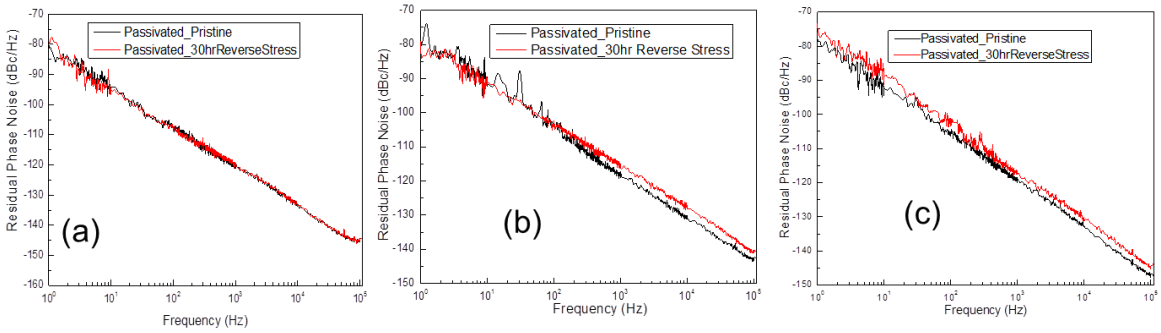

Figure 53 Phase noise spectra of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress. The stress conditions were (a) V_{GS}= -20V and V_{DS}=0V; (b) V_{GS}= -25V and V_{DS}=0V; (c) V_{GS}= -30V and V_{DS}=0V. The results were obtained at V_{GS}= 0V and V_{DS}=6V.

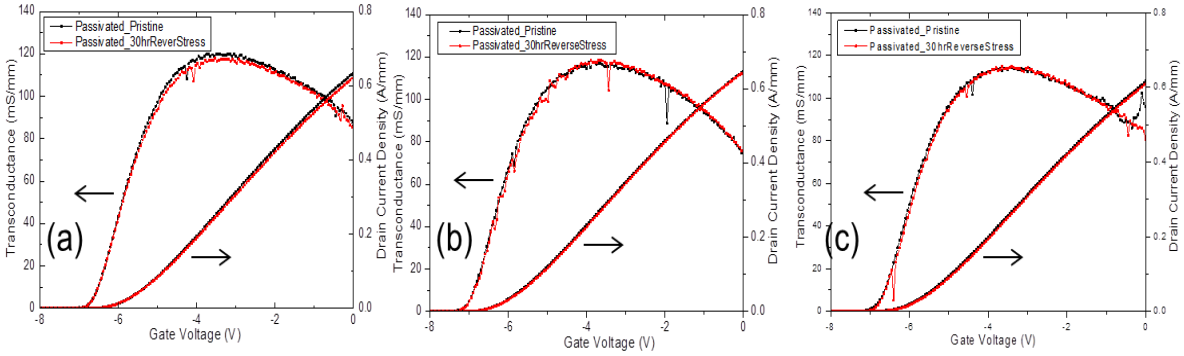

Figure 54 Drain current and transfer characteristic of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress (V_{GS}= -20V and V_{DS}=0V) at different temperatures: (a) room temperature; (b) 100 ^{o}C; (c) 150 ^{o}C. The results were obtained at V_{DS}=6V.

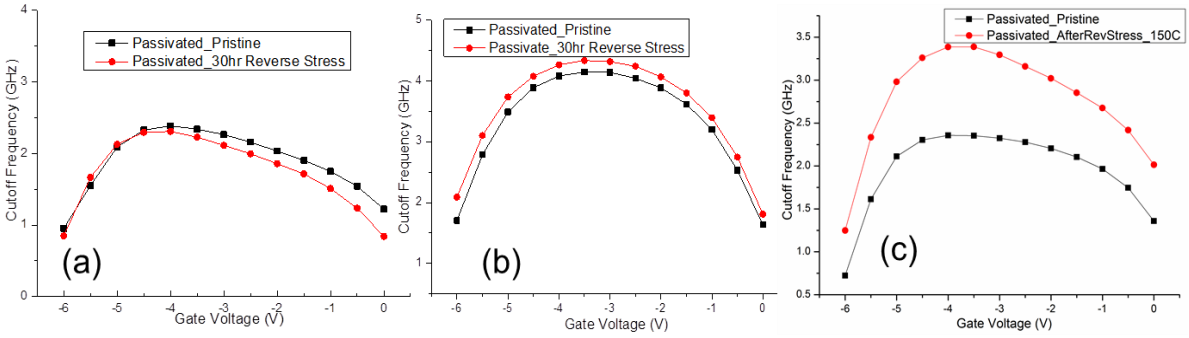

Figure 55 Current gain cutoff frequency (f_T) results of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress at V_{GS}= -20V and V_{DS}=0V at different external base plate temperatures: (a) room temperature; (b) 100 ^oC; (c) 150 ^oC. The results were obtained at V_{DS}=6V.

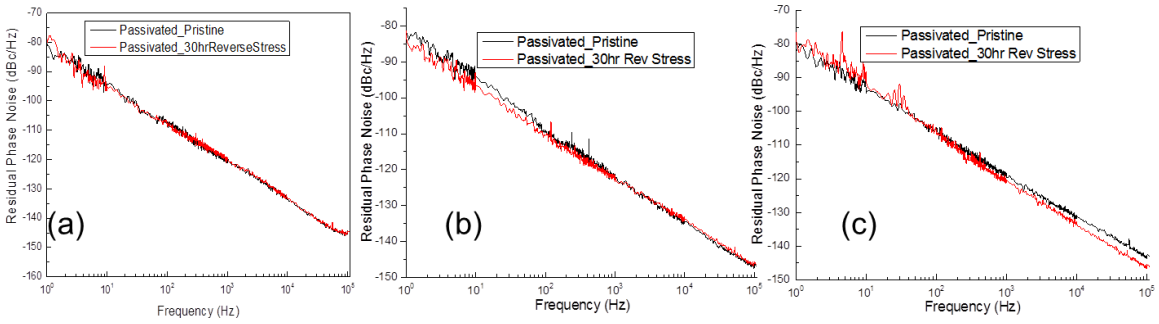

Figure 56 Phase noise results of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours reverse-gate-bias stress at V_{GS}= -20V and V_{DS}=0V at different external base plate temperatures: (a) room temperature; (b) 100 ^oC; (c) 150 ^oC. The results were obtained at V_{GS}= 0V and V_{DS}=6V.

The on-state-high-field stresses differ from reverse-gate-bias stress due to the associated strong the hot-electron/phonon plus self-heating effect under the on-state-high-field stress conditions. Thus the drain current degradation after V_{GS}=0V and V_{DS}=25V or 30V should be due to hot electron/phonon or self-heating effect or the combination of the all three effects. To isolate the self-heating effect from the hot-electron/phonon effect, pristine devices were stressed under reverse-gate-bias stress (V_{GS} = -20V and V_{DS} =0V) for up to 150 ^oC, and the corresponding results are presented in Figure 54, Figure 55, and Figure 56. As we can see from Figure 54, reverse-gate-bias stresses at different temperatures didn't cause any degradation to the drain current, thus self-heating effect is not the reason causing the drain current degradation under on-state-high-field stress as presented in Figure 46(b) and (c). However, the external base plate temperature did make the f_T increase, which means temperature effect did change the surface state and reduced the "virtual gate" or gate extension. However, the total amount of the surface states may still exist since the

phase noise didn't show any change. One plausible situation might be that surface states re-organized under higher temperatures: the gate extension due to the surface states reduced, however, the total amount of surface states did not change. Since the self-heating effect has been demonstrated not be able to cause the drain current degradation, the underlying mechanism contributing to the degradation should be the hot-electron/phonon effects. One more thing need to point out is that only on-state-high-field stress can be able to cause the reduction of phase noise, which is consistent with the conclusion that the hot-electron/phonon effects are the major effect, because the hot-electron effect is proportional to the number of hot-electrons in the channel and only on-state operation can provide large amount of hot-electrons. To further demonstrate this conclusion is correct, we stressed pristine devices at semi-on stress condition (V_{GS}=-5V and V_{DS} =20V) at up to 150 ^{o}C for 30 hours, and the corresponding results are demonstrated in Figure 57 and Figure 58. Although semi-on stress at room temperature didn't cause any change to the RF and noise properties as demonstrated in Figure 57(a) and Figure 58(a) for the time scale of 30 hours, semi-on stress at higher temperature did make the RF and noise properties improved. However, the improvement is much smaller than that under on-state-high-field stress conditions, thus the self-heating effect is secondary effect while the hot-electron/phonon effects are the major effects during the on-state-high-field stress conditions.

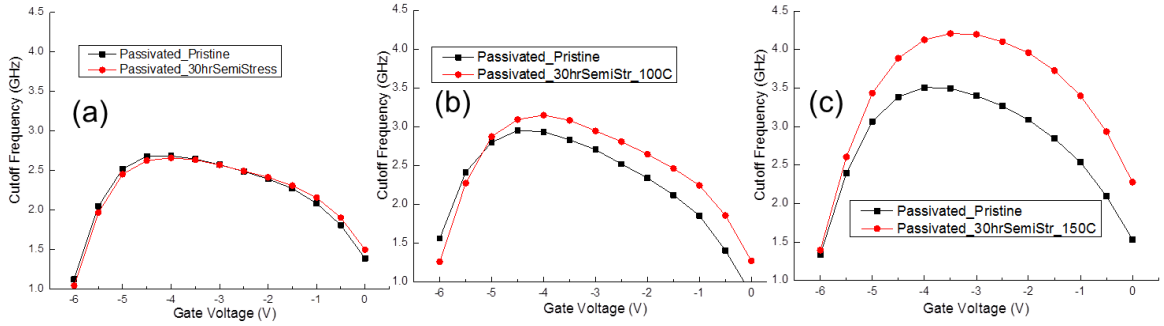

Figure 57 Current gain cutoff frequency (f_T) results of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours semi-on stress at V_{GS}=-5V and V_{DS} =20V at different external base plate temperatures: (a) room temperature; (b) 100 ^oC; (c) 150 ^oC. The results were obtained at V_{DS}=6V.

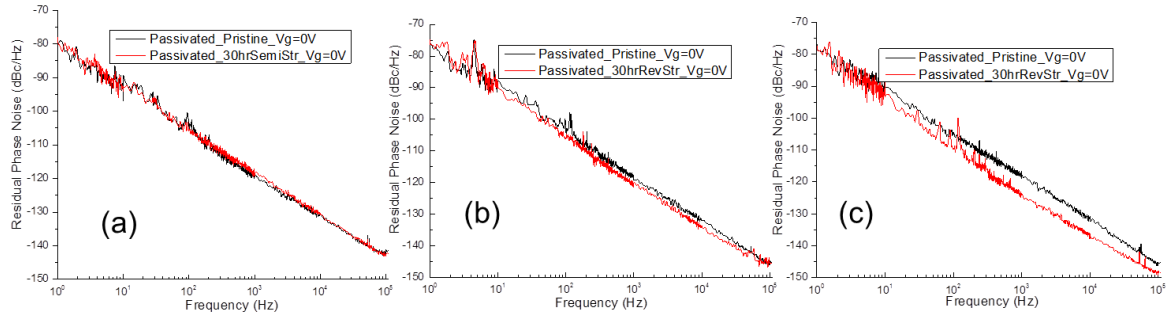

Figure 58 Phase noise results of $In_{0.185}Al_{0.815}N$/GaN HFETs before and after 30 hours semi-on stress at V_{GS}=-5V and V_{DS} =20V at different external base plate temperatures: (a) room temperature; (b) 100 ^oC; (c) 150 ^oC. The results were obtained at V_{GS} =0V and V_{DS}=6V.

Although the phase noise decreases after on-state-high-field stress at V_{DS}=20V in $In_{0.185}Al_{0.815}N$/GaN HFETs, the phase noise eventually increase after on-state-high-field stress at V_{DS}=30V. The decrease is due to the diminishing of the surface effect, probably due to permanent electron trapping around the gate area. The eventual increase of phase noise should be due to the hot-electron/phonon effect because the much larger drain voltage induced stronger hot-electron/phonon effect than that on-state-high-field stressed under V_{DS}=20V. It has been observed that the phase noise also increased slightly after reverse-gate-bias stress with V_{GS}= -30V, however, the increase is smaller than that caused

by on-state-high-field stress at V_{DS}=30V. These results are consistent with the conclusion that hot-electron/phonon effect is more important in lattice-matched InAlN/GaN HFETs than the inverse-piezoelectric effect. More convincing evidence comes from that only on-state-high-field stress caused the reduction of drain current (The drain current didn't show any change after reverse-gate-bias stress under the gate-drain bias). Once again, we emphasize that the degradation induced by the vertical electric field is not as important as the lateral electric field induced hot-electron/phonon effects.

7.5 Comparison of the degradation behavior of AlGaN/GaN and InAlN/GaN HFETs

Although the operation mechanisms of AlGaN/GaN and InAlN/GaN HFETs are exactly the same, the device degradation is different in terms of both degradation behaviors as reflected by DC, microwave, and noise performance and fundamental degradation mechanisms. For un-passivated AlGaN/GaN HFETs, the gate lag always become larger after on-state-high-field stress, however, it becomes smaller for $In_{0.185}Al_{0.815}N$/GaN HFETs after on-state-high-field stress with V_{DS}=20V. Since the phase noise due to surface effect becomes smaller in both cases, negative charges with long time-constant should be generated around the gate in both cases, which make the pre-existing short time-constant traps inaccessible to electron. These long time-constant traps will still be able to trap electrons during the switching of the gate bias, thus they can still contribute to the gate lag. And they should have much larger concentration than the pre-existing short time-constant traps, which is the reason why the overall gate lag becomes larger after stress. However, they should not contribute to the phase noise because their time-constant should be larger than 1 second, which is outside the measurement frequency of phase noise (above 1 Hz). For $In_{0.185}Al_{0.815}N$/GaN HFETs, the generated traps most likely permanently trapped electrons making them negatively charged thus reduce the contribution to gate lag and phase noise from the pre-existing short time-constant traps. While these generated traps will not have any trapping or de-trapping behavior since they already permanently captured

electrons. Thus the overall contribution from pre-existing short time-constant and generated traps to gate lag and phase noise decreased.

Regarding the fundamental degradation mechanisms involved in AlGaN/GaN HFETs and InAlN/GaN HFETs, both inverse-piezoelectric and hot-electron/phonon effects should involve under these two stress conditions. In near lattice-matched InAlN/GaN HFETs, the inverse-piezoelectric effect is not important because the strain in nearly lattice-matched InAlN barrier is very small. Instead, hot-electron/phonon effects dominate due to the large drain current level at on-state operation. However, the behavior in AlGaN/GaN HFET structures is significantly different than that in InAlN/GaN structures, primarily due to the strain and the current level during device operation. And we demonstrated that even in AlGaN/GaN HFET structures where the barrier strain is much larger and the drain current level is much smaller than in InAlN/GaN HFET structures, the hot electron/hot phonon effects are still very important, especially at high drain bias under on-state-high-field condition.

CHAPTER 8 HFETs Conclusions and Future Work

8.1 Conclusion and future work for the degradation study of AlGaN/GaN HFETs

The location of the failure has been exclusively ascribed to the gate edge close to the gate-drain access region in AlGaN/GaN HFETs where the electric field is the highest. A popular proposed mechanism for the degradation is the so-called inverse-piezoelectric effect[9] based on the hypothesis that mechanical strain produced by the high gate-drain voltage may aggravate the tensile stain caused by the lattice-mismatch between AlGaN barrier and GaN layer, where the proposed degradation mechanism indicated the existence of a critical gate-drain voltage, beyond which the HFET device started to degrade abruptly. However, permanent degradation was found even for stress below critical voltage with sufficiently long stress times for reverse-gate-bias stress, supporting the hypothesis that permanent degradation is due to a defect percolation process[10], where the defect generation can be due to the hot-electrons induced by the large vertical electric field under reverse gate bias stress, and the generated defects in the barrier can be acting as gate leakage paths. Besides that, dislocation defects originating from epitaxy growth due to the lattice-mismatch between AlGaN and GaN has been proposed to be impurity diffusion path[11]. It has been demonstrated that devices with larger dislocation densities showed larger degradation in terms of gate lag after electric stress[71], and impurity(s) diffusion along dislocation lines was proposed to be the underlying mechanism, where oxygen impurity was believed to be one possible candidate. Diffusion is long term process, but the stress time in Ref. [71] was just 20 hours. As mentioned above, degradation has been

proposed as a defect percolation process, and dislocation lines can be one type of the defects. The impurity diffusion hypothesis may be possible, but it should be further verified by comparing with HFETs devices with in-situ passivation, for example SiNx[72], where the HFETs surface is free from oxygen and other impurities. Although the major degradation mechanism(s) are still not clear, it has been find out that gate leakage current exclusively get increased for passivated devices after high voltage stress regardless with or without drain current, which is different from un-passivated devices where the gate leakage current got decreased after moderately high voltage stress[39], [67], possibly because the electric field is larger for passivated devices[73]. The increased gate leakage current after stress can be due to the increased electron tunneling from the gate electrode to the barrier, probably via the defect states in the barrier. An in-situ passivation layer, which also acts as a gate dielectric, is expected to decrease the gate leakage and hence may be able to reduce the degradation due to the injection of high kinetic energy electrons into the barrier.

An optimum *in-situ* SiNx layer thickness should be adopted for both good reliability and device performance. A too thick SiNx layer will reduce the transconductance of the device, while a too thin SiNx layer will not be effective to reduce the gate leakage current. However, the SiNx layer may potentially introduce trap states inside the SiNx layer or at the SiNx/barrier interface. Thus, a detailed study should be conducted via dc, microwave and noise measurements. Additionally, degradation under different bias conditions can be conducted for *in-situ* SiNx passivated HFETs to study the degradation behaviors and verify each proposed degradation mechanisms.

HFET devices operated under on-state or high power state will suffer from the self-heating effect due to the hot-phonon and hot-electron effects. In order to alleviate the degradation from hot-phonon effect, the hot phonons need to be effectively removed from the 2DEG channel. As we introduced earlier, the lifetime of the hot-phonons in the channel depends on the 3D electron density in the channel, and the minimum hot-phonon lifetime occurs at a certain 3D electron density. Unfortunately, in the case of AlGaN/GaN and InAlN/GaN HFETs with commonly used aluminum or indium compositions, the 3D electron density is much higher than the one corresponding to the minimum hot-phonon lifetime. It has been demonstrated and introduced in previous section of this thesis that the by using a double-channel HFET structure, the 3D electron density in the channel can be reduced to achieve a smaller hot-phonon lifetime while maintaining the 2D electron density. In this way, the degradation rate due to the hot-phonon effect is expected to be reduced. By adopting a MOSHFET double channel structure, the impact of gate leakage current & surface impurities on the degradation of devices can be minimized by the gate dielectric, enabling us to focus on the effect of double-channel structure on the device degradation.

GaN-based HFETs are usually grown on SiC or silicon substrate, by growing HFETs on GaN substrate, the defect states (especially dislocation density) in the barrier and GaN channel are expected to be much smaller than that on SiC and silicon substrates. The defect states are believed to facilitate degradation, both in the point view of defect percolation hypothesis and impurity diffusion hypothesis. If HFETs are grown on GaN substrates with

in-situ and *ex-situ* passivation, respectively, the defect density due to dislocations are expected to be the same and more importantly small, while the surface impurity densities are not. By comparing the degradation phenomena in these two types of devices, we can evaluate the impact of surface impurity on the degradation of HFETs. And the degradation signature can be associated with corresponding proposed degradation mechanisms.

8.2 Conclusion and future work for the degradation study of InAlN/GaN HFETs

As demonstrated above, the degradation rate of InAlN/GaN HFETs is the largest under on-state-high-field stress, where the degradation has strong dependence on the channel current during the stress. The degradation mechanism is ascribed to be the hot-electron/hot phonon effects. For degradation under other bias points, especially under no drain current bias conditions, the degradation rate is small. For InAlN/GaN HFETs with indium composition smaller than 18%, devices degrade very fast in terms of reduction of drain current, reduction of current gain cutoff frequency, and increase of phase noise. In order to minimize the effect of hot phonon on the degradation of InAlN/GaN, one method can be used is to minimize the hot-phonon lifetime or expedite the transfer of hot-phonon to acoustic phonon as demonstrated in Ref. [50] by introduction of double channel structure. Thus, further research should be done to investigate the degradation of InAlN/GaN HFETs with double channel structure.

For the degradation study of $In_{0.185}Al_{0.815}N$/GaN HFETs, although we passivated the devices with SiNx, the surface effect is still large. Thus, it is important to reduce this surface effect by either surface treatment before passivation or by in-situ passivation as proposed for AlGaN/GaN HFETs. Additionally, the InAlN/GaN HFETs device structure under study are all with barrier thickness of ~ 20nm. Although a minimum barrier thickness of ~ 20nm is necessary to maintain a large 2DEG density in AlGaN/GaN HFETs,

there is no such minimum requirement on the barrier thickness of InAlN/GaN HFETs. And the barrier thickness used in literature is ~10nm. The advantage of using a barrier thickness of only ~10nm is that we can have very good ohmic contact, thus can further increase the drain current. Degradation study of InAlN/GaN with thickness of ~10nm should be conducted to investigate the influence of barrier thickness on the degradation.

The InAlN/GaN HFETs has been demonstrated to suffer even more from the hot-electron/phonon effects than that of AlGaN/GaN HFETs. As we stated above, a method to reduce the hot-phonon effects is to reduce the hot-phonon lifetime so that the hot-phonon can be efficiently removed from the GaN channel. By using a dual channel structure, the hot-phonon lifetime is expected to be reduced and the hot-phonon effect is expected to be smaller as well. In this case, degradation mechanisms other than hot-phonon effects may start to be dominant. By applying electric stress to both single-channel and double-channel InAlN/GaN HFETs, we may further investigate the impact of other degradation mechanisms on the device performance.

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Appendix

Silvaco Atlas code for Electric field simulation

```
go atlas

Title     HEMT Id-Vd and Id-Vg characteristics#

# SILVACO International 1996

#

# SECTION 1: Mesh input

mesh width=1000

x.mesh loc=0            spac=0.05

x.mesh loc=1.4          spac=0.05

x.mesh loc=1.41         spac=0.003

x.mesh loc=1.5          spac=0.003

x.mesh loc=1.6          spac=0.003

x.mesh loc=1.61         spac=0.05

x.mesh loc=3.4          spac=0.05

x.mesh loc=3.41         spac=0.003

x.mesh loc=3.5          spac=0.003

x.mesh loc=3.6          spac=0.003

x.mesh loc=3.61         spac=0.05

x.mesh loc=6            spac=0.05

y.mesh loc=0.0      spac=0.00005
```

```
y.mesh loc=0.0008  spac=0.00005
y.mesh loc=0.0012  spac=0.00005
y.mesh loc=0.0018  spac=0.00005
y.mesh loc=0.0019  spac=0.00005
y.mesh loc=0.002   spac=0.00005
y.mesh loc=0.0021  spac=0.0001
y.mesh loc=0.0022  spac=0.0002
y.mesh loc=0.0025  spac=0.0002
y.mesh loc=0.003   spac=0.0002
y.mesh loc=0.005   spac=0.0005
y.mesh loc=0.008    spac=0.0005
y.mesh loc=0.0155    spac=0.0008
y.mesh loc=0.0165   spac=0.0006
y.mesh loc=0.0174  spac=0.0004
y.mesh loc=0.0175   spac=0.00005
y.mesh loc=0.0176  spac=0.0004
y.mesh loc=0.0181  spac=0.0006
y.mesh loc=0.0185   spac=0.0008
y.mesh loc=0.0195   spac=0.001
y.mesh loc=0.0205   spac=0.002
y.mesh loc=0.05    spac=0.003
y.mesh loc=0.1     spac=0.005
```

```
y.mesh loc=0.2     spac=0.1

y.mesh loc=1       spac=0.25

y.mesh loc=2       spac=0.5

y.mesh loc=4       spac=1

y.mesh loc=20      spac=2



# SECTION 2: Structure Specification

region     num=1  material=GaN    y.min=0.0     y.max=0.001

region     num=2  material=GaN    y.min=0.001   y.max=0.002

region     num=3  material=AlGaN  y.min=0.002   y.max=0.0175 x.comp=0.25

region     num=4  material=GaN    y.min=0.0175  y.max=0.05

region     num=5  material=GaN    y.min=0.05    y.max=1

region     num=6  material=GaN    y.min=1       y.max=20

#

elec num=1 name=source x.min=0    x.max=0.05 y.min=0   y.max=0.022

elec num=2 name=drain  x.min=5.95 x.max=6    y.min=0   y.max=0.022

elec num=3 name=gate   x.min=1.5  x.max=3.5  y.max=0.0


contact name=gate  workfunction=5.2


doping     uniform region=1 n.type conc=0.50e20
```

```
doping     uniform region=2 n.type conc=0.50e19

doping     uniform region=3 n.type conc=5e16

doping     uniform region=4 n.type conc=5e16

doping     uniform region=5 n.type conc=1

doping     uniform region=6 n.type conc=1


interface charge=-1.11875e13 y.min=0.0016   y.max=0.0025 s.s

interface charge=1.1185e13   y.min=0.0155   y.max=0.018  s.s



material region=3 eg300=3.91   nc300=3.23445e18 nv300=1.5678e20   permittivity=8.96
align=0.7 vsatn=1e4   TC.NPOW=1.6 TC.CONST=0.34842 mun=100

material   region=4   eg300=3.42   nc300=2.2343e18   nv300=4.6245e19   permittivity=8.9
TC.NPOW=1.6 TC.CONST=0.34842 mun=1600

material   region=5   eg300=3.42   nc300=2.2343e18   nv300=4.6245e19   permittivity=8.9
TC.NPOW=1.6 TC.CONST=0.34842 mun=1600

material   region=6   eg300=3.42   nc300=2.2343e18   nv300=4.6245e19   permittivity=8.9
TC.NPOW=1.6 TC.CONST=0.34842 mun=1


model    print srh fldmob


mobility material=GaN fldmob.n evsatmod=0 betan=2.6 ALPHAN.FLD=2.326e7
```

```
model   lat.temp
thermcontact num=1 y.min=20 y.max=20 ext.temp=300
output con.band val.band e.field
method block newton vsatmod.inc=0.1 carriers=1 elec

solve init
solve vgate=0
save outf=AlGaN0.25_Vg0_Vd0.str
solve vdrain=0.2 vstep=0.4 name=drain vfinal=5.8
solve vdrain=6.0
solve vgate=0.5
solve vgate=1.0
solve vgate=1.5
solve vgate=2.0
log outf=IV_gm_Vd=6V.log master
solve vgate=2.0 vstep=-0.1 name=gate vfinal=0
solve vgate=0.0 vstep=-0.2 name=gate vfinal=-5
log off
tonyplot IV_gm_Vd=6V.log

method block newton vsatmod.inc=0.1 carriers=1 elec
```

```
solve init

solve vgate=0.5

solve vgate=1          outf=IV_Vg+1.0.out

solve vgate=0          outf=IV_Vg+0.0.out

solve vgate=-1         outf=IV_Vg-1.0.out

solve vgate=-2         outf=IV_Vg-2.0.out

solve vgate=-3         outf=IV_Vg-3.0.out

solve vgate=-4         outf=IV_Vg-4.0.out


# Calculate IV characteristic at Vg=+0

load inf=IV_Vg+0.0.out

log outf=AlGaN0.25_GaN_Vg+0.0.log

solve outf=IV_Vg+0.0.out master

solve vdrain=0.01

solve vdrain=0.02

solve vdrain=0.05

solve vdrain=0.08

solve vdrain=0.16

solve vdrain=0.30

solve vdrain=0.40

solve vdrain=0.40 vstep=0.2 name=drain vfinal=7.0

solve vdrain=7.0 vstep=0.5 name=drain vfinal=15
```

```
save outf=AlGaN0.25_Vg0_Vd15.str
#solve vdrain=20 vstep=0.5 name=drain vfinal=24
#save outf=AlGaN0.25_Vg0_Vd24.str
#solve vdrain=24 vstep=0.5 name=drain vfinal=27
#save outf=AlGaN0.25_Vg0_Vd27.str
#solve vdrain=27 vstep=0.5 name=drain vfinal=30
#save outf=AlGaN0.25_Vg0_Vd30.str
log off

# Calculate IV characteristic at Vg=-1
load inf=IV_Vg-1.0.out
log outf=AlGaN0.25_GaN_Vg-1.0.log
solve outf=IV_Vg-1.0.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.40
solve vdrain=0.40 vstep=0.2 name=drain vfinal=5.0
solve vdrain=5.0 vstep=0.5 name=drain vfinal=15
```

```
save outf=AlGaN0.25_Vg-1_Vd15.str
log off

# Calculate IV characteristic at Vg=-2
load inf=IV_Vg-2.0.out
log outf=AlGaN0.25_GaN_Vg-2.0.log
solve outf=IV_Vg-2.0.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.40
solve vdrain=0.40 vstep=0.2 name=drain vfinal=5.0
solve vdrain=5.0 vstep=0.5 name=drain vfinal=15
#save outf=IV_Vg-6_I.out master
save outf=AlGaN0.25_Vg-2_Vd15.str
log off

# Calculate IV characteristic at Vg=-3.0
load inf=IV_Vg-3.0.out
```

```
log outf=AlGaN0.25_GaN_Vg-3.0.log
solve outf=IV_Vg-3.0.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
solve vdrain=0.08
solve vdrain=0.16
solve vdrain=0.30
solve vdrain=0.40
solve vdrain=0.40 vstep=0.2 name=drain vfinal=5.0
solve vdrain=5.0 vstep=0.5 name=drain vfinal=15
#save outf=IV_Vg-6_I.out master
save outf=AlGaN0.25_Vg-3_Vd15.str
log off

# Calculate IV characteristic at Vg=-4
load inf=IV_Vg-4.0.out
log outf=AlGaN0.25_GaN_Vg-4.0.log
solve outf=IV_Vg-4.0.out master
solve vdrain=0.01
solve vdrain=0.02
solve vdrain=0.05
```

```
solve vdrain=0.08

solve vdrain=0.16

solve vdrain=0.30

solve vdrain=0.40

solve vdrain=0.40 vstep=0.2 name=drain vfinal=5.0

solve vdrain=5.0 vstep=0.5 name=drain vfinal=15

save outf=AlGaN0.25_Vg-4_Vd15.str

log off


# Calculate IV characteristic at Vg=+1.0

load inf=IV_Vg+1.0.out

log outf=AlGaN0.25_GaN_Vg+1.0.log

solve outf=IV_Vg+1.0.out master

solve vdrain=0.01

solve vdrain=0.02

solve vdrain=0.05

solve vdrain=0.08

solve vdrain=0.16

solve vdrain=0.30

solve vdrain=0.40

solve vdrain=0.40 vstep=0.2 name=drain vfinal=8.0

solve vdrain=8.0 vstep=0.5 name=drain vfinal=15
```

```
#save outf=IV_Vg-6_I.out master
save outf=AlGaN0.25_Vg+1_Vd15.str
log off

tonyplot -overlay AlGaN0.25_GaN_Vg-4.0.log AlGaN0.25_GaN_Vg-3.0.log
AlGaN0.25_GaN_Vg-2.0.log AlGaN0.25_GaN_Vg-1.0.log AlGaN0.25_GaN_Vg+0.0.log
AlGaN0.25_GaN_Vg+1.0.log
QUIT
```