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Surface charging and current collapse in an AlGaN/GaN heterostructure field effect transistor

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This work investigates the correlation between surface charging and current collapse in an AlGaN/GaN heterostructure field effect transistor. Surface charging due to applied biases was sensed by mapping the surface potential between the gate and drain using scanning Kelvin probe microscopy. Due to the bias, the surface band bending near the gate edge was observed to increase by as much as 1 eV. This increase of band bending is caused by an accumulation of excess charge near the surface during the applied bias. By varying the duration of the applied bias, we find that this accumulation of excess charge near the gate takes about 20 s to saturate. Continuous monitoring of the surface potential after switching off the bias shows that a complete relaxation of the excess band bending requires about 800 s. Drain current transient measurements show that the collapse and recovery of the drain current also occur on similar time scales. This correlation between time scales indicates that the accumulation of excess charge near the gate edge causes current collapse by depletion of the channel. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1867553]

Nitride field effect transistors are expected to yield high output power at high frequencies,[1] but currently power output from such devices is much lower than expected. It has been reported that radio-frequency excitation causes the drain current to drop below the steady-state values.[2,3] There have been indications that the trapped charge on the surface,[3–5] in the AlGaN barrier[6] or in the high resistivity buffer[7] are likely to be responsible for this anomaly. In this work, we used room-temperature scanning Kelvin probe microscopy (SKPM) and drain current transient measurements to study the correlation between surface potential variations between the gate and drain and current anomalies in a heterostructure field effect transistor (HFET). SKPM enables the measurement of surface potential with nanometer-scale resolution in a few milliseconds. During an applied bias, if there is any charge trapping in the surface states or in the deep levels within the barrier, the surface band bending will change and lead to a change in the surface potential. Using this method to sense the surface potential in a HFET, we find that the current collapse and recovery of the device can be attributed to the accumulation and relaxation of excess charge near the gate on the drain side.

The $Al_{0.25}Ga_{0.75}N/GaN$ heterostructure used in this study was grown by organometallic vapor phase epitaxy on sapphire. The undoped barrier and buffer layers were 25 nm and 3 μm thick, respectively. The room-temperature Hall mobility of the sample was 400 $cm^2/V\,s$. For the source and drain ohmic contacts, Ti/Al/Ti/Au (30 nm/100 nm/30 nm/15 nm) metallization was deposited using electron-beam (for Ti) and thermal evaporation. The contacts were annealed at 900 °C for 60 s by rapid thermal annealing in nitrogen ambient. The gate contacts were formed by depositing Ni/Au (30 nm/75 nm) metallization. The device had a gate leakage current of 12 μA at 10 V reverse bias between the gate and drain.

Drain current transients of the HFET under study were measured by applying biases from a pulse generator with a few ns rise and fall times. To measure the drain current, a digital oscilloscope was used to record the voltage drop across a 100 Ω resistor connected between the source and ground. Fig. 1(a) shows that after applying a −1 V gate and 7.5 V drain bias, the potential drop across the 100 Ω resistor decreases slowly. The drain current in Fig. 1(a) collapses by 20% in approximately 30 s to reach the steady-state value of Fig 1(b). We then applied −4 V pulses to the gate (10 ms on time, 150 ms off time) superimposed on the previous bias (gate −1 V, drain 7.5 V). The trace in the inset in Fig. 1 shows that the drain current during the 150 ms time when the −4 V bias is off is 12% less then the steady-state value of Fig. 1(b), indicating an additional current collapse due to the superimposed pulsed bias. After turning off the −4 V reverse bias pulses, the drain current recovers [Fig. 1(c)] in about 40 s to the level of Fig. 1(b). If we momentarily set both the

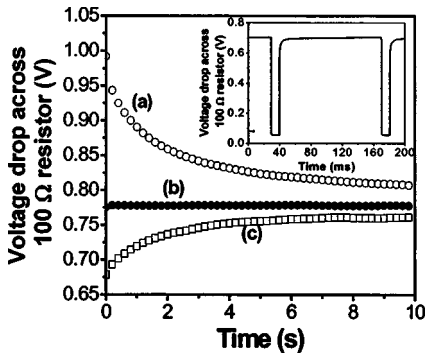

FIG. 1. Drain current transients due to different biases. **(a)** Current collapse with bias on (gate: −1 V, drain: 7.5 V, source: 0 V). **(b)** Steady state after 30 s. **(c)** Drain current recovery after turning off superimposed pulsed bias. **Inset**: Additional current collapse due to superimposed pulsed bias (gate: −4 V, 10 ms on, 150 ms off).

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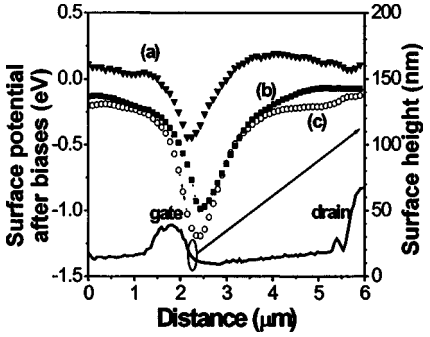

FIG. 2. Surface potential traces between the gate and drain taken within 1 s of turning off biases of different magnitudes. **(a)** gate: −5 V, drain and source: 0 V; **(b)** gate: −9 V, drain and source: 0 V; and **(c)** gate: −1 V, drain: 7.5 V, source: 0V. (The role of dc bias conditions on surface charge accumulation is shown here.)

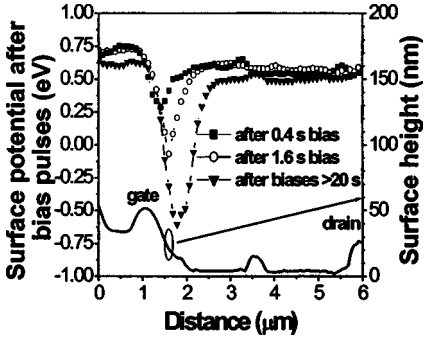

FIG. 3. Surface potential traces between the gate and drain taken within 1 s of turning off biases of different durations. (The time of accumulation and saturation of surface charge is shown here.)

gate and drain potential to 0 V and then reapply the bias, we find that the drain current level is almost the same as that in Fig. 1(b). The gate and drain potentials had to be held at 0 V for over 700 s before reapplying the bias to observe a drain current transient that would start at a level similar to the beginning of the transient of Fig. 1(a).

Turning our attention to surface charge, SKPM was employed to measure the surface potential between the gate and drain for various applied voltages. The SKPM probe can map surface potential with a spatial resolution of about 50 nm along the 4 μm spacing between the gate and drain. To understand the surface potential variations due to biases, three different bias conditions were selected: [Fig. 2(a)] gate: −5 V, drain and source: 0 V; [Fig. 2(b)] gate: −9 V, drain and source: 0 V; and [Fig. 2(c)] gate: −1 V, drain: 7.5 V, source: 0 V. Each of these direct current (dc) biases was applied for 5 min from the pulse generator. The surface potential traces were recorded (Fig. 2) on a straight line from the gate to drain within 1 s of turning off the bias voltages. It was found that from the edge of the gate toward the drain for about 1 μm the amplitude of the surface potential was more negative, i.e., band bending was higher. Figures 2(a)–2(c) show the changes in surface potential near the gate for the three bias conditions indicated earlier, respectively. This figure shows that a higher reverse bias across the gate-drain terminals, as in Fig. 2(b) compared to Fig. 2(a), causes a larger band bending. The cause of the increased band bending is an increase of trapped electrons near the surface. Electrons can be trapped in surface states or in deep levels within the barrier. The source of these electrons can be the gate through tunneling or the channel by hot electron injection.[8] To understand the relative roles of these two processes, we compared the surface potential profiles obtained after applying biases (b) and (c). For bias (b), no drain current was flowing through the device so that no hot carrier injection was possible. For bias (c), the drain current was 10 mA. For both biases, the reverse bias between the gate and drain was similar. After each of these biases, the maximum change of surface potential was about −1 eV. As shown in Fig. 2, the surface potential profile after bias (c) [in Fig. 2(c)] is similar to that observed after bias (b) [in Fig. 2(b)]. The drain current flowing for bias (c) therefore did not noticeably affect the surface potential. This indicates that electron tunneling from the gate is responsible for the observed surface charging phenomena.

In order to find the rate of excess charge accumulation, reverse bias pulses of −9 V were applied to the gate for 0.4, 1.6, 10, 20, 30, 50, and 100 s with the drain and source terminals held at 0 V. The surface potential was mapped within 1 s of turning off the bias. Figure 3 shows that surface charging is a rather slow process taking seconds. A 20 s bias appeared to saturate the surface charging, since the surface potential traces for biases of longer durations were similar. To find the rate at which the excess surface charge disappears, we applied a −9 V bias to the gate with a drain and source voltage of 0 V for 5 min. After turning off this bias, we monitored the surface potential between the gate and drain in successive scans by disabling the slow scan axis. Figure 4 shows that the increased band bending relaxes very slowly, requiring about 800 s to reach the steady-state condition with no excess band bending near the gate edge.

These observations about the surface potential can now be related to the drain current behavior of the device. Figure 2 shows that an applied bias to the device causes charge to be trapped near the gate. Figure 3 indicates a saturation time for this charging of ~20 s, and Fig. 4 shows that discharge of the excess charge is a very slow process taking hundreds of seconds. We can combine these observations to explain the current collapse and recovery of Fig. 1. The gradual decrease of drain current in Fig. 1(a) is because of a slow increase of trapped electrons near the gate. The time it takes for the drain current in Fig. 1(a) to reach its steady-state value is 30 s, which is comparable to the time required for achieving maximum band bending in Fig. 3 (20 s). With regard to current recovery, it takes 700 s for the drain current to recover fully. Similarly, Fig. 4 shows that excess band bending after the −9 V gate reverse bias takes 800 s to relax. The comparable

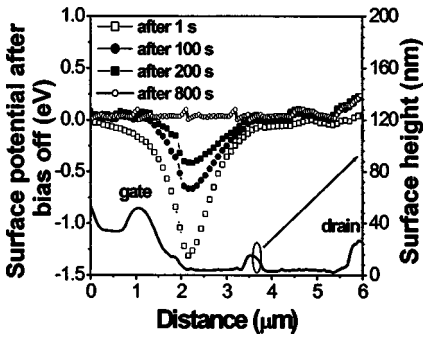

FIG. 4. Surface potential traces between the gate and drain at different times after turning off a −9 V gate reverse bias. (The relaxation rate of excess band bending due to a bias is shown here.)

time scales observed for the drain current behavior and surface charging indicate that the excess band bending near the gate is very possibly related to the drain current level. If we assume that all of the excess charge is on the AlGaN surface and use $\Delta V_{\text{surface}} = Q_s(d/\varepsilon_{\text{AlGaN}})$, where d and $\varepsilon_{\text{AlGaN}}$ are the thickness and the dielectric constant of the AlGaN barrier layer, respectively, a surface charge concentration of about 2×10^{12} cm^{-2} is obtained. This charge should cause a larger drop in the drain current than the 20% reduction observed. Nevertheless, the increase of band bending definitely indicates depletion of the channel and therefore reduction of the drain current. In each of the 10 ms durations of the −4 V bias pulses, shown in the inset of Fig. 1, more electrons are able to tunnel from the gate and be trapped. Discharge of this excess charge was not complete in the 150 ms time when the −4 V pulse was absent. As a result, there was a net increase of the accumulated charge near the gate edge. This caused the drain current level in the 150 ms periods in the inset of Fig 1 to be lower than the steady state value corrosponding to the trace (b) of Fig. 1. One well-known manifestation of current collapse in nitride HFETs is a decrease of gain with the increase of radio-frequency gate drive.[3] During each negative excursion of the radio-frequency gate drive, the reverse bias between the gate and drain becomes higher. This higher reverse bias enables a larger number of electrons to tunnel. All of this excess charge does not dissipate in the duration of the positive half-cycle of the gate drive. As a result, there is a net increase of accumulated charge near the gate edge because of the large gate drive. A larger input drive therefore results in a larger accumulation of charge, and thus a larger current collapse or gain degradation.

In conclusion, the measurement of the surface potential between the gate and drain immediately after turning off an applied bias shows that band bending increases near the gate. This increase of band bending, caused by an increase of trapped electrons near the surface, depletes the channel. Since the surface potential trace observed after a bias that causes no current flow through the device was similar to that of a bias that does, the likely source of the electrons is tunneling from the gate. The time needed for saturation of the excess charge accumulation, as deduced from surface potential traces observed after different durations of the same reverse bias, is comparable to the time of current collapse. Complete relaxation of the excess band bending due to an applied bias takes hundreds of seconds, which also compares well to the time required for drain current recovery. From these correlations, we conclude that current collapse in the device under investigation is caused by the accumulation of excess charge near the gate edge on the drain side.

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