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Room-temperature single-electron charging in electrochemically synthesized semiconductor quantum dot and wire array

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Cylindrical quantum dots of diameter ~8 nm and height 3–10 nm, and wires of diameter 50 nm and height 500–1000 nm, were self-assembled by electrodepositing semiconductors in the nanometer-sized pores of anodic alumina films. Current–voltage characteristics of both wires and dots show Coulomb blockade at room temperature, while the wires also show a Coulomb staircase when exposed to infrared radiation. These results establish that electrochemical self-assembly is a viable technique for producing nanostructures that have potential uses in room-temperature single electronics. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1458683]

Anodic alumina films containing ordered arrays of nanopores are widely used for self-assembling two-dimensional arrays of semiconductor quantum dots and wires of uniform diameter.[1] The semiconductor of choice is simply electrodeposited into the pores to create either dots or vertical wires in an insulating matrix (alumina). Electrical access to the dots or wires are established by following a sequence of steps described in Ref. 2. This synthesis technique is simple, inexpensive, and has a rapid throughput.

In this letter, we present results from transport measurements in electrochemically self-assembled dots and wires showing room-temperature single-electron charging effects. This opens up the possibility of substituting fine line nanolithography with electrochemical self-assembly in the manufacturing of *some* single electronic devices.

Electrochemical self-assembly consists of basically three steps: (i) electropolishing an aluminum foil in a suitable electrolyte to clean and prepare the surface, (ii) anodizing the electropolished foil in either sulfuric or oxalic acid with a dc current to form a porous alumina film on the surface, and finally, (iii) electrodepositing the material of interest within the pores. When the anodization is carried out in sulfuric acid, the pore diameter is about 8 nm (and the areal pore density is $\sim 10^{11}$ cm^2),[3] whereas for oxalic acid based anodization, the pore diameter is 50 nm (with a pore density of $\sim 10^{10}$/cm^2). An atomic force micrograph of the top surface of a porous film produced by anodization in oxalic acid is shown in Fig. 1.

We electrodeposited two different compound semiconductors within the pores: CdS and ZnSe. CdS was electrodeposited within 8 nm pores in thin alumina produced by few seconds of anodization in sulfuric acid, while ZnSe was electrodeposited within 50 nm pores in much thicker alumina produced by a few minutes of anodization in oxalic acid. The CdS electrodeposition was carried out for 10 s so that *dots* of height 3–10 nm (and diameter 8 nm) were formed, whereas ZnSe was electrodeposited for 2 min resulting in cylindrical wires of 0.5–1 μm height and 50 nm diameter. The electrodeposited structures are *buried* in the porous alumina film; their tips neither stick out of the surface for contacting, nor are their bottoms electrically accessible because of a barrier alumina layer that separate the bottom from the aluminum substrate. Electrical access to the dots or wires can be established by carefully etching away a top alumina layer to expose the tips of *some* of the wires/dots (the wires/dots have different lengths so that not all of them are exposed), and then removing the alumina barrier layer from the bottom as well following a sequence of steps described in Ref. 2. Finally, those very few wires that are exposed at both ends can be contacted with gold contacts. The process of electrodepositing ZnSe and CdS inside the pores and making electrical connections to them has been described in detail in Ref. 2.

Electrodeposited structures have been characterized in the past with high resolution transmission electron microscopy (TEM). We found that while structures electrodeposited in ~8 nm pores tend to be mostly single crystal, long wires in 50 nm pores (such as the ZnSe wires) are composed of

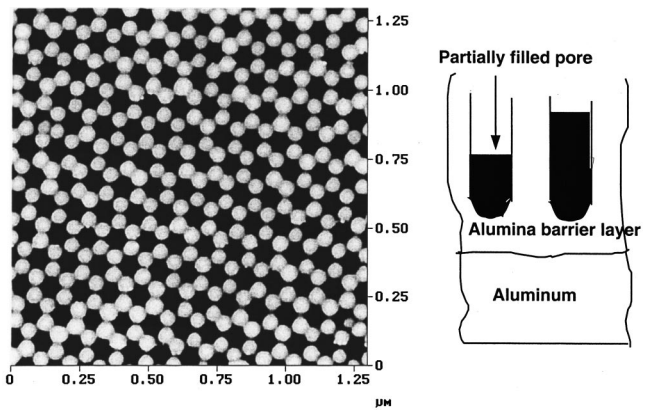

FIG. 1. (Left) Atomic force micrograph of a porous alumina film produced by anodization of aluminum in oxalic acid. The dark areas are the pores and the surrounding white areas are alumina. The average pore diameter is 50 nm. (Right) Cross section view of partially filled pores showing the ''barrier layer'' at the interface with aluminum. Note that the wires are ''buried;'' their tops do not stick out of the surface.

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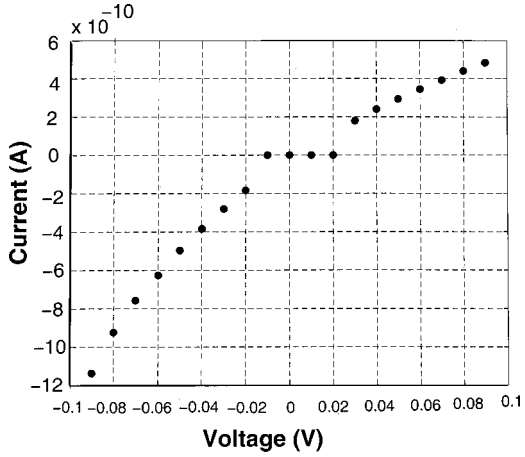

FIG. 2. $I-V$ characteristic of CdS quantum dots (8 nm diameter and 3–10 nm height) showing a Coulomb blockade region of 0.3 V asymmetrically straddling the origin. The blockade voltage V_b is estimated to one half of this voltage, or 0.15 V.

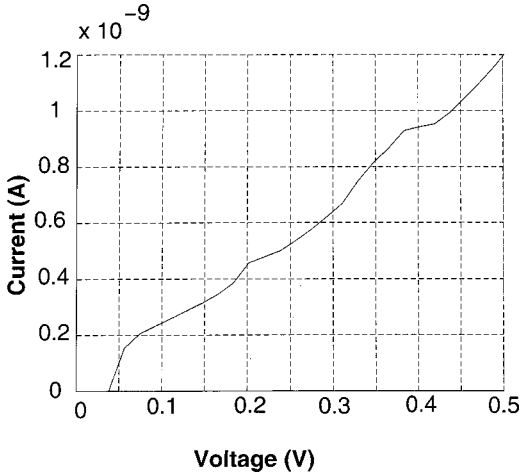

FIG. 3. $I-V$ characteristic of ZnSe quantum wires, consisting of a one-dimensional array of 50 nm grains, measured in the dark. There is a Coulomb blockade, but no discernible staircase.

grains separated by amorphous regions.[4] Electron transport in the ZnSe wires probably takes place by tunneling from grain to grain through the intervening amorphous regions that act as potential barriers or weak links. In the past, there have been reports of forming weakly linked grains in electrodeposited silver nanowires by applying a voltage pulse that melted filaments connecting adjacent grains.[5] These structures showed Coulomb staircase at 80 K temperature. Our ZnSe nanostructures are very similar. We do not need to apply voltage pulses to melt filaments connecting ZnSe grains since the amorphous regions are already highly resistive (amorphous semiconductors have a much higher resistivity than crystalline semiconductors). Like the structures in Ref. 5, our structures can be viewed as a one-dimensional array of tunnel junctions. Such arrays are known to have interesting single-electron charging properties.[6]

Current–voltage ($I-V$) characteristics of both CdS dots and (granular) ZnSe wires were measured using a HP4140B meter at room temperature. The CdS dot results are shown in Fig. 2. The measured resistance (in the quasilinear part of the characteristic) exceeds 10^8 ohms which indicates that only *very few* dots or wires are actually contacted by the contacts. This is expected since the pores are filled to various depths in the electrodeposition process so that only very few of them can be exposed at both ends and made to contact the Au pads.

The unevenness of pore filling—which is a characteristic feature of electrodeposition—is actually a fortuitous happenstance. In fact, it makes the observation of single-electron charging effects possible. The actual contact area of the Au contacts in our experiments is about $1\ \text{mm}\times 1\ \text{mm}$ which means that 10^8-10^9 nanostructures are under the contacts. If they all made electrical connection to the contacts, then the total capacitance of all these parallel capacitors would have been too large to allow the observation of single-electron effects at any reasonable temperature, let alone room temperature. Fortunately, very few nanostructures are contacted (it turns out that one in a hundred million is contacted at both ends—see later calculation) which keeps the total capacitance between the contacts low enough to allow the observation of single-electron charging effects.

From the measured Coulomb blockade voltage V_b of 0.015 V in the case of the dots, we estimate a total capacitance of $C_T=e/2V_b=5.4$ aF between the contacts. If we view the dots as parallel plate capacitors, then the capacitance of a single dot is $C=\epsilon A/d$ (where A is the dot surface area, ϵ is the permittivity, and d is the height). Given that for CdS, $\epsilon=5.4\times 8.854\times 10^{-12}$ F/m (Ref. 7) $A=8\ \text{nm}\times 8\ \text{nm}$ and $d=3-10$ nm, we estimate that $C=3-10\times 10^{-19}$ F. Thus, $C_T/C=5-20$. Therefore, approximately 5–20 dots are contacted by the Au contacts. This translates to about one in a hundred million dots being contacted!

The contacting of such a small fraction of the dots reproducibly is of course difficult. We have to control the etching of the top surface of alumina in phosphoric acid very carefully so as to neither underetch (in which case no dot is exposed and we cannot measure any detectable current), nor overetch (in which case too many dots are exposed and we see no Coulomb blockade). The etching must be carried out at room temperature in phosphoric acid (or at very slightly elevated temperature) so as to keep the etch rate very small and controllable. If this process can be standardized to the point where it is well controlled and completely repeatable, it will be a significant technological advance since then it will essentially obviate the need for nanocontacts (which are difficult to make) or the need for alignment schemes with nanometer scale precision which exist only in very few laboratories in the world.

An interesting feature in the data is that the measured blockade voltage V_b of 0.015 V is actually less than the room-temperature thermal voltage of 0.025 V. Yet, the blockade is quite distinct at room temperature (we cannot measure the blockade at 77 K because of carrier freeze out which makes the current too low, less than 10 fA, which is below our equipment sensitivity). In quantum dots, the discreteness of the energy levels due to quantum confinement aids the Coulomb blockade, making room-temperature observation possible. Room-temperature Coulomb blockade has been observed in the past, for example, in metallic clusters of ~4 nm diameter[8,9] and in molecular clusters;[10] hence, this is not very surprising.

The $I-V$ characteristics of the ZnSe wires are shown in

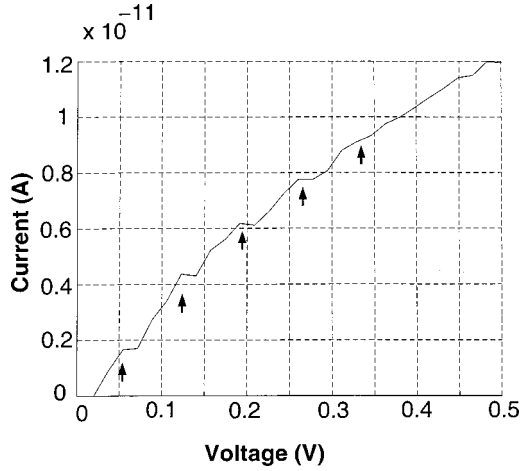

FIG. 4. $I-V$ characteristic of ZnSe quantum wires, consisting of a one-dimensional array of 50 nm grains, measured in infrared radiation. There is a distinct Coulomb staircase in addition to the Coulomb blockade. The conductance of the wires goes down by a factor of ~100 when illuminated with infrared radiation. This effect is believed to be caused by real space transfer of electrons from the wires to the surrounding alumina (see Ref. 3).

Fig. 3. When the characteristics are measured in the dark (Fig. 3), we observe a Coulomb blockade but no discernible staircase. The blockade voltage V_b is 0.0375 V and that is equal to $Ne/2MC$ where M is the number of wires contacted by the Au contacts, N is the number of junctions (one less than the number of grains) in series in an average wire, and C is the average junction capacitance between two neighboring grains. The average grain radius r is approximately 5 nm (estimated from high resolution TEM) and the separation between neighboring grains t is about 1 nm. Using a formula appropriate for grains[11] $C=\epsilon r(1+r/2t)$, we estimate an average junction capacitance C of 1 aF. The number of grains N in an average wire is 500–1000 nm/5 nm=100–200. Using these values in the expression for the blockade voltage yields a value of $M=200-400$. Thus, only 200–400 wires are contacted. This is somewhat larger than the number of CdS dots estimated to have been contacted by the Au contacts, but still not significantly larger. At first sight, this may appear surprising since one might think that many more wires should make electrical contact with the Au pads, than dots, since the wires are much longer. However, in reality, the host film for the ZnSe wires is much thicker than the host film for the CdS dots. Therefore, even though the ZnSe ''wires'' are much longer than the CdS ''dots,'' only about 10–20 times as many wires as dots reach the Au contact.

When the $I-V$ characteristics of the ZnSe wires are measured in the presence of infrared radiation generated by the glowbar of a BOMEM Fourier transform infrared (FTIR) equipment, distinct steps are seen in the characteristic (Fig. 4). It is tempting to attribute them to phase locking of single-electron tunneling (SET) oscillations in a one-dimensional array,[12] but a closer examination reveals that this is not the case. First, the observed stair edges are periodic in voltage, not current. Second, from the relation $I=nef$ ($I=$current, $n=$an integer, and $f=$frequency of radiation), it is obvious that the frequency for SET oscillations is in the microwave range, not infrared.

According to the orthodox theory of single electronics, one-dimensional arrays will exhibit the normal Coulomb staircase due to space correlation of single-electron tunneling events if the array is inhomogeneous (i.e., the junction capacitances/resistance are different for different grains).[13,14] Therefore, we are led to conclude that the infrared radiation somehow promotes this inhomogeneity.

It is well known that single-electron tunneling events are very sensitive to the electromagnetic environment.[15] The electromagnetic radiation can significantly effect the tunneling impedance due to inelastic processes. Thus, it can make the junction resistances of different junctions markedly dissimilar thereby promoting inhomogeneity and making the steps more distinct.

Another possibility is that infrared absorption causes real space transfer of electrons from the semiconductor to the surrounding alumina layer.[2] This not only increases the resistance of the wires by two orders of magnitude (as seen by us in previous experiments),[2] but it also changes the background charge distribution and hence alters the effective capacitances between grains. This could also lead to increased asymmetry between junctions and make the steps more prominent.

In conclusion, we have shown the existence of single-electron charging effects at room temperature in electrochemically synthesized nanostructures. These structures provide a convenient vehicle for the study of single electronics and could offer a viable inexpensive platform for device applications.

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