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# Degradation and phase noise of InAlN/AlN/GaN heterojunction field effect transistors: Implications for hot electron/phonon effects

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$In_{15.7\%}Al_{84.3\%}N$/AlN/GaN heterojunction field effect transistors have been electrically stressed under four different bias conditions: on-state-low-field stress, reverse-gate-bias stress, off-state-high-field stress, and on-state-high-field stress, in an effort to elaborate on hot electron/phonon and thermal effects. DC current and phase noise have been measured before and after the stress. The possible locations of the failures as well as their influence on the electrical properties have been identified. The reverse-gate-bias stress causes trap generation around the gate area near the surface which has indirect influence on the channel. The off-state-high-field stress and the on-state-high-field stress induce deterioration of the channel, reduce drain current and increase phase noise. The channel degradation is ascribed to the hot-electron and hot-phonon effects. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4751037]

$In_xAl_{1-x}N$-barrier GaN-channel heterojunction field effect transistors (HFETs) are candidates for next generation high-power and high-frequency amplifiers.[1] Device performance reported by several groups indicates large current density[2] and large output power density.[3] There are also few reports dealing with degradation mechanisms, and efforts have been made to discern the location of degradation,[4] as well as to delineate the noise sources.[5] However, further studies on the effect of stress on electrical properties, especially on noise characteristics, are still needed. Previously, stress under different bias points has been applied to study the impact of various effects on the degradation of AlGaN/GaN HFETs through the technique of low frequency noise.[6] Since the InAlN barrier can be lattice-matched to the GaN buffer in InAlN/GaN based HFETs, the inverse-piezoelectric effect is expected to be smaller than that in AlGaN/GaN HFETs.[7] Besides, the much larger current density in InAlN/GaN HFETs will impose a more critical issue due to the stronger hot-electron, hot phonon (non-equilibrium optical phonon), and self-heating (excess acoustic phonon) effects. In this letter, we used DC as well as phase noise[8] technique to investigate the degradation of InAlN/GaN HFETs under four different electrical stress conditions to attain a deeper understanding on the mechanisms and locations of the degradation as well as the correlation between the degradation and phase noise.

The $In_{15.7\%}Al_{84.3\%}N$/AlN/GaN HFET structures were grown by metalorganic chemical vapor deposition on *c*-sapphire substrates covered with 250 nm-thick AlN initiation layers. The structures are comprised of a 2-$\mu$m-thick undoped GaN layer followed by a 1-nm-thick AlN spacer, a 20-nm-thick nominally undoped $In_xAl_{1-x}N$ ($x = 15.7\%$) barrier, and a 2-nm-thick GaN cap layer. The source and drain contacts were formed using standard photolithography with Ti/Al/Ni/Au (30/100/40/50 nm) metal stacks annealed at 800 °C. Mesa isolation was performed using a SAMCO inductively coupled plasma system with Cl-based chemistry. Gate electrodes were formed by deposition of Pt/Au (30/50 nm). The gate length, the gate width, and the source-drain spacing are $L_g = 2.0\ \mu$m, $W_g = 90\ \mu$m, and $L_{sd} = 7\ \mu$m, respectively. The devices are not passivated. A schematic description of the HFET structure is presented in Fig. 1.

The four bias points employed here are (1) on-state-low-field stress ($V_{GS} = 0$ V, $V_{DS} = 6$ V), (2) reverse-gate-bias stress ($V_{GS} = -20$ V, $V_{DS} = 0$ V), (3) off-state-high-field stress ($V_{GS} = -10$ V, $V_{DS} = 20$ V), and (4) on-state-high-field stress ($V_{GS} = 0$ V, $V_{DS} = 20$ V). An ensemble of the HFET devices on the same wafer has been studied, and the results from a representative device for each bias point are presented here. Each stress test started with an initial 5 h stress, and then followed by another 20 h stress. The dc transfer characteristics and phase noise were measured before and one day after each stress test. If there were any shifts of pinch-off voltage ($V_{th}$) after stress, the transfer characteristics were adjusted by an amount equaling the shift of $V_{th}$ as it was done in Ref. 9. The gate bias during off-state-high-field stress was chosen to be smaller than the pinch-off voltage ($V_{th} \sim -8$ V) to ensure that the channel is fully depleted in

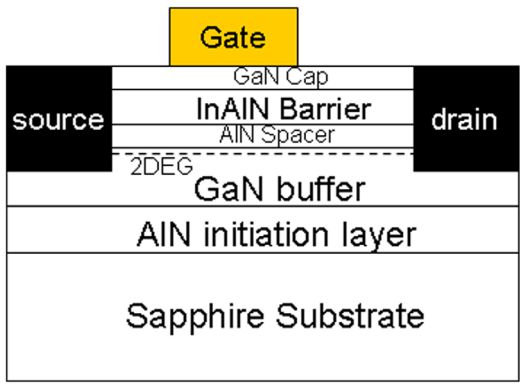


FIG. 1. Schematic diagram of the InAlN/AlN/GaN HFET structure used for electrical stress experiments.

 

case of slight variations in the pinch-off voltage during electrical stress. The noise-spectra-density (NSD) of HFETs can be expressed as[10]

$$\mathrm{NSD} = \frac{A}{f^{\gamma}} + \frac{\sum_i B_i \tau_i}{1 + (2\pi f)^2 \tau_i^2}, \quad (1)$$

where $\tau_i$ and $B_i$ are the time constant and trap concentration, respectively, of traps located at different discrete energy levels, and $\gamma$ is a constant which nearly equals 1. The constant $A$ characterizes either the mobility fluctuations or number fluctuations from continuous trap spectrum, or both processes acting together.[11]

The results for the on-state-low-field stress are demonstrated in Figs. 2(a) and 2(b), where the NSD shows a $1/f^{\gamma}$ shape. The extracted Hooge parameters were on the order of $10^{-4}$, which were comparable to AlGaN/GaN based HFETs.[12] The change in NSD was not discernible even after 25 h of stress, and the drain current shows little change as well. The effects due to the reverse-gate-bias stress are illustrated in Figs. 3(a) and 3(b). The drain current showed little change for the first 5 h stress and a ~5% change after the 25 h stress (Fig. 3(a)). A double peak feature appeared in the $g_m$ plot after 5 h of stress and became more apparent after the 25 h stress. This effect is very similar to the kink effect usually ascribed to hot-electron injection into donor-like traps followed by subsequent field-assisted de-trapping under high electric field.[13] Thus, most likely the hot electrons generated traps in the barrier layer around the gate since only the gate area was affected under corresponding stress condition. The influence was also observed in the noise measurement as demonstrated in Fig. 3(b), where the generation–recombination (G–R) peak below 1 kHz in the pristine devices diminished after the 25 h stress. A plausible explanation can be as follows: deep traps were generated during the stress around the gate area, they rendered the pre-existing shallow donor-like traps inaccessible for electrons and caused the observed reduction of the G–R peak intensity in NSD below 1 kHz.[14] The created deep traps should be temporarily stable or equivalently have a very large time constant, thus they would not be reflected in the NSD spectrum

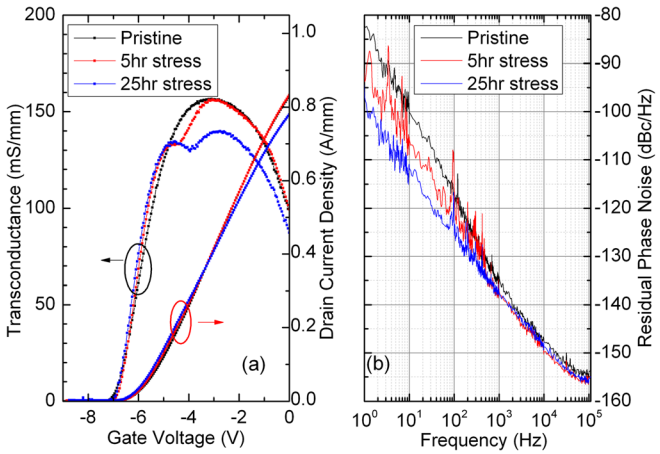


FIG. 3. Effect of reverse-gate-bias stress on (a) *I-V* and transconductance measured at $V_{DS} = 6$ V and (b) phase noise measured at $V_{GS} = 0$ V, $V_{DS} = 6$ V.

which covers from 1 Hz to 100 kHz. For frequencies not influenced by this G–R peak, i.e., above 1 kHz, the NSD remained the same, which meant that the $A$ parameter in Eq. (1) does not change under the reverse-gate-bias stress condition.

In contrast to the above two stress conditions, the off-state-high-field stress exhibited a noticeable reduction in the drain current and an increase in NSD (Figs. 4(a) and 4(b)). And the most damaging stress condition is the on-state-high-field stress as demonstrated in Figs. 5(a) and 5(b), where the drain current permanently decreased to ~25% of the original value and the NSD increased by about 25-30 dBc/Hz after the 25 h stress. One common feature for these two stress condition is that the $g_m$ degradation is most pronounced near the $g_m$ peak rather than at $V_{gs}$ bias points closer to zero volt, thus the major degradation is associated with the decrease of channel conductivity instead of the increase in the drain access resistance $R_d$ caused by the electron trapping in the gate–drain access region.[15] This assertion is consistent with the change of channel resistance $R_{ch}$ and drain access resistance $R_d$ after stress, where the increase of $R_{ch}$ takes around 70% of the total increase of source-drain resistance (the method for the resistance measurement is described in Ref. 16).

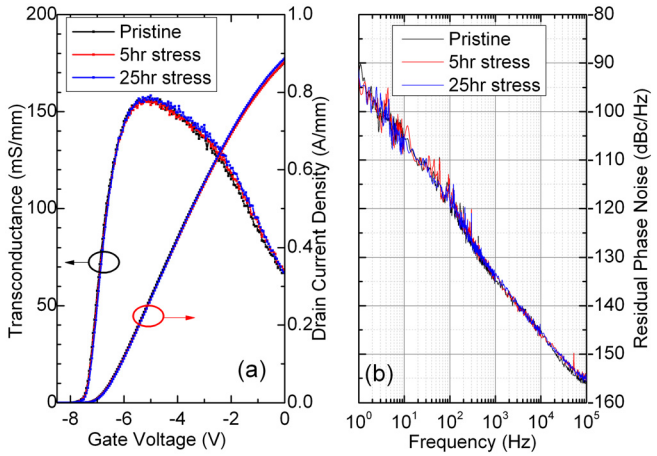


FIG. 2. Effect of on-state-low-field stress on (a) *I-V* and transconductance measured at $V_{DS} = 6$ V and (b) phase noise measured at $V_{GS} = 0$ V, $V_{DS} = 6$ V.

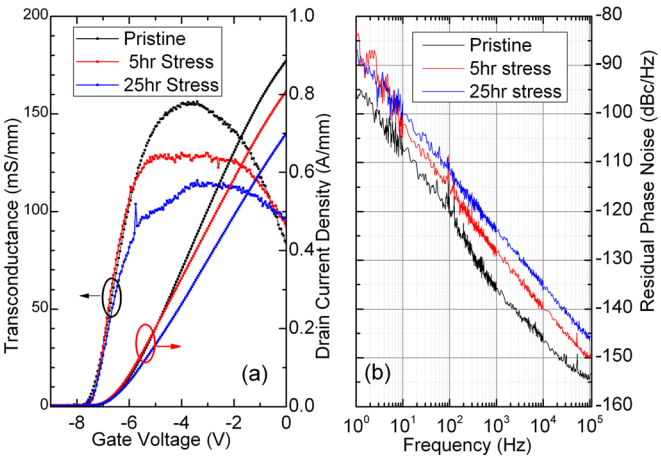


FIG. 4. Effect of off-state-high-field stress on (a) *I-V* and transconductance measured at $V_{DS} = 6$ V and (b) phase noise measured at $V_{GS} = 0$ V, $V_{DS} = 6$ V.

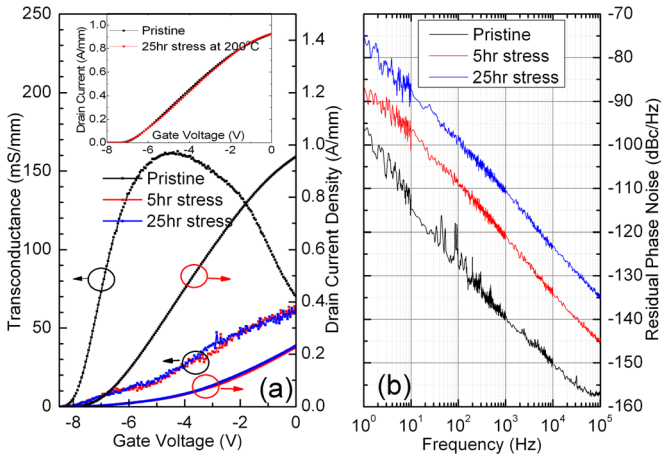


FIG. 5. Effect of on-state-high-field stress on (a) *I-V* and transconductance measured at $V_{DS} = 6$ V (the inset shows the drain current density before and after 25 h on-state-low-field stress at 200 °C) and (b) phase noise measured at $V_{GS} = 0$ V, $V_{DS} = 6$ V.

The results of Figs. 2(a) and 2(b) demonstrate that the electrical properties of the devices show no change after the on-state-low-field stress. Consequently, the channel self-heating effect due to the drain current at moderate drain bias is not likely to cause any degradation in the channel. The excess acoustic phonon temperature under the on-state-high-field stress is expected to be around 219 °C higher than that under the on-state-low-field stress if we assume a thermal resistance of around 27.3 °C mm/W.[17] In order to isolate the effect due to excess acoustic phonons from the on-state-high-field stress, an ensemble of pristine devices was stressed under on-state-low-field stress at 200 °C to test the heating effect only. No permanent degradation of drain current was observed (inset of Fig. 5(a)), which is consistent with the known good thermal reliability of InAlN/GaN based HFETs.[18] Thus, the large degradation under on-state-high-field stress cannot be attributed to the self-heating effect caused by the excess acoustic phonons. The reverse-gate-bias stress and the associated piezoelectric effect can cause damage to the barrier layer and change the drain current by depleting the 2-dimensional-electron-gas (2DEG) in the channel.[19] However, the change in the drain current predominantly results from a shift of the pinch-off voltage in our experiments. Indeed, Fig. 3(a) demonstrates a very small change in the drain current after correcting for the pinch-off voltage. Thus, the degradation is limited to the barrier layer, and moreover, most probably near the surface area far away from the channel, which can have only an indirect influence on the channel properties. This assertion is plausible since the remote ionized impurity scattering will cause minor effect on the mobility of the 2DEG for a typical barrier thickness of 20 nm,[20] particularly at room temperature and above. This is also confirmed by the NSD results since the *A* parameter shows no change after the reverse gate bias stress as discussed above.

The channel degradation induced by the off-state-high-field stress is evidenced through the drain current and the NSD. The degradation is possibly caused by the electrons leaking along the channel through the depleted high-field area. Due to the high source–drain voltage, these electrons are hot and can cause direct damage in the channel, i.e., through the generation of trap states in the channel. This in turn causes a reduction of channel conductivity and increase of the NSD. This is also consistent with the high degradation rate for the on-state-high-field stress considering the large amount of the hot-electrons in the channel compared to that of the off-state-high-field stress condition. Also, the large amount of hot-electrons in the channel will induce high density of hot phonons and the resultant strong hot-phonon effect,[8,21] which can speeds up the degradation. The increase of the *A* parameter in the NSD exclusively correlated with the reduction of the drain current as demonstrated by the on-state-high-field and off-state-high-field stress, thus the increase of noise should directly relates to the increase of $R_{ch}$ caused by channel degradation and/or increase of $R_d$ by electron trapping in the gate-drain access region. Considering the *A* parameter in NSD did not change after the reverse-gate-bias stress, the increase of noise under the off-state-high-field stress and the on-state-high-field stress most likely comes from the increase of $R_{ch}$ due to the channel degradation instead of the increase of $R_d$ caused by electron trapping in the gate-drain access region. Although passivation could reduce surface trapping at the gate-drain access region and therefore alleviate the increase in $R_d$, it would not impact the conclusions presented here as reliability was found to be limited mainly by channel degradation.

Electric stress for InAlN/AlN/GaN HFETs at four different bias conditions has been conducted to probe various degradation mechanisms and their impact on the phase noise performance. The location and nature of the degradation have been correlated with the observed *I-V* and NSD data. Data in aggregate are consistent with the assertion that the dominant degradation is due to the hot-phonon and hot-electron effects, where the primary degradation location is in the channel. The channel deterioration is shown to decrease the channel conductivity and cause almost frequency-independent increase of the NSD. The physical nature of the degradation is still unknown, which is subject to further investigation.

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