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C. Y. Zhu
Virginia Commonwealth University

F. Zhang
Virginia Commonwealth University

Romualdo A. Ferreyra
ferreyrara@vcu.edu

U. Ozgur
Virginia Commonwealth University, uozgur@vcu.edu

Hadis Morkoç
Virginia Commonwealth University, hmorkoc@vcu.edu

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Degradation in AlGaN/GaN heterojunction field effect transistors upon electrical stress: Effects of field and temperature

C. Y. Zhu, F. Zhang, R. A. Ferreyra, V. Avrutin, Ü. Özgür, and H. Morkoç
Department of Electrical and Computer Engineering, Virginia Commonwealth University, Richmond, Virginia 23284, USA

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AlGaN/GaN heterojunction field effect transistors (HFETs) with 2 μm gate length were subjected to on-state-high-field (high drain bias and drain current) and reverse-gate-bias (no drain current and reverse gate bias) stress at room and elevated temperatures for up to 10 h. The resulting degradation of the HFETs was studied by direct current and uniquely phase noise before and after stress. A series of drain and gate voltages was applied during the on-state-high-field and reverse-gate-bias stress conditions, respectively, to examine the effect of electric field on degradation of the HFET devices passivated with SiN_x. The degradation behaviors under these two types of stress conditions were analyzed and compared. In order to isolate the effect of self-heating/temperature on device degradation, stress experiments were conducted at base plate temperatures up to 150 °C. It was found that the electric field induced by reverse-gate-bias mainly generated trap(s), most likely in the AlGaN barrier, which initially were manifested as generation-recombination (G-R) peak(s) in the phase noise spectra near 10^3 Hz. Meanwhile electric field induced by on-state-high-field stress mainly generated hot-electron and hot-phonon effects, which result in a nearly frequency independent increase of noise spectra. The external base plate temperatures promote trap generation as evidenced by increased G-R peak intensities.
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AlGaN/GaN heterojunction field effect transistors (HFETs) continue to receive a great deal of attention owing to their remarkable performance in high-frequency/high-power applications.[1] However, there remain some issues regarding their long-term reliability, as confirmed by accelerated stress tests. As in all field effect transistors, the physical location of main degradation and ultimately device failure have been exclusively ascribed to the gate edge by the gate-drain access region where the electric field peaks. One of the popular proposed mechanisms for the degradation is the so-called inverse-piezoelectric effect,[2] which is based on the hypothesis that mechanical strain produced by the high gate-drain voltage induced vertical electric field may aggravate the tensile strain already present owing to the lattice mismatch between the AlGaN barrier and the GaN layer. In this scenario, beyond a critical gate-drain voltage that corresponds to the critical elastic energy of the AlGaN barrier causing lattice damage the HFET devices begin to degrade abruptly. However, permanent degradation was also found to occur even for stresses below that particular critical voltage with sufficiently long stress time for reverse-gate-bias stress, supporting the hypothesis that permanent degradation is due to a defect percolation process.[3] Other proposed degradation mechanisms include hot-electron-induced trap generation,[4] impurity diffusion during the early stages of degradation,[5] oxidation of the device surface,[6] and hot-electron/phonon effects.[7] However, further studies of the effect of stress on electrical properties, especially on noise characteristics, are still needed. Previously, stress under different bias points has been applied to study the impact of various effects on the degradation of nearly lattice-matched InAlN/GaN HFETs using the low frequency noise technique, where the inverse-piezoelectric effect has been demonstrated to be much less important than the hot-electron/phonon effects.[8] However, the behavior in AlGaN/GaN HFETs may be more complicated due to the large strain in pseudomorphically grown AlGaN barrier layer as well as the still relatively large drain current. In this paper, we measure the phase noise and DC characteristics to investigate the degradation mechanisms in passivated AlGaN/GaN HFETs stressed under various bias points encompassing on-state-high-field and reverse-gate-bias and elevated temperatures in an effort to interrogate the various degradation mechanisms.

The AlGaN/GaN HFET structures were grown by metal-organic chemical vapor deposition on *c*-plane sapphire substrates. The structures are comprised of a 100-nm-thick AlN initiation layer followed by 2-μm-thick undoped GaN layer, a 1-nm-thick AlN spacer, a 20-nm-thick unintentionally doped $Al_{0.25}Ga_{0.75}N$ barrier, and a 2-nm-thick GaN cap layer. The source and drain contacts were formed by standard photolithography and Ti/Al/Ni/Au (30/100/40/50-nm-thick) metal stacks annealed at 800 °C for 1 min. Mesa isolation was performed in a SAMCO inductively coupled plasma system using a Cl-based chemistry. Ni/Au (30/50 nm thick) metallization was used for gate electrodes. The gate length, the gate width, and the source-drain spacing are $L_g = 2.0\,\mu$m, $W_g = 90\,\mu$m, and $L_{sd} = 7\,\mu$m, respectively. The devices were passivated with 150-nm-thick SiN_x deposited by plasma enhanced chemical vapor deposition.

Two sets of stress conditions were used to test degradation of HFETs. The on-state-high-field stress conditions were $V_{gs} = 0$, and $V_{ds} = 20$, 24, 27, or 30 V. The reverse-gate-bias stress conditions were $V_{gs} = -10$, -15, -20, -24, -27, or -30 V and $V_{ds} = 0$ V. Devices were stressed for 10 h in air at external base plate temperatures up to 150 °C. An ensemble

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of HFETs devices on the same wafer was chosen for each stress condition, and all showed similar behavior after stress. Therefore, results from representative devices are presented here. The phase noise spectra were measured at a bias condition of $V_{gs} = 0\,V$ and $V_{ds} = 6\,V$ (details on the measurement instrument can be found in Ref. 9).

Fig. 1 shows the phase noise spectra for devices stressed under on-state-high-field at different drain biases. The noise spectrum for the pristine device is representative of typical *1/f* noise that we observe. As can be clearly noted, the devices stressed under the on-state-high-field with $V_{gs} = 0\,V$ and $V_{ds} = 20\,V$ started to exhibit an increase in phase noise (no noticeable change was observed for smaller drain biases) and the noise level increased further consistently for higher stress drain biases of $V_{ds} = 24$, 27, and 30 V. The changes occurred in the form of a frequency independent increase of 1/f noise plus a generation—recombination (G-R) peak in the frequency range of 10^3 to 10^5 Hz. The appearance of the G-R peak can be attributed to the generation of traps after stress.[10] The drain current also showed significant degradation as the drain bias for the on-state-high-field stress is increased (see Fig. 1 inset). After stress at $V_{ds} = 30\,V$, the drain current decreased to nearly 50% of the pristine value for $V_{gs} = 1\,V$ and $V_{ds} = 4\,V$ bias.

The phase noise spectra after reverse-gate-bias stress are shown in Fig. 2. For devices stressed under reverse-gate-biases of $V_{gs} = -10\,V$ and $-15\,V$, the noise spectra as well as drain current (not shown) did not indicate any change. However, when the reverse gate bias was increased to $V_{gs} = -20\,V$, a weak G-R type peak appeared near 10^3 Hz after stress. The intensity and width of this G-R peak increased for devices stressed at larger $|V_{gs}|$, i.e., higher electric field. For sufficiently large $|V_{gs}|$, i.e., $V_{gs} = -30V$, we suggest the presence of several G-R peaks corresponding to different time-constants superimposed on each other, which leads to frequency-independent increase of 1/f noise.

The above results are consistent with other reports, which suggest that the degradation was induced by the

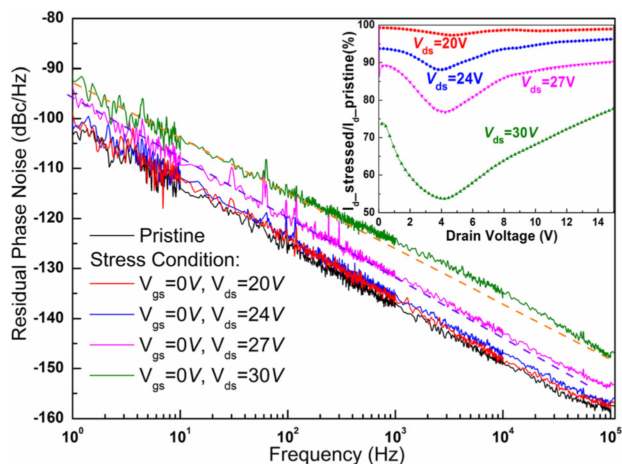

FIG. 1. Phase noise spectra measured at $V_{gs} = 0\,V$ and $V_{ds} = 6\,V$ for pristine devices and devices stressed under on-state-high-field at various drain biases. The inset shows the degradation of drain current after on-state-high-field stress characterized by the ratio of drain current for stressed devices to that in pristine devices. (The drain currents were measured under $V_{gs} = 1\,V$ at various drain biases.) The dashed lines are used as guides for the 1/f noise and to reveal the G-R peaks in the high frequency range.

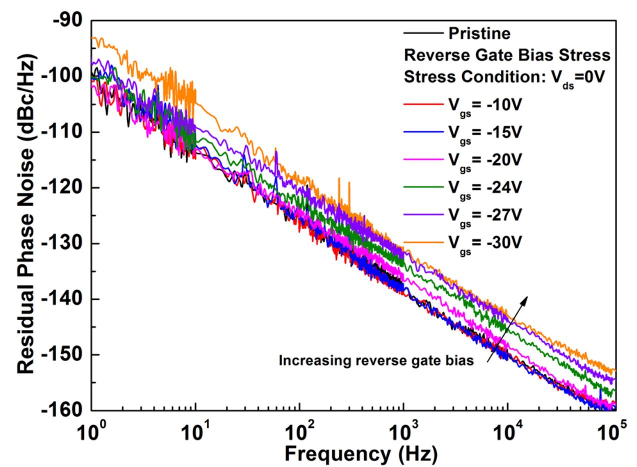

FIG. 2. Phase noise spectra measured at $V_{gs} = 0\,V$ and $V_{ds} = 6\,V$ for pristine devices and devices stressed under different reverse-gate biases.

applied electric field,[11,12] for both on-state-high-field and reverse-gate-bias stress conditions. Electric field simulations using Silvaco Atlas with field dependent mobility model showed that vertical electric field at the gate edge of the drain side induced by reverse-gate-bias stress is ∼10% higher than that induced by on-state-high-field stress for the same applied gate-drain voltage. However, this does not necessarily mean that the reverse-gate-bias stress will inevitably cause higher degradation rate than on-state-high-field stress. For the same gate-drain voltages applied during the reverse-gate-bias and on-state-high-field stress, the role of the applied bias can be significantly different in terms of voltage induced electric field. For the case of on-state-high-field stress, the high source-drain voltage can induce a huge amount of hot electrons in the channel, while the effect of hot-electrons in reverse-gate-bias stress should be much smaller due to the small gate leakage current. Interaction of the huge amount of hot electrons in the channel with the lattice induces self-heating (equilibrium excess acoustic phonons) and hot phonon (non-equilibrium optical phonon) effects.[8,13] Comparing the noise spectra in Figs. 1 and 2, we can clearly see that the degradation behavior is quite different. The degradation under the reverse-gate-bias stress is characterized by a gradual increase of trap(s) intensities, while the on-state-high-field stress is characterized by a nearly frequency-independent increase of phase noise. Thus, the degradation mechanism(s) associated with the on-state-high-field stress is not simply due to the high electric field, but to the electric field induced hot-electron, hot phonon, and self-heating effects in aggregate as demonstrated in the degradation of InAlN/GaN based HFETs.[8] And further evidence comes from the gate leakage current ratios of stressed to pristine devices under these two different stress types as demonstrated in Fig. 3, where larger gate leakage current ratios correspond to larger gate-drain stress voltages for each stress type. For reverse-gate-bias stress under $|V_{gs}| = 10$ and 15 V, the gate-leakage currents showed a small (2–4 times) increase, with no corresponding G-R peak in Fig. 2. For reverse-gate-bias stress under $|V_{gs}| \geq 20\,V$, the gate leakage current showed a large (50–200 times) increase and a G-R peak emerged in the noise spectra. The increase of gate

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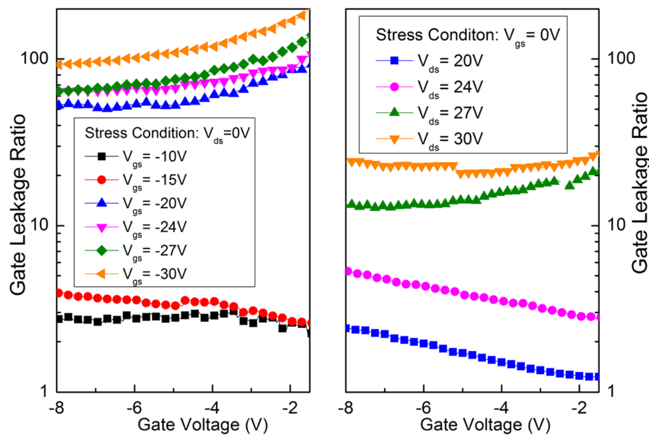

FIG. 3. Gate leakage current ratios of stressed devices to pristine devices for (a) reverse-gate-bias stress and (b) on-state-high-field stress.

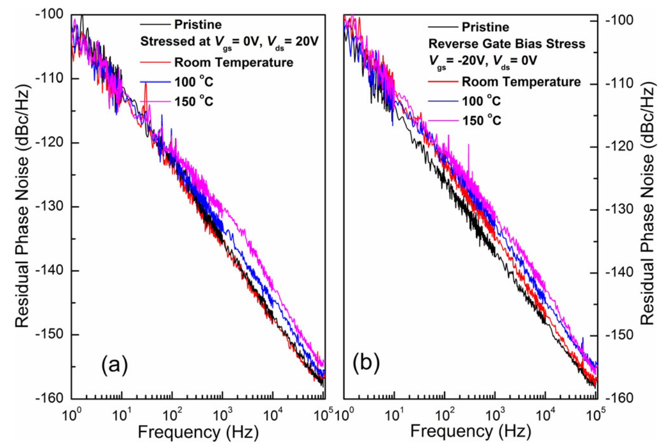

FIG. 4. (a) Phase noise spectra measured at $V_{gs} = 0$ V and $V_{ds} = 6$ V for pristine devices and devices stressed under on-state-high-field at $V_{gs} = 0$ V and $V_{ds} = 20$ V at room temperature, 100 °C and 150 °C. (b) Phase noise spectra measured at $V_{gs} = 0$ V and $V_{ds} = 6$ V for pristine devices and devices stressed under reverse-gate-bias at $V_{gs} = -20$ V and $V_{ds} = 0$ V at room temperature, 100 °C and 150 °C.

leakage current for reverse-gate-bias stress under $|V_{gs}| \geq 20$ V should be due to the trap generation in the AlGaN barrier, which can be a conductive path.[3] In retrospect, the increasing amount of accelerated gate leakage electrons under higher stress electric field may further promote the trap generation in the barrier. For on-state-high-field stress, the gate leakage currents increase gradually from ~2 to ~30 times for V_{ds} from 20 V to 30 V. If the increase of the gate leakage current and noise after on-state-high-field stress is as well due to the trap generation in the barrier, then on-state-high-field stress should generate much lower concentration of traps in the barrier, and therefore, a small increase of noise, which is not the case as shown in Fig. 1.

The effects of the base plate temperature on the device degradation for the on-state-high-field stress were investigated and the results are plotted in Fig. 4(a). A G-R peak emerges at between ~10^3 and 10^4 Hz for the on-state-high--field stress with $V_{ds} = 20$ V at 100 °C and its intensity increases further for a higher stress temperature of 150 °C. The effects of the base plate temperature on the device degradation for the reverse-gate-bias stress were also examined and the G-R peak intensity was also observed to increase with temperature as shown in Fig. 4(b). Using a thermal resistance of approximately 27.3 °C·mm/W,[14] the temperature of devices stressed at $V_{gs} = 0$ V and $V_{ds} = 20$ V and at 150 °C base plate temperature is about 40 °C higher than that of devices stressed at $V_{gs} = 0$ V and $V_{ds} = 30$ V and at room temperature. However, a much larger degradation in terms of phase noise was observed for devices stressed at $V_{gs} = 0$ V and $V_{ds} = 30$ V at room temperature, which means the heat (equilibrium excess acoustic phonons) is excluded as the key factor causing the nearly frequency-independent increase of the noise when large drain bias was applied during the on-state-high field stress. Thus, the degradation should be mainly due to the non-equilibrium hot-electron and hot phonon (non-equilibrium optical phonon) effects.[7,8] It should be noted that the equilibrium excess acoustic phonons (temperature) increased the number of traps for both on-state-high-field and reverse-gate-bias stress. This may be a result of higher temperature causing stronger lattice vibration, and hence promoting atomic displacements, which inevitably will cause more defects, and thus increase the G-R peak intensity.

The hot-electron and hot-phonon effects can be further examined by varying the drain-source voltage during the on-state-high-field stress. Gate-voltage dependent current measurements in the linear operation region of HFETs were conducted to extract the channel resistance R_{ch} as well as the sum of source and drain resistances ($R_s + R_d$). For the case of on-state-high-field stress at $V_{ds} = 30$ V, more than 90% of the increase of source-drain resistance after stress was shown to be due to the increase of R_{ch}, i.e., due to the channel degradation. This correlates well with the findings from phase noise measurements, where the spectra after stress were characterized by a frequency independent increase of noise with a small G-R peak. It should be noted that the drain current did not show any recovery after weeks in ambient environment, and current collapse was not observed during repeated current measurements. Thus, it can be concluded that a permanent degradation has occurred instead of temporary trapping unless the trapped electrons have very long time-constants, in which case the process can be equivalently regarded as permanent defect/trap generation. A frequency independent increase of noise can be due to mobility fluctuation or number fluctuations from continuous trap spectrum (such as the case of reverse-gate-bias-stress at $V_{gs} = -30$ V), or both processes acting together.[10] The drain current and phase noise degradation observed in aggregate as mentioned above suggests that the frequency independent increase of noise should most likely be ascribed to the mobility fluctuations due to the channel degradation, similar to what has been reported in InAlN/GaN HFETs.[8]

In conclusion, in order to shed light on the degradation mechanisms, electrical stress experiments of AlGaN/GaN HFETs under high drain current with high electric field, and no drain current with high electric field, have been conducted and the device degradation monitored by phase noise and dc characteristics. We showed that the degradation is strongly correlated with both the applied electric field and external base plate temperature. The external base plate temperature was shown to promote trap generation for both the reverse-gate-bias and on-state-high-field stress, while the role of

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electric field is different for the two stress conditions. Simulation of electric field intensity across the device together with experimental results suggest that the hot-electron/hot-phonon effects induced by the accelerating electric field are dominant in device degradation under on-state-high-field stress, while degradation under reverse-gate-bias stress is purely due to the high electric field in conjunction with increased gate leakage. The results presented here help distinguish the impact of electric field and hot electron/hot phonon effects on the degradation and electrical performance of AlGaN/GaN HFETs.

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