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Reliability of AlGaN/GaN high electron mobility transistors on low dislocation density bulk GaN substrate: Implications of surface step edges

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To enable gaining insight into degradation mechanisms of AlGaN/GaN high electron mobility transistors, devices grown on a low-dislocation-density bulk-GaN substrate were studied. Gate leakage current and electroluminescence (EL) monitoring revealed a progressive appearance of EL spots during off-state stress which signify the generation of gate current leakage paths. Atomic force microscopy evidenced the formation of semiconductor surface pits at the failure location, which corresponds to the interaction region of the gate contact edge and the edges of surface steps.
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Recent advances in GaN high electron mobility transistor (HEMT) manufacturing have opened the way to a wide range of applications in the radar and communication sectors, as well as to power switching applications. Despite the impressive performance of state-of-the-art AlGaN/GaN HEMTs, in particular for high frequency, high power operation,[1] the question about device reliability remains not fully explored. The reliability issues often result in a de-rating of the devices in order to fulfil the reliability standard, therefore, not taking advantage of the full potential of the GaN device system. Understanding the physical mechanisms underlying the degradation phenomena and their correlation with structural and point defects within the semiconductor is crucial for the further improvement of device reliability. In particular, off-state degradation in AlGaN/GaN HEMTs on SiC substrate has been proposed to be linked to the generation of percolation paths via defects in the AlGaN barrier[2] or threading dislocations in the device epilayers.[3] However, up to date it is still unclear, whether there remain any further, yet unknown, degradation mechanisms, which can play a detrimental role for device reliability in off-state operation.

Bulk-GaN substrate availability has improved significantly over the last years with the steady progress in the development of hydride vapor phase epitaxy (HVPE)[4] and more recently of ammonothermal growth,[5] making these substrates more readily available. Therefore, bulk-GaN substrates are receiving cumulative attention as the potential substrate of choice for future GaN devices, although complete fabrication of GaN-on-GaN electronic devices may not be fully optimized yet. The absence of the nucleation layer, which is needed for the growth of device structures on SiC or Si substrates, as well as the rather high thermal conductivity of the bulk GaN substrate itself makes this device concept thermally competitive to GaN-on-SiC.[6] Most importantly for this work, however, GaN-on-GaN structures exhibit several orders of magnitude lower dislocation densities than GaN-on-SiC,[7–9] removing one of the potential device degradation contribution. These structures are therefore ideally suited for studying device degradation significantly less influenced by threading dislocations. In this work, we explore the impact of step edges in the device epilayers on off-state AlGaN/GaN HEMT degradation by means of electrical device characterization, electroluminescence (EL) imaging, and atomic force microscopy (AFM).

AlGaN/GaN HEMTs were grown by low-pressure metal organic vapor phase epitaxy (MOVPE) on a 500-μm-thick semi-insulating bulk-GaN substrate with a Fe-doping concentration of $3 \times 10^{18}\,\mathrm{cm}^{-3}$. The GaN substrates were grown by HVPE, achieving a dislocation density as low as $\sim 10^5\,\mathrm{cm}^{-2}$.[7] The HEMT structures consisted of a 2-μm-thick unintentionally doped GaN layer, an 18-nm-thick AlGaN barrier layer (25% Al content), and a 2-nm-thin GaN cap layer. Standard ohmic contacts were used for the source and the drain, and a standard Schottky contact for the gate. Devices had a gate length of 0.25 μm, a gate width of $2 \times 150\,\mu$m, and a source-drain distance of 2.5 μm. All devices were passivated with a 100-nm-thick SiN_x layer deposited by plasma-enhanced chemical vapor deposition (PECVD). More details on the devices can be found in Ref. 5.

The GaN-on-GaN HEMTs were step-stressed in off-state at a gate-source voltage $V_{GS} = -10\,\mathrm{V}$, about three times the threshold voltage, while the drain-source voltage V_{DS} was increased in 5 V steps from 0 to 30 V, spending 2 min at each stress step. During device stress, EL images were acquired

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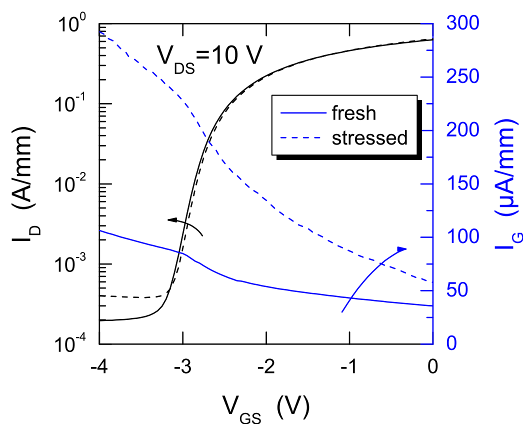

FIG. 1. Transfer characteristics of an AlGaN/GaN HEMT on bulk GaN substrate before and after off-state step stress up to $V_{DS} = 30$ V and at $V_{GS} = -10$ V.

using an astronomy-grade charged-coupled device (CCD) camera combined with a microscope and a $50\times$ (NA = 0.5) objective. The gate current I_G was simultaneously recorded during stress of the devices. DC characteristics of the devices were measured before and after stress to monitor the effect of the off-state stress on the device performance.

Figure 1 depicts the transfer characteristics of a representative 2×150-μm-wide AlGaN/GaN HEMT on bulk-GaN substrate before and after off-state stress. The most apparent observation is the increase in gate leakage current due to off-state stress, which also results in an increase in sub-threshold drain current. Figure 2(a) shows the evolution of the gate current during off-state step stress. For each stress step, the gate current I_G initially decreases over time, consistent with what has been reported previously, e.g., on GaN-on-SiC devices.[10] For $V_{DS} > 15$ V, I_G experiences several abrupt increases during the stress steps. These gate current jumps coincide with the progressive appearance of EL spots near the drain-side edge of the gate contact, as illustrated in Figure 2(b). The EL spots indicate the location of generated gate current leakage paths which electrically connect the gate electrode or in general the device surface through the AlGaN barrier layer with the AlGaN/GaN channel. A similar observation, i.e., the appearance of EL spots and their correlation with the gate current evolution, has been reported for GaN-on-SiC HEMTs during off-state stress.[2,10–12] For a V_{DS} of 30 V and above, I_G showed a monotonous increase over time, which may indicate the onset of an additional wear-out mechanism, as this was not related to the occurrence of further EL spots. Here, we focus on the early-stage degradation of the devices.

To gain insight into the physical mechanisms of the device degradation, the SiN_x passivation layer and contacts were removed after the completion of the electrical stressing procedure by wet chemical etching as in Refs. 11 and 13. AFM images were then acquired from the exposed semiconductor surface. An AFM image taken from a region of the device where EL spots were present (Figure 3) shows pits near the drain side of the gate edge. A careful overlay of the AFM and EL images reveals that surface pits appear at the

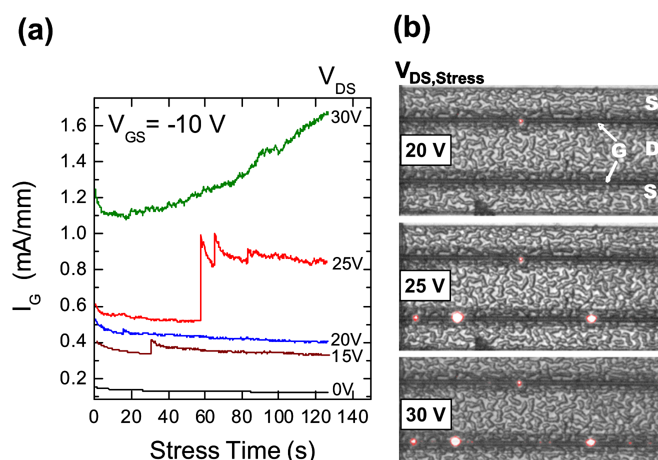

FIG. 2. Off-state step stress of a 2×150-μm-wide HEMT at $V_{GS} = -10$ V and with V_{DS} from 0 to 30 V: (a) Gate current during Off-state stress; (b) EL images at the end of each stress step, acquired with the CCD camera at 1 s integration time. The EL images are overlaid with white light images of the devices.

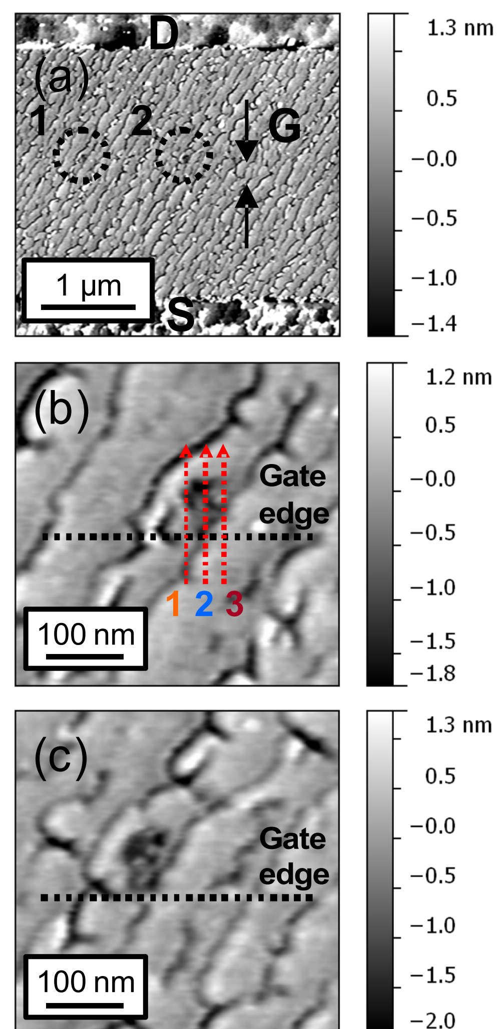

FIG. 3. AFM image of a GaN-on-GaN HEMT after removal of the contacts and passivation: (a) AFM image of the source-drain gap, where the location of the removed source, drain, and gate contacts is indicated, as well as the presence of two failure-spot-related surface pits; (b) and (c) Detailed AFM images of the pits labeled as 1 and 2 in (a), respectively. The former location of the drain-side edge of the gate is indicated as dashed line. The numbered arrows in (b) refer to the AFM profiles in Figure 4.

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exact same locations where the EL spots progressively emerged during stress, similar to what has been reported for GaN-on-SiC.[11] The geometry of these pits (Figures 3(b) and 3(c)), and also the internal structure they exhibit (Figure 4), is rather irregular and does not feature a faceted, symmetric V-type shape. This may suggest that the pit formation mechanism may not directly result from a physical material cracking as a consequence of the inverse piezoelectric effect,[14] but is probably a time-accumulated effect caused by electrochemical reactions on the device surface.[15] The stress-generated pits, as observed in the AFM images, typically feature a lateral dimension of about 80 nm and are on average 1 nm deep (see Figure 4).

The dislocation density in the device epilayers is several orders of magnitude lower than in state-of-the-art GaN-on-SiC devices. Indeed, the lack of surface step termination points observed in the AFM maps denotes the virtual absence of screw-type dislocations in the device epilayers.[16,17] In principle, if threading dislocations, which evidently can be crucial for GaN device reliability,[3] were the only mechanism triggering the off-state degradation of AlGaN/GaN HEMTs, no significant degradation would be expected for GaN-on-GaN HEMTs. Consequently, one could argue that percolated current paths through trap states in the AlGaN barrier layer may play the dominant role for the devices studied here. Nevertheless, considering the spatially random nature of trap generation, a statically random distribution of the failure sites along the gate edge would be expected.

As displayed in Figure 3, we observed ~2-nm-high growth steps on the surface of the devices with relatively rough and non-uniform step edges, i.e., the step edges are ill-defined and reveal numerous grooves. About 85% of the total number of observed pits appear to emerge from a point where the drain-edge of the gate contact crosses one of these step edges, spreading towards the drain. Examples are illustrated in Figures 3(b) and 3(c). The edges of growth terraces may inherit a higher risk of defect generation due to the high density of dangling bonds that may result in surface states.[18] This is consistent with recently demonstrated enhanced surface trapping at step edges in AlGaN/GaN HEMTs,[19] locally impacting the electric field near the gate edge. Step edges have also been reported in as-grown structures to increase gate leakage through the barrier layer.[20] When the drain edge of the gate contact, where the highest electric field occurs, crosses a step edge, these sites may become much more vulnerable to off-state degradation. In contrast, one would expect point defects and generated traps in the AlGaN layer to be distributed randomly along the gate edge, i.e., not correlated to the step edges or any other surface feature. Consequently, point defects alone cannot present the cause for off-state degradation under consideration here. This supports the link of step edges and related surface defects with a possible triggering mechanism for the emergence of gate current leakage paths in GaN HEMTs, underlining that the surface microstructure plays a key role for GaN device degradation. Optimization of the surface morphology of GaN-on-GaN may therefore be an important factor to consider for electronic device developments on bulk-GaN substrate growth.

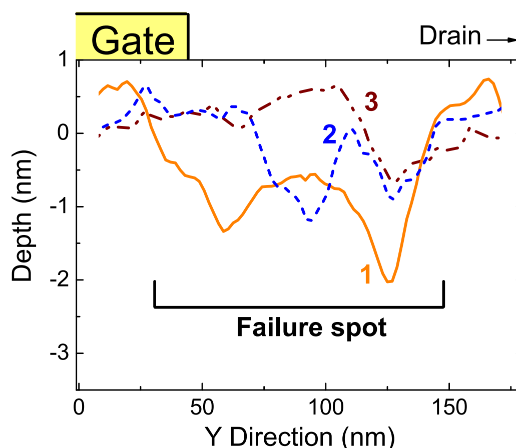

FIG. 4. AFM profiles along the direction of the three arrows indicated in Figure 3(b). The former location of the gate contact is indicated at the top of the graph.

In conclusion, off-state stress of GaN-on-GaN HEMTs was used to demonstrate that step edges and associated electronic trap states can trigger the generation of failure spots in the device epilayers. The surface microstructure therefore plays a key role for off-state degradation in GaN devices. Further advancements in GaN-on-GaN growth minimizing the impact of step edges and further epilayer optimizations may be a way forward towards high reliability GaN electronic devices.

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