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One-transistor one-resistor (1T1R) cell for large-area electronics

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We developed a one-transistor one-resistor cell composed of one TiO_2-based resistive switching (RS) device and one ZnO-based thin-film transistor (TFT). We study the electric characteristics of each component individually, and their interplay when both work together. We explored the direct control of bipolar RS devices, using our TFTs to drive current in both directions. We also report striking power implications when we swap the terminals of the RS device. The target of our work is the introduction of RS devices in large-area electronic (LAE) circuits. In this context, RS devices can be beneficial regarding functionality and energy consumption, when compared to other ways to introduce memory cells in LAE circuits. *Published by AIP Publishing*. https://doi.org/10.1063/1.5040126

Resistive switching (RS) devices are simple capacitor-like two-terminal structures in which the resistance can be adjusted by electric pulsing.[1–4] RS devices are attracting much attention as high capacity memories and in the field of neuromorphic systems because they can be integrated into high-density crossbar arrays.[5–8] It is clear that large-area electronics (LAE, e.g., flexible and transparent electronics) is not the technology to implement large neuromorphic circuits or high-density memories. Nevertheless, the introduction of RS devices can be very beneficial for LAE because, in some cases, it can help to reduce the number of components. Also, RS devices are nonvolatile, which is good for power saving.

As an example, let us consider that we have to integrate a few bits of memory in a flexible circuit, which are generally made with thin-film transistors (TFTs). We should base the memory cells on one of the following technologies: dynamic or static random-access memory (DRAM, SRAM), floating-gate (FG) transistors, or RS devices. SRAM typically requires 6 TFTs per bit and is volatile. DRAM cells are simple, but they need a complicated refresh circuit. FG transistors are nonvolatile and compact, but the technology to make the floating gate is generally out of reach for the flexible electronics manufacturing plants.

RS devices are an attractive alternative; an RS-based memory cell requires only two components and is nonvolatile, simple to use and fabricate, and compatible with LAE fabrication processes. The two required components are one RS device and one selection device. In general, selection devices—an electronic component that controls the current flow through the RS device—are highly nonlinear components or transistors.[9–11] In the latter case, the subcircuit composed of one RS device and one transistor is called a one-transistor one-resistor (1T1R) cell.[12–15]

In standard integrated circuits, the transistor is a single-crystal MOS. Here, we study a 1T1R cell using a thin-film transistor (TFT) instead.[16] This minor change has substantial implications. The performance of TFT is not equivalent to silicon transistors. Silicon transistors behave as ideal switches when controlling RS devices. On the contrary, the ON resistance of the channel in TFTs is comparable (if not higher) to the resistance of the RS device. As a general rule, TFT does not have any advantage over the single-crystal Si-based transistors regarding power consumption and switching performance. But in some cases, such as LAE, single-crystal MOS technology cannot be used; we are focusing on those cases.

Figure 1 presents our 1T1R cell composed of an n-type TFT driving a bipolar RS device. The nodes of this circuit are the transistor gate (G), the source (S), the drain connected to the bottom electrode of the RS device (D), and the top electrode (T) of the RS device. The substrate is highly doped

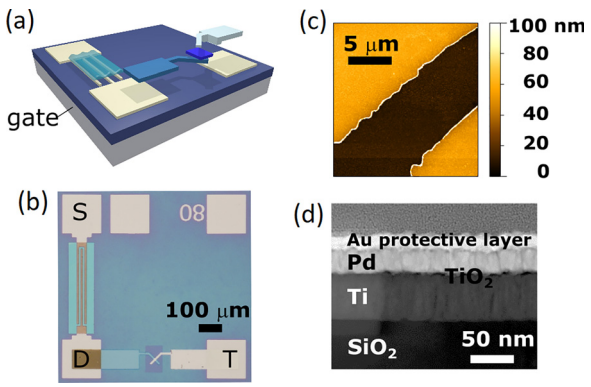

FIG. 1. (a) Exploded view of the structure, composed of a ZnO:N-based transistor and an amorphous TiO_{2-X}-based RS device. The substrate behaves as the gate electrode. The fabrication involves five photolithography steps. The first two steps define the electrodes and access pads (Au/Ti) and the semiconducting channel of the transistor (ZnO:N). The final three stages define the bottom electrode (Ti), the active layer (TiO_{2-x}), and the top electrode (Pd) of the RS device. (b) Optical image. There are three access pads, the source of the transistor (S), drain (D) connected to the bottom electrode of the RS device, and the top electrode of the RS device (T). (c) AFM close up of the transistor channel. (d) HRTEM image of the RS devices.

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Si^{++} with a 300 nm-thick thermal oxide layer, where the Si^{++} is the gate, and the SiO_2 is the gate dielectric. The W/L is 80 (channel width $W = 800\,\mu m$ and channel length $L = 10\,\mu m$). The semiconducting channel, nitrogen-doped zinc oxide (ZnO:N), was deposited by Atomic Layer Deposition (ALD) at 95 °C. In addition to the zinc precursor (diethyl zinc, or DEZ) and H_2O, we used an ammonium hydroxide solution as a third precursor for nitrogen doping. We tested different doping levels looking for the highest ON/OFF ratio and the lowest leakage current. The best result was by alternating a pulse of H_2O and another of a solution of 28% NH_3 in H_2O, after every DEZ pulse.[17]

The RS device is a cross-shaped structure with an overlapping area of $5 \times 5\mu m^2$. The bottom electrode is made of Ti and the top electrode of Pd. We deposited the TiO_{2-x} layer by reactive sputtering at room temperature. We adjusted the oxygen content to have a forming-free operation, as reported elsewhere.[18] A forming-free RS device does not need any electrical preconditioning (electroforming) before use. Swapping the electrodes of the RS device is central to our study, i.e., whether we connect the Pd or the Ti electrode to the transistor. We called "direct" configuration when the Ti bottom electrode is connected to the drain electrode and "inverse" configuration when the Pd top electrode is connected to the transistor. See supplementary material for details on the fabrication. Overall, the maximum required temperature in all the fabrication processes is 95 °C (ALD), which renders all our processes well compatible with LAE fabrication plants.

In this manuscript, we will first report the characterisation of the transistor and the RS device separately and then the study of both devices working together. We start with the transistor. We used two source measure units (SMU): one biased the gate by applying V_{GS} between S and the gate and the other SMU biased the channel between S and D (V_{DS}) and measured the current (I_D).

Figure 2(a) presents the transfer characteristic of our n-type transistors. The ZnO:N layer is near the subthreshold region at zero gate voltage (V_{GS}) due to the nitrogen doping, which compensates most of the free electrons present in the ZnO film. Electrons are electrostatically injected into the ZnO:N film as gate voltage increases. The transistor turns on when V_{GS} exceeds the threshold voltage $V_{TH} = -1.5$ V. Electrons form a conducting channel in the ZnO:N layer, with field-effect mobility (saturation regime) $\mu_{FET} = 2.5\,cm^2/Vs$ (see supplementary material).

Figure 2(b) presents the output characteristics. We observe a strong asymmetry between positive and negative V_{DS}. In general, the output characteristic of n-type transistors is reported only for positive channel bias voltage (V_{DS}). But in this work, we operate the transistor with positive and negative V_{DS} because our resistive switching devices are bipolar.

We use the fundamental equations of field-effect transistors to explain the asymmetry in the output characteristics. We only study the linear regime ($V_{GS} \ll V_{TH} - V_{DS}$). Based on the gradual channel model for thin-film transistors,[19] the current through the channel is[20]

$$I_D = \frac{W}{L} C_i \mu_{FET} \int_0^{V_{DS}} V_{GS} - V_{TH} - v\,dv. \tag{1}$$

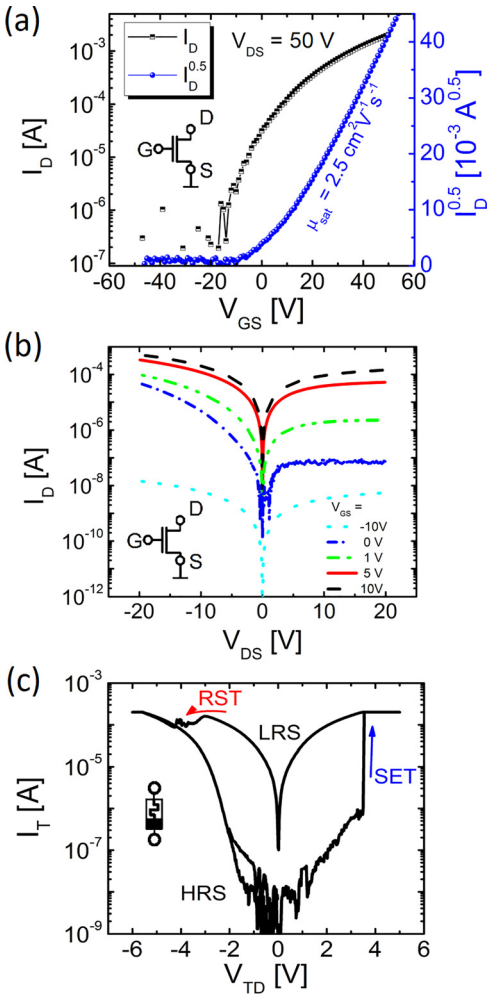


FIG. 2. (a) Transistor transfer characteristic (I_D vs V_{GS} for $V_{DS} = 50$ V). (b) Transistor output characteristics (I_D vs V_{DS}) measured with positive and negative channel bias. The strong asymmetry is central to our work. (c) I-V characteristics of the RS device.

Integrating, we obtain the gate-dependent resistance of the channel, V_{DS}/I_D

$$R_{ch} = R_{ch}^0 \frac{(V_{GS} - V_{TH})}{(V_{GS} - V_{TH}) - \frac{V_{DS}}{2}}, \tag{2}$$

where $R_{ch}^0 = \left[\frac{W}{L} C_i \mu_{FET} (V_{GS} - V_{TH})\right]^{-1}$. The asymmetry of the output characteristics is due to the term $V_{DS}/2$. It is common practice to neglect this term, which leads to the standard linear regime formula $I_D = \frac{W}{L} C_i \mu_{FET} (V_{GS} - V_{TH}) V_{DS}$.[21]

The differential output conductivity dI_D/dV_{DS} for positive V_{DS} approaching V_{GS} is

$$\left.\frac{dI_D}{dV_{DS}}\right|_{V_{DS} \to V_{GS}} = 0, \tag{3}$$

whereas for negative V_{DS}, it is

$$\left.\frac{dI_D}{dV_{DS}}\right|_{V_{DS} \to -V_{GS}} = \frac{3}{2} \frac{1}{R_{ch}|_{V_{DS} \to -V_{GS}}} \approx 30 \text{usA/V at VGS} = 5\,\text{V}. \tag{4}$$

The difference in dI_D/dV_{DS} is because the transistor current saturates for positive V_{DS} (i.e., as the transistor

approaches the saturation regime, the drain current becomes independent of the channel bias), but it always keeps increasing as the negative V_{DS} gets higher (the drain current is proportional to the channel bias). We will see that this difference is essential for our work.

Next, we characterise the RS devices by connecting an SMU between pads D and T. Figure 2(c) shows the principal feature of our RS devices, an I-V loop with two branches, corresponding to the high-resistance state (HRS) and the low-resistance state (LRS). The transition from HRS to LRS, or SET, occurs when the voltage exceeds 4 V. Reset (RST) happens at negative $V_{TD}<-3$ V. The ON/OFF ratio at low bias exceeds two orders of magnitude ($HRS = 9.2\times10^{5}\ \Omega$ and $LRS = 6\times10^{3}\ \Omega$). This kind of resistive switching behaviour is a strong indication of the underlying physical mechanism. Strong electric fields drift oxygen vacancies back and forth from the Pd/TiO_2 interface, which modulates the resistance of the device.[18]

We now study the behaviour of both devices together. We used two source measure units. One SMU sets V_{GS}. The other SMU was connected between S and T (V_{TS}). It biased both the transistor channel and the RS device and measures the current (I_T). We did not connect the D terminal. Regarding the SET and RST thresholds, one can define thresholds on V_{GS} and V_{TS} because the switching of the RS depends on both variables. Throughout this work, we concentrate on the thresholds on V_{TS}, for a fixed V_{GS}.

Figure 3(a) presents the I-V characteristics of the "direct" configuration. We fixed V_{GS} and swept V_{TS}. When the transistor is OFF ($V_{GS}=-10$ V), the current is due to its leakage current; $I_T = 10^{-10}$ A. When the transistor is activated ($V_{GS}=+10$ V), we observe the typical switching response with two resistance states. RST was at -3 V for the individual RS device, but now, it occurs at $V_{TS}=-4$ V. This difference is because a significant fraction of V_{TS} drops at the transistor. The SET remains at 4 V. The current is around 50 μA in both SET and RST.

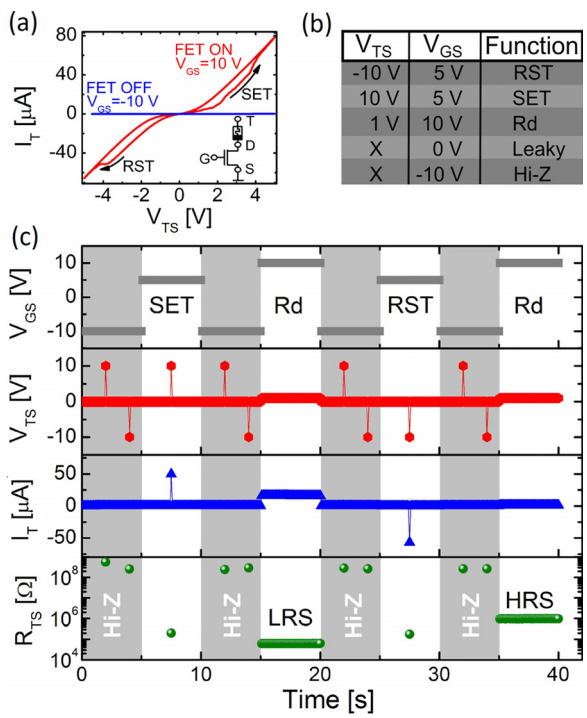
Figure 3(b) presents the conditions for writing and reading information when operating with voltage pulses. We perform the writing functions (SET and RST) at $V_{GS}=5$ V and $V_{TS}=+/-10$ V. One would expect that $V_{GS}=0$ V turns the transistor off and isolates the RS device, but actually, it leads to what we call "Leaky" state (V_{GS} is very close to V_{TH}). We biased the transistor with a negative $V_{GS}=-10$ V to obtain a high impedance state (Hi-Z). The Hi-Z state is useful for energy saving and operation in matrices.

Figure 3(c) shows a sequence of reading/writing/idle operations. V_{GS} and V_{TS} panels present the voltage setting of the SMUs, while I_T and R_{TS} are actual measurements. The system was in the high-impedance (Hi-Z) state between operations. During the Hi-Z states, we applied V_{TS} test pulses to verify the isolation.

We then tested if the "inverse" configuration is better than the "direct" configuration regarding energy consumption. Figure 4 presents the most revealing experiment. Initially, we tried to repeat the I-V curves of Fig. 3(a) ($V_{GS}=5$ V), but we were not able to reset the device. We then repeated the scans, by increasing V_{GS} in steps. The RST process happened only when the gate voltage was increased up to 40 V, at $V_{TS}=19$ V and $I_T=300\ \mu$A. The contrast between the two configurations is quite telling. While in the "direct" configuration the system operated with 10 V/50 μA, it required 19 V/300 μA after swapping the pads of the RS device. Quite significantly, by choosing the right configuration ("direct" configuration), the gate bias and power ($V_{TS}\times I_T$) requirements can be reduced by approximately one order of magnitude (relative to the "inverse" configuration).

Figure 5 helps us to rationalise the difference between both configurations. It presents the operational conditions of the transistor during SET and RST as load-line plots, which are common in the analysis of nonlinear circuits.

During SET, the load resistance of the transistor (*i.e.*, the RS device) largely decreases (it switches from HRS to LRS). In the "direct" configuration, the operating point enters in the saturation regime of the transistor, where it limits the current. Here, we have a crucial difference between both configurations. In the "inverse" configuration, there is a runaway process during the SET. The current largely increases due to the



V_{TS}	V_{GS}	Function
-10 V	5 V	RST
10 V	5 V	SET
1 V	10 V	Rd
X	0 V	Leaky
X	-10 V	Hi-Z

FIG. 3. (a) Electrical response in the "direct" configuration. (b) Table of the different operational modes. (c) Typical operational sequence.

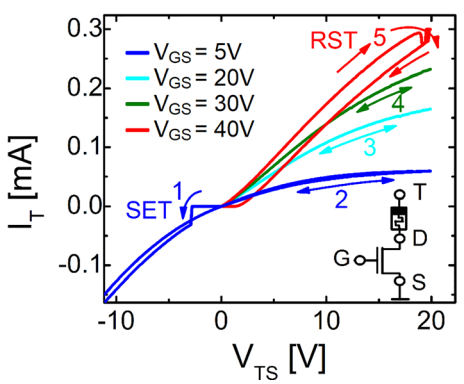


FIG. 4. "Inverse" configuration. In this configuration, we had to increase the gate voltage to 40 V and the channel bias to 20 V to induce the RST.

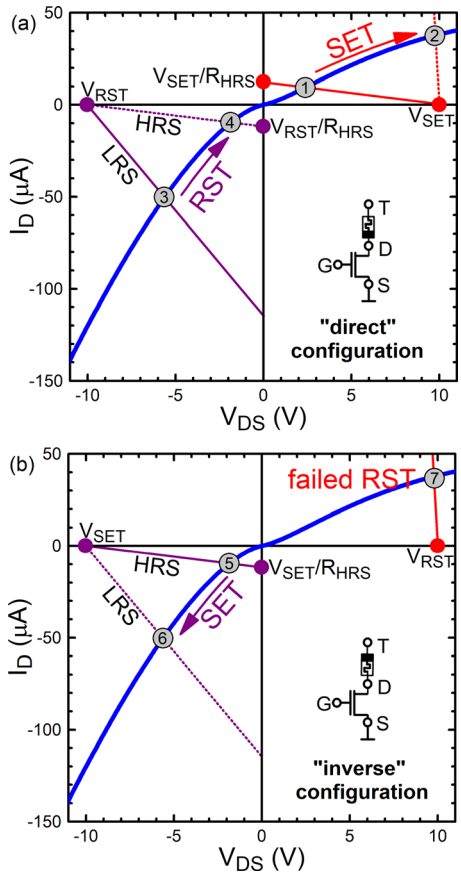


FIG. 5. Load line plots. The operating points are defined in a similar way to the load line analysis in conventional transistors. We used the output characteristics of the transistors (I_D vs. V_{DS}) for $V_{GS} = 5$V. For simplicity, we assumed linear LRS and HRS. V_{SET} and V_{RST} define points in the V_{DS} axis (in red and purple). The HRS defines a point in the I_D axis as $V_{RST}(V_{SET})/R_{HRS}$ (in red and purple). The load lines for the HRS connect these points, defining the operating points (points 1, 4, and 5). The LRS is highly nonlinear; therefore, to draw the load lines for the LRS, we fixed the operating points at $|I_D| = 50\,\mu$A (see the text, points 2, 3, and 6).

nonzero dI_D/dV_{DS}, while the load resistance gets continuously decreased. This process only stops after reaching a strong LRS that is very difficult to reset.[22] By "strong LRS," we mean LRS with a very small resistance, much smaller than the ON channel resistance of the transistor. Therefore, practically all V_{TS} drops on the transistor, and then, it is not possible to establish an electric field in the RS device to reset it. Another advantage of the "direct" configuration is that the current limitation avoids overshoots of current during the SET transition, which increases the endurance of the devices.[23]

During RST, the operating point moves towards the origin because V_{DS} decreases as the resistance of the RS devices increases much above R_{ch}. Therefore, the RST process does not require a limitation. However, the channel resistance should be as small as possible at the beginning of the RST, ideally, smaller than the LRS (otherwise, most V_{TS} will drop on the transistor channel). We indeed have the lowest possible channel resistance during RST in the "direct" configuration. On the contrary, in the "inverse" configuration, the low dI_D/dV_{DS} limits the available power, making harder to come back from a "strong LRS."

The transistor is in the linear regime ($V_{GS} = 10$ V, $V_{DS} < V_{TS} = 1$ V) during the "read" operation (Rd).

In conclusion, we reported a 1T1R cell where a TFT controls a bipolar resistive switching device. We studied the use of TFTs driving current in both directions. We also tested the effect of swapping the terminals of the RS device and discussed its implications regarding power requirements. A practical pulsing protocol to operate in a logic circuit was defined. The target of our work is the development and implementation of a building block that can ease the introduction of RS devices in large-area electronic circuits. It is useful in the cases where conventional single-crystal Si transistors cannot be used.

See supplementary material for details on fabrication, extraction of the FET parameters, and characterization of the RS devices.

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