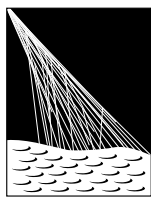SISSA

Design, upgrade and characterization of the silicon photomultiplier front-end for the AMIGA detector at the Pierre Auger Observatory

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ABSTRACT: AMIGA (Auger Muons and Infill for the Ground Array) is an upgrade of the Pierre Auger Observatory to complement the study of ultra-high-energy cosmic rays (UHECR) by measuring the muon content of extensive air showers (EAS). It consists of an array of 61 water Cherenkov detectors on a denser spacing in combination with underground scintillation detectors used for muon density measurement. Each detector is composed of three scintillation modules, with $10 \, \text{m}^2$ detection area per module, buried at 2.3 m depth, resulting in a total detection area of $30 \, \text{m}^2$. Silicon photomultiplier sensors (SiPM) measure the amount of scintillation light generated by charged particles traversing the modules. In this paper, the design of the front-end electronics to process the signals of those SiPMs and test results from the laboratory and from the Pierre Auger Observatory are described. Compared to our previous prototype, the new electronics shows a higher performance, higher efficiency and lower power consumption, and it has a new acquisition system with increased dynamic range that allows measurements closer to the shower core. The new acquisition system is based on the measurement of the total charge signal that the muonic component of the cosmic ray shower generates in the detector.

KEYWORDS: Front-end electronics for detector readout; Pattern recognition, cluster finding, calibration and fitting methods; Performance of High Energy Physics Detectors; Photon detectors for UV, visible and IR photons (solid-state) (PIN diodes, APDs, Si-PMTs, G-APDs, CCDs, EBCCDs, EMCCDs, CMOS imagers, etc)

Contents

1   Introduction

The Pierre Auger Observatory [1] is located in the North of the city of Malargüe, province of Mendoza, Argentina and covers an area of about $3000 \, \text{km}^2$. It is designed to detect ultra-high energy cosmic ray (UHECR) showers with a hybrid detection technique. It consists of 1660 water Cherenkov detectors (WCD) [2] arranged on a triangular grid with a distance of ~1.5 km between stations, conforming the surface detector (SD). It is complemented by 27 fluorescence telescopes (FD) [3] located in four buildings on the perimeter of the array observing the atmosphere above the SD. The Pierre Auger Observatory is currently being upgraded [4], and AMIGA [5–8] (Auger Muons and Infill for the Ground Array) is one of the main enhancements. The two main objectives of AMIGA are the measurement of composition-sensitive observables of extensive air showers (EAS) and the study of features of hadronic interactions. That these goals can be achieved with a muon detection techniques was proven by several experiments like KASCADE [9] and KASCADE-Grande [10] with big impact on cosmic ray physics.

AMIGA detectors are collocated with 61 WCD, which are deployed on a smaller 750 m triangular grid in an infilled array of $23.5 \, \text{km}^2$ size, conforming the Underground Muon Detector (UMD). Three AMIGA modules of $10 \, \text{m}^2$ form an UMD station associated at every WCD. When a cosmic ray shower triggers a WCD, the associated trigger is forwarded to the corresponding UMD station. Each module is buried 2.3 m below ground to shield the electromagnetic component of cosmic ray showers (vertical shielding of $540 \, \text{g/cm}^2$). Every module consists of 64 scintillation bars (of 400 cm length, 4 cm width and 1 cm thickness) and 64 wavelength-shifting (WLS) optical fibers (BCF-99-29AMC from Saint Gobain) of 1.2 mm diameter, which are glued in a lengthwise groove on each bar. Light produced in the bars by scintillation is absorbed by the WLS fiber. The excited molecules of the fiber decay and emit photons, that are propagated due to total reflection towards the fiber end for detection in a single channel of a multi-pixel photon detector. The module design is optimized for a high light output and thus, for an efficient counting of muons that impinge on the $10 \, \text{m}^2$ area. The mechanical AMIGA module design is fixed and detailed in [11].

Until September 2016, an engineering array (EA) of seven UMD stations were equipped with multi-pixel photomultiplier tubes (MPPMT). For the final production of AMIGA modules, the MPPMTs will be replaced with silicon photomultipliers (SiPM) [12]. The electronics with MPPMT began to be replaced by ones with SiPM since October 2016. Currently, the seven UMD stations of the EA are equipped with SiPM electronics.

This paper explains the design and test of the new front-end electronics for the UMD. The design of the front-end electronics for the traditional method of muon counting [12, 13] for low densities is

described in section 2. It is followed by the description of the new acquisition system in section 3 that allows, by measuring the signal charge, the determination of the muon density. In section 4, laboratory as well as data from the Observatory are used to show how the new acquisition system performs.

2   Design overview

This new design is based on the experience gained with the engineering AMIGA system, but it adds the charge measurement as new feature and it improves other parts. The specifications of the new design are detailed in [12]; they take into account the experience of the engineering design with MPPMT. The objectives for the improved electronics are:

1. Reduction of the power consumption below 2 W. The previous design of the front-end with MPPMT consumes 2.4 W without the photodetector connected.

2. The SiPM readout must be able to trigger on short light pulses of 25-35 ns width.

3. The output of each SiPM channel will be digitized as 0-1 signal. The width of the digital output must be similar to the width of the light pulses of the SiPM.

4. The electronic needs to compensate the temperature dependence of the SiPM parameters.

5. The electronic needs to provide a high gain and a low gain signal of the analog sum of all 64 SiPM pixels.

The diagram of figure 1 shows the structure of the new electronics and the interfaces between the different boards.
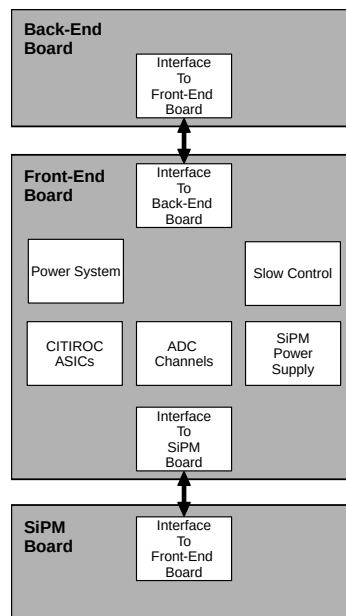

Figure 1. Diagram of the front-end general system and the interfaces to the other boards.

The electronics is divided in different parts: interface to SiPMs, the SiPM readout, ADC channels (charge measurement), the power supply for the SiPMs (pass through the SiPM interface),

the slow control, the power system and the back-end connector (interface to digital electronics). All these parts will be explained in the following sections and subsections. The electronics system of the back-end will be described in a companion future paper.

2.1 SiPM readout

The SiPM readout is realized by CITIROC[1] ASICs[2] [14], special 32-channel integrated circuit designed for the readout of SiPMs [12]. For the readout of 64 optical channels [11], two CITIROC ASICs are required. The chips provide the following functions per channel:

1. 8-bit digital-to-analog converters (DAC) to adjust the bias voltage (V_{BIAS}) of SiPM channels individually.

2. Two pre-amplifier stages with programmable gains for a high-gain and a low-gain output.

3. A fast shaper with 15 ns peak time per channel. This configuration is recommended for SiPMs by Hamamatsu [15] to decrease the pulse decay time. The smaller pulse width improves the double pulse resolutions and the timing of the trigger electronics.

4. A discriminator following the fast shaper combined with a 1-bit comparator to convert analog signals to digital signals. A 10-bit DAC sets a coarse discriminator threshold common for all 32 channels; it is fine-tuned for each channel by individual 4-bit DACs.

The schematics in figure 25 (appendix A) shows how the CITIROC chip is interfaced to the electronics. The 32 analog inputs connect directly to the SiPM interface, the 32 trigger outputs to the digital logic. The power system provides a common 5 V supply, a digital 3.3 V and an analog 3.3 V supply. Every supply line is decoupled by several 10 μF and 100 nF capacitors close to the consumer.

2.2 Power system

The electronics of the SD and UMD is supplied from a battery-powered system charged through solar panels. Maintenance of the batteries and costs demand a very low power consumption for the new front end. To meet the design goal of a consumption below 2 W, a high efficient conversion of the 24 V battery voltage to several lower consumer voltages is required. Modern switching power regulators provide high conversion efficiencies. However, they are by design prone to spikes and ripples. Linear power regulators on the other hand, provide a high ripple rejection and low noise, but are less efficient at large differences between input and output voltages.

The design of the power system (figure 2) combines the advantage of switching regulators and linear regulators in a two stage approach. The first stage made up of switching regulators converts with high efficiency the battery voltage to intermediate voltages of 5 V, 3.4 V and 1.9 V. These intermediate voltages are, in a second stage, converted by linear regulators to the final voltages of 4.9 V, 3.3 V and 1.8 V with low noise.

For the conversion of the nominal 24 V external battery voltage (23 V to 32 V range [16]) to 5 V, two different options have been implemented: a non-isolated power supply and an isolated

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[1]Cherenkov Imaging Telescope Integrated Read Out Chip.

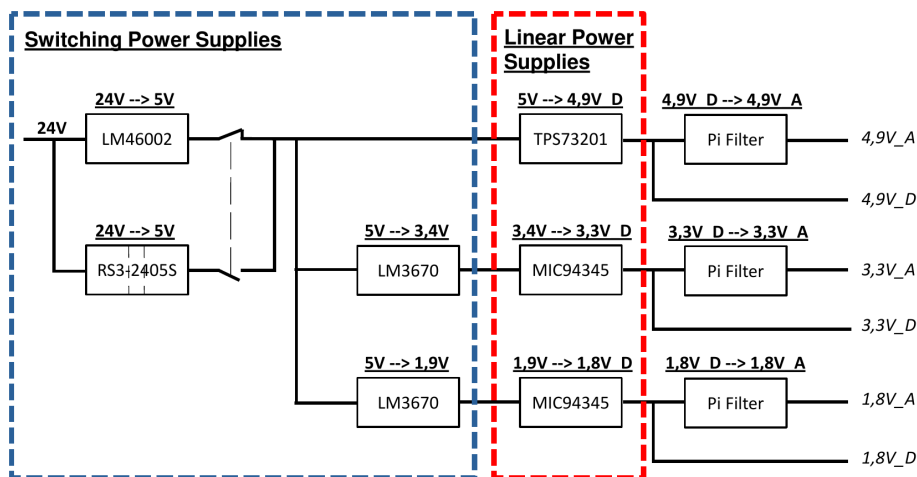[2]Application Specific Integrated Circuit.

Figure 2. Scheme of power system. In a first stage (dotted blue lines), switching regulators convert the nominal 24 V input to intermediate voltages (5 V, 3.4 V and 1.9 V). In a second stage (dotted red lines), linear regulators convert to the final voltages (4.9 V, 3.3 V and 1.8 V). The analog voltages are electrically isolated by pi filters from the digital ones.

power supply to avoid possible ground loops. The buck controller LM46002 [17] from Texas Instruments is used for the non-isolated power supply, which meets the required specifications of high efficiency (η = 88 % at 150 mA) and it provides a wide temperature range (-40° C to 125° C). Figure 26 (appendix A) shows the schematics for this option.

Two solutions were compared for the isolated power supply option: a) the RS3-2405S [18] from RECOM and b) the CC3-2405SF-E [19] from TDK. Both have almost the same properties, including temperature range, input voltage range, maximum output current, low output ripple and isolation voltage. Figure 3 shows the comparison of the converters efficiency for different loads. The converter RS3-2405S has always over the whole current range a higher efficiency compared to the converter CC3-2405SF-E. Therefore, the converter from RECOM was chosen and the schematics is shown in figure 27 (appendix A).

Finally, the power system provides the possibility to choose between the isolated or non-isolated option, but for the better efficiency, lower component count and to avoid possible ground loops, the RS3-2405S is finally selected.

The second part of the switching power supplies are buck controllers of type LM3670 [20] from Texas Instruments. The main characteristics of this controller are low noise, high efficiency and small layout area. The linear regulator stage is delimited by the red dotted lines in figure 2. A low dropout voltage (LDO) and a high ripple rejection are the most important properties of the selected regulators TPS73201 [21] from Texas Instruments and MIC94345 [22] from Micrel. The resistors defining the output voltage of the linear regulators are of 0.1 % tolerance for high output accuracy and low temperature dependency.

To avoid introducing noise from digital circuits to the analog part, the analog power supplies are isolated by a pi filter. This also keeps the signal-to-noise-ratio as high as possible and prevents undesirable ringing.
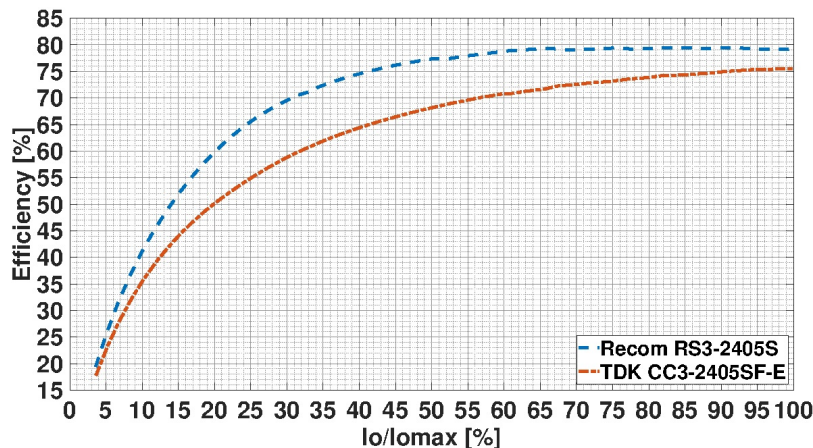
Figure 3. Efficiency measurement of the isolated converters RECOM RS3-2405S (blue line) and TDK CC3-2405SF-E (red line) at an input voltage of 27 V (mean output voltage of the battery-powered system). The efficiency of the RECOM RS3-2405S is better for all load currents.

2.3 Operating temperature range

Figure 4 shows the temperature profile of all the AMIGA modules of the engineering array as recorded with the back-end electronics in the period May 1st, 2014 to July 31st, 2015. All temperatures fall in the range 9° C and 44° C (dotted blue and red line, respectively). In general, we have selected components of industrial or even military temperature grade for best reliability. However, the SiPM power supply is only available in commercial temperature grade. Nevertheless, the operating temperature range still meets the requirements.

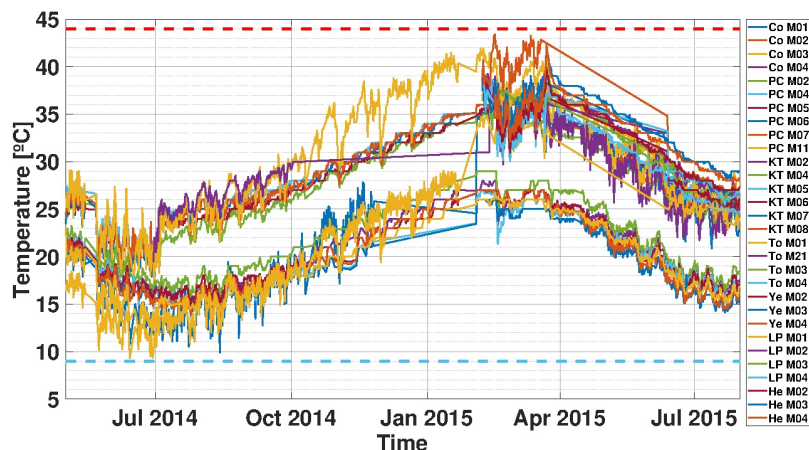**Figure 4.** Temperature profile of several AMIGA modules installed in the engineering array. The measurement period from 1st May 2014 to 31st July 2015 covers all seasons (autumn, winter, spring, summer). The minimum temperature value occurs in winter and the maximum value occurs in summer. All values fall within a temperature band of 9° C (light blue dashed line) to 44° C limits (red dashed line).

2.4 SiPM power supply

The integrated circuit (IC) C11204-01 [23] supplies the voltage for the SiPM (type S13081-050CS [12]) selected for AMIGA. This power supply is recommended by Hamamatsu and allows voltage settings between 50 V and 90 V with a resolution of 1.8 mV. As the SiPM breakdown voltage (V_{BR}) varies with temperature, this power supply includes a built-in high precision temperature based voltage compensation system. This compensation system constantly corrects the SiPM operating point in varying temperatures environments, keeping it stable. The operating point is determined by the over-voltage defined as $\Delta V = V_{BIAS} - V_{BR}$. The IC provides also an output voltage and an output current monitor for slow-control. All these functions are controlled from the back-end board via a serial interface (UART). Due to the digital voltage levels of the back-end board (3.3 V maximum) and the power supply digital voltage levels (5 V powered), a logic level shifter in each UART signal is needed to adapt the different voltage levels. The power supply provides an overcurrent protection, which switches the output voltage off for output currents above 3 mA and duration of more than 4 s. As all 64 SiPM pixels are supplied from a single supply, the inrush current at power-on would trigger this overcurrent protection. To avoid this problem, the limiting resistor of the pi filter (R18 in the schematics figure 28 of appendix A) is increased from the recommended value 10 Ω to 1 kΩ.

2.5 Back-end connection

For the connection with the back-end, two different types of connectors are used. One is a high-speed connector for the CITIROC signals and ADC channel signals (section 2.5.1), the other one is a power connector for the battery voltage and power on/off control signal for the power supplies (section 2.5.2).

2.5.1 High speed connector

The selected high speed connector QTH-090-04-L-D-A-K-TR [24] from Samtec provides a wide bandwidth of 9 GHz/18 Gbps and an inner ground plane for improved noise isolation. CITIROC signals, ADC channel signals, with their respective control signals and I^2C bus signals (see section 2.7) pass through this connector.

2.5.2 Power connector

A power connector is used in this design to eliminate connections cables between the frond-end board and the back-end board. The external battery power is connected to the back-end board and from there distributed to the front-end. The selected power connector HW-06-20-L-D-630-120 [25] from Samtec provides high current capability and the same height as the high speed connector, allowing board stacking. As shown in figure 29 (appendix A), the battery voltage and the on/off control signal for the power supplies pass through this connector. To avoid possible ground loops between the two boards and have separate grounds, an isolated solid stage relay is used for the power supply control stage (CTRL1_PS and CTRL2_PS).

2.6 Interface to SiPM

The connector QMSS-026-06.75-LD-PT4 [26] from Samtec is the interface to the SiPM. Due to the low amplitude of the analog signals from the SiPM, special care has to be taken to avoid introducing

noise. This connector is a shielded ground plane header with a large bandwidth of 6 GHz/12 Gbps. It integrates eight pins for the supply voltages and ground connection.

2.7 Slow control system

The analog to digital converter (ADC) ADS7828 [27] from Texas Instruments is the heart of the slow control system. It supervises all on board (analog and digital) supply voltages and the temperature of the CITIROC ICs as shown in figure 30 (appendix A). The ADS7828 is a single-supply, low-power, 12-bit data acquisition device with a 50 kHz sampling frequency that features a serial I^{2}C interface and an 8-channel multiplexer. An external voltage reference of 2.048 V, instead of the 2.5 V internal reference, provides a stable ADC resolution of 0.5 mV. The SiPM variables, such as the power supply output voltage, the power supply output current and the SiPM temperature, are monitored through the Hamamatsu power supply chip, and are retrieved via an UART interface.

2.8 Layout

As this design is a mixed signal system, special care had to be taken in the printed circuit board (PCB) layout to avoid introducing digital noise into the analog stage. As the SiPM signals are of very low amplitude (around 8 mV typically), a very good signal to noise ratio (SNR) is required. The disposition strategy of the ground planes, explained in 2.8.1, and the controlled impedance transmission lines, explained in 2.8.2, are of special importance.

2.8.1 Ground planes

The layouts of ground and supply planes are based on application notes [28, 29] from Texas Instruments, where the technique of partitioned ground planes is suggested for designs with many mixed grounds (analog and digital) devices. This technique uses a single ground plane in the whole PCB instead of having a separate ground plane for analog devices and for digital devices. In this way, analog signals are routed only in the board analog section, and digital signals are routed only in the board digital section, both on all layers. Under these conditions, the digital return currents do not flow in the analog section of the ground plane and remain under the digital signal trace, not inducing noise in analog signals. In figure 5 is shown the PCB layout diagram.

2.8.2 Controlled impedance lines

As this design includes high speed signals (for example, ADC channel analog signal tracks), lines of controlled impedance are required. The impedance of transmission lines depends on the PCB materials (dielectrics and conductors) and their geometry. As the maximum working frequency is around 200 MHz, the dielectric FR4 ($\epsilon_r = 4.4$) was chosen as the PCB material, which is recommended for frequencies up to 500 MHz. Asymmetrical striplines, differential striplines, microstrips and differential microstrips are used. The geometry and characteristic of each of them was designed with the help of tools detailed in [30–33]. Single-ended signal tracks have a characteristic impedance of 50 Ω and differential signal tracks have a characteristic impedance of 100 Ω. A 10-layer FR4 PCB with a thickness of 93 mil (2.36 mm) ensures the calculated geometries and the impedance values of the transmission lines.
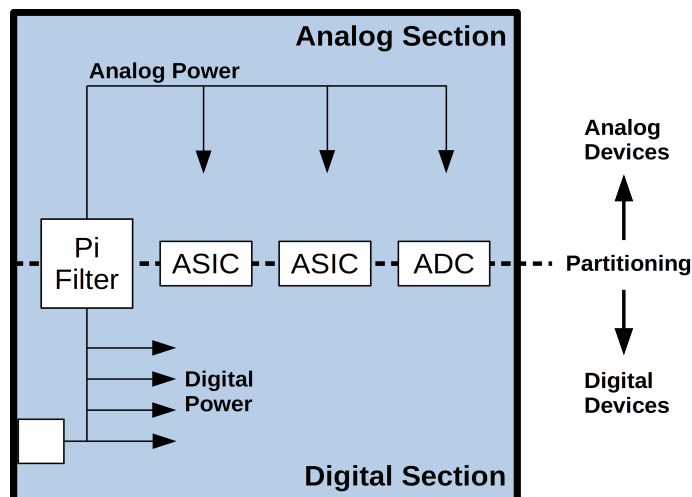
Figure 5. Power and ground strategy for PCBs with multiple ASICs, ADC and digital devices. There is only one ground plane for all the devices. The analog and digital section are separated in different regions. Thus, the return current is restricted to the corresponding section, avoiding noise induction from the digital to the analog section.

3   New acquisition system: charge measurement

The measurement of the total charge is an enhancement of the AMIGA front-end to extend its dynamic range for particle detection. Thus, each module that make up the UMD will be able to measure in regions of high particle density. These regions are located close to the impact point of the core of the air shower. The new acquisition system determines the total charge generated by the muonic component of the cosmic ray showers during its impact on the UMD. It is implemented in two independent channels of different resolution: a high gain channel (HG) and a low gain channel (LG). Figure 6 shows the operating ranges of HG channel, LG channel and the binary channels (counter mode).
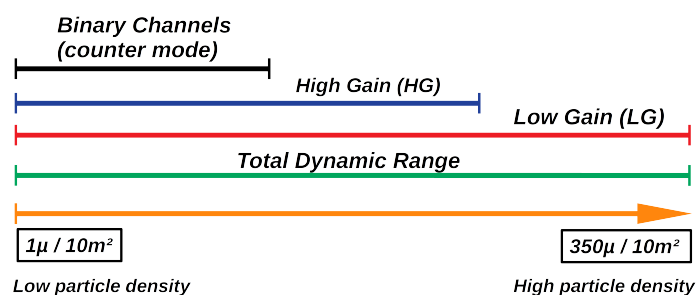

Figure 6. A greatly extended particle density range is achieved by overlapping operating ranges of the binary channels and the LG and HG channels.

The operating ranges of the HG and LG start at the same low particle density value as the binary channels [34], but reach higher values than these. Simultaneously, the LG channel saturates for higher signal charges than the HG channel, allowing to measure up to very high particle densities. That the three ranges start at the same particle density value allows firstly, to obtain complementary measurements at those values and secondly, to perform the comparison of the binary channels with

the HG and LG channels. The main difference in the overlapping ranges is the resolution. The binary channels perform with better resolution at very low particle densities, while the resolution of the HG and LG channels improves as the number of particles arriving at the detector increases. As a result, the measurements range of the AMIGA detector is extended considerably with respect to the previous design implemented for the engineering array. The binary channels saturate when all 64 scintillators have simultaneous signals but, as it will be described in the following sections, the HG and LG channels might measure up to 85 and 362 simultaneous muons without losing its linearity, respectively.

3.1 HG and LG setup (ADC channels)

The determination of the total charge is realized into three stages: the Adder Amplifier Stage, the Differential Output Amplifier Stage and the Analog To Digital Converter Stage as shown in figure 7.
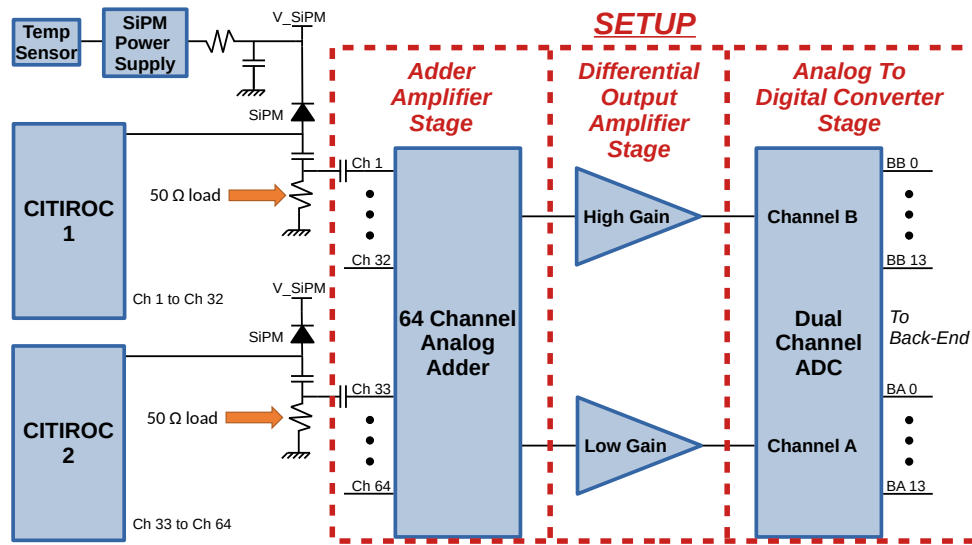

Figure 7. Scheme of the HG and LG channels. The signals from the 64-pixel SiPM array are added in a first stage (Adder Amplifier Stage), amplified and splitted in a high gain/low gain branch (Differential Output Amplifier Stage) and continuously digitized by a dual ADC (Analog To Digital Converter Stage). This circuitry represents a load of $50\,\Omega$ to the CITIROC inputs.

The adder amplifiers built up the analog sum of the 64 SiPM channels. The signals are tapped at the CITIROCs inputs providing a load of $50\,\Omega$ without affecting the CITIROCs functions. The summing of all 64 channels is realized by 4 amplifiers, which adds up groups of 16 signals very close to the two SiPM connectors (two amplifiers per connector). In this way, mismatches and unwanted signal reflections are avoided. The resulting sum-signals are again summed into a last amplifier which is located near the second stage. In this second part, a calibration channel is also added with a SMB connector that connects to this last amplifier. The schematics of the first stage is shown in figure 31 (appendix A). The five adders are realized by the dual amplifier AD8012 [35] from Analog Devices. A positive DC voltage at the positive input shifts the amplifiers operating point such that a dual supply voltages can be avoided.

The following Differential Output Amplifier Stage splits the result of the summation of the 64 SiPMs signals into two independent channels: the low (LG) and high (HG) gain. Differential

output amplifiers are used to have a better immunity to noise and to take advantage of the ADC features of the next stage. Like in the previous stage, a negative supply voltage is avoided by a shift of the operation point to the mid value of the power supply of 4.9 V (2.45 V). The used amplifier is the LMH6550 [36] from Texas Instruments. The schematics of this stage with the two channels are shown in figure 32 (appendix A).

The Analog To Digital Stage is the last one. The dual channel ADC ADS4246 [37] from Texas Instruments digitizes the differential LG and HG signal with 160 Msps, thereby consuming only 332 mW total power. This sampling rate is half of the SiPM back-end sample rate for the binary channels (320 MHz). The input low pass filter is designed for a cutoff frequency of 80 MHz to avoid aliasing. The input driver circuit used is the one recommended by the datasheet to reduce glitches and noise, named *"Drive Circuit With Low Bandwidth (For Low Input Frequencies Less Than 150 MHz)"*. All the output bit and status pins of the two channels are protected from large capacitive load currents by 49.9 Ω series resistors. The schematics of this stage is shown in figure 33 (appendix A).

3.2 Simulation

Every stage of the HG and the LG channels was modelled with the open-source circuit simulator program SPICE [38–40]. The simulation provided the Bode diagrams with gain and phase for every stage. A transfer function was fitted to every diagram and the overall frequency response for the full chain of HG and LG was derived as shown in figure 8. The 3 dB bandwidth determined from the plot is 11.80 MHz for both channels (from 25 kHz to 11,87 MHz). The maximum pass band gain is -2.50 dB for HG and -8.47 dB for LG, respectively. Both channels have the same phase response.
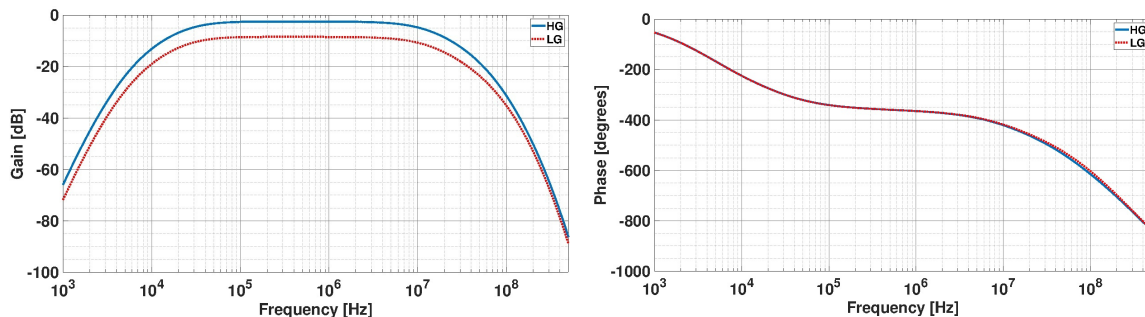

Figure 8. Bode diagram of HG and LG channel. Both channels have similar frequency response, only differing in the gain in the pass band by 6 dB. The bandwidth is about 11.80 MHz for both channels.

3.3 SiPM front-end printed circuit board

The pictures of the front-end board are shown in figure 9. This figure shows the layout of the board and indicates the locations of the main connectors and components.

4 Laboratory tests of the ADC channels

To verify the design of the ADC channels (HG and LG) and measure its performance, two different test setups have been built up. The first one was performed with signals coming from atmospheric
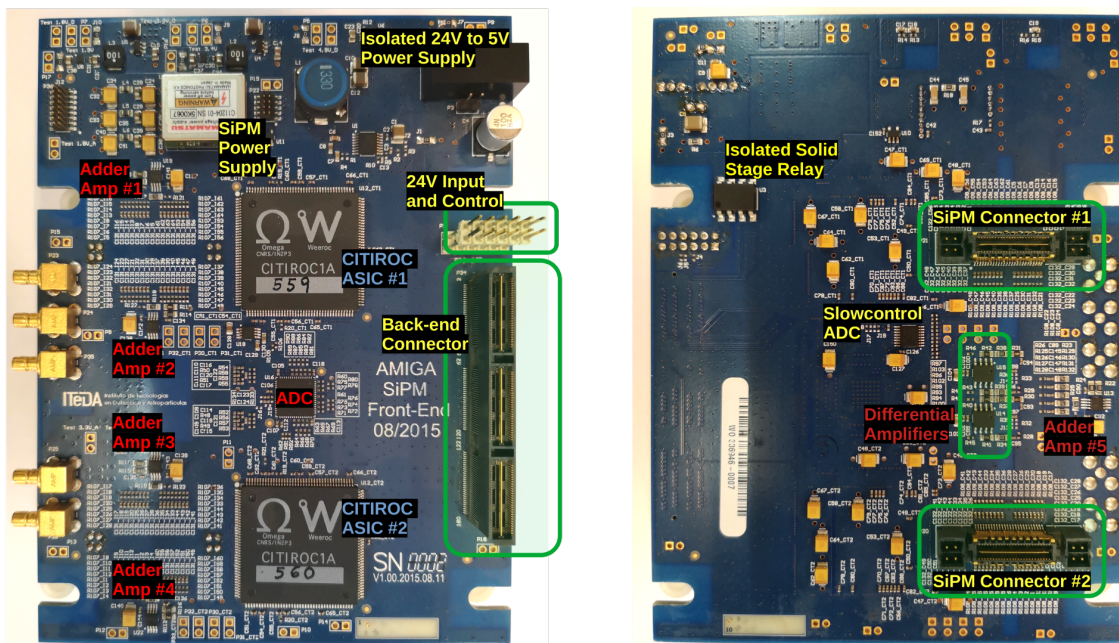
Figure 9. AMIGA SiPM Front-end board, showing the main components and main connectors of the top (left) and bottom (right) side. The components of the charge acquisition system are marked in red.

muons penetrating scintillator bars. How the mean charge is obtained from the muon signal with this setup is described in section 4.2. The second test — based on an array of 64 LEDs — is described in section 4.3. The charge calculation algorithm is explained in section 4.1.

4.1 Charge calculation algorithm

Typical signal traces of the HG and LG channels are shown in figure 10. Each trace consists of 1024 samples with a 6.25 ns separation (corresponding to 160 MHz sampling rate). The recorded traces are triggered at around sample # 600 where the pulses start. In a first step, the baseline B and the standard deviation σ are derived from the first 350 samples in the pre-trigger window. The signal charge is then calculated in the post-trigger window from the raw data corrected by the baseline B determined in step 1. All baseline corrected values are added up for those bins where the signal is more than 2σ away from baseline. The value determined this way is regarded as the signal charge, the quantity considered in the rest of the section.

4.2 Detector characterization setup

The main components of the setup for the detector characterization are shown in figure 11. The full AMIGA electronics with SiPM board, the new front-end board and the back-end board form the device to be calibrated. The parameters of the electronics like SiPM supply voltage and the configuration of the CITIROC ASICs were obtained in advance by the calibration method described in [12]. The SiPM electronics provides the ability to turn individual channels on or off as needed for a specific measurement. A mobile hodoscope [41] (at the left in figure 11) provides a trigger, whenever a particle penetrated the device and the main scintillator bar. It consists of two scintillator sheets of dimensions $4\,\text{cm} \times 4\,\text{cm} \times 1\,\text{cm}$ coupled to a SiPM for light detection. Both sheets are
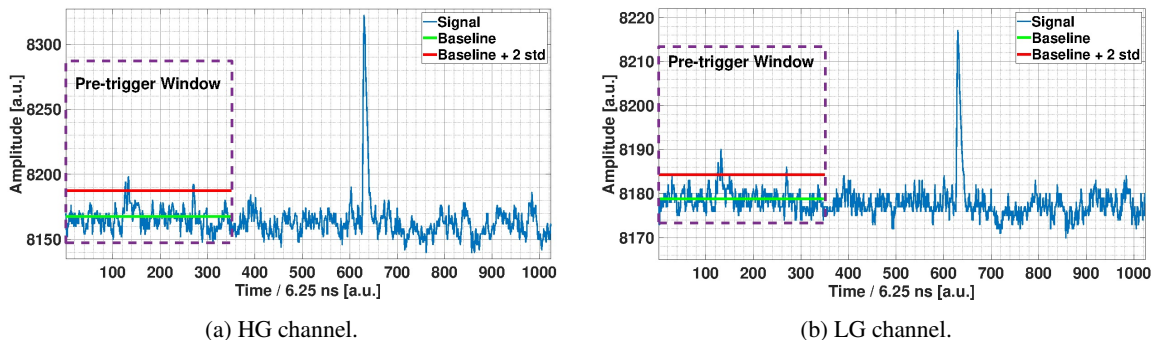
(a) HG channel.

(b) LG channel.

Figure 10. Typical traces of the HG and LG channels. The total number of samples of each trace is 1024.

aligned with a separation distance of 5 cm and the main scintillation bars placed in between. This configuration selects a particular solid angle of muons penetrating the main scintillators.
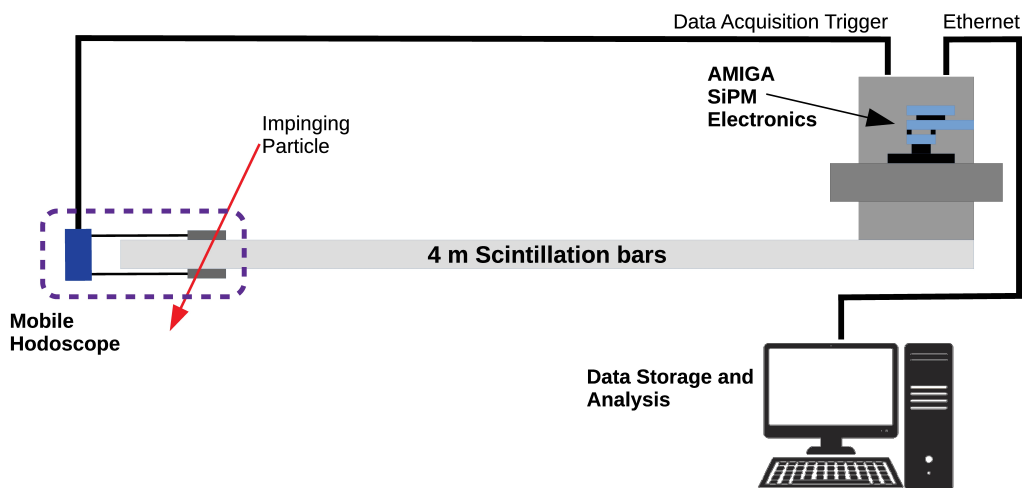

Figure 11. Scheme of setup for muon characterization: particles penetrating the mobile hodoscope generate the data acquisition trigger for the AMIGA electronics. The readout PC is responsible for the data storage and processing.

The trigger condition is fulfilled when the upper and lower SiPM signals from the hodoscope exceed a programmable threshold within a coincidence time of 60 ns. When this happens, the generated trigger enters the AMIGA electronics and initiates the event acquisition and storage in the internal RAM memory. Finally, the events are readout by a server PC, where all the AMIGA programs (acquisition and monitoring systems) are running. The stored events are analysed and processed offline by this server.

The scintillation system consists of eight bars stacked in a configuration of two columns of four bars each. For our tests, we have used only the four bars of one column. They were made of identical material like the final AMIGA production module for best reproduction of the situation at the Pierre Auger Observatory site. Those bars are coupled by optical fibers (same as AMIGA) to four non-adjacent pixels of the SiPM to avoid crosstalk effects.

4.2.1 Muon mean charge

Due to the light attenuation in the fiber, the signal amplitude at the SiPM depends on the position where the muons penetrate the bars. In a pre-analysis, we have averaged the pulse charge over several events and several positions along the bar (at 1 m, 1.5 m, 2 m, 2.5 m, 3 m, 3.5 m, 4 m and 4.5 m of optical fiber distance to the SiPM pixels). The measurement was performed with four enabled pixels corresponding to the four bars in the column. The charge measured at the ADC channels corresponds to a charged particle crossing the four scintillator bars, the total charge seen by the ADC channels is divided by four. Figure 12 shows the charge distribution for the HG channel (a) and LG channel (b). The distribution contains events from several positions along the bar measured for the same duration. q_{avg} is the mean value of the fitted distribution.
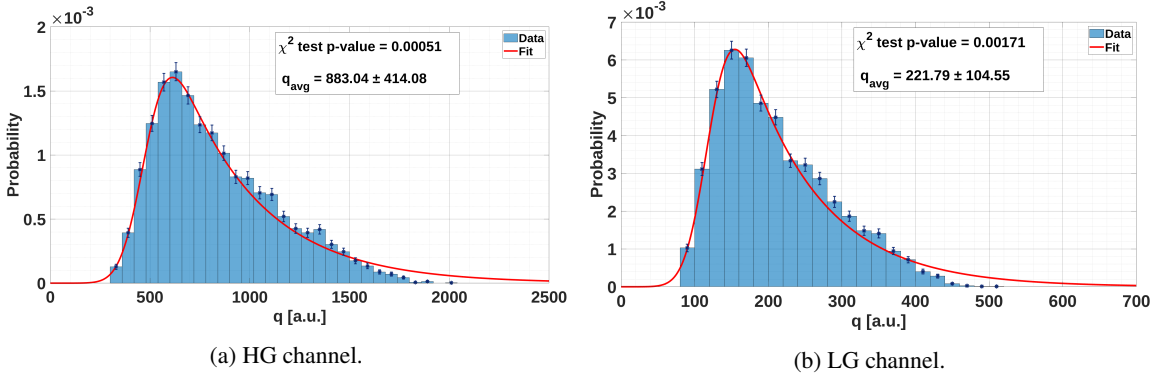

(a) HG channel.

(b) LG channel.

Figure 12. Muon charge histograms. The mean muon charge q_{avg} is derived from the fit.

Every histogram was fitted with the exponentially modified Gaussian (EMG) distribution (exGaussian distribution) whose probability density function is given by equation (4.1). This density function is a convolution of normal and exponential probability density functions.

$$f(x; \mu, \sigma, \lambda) = \frac{\lambda}{2} e^{\frac{\lambda}{2}(2\mu + \lambda\sigma^2 - 2x)} \operatorname{erfc}\left(\frac{\mu + \lambda\sigma^2 - x}{\sqrt{2}\sigma}\right) \tag{4.1}$$

Here x is the random variable, μ and σ are the mean and the standard deviation of the Gaussian distribution, λ the attenuation parameter of the exponential distribution and *erfc* is the complementary error function defined by equation (4.2).

$$\operatorname{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2} dt \tag{4.2}$$

The value q_{avg_n} is the mean of the fitted exGaussian distribution. The mean and the standard deviation of the distribution are obtained by equations (4.3) and (4.4), respectively.

$$\text{MEAN} = q_{avg} = \mu + \frac{1}{\lambda} \tag{4.3}$$

$$\text{STD} = \sqrt{\sigma^2 + \frac{1}{\lambda^2}} \tag{4.4}$$

The parameters μ, σ and λ obtained are shown in table 1.

Ch	μ	σ	λ
HG	480.2 ± 5.6	95.8 ± 7.2	$(24.82 \pm 0.96)\ 10^{-4}$
LG	120.3 ± 1.7	25.3 ± 2.2	$(98.6 \pm 4.6)\ 10^{-4}$

The values for the mean muon charge of table 1 are averages from measurements at different positions. The analysis of the same data, but now for every position of the hodoscope separately, leads to the characteristic light attenuation curves. As it is explained in [41, 42], the double exponential function given in equation (4.5) is a correct model to fit the data points.

$$A_{tt}(x) = A_0 \left(a_f\ e^{-\frac{x}{\lambda_1}} + (1 - a_f)\ e^{-\frac{x}{\lambda_2}} \right) \qquad (4.5)$$

Here A_{tt} is the average signal charge as a function of distance x along the bar, A_0 is a scale factor related to electronic gain, a_f is the relative fraction of two exponential functions with attenuation constants λ_1 and λ_2. The data of figure 13 was fitted with equation (4.5) and the parameters obtained are shown in table 2

Table 2. Double exponential fit parameters.

Channel	A_0	a_f	λ_1	λ_2
HG	3023 ± 172	0.55 ± 0.02	57.9 ± 4.9	509 ± 16
LG	786 ± 48	0.55 ± 0.02	53.8 ± 4.4	479 ± 13

The parameters a_f, λ_1 and λ_2 depend on the light attenuation and the SiPM response, thus they reflect the properties of the optical fiber, the scintillation bars, the optical couplings and the SiPM pixels. As these factors are identical for HG and LG channels, one expects similar values for the fit parameters a_f, λ_1 and λ_2. The shape of the attenuation curve depends on these three parameters and both curves have a similar shape as can be seen in figure 13. However, the scale factor A_0 reflects the channel gain. Thus, the ratio of parameter A_0 for the two channels (HG and LG) is close to a factor 4 as set by design. This proves that HG and LG channels implement complementary behaviour and response, but at different designed operation range.

4.3 Linearity characterization

4.3.1 Methodology

For the determination of the muon density it is essential that the HG and LG outputs are linear within their full dynamic ranges. In system theory, linearity is defined by the principle of superposition, i.e. the system response to superpositioned input $(x + y)$ is equal to the sum of the individual responses to input x and y as expressed in equation (4.6):

$$f(A(x + y)) = A \cdot f(x) + A \cdot f(y) \qquad (4.6)$$

Considering a constant frequency response along the entire spectrum, the task is to determine the gain A and the dynamic range where this gain is constant. This requires measuring both, the
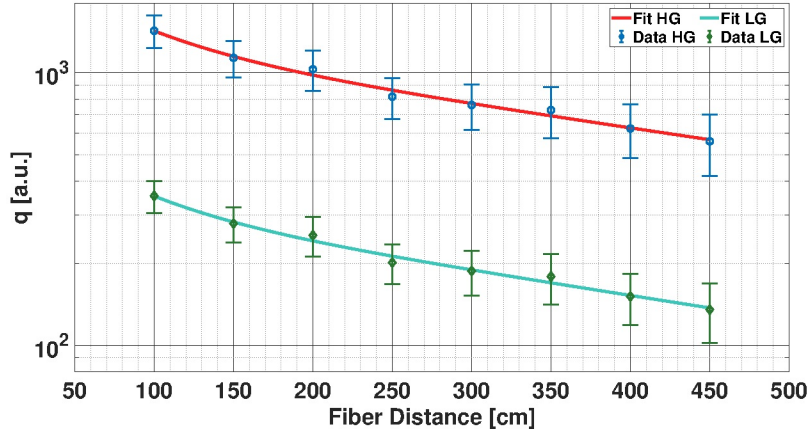
Figure 13. Attenuation of the muon charge signal along the scintillation bar for HG (blue dots) and LG (green dots). The red and green curves are fit function according to equation (4.5). The functional shape of the attenuation is similar as it depends mainly on the optical properties. The different absolute scale reflects the different channel gains.

input and output of the system. In our case, the ADC channels adds up the signals of 64 pixels of the SiPM. In the ideal case, each pixel i is added with an unique gain G. Thus, considering each pixel separately and following the superposition principle the output $y_i(t)$ is:

$$y_i(t) = G \cdot x_i(t) \tag{4.7}$$

Where $y_i(t)$ is the output signal for pixel i, $x_i(t)$ is the input signal of pixel i and G is the gain. Assuming that the ADC channels are a linear system and considering equation (4.6) with $A = 1$, the output considering all signal input is:

$$y_o(x_1(t) + x_2(t) + x_3(t) + \ldots + x_{64}(t)) = G \cdot x_1(t) + G \cdot x_2(t) + G \cdot x_3(t) + \ldots + G \cdot x_{64}(t) \tag{4.8}$$

Where y_o is the total output signal of the ADC channels (sum of the 64 pixel signals), $x_i(t)$ are the input signals on each pixel and G is the common gain for all pixels. On the other hand, the arithmetic sum of the individual signals at the output of the ADC channels (see equation (4.7)) is defined as $y_s(t)$.

$$y_s(t) = y_1(t) + y_2(t) + \ldots + y_{64}(t) \tag{4.9}$$

As the ADC channels operation mode is charge measurement, the dynamic range characterization is made as a function of charge. Consequently, Q_i is defined as the output charge measurement when there is a signal on channel i. Q_o is defined as the output charge measurement when there are signals on all channels. Under these definitions, the equation (4.8) is:

$$Q_o = Q_1 + Q_2 + \ldots + Q_{64} \tag{4.10}$$

Equations (4.9) and (4.10) holds for perfect system linearity. The non-linearity NL (expressed in %) is obtained by evaluating the relative error between the arithmetic sum of the individual charge and the analog sum:

$$NL = \frac{Q_o - (Q_1 + Q_2 + \ldots + Q_{64})}{(Q_1 + Q_2 + \ldots + Q_{64})} \cdot 100 = \frac{Q_o - Q_s}{Q_s} \cdot 100 \tag{4.11}$$

Therefore, it is possible to obtain the total linearity curve simply by measuring the output charge for various levels of Q_i.

The setup described in the next section allows to illuminate each SiPM pixel individually by an array of 64 LEDs. For each charge value Q_i, different numbers of pixels can be excited to reach different values of Q_o (from 1 to 64 pixels). This is called a test run and implies two steps. In a first step, each pixel i is illuminated individually and the charge Q_i at the output is recorded for several shots. In a second step, the pixels of the previous step are illuminate simultaneously and the output charge Q_o is determined. The non-linearity (NL) is then obtained with equation (4.11) as:

$$NL = \frac{Q_o - \Sigma Q_i}{\Sigma Q_i} \cdot 100 \tag{4.12}$$

The NL values are determined for different values of Q_i with different numbers of excited pixels.

4.3.2 Setup

For the linearity characterization, a 64 channel light source illuminates the SiPM pixels and generates individual input signals at the ADC channel inputs (see figure 14).
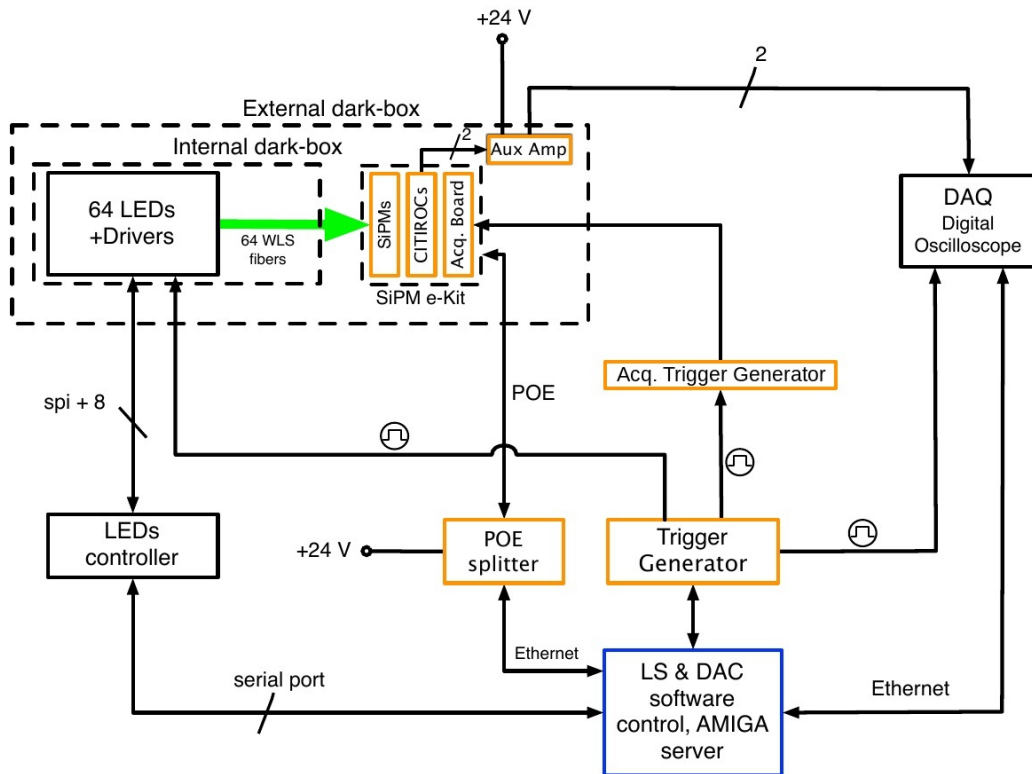

Figure 14. Setup for characterization of linearity. The outermost dashed line delimits the components inside the dark box: the 64 channel LED array (left) distributes the light via 64 fibers to the SiPM (right). Additional components for triggering are indicated by orange boxes. The computer for DAQ and test control (blue box) executes original AMIGA software routines.

This light source has been developed primarily for the MPPMT characterization and system test of the previous AMIGA electronics [43]. Each LED has its own analog driver; the amplitude of each driver is defined by an individual 12-bit DAC steered from a common microcontroller which can be programmed through a serial interface from the control computer. The value set for this DAC is called LSDAC (value). Each LED is connected by the same type of WLS optical fiber as used in the AMIGA modules to the corresponding SiPM pixel. The flexible design allows illumination of SiPM pixel simultaneously or sequentially with a wide range of amplitudes. Design details and explanation of the internal structure are given in [43]. The setup is complemented by the AMIGA SiPM electronics (e-kit) inside the light-tide darkbox and auxiliar electronics for synchronous distributing a trigger signal to the light source and the electronics.

Due to the different light couplings and the varying LED characteristics, individual channels provide different pulse charges for the same LSDAC values. It is thus necessary to determine in a pre-test the individual LSDAC values per pixel needed to obtain the same charge. It is important to note that these values are not used as a reference, but they are used as initial values to optimize the linearity measurement. To obtain these values, the AMIGA SiPM electronics under test was put inside the darkbox, coupled to the LEDs, and calibrated using the method explained in [12]. In this way, the electronics is configured as if it was installed at the Pierre Auger Observatory site.

As the binary channels (CITIROCs) and ADC channels measure in parallel, one analog output per CITIROC is connected to an independent auxiliary analog signal conditioning board (one per CITIROC) and from there, to the DSO[3] WavePro 715Zi [44] from LeCroy Corporation to acquire the SiPM pulse of each pixel. With this setup, individual pulses per SiPM pixel have been acquired. A light source sweep was performed on all 64 SiPM pixels for LSDAC values within the range of 1200 to 2450, in steps of 5. 1000 events per LSDAC value were acquired and for each acquisition the pulse charge was determined.
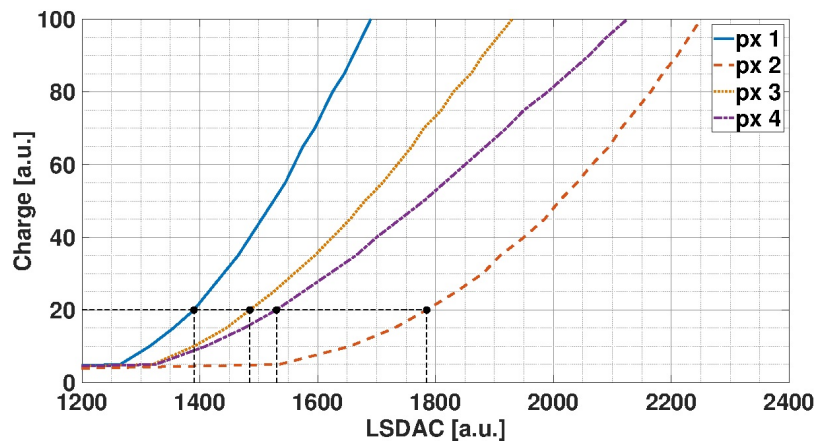

Figure 15. Average charges of the pulses as function of LSDAC values for four different pixels. The dispersion between pixels can be observed. The black dots represent the individual LSDAC values needed for a charge of 20 a.u.

The charge-vs-LSDAC values graph for four example pixels is shown in figure 15. As an example, the LSDAC values are indicated that yield a light level equivalent to a charge of 20 a.u.

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[3]Digital Storage Oscilloscope.

With this different LSDAC values per pixel, a table for every pixels was composed with 20 LSDAC steps (64 values per step) that generate a charge varying from 5 to 100, in 5 a.u. steps. These obtained LSDAC values are the ones used as initial values to perform the linearity curve measurement by using equation (4.11).

These LSDAC values are characteristic for every SiPM electronics, that means that the same process needs to be repeated for every electronics.

4.3.3 Linearity measurement

Once the LSDAC initial values have been determined, the ADC channels dynamic range characterization is performed following the method explained in section 4.3.1. It consists of obtaining the linearity curve for both HG and LG channels, and finding the section of the curve that gives information about the dynamic range of particle measurement. The AMIGA acquisition system (server-client programs) has been used for the acquisition of the test events. No auxiliary board or DSO was required for this measurement. Figure 16 shows a pulse produced by the light source (in blue) compared to a pulse produced by a muon (in orange) for HG (a) and LG (b) channels. Both pulses have a very similar structure and shape.
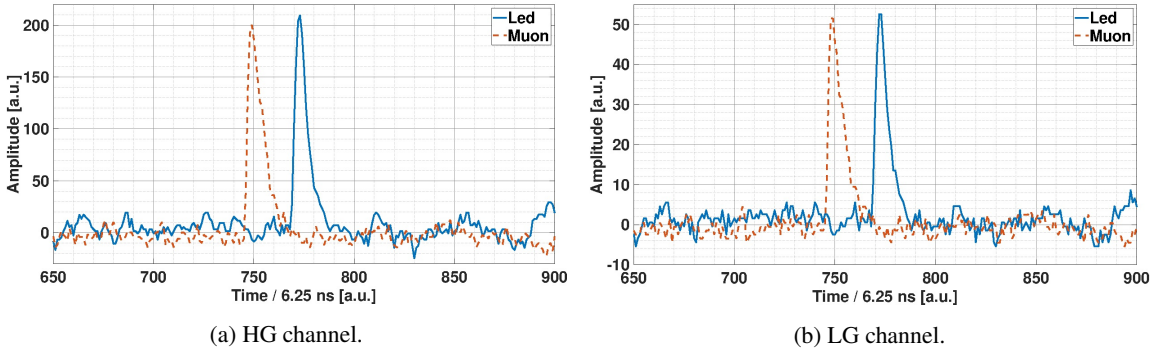

(a) HG channel.

(b) LG channel.

Figure 16. Comparison of a pulse induced by a muon and a pulse initiated after finding the initial LSDAC values for the light source. The pulse shape is very similar for HG and LG.

Different programs are responsible for configuring the light source, for controlling the signal generator that triggers the light source, the electronics and the synchronization of data acquisition, and for the control of event readout and storage. This setup emulates the worst saturation condition, i.e. a situation where all light signals arrive at the photo-sensor at the same time bin. Therefore, the linearity limits obtained with this measurement are the worst case scenario of the whole system, being improved under real conditions where the light arriving to the photo-sensor is spread over several time bins. The procedure used to measure the curves is as follows:

1. Configure the light intensity for each channel (LSDAC values) individually and trigger one at a time. Record N events per channels and calculate the distribution of the pulse charge.

2. The mean value Q_i of the distribution corresponds to the individual mean charge at the output when only the channel i is excited. This is repeated for the desired number of inputs L (for example, eight inputs, two inputs per adder).

3. With the same light intensity (i.e. the same LSDAC) as before, the L inputs are shot simultaneously and the same amount of N events are acquired.

4. A charge histogram is made and the mean value of the total charge Q_o is obtained. This value corresponds to the mean charge at the output when all L inputs receive a light signal.

5. Steps 1 to 4 are repeated for 20 different light intensities or LSDAC values.

Despite the high number of events, the measurement lasts only about 5 minutes. During this time, the environmental conditions don't change significantly, thus e.g. temperature effects are negligible.

To cover the whole range of the HG and LG channels, multiple linearity curves have been obtained: for low charges at a reduced number of inputs (L=4, single adder) up to very high charges (L=64 or 16 per adder), where the saturation is seen as deviation from linearity.

The linearity curve is obtained by measuring Q_o as a function of Q_s, where $Q_s = \sum_{i=1}^{L} Q_i$. When the relative error between Q_o and Q_s is greater than 5 %, the ADC channels are considered to be saturated. This non-linearity can equivalently be defined as a deviation of 5 % or more from the identity function $y = x$.

The measurements obtained in terms of charge are converted to number of equivalent simultaneous muons by using the mean muon charge values from figure 12 of section 4.2.1 (q_{avg}).

The first tests measured the linearity curve of each adder of the HG and LG setup (see section 3.1). Using the respective input channels of the adders (16 for each adder), the procedure described above was applied. The resulting plots of each adder for the HG and LG channels are shown in figure 17. Additionally, the identity function $y = x$ is shown as a reference. The saturation observed in the HG channel is expected due to its lower dynamic range, the LG channel does not present saturation. Within the limits of this test, the adders do not saturate individually, having a wide dynamic range for particle detection.
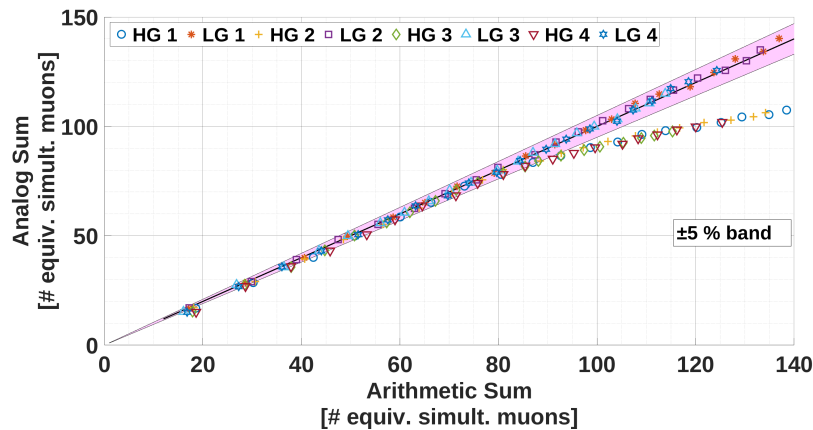

Figure 17. Linearity curves of the four adders. HG n and LG n are the linearity curve for adder n.

With additional tests, the complete linearity curves were found for HG and LG. As mentioned previously, in order to cover the entire range of admitted charges, several runs were made using a different number of inputs. For each new run, one more input was added for each of the four adders. In consequence, four inputs were added at a time, up to a total number of L = 60 inputs.

The complete linearity curves were obtained from the data of the sequence previously explained. Figure 18a shows the HG linearity curve. Saturation effects (deviation of $\geq 5\%$ from perfect linearity $y = x$) starts at a charge equivalent to 85 simultaneous muons. Above this equivalent charge value, the LG channels should be used. Figure 18b shows the LG linearity curve. Similarly, this channel starts to saturate from a charge equivalent to 362 simultaneous muons. It is important to note, that the minimum charge that the HG and LG channel can measure (≈ 1 muon) allows us to cross-characterize the total charge measurement with the muons number obtained by the binary channels.

(a) HG channel linearity curve. (b) LG channel linearity curve.
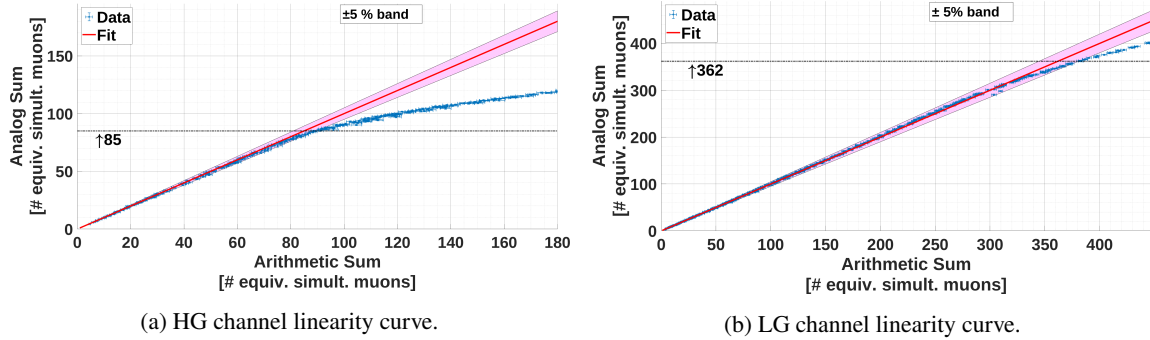
Figure 18. Linearity curves for HG (a) and LG (b) channels together with the identity function $y = x$ as a reference. The dashed line indicates the maximum muon value where the channel is linear within a 5% deviation band.

The observed non-linearity is caused by saturation of the electronic amplifiers. The linearity of SiPMs is quite well known and might be explored in future works.

4.4   On-site results

Data from one UMD station of the engineering array (see figure 19) have been analysed to verify its performance and validate the method of on-site characterization.

The selected station is equipped with eight modules (twin-type arrangement) that have SiPM as photodetector and is fully operational since October 2016. As this position is the first station that was completely equipped with SiPM electronics, the largest amount of data was acquired and stored. Thus, this stations provides the highest statistic for performance studies of the new front-end. The analysis takes into account data from four modules of $5\,m^2$ size (# 1, 2, 5 and 6) and four modules of $10\,m^2$ size (# 3, 4, 7 and 8). The modules of the station are grouped in southern modules (# 1 to 4) and northern modules (# 5 to 8). The analysis considers only events where energy, arrival direction and impact point on ground of the EAS could be reconstructed from SD-750 data of surrounding stations of the infill.

From those events, only showers with zenith angle $\theta \leq 45°$ and with energies $\geq 2 \times 10^{17}$ eV were analysed [34, 45]. The cut in zenith angle allows to minimize the attenuation effects and the statistical uncertainties due to the reduced scintillation-module detection area, while the cut in energy allows us to work in a regime of the full efficiency of the EAS array. No cut in distance to shower core is made. For the analysis of the binary channels data, corrections of the pile-up effect [46] and the time synchronization with the SD data have been done. The pile-up effect occurs when a single segment or scintillator bar is impacted by two or more particles simultaneously,
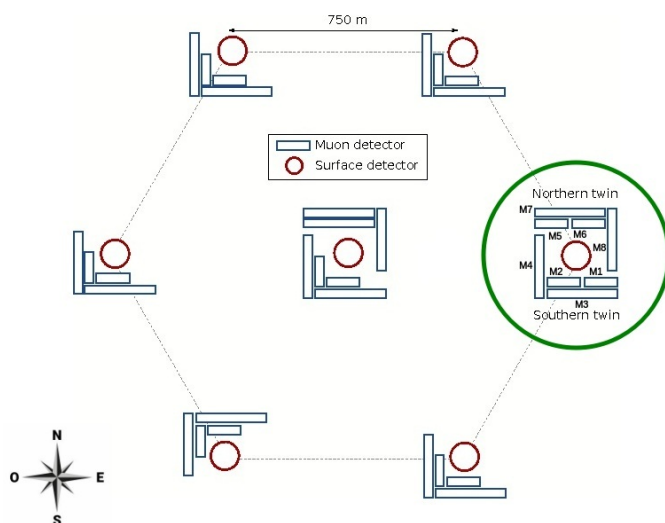
Figure 19. Sketch of the underground muon detector engineering array. Each circle represents a position of the SD detector and each rectangle represents a module of the UMD. The station with eight modules is used for this analysis (inside the green circle).

resulting in undercounting. Then, only events with muon numbers ≤ 85 and ≤ 362 measured by the binary channels were considered for the characterization of the HG and LG channels, respectively. Both cuts in muon numbers allow and ensure to analyse the ADC channels working within the linearity range (see section 4.3.3). The number of events found in the different modules after applying these selection criteria are given in table 3 for HG and LG.

Table 3. Number of events per module.

Events	HG	LG
M1	8043	8141
M2	7974	8077
M3	10013	10173
M4	10078	10240
M5	7970	8057
M6	7765	7853
M7	9249	9391
M8	10108	10291

The charge histograms of one muon for the HG and LG channels of the eight modules were determined by making the quotient between the measured charge and the number of muons obtained by the binary channels in the same event. Each histogram was fitted with equation (4.1) of the exponentially modified gaussian distribution as explained in section 4.2.1. The results are shown in figure 20 for the HG channel and in figure 21 for the LG channel, respectively (separate for the $5\,\mathrm{m}^2$ modules (a) and the $10\,\mathrm{m}^2$ modules (b)).
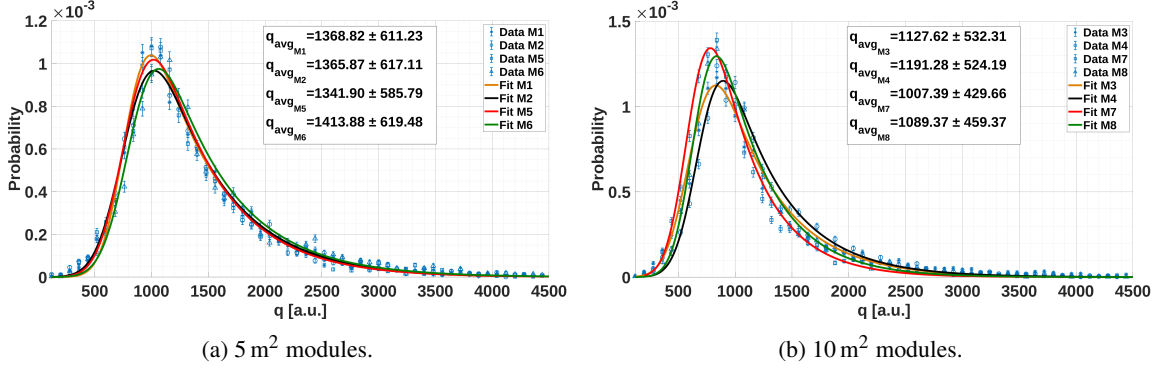
Figure 20. HG channel muon charge histograms for different modules. The data set corresponds to the period from May 2017 to December 2018.
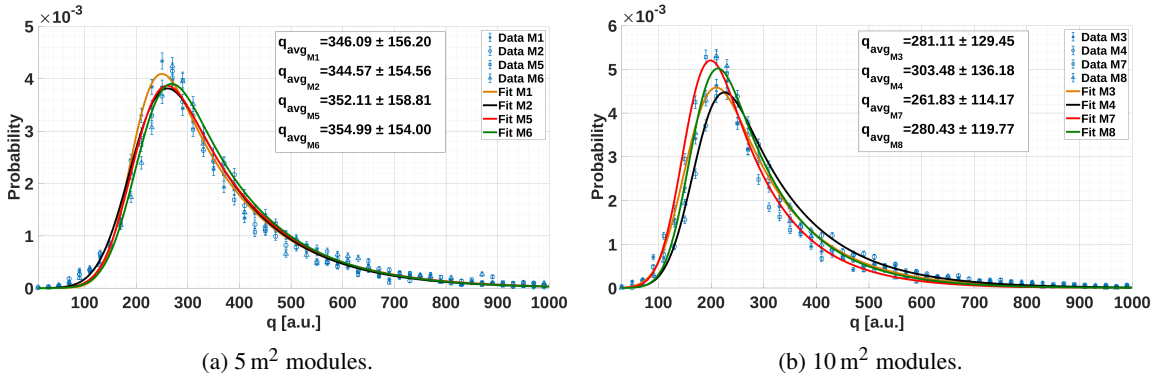

Figure 21. LG channel muon charge histograms for different modules. The data set corresponds to the period from May 2017 to December 2018.

From the figures, it can be seen that the mean muon charge value of the $5\,\text{m}^2$ modules is higher than the one of the $10\,\text{m}^2$ modules (for both HG and LG). This can be explained with the higher light attenuation in the larger modules. On average, the modules behave as if the muon impinges on the middle of the scintillation bar. Light needs to travel in $5\,\text{m}^2$ modules on average 1 m to the fiber end (2 m long scintillator bars), but 2 m in $10\,\text{m}^2$ modules (4 m long bars). Thus, the longer light path in larger modules lead to higher light attenuation. In consequence, the average charge measured in larger modules is lower.

The method of muon determination by total charge in HG and LG channels was verified by comparing groups of detector modules in the southern and in the northern part. Figure 22 compares the number of muons recorded in the southern part with those measured by northern part modules. The ratio of number of muons measured, $\hat{r}$, can be estimated by equation (4.13) [34, 45].

$$\hat{r} = \frac{\sum_{i=1}^{N}(\mu_{M1_i} + \mu_{M2_i} + \mu_{M3_i} + \mu_{M4_i})}{\sum_{j=1}^{N}(\mu_{M5_j} + \mu_{M6_j} + \mu_{M7_j} + \mu_{M8_j})} \tag{4.13}$$

Here μ_{M_i} is the muon equivalent value measured by the module M in the event i and N is the total number of events in the data set. $\hat{r}$ is a maximum likelihood estimator.

We have excluded events with a shower core closer than 200 m away from the analysis as in those events the high muon density gradient influences the muon counting in the 20 m separation between the groups of modules significantly. Such a cut in distance also limits the fluctuations of the muon density. However, no cuts in zenith angle and energy were applied and a total of 9809 and 9818 events were found in the HG and LG data set, respectively.

The ratios line fits show slopes of 0.976 ± 0.003 (HG) and 0.992 ± 0.003 (LG). A ratio close to unity proves an equal behaviour of both groups of modules and the consistency of the ADC channels design.

(a) HG channels.
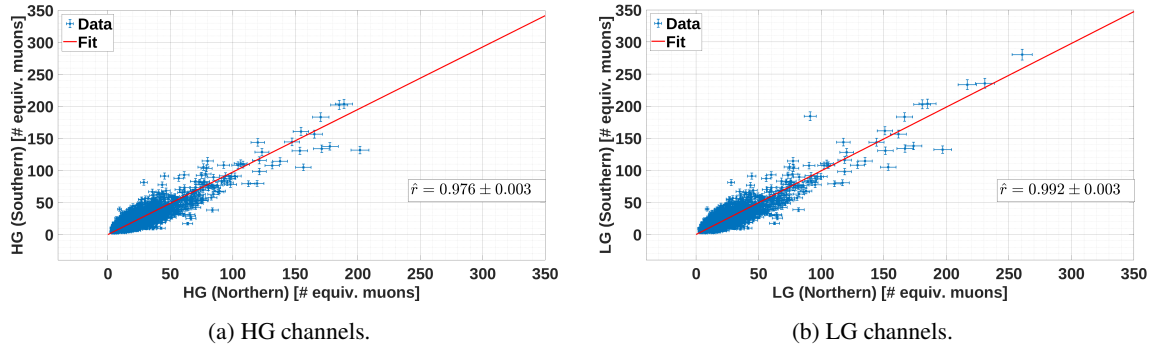
(b) LG channels.

Figure 22. Comparison of the muons measured in the southern modules versus northern modules for the HG (a) and LG (b) channels. The red line represents a strait line fit of the ratio.

Finally, figure 23 compares the number of muons measured by the HG and LG channels for $5\,m^2$ modules (a) and for $10\,m^2$ modules (b). The data sets of these plots are not restricted by any cut. Thus, the analysis was applied to about 200 000 events. The operating ranges of the ADC channels can be observed and have upper limits higher than those obtained in section 4.3.3. This behaviour is expected because the linearity curves were obtained under worst case condition (all light signals reach the SiPM at the same time bin). The analysis shows a saturation of the HG channel around 75 equivalent muons for the $5\,m^2$ modules, but of around 90–100 equivalent muons for the $10\,m^2$ modules. This difference can easily be explained by the higher light attenuation in the larger module, which shifts the saturation point.
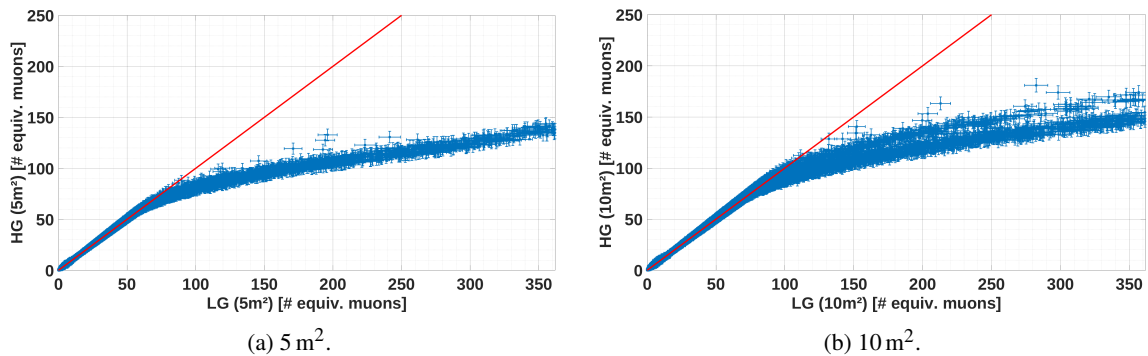

(a) $5\,m^2$.

(b) $10\,m^2$.

Figure 23. Comparison plot of HG vs LG for $5\,m^2$ and $10\,m^2$ modules. The red line represents equal response of HG and LG ($y(x) = x$). The HG channel saturates earlier for $5\,m^2$ modules than for the larger $10\,m^2$ modules.

4.5 Power consumption measurement

As mentioned in section 2.2, a low power consumption is one of the main design goals. The power consumption was measured for an input voltage range from 22 V to 36 V (AMIGA battery voltage range: 23 V to 32 V [16]) with the SiPM board connected to the front-end board. In the measurement, we recorded simultaneously the input voltage with the multimeter U1231A [47] (60 V full scale) and the input current with the multimeter U1242A [48] (100 mA full scale). Figure 24 shows the power consumption versus the input voltage. The power consumption increases with raising supply voltage from 1.83 W to 1.99 W, but it stays within the specification of maximal 2 W for the front-end board combined with the SiPM. The slightly higher power consumption for higher supply voltage can be explained by the lower efficiency of the DC/DC regulator at higher input voltage.
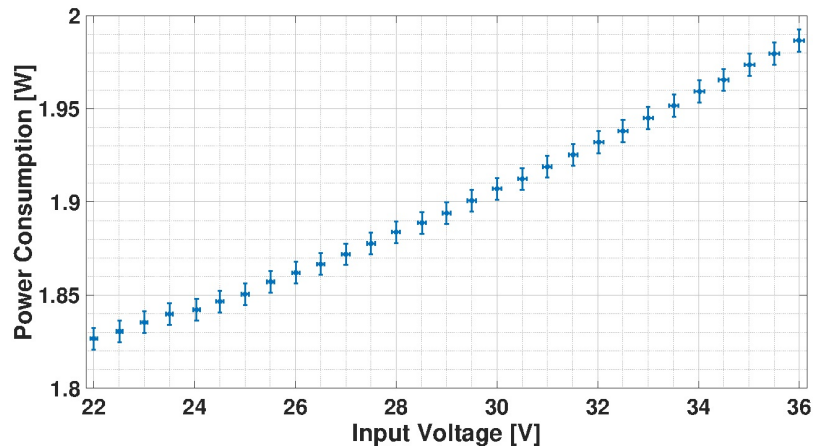
Figure 24. Power consumption versus front-end input voltage. All values are below 2 W along all voltage values.

5 Conclusions

This paper describes the design and the implementation of the front-end electronics for AMIGA in its production phase. The new front-end shows a higher dynamic range (detection of above 362 equivalent simultaneous muons) and higher efficiency (below 2 W for the full allowed supply voltage range) compared to the MPPMT front-end design tested in a prototyping phase. This was achieved by designing a dedicated power system and using high performance power supplies. Low-consumption and high performance ICs were used in all the design. The correct operation of these ICs is monitored by a slow control system based on a low sampling frequency ADC. Special care was taken in the design of the front-end including the mixed-signal PCB board, the power system and the connections with the SiPM and Back-end boards (special high-frequency connectors) to avoid digital interference and mismatch loses in the analog lines. The binary channels measurement system is based on [12]. This includes the SiPM power system (C11204-01 power supply), the SiPM ASIC (CITIROC) and the selected type of SiPM.

A new acquisition system based on charge measurement (ADC channels) was added to the design for enhanced dynamic range for particle detection. It is based on the measurement of the

charge produced by the impinging particles in the detector and the implementation is based on summation of all analog SiPM channels by operational amplifiers. Two differential amplifiers chains provide two channels of high gain (HG) and low gain (LG). The analog to digital conversion of these two channels is handled by the dual channel ADC ADS4246. The characterization method for the ADC channels requires to obtain the average charge deposited by a muon. With this value, the conversion of the measured charge to an equivalent muon number is performed. This characterization can be applied for measurements in the laboratory and for the installed electronics at the Pierre Auger Observatory site.

Laboratory measurements and on-site data analysis show highly consistent results. The dynamic range of the detector was extended according to the analysis of the laboratory data (up to ∼362 equivalent simultaneous muons). The ratio of number of muons measured between identical groups of detectors is close to one and this confirms the new front-end design. All results demonstrate an adequate performance of the charge measurement system.

Acknowledgments

A Schematics

A.1 CITIROC ASIC

Figure 25. Interfacing the CITIROC ASIC. The schematics is divided into 3 different parts: the analog part (all SiPM anodes), the digital part (digital outputs to back-end electronics) and the power supply part (including the power supply capacitors).

A.2 Non-isolated 5 V power supply

Figure 26. Schematics for the non-isolated 5 V power supply. The LM46002 regulator is a synchronous step-down DC/DC converter capable of driving a load currents of up to 2 A from an input voltage ranging from 3.5 V to 60 V. This option is appropriate in a photovoltaic system where the input voltage from battery is limited to a maximum of 32 V at full solar illumination. The CTRL_SW signal controls the power on/off of the converter.

A.3 Isolated 5 V power supply
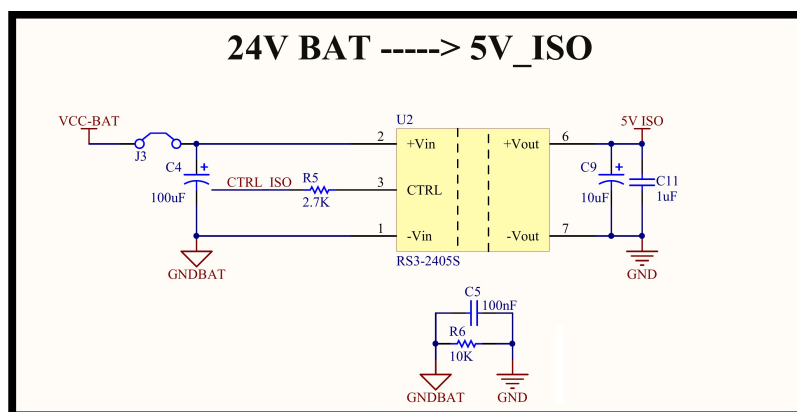
Figure 27. Schematics of the isolated 5 V power supply. The isolated DC/DC converter RS3-2405S is capable of driving up to 600 mA (3 W maximum output power) from an input voltage ranging from 18 V to 36 V. The galvanic isolation avoids ground loops. Capacitor C5 is needed to reduce the output voltage ripple and resistor R6 avoids problems with electrostatic discharge. The CTRL_ISO signal controls the power on/off of the converter.

A.4 SiPM power supply
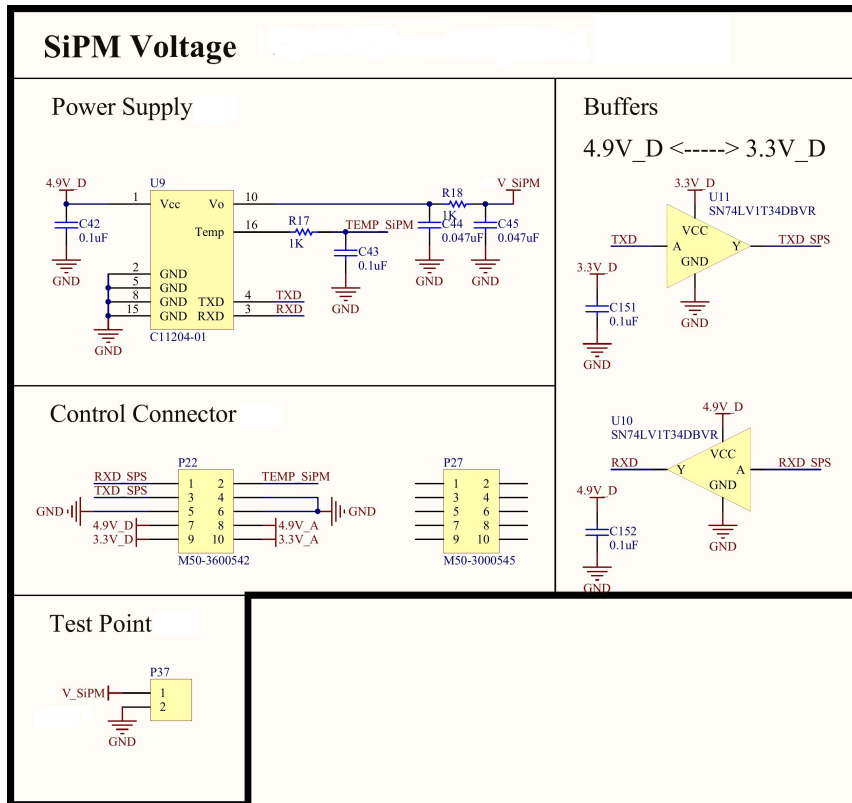
Figure 28. SiPM power supply schematics. The SN74LV1T34 [49] from Texas Instruments is a single supply buffer logic level shifter used to adapt the signal voltage levels of the 5 V SiPM power supply and the voltage levels of the back-end of 3.3 V.

A.5 Back-end power connector
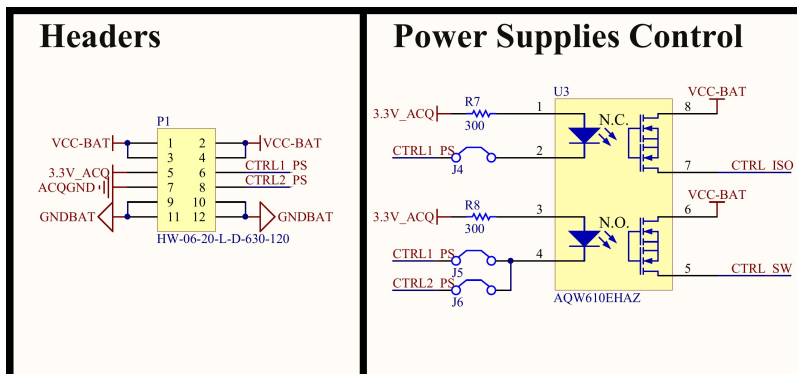
Figure 29. Back-end power connector schematics. The connector P1 is a high-temp flexible board stacker to provide the interface between the front-end and back-end boards. The back-end electronics controls the power on/off of the two converters explained in section 2.2 through optocouplers (right side) to avoid possible ground loops (galvanic isolation).

A.6 Slow control monitor system
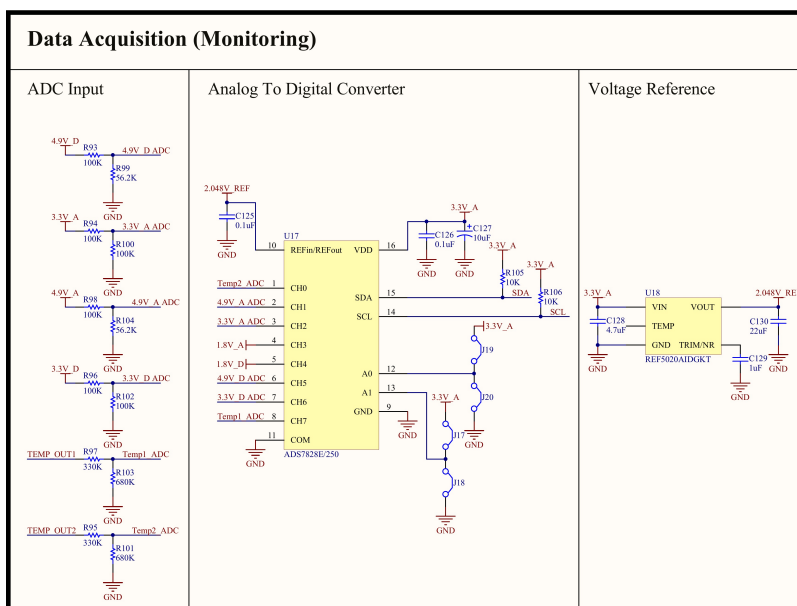
Figure 30. Slow control monitor system. The low power ADC measures all supply voltages of the board and the two temperature voltage outputs of both CITIROCs. A resistor divider at the ADC input adapts the range of the monitored voltages to the ADC input range given by an external 2.048 V voltage reference.

A.7 Adder amplifiers
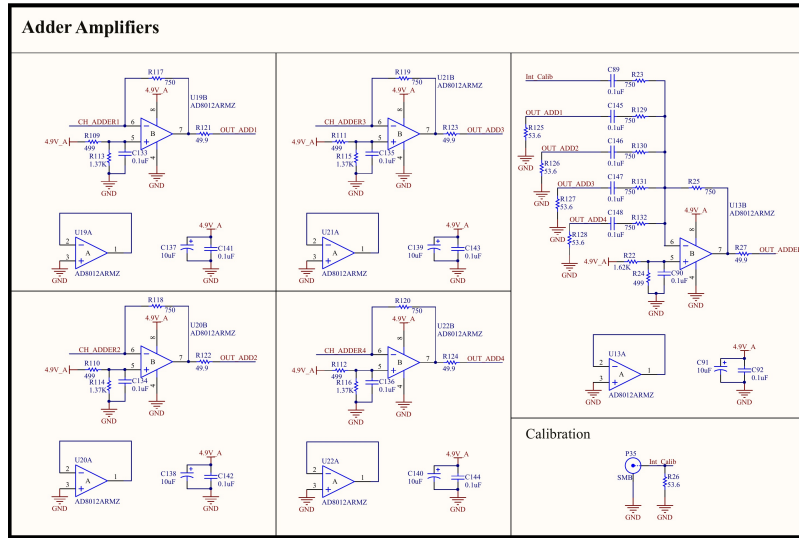
Figure 31. Adder amplifiers schematics. The four amplifiers on the left side (U19, U20, U21 and U22) add up the 64 SiPM anode signals in groups of 16 channels. The amplifier on the right side (U13) is the sum of the outputs of the four previous amplifiers. This amplifier provides a calibration input.

A.8 Differential output amplifiers
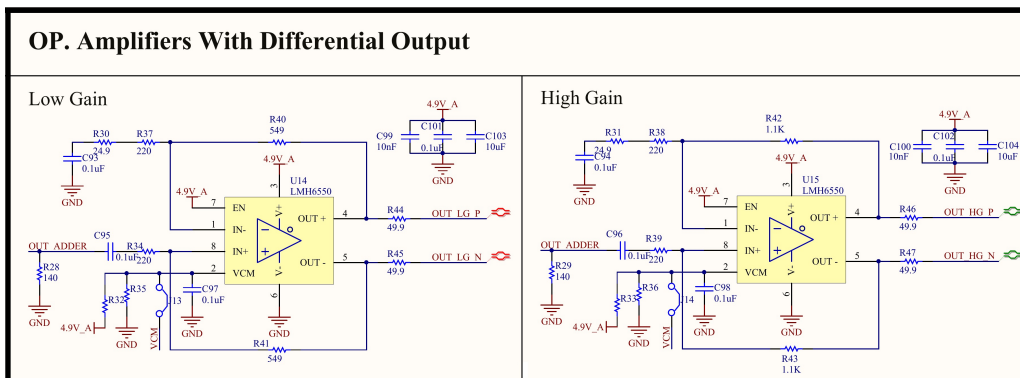
Figure 32. Differential output amplifiers schematics. At this stage, the ADC channels is divided into a high gain channel (right side amplifier) and a low gain channel (left side amplifier) branch.

A.9 Analog to digital converter
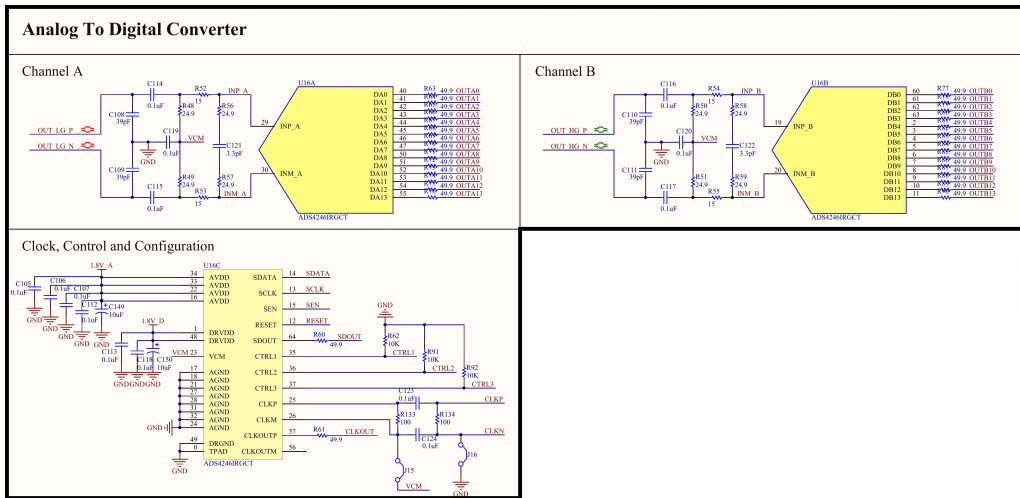
Figure 33. Analog to digital converter schematics. Each channels (high and low gain) is connected to one input of the ADC after passing through an anti-aliasing filter. The serial $49.9\,\Omega$ resistors on the channel outputs limit the output current at high capacitive loads.

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