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# Stabilization of the J-V Characteristic of a Perovskite Solar Cell Using an Intelligent Control Loop

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**Abstract**: The phenomena related to charge trapping are among the most relevant open issues that affect the long-term stability of perovskite-based devices. According to this, the objective of this paper is to report experimental results in which a charge control strategy is used for the first time in a solar cell structure that has a high trap density perovskite absorber. This device has also noticeable J-V hysteresis, produced by non-capacitive effects. The control strategy proposed, based on sigma-delta modulation, applies to the device an appropriate sequence of voltage waveforms determined after periodical current measurements made at a constant voltage. The experimental results obtained and the fittings made with a phenomenological model indicate that this approach allows controlling several charge-related effects. As a consequence, the J-V characteristic of the device is successfully shifted and stabilized to predetermined positions.

Keywords: perovskites; sigma-delta; charge control



In recent years, the use of perovskite materials in photovoltaic, optical and superconductor applications has experienced considerable growing interest. For instance, perovskite solar cells combine good performance with a relatively cheap manufacturing process. To obtain high efficiency and stability in single-junction perovskite solar cells, it is necessary to fabricate efficient charge transport and low charge recombination layers that improve the diffusion length of the charge carriers. In this way, very high power conversion efficiencies around 21% have been obtained [1,2], reaching recently a certified 25.2% for a single perovskite cell [3] and a 28% for a Perovskite-Silicon tandem cell [4].

However, serious reliability problems slow down the rise of this technology, being the biggest the performance degradation of the perovskite material [5–10]. There is a broad consensus in identifying environmental conditions, illumination, heat and electrical stress as factors that produce or exacerbate this degradation. Furthermore, several recent works indicate that the main cause of degradation in perovskite solar cells is the existence of charge trapping due to defects and vacancies in the material [10–14]. It can be said that trapped charge is among the most relevant open issues that affect the long-term stability of perovskite-based devices.

Trapped charge due to ionic vacancies is able to move through the perovskite layer and can also affect the interfaces with the electron and hole transport layers. Depending on the species involved, ionic vacancies can exhibit dynamics with different activation energies and time constants [15,16]. Additionally, electrostatic charges generated by light irradiation are trapped at grain boundaries producing irreversible degradation [12].



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**Copyright:** © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/). Most works try to improve perovskite stability by varying the fabrication process or the composition of the materials. For instance, a very comprehensive review of the progress made in the recent years to improve the stability and the photovoltaic performance of perovskite solar cells, based on improving materials and fabrication processes, can be found in [17].

However, a radical new approach is proposed here for the first time. It consists in using a sigma-delta loop to control the charge trapped in the perovskite layer, allowing one to place the J-V of the device at a previously desired and stable position. This strategy, inspired in one used to successfully controlling dielectric charge trapping effects in MOS capacitors in [18], may open a new way to mitigate perovskite degradation. Accordingly, in this work, a charge trapping control is applied to perovskite solar cell structures that suffer noticeable degradation effects. Specifically, this work investigates the feasibility of using a charge control to stabilize the J-V of the device even for this high ion density perovskite material.

To the best knowledge of the authors, this is the first time that the long-term drifts of the J-V characteristic of a solar cell have been controlled. The proposed control strategy can cope with the fast hysteretic transients due to non-capacitive effects in the device. The control capability depends on the J-V displacements and drifts generated by the bias voltages, which is a phenomenon that typically appears in perovskite or organic solar cells. By applying sigma–delta-like intelligent bias switching, the J-V characteristic is controlled around the desired point. The usual approach to stabilize the J-V characteristic is to improve the fabrication process of the device. In this regard, the proposed control is a new mitigation tool, not previously explored in the literature. Let us remark that other more application-specific objectives, such as mitigating the degradation of the relevant photovoltaic parameters, will be the objective of future work.

The paper is organized as follows: Section 2 describes the fabrication process of the solar cells, their structure, their J-V characteristics. These characteristics are fitted with an analytical model to determine the more relevant physical mechanisms present under both dark and illumination conditions. Section 2 also introduces the control method used in this work to control the displacement of the J-V curves. Finally, experimental results in which the control is applied in different conditions are presented and discussed in Section 3.

## 2. Materials and Methods

#### 2.1. Device Fabrication and Characterization

The perovskite solar cells used in this work have been fabricated in the facilities of the Institute of Photonic Science, ICFO. The fabrication process was as follows: patterned ITO substrates were first covered with a 2.5% wt in methanol TiO<sub>2</sub> nanoparticle precursor (20% wt in water). As in [19,20], the precursor was previously mixed with 2.5% wt of Ti diisopropoxide bis(acetylacetonate). Then, the perovskite was deposited as in [21], without adding the triiodide solution. Figure 1 shows a Field Emission Scanning Electron Microscopy (FESEM) image of the surface of the perovskite layer, obtained after its crystallization on top of the TiO<sub>2</sub> layer.

In the next step, a 72.3 mg/mL 2,2',7,7'-Tetrakis [N, N-di(4-methoxyphenyl) amino]-9,9'-spirobifluorene (Spiro-OMeTAD) solution in chlorobenzene with 17  $\mu$ L of a 520 mg/mL bis (trifluoromethylsulfonyl) amine Li salt solution in acetonitrile and 29  $\mu$ L of 4-tertbutylpyridine was spin-coated on top of the perovskite.

Finally, thermally evaporated gold was used as top electrode using a mask on the device to form an active area of  $0.06 \text{ cm}^2$ . The resulting stack of layers that make up the device is, from bottom to top: ITO (140 nm), TiO<sub>2</sub> (40 nm), perovskite (500 nm), Spiro-OMeTAD (200 nm) and Au (60 nm).



**Figure 1.** Field Emission Scanning Electron Microscopy (FESEM) image of the surface of the perovskite layer, obtained after its crystallization on top of the TiO<sub>2</sub> layer. The morphology of the material and the grain sizes and boundaries can be distinguished clearly.

Figure 2 shows the J-V curves measured in a device when a voltage scan rate of 440 mV/s is applied. The hysteresis-like distortion observed between the forward and reverse scans is typical of this type of devices [22–25], and it is basically due to ion diffusion through high density concentration of trap states at grain boundaries of the perovskite layer, which act as recombination centers.



**Figure 2.** J-V characteristics of a device in dark (**a**) and under  $100 \text{ mW/cm}^2$  illumination (**b**). The voltage scan rate used in these measurements is 440 mV/s. Due to limitations of the setup, the so-called dark results reported in this work have not been obtained in perfect darkness and, therefore, a very small photogenerated current is always present.

Moreover, the hysteresis observed in Figure 2 can be explained by accumulation of mobile ions near the electrodes, which alters the local charge status, then the J-V curves. For this shape of curves, trap density values in the perovskite absorber around 3.6 10<sup>10</sup> cm<sup>-2</sup> have been obtained in [26]. Besides, non-capacitive effects such as chemical interactions at contacts and corrosion can also produce noticeable J-V distortion even at fast scan rates [27]. Additionally, photo-generated carriers interplay with ionic species at contacts and enhance hysteresis-like responses under illumination.

In order to study the relevance of these effects in our case, let us use the general model for current in perovskite devices taken from [28]. This model includes terms accounting for hysteresis contributions, together with the usual solar cell operation, as follows:

$$J = J_d + J_{cap} + J_{non\_cap} \tag{1}$$

where  $J_d$  is the current for a diode working as a solar cell:

$$J_d = J_0 \left( e^{\frac{V - R_S J_d}{nV_t}} - 1 \right) + \frac{V - R_S J_d}{R_{sh}} - J_{ph}$$
(2)

where  $J_0$  is the reverse saturation current, V the voltage applied,  $R_S$  the series resistance,  $R_{sh}$  the shunt resistance,  $V_t$  the thermal voltage,  $J_{ph}$  the photo-generated current and n the ideality factor. This last value indicates the charge carrier recombination process that dominates solar cell operation. When n is close to 1, it indicates band to band recombination in the quasi-neutral region, whereas n close to 2 indicates Shockley–Read–Hall recombination through mid-gap trap centers in the depletion region.

In Equation (1), the hysteresis effect is modeled as two current contributions,  $J_{cap}$  and  $J_{non\_cap}$ . The first one is a capacitive current that accounts for the charge/discharge dynamics associated to ionic polarization at electrodes and electronic accumulation at surface layers. It can be written as:

$$J_{cap} = C(V) \cdot s \tag{3}$$

where *C* is the device capacitance, which typically depends on the voltage applied, and *s* the voltage scan rate used in the measurement. It must be noted that the capacitance also depends on the frequency, when sinusoidal excitations are applied.

On the other hand, *J*<sub>non\_cap</sub> is related to non-capacitive currents and it is usually adjusted with an empirical equation using the Nernst–Monod model [29], as follows:

$$J_{non\_cap} = \frac{J_{max}}{1 + e^{\frac{V - V_A}{nV_t}}}$$
(4)

where the characteristic voltage  $V_A$  is associated to reaction potential and establishes the current onset for these currents, modeled as  $J_{max}$ .

By fitting the experimental J-V curves of Figure 2 with the parameters of Equations (1) to (4), it is possible to evaluate the three current contributions and obtain information about the relevance of the mechanisms involved. Figure 3 shows the very good match obtained between the fittings and the measured J-V curves. The values of the parameters used in the fittings are summarized in Table 1.

Table 1. Values of the fitting parameters us	ed in Figure 3.
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	Dark, Forward	Dark, Reverse	Light, Forward	Light, Reverse
n	2	2	4.2	1.6
$J_0 [pA/cm^2]$	2	1.67	1.67	2.5
$R_S[\Omega]$	73	170	80	112
$R_{sh}$ [M $\Omega$ ]	1	2	0.01	0.04
$C \left[\mu F/cm^2\right]$	7.6	7.6	380	380
$J_{vh}$ [mA/cm <sup>2</sup> ]	0.057	0.057	22	22
$J_{max}$ [mA/cm <sup>2</sup> ]	0.067	83	83	$1.7 imes10^{-9}$
$V_A$ [V]	0.8	1.2	1.02	1.02



**Figure 3.** Measured and adjusted J-V characteristics in dark and under illumination. Dots correspond to experimental data, whereas blue-dashed lines correspond to values fitted with Equations (1) to (4).

For the dark J-V curves in, ideality factors around 2 are obtained. This agrees with typical P-I-N diode operation, where recombination is produced within the bulk-intrinsic layer [28]. Additionally, the measured J-V curves at forward and reverse scans separate from each other around 0.7 V. It is reported in [30] that this type of distortion is due to non-capacitive currents affecting the J-V at high voltages. Accordingly, a very good adjustment with the experimental data is obtained using Equation (4). On the other hand, in [30] it is also demonstrated that the capacitive currents produce hysteresis distortion around 0 V, but this type of effect is not observed in the experimental J-V curves of Figure 2.

For the J-V curves under illumination, ideality factors start from 4.2 for forward scan and decrease down to 1.5 for reverse scan. This evolution indicates a redistribution of mobile ions immediately following illumination that reduce the Shockley–Read–Hall recombination via shallow traps. Therefore, band to band recombination dominates current-voltage behavior in this case. This is probably due to huge accumulation of photo-generated carriers, which chemically interact near the interfaces, and also to interfacial recombination at the intrinsic layer [31]. Finally, between 0.5 V and 1 V the same hysteresis behavior seen in the dark case is observed, therefore indicating that non-capacitive effects are also dominant under illumination for relatively high voltages.

## 2.2. The Control Method

As commented above, the closed-loop control proposed in this work is a variant of that applied for controlling the effect of the charge trapped in dielectrics of MOS capacitors. The method uses the complementary effects on such charge that the application of different

voltages produces, and its objective is to set and maintain a certain level of charge, thus helping to stabilize the J-V characteristic of the device in the long term.

The control is implemented with a first-order sigma-delta loop, as described in Figure 4. The loop applies to the device the voltage waveforms BIT0 and BIT1, also shown in the figure. Note that in BIT0(BIT1), a voltage  $V_0(V_1)$  is applied for a time  $(1 - \delta)T_S$ , while  $V_C$  is applied for a shorter time  $\delta T_S$ , with  $0 < \delta < 1$ .



**Figure 4.** Top: Schematic of the sigma–delta control loop. Bottom: BIT0 and BIT1 voltage waveforms used. The current at the control voltage  $J(V_C)$  is measured at the end of each BIT0(BIT1) waveform application.

As will be shown later, in the devices used, the continuous application of  $V_0$ , and therefore of BIT0 waveforms, produces slow displacements to the right of the J-V curve. On the other hand, applying only  $V_1$ , or BIT1s, produces left displacements of the J-V. Then, taking advantage of this complementary behavior, the control measures periodically the displacement of the J-V and applies the appropriate sequence of BIT0s and BIT1s (bit stream) to keep it around a previously given, or target, position. The J-V position is inferred from a current measurement performed at the end of each BIT0(BIT1) waveform. To ensure that the measured results are comparable, this measurement is always made at a unique test voltage,  $V_C$ .

According to all this, the sigma–delta loop works as follows: depending on whether the current measured at the end of each BIT0(BIT1),  $J(V_C)_n$ , is above or below a previously given threshold value,  $J_{th}$ , either a BIT0 or a BIT1 is applied in the next time  $(n+1)T_S$ , following this decision law:

$$BIT_{n+1} = \begin{cases} BIT1 & when \ J(V_C)_n < J_{th} \\ BIT0 & otherwise \end{cases}$$
(5)

In the experiments, a Keysight 2912A Source and Measurement Unit has been used to both generate the voltage waveforms and perform the current measurements. The timing parameters  $T_S$  and  $\delta$  are chosen such that the voltage switching at the end of each BIT0(BIT1) waveform, necessary to measure  $J(V_C)_n$ , has little effect on the state of the device. On the other hand, the value of the test voltage  $V_C$  is chosen to ensure sufficient current sensibility.

### 3. Results and Discussion

The first experiment performed investigates how the application of BIT0 or BIT1 waveforms results in opposite shifts of the J-V. To this effect, the evolution of  $J(V_C)$  at  $V_C = 1.1$  V was monitored while an open-loop stress, consisting in applying either only

BIT0 or only BIT1 waveforms, was applied to the device in dark. The results obtained are shown in Figure 5. The parameters used in the BIT0 and BIT1 waveforms are:  $V_0 = 0.3$  V,  $V_1 = 0.7$  V,  $T_S = 400$  ms and  $\delta = 1/3$ . To set comparable initial conditions, the device was at 0 V bias for 15 min before each BIT0(BIT1) stress application.



**Figure 5.** (a) Evolution of the dark current at  $V_C = 1.1$  V when only BIT0 waveforms are applied to the device. (b) Same as previous, but when only BIT1 waveforms are applied. The BITx parameters used are:  $T_S = 400$  ms,  $\delta = 1/3$ ,  $V_0 = 0.3$  V,  $V_1 = 0.7$  V.

As seen in the results shown in Figure 5a, a BIT0 stress produces an initial-short increase of the current, then it slowly decreases. Then, the continuous application of BIT0s produces right J-V shifts. On the other hand, applying BIT1s produces left shifts of the J-V, as shown in Figure 5b.

## 3.1. Experiment Set 1: J-V Control in Dark

In the next experiment, a sequence of eight 5-h control steps, with a different  $J_{th}$  each, was applied to the device under dark conditions. The evolution of  $J(V_C)$  and the bit stream provided by the control loop were continuously monitored, and a fast J-V measurement was made at each step end. BIT0 and BIT1 parameters are:  $V_0 = 0.25$  V,  $V_1 = 0.75$  V,  $V_C = 1.1$  V,  $T_S = 400$  ms and  $\delta = 1/3$ .

The  $J_{th}$  values and the evolution of  $J(V_C)$  during the experiment are shown in Figure 6a. Note that all targets are achieved successfully: at each step, the current reaches very fast the desired level, then the control loop keeps the current around  $J_{th}$  by applying an appropriate sequence of BIT0s and BIT1s.

Besides, Figure 6b shows a zoom of the evolution of  $J(V_C)$  during the fourth step, where  $J_{th} = 2 \text{ mA/cm}^2$ . Each time  $J(V_C)$  is below  $J_{th}$ , the feedback loop applies BIT1s until the current goes above  $J_{th}$ . Once this happens, a BIT0 is then applied to decrease the current below  $J_{th}$ , and then BIT1s are again applied, etc. Let us note that this behavior is typical of 1st-order sigma–delta controllers [32,33]. Furthermore, this type of result closely resembles those obtained in previous works where sigma–delta loops were used to control trapped charge in dielectrics of other devices, such as MEMS switches [34,35] and MOS capacitors [18].



**Figure 6.** (a) Evolution of  $J(V_C)$  in dark while control is applied with the sequence of  $J_{th}$  values listed in the table (also green line); (b) Zoom of  $J(V_C)$  for a short time interval within step 4; (c) Average bit stream provided by the control loop during the experiment. The BITx parameters used are:  $V_0 = 0.25$  V,  $V_1 = 0.75$  V,  $V_C = 1.1$  V,  $T_S = 400$  ms,  $\delta = 1/3$ .

The average bit stream generated by the control loop during the experiment is plotted in Figure 6c. It can be seen that the higher the level of  $J_{th}$  is, the higher the injection of BIT1s becomes; and that the bit stream exhibits slow time evolution once the control targets are reached. The fall to zero distortions of Figure 6c are due to the J-V measurements made at each step end, which produce short discontinuities in the experimental data.

The J-V curves obtained, plotted in Figure 7, show that the control allows to set and maintain successfully their positions around the desired thresholds. Note that the instantaneous current has a small deviation from the desired value that is mainly due to the voltage sweep applied to perform the J-V measurement.



Figure 7. J-V curves obtained at each step end in the experiment of Figure 6.

Figure 8 shows the good adjustment between the experimental J-V characteristics and the fittings performed using Equations (1) to (4). The changes of the curves at different steps are mainly due to small changes of the characteristic voltage  $V_A$  used in the Nernst-Monod model for non-capacitive currents, which in this case varies between 1.2 and 1.35 V (step 1: 1.35 V; step 2: 1.25 V; step 3: 1.23 V; step 4: 1.28 V; step 5: 1.26 V; step 6: 1.21 V; step 7: 1.27 V; step 8: 1.20 V). This parameter is usually related to chemical ionic interactions at the perovskite-interlayer interfaces, which may cause accumulation of charge or defects in these interfaces and even in the contacts. All this, in the long term, produces a degradation of the overall performance of the solar cell. However, in our case the material used in the contacts is gold and, therefore, contact degradation can be ruled out. It is then concluded that setting adequate values of the threshold  $J_{th}$  can allow to control perovskite-interlayer interface ionic interactions and, consequently, help to mitigate their effect on device degradation.



**Figure 8.** Measured and adjusted J-V characteristics in dark after each control step in the experiment of Figures 5 and 6. Dots correspond to experimental data, whereas lines correspond to values fitted with Equations (1) to (4).

The objective of the next experiment is to investigate the influence of the sampling time,  $T_S$ , in the effectiveness of the control. To this effect, the control was applied in two consecutive 4-h steps, with the same threshold  $J_{th} = 3 \text{ mA/cm}^2$  and two values of  $T_S$ . The other BIT0 and BIT1 parameters are the same as in the experiment reported in Figures 5 and 6.

Figure 9 shows the evolution of  $J(V_C)$  and the average bit stream obtained. A plateaulike behavior is clearly observed for  $T_S = 1$  s: the bit stream is stacked at zero—which means same average number of BIT0s and BIT1s—while  $J(V_C)$  is varying and, therefore, no control is obtained. In perfect agreement with sigma-delta theory [32,33], reducing  $T_S$ mitigates this undesired effect, as seen in the next 4 h step for  $T_S = 400$  ms, where plateaus or their effects are no longer observed.



**Figure 9.** Evolution of  $J(V_C)$  (**a**) and of the average bit stream (**b**) in dark, while control is being applied with  $J_{th} = 3 \text{ mA/cm}^2$  (green line) and two values of  $T_S$ . The other BITx parameters used are:  $V_0 = 0.25 \text{ V}$ ,  $V_1 = 0.75 \text{ V}$ ,  $V_C = 1.1 \text{ V}$ .

## 3.2. Experiment Set 2: J-V Control under Illumination

In order to investigate the effectiveness of the control for devices under illumination, the following experiment was performed: a sequence of twelve different values of  $J_{th}$  were applied to the device in consecutive 1-h steps. A fast J-V measurement was performed at each step end. The BIT0 and BIT1 parameters used are:  $V_0 = 0.25$  V,  $V_1 = 0.75$  V,  $V_C = 1.2$  V,  $T_S = 400$  ms and  $\delta = 1/3$ .

Figure 10 shows the evolution of  $J(V_C)$  and of the average bit stream. Each time  $J_{th}$  changes, the control loop has been successful in reaching and maintaining the new desired level. For example, it can be observed that in order to achieve the lower current levels, more BIT0 waveforms need to be injected, resulting in lower average bit stream values. It is also seen that the control is lost due to a plateau-related episode for some time in step 7.



**Figure 10.** (a) Evolution of  $J(V_C)$  under illumination while control is being applied with the  $J_{th}$  values listed in the table (also green line). The green line represents the  $J_{th}$  levels. (b) Average bit stream provided by the control loop during the experiment. The BITx parameters used are:  $V_0 = 0.25$  V,  $V_1 = 0.75$  V,  $V_C = 1.2$  V,  $T_S = 400$  ms,  $\delta = 1/3$ .

Figure 11 shows the sequence of J-V curves measured at each step end. The same complementary behavior seen when applying BIT0s or BIT1s in dark is observed under illumination, therefore enabling the control to successfully place the J-V to the desired positions.



Figure 11. J-V curves measured at each step-end in the experiment of Figure 10.

As it was done in the case of control in dark, fittings of the results of this control experiment under illumination with the analytical model provided by Equations (1) to (4)



have also been carried out. Figure 12 shows the good adjustment between the experimental J-V characteristics and the fittings for the odd steps of the experiment.

**Figure 12.** Measured and adjusted J-V characteristics under illumination after some of the control steps in the experiment of Figures 9 and 10. Dots correspond to experimental data, whereas lines correspond to values fitted with Equations (1) to (4).

In contrast with the dark case of Figure 8, here no noticeable variation of the activation voltage  $V_A$  is detected and the effect of the control applied is a variation of the series resistance,  $R_S$ . Specifically, the values found for steps #1 to #12 of the experiment are 46, 45, 44, 40, 39.5, 38, 35.5, 34.5, 32, 29, 31 and 33  $\Omega$ , respectively. Since the ideality factor *n* is constant to 4.2, it could be concluded that, under illumination, huge photo-generated carriers produce mobile ions that recombine via shallow traps, which affect the series resistance [28,31,36]. Then, the BIT waveforms applied by the loop allow to control this charge-related phenomenon and therefore stabilize the J-V characteristic.

It must be noted that the hysteresis and the long-term stability of the perovskite solar cells are phenomena generally not related. On the other hand, both aspects manifest themselves in the control plots presented in Figures 6, 9 and 10. The fast switching applied by the control generates fast current variations at the test voltage. This phenomenon can be linked to the hysteretic behavior observed in Figures 2 and 3, which has fast dynamics, as compared with long term drifts. Additionally, the controls also show long-term variations in their average values (see for example the time evolution in the first 5-h segment of the average bit stream in Figure 6). This slow time evolution can be associated with trapped charge, which is a phenomenon typically linked to the long-term reliability of the device. In any case, the possible reliability improvement that this type of controls might generate will be the subject of further research.

## 4. Conclusions

An intelligent control method, based on sigma-delta modulation, has been applied successfully to a solar cell structure that has a high trap density perovskite absorber. The J-V curves of the device exhibit noticeable hysteresis behavior at high voltages, which is mostly due to non-capacitive currents. The control capability relies on the complementary J-V shifting produced by the voltages applied. The experimental results obtained demonstrate that the control allows to displace and maintain the J-V of the device to a desired point, both under dark and illumination conditions.

To the knowledge of the authors, this is the first time that charge control has been applied to a perovskite solar cell. This may be seen as a new way to improve the stability of perovskite-based devices.

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