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THE USAGE OF A SYSTEM ON A CHIP FOR THE SYNTHESIS OF RADAR

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Most developers who work with DSP tasks face the problem of lack of computing resources for implementing hardware solutions for image processing or synthesis. One way to accelerate computing is to use specialized hardware that has significant computing resources.

One of the priority tasks of the world community at present is to ensure global monitoring of the Earth. Considering the fact that the territory of the Republic of Belarus 70% of the time in a year is covered with clouds, for continuous monitoring of the earth's surface, radar monitoring is very actual, realized at any time of the day and under any meteorological conditions.

Advantages of radar sounding are that they are a means of detecting physical properties of objects in microwave ranges of waves and a measuring tool with the possibilities of using phase information, applying a wide range of survey modes and algorithms for data processing. This allows us to significantly expand the scope of applied problems in scientific and economic spheres, monitoring of disasters and emergency situations, and ensuring state security.

The problem of the formation of the earth's surface radar image (RI) in real time remains one of the urgent tasks in solving the problems of remote sensing of the Earth (ERS).

One of the basic requirements for the hardware of the RI formation is high performance. To achieve high computation speed is possible with the help of parallel calculation methods, which in most cases are realized by means of specialized integrated circuits (ICs), such as FPGA.

A promising trend in improving computing performance in recent years is the usage of systems on a chip (SoC). SoC is an IC containing a processor, some memory, a number of peripherals and interfaces, and FPGAs. The main feature of SoC is the usage of the processor system as a device for controlling the process of information processing, which is implemented on FPGAs.

The algorithm for accelerated preprocessing of input signals for RI implementation obtained on SoC is shown in Fig. 1.

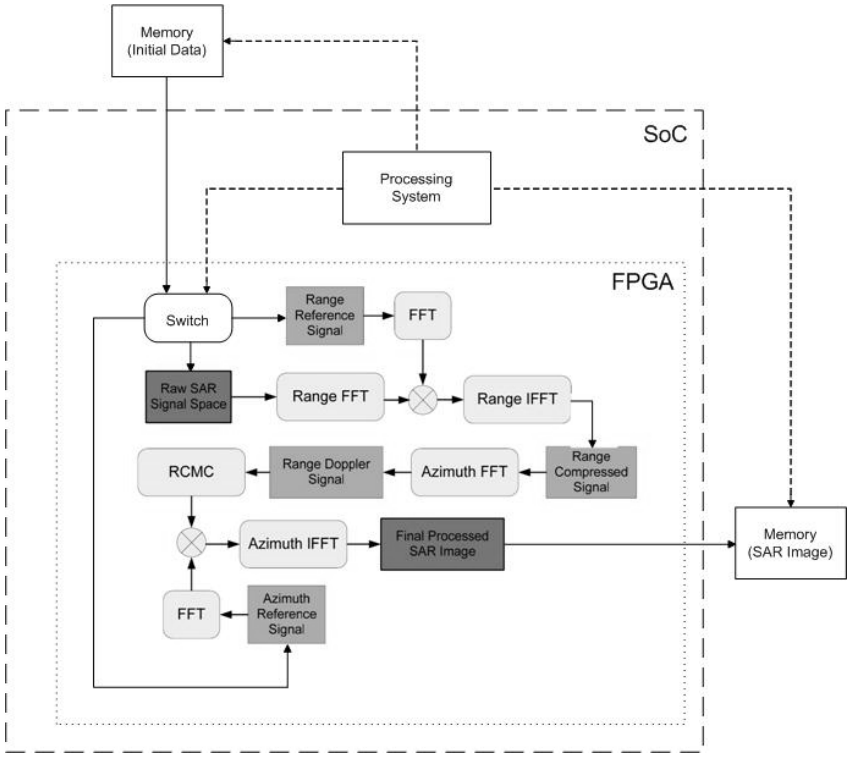

Fig. 1. The algorithm for accelerated preprocessing of input signals for RI implementation obtained on SoC

The original data is transferred from the memory to the switch, which splits this data into groups to form the filter reference functions and synthesize the image.

The two-dimensional signal is first analyzed as a series range time signals for each azimuth bin. Each range time signal undergoes matched filtering in the range frequency/azimuth time domain through range FFTs applied to the range time signals. After each signal is transformed back into the range time/azimuth time domain, the result is the range compressed signal as the matched filtering which is performed in the range frequency domain. In order to obtain azimuth compression, azimuth matched filtering must be performed. The range compressed signal is then composed into a series of signals with respect to azimuth time at different range bins. Each azimuth signal is Fourier transformed via an azimuth FFT and RCMC is performed before azimuth matched filtering in the range-Doppler domain. After azimuth matched filtering of each signal and azimuth inverse fast Fourier transforms (IFFTs), the final target image is obtained [1]. The resulting image is stored in memory.

Control is carried out by a processor system.

Data received by the spacecraft are presented in memory in the format of CEOS (Committee on Earth Observation Satellites).

To represent the ERS radar data in the CEOS format, a structure of four files is used (Fig. 2): Volume directory file, Leader file, Data set file, Null volume file. Each file contains records with the first 12 bytes of the same structure and include information on the sequential number of the record (from the first to the fourth byte), the type of the write code for its identification during processing, located from the fifth to the eighth byte (CEOS code), and the length records (from the ninth to the twelfth byte).

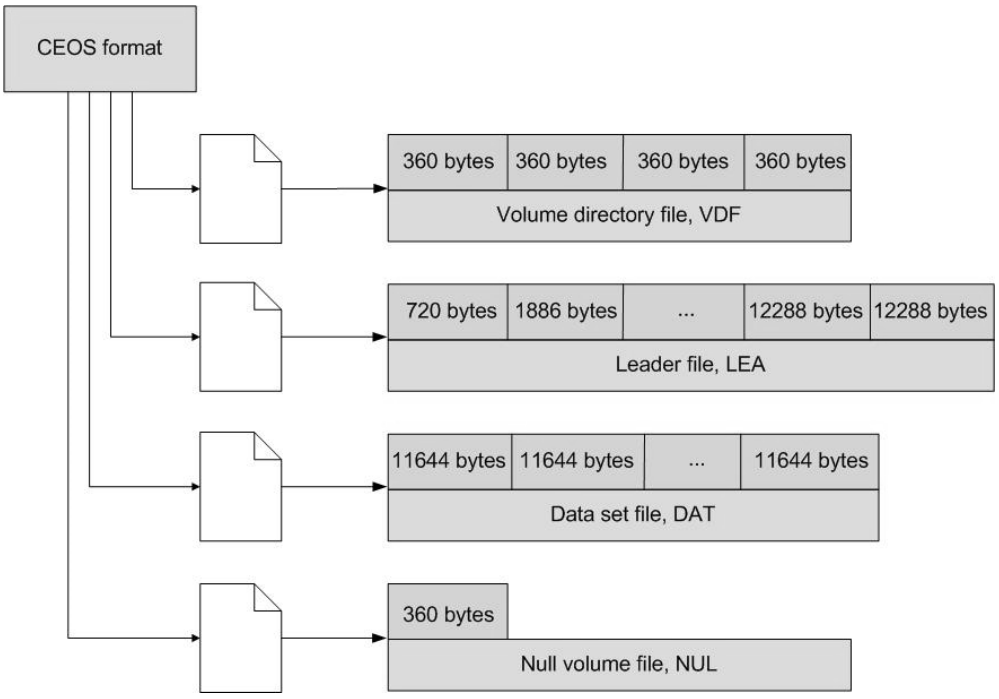

Fig. 2. Presentation of ERS radar data in CEOS format

The volume directory file contains a record of its description, a record of the pointer to the header file, a record of the pointer to the data file, a text entry.

The header file includes a description record, a record of raw data, a record with raw platform position data, a general-type data record for the radar, and a qualitative-type data record for the radar.

The data set file includes a record of the file description and a set of raw data records.

The null volume file contains a description of the file that includes the physical and logical volume identifiers, the number of volumes, their sequence numbers, date, time, country, volume creation organization [2].

Conclusion. The usage of SoC based on FPGA gives a wide range of possibilities for the implementation of complex projects requiring significant computational costs. The processor system of SoC can perform interface organization, load coefficients and other operations that are difficult to implement in hardware. Also, a single

processor core can manage several hundred DSP-blocks of FPGA that continuously process the input data stream.

This approach makes possible to use more modern adaptive algorithms for digital processing of the trajectory signal and image, which will solve the problem of the formation of a qualitative radar image.

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