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Ott, J.

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Processing of AC-coupled n-in-p pixel detectors on MCz silicon using atomic layer deposited aluminium oxide

J. Ott[a,b], A. Gädda[a,c], S. Bharthuar[a], E. Brücken[a], M. Golovleva[a,d], J. Härkönen[e],
M. Kalliokoski[e], A. Karadzhinova-Ferrer[e], S. Kirschenmann[a], V. Litichevskyi[a], P. Luukka[a],
L. Martikainen[a], T. Naaranoja[a]

[a] *Helsinki Institute of Physics, Gustaf Hällströmin katu 2, FI-00014 University of Helsinki, Finland*
[b] *Aalto University, Department of Electronics and Nanoengineering, Tietotie 3, FI-02150 Espoo, Finland*
[c] *Advacam Oy, Tietotie 3 (P.O. Box 1000), FI-02044 VTT, Finland*
[d] *Lappeenranta University of Technology, Skinnarilankatu 34, FI-53850 Lappeenranta, Finland*
[e] *Ruđer Bošković Institute, Bijenička cesta 54, HR-10000 Zagreb, Croatia*

Abstract

We report on the fabrication of capacitively (AC) coupled n^+-in-p pixel detectors on magnetic Czochralski silicon substrates. In our devices, we employ a layer of aluminium oxide (Al_2O_3) grown by atomic layer deposition (ALD) as dielectric and field insulator, instead of the commonly used silicon dioxide (SiO_2). As shown in earlier research, Al_2O_3 thin films exhibit high negative oxide charge, and can thus serve as a substitute for p-stop/p-spray insulation implants between pixels. In addition, they provide far higher capacitance densities than SiO_2 due to their high dielectric constant, permitting more efficient capacitive coupling of pixels. Furthermore, metallic titanium nitride (TiN) bias resistors are presented as an alternative to punch-through or poly-Si resistors.

Devices obtained by the above mentioned process are characterized by capacitance-voltage and current-voltage measurements, and by 2 MeV proton microprobe. Results show the expected high negative charge of the Al_2O_3 dielectric, uniform charge collection efficiency over large areas of pixels, and acceptable leakage current densities.

Keywords: Atomic Layer Deposition (ALD), Al_2O_3, pixel detector, capacitive coupling

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Email address: `jennifer.ott@helsinki.fi` (J. Ott)

1. Introduction

Upon transition to the HL-LHC in 2026, the radiation levels at the innermost silicon layers of the experiments' tracking detectors will increase up to e.g. 2.3×10^{16} $n_{eq}cm^{-2}$, or 12 MGy, in the CMS Tracker detector [1]. Due to extensive radiation damage to the silicon material caused in these conditions, the charge carrier trapping time and electron saturation drift velocity product will limit the distance where the signal charge is collected. The degradation of detector efficiency can be prevented through the detector design, by decreasing the pixel pitch to be comparable with charge collection distance, and optimizing the geometry to enhance weighting field effects [2]. This also provides better spatial resolution through increased granularity of the detector.

Approaches in defect-engineering of Si towards higher radiation hardness include the use of substrates grown by the magnetic Czochralski (MCz) method, where the Si ingot is pulled from a melt in a quartz crucible and therefore has an intrinsically higher oxygen concentration of around (5-10)$\times10^{17}$ cm^{-3}. MCz silicon substrates have exhibited better radiation tolerance than detectors grown by the dominantly used float zone (Fz) method and are thus a candidate for application in HL-LHC conditions [3, 4].

When considering the reduction of pixel size in order to counter the decrease in charge collection distance after irradiation of the detector, one challenge is the need for electrical insulation between pixels. To benefit from the higher mobility of electrons compared to the holes in Si, modern detectors are realized with segmented n^+ implants, on a p-type substrate. However, the traditionally used field insulator dielectric in pixel detectors, silicon dioxide (SiO_2) obtained by thermal oxidation, possesses a weak positive oxide charge that increases with irradiation [5, 6]. In reverse-biased n-in-p detectors, this positive charge would lead to a loss of spatial resolution, as the electron-collecting segments are effectively connected to each other. This is usually avoided by the use of an additional p-type implant between the pixels, referred to as p-spray or p-stop, depending on its width and concentration. However, p-spray/p-stop implants require additional implantation and high-temperature process steps, as well as more space on the detector.

An alternative to the combination of SiO_2 and insulation p^+ implants is the use of a different oxide with negative charge. The main candidate is aluminium oxide (Al_2O_3), which is widely used as surface passivation layer in the silicon photovoltaics industry [7]. The superior performance of Al_2O_3 includes contribution from both chemical passivation by termination of dangling bonds on the Si surface, and field-effect passivation due to its high negative oxide charge, which repels electrons and therefore prevents them from recombining at remaining interface and near-interface defects [8, 9].

One established way to fabricate Al_2O_3 thin films is by atomic layer deposition (ALD). This method is based on the successive, separated, and self-terminating gas-solid reactions of typically two gaseous precursors separated by a purge of inert gas [10–12]. An example schematic visualizing the growth of a layer of Al_2O_3 in tri-methyl aluminum (TMA, $Al(CH_3)_3$) + H_2O process, one of the most well-known ALD processes [13], is shown in Figure 1.

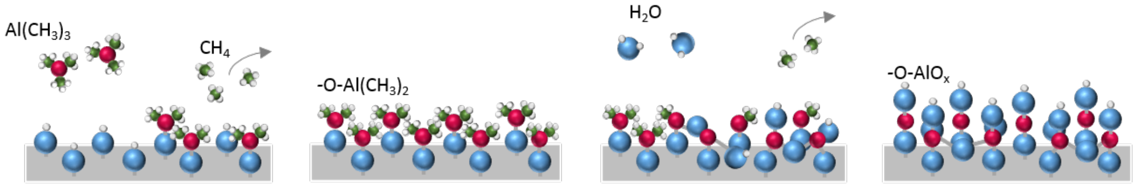


Figure 1: Illustration representing one ALD cycle of the Al_2O_3 process using TMA and water.

The use of Al_2O_3 deposited by ALD in particle and radiation detectors has been demonstrated for Si photodiodes [14] and for strip detectors [15, 16], and has been proposed also for pixel detectors [17]. This paper presents in detail the fabrication process of pixel detectors and reference structures on high-resistivity MCz silicon using Al_2O_3 thin films as field insulator and passivation layers. In addition, titanium nitride (TiN) thin film biasing resistors are used in place of standard punch-through or poly-Si resistors. As opposed to [16], where Al_2O_3 was applied after conventional strip detector processing, following our previous work [15, 17] Al_2O_3 was fully integrated into the detector fabrication process, without any remaining SiO_2 in the final devices.

2. Detector processing

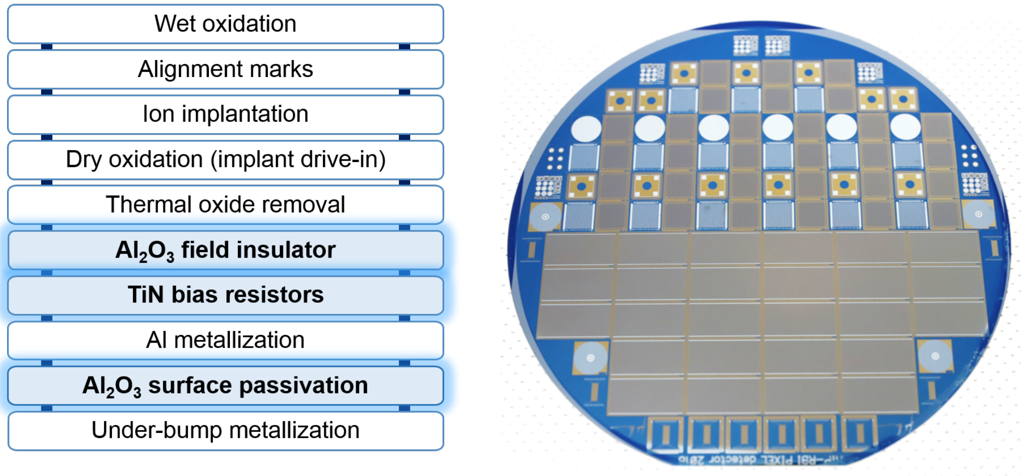
Detector fabrication was carried out in the facilities of Micronova Nanofabrication Centre. The process was implemented on 6-inch Magnetic Czochralski silicon wafers supplied by Okmetic Oyj, with a thickness of 320 μm and crystal orientation <100>. The wafers were boron-doped to a resistivity specified as 4-8 kΩcm.

The wafer layout consisted of the following devices:

- AC-coupled detectors with 4160 pixels in a 80 × 52 double-column structure, with pixel pitch 100 μm resp. 150 μm, to match the CMS PSI46dig read-out chip used in the Phase I pixel detector upgrade [18].

- DC-coupled pixel detectors with 400 × 192 pixels of 50 × 50 μm^2 pixel pitch, corresponding to the geometry of the RD53A read-out chip [19].
- 7 × 7 mm^2 pad diodes with broader central guard ring and a series of outer guard rings.
- MOS capacitors with diameter of 9.4 mm.
- Arrays of various test components, most importantly single-pixel biasing resistor structures.

A schematic presentation of processing steps is shown in Figure 2a, with a fully processed wafer in Figure 2b. The highlighted boxes represent the steps which are presented as a novelty to pixel detector processing in this article, and are discussed in more details in separate subsections. The other steps are summarized below. Lithography was carried out by standard techniques including priming, resist development, baking, and resist stripping. Photoresist patterning was performed with a mask aligner in soft-contact mode.



(a) (b)

Figure 2: a) Schematic of the detector process flow presented in this paper. b) Photograph of a full 6-inch wafer before dicing.

First, wafers underwent wet oxidation at 1000 °C in order to obtain an approximately 300 nm thick thermal oxide as hard mask for ion implantation. The oxidation was preceded by standard chemical cleaning sequence (RCA cleaning) [20]. Alignment marks were etched by reactive ion etching (RIE), using CHF_3 and SF_6 ions to etch SiO_2 and Si, respectively. For ion implantation, the SiO_2 on the wafer front surface was patterned by wet etching with a buffered hydrofluoric acid (BHF) etchant solution at 30 °C. The oxide on the back surface was removed completely. Ion implantation was carried out in an Eaton 8200 Ion implanter, implanting the front side with 60 keV phosphorous ions and the back side with 20 keV boron ions, both to target total doses of $1 \times 10^{15}\,\mathrm{cm}^{-2}$. After implantation, the mask oxide was etched away with BHF, the wafers were RCA-cleaned, and subjected to a 46 min anneal at 1100 °C in dry oxidation conditions, in order to diffuse the implanted ions deeper into the bulk. The resulting fresh thermal SiO_2 was again removed with BHF, and RCA cleaning was repeated. This was followed by the deposition and patterning of Al_2O_3 as field insulator and titanium nitride as bias resistor material (cf. Subsections 2.1 and 2.2). For the metal contacts, aluminium was deposited by direct current (DC) sputtering along with a capping layer of TiN and patterned with a commercial H_3PO_4-HNO_3 Al etchant at 50 °C. This second layer of TiN served as an etch stop in the passivation oxide patterning later in the process. Capacitive coupling from pixel to readout was achieved by contacting only the pixel implant in a small corner, while the largest part of the metal pad with the bump connection to the read-out was situated on a continuous layer of oxide without contact opening. For surface passivation, another thinner layer of Al_2O_3 was deposited (cf. Subsection 2.1). Surface passivation by SiN_x was avoided due to this material's positive charge [21], which would pose a risk to the envisioned field-effect passivation through the negative charge of Al_2O_3. Finally, a gold (Au) under-bump metallization, with an underlying adhesive layer of titanium tungsten (TiW), was deposited by alternating current (RF) sputtering. In this case, photoresist was applied prior to deposition, and the TiW-Au layer was patterned by a lift-off technique.

2.1. Atomic layer deposition of Al_2O_3

Al_2O_3 was deposited at 200 °C in a Beneq TFS-500 batch-type ALD reactor, using $Al(CH_3)_3$ as the metal precursor. A H_2O pulse as primary reactant was complemented by an additional ozone (O_3) pulse. Al_2O_3 films deposited by this combination of oxidants have been found to retain the excellent surface passivation and low-defect interface of films deposited by the TMA+H_2O process, while exhibiting more effective negative oxide charge [22, 23]. Furthermore, the addition of O_3 has been observed to prevent local delamination, also known as blistering, of Al_2O_3 films, which may occur upon low-temperature annealing of films deposited using only water as the oxidant [24, 25]. This phenomenon must be prevented especially in highly segmented devices, such as the pixel detectors described in this work, since it poses a severe risk for short-circuits between neighboring pixels, as well as for sparking between the sensor and read-out chip in high electric fields.

One ALD cycle consisted of a 200+200 ms TMA pulse, followed by a 7 s N_2 purge, and subsequent 200+200 ms H_2O and 3.5+3.5 s O_3 pulses, again with a 7 s N_2 purge.

The same ALD process was used twice in detector fabrication: first to deposit the field insulator dielectric, and a second time as surface passivation on top of the processed pixel structures. For field insulation deposition, the number of ALD cycles was 700, for surface passivation 300, resulting in film thicknesses of 84 and 33 nm, respectively, as determined by ellipsometry. Film thicknesses were also examined after completed processing by cross-sectional scanning electron microscope (SEM) imaging of a diode, which also shows the conformal and pinhole-free deposition of the Al_2O_3 thin films (see Figure 3).

Etching of both films was performed using a commercial Honeywell PWS 80-16-4 phosphoric acid etchant at 50 °C. Etch rates for metallic Al and Al_2O_3 in this solution are sufficiently different for the chemical to also be used later in the process for patterning of the Al metallization layer without significant damage to the Al_2O_3 field insulation. During the passivation opening step, however, the underlying metal contacts need to be protected from the etchant, in this work by a passive layer of TiN which is not related to the bias resistor layer. For the future, other high-κ oxides, such as hafnium oxide (HfO_2) are considered as a replacement to Al_2O_3 as surface passivation in order to provide chemical compatibility in passivation opening etching. After patterning, Al_2O_3 films were sintered for 30 min at 370 °C in order to improve their stability in the following processing, and to establish the negative oxide charge. In case of the annealing of the Al_2O_3 surface passivation, this simultaneously served as sintering step for the Al metallization.

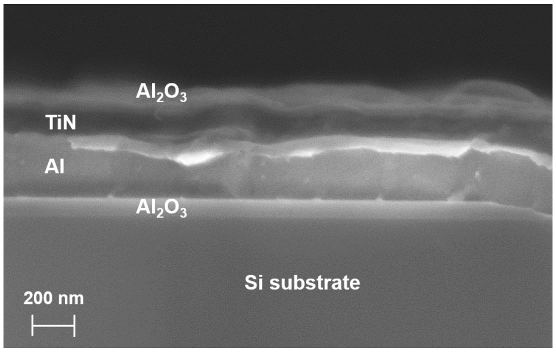


Figure 3: SEM cross-section of a pad detector, showing very uniform Al_2O_3 layers.

2.2. Fabrication of titanium nitride bias resistors

As presented earlier in a preliminary study [17], TiN biasing resistors were employed to provide individual bias resistors for all pixels on the sensor. As opposed to this previous study, the TiN films were now deposited by reactive RF sputtering for technical reasons.

Films were deposited by sputtering a Ti metal target in Ar (18 sccm) as plasma gas, with additional N_2 gas flow (72 sccm). The plasma power was 800 W. A sputtering time of 800 s resulted in a film with sheet resistance of 62 Ω/sq, and thickness of approximately 50 nm. Patterning of the films was performed by wet etching with 30% H_2O_2 at 50°C. Although comparatively slow at an etch rate of around 5 nm/min, this method allows batch processing of wafers (unlike our RIE equipment) and does not attack Al_2O_3.

The AC-coupled pixel detectors were realized in two groups with slightly different pixel biasing schemes, as shown in Figure 4. The actual TiN bias resistor part remained unchanged; however, the bias line connecting each pixel resistor to the common bias rail surrounding the detector was implemented either in the metal layer, or earlier as an additional n^+ implant grid. Simulations indicated that such an implant may improve the breakdown properties of the sensor between pixels, while also being less vulnerable to scratches on the surface that could interrupt the metallic bias line on the surface.

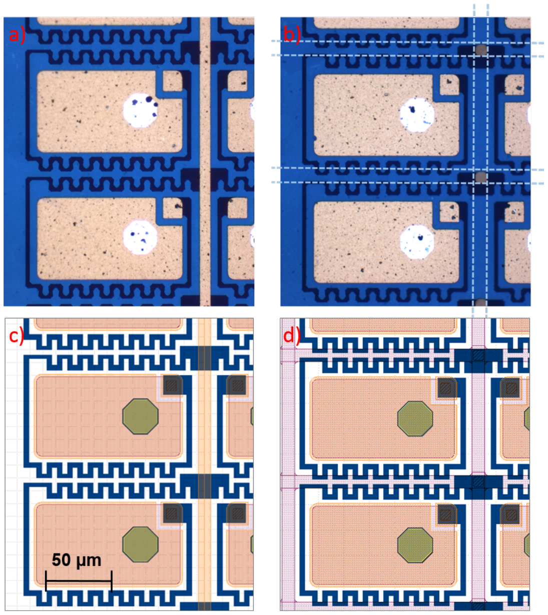


Figure 4: Two different biasing schemes used in our pixel detectors, with microscope images on the top and corresponding layout on the bottom: bias through metal line (left) or through an additional n^+ implant grid not visible in the picture, indicated by the dashed lines (right). The width of the bias resistor is nominally 4 μm, dimension of pixels n^+ implants is 60μm × 100μm (width / length) and the passivation opening for the solder bumps is 30 μm.

3. Characterization

The electrical properties of the various components in the AC-coupled pixel detectors were studied primarily using reference devices - diodes, MOS capacitors and resistor test structures - due to the more straightforward nature of the corresponding measurements.

Leakage current densities, depletion voltage, and silicon bulk capacitance after full depletion were determined by current-voltage (IV) and capacitance-voltage (CV) measurements on pad diodes. The effective charge, as well as an estimation of mobile charges, of Al_2O_3 was examined through CV measurements on MOS capacitors. The total resistance of a bias resistor for a single pixel was extracted from an IV measurement on a simple reference resistor structure between two metal pads. IV measurements on the AC-coupled pixel detectors were also performed, however, in a configuration with floating guard rings (which did not have passivation openings, as visible in Figure 7a) and the current read from the bias rail. This does not provide any separation of pixel leakage currents from possible high edge and surface currents, and is therefore interpreted as an overestimation of the leakage current in the detector during real operation, where the bias rail is grounded.

For IV measurements, a Keithley 2410-C SourceMeter unit was used to supply the bias voltage through the probe station chuck to the backplane of the device, and simultaneously to measure the total current. Pad currents were read by a Keithley 6487 PicoAmmeter connected through a probe needle to the device's metal pad. In diodes, the main guard ring was grounded through a second probe needle.

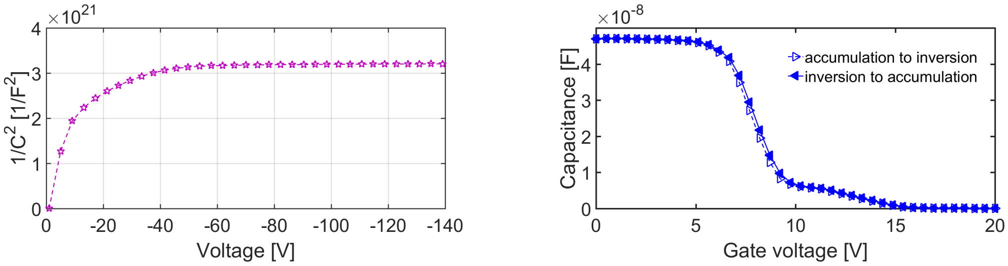
For CV, the device was connected by probe needle through a current-potential decoupling box to an Agilent E4980A Precision LCR meter, with the Keithley 2410-C still supplying the DC bias. Capacitances were recorded at an AC frequency of 1 kHz.

An AC-coupled pixel detector with implanted bias line was studied by ion beam induced current (IBIC) method. The IBIC measurements were performed at the Laboratory for Ion Beam Interactions of the Ruđer Bošković Institute with 2 MeV protons from a 1.0 MV HVE Tandetron. The beam frequency was set to around 1 kHz with beam current level at 20 pA. Due to the limited scanning range of the beam in a single measurement, only selected areas of approximately $1 \times 1\,\mathrm{mm}^2$ were studied. The beam centroid was moved over the selected area with scanning speed of about 1.3 ms per measurement point. The detectors were irradiated through the front plane which was connected to ground through a $50\,\Omega$ resistor. The bias voltage was applied to the backplane. The detectors were biased and read out through an Ortec 142 pre-amplifier, and the resulting signals were further amplified with Ortec 572 amplifier. After the amplification, the signal was passed through an analogue to digital converter (ADC) to a field-programmable gate array, and mapped with the SPECTOR system [26], [27]. More details of the microbeam readout chain and the IBIC mapping can be found in [28].

4. Results

An illustrative example of a diode C-V curve is shown in Figure 5a. It indicates full depletion (defined as the point where capacitance remains constant) at around -50 V. This corresponds to an effective doping concentration of 6.3×10^{15} cm^{-3} and a resistivity of 22 kΩcm, which is clearly higher than the original wafer specifications. Such a difference may be due to a deviation of substrate properties in the manufacturing process, for example a change in oxygen concentration across the silicon ingot. Alternatively, this could be an indication that thermal donors were introduced into the MCz substrate at some stage of the detector fabrication process, lowering the effective p-type doping concentration. In principle, a lower full depletion voltage is seen as an advantageous property regarding detector operation.

The MOS capacitor C-V curve shown in Figure 5b demonstrates a high positive flat-band voltage (V_{fb}). Curves were recorded both from accumulation of the gate towards inversion, i.e, in this case for p-type substrate, starting from negative gate voltages or zero, and vice-versa. The absence of significant hysteresis between the two indicates that the density of mobile charges at the oxide-silicon interface is negligible.



(a)

(b)

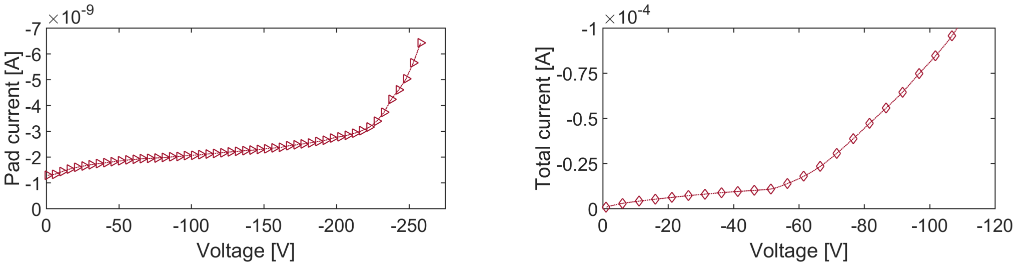
Figure 5: a) A typical diode reciprocal capacitance curve. b) C-V curve for a typical MOS capacitor.

Neglecting interface states and thus the effect of substrate doping, the oxide charge Q_{eff} can be estimated from V_{fb} according to Equation 1:

$$Q_{\mathrm{eff}} = -C_{ox}\Delta V_{fb} \tag{1}$$

Using a V_{fb} value of 8 V, this yields an effective oxide charge of -3.5 $\times 10^{12}$ qcm^{-2}. This value is in good agreement with the literature, as well as the contactless CV measurements on thin film reference samples.

The illustrative I-V curves of a diode and an AC-coupled pixel detector are presented in Figures 6a and 6b, respectively. The leakage current of the simple diode structure at full depletion is low, in the order of magnitude of 7 nA/cm2. The pixel detector current is much higher, as expected. It appears to increase proportionally to $\sqrt{V}$ until the detector is depleted, after which the current rises more sharply. This indicates either early breakdown, likely between pixels, or the formation of an Ohmic current path along the detector surface.



(a) (b)

Figure 6: a) Diode IV. b) Pixel detector IV.

The biasing resistors' resistances were calculated as the reciprocal slope of a resistor test structures' I-V curve (not displayed here). This method gave resistance values of around 15 kΩ for a resistor around a single pixel.

The IBIC map of an AC-coupled pixel detector with an implanted bias line grid is shown in Figure 7, along with a microscope image of the detector's corner section where the map was recorded. Bias rail, pixel and bias line implants are clearly visible as areas with higher current, thus implying that these areas are collecting charge. The collected charge over several rows and columns of pixels is uniform and the individual pixels are clearly separated from each other. The measurements also demonstrate that the additional bias line implant may result in reduced charge collection efficiency of the pixels, since some signal is collected at the bias line and transferred to the common bias rail, which would be grounded in final detector operation.

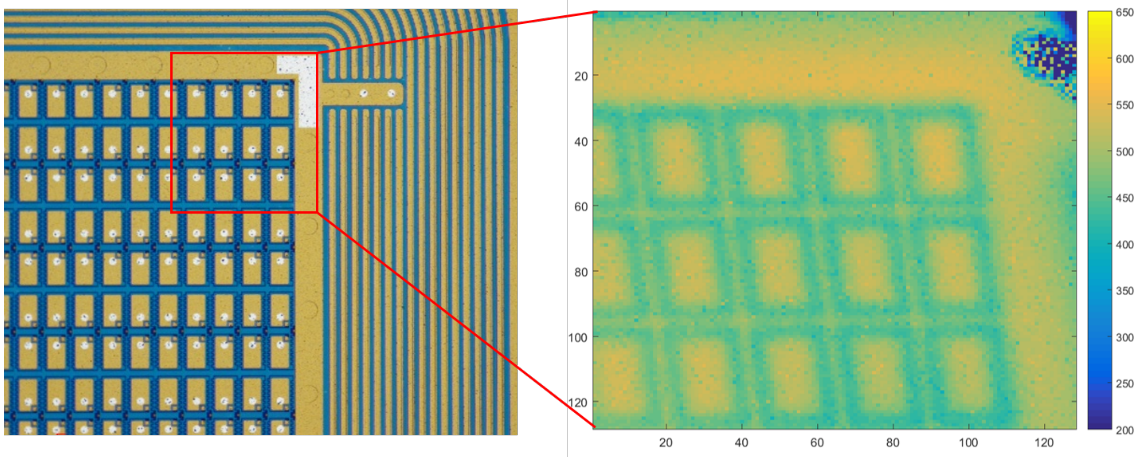


Figure 7: Microscope image of an AC-coupled pixel detector (left), with a section of it scanned by proton microprobe (right). Charge collection efficiency is in arbitrary units.

5. Conclusions

We demonstrated the integration of Al_2O_3 as field insulation dielectric and surface passivation layer into a pixel detector fabrication process. We were able to deposit blister-free, uniform Al_2O_3 layers with highly negative oxide charge. TiN bias resistors with suitable resistance were fabricated. The performed C-V and I-V measurements on pad detectors show low leakage currents and sufficiently high breakdown voltage of the devices, which is very promising for the operation of more complex, pixelated detectors. The obtained IBIC map indicate that our AC-coupled pixel detectors are functional and have uniform charge collection efficiency, despite high initial leakage currents.

Further studies on the characterization of MCz devices with Al_2O_3 as field insulator, and their behavior in gamma irradiation [29] are left for a subsequent publication. In addition, a production of AC-coupled pixel detector/CMS PSI46dig read-out chip assemblies and assessment of their performance by test-beam campaigns is ongoing.

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