

Scalable Cryoelectronics for Superconducting Qubit Control and Readout

Meraj Ahmad, Christos Giagkoulovits, Sergey Danilin, Martin Weides, and Hadi Heidari*

Quantum computing promises an exponentially higher computational power than classical computers; although all the building blocks have become available, certain constraints still prevent quantum advantage. The fundamental challenge in building a practical quantum computer is integrating thousands of highly coherent qubits with the control and readout electronics. The need for a high-coherence qubit drives the effort for quantum error correction algorithms to create fault-tolerant quantum systems. Error correction becomes tangible in a quantum processor only in large numbers of qubits. Thus, the other challenge is reducing the number of physical interconnects (coaxial lines) between the quantum–classical interface and bulky room-temperature electronics. To interface thousands of qubits, interconnects can be reduced by bringing the control and readout electronics near the quantum processor. Cryogenic complementary metal–oxide–semiconductor (CMOS) technology has been an ideal candidate for this purpose. Integrated control and readout at cryogenic temperatures require low power dissipation circuit designs and techniques such as frequency-division multiplexing (FDM) due to the finite cooling power of a dilution refrigerator. Herein, an overview of each building block in a superconducting quantum computer is provided, focusing on scalability. Furthermore, this article is concluded with an outlook discussing current challenges and future directions for the scalable superconducting control and readout.

1. Introduction

Quantum computers possess the efficacy of solving very hard computational tasks in a reasonable time compared to the tremendously huge time it would take for a classical computer.^[1–3] While in quantum computers, quantum bits (qubits) replace traditional logic, they also require classical electronics to control and


readout qubits, as shown in Figure 1a. Figure 1b–d represents the quantum computer's evolution from a conventional approach to scalable architecture. A qubit is the fundamental computational block in the quantum computer, enabling exponentially faster computation due to the properties superposition and entanglement. A qubit is a two-level system that can be in quantum state $|\psi\rangle$, which can be represented as a superposition of its two computational basis states $|0\rangle$ and $|1\rangle$. The two states occupy distinct levels, precisely analogous to classical digital logic zero and one. The state of a qubit has a distinct annotation as a point on the surface of a unit sphere called the Bloch sphere. As shown in Figure 1e, the north and south poles of the Bloch sphere represent the $|0\rangle$ and $|1\rangle$ states, respectively, whereas all other points on the surface of the Bloch sphere correspond to distinct superposition states $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$. An analogy can be drawn between the amplitude of the quantum superposition state and the classical analog of an averaged duty-cycle signal. The two voltage levels, VDD

and GND, when duty-cycled and averaged, provide all the levels between VDD and GND, $S_{\text{avg}} = \alpha\text{VDD} + \beta\text{GND}$, as shown in Figure 1f. Moreover, during the readout of quantum states, the output is either in states $|0\rangle$ or $|1\rangle$. Similarly, during the readout of the duty-cycle averaged signal in the classical analog, the output is either VDD or GND.

2. Superconducting Transmon Qubits

There are several candidates for a qubit architecture to build quantum computers, including trapped ion qubits, spin qubits, superconducting qubits, and topological qubits. Transmon qubits, and all superconducting qubits, are based on microwave circuits, a technology that has matured and established interrogation components, fast operation, and the possibility to reach high coupling strengths between circuit elements, making the architecture ideal for high qubit integration. A Josephson junction (JJ) is a critical component of the superconducting transmon qubit. The JJ is a superconducting tunnel junction that is analogous to a nonlinear inductor (L_J). A transmon qubit consists of JJ

M. Ahmad, C. Giagkoulovits, S. Danilin, M. Weides, H. Heidari
James Watt School of Engineering
University of Glasgow
Glasgow G12 8QQ, UK
E-mail: Hadi.Heidari@glasgow.ac.uk

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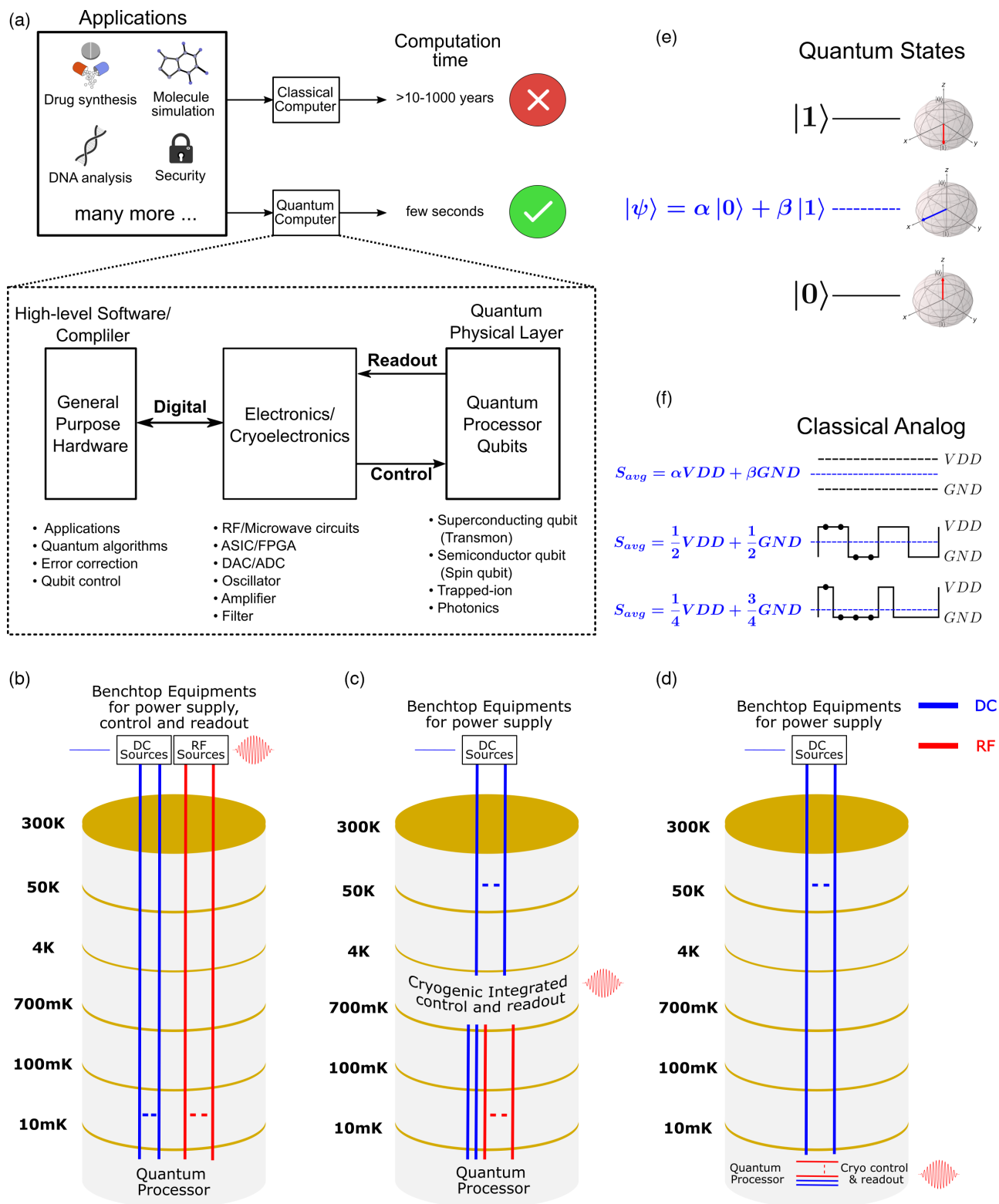


Figure 1. a) Overview of quantum computing advantages and system hardware block diagram. b) Conventional Quantum control and readout architecture. c) Scalable architecture with integrated control and readout. d) Future architecture for high qubit integration. e) Quantum instantaneous state $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ with basis states $|0\rangle$ and $|1\rangle$. f) Classical analog analogy to quantum superposition.

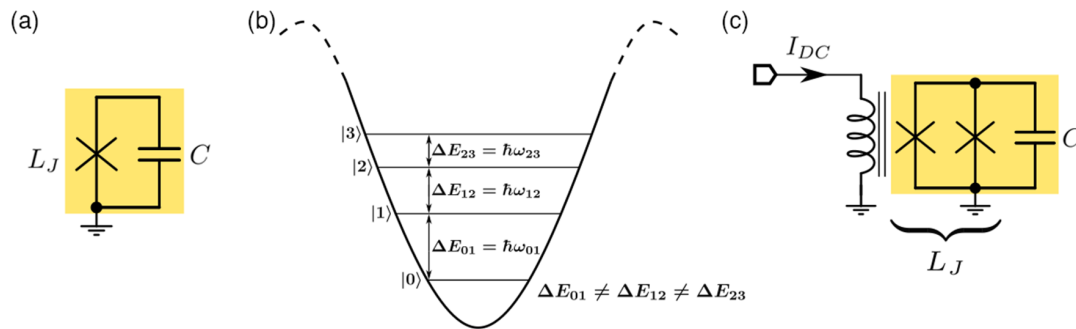


Figure 2. Superconducting qubit. a) Fixed frequency transmon qubit. b) Potential and energy diagram of a transmon qubit. c) Tunable frequency transmon qubit or dc-superconducting quantum interference device (dc-SQUID), adapted from Ref. [4,5].

in parallel with a capacitor C , assembled to create a nonlinear resonator, as shown in **Figure 2a**. The nonlinear nature of the JJ creates anharmonicity, which is an uneven spacing between the energy levels of the transmon ($\Delta E_{01} \neq \Delta E_{12} \neq \Delta E_{23}$), as shown in **Figure 2b**. Anharmonicity is a crucial characteristic that enables the operation of a transmon as a qubit when only its two lower energy levels are involved. A scalable quantum computer will require many qubits, with each qubit having its distinct transition frequency (ω_{01}). Consequently, a tunable frequency transmon qubit is needed, which can be implemented by changing the current I_{DC} , as shown in **Figure 2c**. Tunability is achieved using a flux tunable Josephson junction loop or superconducting quantum interference device (SQUID).^[4,5]

3. Quantum Control

Quantum computation requires performing independent rotations of the quantum state around the Bloch sphere axes, which are called X , Y , and Z gates. **Figure 3a** shows a single port XY control drive used to drive the qubit state rotations around an XY -plane. In order to independently drive the X and Y rotation on a single port of the qubit, an IQ mixer can be incorporated with the transmon qubit.^[4,6] The IQ mixer combines the two X and Y control drive orthogonally at the qubit transition frequency (ω_{01}), enabling a single port XY control, as shown in **Figure 3b,c**. In the homodyne IQ mixing scheme shown in **Figure 3c**, the local oscillator frequency is equal to the qubit transition frequency (ω_{01}). The homodyne IQ mixing scheme is a straightforward concept. However, its implementation is rather challenging as qubit scaling will require a different local oscillator for each qubit, operating at a different frequency. A heterodyne mixing scheme, on the other hand, is a more suitable solution for multiqubit control, where the local oscillator frequency (ω_{LO}) is fixed and the in-phase and quadrature components $I(t)$ and $Q(t)$ are generated using the digital-to-analog converter (DAC) with the low-frequency component $\omega_{01} - \omega_{LO}$, as shown in **Figure 3d**. The output of the mixer drives the qubit with complete in-phase and quadrature control, similar to the homodyne mixing scheme. The Z control drive, shown in **Figure 3a**, can be used to control the qubit transition frequency (ω_{01})^[7], qubit initialization,^[8] and two-qubit interactions.^[9]

A quantum algorithm is executed by driving the qubit with various waveforms stored in a database in a particular pattern.^[10] A problem that arises with stored qubit waveform patterns is that waveform data point digital storage space for each qubit control instruction will consume considerable memory space. Moreover, the qubit phase needs to be tracked for coherent control and non-uniform sequential operations.^[11] Furthermore, each qubit requires a distinct reference clock^[12] for the qubit transition frequency (ω_{01}). To address these issues, a solution that has been proposed is the use of a numerically controlled oscillator (NCO) and direct digital synthesis (DDS), enabling power and area efficient qubit control^[11,13,14] (**Figure 3e**). Over and above, the non-idealities (amplitude mismatch, phase error, and LO leakage) of the IQ mixer can significantly degrade the performance of the qubit control. These nonidealities can be mitigated using a digital IQ calibration scheme.^[11]

4. Quantum Readout

The probabilistic nature of quantum mechanics does not allow the qubit state to be evaluated in a single measurement. Multiple statistical measurements of the qubit state ($|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$) are needed instead to evaluate the state $|0\rangle$ with probability $|\alpha|^2$ and state $|1\rangle$ with probability $|\beta|^2$. The qubit state measurement must be performed accurately with an error rate of 1% or lower for practical quantum algorithms.^[15] A critical requirement of the precise readout setup is that the measurement setup or readout method may not interfere with the qubit state. A simple projective measurement approach could be to connect the qubit directly to the readout circuit through a capacitor C_k (**Figure 4a**). In this approach, the two states can be evaluated by monitoring the phase shift between the forward wave (a_1) and reflected wave (b_1). However, the readout circuit loads the qubit state, causing an error in the measurement. This error can be reduced by adding a linear resonator (frequency detuned from the qubit) that is coupled to the readout circuit through the capacitor C_k (**Figure 4b**). The addition of the readout resonator isolates the qubit and the readout circuit, enabling error reduction. The interaction between the qubit and the readout resonator in the dispersive regime shifts the readout resonator frequency depending on the qubit state. A bandpass filter (Purcell filter) around the readout resonator frequency (ω_r) can be incorporated to reduce the error further, as shown in **Figure 4c**. **Figure 4d** shows the scalable control and readout architecture for a

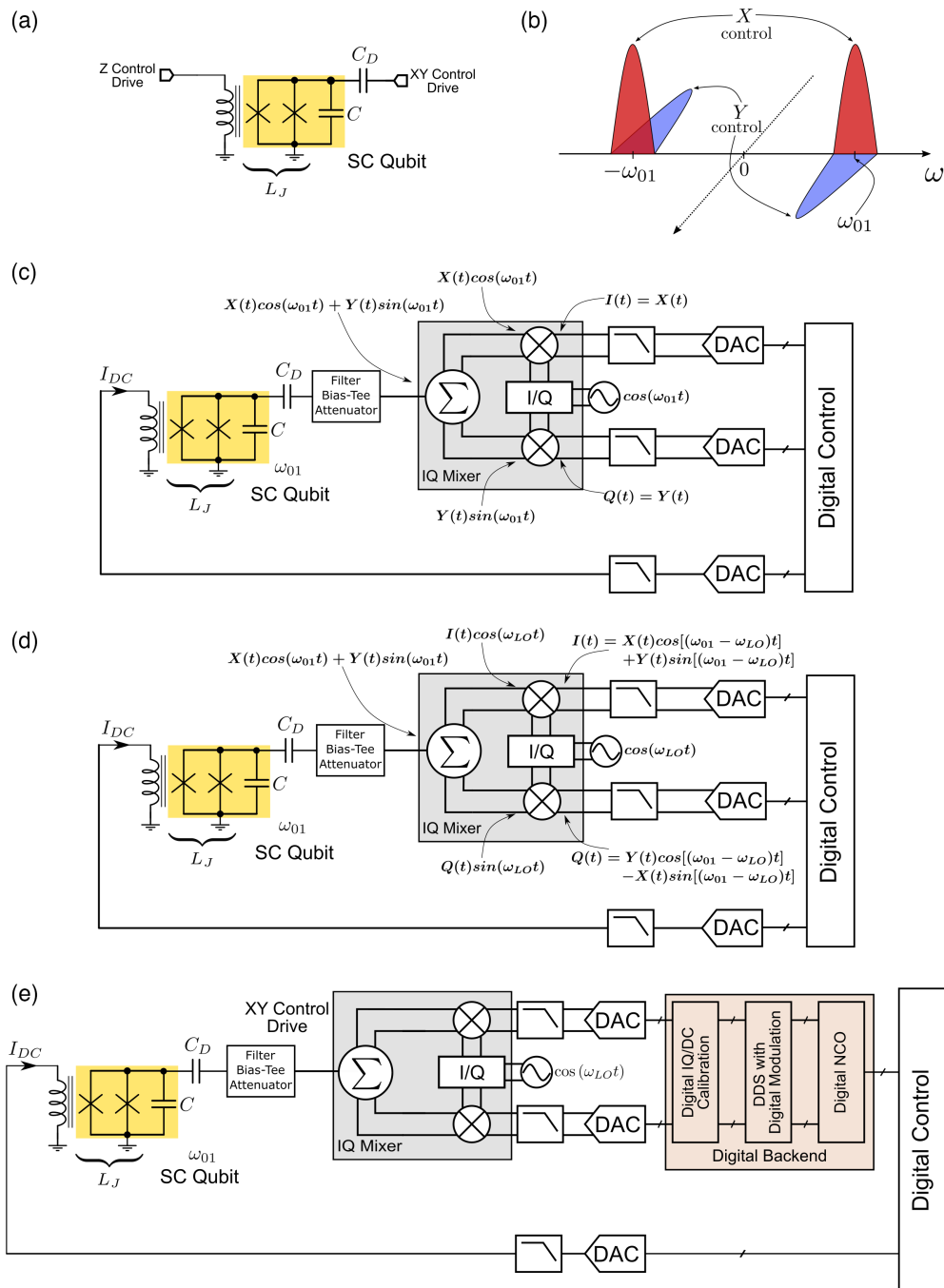


Figure 3. Quantum control setup. a) Control. b) Frequency response of orthogonal single sideband mixing. c) Homodyne mixing scheme. d) Heterodyne mixing scheme. e) Quantum control block with digital backend.

superconducting qubit; the same architecture can also be used in spin qubits.^[16] The control and readout electronics can be easily multiplexed between 10s or even 100s qubits.^[17]

5. Performance Metrics/Characterization

The energy relaxation time (T_1) for the qubit can be characterized by first resetting the qubit to the $|0\rangle$ state, and then exciting the

qubit to the $|1\rangle$ state using a X_π pulse, as shown in **Figure 5a**. The state of the qubit is measured after a delay time τ . A single measurement will project the quantum state into either state $|0\rangle$ or state $|1\rangle$. To estimate the probability, one must drive the qubit consistently, repeat the experiment multiple times, and take the ensemble average. The decoherence time (T_2) for the qubit can be characterized using Ramsey interferometry by first initializing the qubit to the $|0\rangle$ state, and then exciting the qubit to the

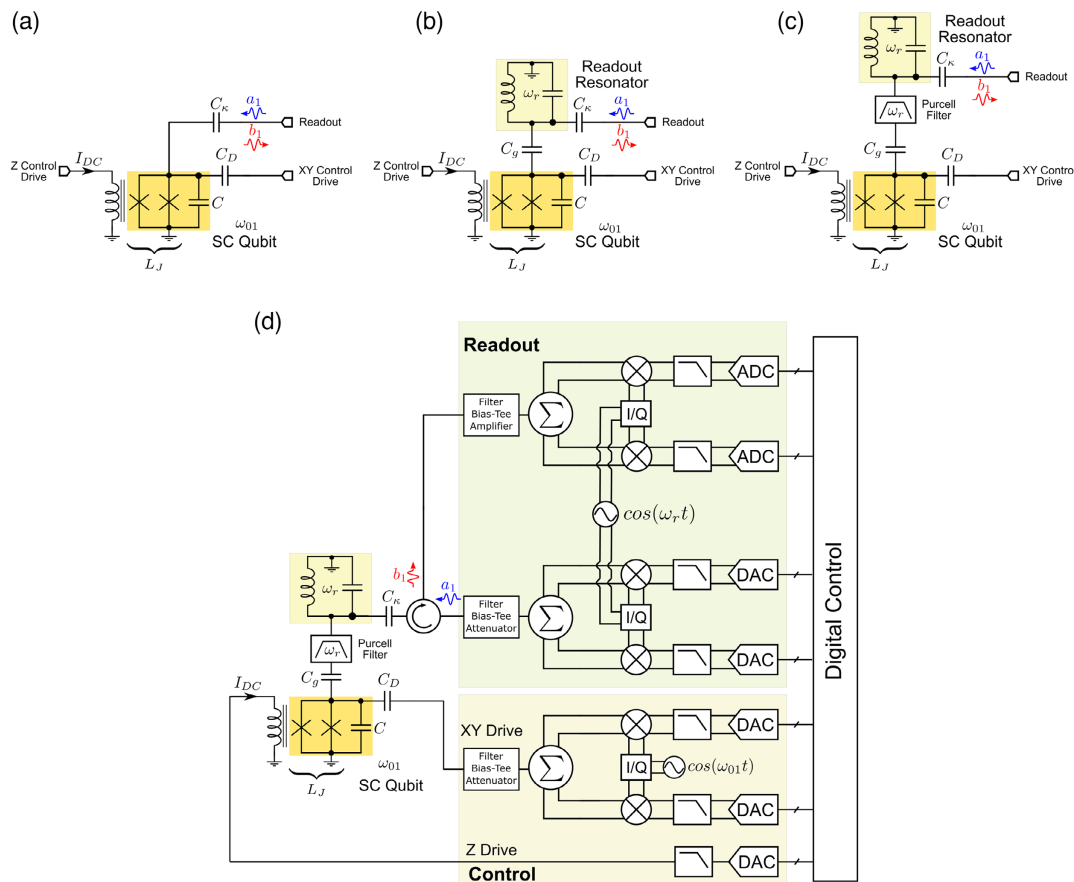


Figure 4. Reflective quantum readout setup. a) Directly coupled measurement readout. b) Dispersive measurement readout. c) Dispersive measurement readout with Purcell filter.^[15] d) Complete control and readout.

equator (XY plane) using a $X_{\pi/2}$ pulse, as shown in Figure 5b. After a delay time τ , a second $X_{\pi/2}$ pulse is applied, and the state of the qubit is measured. The decay function is almost exponential, with a characteristic time T_2 . The decoherence time (T_{2e}) for the qubit can be characterized using the Hahn echo experiment. The qubit is driven and measured in the same manner as the Ramsey interferometry experiment, except that a single X_{π} pulse is applied midway through the free-evolution time τ , as shown in Figure 5c. Same as T_2 , the decay function is almost exponential, with a characteristic time T_{2e} . The $|2\rangle$ state population for the qubit is characterized by first initializing the qubit to the $|0\rangle$ state, and then exciting the qubit with a sequence of N pulses, as shown in Figure 5d. After the final pulse, the qubit state is measured using a readout scheme that differentiates the $|0\rangle$, $|1\rangle$, and $|2\rangle$ states. The undesirable state $|2\rangle$ will appear due to ω_{12} transition frequency and represent the anharmonicity of the qubit. The Ramsey-style experiment characterizes the coherent qubit phase control over the two axes, as shown in Figure 5e. The qubit is first initialized to the state $|0\rangle$ and two $X_{\pi/2}$ pulses are sandwiched by a Z_{θ} gate of varying angles from 0° to 360° . After the qubit state measurement, the $|1\rangle$ probability is expected to be cosinusoidal. The qubit amplitude control can also be characterized using the Rabi experiment, as shown in Figure 5f. The qubit is first initialized to the state $|0\rangle$, then X_{θ} pulse is applied,

and finally, the quantum state is readout. By applying pulses with increasing duration, the qubit angle of rotation φ is increased, producing an oscillating pattern called Rabi oscillation.

6. Quantum Hardware Challenges and Future Perspectives

For the quantum system to be truly scalable and perform fault-tolerant quantum computations, the electronics must be designed with high-performance, low-noise, and high power efficiency. Moreover, the high-frequency interconnects from the room temperature (300 K) electronics to the quantum processor at cryogenic temperature (<1 K) should be minimized, also to minimize the need for filtering of infrared photons.^[18] Ideally, the electronics need to reside with the quantum processor at cryogenic temperatures to address the obstacles mentioned above; however, due to the dilution refrigerator's current cooling limitation, as a first step, cryogenic electronics can be placed close to the quantum processor with short high-frequency interconnects and using multiplexed circuit architecture. Efficient cryogenic circuits and systems can only be designed if reliable cryogenic CMOS (CryoCMOS) device models are available. Existing CMOS device models are only available in the industrial

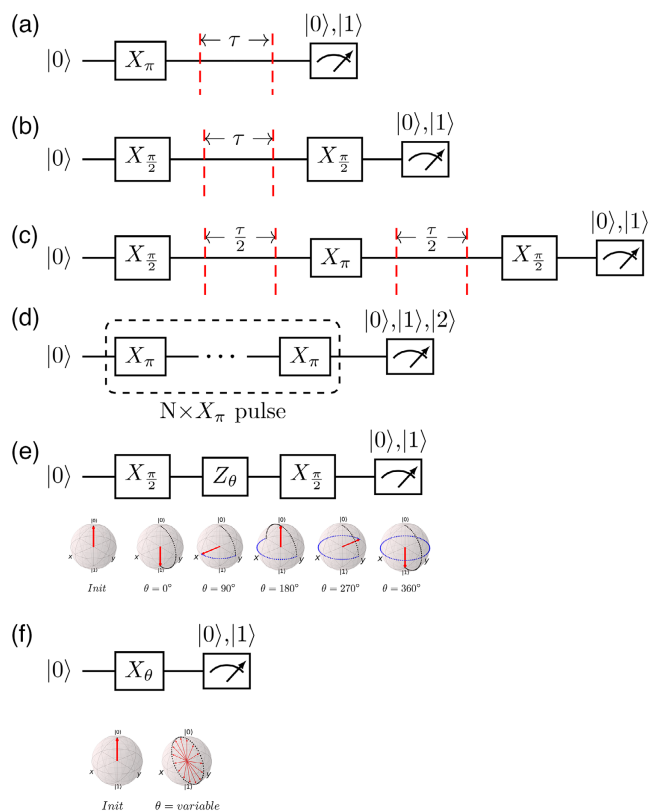


Figure 5. a) Longitudinal (energy) relaxation time (T_1) characterization setup.^[5,19] b) Transverse (energy and decoherence) relaxation time (T_2) characterization via Ramsey interferometry.^[5,19] c) Transverse (decoherence) relaxation time (T_2) characterization via a Hahn echo experiment.^[5,19] d) $|2\rangle$ state population characterization setup with variable pulse duration.^[4] e) Two axes coherent qubit control with a Ramsey-style experiment.^[6,19] f) qubit control with a Rabi experiment.^[6,19]

temperature range (-40 to $+125$ °C). Specialist cryogenic CMOS processes have not yet been developed. However, existing CMOS processes could be used as there have been indications that they function similar to the industrial temperature range with certain changes in specific parameters. Therefore, the development of cryogenic device models in existing CMOS processes is a field that is being investigated to develop reliable cryoCMOS circuits.

To select the most appropriate technology for the cryogenic circuit and system development, the characterization of MOS transistors close to qubit cryogenic temperatures needs to be studied extensively in several technologies like bulk CMOS, FinFET, and FD-SOI in terms of wideband and low-frequency noise, device mismatches, small-signal and large-signal device parameters, and DC and high-frequency response. Dynamic mismatch and offset cancellation techniques such as chopping, auto-zeroing, and dynamic element matching need to be incorporated to address the nonidealities in the circuits. Furthermore, foreground and background calibration techniques can be used to mitigate the timing skew and device mismatches to improve the performance of the essential building blocks such as ADC, DAC, mixer, voltage regulator, and temperature sensor. Another critical challenge is integrating derivative removal by

the adiabatic gate (DRAG) and ac stark-shift compensation block in the circuit architecture to further improve coherence time and anharmonicity of the scalable quantum system.

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Conflict of Interest

The authors declare no conflict of interest.

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Meraj Ahmad is a postdoctoral research associate at the James Watt School of Engineering of the University of Glasgow. He has received dual MTech and Ph.D. degrees in microelectronics and VLSI from the Indian Institute of Technology Bombay, Mumbai, India. His research interests include analog/mixed-signal circuits and system design for applications in quantum computing.



Christos Giagkoulovits is a postdoctoral research associate at the James Watt School of Engineering of the University of Glasgow where he also obtained his Ph.D. in electronic and nanoscale engineering in 2018. He holds a B.Sc. degree in physics and an M.Sc. degree in electronics and communications (radioelectronics) from the University of Patras, Patras, Greece in 2011 and 2013, respectively. He has developed a number of CMOS-based portable sensing platforms and cofounded a microelectronics spin-off company. His research interests include low-temperature mixed-signal CMOS VLSI circuit and system design of cryogenic quantum computing interfaces for qubit scale-up.



Sergey Danilin is a postdoctoral research associate at the James Watt School of Engineering of the University of Glasgow since January 2019. He worked as a postdoctoral researcher at the Physics Department of the Karlsruhe Institute of Technology, obtained his Ph.D. degree in superconducting quantum circuits in May 2018 from the Applied Physics Department of the Aalto University, and worked as a laboratory assistant at the low-temperature physics laboratory of the P.L. Kapitza Institute for Physical Problems in Moscow. His research interests are in the improvement of operation and characteristics of superconducting quantum circuits for applications in quantum computing and quantum sensing.



Martin Weides, FlnstP is professor and associate director at the Centre for Quantum Technology, University of Glasgow. His Quantum Circuit Group conducts groundbreaking research at the interface of material science, electrical engineering, and circuit quantum electrodynamics, for scaled coherent quantum electronics with superconductors. He is founding member of the Quantum Computing Application Cluster, a co-I in the EPSRC Hub in Quantum Computing and Simulation, and leads jointly with Heidari the EPSRC network “Empowering Practical Interfacing of Quantum Computing (EPIQC).”



Hadi Heidari is a professor of nanoelectronics at the James Watt School of Engineering at the University of Glasgow, UK. His Microelectronics Lab (meLAB) conducts pioneering research on micro/nanoelectronics design for medical and quantum technologies. He is a member-at-large of IEEE Sensors Council (2020–2021), senior member of IEEE, and fellow of Higher Education Academy (FHEA). He is the general chair of the 29th IEEE ICECS 2022 and serves on the organizing committee of several conferences. He holds a Royal Society of Edinburgh Saltire Fellowship.