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I am submitting herewith a thesis written by Sashi Kiran Challa entitled "The Effects of Carbon Nanotubes on CPU Cooling". I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Computer Science.

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THE EFFECTS OF CARBON NANOTUBES ON CPU COOLING

A Thesis Presented for the

Masters of Science Degree

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Sashi Kiran Challa

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Dedication

I would like to dedicate this Master's thesis and my Master's degree to my parents and my brother, for supporting me, believing in me in and all my endeavourers, being excellent role models, and for inspiring me and encouraging me to always reach higher and achieve my goals.

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Lastly, I would like to thank my parents and brother for their suggestions and encouragement which made this work possible.

Abstract

Computers today have evolved from being big bulky machines that took up rooms of space into small simple machines for net browsing and into small but complicated multi-core servers and supercomputing architectures. This has been possible due to the evolution of the processors. Today processors have reached 45nm specifications with millions of transistors. Transistors produce heat when they run. Today more than ever we have a growing need for managing this heat efficiently. It is indicated that increasing power density can cause a difficulty in managing temperatures on a chip. It is also mentioned that we need to move to a more temperature aware architecture.

In this research we try and address the issue of handling the heat produced by processors in an efficient manner. We have tried to see if the use of carbon nanotubes will prove useful in dissipating the heat produced by the processor in a more efficient way. In the process we have also tried to come up with a repeatable experimental setup as there is not work that we have been able to find describing this exact procedure. The use of carbon nanotubes seemed natural as they have a very high thermal conductivity value. Also one of the uncertain aspects of the experiment is the use of carbon nanotubes as they are still under study and their properties have not been completely understood and there has been some inconsistency in the theoretical values of their properties and the experimental results obtained so far. The results that we got were not exactly what we expected but were close, and were in the right direction indicating that more work in future would show better and consistent results.

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Chapter 1

Introduction

Computers have come a long way from the first mechanical calculating machine made by Charles Babbage, to the ENIAC, to the 4004 microprocessor, to the 8086 processor. Processors today have evolved into faster, smaller, high performance multi-core architectures. The processors from the 4004 to the ones in use today have one thing in common - they are made up of transistors. What differentiates the processors over time is the increase in the number of transistors present in the processors. The Intel 4004 microprocessor that was released in 1971 had about 2000 transistors. The Intel Quad core extreme processor has approximately 820 million transistors, with the space between the transistors reduced to about 45 nanometers. This progress is in line with Moore's law and leads to faster and more capable computers.

However everything good comes with its own side effects, one of them being heat. A couple of questions that one would ask are

- How is this heat produced, and
- Why is heat a problem?

Firstly, heat from a processor is produced by the transistors when they run^[12]. This heat is a problem because the performance of the transistors is inversely proportional to heat. So simply put, more heat means lower performance from the transistors, reducing the performance of the processor.

There are varieties of methods people use to cool the processors, but the basic method is to use a heat sink. These heat sinks come bundled generally with the CPU^[12]. There is also a layer of thermal paste between the heat sink and the processor which helps increase the transfer of heat from the processor to the heat sink. Also, on top of the heat sink is a fan that draws the heat out and blows it out or blows in cool air on to the heat sink.

In this research we have tried to modify the thermal paste to help achieve faster heat transfer from the processor to the heat sink. To modify the thermal paste Single Walled Carbon nanotubes (SWNT) were added to the mixture. Carbon nanotubes were chosen for their high thermal conductivity which ranges anywhere from 1750 W/mK⁻¹ to 5800 W/mK⁻¹ [^{14]}. The nanotubes were mixed with an off - the - shelf silicon based thermal paste.

The experiment was done in two stages. Stage one was done at the University of Alabama at Birmingham, Material Science and Engineering Department, under Dr. Uday Vaidya. Here, the nanotube based paste was prepared the basic method of the experimental setup was outlined, and a set of initial readings was made (section 3.1).

The second stage of the experiments was at the Indian Institute of Science, Bangalore, India, in the Department of Aerospace Engineering under Prof. C. R. L. Murthy. A few modifications were made in the experimental setup in this stage (section 3.2), and a few more readings were taken.

The focus of this research was to try to see if the use of Single Walled Nanotubes (SWNTs) in combination with standard thermal paste between the processor and the heat sink would help to achieve more efficient thermal transfer from the processor to the heat sink and would result in better cooling of the processor.

The following sections provide an in-depth look at:

- Why heat is a problem
- An overview of carbon nanotubes, and why we used carbon nanotubes
- What are the current solutions
- A brief look at today's heat sinks

1.1 Introduction to processor heat

On the one hand, it is exciting to see the rate at which the high performance processors containing millions of transistors are doubling, following Moore's law. But this also leads to a worrying situation. With the increase in the clock rate and transistor count of the processor it is becoming exceedingly important to be able to handle the power dissipation more efficiently^[5].

Designers and users of computer systems face a common problem today, keeping the processor below a safe operating temperature. Ideally, processors reach unsafe operating temperatures only under unrealistic working conditions. But this is not completely true; these cases do rarely happen ^[12]. The heating up of processors today depends not only on the working conditions but also on other things such as the specifications, the build of the CPU and the ambient temperature. Also, maintaining the processor under a given temperature directly relates to the power consumption rating of the processor, as high power devices produce more heat ^[1, 12]. Looking at the current trends in the levels of VLSI integration and high clock speeds being achieved these days, controlling the heat dissipation from processors is becoming even more critical ^[6]. Many analysts also suggest that increasing power density

results in difficulty in managing on chip temperatures, and just as in the past, we have achieved power aware computing, we now need to start approaching "temperature aware computing"^[5].

Also, this rapid increase in transistor density was mainly to achieve high levels of instruction level parallelism which reduces memory access times, hence improving overall efficiency. Unfortunately these benefits are slowly being overshadowed by the increase in the power dissipation. Today, as we move toward the one billion transistor mark the problem of increased power dissipation will only begin to magnify. As the number of transistors goes up and the promise of faster processors is met, there will always be a section of the users who will push the processor beyond its prescribed limits. Overclockers and gamers come under this section of users who will use the chip faster than it was rated. To achieve this they also increase the supply voltage and this in combination with the higher frequency of operation leads to increased power dissipation and hence increase in the processor's temperature ^[5]. This is not just limited to overclockers and gamers, even regular users who run processor intensive applications or applications that might need higher specification machines, without adequate hardware support would lead to increased load on the processor, causing it to heat up more than normal. An example is running a program that would work better with a graphics processor and high amounts of ram, without either. Also sometimes due to restrictions on space in the tower, the size of the fans on the heat sinks are smaller. To compensate for this the heat from the processor needs to be sent to the heat sink as fast as possible so there is no build up of heat.

One of the aspects of dealing with this situation is to design an efficient cooling method for the processor. It is estimated that after exceeding 35-40W, additional power dissipation increases the total cost per CPU chip by more than \$1/W to \$3/W^[1, 12]. In order to have an efficient and economically viable solution we must have the ability to handle the maximum heat generated by the processor, even though this might not be a daily occurrence. This will ensure the user that the overhead cost of the CPU will not go up and they can keep the increased power dissipation under check.

Micro scale electronics can generate heat fluxes thousands of watts per square centimeter in very small areas on the order of micrometers in size ^[6]. Typical IC chips have millions of transistors embedded in them. These performing various tasks either in combination or independent of each other, and this can lead to creation hotspots that can be of the order of a couple of hundred micrometers in diameter and can be 10 °C to 40 °C hotter than rest of the chip ^[6]. We need an efficient method to handle this generated heat.

The current temperature management schemes also involve thermal packages that contain large heat sinks, some of which include liquid cooling methods ^[12]. But these heat sinks are large, bulky, and take up a lot of room in the CPU cabinet, which leads to an increase in the size of the cabinet. One of the goals of the current research is to see if the heat that is generated by the processor can be more efficiently transferred to the heat sink, which might lead to faster cooling of the CPU.

1.2 Carbon Nanotubes: A brief overview

Carbon nanotubes (CNTs) are allotropes of carbon with a nanostructure that can have a length-to-diameter ratio greater than 1,000,000. They are cylindrical carbon molecules and have novel properties that make them potentially useful in many applications in nanotechnology, electronics, optics and other fields. They exhibit extraordinary strength and unique electrical properties, and are efficient conductors of heat. The name is derived from their size, since the diameter of a nanotube is of the order of a few nanometers, approximately 1/50,000th of the width of a human hair, while currently they can be up to several millimeters in length. Nanotubes are categorized as single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs).

The decision to use carbon nanotubes (CNT's) as a medium to help improve the thermal conduction between the processor and the heat sink was based on research that was being conducted on the CNT's that showed them to possess high thermal conductivity, even outperforming materials like diamond^[7, 8]. Also, in the past few years people have begun exploiting this property of high thermal conductance to efficiently remove heat from integrated circuits ^[6]. One of the interesting aspects of research involving CNT's is that the thermal conductivity of individual single walled CNT's has still not been well established. The existing simulation results indicate the range of the thermal conductivity of single walled CNT's from several hundred to around 6600 W/mK, compared to theoretical predictions that range from several dozens to 9500 W/mK ^{5]}. A lot of research is finding

uses for this high thermal conductivity that the nanotubes possess, and to use them in many different cooling solutions ^[6].

Most single-walled nanotubes (SWNT) have a diameter of close to 1 nanometer, with a tube length that can be many thousands of times longer. Single walled nanotubes have been used to increase the thermal conductivity of different materials. In one case the thermal properties of industrial epoxy increased by 70% at 40K (-233°C) and increased to 125% at room temperature with the addition of 1 wt% (weight percent) nanotubes. Such results were what prompted the use of carbon nanotubes in this experiment.

Section 2 of the thesis reviews related work that has been carried out handling heat problems of CPUs and some work that has been done on carbon nanotubes. Section 3 covers the experimental setup, the issues that we faced in designing the setup and when we were performing the experiments. Section 4 discusses the results and analysis of the results that we obtained. Section 5 summarizes the work we did and some future work that can be done.

Chapter 2

Literature review

A lot of work has been done on the study of nanotube thermal conduction [4, 5, 6, 9, 11, and 12]. The work done covers a wide spectrum of analysis and behavioral studies done on nanotubes.

Nanotubes have been analyzed under various factors like temperature, pressure, and heat transport phenomena ^[6]. Efforts have been made to get a more accurate figure of thermal conductivity of nanotubes clarifying the several – order – of – magnitude discrepancy (these range from several 100 to 6600W/mK⁻¹ obtained using molecular dynamics simulation, to values ranging from several dozens to 9500W/mK⁻¹ obtained from theoretical predictions) ^[14]. A study of carbon nanotube based nano-composites that showed a 250% conductivity increase with the addition of 9% by volume nanotubes with random orientation ^[13].

A study of the thermal conductivity of carbon nanotubes was made using molecular dynamics simulation to predict the thermal conductivity of carbon nanotubes, in use in the cooling of electronic devices to prevent structural damage of the electronic components. The study showed a potential conductivity value of 6600W/mK⁻¹. Another study was made on the interaction between heat and electricity (thermoelectric interaction) and how nanotubes can be used to modify the interactions to aid in better cooling of integrated circuits and the

removal of high power hot spots in IC chips. More work has been done and is currently being done [7, 8, 13, 14] which is not covered here.

As mentioned earlier carbon nanotubes play a significant role in this research. In particular, the thermal properties of the nanotubes are a key consideration as we are trying to improve the thermal properties of the silicon paste. Some similar work has been done where studies have been carried out on epoxy pastes that have been modified by adding carbon nanotubes. The work carried out by M.J. Biercuka, M.C. Llaguno, et al. in their paper titled "Carbon nanotube composites for thermal management"[15] studies the change in the thermal conductivity of industrial epoxy paste with the addition of 1 wt% nanotubes. The paper gives a study of the changes in the electrical conductivity and talks about the mechanical properties of the nanotubes, as well. But as this research primarily focuses on the improvement in thermal conductivity, we will concentrate on that aspect of the paper.

In the paper, the authors add 1wt% of nanotubes to an industrial epoxy. After this addition the authors note at room temperature a 125% increase in conductivity of the epoxy. In the process of adding the nanotubes and preparing the paste, the authors mention that care was taken to make sure that the nanotubes were dispersed evenly through the epoxy, and also when cutting the sample into a 1mm x 1mm x 2mm piece they verified that the different pieces that they cut gave matching results. For the actual experiment, the authors mounted a sample between two constantan rods of known thermal conductivity and heat was passed through this setup. Temperatures were measured across each rod and the sample using different thermocouples, and this gave the relative thermal conductivity of the sample.

With this experimental setup at room temperature they saw a 125% increase in thermal conductivity. They concluded from their observations that it was simple to note that a small percentage of nanotubes added to an epoxy material dramatically enhanced the thermal conductivity of the sample. But even though this looks promising from a point of view of this research, there is a mention that the results were not in agreement with the enhancement predicted by the law of mixtures.

There are also studies that have been done on the impact of nanoscale thermal transfer on IC's. Ali Shakouri in [6] has reviewed the impact of the recent findings in nanoscale thermal properties and their effects on cooling chips. He gives an elaborate insight into what makes nanotubes such excellent conductors of heat and how they conduct heat. The paper also mentions the various kinds of micro-refrigerators made from different materials like SiGe. He also talks about some modeling work that has been done to show the temperature distribution in a micro-refrigerator. The work done by Ali Shakouri is a review and analysis of a lot of others works. He talks about the work done by others and presents suggestions and comments about it.

One of the most important things that we can take away from his body of work in relation to this thesis is that he has stated that there is quiet a significant difference in the theoretical and experimental results of the thermal conductivity of nanotubes. The results from the experiments for the thermal conductivity of nanotubes yielded significantly lower thermal conductivity values than what was theoretically expected. "On the experimental side, the first attempts to measure thermal conductivity of a collection of CNTs gave values much lower than predicted. This is due to weak coupling between CNTs in the array that can affect the thermal transport." ^[6].

Computer architecture has been in the process of continuous change for a long time. The processor technology has also been evolving for almost the same period of time. The processor architecture has evolved from having a few thousand transistors to millions, and the size of the processor has decreased drastically, as well. The architecture today includes multiple cores and multilevel caches, which means the design of the processor is getting complicated as it evolves. Today we have processors that are designed for specific applications, as well as general purpose processors; we have small processors (Intel atom), and bigger multicore processors.

Kevin Skadrony, Mircea Stanz, et al. [5] indicate that increasing power density in processors causes difficulty in managing on chip temperatures, and this is an important issue that needs immediate addressing. It is one of the major obstacles today. They state that we need to move towards a more "temperature aware" architecture and also "Yet the architecture community is currently completely lacking a way to model temperature at any level of granularity other than low-level circuits!"

In their work they highlight their work under progress called "hotspot" which is a thermal modeling framework for processor architects. This framework uses natural partitioning by grouping together functional blocks on the chip into the circuit model. The remaining RC elements of the processor are grouped as packaging components. This tool also differs from the other tools in that the current processor architectures do not model the floor plan information of the processors. This information is becoming more and more essential for modeling power

performance and heat at an architectural level. One of the interesting observations brought forth in the paper is that published floor plans of processors generally reflect pipeline order, in a sense that adjacent units on the processor (in a pipeline stage) are also adjacent in the floor plan. This fact has been used to design their framework.

The tool works by taking given a floorplan with the areas of thermal resistance and capacitance values for the package. It derives a circuit to model dynamic heat flow in the chip, and compute the values for the remaining thermal Rs and Cs. For every time step, the thermal model receives the power dissipated in each block, and determines the average temperatures of each of those blocks at the end of that time step. Another available tool called "hotblocks" is available that computes the thermal resistance and a capacitance from each block to all its neighbors.

The authors also mention that there is no actual way of measuring localized temperatures from a real chip, so they used a heat flow modeling tool called "floworks" to generate some reference data. In conclusion, the paper describes an approach to modeling thermal behavior in an architecture-level power/performance simulator. The results that they have proposed with the generated circuit models come within 2% of the reference results found with Floworks.

Work done by M. J. Biercuka, M. C. Llaguno, et al. In [1] is similar to what we have tried to do. We have tried to modify the existing thermal paste present in the CPU using nanotubes to see if we can achieve faster cooling of the processor. Our goal was to see if this modification would help cool the CPU faster. The work done by M.J. Biercuka, M.C. Llaguno, et al. [1] and Ali Shakouri [8] both state that the nanotubes did not yield the expected (theoretical) thermal conductivity values, but that they came out with conductivity values that were considerably lower than expected.

Although there has not been a lot of work done on the same topic, there is some related work that has been done and which is currently being done. Carbon nanotubes are still a new research area and their properties have not been completely studied, and, as mentioned in some of the work of [8] the results obtained in the experiments and the theoretical values show a significant difference. The fact that carbon nanotubes do have physical properties that exceed any of the other materials that are being used for similar purposes is reason enough to continue to experiment using them.

Chapter 3

Experimental setup

The main idea of the experiment is to try and modify the thermal paste used in between the processor surface and the heat sink, so that it would provide better heat flow from the processor to the heat sink. This would help in better cooling of the CPU and in the longer run maybe lead to complete elimination of heat sinks. A diagrammatic representation of what we are trying to do is given below in figures 3(a) and (b).



Figure 3 (a) - Normal CPU – silicon paste- heat sink assembly



Figure 3 (b) – CPU - heat sink assembly but now with nanotubes

The hardest part of the experiment was designing an experimental setup giving valid test results. Usually ideas for experimental setups and procedures come from reading related published work. However, in this case, the amount of published work was not specific to what was being tried, which made it that much harder to come up with an experimental setup or method. We considered the following issues in order to have a proper experimental method.

- How the nanotubes need to be prepared
- What percentage of nanotubes to use
- The best way of mixing the nanotubes and the silicon paste used.

Some of these points needed to be looked into, as nanotubes were expensive and availability of facilities and resources were a prime concern. The next points under consideration were

- How to apply the paste as the evenness of the paste was important to the study.
- How the measurements would be made
- Validity of the experimental method (if the method used provides consistent results every time)
- Proof of concept
- Usability of concept

The aim of the experiment was to meet all of the above.

The experiment was performed in two stages. The first stage involved the preparation of the nanotubes, setting up a methodology of conducting the experiment, and identifying a few key points to see whether the experimental setup would work. The second stage involved taking more readings and trying to get comprehensive sets of data to analyze the proposed idea that inclusion of nanotubes in the thermal paste used would help in better cooling. The first stage of the experiment was performed at the University of Alabama, Birmingham, at the Department of Material Science and Engineering, under the supervision of Dr. Uday Vaidya, at UAB. Most of the experimental procedure and initial testing of the chosen method was done in his lab. The nanotube paste was also prepared under the supervision of Dr. Derrick Dean, also from the Material Science and Engineering department at UAB. The second stage of the experiment was performed at the Indian Institute of Science, Bangalore, India in the Composite Material Lab at the Department of Aerospace Engineering, under the supervision of Prof C.R.L. Murthy. Here, multiple readings were made at various points on the processor and heat sink. Many unexpected problems were encountered and tackled in order to get readings, including very basic issues like improper grounding, which led to more complicated problems described in section 3.1 and 3.2.2.

The details of both the stages are discussed in the following sections.

3.1. Work done at University of Alabama, Birmingham

3.1.1 Preparation of nanotubes.

The very first step of the experiment was to prepare the nanotube paste that was to be used for the experiment and deciding the amount of nanotubes to be added to silicon paste. This was important, as adding too much of nanotubes would make the paste an inefficient thermal conductor, while too little would not cause any substantial change in the conductivity of the silicon paste.

The preparation was done at the University of Alabama, Birmingham. The nanotubes were provided by Dr. Derrick Dean, and the mixture was prepared in his lab at UAB in the department of Material Science and Engineering, under his supervision.

For the preparation of the paste, Single Walled Carbon Nanotubes were used, and the silicon paste was bought form Radio Shack[®]. The silicon paste contains a mixture of the following four materials:

- Polydimethylsiloxane (PDMS) ((H₃C)₃SiO[Si(CH₃)₂O]_nSi(CH₃)₃): It is viscoelastic, that is at high temperatures acts like a viscous liquid, and at low temperatures acts like an elastic solid.
- Zinc Oxide (ZnO): Zinc oxide has good thermal stability. Zinc oxide decomposes into zinc vapor and oxygen only at around 1975 °C, reflecting its considerable stability
- Polytetrafluoroethylene (PTFE): commonly known as Teflon, PTFE is a white solid at room temperature. Its melting point is 327 °C (620.6 °F), but its properties degrade above 260 °C (500 °F according to DuPont). Adhesion to PTFE surfaces is inhibited. Due to this property of PTFE is used as a non-stick coating. It is very non-reactive.
- Fumed silica: Fumed silica is made from quartz sand vaporized in a 3000°C electric arc. Fumed silica serves as a universal thickening agent and is used as an anticaking agent in powdered foods. Like silica gel, it serves as a desiccant. It is used in cosmetics for its light-diffusing properties and is used as a light abrasive in products like toothpaste.

For the preparation of the paste, the amount of nanotubes to be used was decided at 0.05 wt%. For 9 grams of silicon paste about 0.454 grams of nanotubes were added in powder form. There was no specific reason to go with this percentage of nanotubes; the choice was made arbitrarily. The mixing was done manually using a stirrer. The final product was a thick black paste as shown in Figure 3.1 below, with the viscosity approximately a match to the original silicon paste. This is important because if the end paste becomes less viscous or thicker, then it will be harder to apply.



Figure 3.1 - The final nanotube paste (silicon paste +nanotubes)

The final mix was stored in an airtight glass vial to avoid any effects due to change in ambiance. In addition to the decision of the percentage of nanotubes to be used was the issue of how the two materials need to be mixed. The mixing of the two materials was an important aspect as we had to make sure the properties of both the materials were not lost. Also, it is known that nanotubes are cylindrical structures and they let heat flow through them for conduction ^{[8] [7] [9]}. So one of the key considerations was to see if we had to keep the nanotubes aligned in a certain way or leave them random. Since aligning nanotubes is still an open research topic, we made no attempt to align the nanotubes.

3.1.2 System used and Application of the Nanotube paste

The system used for the experiment was a Dell Optiplex Gx620 system, with, a Pentium 4 processor and 512 MB of ram.

The reason for choosing this machine was the availability of the system. This was the best possible system that was available and specifications were reasonably up to date (considering the fact that P4 processors are still not outdated). This seemed the best choice among the other available older P3 machines and old MAC G3 machines. The system was in very good running condition.

The inside of the CPU looked as shown in Figure 3.2 (a) and 3.2 (b), the fan assembly on the heat sink is also highlighted.



Figure 3.2 (a) – The inside of the Dell Optiplex GX 620



Figure 3.2 (b) – The fan assembly on the heat sink

The interesting thing to note here is the size of the heat sink, and its enclosure as highlighted. Because of the bulky size of the whole unit (heat sink + fan + enclosure) one of the long term goals is to eliminate such bulky installation on the CPU totally while providing better cooling. If it were not for the bulky heat sink unit the CPU could have been much thinner taking up much less space. This will make the CPU cabinets smaller.

Under the enclosure the heat sink was made out of aluminum and had a plastic fan attached over it to draw the heat out. The heat sink was clamped on top of the processor as indicated by the arrows in Figure 3.3 below.



Figure 3.3 – Clamping system of the heat sink

This clamping system was made out of plastic and though very basic did an excellent job of holding down the heat sink. The effectiveness of the clamping system was tested by holding the entire mother board upside down and shaking it, to verify if the clamping would let the heat sink go (crude but effective). The clamping system was tough enough to hold the heat sink in place.

Also when the heat sink was taken out to apply the nanotube paste, the older original thermal paste was still there. It was pink in color and was not in the form of a paste. It was elastic and stretched quite a bit (like a rubber string). This indicated that, it was still in useable condition. Most of the pastes are in solid state at room temperature, but, when the processor starts to get hot, the paste became a semisolid. The old paste was completely cleaned before apply the newly prepared paste.

For the application of the paste (silicon + nanotubes) methods like spraying were considered. Finally, the paste was applied using a spreader. This was for two reasons; some of the methods considered were either time consuming or were not feasible. They lacked feasibility because of the thickness of the paste. The application instructions said the silicon paste can be applied using a finger or a spreader. So using any other method with the nanotubes would not give conditions similar to the existing paste.

So, using a metal spreader the nanotube paste was applied evenly. The recommended thickness was about paper thick. We tried to match this as accurately as possible.

The application of the paste is shown in Figure 3.4 (a) (b) below.





Figure 3.4 (b)

Application of the nanotube paste

Once the application of the paste was complete, the heat sink was replaced, clamped on, and the areas around the heat sink were checked to see whether any paste was leaking (in case too much of it was applied). No leakage was found.

3.1.3 Initial measurements and temperature readings.

Before measurements could be made, we needed to determine how to heat the processor. This was important because, if the heating method was not consistent throughout the testing it would lead to discrepancy in the readings. This meant would not get a clear comparison between the two pastes being used.

Some of the methods that were considered for heating the processor were:

- Heating the processor using an air gun
- Using a hotplate to heat the processor.
- Using a software to load the processor

But the first two methods meant that the processor had to be taken out from the motherboard and then heated. These methods were abandoned as they would not mimic the actual working of the CPU.

The third method considered was, to use software which would work on the processor by running different operations like arithmetic, graphical, audio, video, and memory all at the same time to get the processor hot. But this method was abandoned too as it depended on the number of resources the operating system was using at any given time. If the processor was on lesser load when the software was run then it would take comparatively longer for the system to heat up than if we ran the software when the operating system was using more resources. So, this method was not consistent.
Finally, the method that was considered was just to run the processor without the fan until it stopped automatically (because of the thermal cutoff built in to the processor). The way this would work was to start up the CPU and let it run without booting (loading the Operating System) and keep it running till it turned off automatically. This method was chosen because this was consistent compared to the other methods mentioned above.

Once the method was set and the paste was ready, before testing it with the original CPU, a few tests were done to make sure that the paste held up as well as, if not better than the standard silicon paste.

In this test the paste was subjected to a continuous hot air for over 2 hours at an approximate temperature of 220°C. This was done to see if there would be any change in the consistency of the paste. Also the paste was subjected to cold air for the same duration of time to see if the paste showed any signs of hardening or any other physical change. This was done using a blower that was capable of blowing both hot and cold air, as shown below in Figure 3.5



Figure 3.5 - testing the consistency of the paste

It was found that, both the silicon paste and the paste that had the nanotubes mixed with it performed the same. This result was not expected but logically it seemed correct as the amount of nanotubes in the silicon paste is too little to show any significant difference when it came to physical changes at the macroscopic level.

Once this was done the next step was to test it on the actual CPU. Some of the thoughts while preparing for the test were

- Nanotubes are good conductors of electricity as well. At best, this could cause problems by shorting out parts of the processor
- We were not sure how consistent the method would be for heating the CPU
- Running the setup without the fan was a deliberate choice, so we could push the CPU to the maximum operable temperature before it would turn off automatically
- The time it might take for the CPU to turn off was also a concern because if the CPU did not turn off as expected it might cause the processor to burn out
- The placement of the thermocouples (which were used to take the temperature readings) was important, as wrong placement of the thermocouple could cause uneven contact between the processor and the heat sink. In some cases this would not let the CPU turn on. This was noticed when the CPU was not placed properly on the clamp; the improper contact caused the CPU not to turn on properly
- Since the thermocouple is a metal measuring device, great care had to be taken to make sure it does not cause any short circuit

• The ambient temperature was a concern, if the temperature changed a lot during readings this would lead to discrepancies in the results

These were some of the key concerns as the CPU was being setup for the initial test run. To get the temperature reading from the heat sink a K-type thermocouple was used.

The theory behind the thermocouples is as follows:

When two wires composed of dissimilar metals are joined at both ends and one of the ends is heated, there is a continuous current which flows in the thermoelectric circuit. Thomas Seebeck made this discovery in 1821. If this circuit is broken at the center, the net open circuit voltage called the Seebeck voltage is a function of the junction temperature and the composition of the two metals as shown in the Figure 3.6 (a) below



For example if the voltage $e_{ab}=1.112$ mv (Millivolts) then the equivalent temperature is 28° C. All the voltage measurements are made in Millivolts. The thermocouple was connected to

a DAQ (data acquisition) from Omega - OMB-DAQ. The DAQ came bundled with software called P-DAQ viewer that was used to get the temperature values and save them. Figure 3.6 (b) below show the Omega OMB-DAQ.



The next step was to choose the correct place to place the thermocouple, so we could get the readings. Three places were chosen, the base of the heat sink, in between the fins halfway up the heat sink, and the top of the heat sink, as shown in Figures 3.7 (a) and (b).



Figure 3.7 (a) – Thermocouple at the top of the fin

Figure 3.7 (b) - Thermocouple at the base of the heat sink

As can be seen, the thermocouples were glued to the heat sink using thermally conductive aluminum tape. This tape being conductive in nature helped in keeping the temperature being read by the thermocouple accurate. Also this setup meant that, the readings were taken from the heat sink and not directly from the processor.

The DAQ was designed to specifically obtain thermocouple readings, which made the task easy. The readings were made at one second intervals and were taken for a period of 30 minutes. This was the time for the processor to start from room temperature (approximately 28° C), run, turn off by reaching the cut off temperature (approximately 52° C), and cool back to about 30° C. The cut off temperature (at which point the CPU turned off) was around 52° C because the data sheets that were available mentioned that the maximum safe operating temperature for the chip was about 60° C to 65° C. So no chances were taken to get too close to the maximum operating temperature and risk a burnout of the processor.

The readings from the thermocouple were stored in Excel, and had headers, that indicated various settings of the DAQ like acquisition rate (number of readings per second). The software also labeled the columns appropriately indicating time and temperature columns.

The positions of the thermocouples were kept the same and the readings for the nanotube based paste and the silicon pastes were made. The values were saved in Excel, and were plotted to get a comparison between the nanotube paste and the silicon paste. The graphs from the plots are shown below in Figures 3.8 (a), (b), (c).



Figure 3.8 (a) – thermocouple at the base







Figure 3.8 (c) – thermocouple at the base with the fan on

3.1.3 Preliminary analysis

As shown in the above graphs the red line indicates the silicon paste without the nanotubes and the blue line indicates the one with the nanotubes.

From the first graph, it can be seen that the paste with the nanotubes reached the cutoff temperature of around 52 degrees slower than the silicon paste and cooled almost as quickly. This indicated that the nanotube paste was slightly efficient in terms of conducting the heat. But, when it came to the fin (Figure 3.8 (b)) the nanotube paste heated up to the cutoff point much faster than silicon paste and cooled off almost at the same time as the silicon paste. This indicated contradiction in the results when there was a change in the position of the thermocouple.

The third graph is an interesting one. Here the fan was placed back on the heat sink and the earlier thermocouple was connected back to the base. As it can be seen that the non-nanotube based paste reached a maximum temperature of about 38 to 39 degrees while with the nanotubes the maximum temperature it reached was only about 35 degrees. This is a 4 degree drop which in terms of the operation of the computer is good.

Both the plots indicated that the paste was effective. But the contradiction in the readings meant that there were some inconsistencies. We might not have taken the readings properly, or it might have been because the processor was old and that made the behavior of the processor finicky. All these doubts and inconsistencies led to the next stage of the experiment where more thermocouples were incorporated at different positions and a newer processor (Pentium D) was used.

3.2. Work done at the Indian Institute of Science, Bangalore, India

The experiments in this stage were performed at the Indian Institute of Science, Bangalore, India, in the composite lab at the Department of Aerospace engineering, under Prof. C R L Murthy.

The procedure and experimental setup were already outlined from the work previously done at UAB. It was now just a matter of repeating the procedure, and collecting the data from multiple points, to try and determine the source of the inconsistencies that were seen in the previous stage with readings from just one point. The system used was upgraded to a newer system with higher specifications. The use of a newer system felt more relevant as getting readings from the machines that are currently in use would give a better idea of how the paste held up with the current systems. The nanotube paste and the silicon paste used were the same as at UAB. There was no change in the procedure of the experiment, including the application of the paste.

3.2.1 System used and application of the nanotubes.

For this stage of the experiment, a machine with Pentium D processor and of 2GB ram was used. The availability of this machine for the experiment was exciting as this is a newer machine and the processor is in use today, giving a more realistic outlook to the experiment.

The changes in the CPU were obvious. As the processor technology evolved so did the heat sink. The older Pentium 4 processor used a heat sink made from aluminum (as shown in Figures (3.3, 3.7)). The heat sink that came with this machine was made with a combination of

aluminum and copper. The part of the base of the heat sink that was in direct contact with the paste and the processor was made of copper to help get better conduction.

On a side note about the heat sinks, one of the main reason aluminum is used more often than copper is that copper is much heavier than aluminum. The fact that these heat sinks are just fixed to the motherboard by 4 pins, and also, that they stand projected outward from the surface of the motherboard without any additional support is a concern. This is because the additional weight can cause it to lose contact or even break off from the processor. But, this does not stop people from using bigger and heavier heat sinks that come in various sizes and shapes and some even are liquid cooled. People who tend to use these bigger heat sinks are mostly people who are overclockers or gamers who use their systems under extreme performance conditions.

The heat sink on this system was made with a mix of aluminum and copper. It was circular and the outer fins were curved to follow the circular contour of the heat sink. The inner copper section was conical in shape as shown in Figure 3.9 (a) and (b) below.



3.9 (a) – Top view of the heat sink



3.9 (b) – Bottom view of the heat sink, with some nanotube paste on the back copper surface

Also below are some more Figures (3.10 - (a), (b), (c)) of the heat sink in different angles. Figures copyright owned by frostytech[©].com.



Figure 3.10 (c) – A complete view of the heat sink-dismantled.

The nanotube paste and the silicon paste were applied using a spreader, to the approximate thickness of a paper (as we had no exact way of making sure of the thickness we tried to visually approximate).

In the previous case (3.1) there was only one thermocouple used at a time; in this case 7 thermocouples were used simultaneously. The positions of the thermocouples on the heat sink are indicated below in Figures (3.11 (a) and (b)) below:



3.11 (a) –Positions of the thermocouples on the top surfaceheat sink



3.11 (b) –Positions of the thermocouples on base of the heat sink

- TC 1 The center copper contact
- TC 2, 3, 4 Bottom section of the heat sink next to the copper contact that sits right on top of the processor
- TC 5- Between the outer fins of the aluminum fins
- TC 6- In between the external fins and about midway at the intersection of the copper and aluminum center sections
- TC 7 The intersection of the copper center and the aluminum

The reason that the thermocouples were not placed directly on the copper contact that sits on the processor was that would not let the base come in complete contact with the processor. Partial contact of the heat sink with the processor was not sufficient, the entire base of the heat sink needed to be in contact with the processor. If this does not happen the system will not start up. (This was also verified by not clamping the heat sink on properly both at UAB and in this case, and because of this the CPU did not power up). So, just like the previous stage (at UAB), this meant that, we could not make the readings directly from the CPU. So, the readings that we obtained were a reflection of the CPU temperature on the heat sink.

That was the reason the thermocouples were placed around the base of the heat sink and not directly under the heat sink. The reason for placing the thermocouple in the center copper cylinder was simple; it was the part that was in the direct contact with the processor and was the hottest part of the heat sink. Placing the thermocouple at the junction of the copper center and the aluminum was to measure the temperature difference between the two places as no direct heat from the processor was sent into the aluminum part of the heat sink. The heat predominantly was conducted from the copper section. Placing the thermocouples around the fins made sense too. This is because, the fins are designed to help dissipate the heat at a faster rate that a solid block of aluminum or copper could. Once the thermocouples were connected the next logical step was to connect it to the DAQ and start taking readings.

3.2.2 Temperature measurement and problems encountered.

For the temperature measurements, instead of using a DAQ designed just for temperature measurement (as at UAB), a more general purpose DAQ designed by National Instruments was used. It was NI PXI 1031, designed to receive an analog signal and analyze it with the help of the proprietary software that National Instruments provides. For example, the input can be a voltage signal and it can be analyzed as a temperature input provided the input is coming from a

thermocouple, or the signal can be an electrical signal that can be analyzed by passing it through a circuit designed by the software provided. In general LABVIEW can be configured and used as needed. In this case it was configured to be used as a DAQ for recording temperature data using a K-type thermocouple. The DAQ looks as shown in Figure 3.12 below



3.12 – NI PXI 1031, with two 4 channel NI-TB 2705 DAQ cards.

The DAQ came with two 4 channel cards (meaning they can take 4 connections), so, two cards connected at the same time meant we had 8 channels to work with 7 simultaneous

thermocouples. Labview was configured to read the temperature data and store it in a text file (because the volume was too large to use Excel directly).

At this stage a lot of problems were encountered. The first and the hardest problem was leakage current flowing through the heat sink. This problem was not encountered in the previous experimental setup (at UAB). There was about 30 mA of current present in the heat sink and this drove the thermocouple readings off the scale and caused fluctuations in the readings (to the extent of $2*10^{-128}$ to $2*10^{128}$ degree Celsius). Though this problem looked like a simple issue of leakage current which might be due to improper grounding it took almost two weeks to solve. Various methods were tried to get rid of it. First the simplest method was tried; a UPS (uninterrupted power supply) was connected. This was because UPS is known to reduce or eliminate any leakage current. But this did not work. The leakage current dropped 2 mA to 28 mA.

After some thinking we hypothesized that the current may actually be EM radiation from various components that were present in the open CPU. It was an interesting analogy for the cause of a leakage current, which seemed quite plausible, given the number of high frequency devices in use, and also, the transformer present in the power supply unit of the CPU and other such devices. This gave a different perspective of looking at a CPU.

So the all the exposed wires of the CPU were shielded. This was done using metal mesh (flexible) casing covered up with Teflon tape which was expected to stop any radiation coming out of exposed cables or other parts of the CPU. The Figure 3.13 (a), (b) below shows the shielded CPU.



Shielded Cables, shielded with metal mesh casing and Teflon tape

3.13 (a)– Partly shielded CPU cabling.

As it can be seen in the above figure (3.13 (a)) only two cables were shielded. Initially all the loose wires and cables going into and coming out of the CPU (including the wires from the power supply) were shielded (the entire CPU was almost covered with white Teflon tape) and covered with aluminum foil as seen in the figure below (3.13 (b))



Shielding of all the cables coming into the CPU, shielded with metallic mesh, Teflon tape and finally outer aluminum foil casing

3.13 (b) – Completely shielded CPU

But even after doing this there was very little change in the leakage current value. So, this idea was discarded. This was one of the most interesting ideas for the cause of the leakage current, and one of the more interesting methods that was tried to eliminate the leakage current.

When the above methods did not work as successfully as needed, a more basic approach was tried – connecting the CPU to an external ground. The external ground in this case was a simple iron rod that is packed with crystalline salt (large pieces of salt that are not broken down into smaller pieces), and inserted into the ground in a hole about 3 feet deep with a thick copper wire (about ½ an inch thick) connected to it and used to ground the devices. This is the simplest and one of the most effective ways of grounding electronic devices. This method is generally

applied to ground devices that are high voltage devices. It can be seen in Figures 3.14 (a), (b) below, which shows the leads that were pulled out from the CPU and the heat sink for the purpose of grounding.



3.14 (a) – Grounding connections/leads drawn to connect to the external ground

Grounding connections drawn out to connect to the external ground.

Also as seen in the Figure 3.14 (b) below, the various components that were grounded to try to eliminate most of the leakage issues are indicated. As it can be seen almost all the components were grounded including the SMPS, the heat sink, the motherboard, the thermocouples, and the DAQ itself also had a lead drawn out and connected out.

Spike buster given connected to the UPS Grounding connections for the thermocouples given to the grounding point of the DAQ Grounding ground the

connections of the DAQ given to the common

Grounding connections of the heat sink given to

Grounding connection of the SMPS given to the common ground

3.14 (b) - Grounding connections/leads drawn to connect to the external ground

The wire connected to the external ground. All the wires that were drawn out to go to the ground are connected to this wire.

A common surge protector was used to supply power to all the instruments and this surge protector was connected to a pure sine wave inverter (UPS), just as a backup measure. This method worked and the leakage voltage dropped from 30mA to around 0.8 to 1.0 mA. Though this still caused some fluctuations in the readings, a low pass filter was added in the software that was used to collect the temperature data.

3.2.3. Collecting data and software used.

The software used for collecting data as mentioned was Labview. This software came bundled with the NI- DAQ. As mentioned earlier the software was multipurpose and included support for different types of data acquisition like audio signal, electric signals, it also had various post processing tools that could be used, including a graph generator, and a DSP processor. The design that was used for this experiment was set up to have a DAQ node that would acquire the voltage signal from the (k-type) thermocouple, and, convert it to the equivalent temperature value. Also as mentioned above, even though the leakage current was reduced to 0.8 to 1.0 mA, this still caused a fluctuation in the readings. To overcome this, a filter of 100 Hz was added that made sure that the input would be filtered, so, the fluctuation could be reduced. Once the filter was added the fluctuation dropped considerably, and the temperature readings were made. The filter was set at a 100 Hz, so any signal below that range would be filtered out. One of the side effects of this was that, the data that were collected had a lot of points. The data were collected over a period ranging from 2800-3000 seconds and this meant that there would be about 280,000 to 300,000 points.

Given that there was fluctuation in the software that was recording the readings due to the presence of leakage current, an infrared (IR) thermometer was used to check the accuracy of the

thermocouple measurements. The readings from the thermocouple matched the readings indicated on the IR thermometer, which was indicative that the grounding method and the low pass filter of 100Hz that was added in the acquisition software worked.

Also, a thermal camera was used as a backup measurement device to see if the readings and the rate at which the processor gained and lost heat would be the same. The readings from the thermal camera matched the readings obtained using the thermocouple, in terms of the time taken to complete the cycle of heat up – cutoff - cool down. A snapshot of the thermal camera is shown in Figure 3.15 below.



.15 – thermal camera snapshot a approximately the cutoff point

Minimum temperature at that instance A comparison of the normal aluminum heat sink and the copper-aluminum heat sink were also done with the thermal camera. The snapshot of the thermal camera video is shown below in Figure 3.16



3.16 – thermal camera snapshot of two different heat sinks

As it can be seen, the heat sink with copper is at a higher temperature (more white spots indicating higher temperature) compared to the aluminum heat sink. Also, it can be observed that, in the copper heat sink the heat is being radiated out in a circular pattern from the center region that is the hottest to the fins that get cooler at the outer ends, it is as though the heat is following a pre set path. In case of the aluminum heat sink it can be seen that the outer ends seems to be hotter with scattered hot regions.

3.3 Common observations in both cases of the experiment.

One of the interesting observations in both the cases of the experiment was when the heat sink was removed from on top of the processor. In both cases the paste (both the nanotube and the silicon paste) seemed to form a pattern as shown in the Figure 3.17 (a), (b), (c), (d) below. For the images 3.17 (c), (d) the contrast of the images has been changed to highlight the pattern formed by the white silicon paste



Figure 3.17 (a) – Pattern formations on the processor after the heat sink was taken out

Figure 3.17 (b) – Pattern formations on the back of the heat sink

Nanotube Paste



Figure 3.17 (c) – Pattern formations on the processor after the heat sink was taken out

Figure 3.17 (d) – Pattern formations on the heat sink

Silicon Paste

(The contrast of the images has been changed to highlight the pattern formed by the white silicon paste)

This pattern formation was found common in both experimental cases. We are still not sure why this pattern was formed.

A second observation was during plotting the results. As it can be seen from the plots below the curve followed by the two heat sinks were the same. The only difference seems to be the time taken for the processor to reach its cut off point.



Figure 3.18 (a) – Similarity in the plots of the two heat sinks



two heat sinks

As it can be seen from the above plots (concentrating on the heating up part), in the first plot with the aluminum heat sink and the nanotube paste plot (blue line), it seems to reach the cutoff point (of approximately 52^{0} C) somewhere at about 639 seconds. Looking at the second plot from the second heat sink the indicated nanotube line shows that the CPU reached the same approximate temperature at about 600 seconds. In both the cases, the thermocouple was at the base of the heat sink. This is an interesting observation because the second heat sink used (in the second stage of the experiment), was a composite heat sink (made with copper and aluminum), and ideally it should have had better conductivity and should take a little longer to reach this temperature, as it would be able to conduct heat from the processor at a faster rate due to presence of copper, which is in direct contact with the processor.

Chapter 4

Results and Analysis

4.1 Results

The plots below compare the performance of the nanotube based paste and the regular silicon paste. Some points to keep in mind are as follows:

- The thermocouples were placed in the first case (UAB) for measurement as indicated in Figures 3.7 (a), (b).
- In either case the thermocouple was not placed in direct contact with the processor; in both cases the thermocouples were placed to measure the temperature at the base and other areas on the heat sink
- The positions of the thermocouples for both the stages of the experiments are mentioned in sections 3.1 and 3.2
- The thermocouples were glued to the heat sink using aluminum tape that was also heat conduting
- In the first case of the experiment only 1 thermocoule was used, while in the second case 7 thermocouples were used
- The paste remained the same and the overall experimental setup remained the same

The reason for not placing the thermocouple directly on the processor was that, unless there was the a direct contact of the heat sink with the processor the system did not get turned on, this true in both cases. This again meant that, the readings we made were only from the heat sink nothing directly from the CPU.

4.1.1 Results stage 1 (UAB)

Below are plots from the first set of readings. The plots show a comparison between the nanotube and non-nanotube based paste. The plots below are from UAB (only one set of readings with one thermocouple)

Given below is the first set of readings from UAB.







Figure 4.1 (b) – thermocouple at

the fin



Figure 4.1 (c) – thermocouple at the base with the fan on

In the plots, the red line indicates the non nanotube based paste and the blue line indicates the nanotube based paste. The same color scheme for distinciton between the pastes applies through out this section.

Looking at the plots

- From the first graph it can be seen that, the paste with the nanotubes reached the cutoff temperature of approximately 52 degrees slower than the silicon paste. It cooled almost as quickly, indicating that the nanotube paste was slightly more efficient in terms of conducting the heat.
- But in figure 4.1(b) (the fin), the nanotube paste heated up to the cutoff point much faster than silicon paste and cooled off at rate almost similar to the silicon paste. This shows a contradiction in the results with a change in the position of the thermocouple.
- The third graph Figure 4.1 (c) is an interesting one. Here the fan was placed back on the heat sink and the thermocouple was connected to the base. It can be seen the non-nanotube based paste reached its maximum consistent temperature of about 38 to 39 degrees while with the nanotubes the maximum temperature reached was only about 35 degrees. This is a 4 degree drop.

Again from the work done in [1], the authors mention that, they saw a 125% increase in the thermal condutivity of the epoxy paste that was preared with 1 wt% of nanotubes. Looking at the third plot it can be seen that there was a reduction in operation temperature by approximately 4 degrees with the fan on. Under ideal circumstances, and, according to [1], we were to expect about 6.5% difference in operating temperature.

A 6.5% drop in temperature just for the third plot without the nanotubes reached 39 degress would be approximately 2.53 degrees. But a 4 degree drop resulted; indicating a 10.25 % difference in the temperature. But, the results of the experiment can not be concluded just on this one result. The other two plots of this stage did not support this conclusion. In this stage, the CPU was not let to run till it cut off automatically. In this stage the CPU was turned off at approximayely 52 degrees to make sure the CPU was kept under the recommended running temperature. This is where the second stage of results differ, this is because, in this case the CPU was run till cut off in this stage. This is because for second stage the recommended safe operating temperature was higher than the first case and the CPU cut off automatically before the CPU could reach that temperature.

4.1.2 Results stage 2 (IISc)

Given below are the plots from the second stage of the experiment. The data as mentioned earlier, had anywhere between 250,000 to 300,000 points. These points have been averaged using the moving average method (with an average of 1000 points), the starting point for all the plots was made common; from the point when the CPU was turned on, rather than from when the thermocouple was placed on the heat sink.

The time readings for when the cpu was started, to when it turned off automatically after reaching the cutoff point, and when the readings stopped indicated in Table 4.1 below.

Paste	CPU turned on at (seconds)	Auto off at (seconds)	CPU power off at (seconds)	Readings stopped at (seconds)
Non-nanotube set 1	305 seconds	815 seconds	855 seconds	2948 seconds
Non-nanotube set 2	310 seconds	660 seconds	705 seconds	3240 seconds
Nanotube set 1	240 seconds	767 seconds	780 seconds	2880 seconds
Nanotube set 2	420 seconds	888 seconds	907 seconds	3360 seconds

Table 4.1 – Time readings

As it can be seen from the above table

- first set of non nanotube data readings ran for 510 seconds before getting cut off (Auto cut off)
- the second set of non-nanotube data ran for 350 seconds (Auto cut off)
- the first set of nanotube data ran for 527 seconds (Auto cut off)
- And the second set of nanotube data ran for 468 seconds (Auto cut off)

From the above observations it can be seen that, the nanotube based paste ran for longer than the non-nanotube based results. The time difference between them is not substantial in the case of the first set of readings (nanotube and non-nanotube set 1); also meaning that it did not show a substantial increase in running time. But in the second set of readings, the nanotube paste ran for a substantially longer time than the non nanotube paste. This indicated inconsistency in the readings, which are discussed in detail in Section 4.2

In [1], the sample that was loaded with 1wt% of single walled nanotubes showed a 125% increase in the thermal conductivity of the specimen. In our case the silicon paste was mixed with 0.05 wt% of nanotubes. This should ideally give us a 6.25 % ((0.05*125%)) increase in thermal conductivity. The positions of the thermocouples on the heat sink are given below, the plots are based on these positions (plot $1 - 1^{st}$ thermocouple and so on)

- TC 1 The center copper contact
- TC 2, 3, 4 Bottom section of the heat sink just next to the copper contact that sits right on top of the processor.
- **TC 5-** Between the outer fins of the aluminum fins
- 6- In between the external fins and about midway at the intersection of the copper and aluminum center sections.
- 7 The intersection of the copper center and the aluminum

The graphs below also follow the same color scheme mentioned earlier, where the blue graph indicates the nanotube based paste and the red graph indicates the normal silicon paste. Also, in the plots below the CPU was let to run till the cutoff point as the CPU turned off before it could reach the recommended maximum operable temperature. Again according to [1], we are to expect to see a 6.5% change in temperature for the amount of nanotubes used in our case. For this case, the average cutoff temperature for the normal silicon paste is in the range of 76-77°C, so a 6.5% difference should yield a difference of approximately 5°C. We shall analize the

graphs below individually, to see if we have obtained a temperature difference between the two pastes close to the expected value.

There are 14 different plots for the second stage of the experiment, two each for the 7 different thermocouples used in this stage, for two rounds of experiments. The numbers below indicate the number of the thermocouple and its position on the heat sink, and the graphs follow the same numbering method as well, that is the first plot corresponds to the first thermocouple and so on.

For the plots the data have been modified. The data have been cropped to the time the computer was booted up. The earlier plots had data that were collected from even before the cpu was started up. For example, the cpu for the non-nanotube based paste for the second stage of the experiment was started up 5.05 minutes (305 seconds) after begning to make a note of the temperature readings. So in these plots start time is the time at which the cpu was booted.





In the above plot, for the first thermocouple it is observed that the non-nanotube paste cutoff at approximately 78.1°C, and the nanotube based paste cutoff at approximately 80.3°C. This gives us a temperature difference of approximately 2.2°C. Our expected difference is about
5°C (from [1], according to which we need to get a 6.7% difference in temperature which is approximately 5°C. The 2.2 degree increase in temperature is approximately 66% lower than the expected reading.



Figure 4.3 (b) - Thermocouple 2 - X – Time, Y - Temperature nanotube paste (blue) vs silicon paste (red)

Again looking at the data and the plot for the second thermocouple, it is observed that the non-nanotube based paste cutoff at approximately 78.1°C, while the nanotube based paste cutoff

at approximately 81.5° C, showing a 3.4° C difference in temperature. Though we see an increase from the temperature of the previous thermocouple we are still off by about 32% from the expected value (6.7% increase).



In the above plot for the third thermocouple, it is observed that the non-nanotube paste cutoff at approximately 76.6°C, and the nanotube based paste cutoff at approximately 80°C. This gives us a temperature difference of approximately 3.4°C. Even in this case we are still off by about 32% from the expected value (6.7%Increase).



In the above plot for the fourth thermocouple, it is observed that the non-nanotube paste cutoff at approximately 77.6°C, and the nanotube based paste cutoff at approximately 79.04°C.

This gives us a temperature difference of approximately 1.44°C. This is off by approximately 71.2 % from the expected value.



In the above plot for the fifth thermocouple, it is observed that the non-nanotube paste cutoff at approximately 74.2°C, and the nanotube based paste cutoff at approximately 75.2°C. This gives us a temperature difference of approximately 1.03°C. For this thermocouple we are off by 79.4 % from the expected value.



In the above plot for the sixth thermocouple, it is observed that the non-nanotube paste cutoff at approximately 75.2°C, and the nanotube based paste cutoff at approximately 79.°C. This gives us a temperature difference of approximately 3.8°C. This is approximately 23.8% less than the expected value.



In the above plot for the seventh thermocouple, it is observed that the non-nanotube paste cutoff at approximately 74.3°C, and the nanotube based paste cutoff at approximately 75.6°C. This gives us a temperature difference of approximately 1.3°C. Again this off by approximately 73.6% from the expected value.

The table 4.2 below gives an overview of the approximate expected temperatures, and the obtained temperatures with the percentage difference between the expected value and the obtained value.

	values re	ound 1	
Thermocouple number	Expected temperature difference (6.7%)	Actual temperature difference	Percentage difference
1	5	2.2	56%
2	5	3.4	32%
3	5	3.4	32%
4	5	1.44	71.2%
5	5	1.03	79.4%
6	5	3.81	23.8%
7	5	1.32	73.6%

Table 4.2 – Expected VS Obtained

As it can be seen from the results indicated in the above table, it is not as per the expected value indicated in [1]. There are also some inconsistencies in the results as well, and the values do not show any specific pattern. The difference in temperatures for different thermocouples could be due to the positions. This has been discussed more in detail in the nest section (4.2).

Stage 2 - Experiment round 2 results

Given below are plots for the second set of experiments. From the plots it is evident that there is a serious contradiction from the first round of experiments. This becomes more evident when we look at the difference in the expected and obtained values.



In the above plot for the first thermocouple, it is observed that the non-nanotube paste cutoff at approximately 69.9°C, and the nanotube based paste cutoff at approximately 81.81°C.

This gives us a temperature difference of approximately 11.91°C. This shows an approximate improvement of 138.2%.



In the above plot for the second thermocouple, it is observed that the non-nanotube paste cutoff at approximately 71.8°C, and the nanotube based paste cutoff at approximately 81.3°C. This gives us a temperature difference of approximately 9.5°C. This shows an approximate improvement of 91%.



In the above plot for the third thermocouple, it is observed that the non-nanotube paste cutoff at approximately 67.2°C, and the nanotube based paste cutoff at approximately 80°C. This gives us a temperature difference of approximately 12.7°C. This shows an approximate improvement of 154.6%.



In the above plot for the fourth thermocouple, it is observed that the non-nanotube paste cutoff at approximately 69.23°C, and the nanotube based paste cutoff at approximately 80°C. This gives us a temperature difference of approximately 10.7°C. This shows an approximate improvement of 115.4%.



In the above plot for the fifth thermocouple, it is observed that the non-nanotube paste cutoff at approximately 67.2°C, and the nanotube based paste cutoff at approximately 76.1°C. This gives us a temperature difference of approximately 8.8°C. This shows an approximate improvement of 77.8%.



In the above plot for the sixth thermocouple, it is observed that the non-nanotube paste cutoff at approximately 67.2°C, and the nanotube based paste cutoff at approximately 79.9°C. This gives us a temperature difference of approximately 12.6°C. This shows an approximate improvement of 77.8%.



In the above plot for the seventh thermocouple, it is observed that the non-nanotube paste cutoff at approximately 65.4°C, and the nanotube based paste cutoff at approximately 74.5°C. This gives us a temperature difference of approximately 9.09°C. This shows an approximate improvement of 81.8%.

The table 4.3 below gives a summary of the expected and obtained values for the second round of experiments.

	values ro	ound 2	
Thermocouple number	Expected temperature difference (6.7%)	Actual temperature difference	Percentage difference
1	5	11.91	138.2%
2	5	9.55	91%
3	5	12.73	154.6%
4	5	10.77	115.4%
5	5	8.89	77.8%
6	5	12.63	152.6%
7	5	9.09	81.8%

Table 4.3 – Expected VS Obtained

As it can be seen from both the plots and the table the results completely contradict the results that we got both at UAB and the first round at IIS Bangalore. We are not sure why the results obtained in this round show this much of an increase. A more detail analysis of these results is in the next section (4.2).

4.2 Analysis

As it can be seen from Table in section 4.1 table the results we got were not the expected values. There could be many reasons for this, but first let us go back again to what we were trying to achieve in this experiment.

Carbon nanotubes even though are still a new technology they have created a lot of interest for their thermal conductivity properties (6600 W/mK) among many other excellent properties they possess ^[7, 8]. There have been various experiments that have been and that are being conducted ^[1] to try to see if using carbon nanotubes in materials can help in improving its thermal conductivity.

Thermal pastes have been used in CPU's to help aid heat transfer from the processor to the heat sink. Of late a lot of varieties of these thermal pastes have been available in the market. Some of these come with silver particles in them so they can help improve the heat transfer from the processor to the heat sink. These kinds of pastes are indicative that modifying the thermal paste in use with materials with higher conductivity can improve the heat transfer rate. This means that carbon nanotubes that have excellent thermal conductivity values (in the range of 6600W/mK) can dramatically improve the heat transfer rate from the processor to the heat sink if the thermal paste used is modified by adding nanotubes. A simple explanation for this hypothesis is as follows:

Let us consider a heating circuit (if we look at the above figures 3(a), (b)) with the CPU as the source and the thermal paste as a conducting medium, another intermediate material (in our case the heat sink) and the final part of the circuit air. Tm is the intermediate temperature between the CPU and the air, this is the temperature that we actually measured.

Now when the heat is generated by the CPU it travels through the paste to the intermediate material (heat sink) and then to air. Like any conducting circuit in this case as well there will be resistance to the flow of heat through the paste, the intermediate material (heat sink) and air.

Let the resistance of the paste be (=) Rp, and the resistance of the intermediate material (heat sink) and air be (=) Ro, let Q denote be the heat, then,

Q = ((T(cpu) - T(air)) / (Rp+Ro)).

Now, let B = (Rp / (Rp+Ro)), and (then,) we get

The intermediate temperature (thermal conductivity) Tm = ((T(cpu) * (1-B) + B * T(air))).

This means that, as the nanotubes reduce the resistance B decreases. (This gives us Tm > T(cpu) implying a higher T(cpu) (higher CPU temperature).) Thus Tm approaches Tcpu with nanotubes in the paste and a higher temperature reading is obtained

In the equation, if B went to zero (no resistance between the CPU and the first thermocouple) the two readings would be the same.

The results that have been obtained so far have been in line with the equations above. But, they have not been reflective of the predicted dramatic improvement in thermal conductivity ^[1]. At best, the results that we have got in both the stages of experiments have lacked consistency each time the experiment has been performed. The results have jumped from showing a promising increase in the running temperature, to values that were approximately 50% or more below the expected value. The tables below (repeated from the previous sections) are indicative of this inconsistency in results.

Let us first take a closer look at the results from the first set of experiments done at UAB. The figures 4.5 (a), (b), (c) below show the plots for the results from the first stage of the experiment (UAB). One thermocouple was used, and it was placed first at the base, on the fin and at the base with the fan running on the heat sink. The plots below were obtained from the above placements of the thermocouple.







As it can be seen from the graphs the only plot that is close to the expected result of approximately 5°C [from 15] is the one with the fan on. But as it can be seen from Figure 4.5 (a) there was a difference in running time between the paste with the nanotubes and the silicon paste. The nanotube paste shows a slightly longer running time of 100 seconds (1.40 minutes). But in the second plot (Figure 4.5 (b)), with the thermocouple at the base shows that the silicon paste ran longer than the nanotube paste although there is very little difference of about 35 seconds. This is still a contradiction with respect to the previous plot and with respect to the expected results.

Now, let us consider the second set of results from the experiments done at the Indian Institute of Science, Bangalore, India. The table below (table 4.1 as before) shows the running times for the two sets of experiments that were run.

Paste	CPU turned on at (seconds)	Auto off at (seconds)	CPU power off at (seconds)	Readingsstoppedat(seconds)
Non-nanotube set 1	305 seconds	815 seconds	855 seconds	2948 seconds
Non-nanotube set 2	310 seconds	660 seconds	705 seconds	3240 seconds
Nanotube set 1	240 seconds	767 seconds	780 seconds	2880 seconds
Nanotube set 2	420 seconds	888 seconds	907 seconds	3360 seconds

Table 4.1 – Time readings

It can be seen from the Table that there is a difference between the running times between the two sets of experiments. The first set without the nanotubes, ran for 510 seconds before it cut off automatically, and for the same set with the nanotubes it ran for 527 seconds, an improvement of 17 seconds. For the second set of the experiment the non nanotube paste ran for 350 seconds while the one with the nanotube ran for 468 seconds. That is an improvement of 118 seconds, compared to the 10 seconds of the first set of the experiments. From the running times the inconstancy in the results from the two rounds of experiments can be seen.

Now, taking a look at the expected and obtained temperature values from the graphs this inconsistency become more significantly visible. The table below (table 4.2, from the previous section), shows the difference in the expected and the obtained values can be seen.

Thermocouple number	Expected temperature difference (6.7%)	Actual temperature difference	Percentage difference
1	5	2.2	56%
2	5	3.4	32%
3	5	3.4	32%
4	5	1.44	71.2%
5	5	1.03	79.4%
6	5	3.81	23.8%
7	5	1.32	73.6%

Table 4.2 – Expected VS Obtained values round 1

Let us consider thermocouples 2, 3 and 4. They were placed at the base of the heat sink. This means that they would be the least exposed to surroundings and would have most of the heat coming from the processor to pass through the heat sink, and hence any large difference that could be seen will be seen here. We can see a considerable difference in the temperatures from thermocouples 2, 3 and 6 (6, which was placed in between the external fins and about midway at the intersection of the copper and aluminum center sections) compared to the rest. As it can be seen, the best values that are closest to the expected value of 5°C [from 15] are number 2, 3, and 6. The rest are off by (lower) 66% to 79%.

Now taking a look at the second set of the experiment, the table below (table 4.3 from the previous section) indicates the expected values and the obtained values (in this case much higher than the expected results).

Thermocouple number	Expected temperature difference (6.7%)	Actual temperature difference	Percentage difference
1	5	11.91	138.2%
2	5	9.55	91%
3	5	12.73	154.6%
4	5	10.77	115.4%
5	5	8.89	77.8%
6	5	12.63	152.6%
7	5	9.09	81.8%

Table 4.3 – Expected vs Obtained
values round 2

As it can be seen from the previous table (Table 4.3), the difference was between 66% to 79% and the obtained results were less than the expected value by that percentage. But in the second set, the difference lie between 81% and 154%, and it was higher than the expected value by that percentage. There is not much that can be said about these results that show such a dramatic increase in conductivity. The only thing that we can hypothesize is that the reading in this stage might have some kind of an error, or there might have been an error during the measurement. A Possible hypothesis is that, because we were removing and placing the heat sink back multiple times there might have been some damage. Also, as we were

running the processor without the fan at high temperatures this might have caused possible damage to the processor.

A range of difference between the expected and obtained values for both the rounds of experiments lies between -66% (lower than expected) to +154% (above the expected value). This range of difference between the values is difficult to analyze. To begin to put a finger on it is hard, but some of the first flaws that come into mind are that might have caused the difference to this extent (also taking into consideration the contradiction in the results from the first set of data from UAB) are as follows.

- Inconsistency in the way the paste was prepared/mixed: As mentioned in section 3.1, the paste was prepared by mixing the silicon paste with nanotube powder by hand.
 Although, the mixture looked uniform to the eye, there could have been inconsistency at the microscopic level that could have led to the results that we got
- ii. The application of the paste: As mentioned in Sections 3.1 and 3.2, for both the experiments the paste was applied by hand. This could have led to a inconsistent application of the paste that again led to the inconsistency in the results
- iii. The concentration of nanotubes: The amount of nanotubes added was about 0.05 wt%, and this could have been the reason that in the first round of experiments at UAB and the second round first set from the experiments done in India showed values approximately 50-60% less than what was expected. But, this does not explain why the second set of data from the experiments in India gave exceedingly high values

- iv. Alignment of the nanotubes: Alignment of nanotubes in itself is a topic under research. Alignment of nanotubes would theoretically give better heat flow ^[7, 8]. So, hypothetically, non aligned nanotubes could show a difference of approximately 50% than aligned nanotubes (assuming the best case scenario). This is about what our results from UAB and the first set from India indicate. Also in [1], the nanotubes were aligned and so they showed a 125% increase in the thermal conductivity. But, this does not explain the unusually high results we got for the second set of experiments in India
- v. Ambient conditions: As the heat from the heat sink was not dissipated using a fan, but it was left to radiate out to the surroundings any change in the ambience and the ambient temperature could have led to the differences seen in the results. The two sets of experiments done in India took a long time to run, and the experiments were run from the afternoon till late in the night. The two sets were run on different days. The test runs in the afternoon might have shown lesser temperature difference as the ambient temperature was hotter then than night times

If we might consider the results obtained in the second set of experiments from India (with 154% difference) as unexpected and erroneous readings and disregard the readings. Then the readings from UAB and first set from India are more in agreement with each other and as they show more consistency. If we take those two cases as the only results in consideration, then points I, iii and iv make a lot of sense. Also, if they were the only two results in consideration then:

- vi. According to [8], the nanotubes have so far shown a lot of difference between the theoretical and experimental values (about 40%). As in our case this explanation can hold true and then our results would be almost in line to what was expected.
- vii. Also in [1], it is indicated that, the epoxy they prepared did show substantial improvement but the nanotubes when mixed with the epoxy did not show an increase in thermal conductivity in accordance with the Law of Mixtures, the value obtained was lower. This again would explain why we would see the difference that we see in the expected values and the obtained values from UAB and the first set of experiments from India
- viii. It might be that two materials that do not mix well i.e., they may not form a consistent and homogenous mixture and the silicon may actually be hindering or bringing down the thermal conductivity of the nanotubes, which may lead to the discrepancy we see. This is an only my hypothesis.

The previous three points would hold argument only if the last set of experiments done in India (with 154% difference) were not taken into account or, the previous points would not hold good and if the 154% difference values may be the right ones to consider. The only solutions to this is more future work, and to collect more results with a variation in the concentration of nanotubes. Also, a way to mix and apply the nanotubes in a more consistent way, and a more thermally controlled environment to perform the experiments may lead to more clarity.

Chapter 5

Conclusion and Future work

In this experiment, we have tried to see if modifying a commercially available silicon paste used in CPUs by adding carbon nanotubes would help in cooling CPUs faster. The experiment was done in two stages. In the first stage, which was at the University of Alabama, Birmingham, we came up with the initial experimental setup, prepared the nanotube paste and ran a few rounds of tests. In the second round of tests, which were run at the Indian Institute of Science, we tried to eliminate the inconsistencies that we encountered in the first stage. We tried to achieve this by increasing the number of points from which we got our readings, so the data collection points went up from 1 in the first stage, to 7 in the second stage.

Though the results that we got showed some positive indications, they were not close to expected values. There were some inconsistencies in the results that we got. The results from the first stage in the experiment were in partial agreement with the results of the first set of data from the second round of experiments. The second set of data from the second stage of the experiment, showed results that were much higher than the expected results. Among all the readings, the reading that showed the most promise was the one from the first set of data with the fan on. This showed a 5 degree difference in operating temperature which was promising.

Ali Shakouri [8] mentions that the experimental and theoretical values for the thermal conductivities for CNTs showed a lot of difference. This could also be a reason why we did not get the results as expected. The results that we got, as shown in the difference between the expected and actual obtained results with the use of CNTs.

Another factor that could be hypothesized as a reason for getting results that were mostly lower than what was expected could be that the nanotubes were not aligned. The procedure for aligning nanotubes is also an active research area as of now. As in [1] the nanotubes that were aligned showed a higher increase in the thermal conductivity. As hypothesized in section 4.2 this improper alignment could be the reason why we saw results that were approximately 50% lower than what was expected.

Although the results were not as expected there are a number of positive indications, enough to encourage future work. Some of the focus points for future work could be

- Change in the concentration of nanotubes to see if an increase in the percentage of nanotubes would make a difference
- More measurement points and if possible, closer to the processor so we can get better readings
- Aligning the nanotubes so as to get better conductivity
- A more consistent method to prepare and apply the nanotube based paste

These are a few aspects if improved we should be able to see a noticeable difference in the conductivity.

Although the results that we got were not very consistent, and were not very close to the expected values there are a lot of positives that we can get out of this research. We were able to establish an experimental setup for the first time for this kind of an experiment. We were able to make multiple readings without changing the experimental setup, which tells us that the experimental setup is capable of consistent performance. This exact kind of work has not been

done so far, and so, getting the results that we have, which show a positive trend is a step in the right direction. If the above points were implemented and if additional work can be done, there is a possibility of seeing a noticeable improvement in the thermal conductivity of the paste and also an improvement in the processors performance, which is the ultimate goal of this research work.

At this point, there are inadequate data to conclusively state if the experiment was a success or a failure. The only conclusion that can be drawn out of this entire experiment is that the number of variables that can cause the experiment to go wrong (preparation of the nanotube paste, application of the paste, etc) are numerous, and although the experimental setup worked the way we wanted it to the results were inconclusive. Unless the variables can either be brought down, or a method can be developed that can keep these variables in check it is hard to get consistent results. But, there is a lot of work that supports the fact that nanotubes do not yield the same values experimentally as the theoretical values state. This is one of the biggest factors that could have been a cause of the inconsistency as well.

In conclusion, the only solution as of now is to just do more work and perform more experiments and try to investigate and eliminate each variable cautiously and see if there is a noticeable difference.

Chapter 6

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