THÈSE

En vue de l'obtention du

DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

Délivré par :

Institut National Polytechnique de Toulouse (Toulouse INP)

Discipline ou spécialité :

Génie Electrique

Présentée et soutenue par :

M. DAVIN GUEDON

le mercredi 2 février 2022

Titre :

Amélioration des performances des convertisseurs HVDC mis en oeuvre pour le raccordement des parcs éoliens offshore lointains : évaluation du potentiel des nouveaux composants IGCT

Ecole doctorale :

Génie Electrique, Electronique, Télécommunications (GEETS)

Unité de recherche :

Laboratoire Plasma et Conversion d'Energie (LAPLACE)

Directeur(s) de Thèse :

M. PHILIPPE LADOUX

Rapporteurs :

M. CYRIL BUTTAY, INSA LYON

M. DRAZEN DUJIC, ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE

Membre(s) du jury :

M. SEDDIK BACHA, INP DE GRENOBLE, Président

M. CHRISTIAN WINTER, ABB SEMICONDUCTORS LENZBURG, Invité(e)

M. MEHDI KANOUN, EDF ECUELLES, Membre

MME MARIE-LAURE LOCATELLI, TOULOUSE INP, Membre

M. PHILIPPE LADOUX, TOULOUSE INP, Membre

M. SÉBASTIEN CORNET, EDF ECUELLES, Invité(e)

M. SÉBASTIEN SANCHEZ, TOULOUSE INP, Membre

M. THOMAS STIASNY, ABB SEMICONDUCTORS LENZBURG, Membre

Acknowledgements

J'ai démarré ma thèse en novembre 2018 au laboratoire LAPLACE, via le dispositif CIFRE, avec l'entreprise EDF. Je tiens à m'adresser aux personnes que j'ai côtoyées durant ma thèse, ponctuellement ou régulièrement, et qui m'ont apporté leur soutien technique et/ou humain.

Je souhaite premièrement remercier mon directeur de thèse, Monsieur Philippe Ladoux, Professeur des Universités à l'INP de Toulouse, de m'avoir accompagné tout au long de cette aventure. Son expérience, ses connaissances et son appétence pour le domaine ont très fortement contribué à la réussite de ma thèse. Je lui dois cette collaboration avec EDF R&D, qui tient ses origines d'une blague que je ne peux malheureusement pas retranscrire ici, et ABB Semiconductors. Je le remercie plus encore pour sa bonne humeur en toutes circonstances, ainsi que pour les expériences sportives et culinaires que nous avons partagées. Merci. Je remercie mon co-encadrant de thèse, Monsieur Sébastien Sanchez, enseignant-chercheur à l'ICAM de Toulouse. J'ai apprécié son engagement durant ces trois années, et l'intérêt immuable qu'il a porté à mes travaux. Sa présence à mes côtés dans les moment importants de la thèse, de Toulouse à Busan en passant par Moret-sur-Loing, a beaucoup compté.

Je tiens à remercier Monsieur Mehdi Kanoun, ingénieur-chercheur à EDF R&D, d'avoir encadré les premiers mois de ma thèse ainsi que mon stage de fin d'études. Il a su m'accompagner dans mes débuts à EDF, malgré la distance. Je le remercie également d'avoir intégré mon jury de thèse. Je veux remercier mon (deuxième) encadrant industriel Monsieur Sébastien Cornet, Chef de Projet Senior à EDF R&D. Ses corrections d'articles et de documents m'ont beaucoup apporté sur le plan technique et professionnel. Son expérience et ses connaissances "des labos" ont été décisives lors de la mise en exploitation du "Power Conversion Lab" (que nous n'avons pas pu appeler "POSEIDON" à mon grand regret). Je remercie Monsieur Thomas Stiasny et Monsieur Christian Winter, de Hitachi Energy, pour la richesse de la collaboration établie avec le laboratoire LAPLACE et EDF R&D. Merci à eux pour le matériel et les données qu'ils ont fournis, pour leur expertise sur l'IGCT, et plus largement pour leur implication dans le projet.

Je souhaite remercier les deux rapporteurs, Monsieur Cyril Buttay, Directeur de Recherche au laboratoire Ampère, et Monsieur Drazen Dujic, Professeur titulaire à l'Ecole Polytechnique Fédérale de Lausanne (EPFL), d'avoir accepté de réviser mon manuscrit de thèse. Je remercie également les membres du jury non cités ailleurs, à savoir Monsieur Seddik Bacha, Professeur des Universités au G2Elab, et Madame Marie-Laure Locatelli, Chargée de Recherche au laboratoire LAPLACE, d'avoir accepté d'évaluer mes travaux de thèse.

Je souhaite remercier Monsieur Jean-Marc Blaquière, ingénieur d'études au laboratoire LAPLACE, pour l'expertise qu'il a apporté à la conception du banc d'essais, pour le temps qu'il y a consacré ainsi que pour son implication globale dans le projet. Merci à Monsieur Didier

Flumian, ingénieur au laboratoire LAPLACE, pour son aide précieuse lors des essais ! Je tiens à remercier de manière plus globale le groupe de recherche Convertisseurs Statiques (CS), auprès duquel j'ai appris et évolué.

Je tiens à remercier le bureau E410, entité immobilière du laboratoire LAPLACE, qui a abrité de chaleureux locataires : merci à Andrea Verdicchio de m'avoir initié au café napolitain, et à Kamil Mrozewski de m'avoir préféré à Andrea pour le bureau à côté de la fenêtre (c'est le meilleur). Je veux également remercier Mohsin et Thomas pour les moments que nous avons passés ensemble. Un grand merci au patriarche de ce bureau, Monsieur Joseph Fabre, ancien ingénieur-docteur à la SNCF (et "extérieur émérite" au laboratoire), désormais à la SCLE. J'ai apprécié nos innombrables échanges autour de la machine à café, et nos sorties au-delà du cadre professionnel. Je me dois ici de souligner l'aide précieuse qu'il m'a apportée tout au long de ma thèse. Merci. Je souhaite remercier le bureau de l'Association Des Laplaciens (ADeL) de 2019, à savoir Maxime Bafoil, Yazan, Timothé et Laura. Ils m'ont offert une belle expérience humaine dès ma première année de thèse, et plein de crédits pour l'école doctorale (merci encore Maxime). Je voudrais remercier les autres doctorants dont j'ai croisé le chemin, au laboratoire et ailleurs, en particulier Quentin, Lucille, Youssef, Pawel, Matthieu, Abdulrahman, Grégoire, Daouda, Lucas, Corentin.

Je veux de manière générale remercier l'ensemble du groupe M2A, du département Laboratoire des Matériels Electriques (LME) à EDF R&D, basé aux Renardières. De plus, merci à Monsieur Vincent Vernhes, Chef de Groupe à M2A, pour son professionnalisme et pour sa bienveillance. Je remercie Rafael Coelho-Medeiros, doctorant à M2A, pour ces trois années (et 3 mois) de thèse passées ensemble, malgré la distance. Je tiens à remercier "l'équipe montage" pour son travail, en amont de la mise en exploitation du laboratoire, au hall 400 kV. Je souhaite également remercier Bruno et Laurent pour leur accueil dès mes premiers jours aux Renardières, et pour leur gentillesse. Merci à Edouard de m'avoir fait assister à cet essai !

Enfin et surtout, je veux remercier ma famille pour tout ce qu'elle m'a apporté durant cette période. Merci à Andrea pour son soutien indéfectible, et pour ces trois années de thèse communes. Merci.

Abstract

For more than a decade, high-voltage direct-current (HVDC) grid-connection of offshore wind farms has intensified. It allows transporting to the mainland power levels around 1 GW, over underwater distances exceeding 50 kilometres. A key issue related to the sizing of HVDC converter-stations, based on MMC (Modular Multilevel Converters), is their efficiency. Only 0.1% of power losses represents several GWh lost for each year of operation of the wind farm.

These power losses are related to the characteristics of the semiconductors used. Today, the IGBT (Insulated-Gate Bipolar Transistor) is the only semiconductor device used in this type of application. Historically, the IGBT has been developed for medium-power industrial applications, and does not appear as the best candidate to realize HVDC systems. On the other hand, the IGCT (Integrated Gate-Commutated Thyristor) has performances and features that seem better adapted, however no HVDC system has been implemented with IGCTs so far.

The aim of this PhD thesis is to optimize the performances of HVDC converters, based on IGCT, as part of the grid-connection of offshore wind farms. This work has been the subject of a collaboration between the LAPLACE Laboratory in Toulouse, Electricité de France Research & Development (EDF R&D), and the semiconductor manufacturer Hitachi ABB Power Grids, Semiconductors.

In a first approach, the static and dynamic characteristics of the IGCTs have been measured experimentally on a double-pulse test bench. Then, an electro-thermal model has been built, in order to determine precisely the power losses in the hundreds of sub-modules present in an MMC arm. This approach has allowed a comparison of different IGCTs, according to their power losses, taking into account the intermittent production of the offshore wind farm.

Following this study based on calculations and simulations, a test bench in steady-state, consisting of two IGCT-based sub-modules connected in a back-to-back configuration, has been designed and implemented to accurately measure on-state and switching losses through dedicated instrumentation. With a working voltage up to 5 kV and currents exceeding 2 kA, 4.5 kV and 10 kV devices have been tested under operating conditions equivalent to those of a 1 GW HVDC station.

The power loss measurements using the calorimetric method have confirmed the validity of the electro-thermal models related to IGCT and its clamp circuit, with an accuracy of about 10%. The waveforms have highlighted larger deviations regarding the switching losses, caused by the stray inductances of connection within the switching cell. The cross-use of electro-thermal models and experimental measurements demonstrates that 4.5 kV IGCTs can allow a significant rise in the power levels of the MMC-based HVDC stations, while 6.5 kV and 10 kV IGCTs are

the most suitable devices for prospective applications, guided by the voltage upgrade of HVDC cables. Soft switching circuits are promising to reduce the volume of the sub-modules, and would be particularly relevant for 6.5 kV and 10 kV devices, whose switching losses are the main limiting factor.

Résumé de la thèse

Depuis plus d'une dizaine d'années, le raccordement à courant continu haute tension (HVDC) des parcs éoliens en mer s'intensifie. Cela permet de transporter vers le continent des niveaux de puissance avoisinant le GW, sur des distances sous-marines excédant la cinquantaine de kilomètres. Un enjeu clé lié au dimensionnement des stations de conversion HVDC, basées sur des MMC (convertisseurs modulaires multiniveaux), est leur rendement. Rien que 0.1% de pertes représente plusieurs GWh perdus pour chaque année d'exploitation du parc éolien.

Ces pertes sont liées aux caractéristiques des semi-conducteurs utilisés. Aujourd'hui, l'IGBT (transistor bipolaire à grille isolée) est le seul composant utilisé dans ce type d'application. Historiquement, l'IGBT a été développé pour des applications industrielles de moyenne puissance, et ne parait pas a priori bien placé pour réaliser des systèmes HVDC. A contrario, l'IGCT (thyristor intégré commuté par la gâchette) présente quant à lui des performances et des spécificités qui semblent mieux adaptées, néanmoins son usage dans de tels systèmes n'a jamais été considéré.

Le but de cette thèse est d'optimiser le rendement de convertisseurs HVDC à base d'IGCT, dans le cadre du raccordement des parcs éoliens en mer. Ce travail a fait l'objet d'une collaboration entre le Laboratoire LAPLACE à Toulouse, EDF R&D, et le fabricant de semi-conducteurs Hitachi ABB Power Grids, Semiconductors.

Dans un premier temps, les caractéristiques statiques et dynamiques des IGCT ont été relevées expérimentalement sur un banc d'essais impulsionnel. Un modèle électro-thermique a ensuite été élaboré, ceci afin de déterminer avec précision les pertes dans la centaine de sous-modules équipant un bras de MMC. Cette approche a permis de comparer différents IGCT suivant les niveaux de pertes, en prenant en compte l'intermittence de production du parc éolien en mer.

Suite à cette étude basée sur des calculs et des simulations, un banc d'essais en régime permanent, constitué de deux cellules à base d'IGCT mises en opposition, a été conçu et mis en oeuvre afin de mesurer avec précision les pertes en conduction et les pertes par commutation grâce à une instrumentation dédiée. Avec une tension de travail allant jusqu'à 5 kV et des courants dépassant 2 kA, des composants 4.5 kV et 10 kV ont pu été testés dans des conditions de fonctionnement équivalentes à celles d'une station HVDC d'une puissance de 1 GW.

Les mesures de pertes utilisant la méthode calorimétrique ont pu confirmer la validité des modèles électro-thermiques relatifs à IGCT et à son circuit d'aide à la commutation, avec une précision de l'ordre de 10%. Les relevés des formes d'onde ont mis en avant des écarts plus importants concernant les pertes par commutation, causés par les inductances parasites de

connexion au sein de la cellule de commutation. L'utilisation croisée des modèles de pertes et des mesures expérimentales démontre que les IGCT 4.5 kV peuvent permettre une montée en puissance notable des stations HVDC à base de MMC, tandis que les IGCT 6.5 kV et 10 kV sont les plus adaptés pour accompagner la montée en tension des câbles HVDC. Les circuits permettant la commutation douce des composants sont prometteurs afin de réduire le volume des sous-modules, et seraient particulièrement favorables aux composants 6.5 kV et 10 kV, dont les pertes par commutation constituent le principal facteur limitant.

Résumé de la thèse en français

Chapitre 1 : Raccordement des parcs éoliens en mer éloignés et composants semi-conducteurs de puissance

Le premier chapitre présente les technologies actuelles et futures du génie électrique, impliquées dans le raccordement des parcs éoliens en mer dits lointains. L'intérêt du transport en haute tension à courant continu (HVDC) est mis en avant, a contrario de la plupart des réseaux terrestres existants, basés sur la haute tension à courant alternatif (HVAC). La technologie HVDC, plus rentable dès lors que la liaison s'étend typiquement sur plus de 50 km, requiert en contrepartie des stations de conversion.

Pour les stations de conversion en question, les topologies du type "convertisseur source de tension" (VSC) sont mises en avant : elles apportent davantage de flexibilité que les traditionnels ponts à thyristors du point de vue du réseau. Le convertisseur modulaire multiniveaux (MMC), utilisé dans des projets industriels depuis plus d'une dizaine d'années, permet de réduire de manière notable l'encombrement du système, et de réduire dans l'ensemble le coût d'installation de la liaison HVDC. Les performances du MMC, incluant le rendement et la fiabilité, ainsi que les coûts d'investissement (CAPEX) et les coûts d'exploitation (OPEX), sont néanmoins très dépendantes des composants semi-conducteurs de puissance utilisés.

Une étude est donc dédiée à ces semi-conducteurs de puissance. Le composant historiquement utilisé, le thyristor, est introduit, ainsi que sa première déclinaison en composant potentiellement utilisable dans une topologie VSC (le thyristor à extinction par la gâchette, ou thyristor GTO). En parallèle, le développement du transistor bipolaire à grille isolée (IGBT) est présenté, ainsi que ses évolutions afin de répondre aux contraintes de la forte puissance. La genèse du thyristor intégré commuté par la gâchette (IGCT) découle du besoin d'un composant de forte puissance pour les topologies VSC. De ce fait, l'IGCT se veut très performant à basse fréquence de commutation, à fort courant, et peut travailler sous des tensions allant jusqu'à 10 kV.

L'IGCT présente également des propriétés attractives pour le HVDC, notamment sa fiabilité accrue ainsi que son mode de défaillance en court-circuit. Il existe aussi sous forme de composant à conduction inverse, ce qui permet potentiellement d'accroître la compacité de la cellule de commutation.

Le premier chapitre se termine par un bilan des projets de raccordement en HVDC des parcs éoliens, listant les topologies et les technologies utilisées. Cet inventaire montre la prédominance des solutions à base de MMC, avec l'IGBT. Dans le même temps, la montée en puissance attendue de ces liaisons dans les années à venir requiert des calibres en courant et en tension plus importants, que seuls les IGCT sont en mesure de fournir à l'heure actuelle.

Chapitre 2 : Conception de la liaison haute tension à courant continu (HVDC)

Le deuxième chapitre se concentre sur la conception des stations de conversion HVDC, en intégrant les problématiques liées à la gestion des défauts à l'échelle du convertisseur et de la liaison HVDC. L'utilisation de l'IGCT, en remplacement de l'IGBT, permet d'alléger les sous-modules composant le MMC, grâce à une stratégie de protection alternative en cas de défaut côté DC. En remplacement du circuit d'aide à la commutation traditionnel, dissipant de la puissance, plusieurs autres circuits sont étudiés. Le circuit auxiliaire résonant à pôle commuté (ARCP) apparaît comme prometteur, il permet d'effectuer de la commutation douce avec un petit nombre de composants. Cela induit une réduction des pertes par commutation, ainsi qu'une diminution du volume des composants passifs.

Le dimensionnement des MMC au sein des stations de conversion HVDC constitue un enjeu important. En particulier, les composants passifs influent de manière significative sur le volume (condensateurs), mais également sur l'aire de fonctionnement du convertisseur, sur sa stabilité, ainsi que sur son comportement en cas de défaut (inductances de bras). Le nombre de sous-modules par bras dépend quant à lui du calibre en tension des semi-conducteurs utilisés, et de la tension de la liaison HVDC. La tension nominale des sous-modules, V_{SM}, est définie pour des IGCT 4.5 kV, 6.5 kV, et 10 kV, en prenant en considération l'influence du rayonnement cosmique ainsi que la température de jonction en fonctionnement.

Afin de valider la cohérence des choix effectués, le cas d'un court-circuit franc entre pôles côté DC est simulé, à l'aide d'un modèle complet de la liaison HVDC sous PLECS. En plus des disjoncteurs AC classiquement utilisés, des disjoncteurs DC dits "hybrides" (parties mécanique et statique) sont considérés. Les simulations montrent que les disjoncteurs AC seuls, lents, induisent des courants de défaut pouvant détruire les modules de puissance IGBT traditionnels ainsi que les IGCT à conduction inverse, en l'absence de protections complémentaires au sein des sous-modules. Les IGCT asymétriques, couplés à des diodes discrètes, sont idéaux dans ce cas de figure, afin de simplifier le sous-module. Au contraire, les disjoncteurs DC possèdent une action rapide, de l'ordre de quelques millisecondes. Il en résulte des courants de défaut réduits, et la possibilité d'utiliser des IGCT à conduction inverse, ou des modules de puissance IGBT, avec un degré d'intégration plus important.

La dernière partie du chapitre se concentre sur la commande du MMC, en intégrant les contraintes liées au HVDC. Le nombre de niveaux important, combiné au besoin de réduire les pertes par commutation des composants semi-conducteurs, conduit à favoriser une commande dite NLC (Nearest-Level Control en anglais). A la NLC s'ajoute un algorithme de tri, chargé d'équilibrer les tensions des centaines de sous-modules de chaque bras, à chaque instant. Dans le cadre de la thèse, un nouvel algorithme de tri, faisant l'objet d'un dépôt de brevet à l'écriture de ces lignes, a été développé afin de faciliter une étude paramétrique. Il permet notamment d'ajuster automatiquement la fréquence de commutation lorsque les conditions de fonctionnement du convertisseur varient.

Chapitre 3 : Modélisation électro-thermique du convertisseur modulaire multiniveaux (MMC) pour le transport haute tension à courant continu (HVDC)

Le troisième chapitre aborde, avec une approche déductive, la modélisation des stations de conversion HVDC, en vue d'évaluer les pertes des semi-conducteurs de puissance. Un des objectifs clés est de conserver un fort caractère paramétrique, en réduisant le temps de calcul autant que possible. La dépendance thermique, souvent négligée dans la littérature, est intégrée dans

l'étude et fait l'objet de multiples discussions.

Le point de départ est le modèle complet, dit détaillé, du MMC : il intègre plusieurs milliers de composants discrets. Il est démontré qu'un modèle dit moyenné est plus pertinent pour évaluer les pertes en régime permanent, les formes d'ondes sont reproduites avec précision et le temps de calcul est réduit d'un facteur 40 000.

Afin de correctement représenter le couplage électro-thermique impliqué dans l'évaluation des pertes, une série de mesures sur banc d'essai impulsionnel a été effectuée. De multiples IGCT ont ainsi été caractérisés, par Hitachi ABB Power Grids, pour différents courants, tensions et températures de jonction. Ces caractérisations ont permis de constituer des tables de correspondances ("look-up tables" en anglais), facilement exploitables par des logiciels de simulation comme PLECS. Le concept de "bras extérieur" a été introduit : ce dernier est obligatoire afin d'évaluer les pertes, en complément du modèle moyenné. Pour finir, une nouvelle méthode d'évaluation des pertes dans le circuit d'aide à la commutation a été proposée. En se basant sur les formes d'ondes à la commutation, il est possible d'évaluer de manière théoriquement précise les pertes dans la résistance du circuit en question.

Le modèle conçu souffrait de lacunes sous PLECS, notamment en termes de temps de calcul et de représentation du circuit thermique. Les fonctions liées au modèle moyenné et au "bras extérieur" ont donc été analytiquement implémentées sous MATLAB, afin d'accélérer les calculs. L'outil de simulation développé comprend le chargement des tables de correspondances précédemment établies, permettant de calculer les pertes dans les semi-conducteurs et dans les circuits d'aide à la commutation. Cette transition de PLECS vers MATLAB a également permis d'intégrer un modèle thermique plus précis des IGCT à conduction inverse.

L'outil de simulation mène à l'obtention des résultats voulus 40 fois plus rapidement qu'avec le modèle précédent, soit 30 secondes en moyenne avec un ordinateur de bureau. Les températures de jonction de l'ensemble des semi-conducteurs du convertisseur en régime permanent sont calculées, pour tout point de fonctionnement accessible. Ces développements ouvrent la voie à une étude paramétrique, car l'ensemble des paramètres électriques définissant la liaison HVDC peuvent être modifiés. Dans le même temps, l'influence de grandeurs telles que la température de l'eau de refroidissement, ou le débit d'eau, peut être étudiée. Cette fonctionnalité permet de faire l'interface entre le dimensionnement électrique du convertisseur et le dimensionnement du système de refroidissement de la station de conversion HVDC.

Chapitre 4 : Analyse des pertes dans les stations de conversion HVDC

Le quatrième chapitre repose sur les modèles développés dans le troisième chapitre, et utilise les principes de dimensionnement des stations de conversion HVDC du deuxième chapitre. Il y est expliqué que la production d'énergie éolienne est intermittente, puisque la vitesse du vent varie suivant les conditions météorologiques. Cela induit un calcul des pertes non trivial, il est alors proposé de considérer l'ensemble des points de fonctionnement induits par les différentes vitesses de vent, en intégrant les propriétés des turbines éoliennes. Pour cela, une distribution statistique typique des vitesses de vent est considérée. Le calcul des pertes dites "moyennées" est présenté : il s'agit des pertes moyennes observées dans les stations de conversion HVDC, avec une durée de fonctionnement suffisamment longue pour qu'une approche statistique soit applicable.

Une première étude comparative est menée entre les composants semi-conducteurs, à tension côté DC fixée à ± 320 kV. Cette étude montre que les contraintes thermiques sont croissantes avec l'augmentation du calibre en tension des IGCT. L'épaisseur de silicium requise augmente

avec le calibre en tension du composant, ce qui accroît à la fois les pertes en conduction et les pertes par commutation. Ainsi, la température de jonction des IGCT 10 kV dépasse la valeur admissible pour les points de fonctionnement critiques. Les IGCT à conduction inverse 4.5 kV et 6.5 kV s'avèrent quant à eux très performants, ils n'impliquent qu'une faible augmentation des pertes pour un gain significatif en termes de volume, et de coûts d'investissement (CAPEX), par rapport aux IGCT asymétriques 4.5 kV.

En complément de cette étude, une seconde étude comparative est menée à puissance constante et à nombre de sous-modules dans le convertisseur constant. Cela implique que la tension de la liaison HVDC augmente avec le calibre en tension des semi-conducteurs de puissance. Cette approche est pertinente, car elle permet d'envisager l'évolution des stations de conversion HVDC avec des câbles à isolation synthétique (XLPE) 525 kV et 600 kV, qui possèdent à l'heure actuelle des niveaux de maturité technologique (TRL) plus bas que les câbles XLPE 320 kV. Cette seconde étude comparative montre que les IGCT haute tension, c'est-à-dire avec des calibres en tension de 6.5 kV et 10 kV, permettent de réduire les pertes dans les stations de conversion HVDC jusqu'à 10%. Cela montre qu'il est possible de monter la tension de la liaison HVDC, et d'augmenter le rendement de l'installation, tout en évitant d'augmenter le nombre de sous-modules dans les stations de conversion. Cette conclusion est importante, car c'est actuellement un facteur contraignant lors de la conception des stations de conversion HVDC.

La seconde étude comparative met en exergue l'importance des pertes par commutation des IGCT haute tension, ainsi que la part croissante des pertes liées au circuit d'aide à la commutation. Elle fait donc écho à l'étude du deuxième chapitre, portant sur les circuits auxiliaires pour l'IGCT. L'ARCP, permettant de réduire les pertes par commutation des semi-conducteurs sans dissiper d'énergie, présente alors un potentiel accru aux yeux des résultats du quatrième chapitre.

Chapitre 5 : Réalisation et test de sous-modules à base de thyristors intégrés commutés par la gâchette (IGCT)

Le but du cinquième chapitre est d'obvier à l'absence de validation expérimentale concernant les résultats du quatrième chapitre. Bien que basés sur des caractérisations expérimentales, les modèles multi-physiques du troisième chapitre reposent sur des hypothèses qui n'ont, jusqu'à ce stade, pas été vérifiées. Reproduire les conditions de fonctionnement des semi-conducteurs de puissance dans un convertisseur 1 GW est a priori complexe et onéreux, à l'échelle d'un laboratoire. Pour pallier cette difficulté, une topologie utilisant le principe de mise en opposition a été considérée : deux sous-modules identiques sont raccordés sur le même bus DC. Une inductance, connectée aux sorties des sous-modules, permet d'assurer une circulation de l'énergie au sein des deux cellules de commutation. De ce fait, une alimentation DC ne fournissant que les pertes du montage est suffisante, ce qui correspond à seulement quelques dizaines de kilowatts.

Le banc d'essais a été conçu pour tester des composants semi-conducteurs de puissance allant de 4.5 kV à 10 kV, c'est-à-dire que la tension maximale nécessaire sur le bus DC est de 5 kV. Par équivalence avec le dimensionnement du deuxième chapitre, des courants maximum supérieurs à 2 kA sont attendus en sortie, pour des valeurs efficaces allant jusqu'à 1200 A. Le système de refroidissement, à eau désionisée, est instrumenté afin de mettre en oeuvre une méthode calorimétrique, permettant de déterminer la puissance évacuée par chaque plaque à eau du montage. Des sondes de tension et de courant spécifiques ont été prévues afin d'observer les commutations des IGCT et des diodes, puis de calculer les pertes associées. Les cellules de commutation sont contrôlées par une "Boombox", ce système permet d'implémenter les lois de commande du banc d'essais grâce à une interface MATLAB/SIMULINK, et de facilement

analyser les signaux d'entrée/sortie.

Dans un premier temps, ce sont des composants asymétriques 4.5 kV qui ont été testés. Les résultats expérimentaux ont été comparés aux modèles théoriques, pour un courant de sortie continu, afin de permettre la séparation des pertes en conduction et des pertes par commutation. Il a été observé que les pertes en commutation sont plus faibles que prévu. Cet écart, d'environ 25% pour les diodes et d'environ 15% pour les IGCT, s'explique par les inductances parasites du montage, qui diffèrent du montage où les premiers relevés ont été effectués. L'estimation des pertes en conduction est des pertes dans le circuit d'aide à la commutation s'est révélée précise, avec une erreur relative de l'ordre de 10%. D'après les simulations, pour une température ambiante de 25°C, la température de jonction des semi-conducteurs testés n'a pas dépassé 70°C. Cela démontre que les composants asymétriques 4.5 kV choisis sont des solutions viables, mais également qu'ils sont sollicités bien en-dessous de leur capacité maximale en courant.

La seconde série d'essais a porté sur des IGCT à conduction inverse (RC-IGCT) 10 kV. Ces RC-IGCT peuvent opérer à une tension nominale de 4700 V; une fréquence de commutation maximale de 150 Hz a été fixée afin de limiter l'influence des pertes par commutation. Le fonctionnement de ces interrupteurs a été testé pour des courants maximum dépassant 1 kA, et des courants efficaces dépassant 500 A, où la forme d'onde d'un courant de bras de MMC a été reproduite aussi fidèlement que possible. La dynamique lors des commutations s'est révélée suffisante pour que ces IGCT soient utilisés dans les stations de conversion étudiées dans le deuxième chapitre. Les modèles électro-thermiques de pertes se sont avérés aussi précis que pour les composants 4.5 kV, démontrant ainsi leur validité pour une large gamme de paramètres. L'étude de la répartition des pertes montre que la réduction de l'inductance de limitation de di/dt, L_{cl}, permet de réduire les pertes totales du sous-module. Des circuits permettant la commutation douce seraient donc particulièrement avantageux pour les RC-IGCT 10 kV : ils offriraient une réduction conséquente des pertes pour un volume similaire, voire moins important.

Conclusion et perspectives

Cette thèse de doctorat a montré, en se concentrant sur les stations de conversion HVDC et sur les semi-conducteurs de puissance qu'elles contiennent, que des solutions technologiques efficaces et prometteuses existent pour raccorder les parcs éoliens en mer lointains au réseau terrestre. L'IGCT anticipe la tendance actuelle, où les puissances transmises et les tensions de raccordement augmentent, tout en offrant un niveau de pertes réduit. Ces caractéristiques favorisent la réduction progressive du coût moyen de l'énergie (LCOE en anglais) éolienne en mer, ce qui est primordial pour accroître la production d'électricité à base d'énergies renouvelables.

Un état de l'art a été présenté, afin de comprendre les principales thématiques gravitant autour du raccordement des parcs éoliens en mer lointains. Parmi les convertisseurs statiques pour le HVDC, la technologie VSC est apparue comme une solution pertinente. En particulier, le MMC offre de nombreuses caractéristiques pour faciliter le développement des liaisons HVDC dans les zones éloignées ou isolées. L'IGCT présente des performances et des propriétés intéressantes dans le domaine du HVDC : avec des tensions allant jusqu'à 10 kV et des diamètres de wafer entre 4 et 6 pouces, il dépasse les capacités en courant et en tension de l'IGBT.

La conception de la liaison HVDC a été traitée, incluant les deux stations de conversion et les sous-modules qu'elles contiennent. Avec l'IGCT, la stratégie de protection d'un sous-module peut être simplifiée, notamment grâce à son mode de défaillance naturel en court-circuit et à son inductance de limitation de di/dt. L'ARCP, qui vise à remplacer le snubber RCD, est un circuit de commutation douce prometteur avec un volume réduit et une faible complexité. En ce qui concerne la commande du MMC, la NLC est plus appropriée que la MLI (modulation de

la largeur d'impulsion) en raison de la largeur d'impulsion minimale qu'elle garantit pour tous les sous-modules. En outre, elle offre davantage de flexibilité pour adapter dynamiquement la fréquence de commutation, et la possibilité de réduire les pertes par commutation grâce à des algorithmes de tri dédiés.

En tenant compte des grandeurs électriques et des propriétés du circuit de refroidissement, un modèle de pertes des composants semi-conducteurs a été proposé. Les étapes successives de simplification du modèle du MMC ont été présentées, orientées vers une réduction du temps de calcul. Une nouvelle approche pour estimer les pertes du snubber RCD a été introduite. Les différents modèles ont été rassemblés dans un outil de simulation unique, mis en oeuvre avec MATLAB. L'outil est capable de fournir toutes les variables de l'espace d'état du convertisseur, y compris les pertes et les températures de jonction de tous les semi-conducteurs, en 30 secondes depuis un ordinateur de bureau.

Une analyse des pertes dans les stations de conversion HVDC a été réalisée, en tenant compte de la production d'énergie intermittente des parcs éoliens en mer. Les IGCT asymétriques 4.5 kV ont montré des pertes et des contraintes thermiques réduites. Les RC-IGCT se sont révélés être un compromis intéressant en termes de rendement, de volume et de coût. Les IGCT 6.5 kV et 10 kV présentent un avantage certain, car ils permettent de réduire le nombre de sous-modules dans les stations de conversion, même si leur potentiel est limité par les pertes par commutation et les pertes du snubber RCD.

Pour finir, une validation expérimentale des modèles électro-thermiques de pertes a été considérée. La tenue en courant des IGCT 4.5 kV, importante, a été confirmée, pour une large plage de fonctionnement, propre aux stations de conversion HVDC. Les pertes ont été mesurées à l'aide de différents instruments et de différentes méthodes. En outre, des protocoles d'étalonnage ont été réalisés pour garantir la précision des résultats. Les erreurs de modélisation concernant les pertes par commutation ont été évaluées, les principaux facteurs les influençant ont été identifiés pour l'IGCT et pour la diode. La précision des modèles de pertes a été validée pour différentes tensions, courants, fréquences de commutation, et une température de jonction variable, en régime permanent. Les RC-IGCTs 10 kV ont dévoilé d'importantes pertes, mais une aire de fonctionnement suffisante pour travailler sous une tension nominale de 4700 V, une fréquence de commutation de 150 Hz, et des courants supérieurs à 500 A_{rms}/1 000 A_{peak}.

Plusieurs axes de recherche ont été mis en lumière pour améliorer les performances des sous-modules de MMC. En ce qui concerne le rendement et le volume, la réduction de l'inductance limitant le di/dt est bénéfique : les diodes supportant un di/dt élevé, c'est-à-dire supérieur à 5 kA/μs, sont pertinentes avec l'IGCT. De telles diodes existent déjà en tant que composants discrets, mais leur intégration dans un RC-IGCT contribuerait encore plus à améliorer la compacité du sous-module.

En ce qui concerne les IGCT dits "haute tension", les pertes par commutation et les pertes du snubber RCD contribuent de manière significative aux pertes totales. De plus, l'ARCP étudié est apparu comme une alternative potentielle au snubber RCD traditionnel. Pour un volume et une fiabilité similaires, les pertes par commutation peuvent donc être considérablement réduites, et les pertes du circuit d'aide à la commutation n'existeraient plus avec l'ARCP. Par conséquent, il serait intéressant de tester l'ARCP avec des IGCT 6.5 kV et 10 kV, afin de comparer les deux solutions techniques, et de conclure quant au potentiel des circuits de commutation douce avec des IGCT haute tension.

Les contraintes de volume n'ont pas été prises en compte, puisque les sous-modules assem-

blés ont été spécialement conçus pour la mesure de pertes et les tests en laboratoire, avec la possibilité d'être reconfigurés. La conception d'un sous-module à base d'IGCT, orientée vers des applications industrielles, pourrait dévoiler des avantages supplémentaires par rapport à l'IGBT.

List of specific acronyms

A-IGCT	Asymmetric IGCT
AAC	Alternate Arm Converter
ACCB	AC Circuit-Breaker
ARCP	Auxiliary Resonant Commutated Pole
AVM	Averaged Model
CCSC	Circulating Current Suppression Controller
DCCB	DC Circuit-Breaker
DM	Detailed Model
FIT	Failure In Time
HB	Half-Bridge
ICCT	Internal Current Commutation Time
IEGT	Injection-Enhanced Gate Transistor
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
LCC	Line-Commutated Converter
LCOE	Levelized Cost Of Energy
MMC	Modular Multilevel Converter
MTBF	Mean Time Between Failures
MTTF	Mean Time To Failure
NLC	Nearest-Level Control
PPI	Press-Pack IGBT
PSC-PWM	Phase-Shifted Carrier PWM
RC-IGCT	Reverse-Conducting IGCT
SiC	Silicon Carbide
SCFM	Short-Circuit Failure Mode
SM	Sub-Module (elementary brick of a MMC)
SOA	Safe Operating Area
TIV	Transient Interruption Voltage
TSO	Transmission System Operator
WTG	Wind Turbine Generator
XLPE	Cross-Linked Polyethylene Extruded

Table of contents

General introduction **21**

1 Grid-connection of wind parks and semiconductors **23**
1.1 HVDC systems for grid-connection of offshore wind parks 23
1.1.1 Advantages of HVDC over HVAC for cable power transmission 23
1.1.2 HVDC configurations for grid connection of offshore wind parks 25
1.1.3 Grid codes for offshore wind parks 27
1.2 Power converters for HVDC power transmission 28
1.2.1 Line-Commutated Converter (LCC) 28
1.2.2 Two-level Voltage-Source Inverter 28
1.2.3 Modular Multilevel Converter (MMC) 29
1.2.4 Alternate Arm Converter (AAC) 31
1.3 Semiconductor devices for HVDC power transmission 32
1.3.1 Overview of the semiconductor devices for HVDC power transmission . . 32
1.3.2 Other relevant turn-off devices for present and futures applications 38
1.3.3 Integrated Gate-Commutated Thyristor (IGCT) 38
1.4 Existing HVDC systems connecting offshore wind-farms 44
1.4.1 Overview of the existing projects 44
1.4.2 Incoming HVDC projects in Europe 44
1.5 Future trends and conclusions 45

2 Design of the HVDC link **47**
2.1 Design of the IGCT-based sub-modules 47
2.1.1 Selection of the topology 47
2.1.2 Sub-module failure, protection and redundancies 48
2.1.3 Auxiliary circuits for IGCT 49
2.2 Design of the converters 55
2.2.1 Selection of the passive components in an HVDC-MMC 55
2.2.2 Choice of the number of sub-modules per arm 57
2.3 Behaviour of the HVDC link during faulty operation 59
2.3.1 Circuit-breakers and HVDC cables 59
2.3.2 Comparison between ACCBs and DCCBs in case of DC fault 62
2.3.3 Influence of the DCCB's Internal Current Commutation Time (ICCT) . . 65
2.4 Control of the converters 67
2.4.1 Inner control loops 67
2.4.2 Multilevel modulation strategy 69
2.5 Conclusion 72

3 Electro-thermal modelling of the HVDC-MMC 73
3.1 Electrical model of the MMC . . . 73
3.1.1 Detailed model (DM) . . . 73
3.1.2 Averaged model (AVM) . . . 75
3.1.3 Comparison between the DM and the AVM . . . 76
3.2 Electro-thermal model of the sub-modules . . . 78
3.2.1 Measurement of the semiconductors' characteristics . . . 78
3.2.2 Electro-thermal models for the semiconductors . . . 80
3.2.3 External arm for power-loss calculation . . . 83
3.2.4 Clamp circuit and di/dt snubber . . . 84
3.3 Implementation of the model with MATLAB . . . 88
3.3.1 Motivations . . . 88
3.3.2 Simplification of the AVM with analytic expressions . . . 88
3.3.3 Structure of the simulation tool . . . 88
3.3.4 Performances and validation of the simulation tool . . . 90
3.3.5 Conclusions regarding the simulation tool implemented with MATLAB . 94
3.4 Conclusion . . . 94

4 Power-loss analysis in the HVDC converter-stations 97
4.1 Modelling of the offshore wind park . . . 97
4.1.1 Problematic, approach . . . 97
4.1.2 Statistical distribution of the wind-speeds . . . 97
4.1.3 Wind turbine power curve . . . 98
4.1.4 Calculation of the averaged power losses . . . 98
4.1.5 Parameters of the converter-stations . . . 99
4.2 Power losses of the HVDC stations, V_{DC} fixed . . . 100
4.2.1 10 kV IGCTs . . . 100
4.2.2 4.5 kV IGCTs . . . 102
4.2.3 6.5 kV RC-IGCT . . . 104
4.2.4 Summary for constant voltage, V_{DC}=±320 kV . . . 104
4.3 Power losses of the HVDC stations, N=256 sub-modules fixed . . . 106
4.3.1 6.5 kV RC-IGCT . . . 107
4.3.2 10 kV IGCTs . . . 107
4.3.3 Summary for constant number of SMs, N = 256 . . . 108
4.4 Comparison with other semiconductors, V_{DC} fixed . . . 110
4.4.1 Context and limits . . . 110
4.4.2 Results . . . 110
4.4.3 Conclusions . . . 111
4.5 Conclusion of the power-loss analysis . . . 111

5 Realization and testing of IGCT-based sub-modules 113
5.1 Design of the test bench . . . 113
5.1.1 Constraints, topology and electrical ratings . . . 113
5.1.2 Measurements . . . 120
5.1.3 Control and protections . . . 122
5.1.4 Overview of the test bench . . . 123
5.2 Power-loss analysis with the 4.5 kV A-IGCTs . . . 123
5.2.1 DC output current . . . 125
5.2.2 Calibration of the thermal measurements - semiconductor power losses . . 134
5.2.3 MMC-like output current . . . 136
5.3 Power-loss analysis with the 10 kV RC-IGCTs . . . 138
5.3.1 DC output current . . . 139

5.3.2 MMC-like output current 142
5.4 Conclusion of the experiments 146

Conclusion and outlook **147**

Bibliography **149**

A Analytic expressions of the electrical waveforms **161**
A.1 Arm-voltage $v_u(t)$ 161
A.2 DC link current I_{DC} 162
A.3 Arm-energy $E_{cu}(t)$ 162
A.4 Average sum capacitor-voltage v_{cu0} 163
A.5 Reference arm-voltage $v^*_u(t)$ 164

B Thermal model of PPI, BIGT and IEGT **165**
B.1 Press-pack IGBT 165
B.2 Bi-mode IGBT 165
B.3 Injection-enhanced gate transistor 166

C Instruments, sensors and probes of the test bench **167**

General introduction

Climate imbalance has been a major concern for the last decades, due to human activity and more specifically to the emission of greenhouse gases. Among them, electricity production is regularly pointed out as one of the main sources of carbon dioxide emissions, 31% over the last three decades in the case of the USA, according to the Environmental Protection Agency (EPA). Politically, a step forward has been made to banish fossil fuels from electricity production as much as possible: the European Union plans to install a capacity of 60 GW offshore wind by 2030 [1], whereas the USA targets 110 GW by 2050 [2].

Offshore wind power is especially interesting for many reasons, first of all offshore areas benefit from more important wind-speeds than onshore areas [3][4]. Moreover, it is estimated that the effective available offshore area in Europe could provide about 78% of the total electricity demand in 2030 [5], thanks to wind power. This huge potential of production could drive the energy transition at the scale of a continent.

The distance of a wind-farm to the shore is a key factor: remote offshore areas are larger and they are supposed to provide higher wind-speeds, thus enhancing energy production. Furthermore, the visual impact, often source of critics for wind parks installed close to the shore, could be avoided. In practice, the distance to the shore is limited by the water depth: 60 m is the current maximum, due to the wind turbine foundations [6]. In the meantime, floating wind turbines are emerging, promising the removal of the water depth barrier [7].

The massive offshore energy production, typically up to 1 GW, requires high-voltage direct current (HVDC) transmission to reduce costs; this technology relies on power converters and semiconductor devices. The main concern regarding the whole system is the Levelized Cost Of Energy (LCOE), i.e. the cost of the electricity effectively produced, and averaged over the total duration of operation, as expressed in (1):

$$LCOE = \frac{\text{OPEX+CAPEX}}{\text{raw energy production - energy loss}} \tag{1}$$

In Europe, LCOE tends to decrease with the rising maturity of the projects, and their associated technologies [8]. The denominator shows that energy loss is a factor which contributes to increase LCOE. Consequently, the efficiency of the conversion system is a critical issue: even with a typical efficiency of 99% per converter-station, the remaining 1% of power losses represent 175 GWh of energy loss per year for the two converter-stations, i.e 8.7 M€ per year for an average electricity price of 50€/MWh.

Nowadays, converter-stations are based on modular multilevel converters (MMCs), using thousands of insulated-gate bipolar transistors (IGBT) due to the large number of levels. Then, IGBT's characteristics are of paramount importance to ensure system's availability, reliability

and minimum power losses. Historically, IGBT was a medium power device: it has been introduced in the field of HVDC at the end of the 1990s. A new device was emerging during the same period, the integrated gate-commutated thyristor (IGCT). IGCT, an evolution of the Gate Turn-Off thyristor (GTO), benefits from the advantages of thyristor and the turn-off capability of IGBT, with potential benefits in terms of voltage and current ratings, reliability and cost compared to IGBT. For this reason, the use of this device for MMC-HVDC applications is seriously considered.

This PhD thesis has been carried out at the Laboratoire Plasma et Conversion d'énergie (LAPLACE Laboratory) in the Power Converter research group, Toulouse, and at Electricité de France Recherche et Développement (EDF R&D), Les Renardières. A partnership has been made from the beginning of the thesis with Hitachi ABB Power Grids, Semiconductors, to study the applications of IGCT in the field of high-voltage power transmission.

The estimation of the semiconductor power losses is necessary to carry out a relevant study on IGCT in MMC-HVDC applications. Nevertheless, the implementation of fast and accurate simulation models is complex due to the large number of components in a converter-station. Furthermore, the electro-thermal coupling inherent to semiconductor's operation must be considered, since the packaging of the device and the characteristics of the cooling circuit influence the efficiency of the converter-station.

Then, this PhD thesis focuses on the assessment of the potential of new IGCTs for grid connection of remote offshore wind parks, considering the intermittent power production. It aims at studying the main features of IGCTs for HVDC, but also their influence on the converter-stations' design. Despite the high level of power of these systems, an experimental approach has been proposed to validate the results obtained with the proposed models. Using the opposition method, the behaviour of IGCT in steady-state, going through the same electrical and thermal stresses as in a real converter-station, has been investigated.

The dissertation has been divided into five chapters: the first chapter presents a state of the art of HVDC technology dedicated to offshore wind-parks, HVDC power converters and high power semiconductor devices. The second chapter deals with the design of the converter-stations for offshore wind applications, including protection aspects from the sub-module to the whole HVDC link.

The third chapter presents the approach to model a MMC sub-module, including electrical and thermal dependencies, to end up with the implementation of a complete simulation tool, fast enough to consider a large number of operating conditions. The fourth chapter is about the power-loss analysis in the two converter-stations of the HVDC link, connecting an offshore wind park, based on the models of the third chapter. Different parametric studies are carried out to compare IGCTs with different voltage ratings, which unavoidably modifies the converter-stations' design. Following the power-loss analysis, potential applications for the different IGCTs are proposed.

The fifth and last chapter focuses on the experimental realization of two IGCT-based sub-modules for MMC, connected in a back-to-back configuration. The power losses are measured with a dedicated instrumentation, allowing a comparison with the power-loss models of the third chapter. Waveforms at the scale of commutation were recorded for different currents, voltages, switching frequencies and different di/dt chokes. Two series of semiconductor devices have been tested, 4.5 kV asymmetric IGCTs with free-wheeling diodes and 10 kV reverse-conducting IGCTs, in realistic steady-state operating conditions.

Chapter 1

Grid-connection of remote offshore wind parks and high-power semiconductor devices

This chapter proposes a state of the art of HVDC technologies for cable power transmission, which aims at understanding the benefits and the constraints related to such systems. Then, power converters for HVDC power transmission and high-power semiconductor devices are introduced. A list of the existing projects of HVDC offshore systems has been established in the end of this chapter.

1.1 HVDC systems for grid-connection of offshore wind parks

1.1.1 Advantages of HVDC over HVAC for cable power transmission

1.1.1.1 Transmission capacity

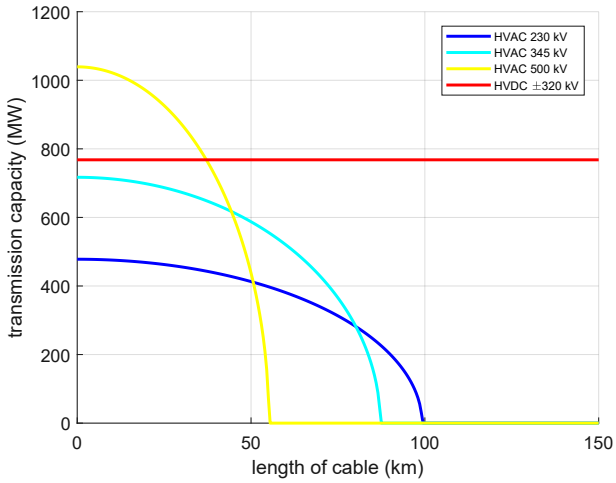


Figure 1.1: Cable transmission capacity for HVAC and HVDC with $I_{cable,\ max}$=1200 A

HVAC power transmission has historically spread worldwide. However, it has an unavoidable drawback: cables generate reactive power. Besides, this phenomenon is amplified with the transmission distance. In the case of cable power transmission, the cables generate a significant amount of reactive power, due to the parasitic capacitance between the core and the earthed

screen, which increases the Root Mean Square (RMS) currents flowing in them [9]. Considering the thermal limit of the cables, the rise in the transmission distance implies a reduction of the transmission capacity [10]. In order to increase the transmission distance, solutions such as passive reactive power compensation or Flexible AC Transmission Systems (FACTS) can be employed [11]. As a consequence, the transmission distance is a key parameter to consider during the design of HVAC systems.

On the other hand, there is no reactive power involved with DC power transmission, so the transmission capacity is constant with the transmission distance. Figure 1.1 presents the typical evolution of the cable transmission capacity with the length of the cable, it can be observed that HVAC power transmission is seriously penalized beyond 50 km, where capacitive effects are dominant. Consequently, HVDC is an attractive solution for high-power transmission over long distances, either with overheads lines or underground/submarine cables.

1.1.1.2 Technologies of submarine cables

Another important aspect related to power transmission is the technology of the cables. Because of their length and the laying engineering works, they have a consequent influence on the cost of the system.

Mass-impregnated cables Mass-impregnated cables have been used since 1895 in the field of high-voltage systems, with a first application for an HVDC system in 1954 for Gotland I [12]. Its insulation lies in a paper impregnated with a high-viscosity oil, which has proven to be reliable over the past sixty years for HVDC systems. For submarine applications, they also include a steel armour for better mechanical performances. Nowadays, mass-impregnated cables with voltage ratings up to 600 kV and current ratings up to 1800 A are available in Europe [13], leading to a maximum power rating of 2.2 GW per end-station. This technology, though well-established, suffers from some limits such as its weight, in a range of 40-60 kg/m for submarine applications.

Cross-Linked Polyethylene Extruded (XLPE) HVDC cables Cross-Linked Polyethylene Extruded (XLPE) HVDC cables have been used for the first time in the Cross-Sound Cable project in 2002 [14], with a voltage rating of 150 kV. This technology is much more recent than mass-impregnated cables in the field of HVDC. An important constraint is that they do not support regular polarity reversal: as a consequence, they are generally not compatible with Current-Source Converters (CSCs). On the other hand, they are suitable for connecting Voltage-Source Converter (VSCs). XLPE insulation leads to lighter cables due to a higher compactness, in a range of 20-35 kg/m [15]. Nevertheless, it remains limited in terms of voltage rating, 320 kV is the maximum for industrialized solutions in the moment [10]. Two times lighter than mass-impregnated cables, it is reported than XLPE cables are also cheaper than mass-impregnated cables [14] in terms of manufacturing, and easier to install [10]. Consequently, they embody a key technology for the development of HVDC offshore converter-stations.

525 kV XLPE cables, already developed by some manufacturers [16][17], must be used in prospective HVDC projects, as they contribute to increase the transmission capacity of the link. A further reduction of manufacturing and installation costs at the scale of the whole system is expected [18]. 600 kV and 640 kV XLPE cables have also been reported [19][20] and are the next milestone.

1.1.1.3 Investments costs for HVAC and HVDC offshore power transmission

The observations made in 1.1.1.1 and 1.1.1.2 have pointed out that HVDC is clearly favoured when the cable transmission distance increases. Regarding costs, Figure 1.2 presents the typical trade-off in the field of power transmission:

- The cost of HVDC converter-stations is the highest due to the power electronics systems, which makes HVAC power transmission the cheapest for small transmission distances.
- The cost of HVAC power transmission increases faster than with HVDC power transmission. HVAC cables are penalized by the need of three circuits, instead of two circuits compared with HVDC.

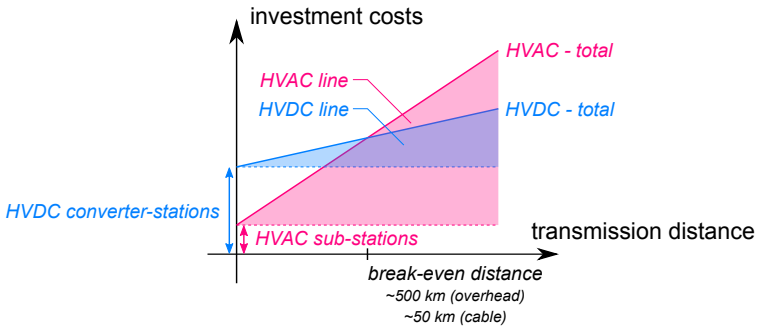


Figure 1.2: Relation between cost and distance for high-voltage AC and DC transmission

A so-called critical distance, or break-even distance, is defined as the distance when investment costs are identical for HVDC and HVAC power transmission. Break-even distances between 50 km and 80 km are reported in the literature [9][21][22], for cable power transmission. It explains why HVAC power transmission is preferred when offshore wind-farms are close to the coast, whereas remote offshore wind-farms are most preferably connected using HVDC power transmission, as in the case of many German projects [23].

1.1.2 HVDC configurations for grid connection of offshore wind parks

1.1.2.1 Connection from the wind turbine generators to the onshore AC grid

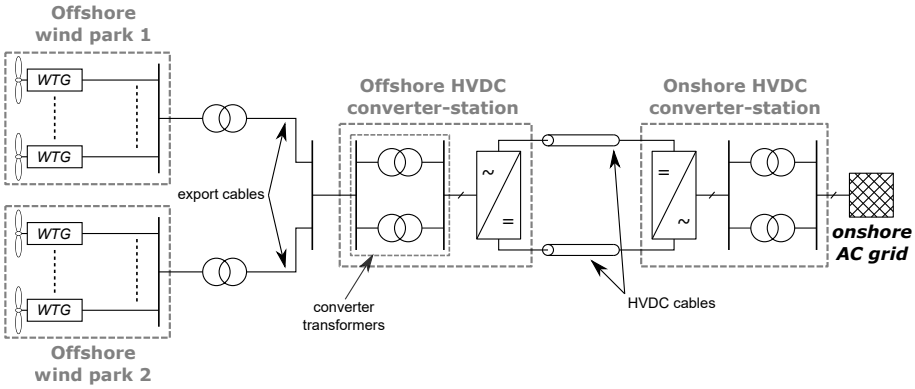


Figure 1.3: Schematic representation of an HVDC grid connection system for offshore wind parks

Figure 1.3 shows a classic configuration to connect one or more wind parks, each composed of several WTGs, to the onshore AC grid [22]. WTGs typically supply power through a 66 kV AC inter-array cable network [6], then the collector networks are connected to collector platforms to step-up the AC voltage, between 132 kV and 220 kV (variable) [6], 155 kV in the case of TenneT (the transmission system operator in Germany and the Netherlands) [24]. Within the offshore HVDC converter-station, the converter transformers increase the AC voltage to reach the nominal input voltage of the rectifier [25]. The offshore converter-station, operating as a rectifier, is connected to HVDC cables ensuring the connection to the onshore HVDC converter-station. The number and the arrangement of collector platforms is chosen to minimize costs, leading to many investigations such as the direct removal of these collector platforms [26], or the use of a DC inter-array collector grid [27][28].

1.1.2.2 Configuration of the main HVDC link

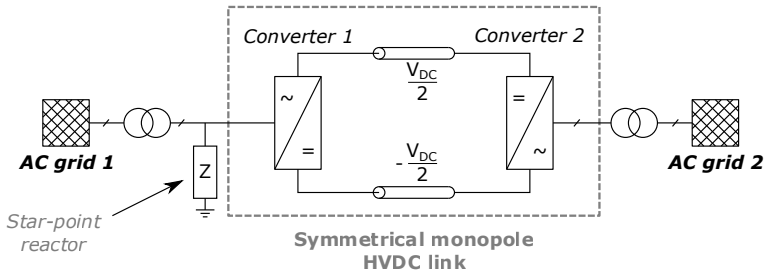


Figure 1.4: Symmetrical monopole configuration for an HVDC link, connecting two AC grids

The HVDC link itself is generally composed of two converter-stations, with a maximum pole-to-ground voltage equal to half the DC link voltage [29]. This configuration is called symmetrical monopole, it provides the maximum DC link voltage with the minimum voltage rating of the cables, as presented in Figure 1.4. Since the maximum transmitted power is restrained by the HVDC cables, a symmetrical monopole link can be doubled to increase the power as in the case of the HVDC links INELFE [21] and Pugalur-Trichur [30]. Special attention must be paid that symmetrical monopole configuration has no natural connection to the ground. Therefore, a star-point reactor, which consists of a high impedance grounding, must be used [31][32][33].

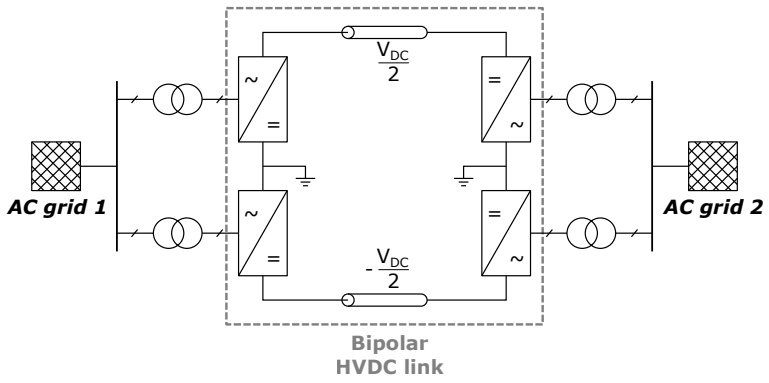


Figure 1.5: Bipolar configuration for an HVDC link, connecting two AC grids

Bipolar systems, as shown in Figure 1.5, are uncommon for offshore installations. They

could be considered in the future as two converters per pole allow redundant operation: even if one converter fails, the HVDC link may remain in operation [34].

1.1.3 Grid codes for offshore wind parks

Offshore wind-farms, and their grid connection, embody a complex system: to ensure their reliability and their safety, standards are necessary. Besides, standards aim at handling issues of stability and compatibility between the large number of connected systems, which may become more complex with the generalized use of power electronics systems. Transmission system operators (TSOs) are responsible for the establishment of the grid codes, defining a set of rules that connected equipment must follow. Since a TSO is associated to a country or a region, many grid codes with various specifications have appeared. For this reason, the European network of TSOs for electricity (ENTSO-E) also works to the establishment of a grid code, providing common standards within the European Union [33]. As Germany is an European leader in the field of HVDC-connected offshore wind-farms (see 1.4 hereinafter), the grid code of its TSO TenneT is one of the most advanced in this specific domain. ENTSO-E's grid code [35] provides more general requirements that are helpful to analyse the other regional grid codes.

1.1.3.1 Connection point voltage

For TenneT, the AC voltage at the connection point is set to 155 kV. Furthermore, a variation up to ±10% is requested to comply with voltage stability issues and to facilitate reactive power injection. ENTSO-E has a more generic approach, as it depends on the country. Connection point voltage is generally equal to 380 kV, but a per unit (pu) system is employed. Maximum non-permanent voltage variations go from 0.85 pu to 1.15 pu, including all areas in Europe. This requirement leads to an important constraint for the design of the converter: the nominal AC voltage cannot be delivered at the maximum modulation index m_a, m_a must be small enough to benefit from the 15% over-modulation capability aforementioned.

1.1.3.2 P-Q profile

The P-Q profile has also a significant influence on the sizing of the converters, as it defines the maximum apparent power. It also affects reactive power exchange capability and thermal stress of the systems as presented in Figure 1.6. The larger the P-Q profile the higher the cost, due to the increase in the initial maximum ratings of the components. In the meantime, the P-Q profile has to be consistent towards grid issues: the growing complexity of grids asks production systems for being flexible, either under-excited or over-excited, at any moment.

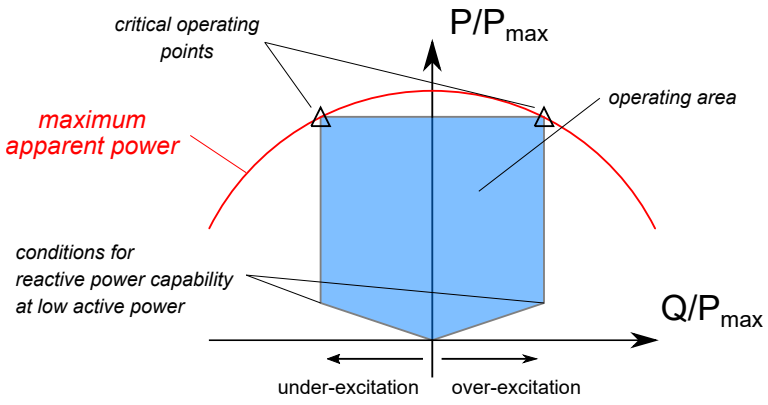


Figure 1.6: Generic P-Q profile for a grid-connected power park

Both TenneT's and ENTSO-E's profiles are normalized. TenneT requires a range of Q/P_{max} equal to 0.7 pu, from -0.3 pu to 0.4 pu, where Q is the reactive power. ENTSO-E's profile is equivalent for the upper limits, with some additional requirements: an inner envelope that can be horizontally translated is defined. Furthermore, the range of reactive powers can be higher for some areas in the European Union: the Nordic area has a maximum range of Q/P_{max} equal to 0.95 pu, whereas it is only 0.75 pu for continental Europe.

1.2 Power converters for HVDC power transmission

1.2.1 Line-Commutated Converter (LCC)

The line-commutated converter (LCC) belongs to the category of CSCs: power reversibility is obtained by reversing voltage polarity, while the converter has unidirectional current capability. In 1954 the first commercial HVDC link Gotland I in Sweden, based on this topology, was commissioned [12]. It was able to transfer 30 MW for a rated voltage of ±150 kV, between two stations composed of mercury-arc valves, and connected by a 96 km-submarine cable.

The simplest LCC is a six-pulse unit, as shown in Figure 1.7. Because of the consequent DC link voltage, several thyristors must be series-connected which implies that hundreds of these semiconductor devices are necessary to realize a six-pulse converter unit. To reduce harmonic distortion, twelve-pulse converters are more common as shown in Figure 1.8. Two six-pulse converters are associated and connected to the AC grid through different transformers: a wye-wye transformer keeps the phase-shift constant, whereas a wye-delta or a delta-wye transformer leads to a ±30°phase-shift. Converter's operation is adjusted with the firing angle, generally represented by the letter ψ, which is the turn-on delay angle applied to all thyristors, compared to an operation with diodes.

LCCs have serious drawbacks: due to the transformers and the filters they have a large footprint, which makes their use in specific areas prohibitive. Besides, active and reactive powers cannot be independently fixed, because of the CSC technology. HVDC links using LCCs cannot be connected to AC grids with low short-circuit ratios [36][34], typically inferior to 3 [37]: converter's operation is sensitive to the variations of the AC grid voltages, commutation failures are more likely to happen when the AC grid is weak.

Nowadays, LCCs are used for high-power transmission and ultra HVDC systems, where the DC link voltage reaches ±800 kV and even ±1100 kV in China, for power ratings of several gigawatts. LCC remains attractive because of its high efficiency, of about 99%. Besides, it is competitive with VSC technology thanks to the use of thyristor, cheaper and more reliable than insulated-gate bipolar transistor (IGBT). Furthermore, LCC is able to handle DC link fault currents before the protections trip [38], limiting potential damage and increasing system's availability.

1.2.2 Two-level Voltage-Source Inverter

On the contrary of CSCs, VSCs require power semiconductors with turn-off capability. The appearance of the IGBT in the 1990's has allowed the development of the first commercial HVDC link based on VSC technology, Gotland Light, commissioned in 1999 [39]. With VSC technology, many advantages such as independent control of active and reactive powers, compactness due to capacitive energy storage are brought by the two-level voltage-source inverter [40]. However, it requires a switching frequency of around 2 kHz [41], which severely increases the switching losses compared to a LCC. Besides, tens of IGBTs must be series connected [36], which means that they must commutate exactly at the same moment to ensure a proper sharing of the full

DC link voltage. Figure 1.9 shows a two-level voltage-source inverter. A DC bus capacitor is necessary since the HVDC link must be perceived as a voltage-source by the two converters. Besides, AC filters are mandatory to comply with the harmonic standards. The choice of the switching frequency is a compromise, the higher it is the lower the Total Harmonic Distortion (THD) of the currents, at the price of higher power losses.

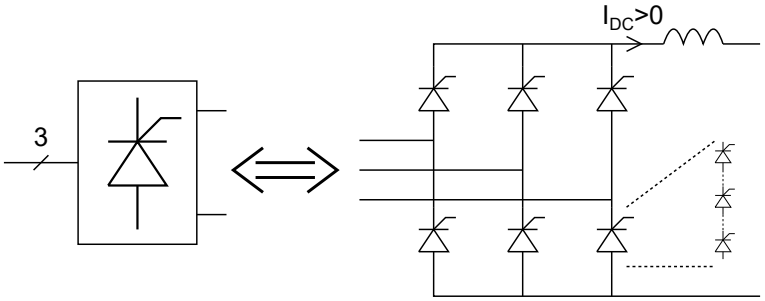


Figure 1.7: LCC - six-pulse converter unit

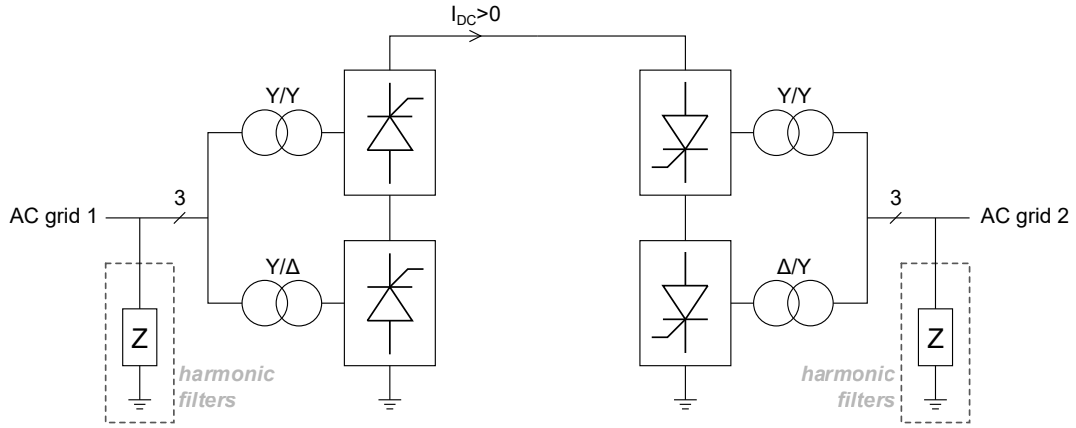


Figure 1.8: HVDC link with twelve-pulse converters, using asymmetrical monopole configuration with ground return

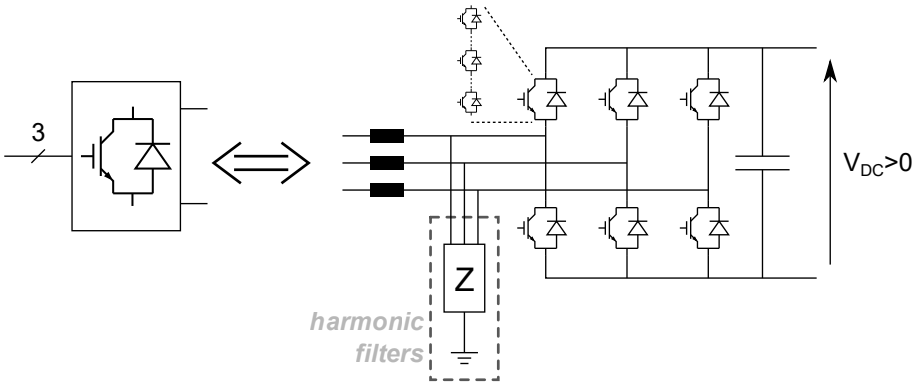


Figure 1.9: Two-level voltage-source inverter: electrical schematic and representation

1.2.3 Modular Multilevel Converter (MMC)

Multilevel converters have progressively been introduced in the 1980's (neutral-point clamped converter) and in the 1990's (flying capacitor converter, active neutral-point clamp converter):

they provide many benefits compared to two-level topologies such as lower THD and higher power rating. In the field of HVDC, multilevel topologies are particularly attractive because they allow a division of the DC bus voltage among the semiconductors: the end goal is to avoid series connected devices.

In the beginning, these topologies were only suitable for a few levels: typically, their mechanical assembly becomes too complex beyond fives levels [33]. In the meantime, the number of levels must be large enough to avoid series connection of semiconductor devices. Topologies such as the cascaded H-bridge converter have been proposed, to easily extend the number of levels N. Nevertheless, they require N isolated DC power supplies, which is too expensive at the scale of an HVDC system.

In this context, the introduction of a multilevel and modular solution in the beginning of the 2000's [42] was especially promising. The modular multilevel converter is highly scalable, allows simple mechanical assembly and removes the need for series-connected devices. Figure 1.10 shows the topology: each AC phase is connected to the DC poles by two arms, fitted with inductors to control the arm-currents. An arm is composed of N sub-modules (SMs), where a SM can be considered as an elementary converter with semiconductor devices and at least one capacitor. An arm operates as a controllable voltage-source: the purpose is to reproduce both DC and grid-frequency components inside each phase. Based on Figure 1.10, the following properties can be observed:

- For each phase, the sum of the upper voltage (or current) and the lower voltage (or current) is constant.
- For each phase, the difference of the upper voltage (or current) and the lower voltage (or current) is proportional to the AC grid voltage (or current) of the given phase.
- The sum of the upper/lower voltages/currents is constant, since the sum of the grid-frequency components is null.

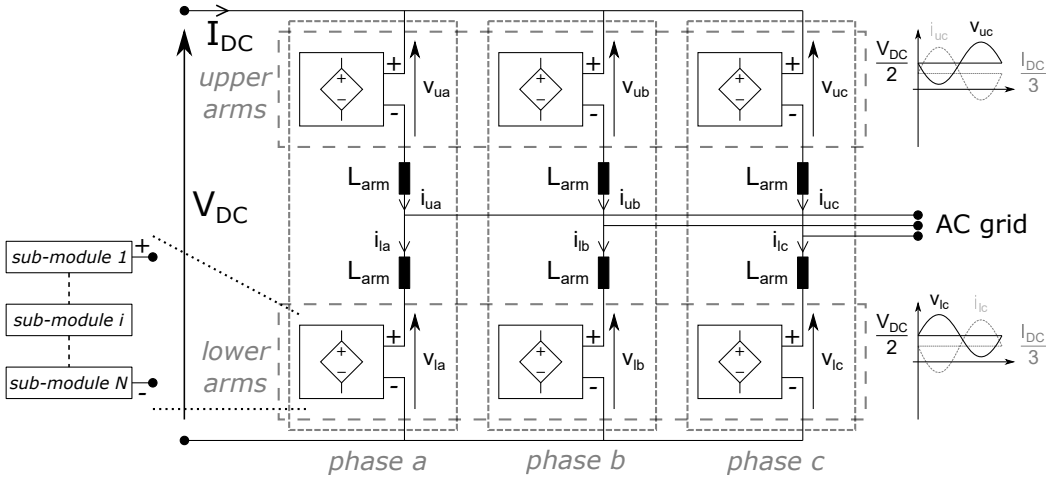


Figure 1.10: Modular multilevel converter (MMC): electrical schematic, SMs and simplified arm waveforms

These properties also show that all arm-currents are continuous, which means that high di/dt are removed during normal operation. The large number of levels has many positive consequences: the transition between two successive levels is hardly visible, which means that resulting dv/dt are not problematic. Furthermore, it leads to a THD below international harmonic standards

for the AC grid [21][32]. The apparent switching frequency is N times the effective switching frequency, which leads to a switching frequency typically below 200 Hz, i.e. ten times less than in the case of a two-level voltage-source inverter. Then, it automatically reduces converter's power losses, which is a serious drawback of the two-level voltage-source inverter. This observation also unveils that the semiconductor devices must be adapted to low frequency operation, switching performances can be reduced to enhance on-state performances, thus increasing converter's efficiency. This is further discussed in the next chapters.

Redundant operation can be easily foreseen: any failed SM is bypassed and replaced at the next scheduled maintenance, thus ensuring a high degree of availability [43]. Energy is stored by the SMs, there is no central DC link capacitor which avoids important surge currents in case of DC faults. Due to these features, especially appreciated in the field of HVDC, the first commercial MMC has been commissioned in 2010 for the Trans Bay Cable project, allowing a power transfer of 400 MW along 88 km of submarine cables, throughout a ±200 kV DC link [44]. Ever since, the MMC has become the most suitable solution for HVDC systems, operating at powers up to 1 GW [45]. In France, the project INELFE using two 1 GW HVDC links in parallel to interconnect France and Spain with a rated power of 2 GW has been completed in 2013 [21], more recently the 1 GW interconnection IFA2 with England has been commissioned in 2021 [46].

Despite a long list of benefits, MMC also suffers from some drawbacks that explain its limited range of applications. All the capacitors included in the SMs must be balanced: a voltage-ripple naturally appears and voltage deviation unavoidably occurs without active control. Capacitor-voltage balancing requires a constant monitoring and important calculation capabilities from the controllers. The stored energy is much higher than in the case of two-level topologies [47], capacitor represents more than 50% of the SM's volume [48]. Approximatively 40 kJ/MVA for the whole MMC should be considered [49]: it is worth mentioning that this figure is based on classic requirements from grid codes in terms of reactive power injection, upper and lower limits of the AC grid voltage. Many optimization methods allow a significant reduction of the stored energy, in the meantime an important criterion remains the limitation of the fault currents for HVDC power transmission. Consequently, MMC's design is sensitive to its environment, including the protection strategies.

1.2.4 Alternate Arm Converter (AAC)

The minimum volume of the converter-station is determined by the energy storage requirements, inherent to the VSC topology selected. Moreover, compactness leads to a smaller offshore platform for remote applications, thus cutting down costs. So, the cost of an offshore HVDC converter-station strongly depends on its energy storage requirements. From an electrical point of view, it has been observed in the MMC that the continuous flow of currents in both upper and lower arms contribute to increase the amount of energy stored per unit of power. To address this issue, the alternate arm converter (AAC) has been introduced [50], its schematic is presented in Figure 1.11. The AAC is a hybrid solution: it combines both the modularity of the MMC and the conventional switching process of a two-level voltage-source inverter. The purpose is to benefit from the advantages of the two topologies. The initial concept is to use one arm per half-cycle of operation, while the other arm is blocked thanks to the director switches. Nevertheless, this ideal behaviour is only reachable for a specific operating point, called "sweet spot". Otherwise, an overlap period during where both arms conduct is necessary to balance arm energies.

The use of director switches affects the arm-currents: there is no circulating currents in the converter, the ideal arm current is a half sine wave. It results in a six-pulse current in the DC link, that must be filtered. Even by considering it, the energy requirement is significantly

lower than with an MMC: an energy of 15 kJ/MVA is reported for an AAC, whereas for the same design constraints an MMC needs 39 kJ/MVA [51]. This gain of volume, due to reduction of energy storage, is mitigated by the use of director switches: they are composed of many series connected devices, inducing voltage balancing constraints. The total number of devices is increased by 50%, compared to an MMC based on half-bridge SMs. Consequently, the AAC is a promising structure, having advantages but also drawbacks in comparison to the MMC. It is much less mature than the MMC, since it has never been used in a commercial HVDC project. It might be adopted in the years to come, only if the manufacturers are able to overcome the drawbacks inherent to this structure.

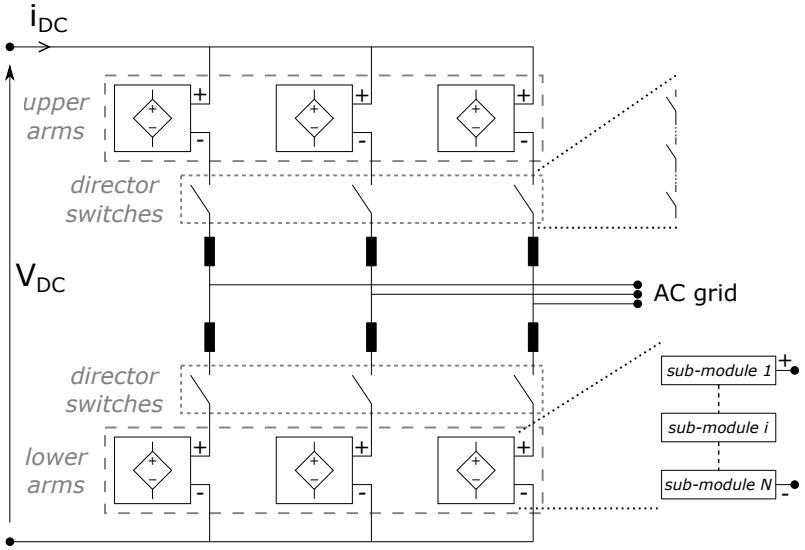


Figure 1.11: Overview of the alternate arm converter (AAC)

1.3 Semiconductor devices for HVDC power transmission

1.3.1 Overview of the semiconductor devices for HVDC power transmission

1.3.1.1 Thyristor

Presentation The thyristor was commercially introduced by the General Electric Company in 1957, as the first solid-state valve. The name "thyristor" lies in the mix of "thyratron" and "transistor", mentioning both semiconductor devices and mercury-arc valves [52]. Other names refer to thyristor, such as Silicon-Controlled Rectifier (SCR) and Phase-Controlled Thyristor (PCT). Since its first use in the HVDC project "Eel River" in 1972, it has remained the main semiconductor device in the field of high-power transmission. It has brought lower cost, higher robustness and higher efficiency than mercury-arc valves. Nowadays, thyristor is the elementary brick of power electronics for ultra HVDC systems, mainly present in China [53]. Corresponding thyristors have a blocking voltage capability of 8.5 kV for a wafer area of 150 mm (six-inch), allowing current ratings up to 4 kA [10].

The thyristor is a four-layer semiconductor device, as shown in Figure 1.12. To turn it on, it is necessary to bring a certain gate charge, i.e. a pulse of gate current with a minimum duration, under a positive anode-cathode voltage. Afterwards, the process is self-fed, the thyristor conducts the current without any action on the gate. Initially, a positive gate current in the base of the lower NPN transistor induces an amplified positive collector current, i.e. a positive current in the base of the upper PNP transistor (with respect to the notations). Then, the base

current of the PNP transistor induces a collector current, also amplified. This current goes into the base of the NPN transistor. Thus, this phenomenon goes on until the complete switching of the thyristor [54], it is said that the thyristor has a latching structure at turn-on (latch-up structure). It must be noted that during turn-on, a small gate current, called "back-porch" current, is required to ensure a stable on-state operation. Nevertheless, a thyristor cannot be turned off by acting on the gate, because turn-off depends on the anode-cathode voltage V_{AK} and the anode current I_A. Actually, the current has to fall to zero, with a negative anode-cathode voltage, applied during a minimum duration t_q. It corresponds to a reverse-recovery process, the recombination of electrons and holes that occurs must not be interrupted to ensure a proper blocking of the device [55].

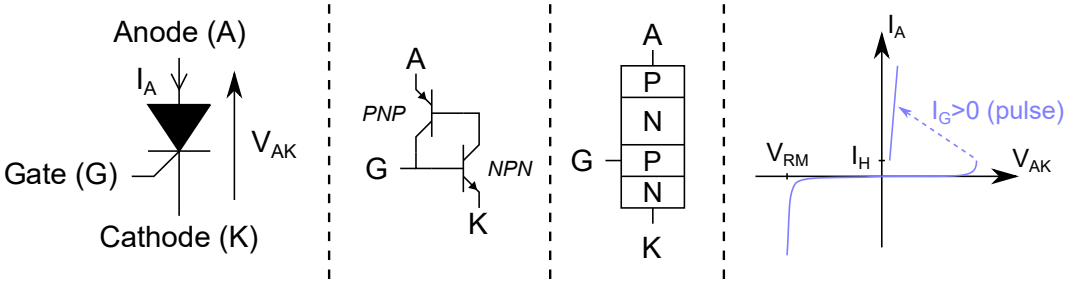


Figure 1.12: Thyristor: symbol, equivalent representation, simplified physical structure and v-i static characteristic

Figure 1.12 also shows the static characteristic of a thyristor: it is a two-quadrant device, conducting the current in one direction and blocking both positive and negative voltages. This is the most common device in CSCs, where the direction of power flow depends on the sign of the average DC link voltage. Used for more than sixty years, its technology is mature and well-established. It explains the possibility to reach such voltage and current ratings, with an exceptional reliability. Moreover, thanks to its simple control and assembly, its cost is very attractive compared to other semiconductor devices with similar ratings.

Performances The thyristor benefits from very low conduction losses: for a rated voltage of 8.5 kV, the threshold voltage is around 1 V for a slope resistance below 0.5 mΩ. The same device can be turned on in less than 10 μs. Nevertheless, its turn-off time t_q may be superior than 100 μs: it limits the switching frequency of the thyristor. Corresponding power losses are much more important than during turn-on. Thyristor systematically fails into short-circuit mode: a part of the wafer melts, creating a sustainable short-circuit path. Short-circuit failure mode (SCFM) is particularly appreciated in the field of HVDC transmission, since a semiconductor failure does not endanger a converter's availability. The device is robust: it is reported that its lifetime can reach half a century [10], considering than most of the devices under operation have never been replaced.

1.3.1.2 Insulated-Gate Bipolar Transistor (IGBT)

Presentation IGBT, present in the market since 1988 [56], has quickly become a paramount device for a wide range of power. In 1997, it has been used in the first VSC-HVDC project in Sweden by ABB [57]. Firstly, in two-level structures, IGBTs were stacked to realize a series association of devices. Multilevel topologies then the MMC appeared, leading to a more efficient use of the device: it is no longer mandatory to connect IGBTs in series in HVDC converters. Nowadays, IGBT is the main semiconductor device for HVDC power transmission based on VSC

technology.

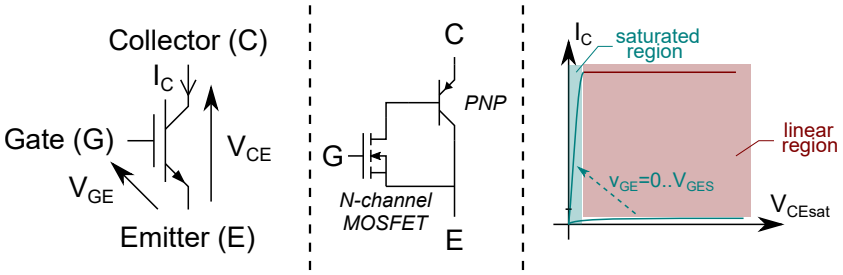


Figure 1.13: IGBT: symbol, simplified equivalent representation and static v-i characteristic

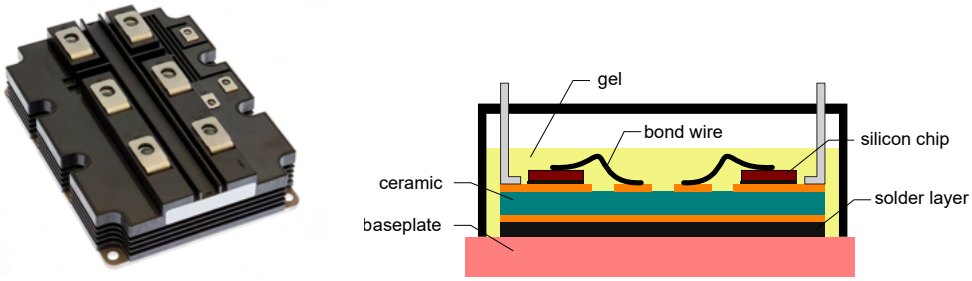
As shown in Figure 1.13, the IGBT is a single-quadrant device. Then, it is systematically associated with a diode to benefit from bidirectional power flow in VSC-based converters. Besides, it cannot block a negative voltage. IGBT aims at combining the benefits of bipolar transistor and metal-oxide-semiconductor field-effect transistors (MOSFET): a bipolar transistor involves both electrons and holes in its operation. However, it is controlled by the base current, which requires a complex gate driver. On the other hand, a MOSFET has a v-i static characteristic determined by the gate-emitter voltage V_{GE}, but it only uses one kind of charge carrier, which implies an important on-state voltage at high currents. Figure 1.13 shows a simplified representation of the IGBT: an N-channel MOSFET drives a PNP transistor, so the electrical conductivity of the whole device is modulated by V_{GE}. This mode of operation is opposed to the latch-up effect inherent to a thyristor, turn-on and turn-off speeds are controllable. Nowadays, IGBT power modules are available with voltage ratings up to 6.5 kV, and current ratings up to 3 kA. Figure 1.13 unveils two distinct areas:

- An ohmic area, also called saturation region, where the current increases with a small voltage drop V_{CE}. This region is preferred for on-state operation since power losses are minimized.
- A linear region, where the current is almost constant for a given gate-emitter voltage. This area is not used for normal operation. On the other hand, it is possible to limit the current by reducing V_{GE}: the IGBT is desaturated in this area, which leads to an important power dissipation. This kind of strategy can be applied to handle short-circuits [58][59].

On the contrary of thyristor, IGBT cannot be made on a single wafer. MOS technology requires the use of several dies [60], with typical surfaces of 1.6 cm^2 [58]. For medium-power and high-power applications, it implies that chips must be parallel connected with a common gate, these links are generally realized with bond wires. Still for such applications, IGBTs are generally packed with diode chips inside modules. These modules are single-side cooled by the baseplate, as presented in Figure 1.14. For such modules, bond wires are one of the main weaknesses: in case of important surge currents they may be vaporized [61]. Besides once a chip has melted, its associated bond wires melt as well, and the remaining chips have to carry a higher current, which triggers a domino effect [60]. Consequently, wire-bonded IGBT modules have an open-circuit failure mode. This requires an external bypass mechanism to ensure an uninterrupted operation in case of fault. Without it the device may explode, endangering the nearby systems [61].

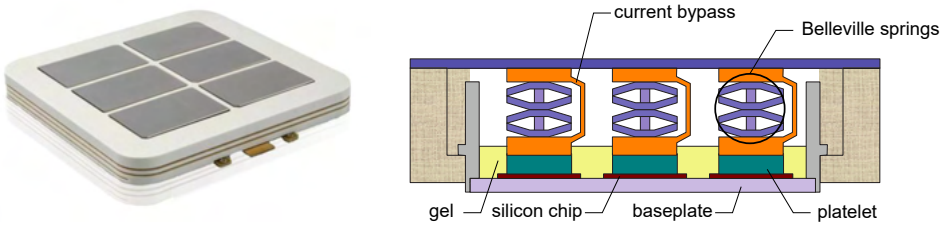
The introduction of VSCs with series connected devices in the end of the 1990's has led to the development of Press-Pack IGBTs (PPIs): mechanically speaking the devices are easily stackable, which is a desirable feature for HVDC where a large number of devices is used. Indirect

pressure PPIs, as presented in Figure 1.15, have been originally introduced to figure out issues of pressure distribution between the chips. In case of fault, the platelet melts and spills onto the silicon chip, creating an electrical contact with the baseplate: an artificial SCFM is realized [62]. This feature is more and more attractive as it increases converter's reliability, in case of failure the device remains explosion-free. PPI generally has higher current ratings: thanks to the double-side cooling and the packaging, the thermal impedance is generally lower [63]. However, the SCFM introduced within PPIs has a slight drawback: the mechanical arrangement made of the platelet, the silicon chip and the solder layers is more sensitive to ageing, due to thermal cycling [62].



(a) (b)

Figure 1.14: Wire-bonded IGBT module. (**a**) Illustration. (**b**) Simplified schematic.



(a) (b)

Figure 1.15: Indirect pressure PPI. (**a**) Illustration. (**b**) Simplified schematic.

Performances IGBT exhibits good static and dynamic performances: a threshold voltage of about 1.2 V and a slope resistance below 0.8 mΩ are typical. Turn-on is around some microseconds, while turn-off may last approximately 10 μs for 4.5 kV devices. For medium-voltage IGBTs, the switching frequency can reach 10 kHz due to the low switching losses. For higher voltages, thermal issues become dominant and the switching frequency must be limited to a few kHz, and even a few hundred Hz in the field of HVDC. IGBT has a large safe operating area (SOA), commutations involve high di/dt, e.g. 2800 A/μs for the collector current I_C, and high dv/dt, e.g. 3500 V/μs for the collector-emitter voltage V_{CE} [58]. IGBT power modules are sensitive to thermal cycling, a degradation of the thermal contacts realized by the solders and the thermal contact grease can be observed during power cycling tests [58]. Consequently, the thermal resistance of the device progressively increases, which reduces the cooling capabilities and increases the power losses.

Bi-mode IGBT (BIGT) Bi-mode IGBT (BIGT) is an improvement of the reverse-conducting IGBT: BIGT essentially allows the use of the same silicon area to conduct current in both directions, whereas a reverse-conducting IGBT only regroups the two "functions", IGBT and diode,

on the same chip. It reduces the junction-to-case thermal resistance, as well as thermal cycling since the major part of the silicon area is always conducting [64]. Nowadays, BIGT is available at voltage ratings of 5.2 kV and current ratings up to 3 kA. This technology has a great potential for medium-power and high-power converters since the silicon area is minimized, thus reducing costs. BIGT is considered for the next generation of VSC valves by Hitachi ABB [65].

1.3.1.3 Diode

Presentation The diode is a non-controllable single-quadrant semiconductor device. Its origin lies in a simple P-N junction to provide asymmetrical behaviour. Then, it has evolved towards several technologies depending on the considered application: for high-voltage operation, PIN diodes ("I" for intrinsic) are preferred [56]. At turn-on a forward voltage appears: the resulting overshoot V_{FR} depends on the di/dt that is applied. At turn-off, a reverse-recovery phenomenon occurs and leads to the appearance of a negative current, whose peak value is I_{rr}, as presented in Figure 1.16. Diodes are paramount devices to build VSCs, as they ensure proper commutations when used as a free-wheeling with IGBTs and MOSFETs, for medium-power and high-power applications.

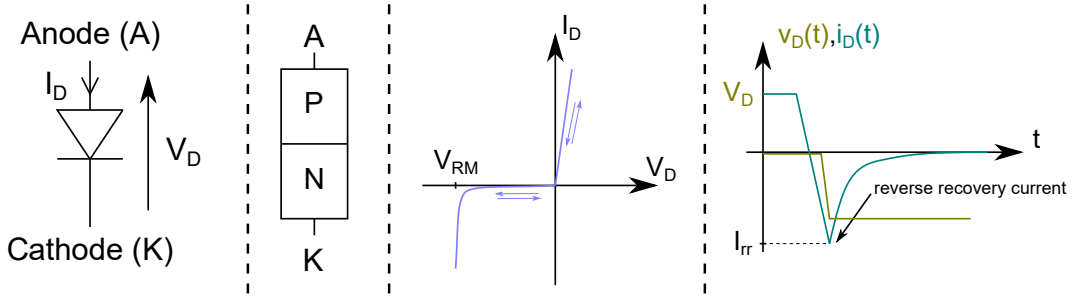


Figure 1.16: Diode: symbol, simplified physical structure, static v-i characteristic and turn-off waveforms

Performances During on-state, a threshold voltage of about 1.5 V and a slope resistance inferior than 1 mΩ are typical for a 4.5 kV diode. Turn-on duration is a few microseconds, corresponding losses are negligible. At turn-off, di/dt around 1000 A/μs is typically reached. The SOA of diodes is a critical issue, it is mainly defined by the di/dt at turn-off: the higher it is the higher the reverse recovery current I_{rr}, which significantly increases diode's failure rate [66]. di/dt must be limited either by the gate resistor, in the case of an IGBT or a MOSFET, or by a di/dt choke in the case of a thyristor. Considering a controllable device and a diode, diode's SOA is generally the limiting factor [67]: therefore, diodes with higher di/dt capabilities, up to 10 kA/μs at a junction temperature up to 140°C have been developed [68]. Consequently, the selection of the maximum di/dt is an important trade-off between reliability and performances. It involves both the diode and the controllable device, and it directly affects the design of the commutation cell.

1.3.1.4 Gate Turn-Off Thyristor (GTO)

Presentation The development of the gate turn-off thyristor (GTO) has lied in the need to control turn-off, in order to expand the possible applications of thyristors. Invented in 1960, it took time to become a paramount device in the field of traction and industrial medium-voltage drives [69]. In a power range between 500 kVA and 20 MVA [58], it was the main turn-off device

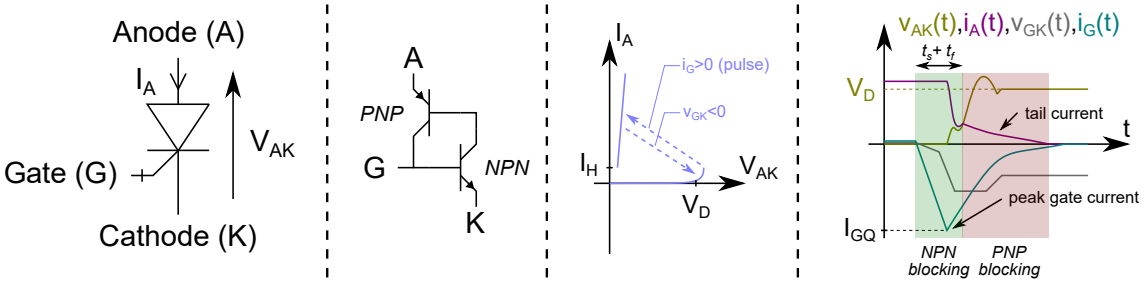


Figure 1.17: Gate Turn-Off thyristor (GTO): symbol, equivalent representation, simplified v-i static characteristic and waveforms during turn-off

before the appearance of IGBT.

A GTO cannot be turned off with the same physical structure as a "classic" thyristor, as presented in the previous section. It is necessary to drop the gain of the upper PNP transistor, by using anode shorts [58], to limit its influence during turn-off. The new structure, allowing turn-off, has a negative impact on the overall performances of the device: both on-state and turn-on induce more power losses. Moreover, the back-porch current is significantly increased compared to a classic thyristor with the same electrical ratings.

The turn-off process requires the application of a negative gate-cathode v_{GK} voltage [54]. As shown in Figure 1.17, the gate current i_G decreases slowly, with a constant slope. It reaches a minimum, I_{GQ}, allowing the decrease of the anode current i_A. In the meantime, the anode-cathode voltage v_{AK} starts to rise. The blocking of the NPN transistor is complete when the cathode current is null, with a non-null anode-cathode voltage: its duration is the sum of the storage time t_s and the fall time t_f. When the cathode current reaches zero, the gate has taken over the full anode current i_A: the turn-off process occurs within the PNP transistor, where a "tail current" and the full anode-cathode voltage V_D coexist. This second step of the turn-off process generates substantial power losses.

Another issue than must be handled is the homogeneity of the turn-off, the current distribution must remain identical over the cathode area. Because of the monolithic structure of the gate turn-off thyristor, a process named interdigitation must be employed to ensure a homogeneous extraction of the current from the cathode to the gate during turn-off [70]. It consists in splitting the cathode into several islands [58], distributed in concentric circles. This modification of the wafer geometry remains limited, the current distribution remains non-homogeneous within the cathode islands, which facilitates the appearance of hot-spots. Therefore, a dv/dt snubber is mandatory to remain within the SOA of the semiconductor [69].

Performances On-state losses of GTO are substantially high, for a rated voltage of 4.5 kV the threshold voltage can reach 1.8 V. Turn-on time is around 10 μs, whereas turn-off time is about tens of microseconds [71], where the storage time t_s is dominant. The snubber allows dv/dt typically below 500 V/μs, up to 1000 V/μs [56]. Turn-off gains are between 3 and 5 [58], i.e. the maximum gate current I_{GQ} as named in Figure 1.17 may reach 750 A for an anode current i_A of 3 kA [71]. The back-porch current during on-state is typically between 4 A and 8 A in the same conditions: it leads to a bulky gate driver, which increases costs and reduce the reliability of the whole system because of the important number of components. Switching frequency is not limited by the turn-off time, but by thermal issues: 300 Hz is generally the maximum reachable value [54]. Therefore, GTOs suffer from severe drawbacks that cannot be

overcome. For HVDC applications, it has been shown that its cost is prohibitive compared to equivalent designs with classic thyristors [72].

1.3.2 Other relevant turn-off devices for present and futures applications

1.3.2.1 IEGT

The injection-enhanced gate transistor (IEGT) is based on a standard IGBT structure with a modification of the distance between the emitter contacts, which leads to a higher carrier concentration close to the emitter [73]. Then on-state voltage is reduced, which favours the use of IEGT for high current applications. Its manufacturer Toshiba provides IEGT in a press-pack device. 4500 V/2000 A IEGTs including an anti-parallel diode with SCFM are available: such ratings compete with the available IGBTs for HVDC applications.

IEGT is already used in the Hokkaido-Honshu VSC-HVDC project, transmitting 300 MW under 250 kV in Japan, since 2019 [74]: the press-pack packaging, the SCFM and the high current rating are presented as key features of this semiconductor. From the last ten years, six VSC-HVDC projects using IEGT have been delivered in China, with power ratings from 200 MW to 1100 MW [75]. Consequently, IEGT is considered as a potential device for HVDC links dedicated to grid connection of offshore wind-farms.

1.3.2.2 Silicon carbide (SiC) MOSFET

Silicon Carbide (SiC) devices belong to the group of wide-band gap semiconductors. Due to their intrinsic properties they benefit from lower switching losses, with the ability to operate at higher junction temperatures, under higher blocking voltages than traditional silicon devices. Nowadays, practical realizations have led to the development of SiC MOSFET modules with ratings up to 3300 V/750 A/175°C, for medium power applications [76]. In the meantime, a class of SiC devices with voltage ratings superior to 10 kV is emerging [77][78]. Nevertheless, current ratings remain low, inferior to 150 A. Consequently, the maximumu current ratings of SiC MOSFETs are still lower than the minimum requirements for HVDC applications [79].

Looking at the performances, SiC MOSFETs exhibit very low switching losses compared to Si IGBTs [80]. They are especially relevant for medium or high frequency applications, at powers up to several hundred kilowatts, where a significant reduction of the power losses can be obtained [81]. However, SiC MOSFETs, as unipolar devices, have higher on-state losses than Si IGBTs at high current densities, which makes SiC less attractive for high-power applications where on-state losses tend to be dominant [82]. A comparison of power losses between SiC MOSFETs and Si IGBTs applied to an HVDC-MMC solution has shown that a break-even point exists, typically at 600 MW, where Si IGBTs lead to a higher efficiency than SiC MOSFETs [83]. To overcome this limit, bipolar SiC devices are the most promising solution and clearly exhibit better performances than both Si IGBTs and Si IGCTs on the paper [84]. Nevertheless, practical realizations currently have tiny current ratings [78][85]. Issues of cost related to SiC devices should be considered as well, as it has been reported that because of the materials and the fabrication process they remain significantly more expensive than comparable Si devices [86][87].

1.3.3 Integrated Gate-Commutated Thyristor (IGCT)

1.3.3.1 Presentation

The GTO suffers from many drawbacks: at the price of turn-off capability, on-state losses have been increased compared to a standard thyristor. Besides, bulky snubbers are required to limit

both dv/dt and di/dt during turn-off. It has become clear that the turn-off process is the weakness of the GTO, blocking a four-layer device induces many issues. The integrated gate-commutated thyristor (IGCT) has been developed by Asea Brown Boveri (ABB) in the end of the 1990s to figure out this issue. The thyristor structure is converted to a single transistor prior to being turned off. Nowadays, IGCT coexists with IGBT in the domain of medium voltage drives, and more generally for a range of power between 2 MW and 20 MW.

IGCT is intrinsically a thyristor: it has a latch-up structure at turn-on, and a back-porch current is required to keep the on-state stable. To turn off an IGCT, a negative gate-cathode voltage V_{GK}=-20 V is applied, as presented in Figure 1.18. Then, the cathode current quickly decreases while the gate current rises in absolute value: the gate withstands the whole anode current during a short time. This step is quick enough to occur before any rise of the anode-cathode voltage v_{AK}. When the cathode current is equal to zero, the device is equivalent to a PNP structure with a non-connected base. Consequently, it turns off like a transistor [69][88]. Such turn-off is homogeneous: SOA is greatly enhanced, and dv/dt limitation is not necessary any more [71]. The transparent anode technology has been introduced as well to remove anode shorts, used for GTO: this term designates the replacement of the lower P layer, connected to the anode, with a P-N junction where the P layer is thinner. A relevant design of these junctions allows a smaller back-porch current and a faster turn-off, involving less energy [58]. The resulting device benefits from better static and dynamic performances than the GTO, with a drastic reduction of the requirements for the gate unit [71].

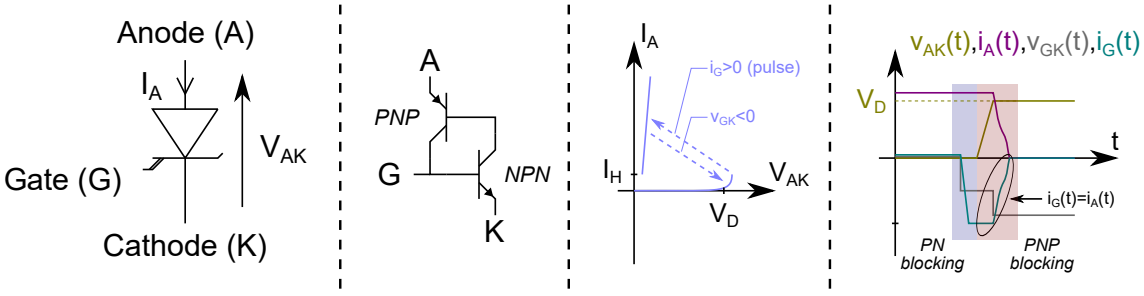


Figure 1.18: Integrated Gate-Commutated Thyristor (IGCT): symbol, equivalent representation for turn-on and on-state, simplified v-i static characteristic and waveforms during turn-off

Several improvements have been performed on the device itself including its gate unit, leading to a complete modification of the device. Hence an IGCT cannot be separated from its gate unit, due to the crucial role of integration in the behaviour of the device. Turn-off process, to be fast enough, lies in a high di/dt of the gate current: several MOSFETs are associated in parallel to divide the parasitic inductance of the connection, allowing a fast energy exchange with the capacitor bank as shown in Figure 1.19. Then the gate contacts are circularly shared around the wafer to minimize the parasitic inductances between the capacitor bank and the actual gate of the device. Compared to a traditional GTO, these developments have led to a stray inductance 60 times smaller [69], inferior to 5 nH for the first generation of IGCTs.

1.3.3.2 Performances

IGCT currently exists in four-inch (approximately 91 mm) and six-inch (approximately 150 mm) sizes, with voltage ratings of 4.5 kV, 6.5 kV, and 5.5 kV for specific applications on the American continent. 10 kV IGCTs exist as prototypes [89]. Turn-off current can reach 7 kA with four-inch wafers [53], and 10 kA with six-inch wafers [90]. Hitachi ABB has introduced the concept of "High Power Technology +" in the latest generations of IGCTs, allowing junction

temperatures up to 140°C [91]. The excellent on-state performances of IGCT are regularly pointed out [56][92][93]: conduction losses are systematically lower than that of IGBT for the same voltage ratings. Turn-on and turn-off have approximately the same duration, below 10 μs. Thanks to the reduction of switching losses and the smaller turn-off times, it is possible to reach a permanent switching frequency of 2 kHz [71]. High-frequency bursts can be considered for specific operations, for instance ten pulses, at 25 kHz, and under 3.3 kV/400 A have been demonstrated, which is exceptional for a thyristor [94]. Using soft switching operation with low currents, where switching losses are almost neutralized, steady-state operation above 4 kHz has been demonstrated under 2500 V [95], which proves that IGCT can compete with IGBT beyond low-frequency operation with a dedicated converter design. With a stray inductance lower than 5 nH and a nominal gate-cathode voltage V_{GK}=-20 V, the anode current has a rate of rise superior to 3 kA/μs.

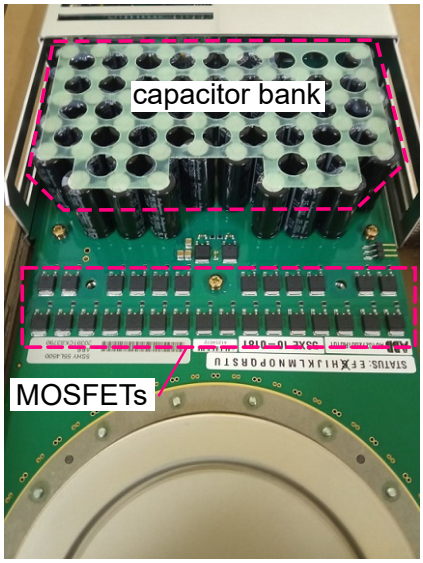


Figure 1.19: Turn-off circuit of the IGCT, mainly composed of MOSFETs and electrolytic capacitors to increase the maximum di/dt of the gate current

Despite all the improvements made on IGCT, the power consumption of its gate unit remains non-negligible: typically, it is about 40 W for a turn-off current of 2 kA at a switching frequency of 150 Hz [96]. In the meantime, an IGBT gate unit only consumes a few watts: IGCT gate units require bulkier power supplies. In terms of packaging, the IGCT is a press-pack device: mounting is based on high axial efforts to have a proper electrical and thermal contact, as presented in Figure 1.20. Besides, materials benefit from low thermal expansion coefficients so IGCT has excellent thermal cycling capabilities [97], superior to IGBT's [54][98], whose assembly lies in bonding wire and/or thermally heterogeneous parts [99].

1.3.3.3 IGCT with free-wheeling diode

IGCT is intrinsically a single-quadrant device: it requires a diode connected in anti-parallel to operate in the second quadrant, as necessary with VSC systems. However, a diode cannot naturally operate with an IGCT as a free-wheeling device. Indeed, the latching properties of IGCT at turn-on must lead to the destruction of the diode, because di/dt is not limited [69]. This issue is easily handled with IGBTs, commutation speed is controlled with gate resistors. Since commutation speed cannot be modulated with IGCTs, an external circuit is added: the traditional solution consists of a di/dt choke L_{cl}, with an RCD snubber that limits the inductor-

voltage [88]. The four elements have been represented in Figure 1.21.

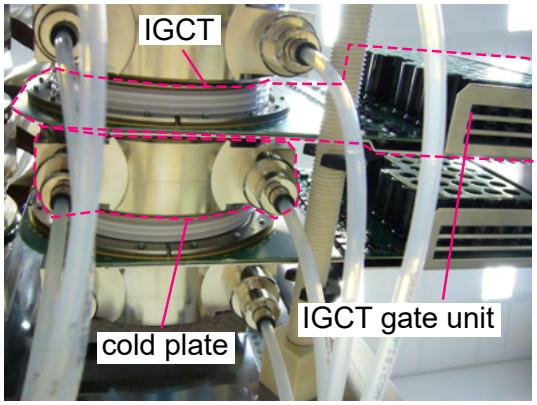


Figure 1.20: Typical mounting of two IGCTs into a stack, each IGCT is in contact with two cold plates

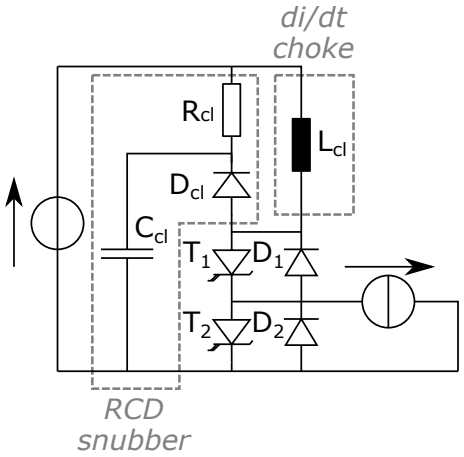


Figure 1.21: Clamp circuit with di/dt choke in an IGCT-based commutation cell

The design of the circuit is divided into three steps. The most important one is the selection of the di/dt inductance L_{cl}: it influences the reverse-recovery losses of the diodes and the energy dissipation through R_{cl} [66][90], but also the volume of the clamp circuit. Then, R_{cl} and C_{cl} are used to adjust the trade-off between the overvoltage at IGCT turn-off and the total turn-off time [54][100]. In the end, it is advised to validate and adjust the design with simulations [67]. The clamp circuit is supposed to operate during a short period, right after commutations: it ends when D_{cl} naturally turns off. If an event due to the converter's control triggers the clamp circuit while D_{cl} conducts, the diodes within the commutation path of the clamp circuit may be destroyed. This phenomenon can be encountered when the switching frequency is too important or when the lower and upper limits of the duty-cycle have not been correctly defined. Moreover, this situation may occur when multiple commutation cells are bound to the same clamp circuit, as in the case of multi-phase systems, so it becomes mandatory to space out the control signals of the commutation cells [69].

1.3.3.4 Reverse-conducting IGCT

Reverse-conducting IGCT (RC-IGCT) Reverse-conducting devices are generally relevant in power electronics, because they contribute to increasing the power density of the converter:

a single packaging regroups a two-quadrant device, which simplifies the assembly, increases the overall reliability, and reduces the total silicon area. Reverse-conducting IGCTs (RC-IGCTs) have been introduced straight after asymmetric IGCTs to address these concerns [94]; the diode part is in the centre of the wafer as presented in Figure 1.22.

In the beginning, RC-IGCTs are mainly developed for medium-voltage inverters, so the diode part was quite small compared to the GCT part. More recently, RC-IGCTs with consequent current ratings (6.5 kV/2.1 kA and 4.5 kV/3 kA) have been proposed [101]. From now on, these devices are optimized for a more even use of both GCT and diode parts, typically within an MMC. For a six-inch wafer, the maximum turn-off current exceeds 10 kA at 25°C, whereas the diode part can handle a di/dt at turn-off up to 2500 A/μs under 2800 V: large SOAs can be reached with RC-IGCTs.

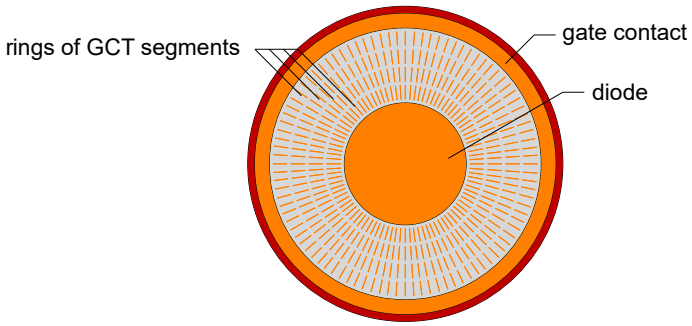


Figure 1.22: Representation of a RC-IGCT wafer; gate, GCT cathode segments and diode (anode side) are drawn in orange

Bi-mode IGCT (BGCT) The Bi-mode IGCT (BGCT) is sort of an improvement of the RC-IGCT, where the diode and GCT parts have been interdigitated to share the same silicon volume in both GCT and diode modes [102]. This evolution leads to smaller on-state losses, better thermal distribution and softer reverse-recovery [103]. So, the BGCT is a promising device to optimize the use of the available silicon area.

1.3.3.5 Reliability and related failure mechanisms

Definition of reliability for high-power semiconductors Reliability theory is commonly based on the failure in time (FIT) rate. 1 FIT corresponds to 1 failure within 10^9 hours, i.e. a mean time to failure (MTTF) of 114 000 years. In a system, the FIT rates are summed, then the MTTF is expressed as the inverse of the total FIT rate. For a given discrete component, the FIT rate evolves with lifetime:

- In the beginning, failures mechanisms due to manufacturing or assembly imperfections are dominant. The corresponding FIT rate quickly decreases with lifetime.
- In the effective lifetime of the device the FIT rate is almost constant, it slightly increases with a low slope because of ageing. Failure mechanisms can be described as random phenomena, following a statistical law.
- In the end, failure mechanisms due to ageing are dominant, so the FIT rate steadily increases.

Consequently, all FIT rates λ given by manufacturers are related to the intermediate region, where a statistical approach is applicable.

Failure mechanisms An important source of failure for the IGCTs is the turn-off. As all turn-off devices, it must comply with specific conditions of operation prior to turn-off including the turn-off voltage, the turn-off current and the junction temperature. As its junction temperature increases, an IGCT is more likely to fail in the same turn-off conditions (V,i) because of the important energy dissipation that occurs: a derating factor related to the junction temperature must be considered, defining the SOA of the IGCT during turn-off. Concerning the gate unit failure, causes are plentiful. However, optical transmitters and receivers appear to be the main source of failure [54]. Failures due to the capacitor bank are marginal: lifetime between 10 years and 20 years is expected at maximum ambient temperature [104][67].

Failure due to cosmic rays is a different type of failure. It corresponds to localised breakdowns caused by high-energy particles [105]. This phenomenon can be statistically described to obtain a failure rate, that depends on the blocking voltage, the duty-cycle and the junction temperature. To reduce the failure rate due to cosmic rays, the IGCT must ideally operate with a high duty-cycle, at a high junction temperature, and under a low blocking voltage. These conditions are not met in classic applications, so a compromise has to be found to keep the device under a reasonable threshold. It leads to a criterion that generally limits the maximum blocking voltage, which highly influences this failure rate.

Comparison of FIT rates between IGCT and IGBT Based on [60], the FIT rates of a half-bridge SM using reverse-conducting IGCTs (RC-IGCTs), wire-bonded IGBT modules and PPIs have been reported in Table 1.1. The devices themselves, the gate units and the clamp circuit in the case of the IGCT have been considered.

The FIT rates related to the device itself is important for both IGBT power modules, mainly because of the large part count. Actually, the PPI has 72 chips while the wire-bonded IGBT module has 36 chips. The power level is also concerning: the six-inch RC-IGCT has more than twice the power rating of the wire-bonded IGBT module. Then, it is compulsory to associate two wire-bonded IGBT modules in parallel to obtain similar power ratings, which multiplies the corresponding FIT rate by two as well. As a consequence, the total FIT rate is the smallest with the RC-IGCTs, a significant difference is observed compared to the two IGBT technologies. A second approach is to assess the FIT rate per MVA: these three devices have the same rated voltages, nevertheless, they have different current ratings. The total FIT rate, normalized by the power rating of the semiconductors, favours the IGCT even more since it benefits from the highest current rating.

Designation	**wire-bonded IGBT module**	**PPI**	**RC-IGCT**
device	2x2x180	2x324	2x100
gate unit	2x2x150	2x150	2x200
clamp circuit	-	-	55
total FIT rate	1320	948	655
rated voltage	4500 V	4500 V	4500 V
rated current	2x1200 A	2000 A	3 kA
device	66 per MVA	72 per MVA	14 per MVA
gate unit	55 per MVA	33 per MVA	29 per MVA
clamp circuit	-	-	4 per MVA
total FIT	122 per MVA	105 per MVA	48 per MVA

Table 1.1: FIT rate of a half-bridge SM including at least two devices, two gate units and a clamp circuit (IGCT only), for different semiconductor devices [60]

Short-circuit failure mode Having a mechanical structure that of the thyristors and GTOs, IGCTs benefit from SCFM [69][71]. [106] has led a long and comprehensive study to validate this property. It has shown that the short-circuit is stable, with a low forward voltage, allowing an operation after failure during several years. This paramount property is further discussed in the second chapter.

1.4 Existing HVDC systems connecting offshore wind-farms

1.4.1 Overview of the existing projects

Table 1.2, Table 1.3 and Table 1.4 summarize the main data for 9 HVDC links that are in operation in the North Sea, handled by the Dutch-German TSO TenneT. In Table 1.3, CTL refers to Cascaded Two-Level topology, which corresponds to an MMC where series connection of IGBTs within SMs is made [107]. According to the last projects, the current trend is to use one HVDC link to connect between two and three offshore wind parks, leading to an approximate power rating of 900 MW. Symmetrical monopole is the best-suited configuration in this case, as it leads to a DC link voltage twice as large as the maximum pole-to-ground voltage, limited by the technology of XLPE cables, confirming the observations of 1.1.2.2. As explained in 1.1.1.1 HVDC is preferred because the transmission distance is important, between 130 km and 205 km here.

Name	**BorWin1**	**BorWin2**	**BorWin3**
Location	North Sea		
TSO	TenneT		
Manufacturer	Hitachi ABB	Siemens	Siemens
Power	400 MW	800 MW	900 MW
DC voltage	±150 kV	±300 kV	±320 kV
Configuration	symmetrical monopole		
Distance	200 km	200 km	160 km
Cables	XLPE		
Wind-farms	1	3	2
Topology	2-L VSI	HB-MMC	HB-MMC
Devices	IGBT		

Table 1.2: Existing offshore HVDC systems - BorWin family [108][109][110][111][112][29][113]

1.4.2 Incoming HVDC projects in Europe

DolWin5, DolWin6 and BorWin5 should be in operation in the years to come, increasing the offshore wind power production by 2.7 GW in Germany, thanks to the low water depths in the North Sea [119]. Dogger Bank is the first HVDC project ordered in the United Kingdom, it is divided into three sub-projects of 1.2 GW wind-farms with their corresponding HVDC systems, leading to a total transmission capacity of 3.6 GW [110]. In the past twenty years, the United Kingdom has always chosen HVAC systems to ensure offshore power transfer, as wind-farms have been installed at distances inferior to 20 km from the coast. Therefore, this investment throws light on the HVDC technology, which has come out as the best choice to connect wind-farms in the Dogger Bank area, located more than 130 km off the United Kingdom's coast.

Name	**DolWin1**	**DolWin2**	**DolWin3**
Location		North Sea	
TSO		TenneT	
Manufacturer	Hitachi ABB	Hitachi ABB	GE
Power	800 MW	916 MW	900 MW
DC voltage	±320 kV	±320 kV	±320 kV
Configuration		symmetrical monopole	
Cables	2	2	2
Distance	165 km	135 km	162 km
Cables		XLPE	
Wind-farms	3	3	2
Topology	HB-CTL	HB-CTL	*HB-MMC*
Devices		IGBT	

Table 1.3: Existing offshore HVDC systems - DolWin family [110][114][115][29][113]

Name	**HelWin1**	**SylWin1**	**HelWin2**
Location		North Sea	
TSO		TenneT	
Manufacturer		Siemens	
Power	576 MW	864 MW	690 MW
DC voltage	±250 kV	±320 kV	±320 kV
Configuration		symmetrical monopole	
Distance	130 km	205 km	130 km
Cables		XLPE	
Wind-farms	2	3	2
Topology		HB-MMC	
Device		IGBT	

Table 1.4: Existing offshore HVDC systems - HelWin and SylWin projects [29][116][117][118][113]

1.5 Future trends and conclusions

The MMC is the dominant topology for the above-mentioned projects. In the meantime, IGBT remains the only turn-off device used in such HVDC converter-stations. Throughout the HVDC projects in operation and the future projects of offshore wind-farms, it can be seen that the power rating is globally going higher, with a limitation due to the maximum voltage rating of HVDC XLPE cables. In the next years HVDC offshore projects could temporarily adopt mass-impregnated cables to increase the transmitted power, as in the case of the ±525 kV/1400 MW/623 km HVDC link between Germany and Norway, Nordlink [65][120]. Such realizations show that beyond challenges related to the installation of offshore wind-farms in deep water, MMC-based HVDC technology provides a wide range of solutions.

From a semiconductor point of view, IGCTs are favoured by its SCFM and its higher reliability compared to IGBTs. In the meantime, they could facilitate the development of HVDC systems as described in the previous paragraph, since they benefit from large current ratings and higher blocking voltage capabilities. However, the use of IGCTs in HVDC converter-stations implies a new design of the MMC SMs, which is initially determined by volume and fault concerns. Consequently, the second chapter focuses on the design of the whole HVDC link, as the

technology of the semiconductors does not only affects the efficiency of the converters, but also the protection strategies for the different fault cases.

Chapter 2

Design of the HVDC link

2.1 Design of the IGCT-based sub-modules

2.1.1 Selection of the topology

The modular multilevel converter is a generic topology, as its global operation and its behaviour in case of fault are defined by the topology of its SMs. Many topologies of SMs have been proposed in the literature [121]: it comes from the fact that an SM is an elementary VSC, then standard topologies such as the half-bridge, the full-bridge, but also the double-clamp [122], the flying capacitor and 3-level neutral-point clamp type commutation cells are compatible with MMC's operation. However, it is more relevant to keep the SM as basic as possible: for instance the half-bridge SM leads to the lowest semiconductor losses [123] with a minimum number of components and the simplest control strategy.

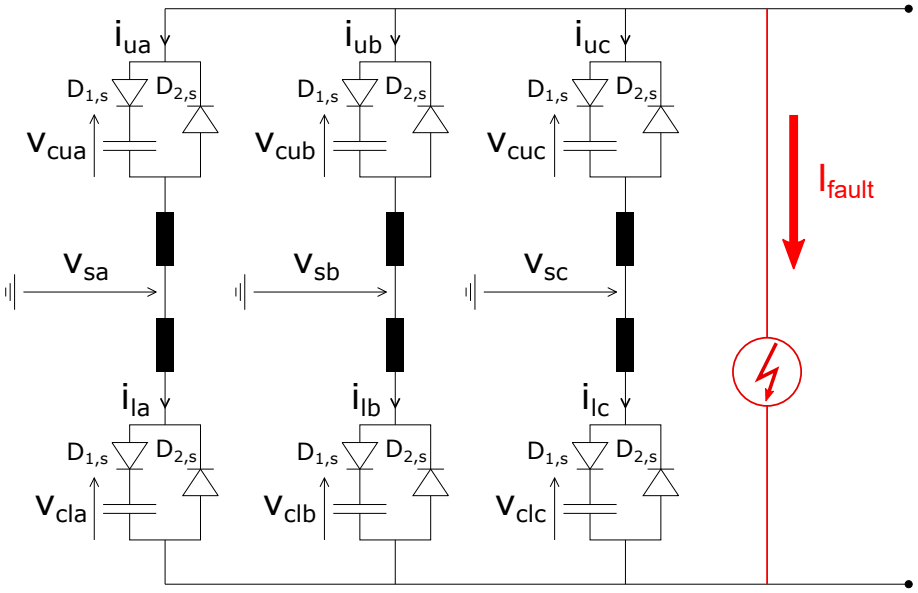


Figure 2.1: Equivalent schematic of an MMC with half-bridge SMs during DC fault after blocking the controllable devices, without protection material, $D_{1,s}$ and $D_{2,s}$ are respectively the N diodes D_1 and D_2 connected in series

On the other hand, full-bridge and double-clamp SMs have inherent DC fault blocking capability: this property well appreciated in HVDC is obtained by reversing the polarity of the SM outputs, which permanently interrupts the transfer of power from the AC grid to the DC

grid in case of DC-side fault [124]. On the contrary, an MMC with half-bridge SMs behaves like an uncontrolled rectifier during DC fault [125] as shown in Figure 2.1. It implies that the use of half-bridge SMs requires complementary protections. With this in mind, a comparative study has shown that half-bridge SMs lead to the highest efficiency even by considering the losses of the DC circuit-breakers [126], compared to an MMC using full-bridge SMs.

2.1.2 Sub-module failure, protection and redundancies

2.1.2.1 IGBT sub-module

All the SMs of the same arm are connected in series: in case of SM failure, the risk is to end up with a bad ohmic contact between the terminals, or even worse, an interruption of the current flow, which is inconceivable. This is likely to happen with IGBT power modules: as seen in 1.3.1.2 wire-bonded IGBT modules are unable to provide a stable and reliable short-circuit in case of failure. Besides, they may damage other parts of the converter in case of explosion. Therefore a bypass contactor must be connected at the terminals of the SM to properly disable it, which enables a continuous operation of the converter even after a SM failure [40]. As proper management of SM failures is a major concern, IGBTs with SCFM and a press-pack packaging are preferred: Hitachi ABB has been one of the first manufacturers to use it [127]. Rongxin Power Electronic (RXPE) benefits from this feature with Toshiba's IEGT [128], whereas Siemens may select Infineon's last generation of PPIs [63] for its prospective sub-modules.

In case of external fault such as DC fault or AC-side fault, semiconductors experience important surge currents before the protections take action. The controllable devices are blocked [124], which leaves the diodes into conduction mode with fault currents that can reach ten times the nominal values [129]. Once again the packaging of the semiconductor devices is involved in the management of this kind of event; diodes integrated with IGBTs have smaller surge-current integrals (I^2t) than individual devices. In the case of wire-bonded IGBT modules and PPIs, a press-pack thyristor is added in parallel of the lower diode. This thyristor is fired to deviate most of the current that should have flowed in the diode, thanks to its very-low on-state voltage [31]. On the contrary, the use of discrete press-pack diodes allows to withstand the surge currents without any additional device [128]. Figure 2.2 shows an IGBT SM with the additional components necessary to handle the different fault cases.

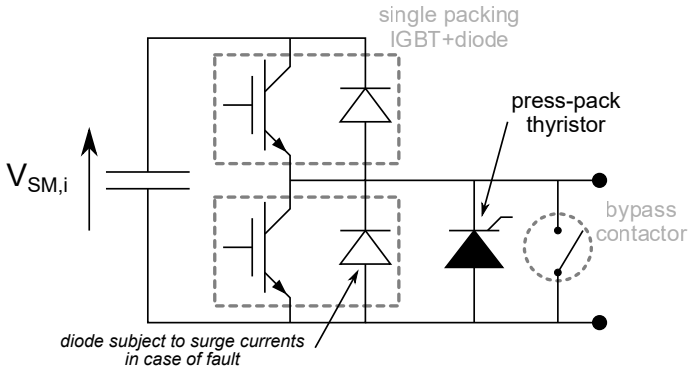


Figure 2.2: IGBT-based SM with a press-pack thyristor, to withstand fault currents, and a bypass contactor

2.1.2.2 IGCT sub-module

As developed in 1.3.3, IGCT's SCFM is stable and does not lead to external damage, considering that the assembly is able to withstand the electrodynamic efforts. Moreover, the management

of a short-circuit within the SM is safer with IGCTs than with IGBTs; for two different reasons [59]:

- In case of SM failure, the short-circuit current depends on the inductance of the commutation path, which is much higher with an IGCT thanks to the di/dt choke. Consequently, the maximum short-circuit current is much smaller with an IGCT, reducing both thermal and mechanical stresses.
- IGCT's on-state voltage remains low whatever the forward current, about a few volts (for instance 8 V at 30 kA for an IGCT 5SHY 55L4500). On the other hand, an IGBT desaturates, thus entering in the linear region as presented in 1.3.1.2, which leads to a huge dissipation of energy.

These considerations lead to a different protection strategy, Figure 2.3 shows that a press-pack thyristor is connected in anti-parallel with the commutation cell. This bypass thyristor has a different function than in the previous case. If a failure is detected, it is fired to take over the short-circuit current, causing the short-circuit failure of the bypass thyristor itself for a wide range of initial capacitor-voltages [98]. The thyristor ends in stable short-circuit with a voltage drop of a few volts as expected [59], providing a safe bypass to the SM and ensuring continuity of operation. This SM topology has the advantage of reducing the number of additional protections, thus reducing the cost and the volume of the SM as well. The removal of the bypass contactor with its dedicated control also improves the reliability of the SM, since these elements have failure rates comparable to those of an IGCT [60]. This protection technique has also proven to be valid with PPIs [130]. However, as aforementioned, the short-circuit currents are more important due to the lower inductance of the commutation path.

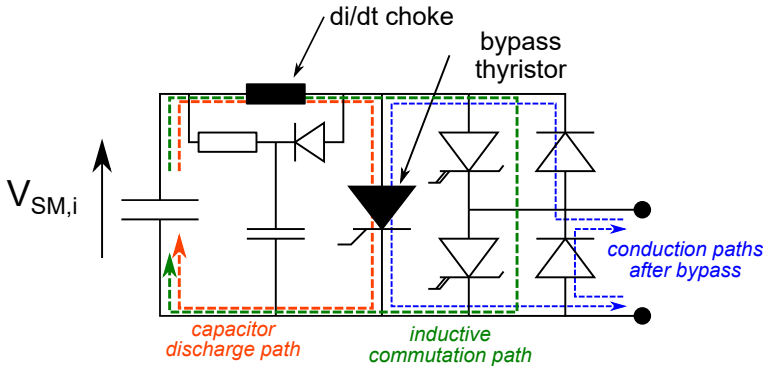


Figure 2.3: IGCT-based SM with a single bypass thyristor to protect the SM

Following the same concept, it has been proposed to induce the failure of the IGCT in order to bypass the SM [131]. In order to realize it, a specific design of the IGCT is necessary, to obtain a regular breakdown at the selected voltage. SCFM is obtained after a surge-current integral of 149.3 MA^2s without outer damage, which shows the capability of simplifying the design of the SM even more with IGCT.

2.1.3 Auxiliary circuits for IGCT

As exposed in 1.3.3.3, an additional circuit is required to use IGCT and diode in the same commutation cell. The simplest and the most common structure is an RCD snubber (also called clamp circuit) with a di/dt choke. This circuit increases the volume of the SM and it dissipates energy, so the replacement of the clamp circuit with an other auxiliary circuit could be relevant.

2.1.3.1 Flyback-type snubber

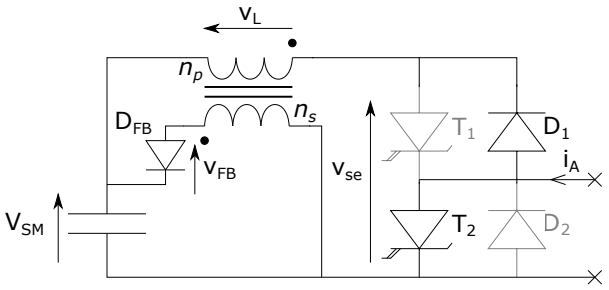
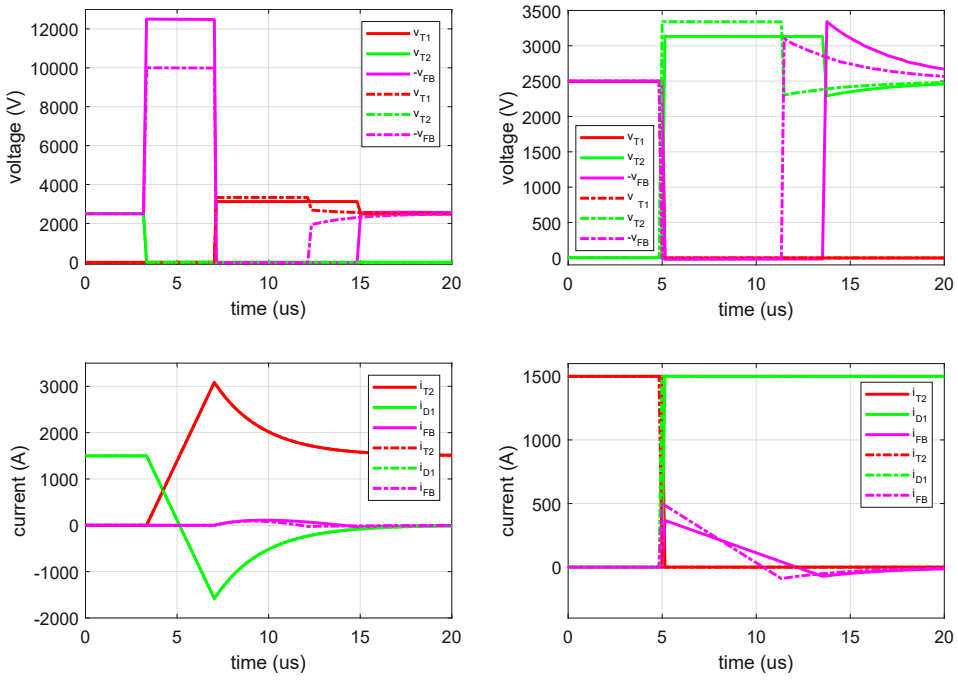


Figure 2.4: Flyback-type di/dt snubber for an IGCT half-bridge SM

The main drawback of a simple di/dt choke with a clamp circuit is the dissipation of energy in the resistor R_{cl}. To figure out this issue, a flyback-type di/dt snubber has been proposed [132]. This solution, presented in Figure 2.4, allows to retrieve the energy stored in the inductor, here the magnetizing inductance of the transformer, instead of dissipating it. The flyback diode only conducts when the voltage v_L exceeds $-\frac{n_p}{n_s}V_{SM}$. In the meantime, this solution remains interesting because of its limited number of components.



(a) Diode turn-off (b) IGCT turn-off

Figure 2.5: Waveforms during commutations, $\frac{n_s}{n_p} = 4$ (solid line) and $\frac{n_s}{n_p} = 3$ (dotted line), V_{SM}=2500 V, i_A=1500 A

Figure 2.5 shows the waveforms of the flyback-type di/dt snubber for a DC current of 1.5 kA, with two different turns ratios. The magnetizing inductance is constant and equal to 3 μH. When D_1 turns off, i_{T2} quickly increases: di/dt is limited by the magnetizing inductance. During this first phase, D_1 and T_2 both conduct, it means that the whole DC link voltage is withstood by the primary winding of the transformer, $v_L = V_{SM}$. Consequently, $v_{FB} = -\left(\frac{n_s}{n_p} + 1\right) V_{SM}$, as shown in Figure 2.5(a) v_{FB} exceeds 10 kV for the two different turns ratios. When the peak

reverse recovery current I_{rr} is reached, i_{T2} starts to decrease: the corresponding di/dt triggers the flyback transformer, $v_{se} = V_{SM}\left(1 + \frac{n_p}{n_s}\right)$ and $v_{FB} = 0$. After a few microseconds the diode D_{FB} turns off, $v_L = 0$ and $v_{FB} = -V_{SM}$.

When T_2 turns off (Figure 2.5(b)), a high negative di/dt appears in the transformer: the voltage v_L exceeds $-\frac{n_p}{n_s}V_{SM}$ which turns on D_{FB}. As soon as D_{FB} conducts, $v_{se} = V_{SM}\left(1 + \frac{n_p}{n_s}\right)$, during this period the whole energy in the magnetizing inductance is transferred to the secondary winding. Because of the reverse recovery of D_{FB}, i_{FB} becomes negative: when the peak reverse recovery current is reached v_{se} falls down slightly below V_{SM}, and converges towards V_{SM} after a few microseconds.

It can be observed that low turns ratios make commutations faster, with a smaller overvoltage for diode D_{FB}. However, v_{se} is higher which means that the failure rate of the main semiconductors is increased. This principle of operation shows the limits of a flyback-type di/dt snubber. The turns ratio $\frac{n_s}{n_p}$ must be properly chosen since a high turns ratio requires a higher voltage rating for the diode D_{FB}, whereas a low turns ratio leads to a high overvoltage for the main semiconductors. For instance, a turns ratio $\frac{n_s}{n_p}$ of 4 implies an overvoltage of 25% for the semiconductor and a voltage rating of 5 pu for the flyback diode.

To figure out these issues, particularly the high voltage stress of the flyback diode, it has been proposed to realize a series association of flyback converters. Then, the voltage stress of each secondary winding is divided by the number of flyback converters. A multi-winding flyback has been proposed as well [133]. The drawback of these solutions is that the number of components is increased while the current rating remains identical, since it is based on series associations. The overall volume of these flyback-type snubbers unavoidably increases, compared to a traditional clamp circuit with a single di/dt choke.

2.1.3.2 Auxiliary Resonant Commutated Pole (ARCP) circuit

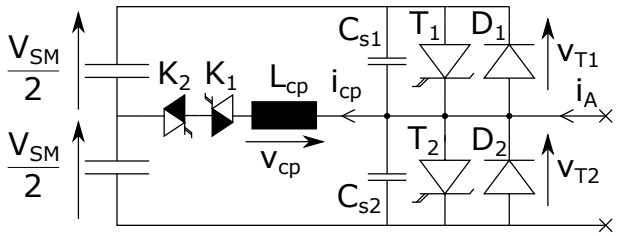


Figure 2.6: Auxiliary Resonant Commutated Pole (ARCP) circuit; the four-quadrant device is realized with two RC-IGCTs here

Presentation, control Figure 2.6 shows the Auxiliary Resonant Commutated Pole (ARCP) circuit [134] with IGCTs, where the auxiliary pole is composed of a four-quadrant device and an inductor. It is used during diode turn-off to limit di/dt, while the capacitors C_{s1} and C_{s2} allow a control of dv/dt, thus ensuring soft switching.

Figure 2.7 shows the general control strategy that can be applied to the semiconductors. When a turn-on order is sent by the controller, the circuit does not modify the output signal while the cathode-anode voltage is above a certain threshold V_{th}, which is a few tens of volts. The zero voltage detection is an important element to properly manage the ARCP circuit, as it allows the zero-voltage switching of IGCT. Regarding the threshold voltage, 20-30 V are typical

values [135][136]. The control of the auxiliary devices can be realized with a simple pulse, triggered by the rising edges of the control signals, as presented in Figure 2.8.

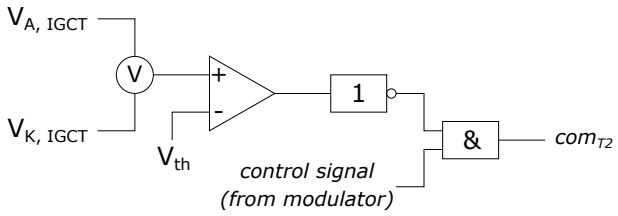


Figure 2.7: Control of T_2 to match ARCP's requirements (i_A>0)

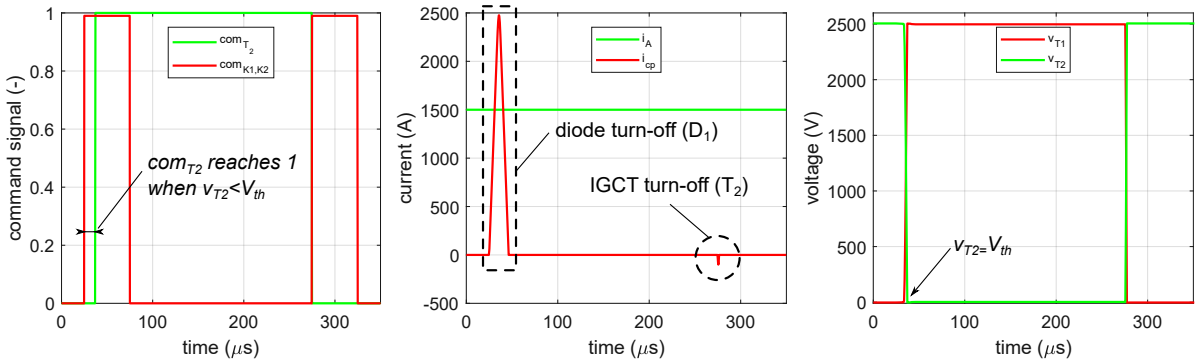


Figure 2.8: Evolution of the commutation orders (com_{T2} for T_2 and $com_{K1,K2}$ for the auxiliary switches), the arm-current, the auxiliary pole current i_{cp}, v_{T1} and $_{T2}$, over a switching period (500 μs for illustration purposes only), V_{SM}=2500 V, i_A=1500 A

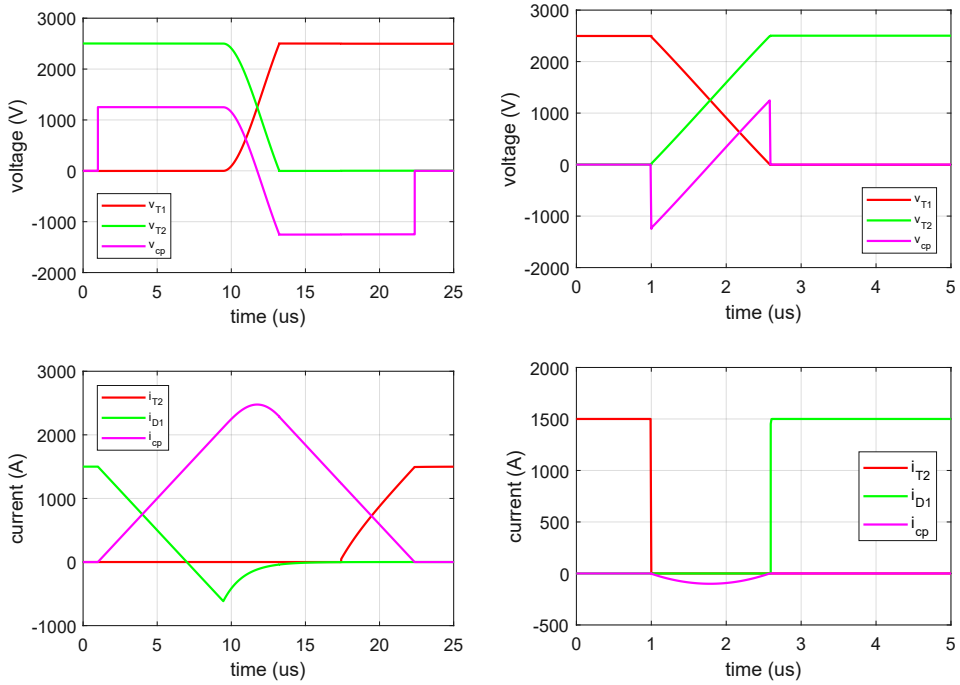
Principle of operation during commutations The circuit has the following behaviour:

- An IGCT turn-off is characterized by the charge of its dedicated capacitor and the discharge of the complementary capacitor. This soft transient leads to smaller power losses [137]. The energy exchange between the capacitors does not require the activation of the auxiliary circuit if the arm-current is high enough [134], otherwise the auxiliary circuit is able to increase the IGCT turn-off current and thus the amount of involved energy. The corresponding waveforms, for a positive arm-current, are presented in Figure 2.9(b).

- A diode turn-off is initiated by an activation of the auxiliary circuit, either K_1 of K_2 is turned on depending on the sign of the current. The current through the diode is deviated to the auxiliary pole: the purpose is to store energy in the auxiliary inductor L_{cp}. As soon as the diode is reverse-biased, the exchange of energy between the two capacitors C_{s1} and C_{s2} occurs: a resonant effect is obtained with the auxiliary inductor L_{cp}. In the end, the opposite IGCT is turned on at zero voltage, and the auxiliary switch turns off at zero current after the current zero crossing of i_{cp} through the auxiliary diode. The corresponding waveforms, for a positive arm-current, are shown in Figure 2.9(a).

The ARCP circuit has many interesting properties. On the contrary of many auxiliary circuits, it only conducts during a short portion of the switching period. It leads to smaller thermal constraints for the auxiliary switch and the resonant inductor L_{cp}. Furthermore, IGCT turn-on losses are reduced compared to its classic operation because turn-on occurs at low voltage. However, this gain is mitigated since IGCT turn-on losses are generally negligible. Diode turn-off is softer, corresponding power losses are expected to be reduced by 75% [137]. IGCT turn-off is

also softer, because the parallel capacitors reduce the peak power during commutation time. In the end, it has been proven that related losses are reduced by 50% [137]. The auxiliary switches operate under zero-current switching (ZCS), which significantly decrease their total power losses. Compared to the RCD snubber used with a di/dt choke, there is no energy loss, which leads to a meaningful reduction of the SM power losses.



(a) Diode turn-off (D_1, i_A>0) (b) IGCT turn-off (T_2, i_A>0)

Figure 2.9: Waveforms during commutations, IGCT in red, diode in green, auxiliary inductor in magenta, V_{SM}=2500 V, i_A=1500 A

It has been demonstrated that the additional cost of an ARCP circuit with IGCT is written off within less than a year [135] for offshore wind-farms applications, which is cost-effective for a system supposed to operate between 25 years and 30 years. Another comparison points out that the ARCP circuit is cheaper than the clamp circuit [136], the larger number of devices is counterbalanced by the much smaller current ratings of the components. The reasonable number of devices in the ARCP circuit ensures that the overall reliability of a MMC SM is not deteriorated.

Sizing of the ARCP circuit An ARCP circuit has been designed with the following constraints reported in Table 2.1. The resulting electrical stresses have been gathered in Table 2.2.

Power	$\mathbf{V_{DC}}$	$\mathbf{V_{SM}}$	$\mathbf{m_a}$	$\mathbf{D_1/D_2}$
1 GW	±320 kV	2500 V	0.85	5SDF 28L4520

Table 2.1: Sizing parameters chosen for the ARCP circuit

Concerning the inductor, it can be observed that the RMS current is very low, 0.06 pu compared to the arm-current. Nevertheless, the maximum current is important because the reverse recovery current adds to the arm-current in the auxiliary pole during diode turn-off.

Component	**L_{cp}**	**K_1 & K_2**	**C_{s1} & C_{s2}**
Value	4.5 μH	-	250 nF
max. voltage	$\pm$1250 V ($\pm$0.5 pu)	$\pm$625 V ($\pm$0.25 pu)	2500 V (1 pu)
RMS current	66 A (0.07 pu)	66 A (0.07 pu)	8 A (0.01 pu)
max. current	3020 A (1.73 pu)	3020 A (1.73 pu)	1900 A (1.09 pu)

Table 2.2: Electrical stresses of the ARCP circuit, per unit system is related to V_{SM} and i_a

Thermal constraints are reduced for the auxiliary switches according to the RMS current. The main constraint is the maximum current that has to been withstood, which favours the use of a thyristor-based solution. Thanks to the middle-point connection the maximum voltage is divided by two, so the auxiliary switches are significantly less stressed than the main switches.

Comparison with the traditional clamp circuit, conclusions Table 2.3 summarizes the electrical characteristics bound to the different components of the traditional RCD clamp circuit and the ARCP circuit. It can be noticed that the inductance for the ARCP circuit is higher than for the RCD clamp circuit, because the maximum peak current is intentionally limited to 3 kA. In the meantime, the RMS current is divided by more than 10 for the inductor of the ARCP circuit, while the insulation voltage is divided by two. The inductor L_{cp} (of the ARCP circuit) is expected to be more compact than the inductor L_{cl} (with the RCD snubber). The ARCP circuit needs much smaller capacitance, 2x250 nF against 20 μF with the clamp circuit, for the same voltage ratings. Concerning the switches, the diode of the clamp circuit is replaced by at least two controlled semi-conductors, which leads to different possibilities:

1. Two thyristors in parallel, this solution is the simplest and the most relevant considering the operation of the ARCP circuit. Controlled turn-off is not necessary, since ZCS is achieved. These thyristors have to be fast enough to turn-off within a few tens of microseconds, typically less than 50 μs, to be compatible with MMC's operation.

2. Two reverse-conducting IGCTs in series, this solution leads to a slight increase in conduction losses and higher complexity because of the turn-off circuit.

Consequently, the ARCP circuit can compete with the traditional clamp circuit for HVDC-MMC applications as it reduces the power losses and potentially the volume of the SM with a proper mechanical arrangement.

Component	**Inductor**		**Switch**		**Capacitor**		**Resistor**
Circuit	RCD	ARCP	RCD	ARCP	RCD	ARCP	RCD
Value	3 μH	4.5 μH	-	-	20 μF	250 nF	0.33 Ω
Quantity	1	1	1	**2**	1	2	1
max. voltage	2500 V	$\pm$1250 V	2500 V	$\pm$625 V	2840 V	2500 V	340 V
RMS current	715 A	66 A	49 A	66 A	30 A	8.3 A	38 A
max. current	1910 A	3020 A	1750 A	3020 A	1750 A	1900 A	1030 A

Table 2.3: Comparison of the electrical stresses between the RCD snubber with its di/dt choke and the ARCP circuit

2.2 Design of the converters

2.2.1 Selection of the passive components in an HVDC-MMC

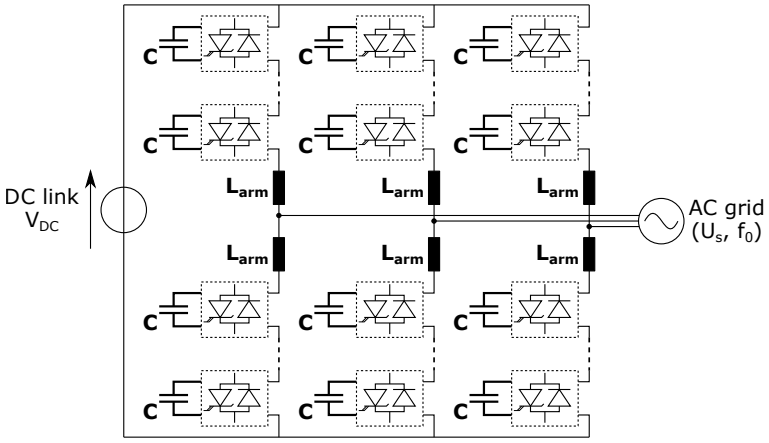


Figure 2.10: Passive components of the MMC, the AC grid is characterized by a phase-to-phase voltage $U_s = \sqrt{\frac{3}{2}} m_a \frac{V_{DC}}{2}$ and a frequency f_0, m_a being the modulation index

As shown in Figure 2.10, an MMC based on half-bridge SMs comprises 6N identical capacitors and 6 arm inductors. Almost all the energy stored by the converter is present in the capacitors.

2.2.1.1 Capacitors

The amount of energy stored in the MMC, per MVA or per megawatt, is discussed in many papers. In an SM, the volume of the capacitor can be about 50% of the total volume [48], so the capacitance mostly defines the volume of the converter. It explains why the trend is to decrease the energy storage requirements: it allows a reduction of the site area and it is less expensive.

Film capacitors are generally limited to a peak-to-peak voltage ripple of 20% of the rated DC voltage. Besides, a safety margin is taken into account between the rated DC voltage and the maximum voltage, to ensure a satisfactory lifetime. In an MMC, the capacitor-voltage ripple has two origins: the first one is that the natural operation of the converter requires a periodic energy exchange with the SMs which unavoidably leads to an energy variation. Assuming that all SMs are balanced, i.e that the switching frequency is infinite, the capacitance C per SM to ensure a voltage ripple inferior to Δv_c follows:

$$C = N \frac{S_{max}}{3 V_{DC}^2 \omega_0 \Delta v_c} \frac{2}{m_{a,min}} \left(1 - \left(\frac{m_{a,min} p_{f,min}}{2} \right)^2 \right)^{\frac{3}{2}} \tag{2.1}$$

where S_{max} is the maximum apparent power, ω_0 is the grid pulsation, $m_{a,min}$ is the minimum modulation index, and $p_{f,min}$ is the minimum power factor.

Nevertheless, the switching frequency cannot be infinite, or even high enough to consider this relation accurate enough: the capacitor voltages deviate from the natural capacitor voltage $V_{SM,\,nat}$[138], as shown in Figure 2.11. It can be concluded that since the average of all the capacitor voltages is equal to the natural capacitor voltage, the effective capacitor voltage ripple is necessarily higher than estimated with (2.1), or equal if specific predictive algorithms are used [139].

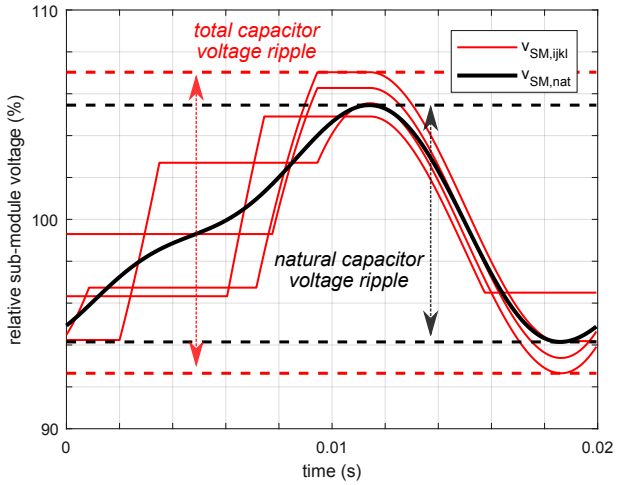


Figure 2.11: Evolution of four capacitor voltages among 256 SMs over a grid period; $v_{SM,nat}$ is the capacitor voltage for an infinite switching frequency

A maximum average peak-to-peak voltage ripple of Δv_c=14% is selected. The voltage ripple due to modulation adds, which can represent up to 40% of the average voltage ripple. This result strongly depends on the modulation strategy and the switching frequency [140]. A capacitance high enough is retained in order to experiment the use of different modulation strategies, without limitations due to the maximum capacitor-voltage ripple. Thus, a maximum total peak-to-peak voltage ripple of 18% is expected. It gives a stored energy of 45.5 kJ/MVA which is slightly superior to the average values in the literature, about 35-40 kJ/MVA [33][47], but remains in the general range 30-70 kJ/MVA [141][142].

2.2.1.2 Arm inductors

The sizing of arm inductors is more complex as it involves multiple considerations. Their primary role is to allow the control of the arm-currents. Indeed, the arm is strongly capacitive and requires an inductor in series to act as a current source to properly interconnect the AC grid with the DC bus.

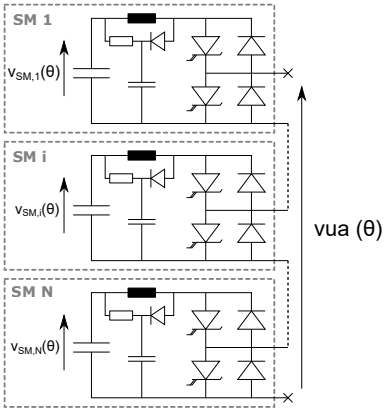
The second concern is trickier: the internal impedance of the converter must be high enough to reduce the harmonics of the circulating currents [123]. It has been clearly identified as a potential threat for the semiconductor devices as it increases the RMS arm-currents [143]. A practical realization, where the second and the fourth harmonics are passively amplified, is presented in [144]. Analytic expressions of the resonant frequencies implying the SM capacitance have been formulated [145], they can lead to the simplified criterion (2.2):

$$L_{arm} \geq \frac{1}{4C\omega_0^2} \tag{2.2}$$

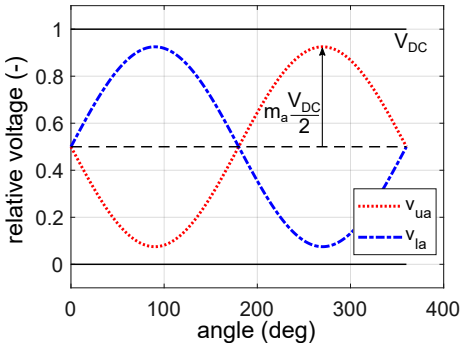
(2.2) is a sufficient condition to ensure that the harmonics of the circulating currents are damped, thus avoiding resonant effects whatever the operating conditions. A third issue is the limitation of fault currents, one common criterion mentioned is the maximum fault current rate of rise [146][40], about some tens of amps per microsecond. The criterion (2.2) includes it. Besides, DC inductances are systematically added to fulfil requirements from the protection systems [147], particularly when DCCBs are used [148]. Finally an arm inductance of 0.19 pu is obtained, close to the range of values met in the literature (0.05 pu - 0.18 pu [33][29]).

2.2.2 Choice of the number of sub-modules per arm

2.2.2.1 Voltage rating of a SM



(a) Upper arm with IGCT-based half-bridge SMs



(b) Upper and lower arm-voltages of phase a with half-bridge SMs

Figure 2.12: Upper arm of phase a and arm-voltages for phase a, in an MMC using half-bridge SMs

The relation between the DC link voltage V_{DC}, the SM nominal voltage V_{SM} and the number of SMs per arm depends on the topology of the SMs themselves [123]. Figure 2.12 shows that the arm-voltage v_{ua} must remain within two boundaries, 0 and V_{DC}. Besides (2.3) can be demonstrated:

$$v_{ua}(\theta) = \frac{V_{DC}}{2}\left(1 - m_a \sin(\theta)\right) \tag{2.3}$$

where $\theta = \omega_0 t$ is the phase angle of the grid voltages, and ω_0 the grid pulsation. Knowing that the modulation index m_a is inferior to 1, (2.4) can be deduced from (2.3):

$$NV_{SM} \geq V_{DC} \tag{2.4}$$

V_{SM} is directly related to the voltage ratings of the semiconductor devices in the SM. Besides, the SM voltage must be lower than the maximum rating due to reliability issues: cosmic ray leads to unacceptable FIT rates when the blocking voltage is too high [105]. Hitachi ABB typically defines 100 FIT for a device withstanding approximately 62% of the maximum voltage rating. Moreover, the capacitor-voltage ripple must be considered: for a maximum average-to-peak voltage ripple of 12%, the nominal SM voltage becomes about 55% of the maximum semiconductor voltage rating. Regarding 10 kV IGCTs, it has been shown that the turn-off SOA capability can be more restrictive than the criterion based on the FIT rate [149]. Even if a failure rate of 100 FIT is obtained at a voltage of 6.6 kV, a maximum voltage of 5.3 kV must be retained to ensure proper turn-off, with currents up to 1.8 kA, at a junction temperature of 125°C. Consequently, the maximum SM voltage is decreased to 4700 V, thus considering the capacitor-voltage ripple. Table 2.4 presents the maximum SM voltages and the nominal SM voltages, for the available IGCT's voltage ratings, i.e. 4500 V, 6500 V and 10 000 V.

2.2.2.2 Choice of the number of SMs

Table 2.4 and (2.4) lead to the minimum number of SMs per arm. These values have been reported in Table 2.5. As presented in 1.1.1.2, 320 kV, 525 kV and 600 kV voltage levels are based on existing products, having different technology readiness levels. An intermediate voltage level, 460 kV, has been intentionally introduced to compare semiconductors having different voltage ratings. This comparative study is carried out in the fourth chapter. As seen in 2.1.2, SM failure

may occur and must be considered in the design of the converter. The failure of an SM has an important consequence on the arm: since the total available voltage must remain identical, it naturally leads to a rise in the SM voltages [98]. Such a behaviour is concerning, as it can decrease the capacitor lifetime and increase the failure rate of the semiconductor devices. To figure it out, it is mandatory to consider additional SMs during the assembly of the converter: between 5% and 10% of the number of SMs per arm is forecast [150] to keep the maximum SM voltage reasonable, while allowing a certain number of faulty SMs. More details about the management of the redundant SMs are given in [33].

V_{DRM}	maximum SM voltage	V_{SM}
4500 V	2800 V	2500 V
6500 V	4000 V	3600 V
10 000 V	5300 V	4700 V

Table 2.4: Maximum and nominal SM voltages for the different IGCT's voltage ratings

V_{DC}	±320 kV			±460 kV			±525 kV			±600 kV		
V_{DRM} (kV)	4.5	6.5	10	4.5	6.5	10	4.5	6.5	10	4.5	6.5	10
min. N	256	178	137	369	256	196	420	292	224	482	335	256

Table 2.5: Minimum number of SMs per arm for different DC link voltages and different semiconductor voltage ratings, from the criterion retained in Table 2.4

Component	Unit FIT	Quantity	Total FIT
IGCT	100	2	200
gate unit	200	2	400
diode	100	2	200
clamp circuit	45	1	45
di/dt choke	10	1	10
bypass thyristor	20	1	20
gate unit	100	1	100
avalanche device	20	1	20
cell capacitor	91	1	91
total FIT per SM		1086	

Table 2.6: FIT rate per component of a MMC SM [60]; mechanical and hydraulic parts have not been included

In practice, this additional number of SMs has to be calculated. Table 2.6 summarizes the list of electrical components in a SM with their corresponding FIT rates, where the reference value of 100 FIT has been taken for IGCTs and diodes. For the SM capacitor, a model from the manufacturer AVX has been considered where the FIT rate takes into account the temperature of the hot spot, the maximum SM voltage and environment factors. The total per SM is 1086 FIT.

Then, it is possible to obtain the mean time between failures (MTBF) of the arm as reported in Table 2.7. It shows that a larger number of SMs per arm induces a smaller MTBF, since

the number of components is more important. For a yearly scheduled maintenance, at least two additional SMs are required with 4.5 kV devices whereas only one is necessary with 6.5 kV devices and 10 kV devices. It should be noted that the amount of additional SMs to use is necessarily underestimated, since the other elements of the SM such as mechanical and hydraulic parts have not been taken into account. It can be concluded that the nominal SM voltages specified in Table 2.4 are consistent regarding reliability aspects. The semiconductor devices do not significantly decrease the MTBF of the converter. Furthermore, using a high number of SMs can lead to additional operating expenditure (OPEX) as the number of SMs supposed to fail increases, thus affecting maintenance costs.

Design	total FIT per arm	MTBF of an arm
N=256/V_{SM}=2500 V	278 000 FIT	149 days
N=178/V_{SM}=3600 V	193 000 FIT	215 days
N=137/V_{SM}=4700 V	148 000 FIT	280 days

Table 2.7: FIT rates and MTBFs of an arm with asymmetric IGCTs and different numbers of SMs

2.3 Behaviour of the HVDC link during faulty operation

It has come out in 2.1 and 2.2.1.2 that fault conditions must be investigated in order to validate any design of the converter-stations. Then, the equipments used for protection are paramount as they define the thermal and electrical stresses during fault, as well as the HVDC cables which affects the interactions between the two converter-stations during fault condition.

2.3.1 Circuit-breakers and HVDC cables

It has been seen in 2.1.1 that an MMC based on half-bridge SMs cannot break currents resulting from a DC-side fault, implying that the converter has to rely on additional protections to be isolated in case of such failure. The cases of AC circuit-breakers (ACCBs) and DC circuit-breakers (DCCBs) are considered.

2.3.1.1 AC circuit-breakers

The use of ACCBs is generalized for AC grids, besides these circuit-breakers have proven to be compatible with HVDC links. Many fault cases have been investigated during the commissioning of the Caprivi link: when the AC lines trip, the superior dynamic of the HVDC link enables frequency and voltage stabilization in a few seconds [151].

However, this solution appears to be less relevant in case of a DC fault. An ACCB requires several grid periods prior to utterly break the current (up to 100 ms [152][153]), during which the converter is exposed to the fault current. LCCs are able to withstand fault currents thanks their high inductive behaviour [36], combined with the control of the thyristors [38]. Nevertheless, fault currents increase quicker with VSC-HVDC converters and it is not possible to control them with half-bridge SMs [154].

An ACCB can be modelled in a simple way, as its response-time is very long compared to its turn-off dynamic: a TRIAC with a delayed control signal is an excellent representation. Figure 2.13 shows the equivalent circuit of the converter after the tripping of the ACCBs, resulting from the equivalent schematic of Figure 2.1 presented in 2.1.1. It can be observed that arm-currents are not immediately interrupted. They circulate through the fault path and the

diodes $D_{2,s}$ which induces additional thermal stresses for the semiconductors. Another concern is that the tripping of the ACCBs in one converter-station cannot isolate a DC fault. All the AC grids directly connected to the HVDC link must be disconnected. Consequently, this protection strategy is very restrictive for future multi-terminal HVDC systems [150].

2.3.1.2 DC circuit-breakers with fault-current limiters

DCCBs aims at figuring out the aforementioned issues of ACCBs: long switching times and lack of flexibility. Each pole is equipped with a DCCB as it must be disconnected in case of fault to fully isolate the converter-station.

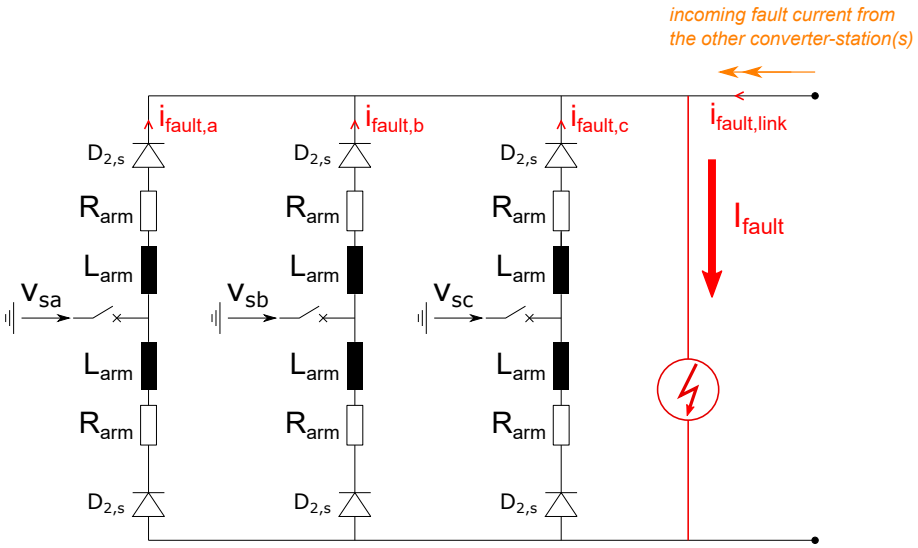


Figure 2.13: Equivalent schematic of the converter-station after DC fault detection and tripping of the ACCBs. R_{arm} represents the power losses in the arm, mainly due to the conduction losses of the semiconductors.

Technologically speaking, a DCCB is more complex to realize as there is no natural zero current crossing: it must withstand high overvoltages when it breaks the full fault current [153] as well as operate quickly to limit the prospective fault current [155]. In the meantime, it must generate negligible losses in normal operation. Different families of DCCBs exist; hybrid and active current injection circuit-breakers exhibit excellent performances with opening times inferior to 10 ms and breaking current capabilities of about 15 kA [156]. Hybrid circuit-breakers combine the advantages of solid-state breakers and mechanical breakers: electric arc, contact erosion and bouncing effects are removed, while a higher electric strength is obtained [157]. The DCCB presented in Figure 2.14 has been retained. It contains a main current path, a commutation path and an energy absorption path, composed of metal-oxide varistors (MOVs), which dissipates a significant amount of the system's magnetic energy and limits the transient interruption voltage (TIV).

During normal operation, the current flows through the main current path, which is generally composed of a low-losses mechanical switch and a power electronic switch. When a fault is detected, the power electronic switch opens which deviates the current in the commutation path. Then, the mechanical switch opens to protect the power electronic switch against the upcoming transient interruption voltage. The opening of the commutation path generates the TIV, which triggers the conduction of the MOVs. The deviation of the current from the main path to the commutation path and the opening of the commutation path are modelled by a

pure delay, since it is the internal operation of the circuit-breaker: A delay of a few milliseconds [158] is reasonable to represent the internal commutation time of the DCCB. A MOV can be modelled by a series association of a constant voltage source and a non-linear resistor thus obtaining a logarithmic approximation of the MOV's v-i characteristic. More details about the characteristics, the modelling and the selection of MOVs can be found in [159].

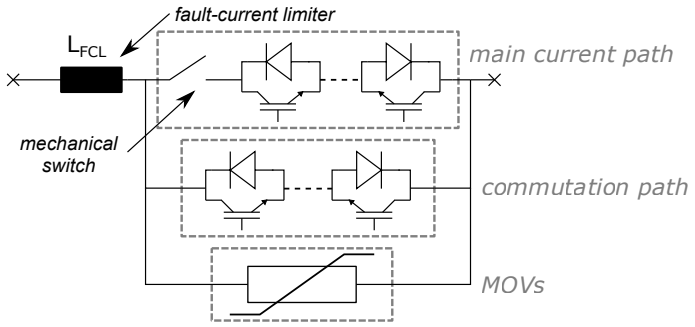


Figure 2.14: Components of a hybrid DCCB; a low-losses main commutation path, a fast static commutation path, and metal-oxide varistors

A fault-current limiter, which consists of an inductor L_{FCL}, is added in order to mitigate the maximum current derivative during fault. It ensures that the DCCB remains in its rated current capability. A maximum rate of rise of 10 kA/ms is typical [160] for the DC link current. From this criterion, the arm inductors of the closest converter should be taken into account: the circulating component of arm-currents sees an inductance of $2xL_{arm}$, so the total inductance seen from the DC link is $\frac{2}{3}L_{arm}$. Thus, the fault-current limiter should have the following value:

$$2L_{FCL} = \frac{V_{DC}}{\left(\frac{di_{DC}}{dt}\right)_{MAX}} - \frac{2}{3}L_{arm} \tag{2.5}$$

2.3.1.3 HVDC cables

Modelling of HVDC cables is optional for steady-state analysis. However, it is paramount for transient phenomena study, since the properties of the HVDC cables influence the interactions between the two converter-stations.

Modelling with pi-sections Pi-sections [161] are a basic way to model DC cables. The relation between the number of pi-sections and the modelling error of the line has been shown to depend on the line's resonant frequency [162]. It presents the limits bound to pi-sections which are dedicated to modelling low-frequency phenomena. These limitations have been confirmed and a more accurate model, the FD-π model, has been proposed [161]. A comparison with the real impedance of an HVDC XLPE cable shows that resonances are damped, while the representation with pi-sections results in sharp variations at the resonant frequencies. Simulations using pi-sections are characterized by high-frequency ripples which are not realistic, because of the discrete resonant frequencies of the model.

Modelling with travelling wave theory Travelling wave theory lies in local equations instead of discrete passive components. This more accurate representation is chosen in a simulation software to avoid the drawbacks of pi-sections. The corresponding implementation in a simulation software is based on [163]. The characteristics of the HVDC cables, chosen for the study, are gathered in Table 2.8.

Name	Symbol	Value
Pole-to-ground capacitance per km	c_{cable}	0.2185 μF/km
Conductance per km	g_{cable}	0.055 μS/km
Inductance per km	l_{cable}	2.615 mH/km
Resistance per km	r_{cable}	11 mΩ/km

Table 2.8: Macroscopic characteristics of a 200 kV DC cable

2.3.2 Comparison between ACCBs and DCCBs in case of DC fault

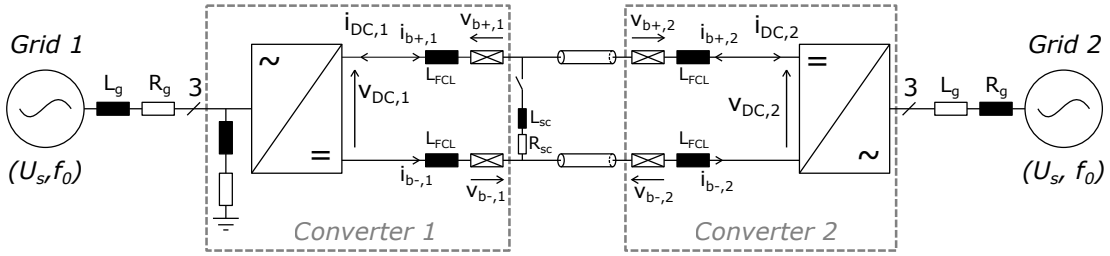


Figure 2.15: Detailed schematic of the HVDC link with DCCBs; U_s=220 kV and f_0=50 Hz

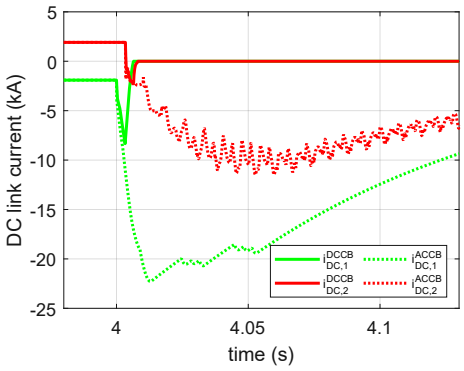
To reproduce a DC fault, a low-impedance path is created between the two poles of the HVDC link as shown in Figure 2.15. As explained in 1.1.2.2 a star-point reactor is placed to provide a ground reference. Four DCCBs are used but to avoid interferences in the waveforms, the tripping of the DCCBs in the positive poles of the two converters is voluntarily delayed by 7 ms, for the sake of the simulation only.

The system starts at the nominal DC link voltage $V_{DC,nom}$ of 400 kV with an active power of 800 MW. At t_0=4 s, when a steady-state operation is reached, the positive and negative poles of Converter 1 operating as a rectifier are short-circuited, as shown in Figure 2.15. It should be noted that this is a critical case of study for Converter 1: the DC link current already flows in the direction of the short-circuit, which increases the maximum fault current. The numerical values of the different passive elements, including the model of the short-circuit, the transformers and the fault-current limiters, are presented in Table 2.9. The value of the fault-current limiter is consistent with those reported the literature, which provides a wide choice of values with various criteria [148, 164, 160].

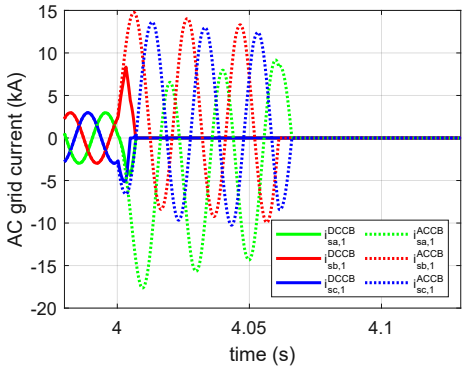
Name	Symbol	Value
Transformer leakage inductance	L_g	35 mH
Transformer series resistance	R_g	0.363 Ω
Short-circuit inductance	L_{sc}	100 nH
Short-circuit resistance	R_{sc}	1 mΩ
Fault-current limiter	L_{FCL}	22.5 mH
SM capacitance	C	10 mF
Arm inductor	L_{arm}	29 mH

Table 2.9: Characteristics of the short-circuit, the transformers, the DCCBs and the converter-stations

2.3.2.1 Waveforms and behaviour of the DC circuit-breaker



(a) DC link current - zoom - green for Converter 1, red for Converter 2, solid line for DCCBs and dotted line for ACCBs



(b) AC grid currents $i_{s,i}(t)$, $i \in \{a; b; c\}$, green for phase a, red for phase b and blue for phase c, solid line for DCCBs and dotted line for ACCBs

Figure 2.16: DC link current and AC grid currents during DC pole-to-pole fault with ACCBs (dotted lines) and DCCBs (solid lines)

Figure 2.16(a) shows that the fast opening-time of the DCCBs significantly reduces the constraints on the system: the peak DC link current is less than 10 kA with DCCBs, while it is greater than 20 kA with ACCBs. Besides, the duration of fault-limitation is much greater with ACCBs; Figure 2.16(b) shows that approximately 70 ms are required to open the three ACCBs of Converter 1. Even after the opening of the ACCBs, the fault is still not cleared because the short-circuit has created an inductive closed loop which allows the circulation of arm-currents, as explained in 2.3.1.1. It explains why a non-zero DC link current remains even after the opening of the ACCBs in Figure 2.16(a). The time-constant of this phenomenon is given by (2.6):

$$\tau = \frac{L_{arm}}{R_{arm}} = 106\,ms, \text{ with } \begin{cases} R_{arm} = 273\,m\Omega \\ L_{arm} = 29\,\text{mH} \end{cases} \tag{2.6}$$

This phase is critical because of its duration, which is another drawback of ACCBs: contrary to a converter fitted with DCCBs, fault-clearance takes several hundred milliseconds. The arm-currents slowly decrease as seen in Figure 2.17 and the energy is dissipated through the inductors' resistances and the diodes. Figure 2.16(a) also shows that the position of the short-circuit greatly affects fault currents: the DC link current of the rectifier (Converter 1) quickly rises, while the DC link current of the inverter (Converter 2) has a smaller rate-of-rise. This is due to the impedance of the DC cable, which attenuates and delays the effects of the short-circuit since Converter 2 is at D=200 km of the short-circuit.

Figure 2.18 shows voltages and currents of the two first DCCBs to open: the first one is located in the negative pole of Converter 1, the second is located in the negative pole of Converter 2. In the beginning, the DC link current of Converter 1 rises quickly, at a rate mostly determined by the fault-current limiters L_{FCL}. The first DCCB limits the fault after Δt=3.27 ms and breaks a current of 8.34 kA. This time is the sum of the detection delay, 271 μs and the internal current commutation time (ICCT) of the DCCBs, assumed equal to 3 ms. It induces the TIV, defined by the v-i characteristics of the MOV and rises to slightly less than 600 kV, i.e., 150% of the DC link voltage $V_{DC,nom}$. From this moment on, the DC link current decreases in absolute value and reaches zero within 3.2 ms, which corresponds to an average current slope of 2.6 kA/ms. Due to the duration of detection and the ICCT of the DCCB, the second DCCB neutralizes the fault after Δt=6.48 ms. It occurs after the inversion of the DC link current'

sign, induced by the short-circuit in the other extremity of the DC line. The associated TIV is smaller and the fault current suppression time is shorter, because the circuit-breaker opens at 2.21 kA, which is much lower than that of the first DCCB. Therefore, the fast operation of the DCCB in Converter 1 has reduced the fault currents seen by Converter 2.

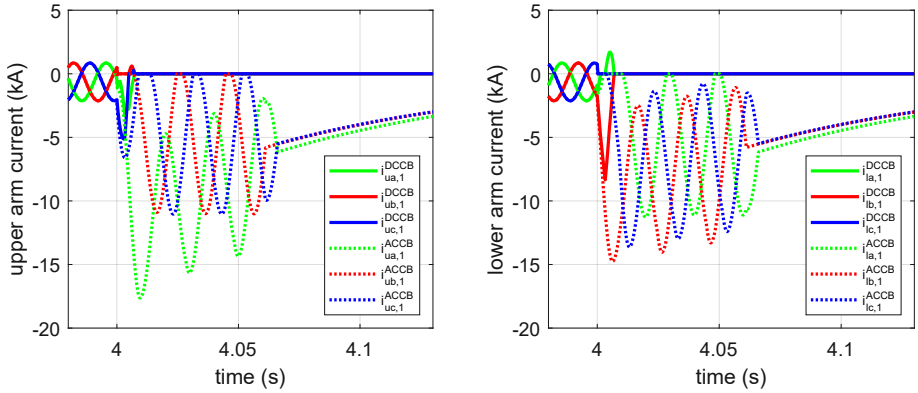


Figure 2.17: Upper and lower arm-currents during DC pole-to-pole fault with ACCBs (dotted lines) and DCCBs (solid lines); green for phase a, red for phase b and blue for phase c.

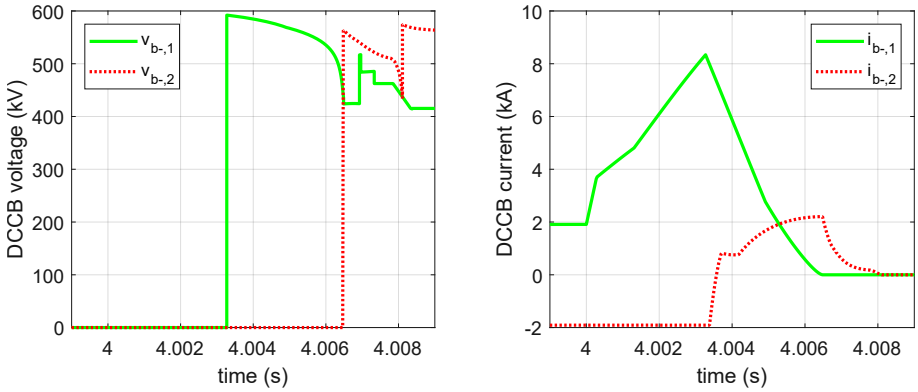


Figure 2.18: Voltage and current of the lower DCCBs during DC pole-to-pole fault

2.3.2.2 Surge-current integrals

From Figure 2.17 it is possible to calculate the surge-current integral of the diodes in each arm, according to the formula (2.7):

$$I^2t = \int_{t=t_0}^{+\infty} (i_{Diode}(t))^2 \, dt \tag{2.7}$$

As explained in 2.1.1, the converter tends to behave like a diode-rectifier after a DC pole-to-pole fault: diodes $D_{2,s}$ are involved in the fault, thus making surge-current capability an important issue for these diodes. Table 2.10 shows the surge-current integrals for diodes D_2 in the different arms of Converter 1 with ACCBs; the maximum is 8.60 $MA^2{\cdot}s$. This value can be compared to some high-power diodes proposed by different manufacturers, presented in Table 2.11. It appears that individual press-pack diodes have higher surge-current integral; hybrid IGBT or IEGT packages do not withstand the required surge-current integral. It explains the different technological choices made by the manufacturers, exposed in 2.1.2.1:

- When PPIs are used in the converter-stations the surge-current integral cannot be withstood by the diodes, so a press-pack thyristor must bypass them during faulty operation;

- The use of press-pack diodes is also relevant as it allows to withstand the surge-current integral without additional components.

In the case of IGCT, the solution presented in 2.1.2.2 is valid as long as the diodes withstand the surge-current integral, so discrete press-pack diodes must be used. The conclusion is different with DCCBs, as shown in Table 2.12, the surge-current integrals are much smaller because of the drastic reduction of fault-interruption time. Among the list of devices of Table 2.11, all are compatible with the case study. Therefore the investment in a DCCB is mitigated by the removal of a press-pack thyristor. It also allows the use of devices with integrated diodes, with smaller surge-current integrals, for instance, 5SNA 2000K450300 of ABB or ST1500GXH24 of Toshiba according to Table 2.11. There is no further possible simplification of the SM topology with IGCT, because the diodes are supposed to withstand the surge-current integrals on their own. Meanwhile, DC fault protection with DCCBs allows the use of reverse-conducting devices which reduces the cost, the failure rate and the volume of the SMs.

Phase	**a**	**b**	**c**
upper arms	8.60	4.36	4.15
lower arms	4.88	6.47	5.42

Table 2.10: Surge-current integral ($MA^2{\cdot}s$) for D_2 in Converter 1 with ACCBs

Manufacturer	**Device**	**Technology**	$\boldsymbol{I^2t}$ $\boldsymbol{(MA^2 \cdot s)}$
ABB	5SNA 2000K450300	PPI + diode	5.12
ABB	5SDF 20L4520	press-pack diode	10.1
Infineon	D1961SH45T	press-pack diode	8.0
Infineon	D4600U45X172	press-pack diode	32.0
Toshiba	ST1500GXH24	IEGT + diode	0.5
ABB	5SHX 36L4520	RC-IGCT	1.12

Table 2.11: Surge-current integral ($MA^2{\cdot}s$) for typical 4.5 kV devices

Phase	**a**	**b**	**c**
upper arms	0.026	<0.001	0.075
lower arms	<0.001	0.18	<0.001

Table 2.12: Surge-current integral ($MA^2{\cdot}s$) for D_2 in rectifier with DCCBs

2.3.3 Influence of the DCCB's Internal Current Commutation Time (ICCT)

2.3.3.1 Waveforms

The Internal Current Commutation Time (ICCT) is a key parameter of the DCCB: the faster it is, the smaller the fault currents. As shown in Figure 2.19, the maximum fault-current increases with the ICCT for Converter 1: the current rise is approximately constant between the blocking of the turn-off devices and the limitation of the fault current. The trend is different for Converter 2: the maximum fault-current is almost constant. Table 2.13 summarizes the main factors defining the operation of the DCCB, for different ICCTs. It shows that the TIV remains in an acceptable range despite a significant variation of the maximum fault current for

Converter 1, because of the non-linearity of the MOV's electrical characteristic. Furthermore, the difference between the fault-current suppression time and the ICCT increases for Converter 1, because for a given di/dt a higher fault current takes longer to reach zero.

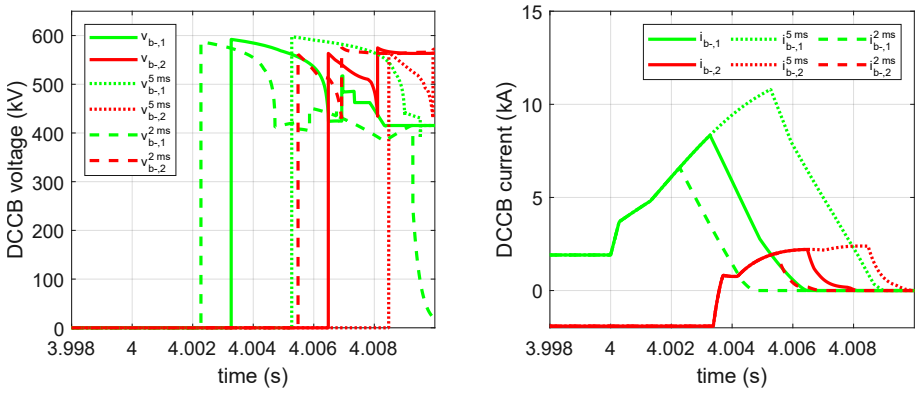


Figure 2.19: Current and voltage for the DCCBs of the negative poles of Converter 1 (green) and Converter 2 (red) with different ICCTs Δt_{ICCT}, dashed line for Δt_{ICCT}=2 ms, solid line for Δt_{ICCT}=3 ms and dotted line for Δt_{ICCT}=5 ms

Converter	$\boldsymbol{\Delta t_{ICCT}}$	**2 ms**	**3 ms**	**5 ms**
1	Maximum fault current	6.60 kA	8.34 kA	10.8 kA
	Fault current suppression time	4.70 ms	6.45 ms	8.99 ms
	TIV	587 kV	592 kV	598 kV
2	Maximum fault current	2.01 kA	2.21 kA	2.39 kA
	Fault current suppression time	6.86 ms	8.08 ms	9.89 ms
	TIV	561 kV	563 kV	565 kV

Table 2.13: Maximum fault current, fault current suppression time and TIV for different ICCTs

2.3.3.2 Surge-current integrals

Table 2.14 points out that surge-current integrals are significantly affected by the ICCT: the maximum surge-current integral has been multiplied by 2.3 for Converter 1 and by 2.1 for Converter 2, for an ICCT increasing from 3 ms to 5 ms. On the other hand, the maximum surge-current integral has been divided by 1.9 for Converter 1 and by 2.1 for Converter 2, for an ICCT dropping from 3 ms to 2 ms. As expected, the reduction of the ICCT has a double positive impact on the surge-current integral. Therefore, this parameter is sensitive and should be properly estimated and managed.

$\boldsymbol{\Delta t_{ICCT}}$	**2 ms**	**3 ms**	**5 ms**
Converter 1	0.093	0.18	0.43
Converter 2	0.0046	0.0095	0.02

Table 2.14: Surge-current integral ($MA^2{\cdot}s$) for $D_{2,s}$ with DCCBs for different ICCTs

2.4 Control of the converters

The control of the modular multilevel converter is widely discussed in the literature [123][33], many implementations are possible. Inner and outer control loops are presented. Then, a focus on a specific modulation strategy is made. Considerations related to the influence of the control on the converter's losses are presented.

2.4.1 Inner control loops

Arm-currents contain two components, as presented in Figure 1.10 in the first chapter: alternating components are phase-shifted by 180° between the upper arm and the lower arm of the same phase, whereas a zero sequence component comes from the DC link current. Inherently it could be demonstrated that circulating currents, which add to the zero sequence component, can appear at specific frequencies, second-order and fourth-order harmonics being dominant [144]. These circulating currents represent an important concept of the MMC's operation, as they depend on the passive elements of the converter as mentioned in 2.2.1.2. Moreover, it is possible to control them, resulting in a trade-off between power losses and arm-energy variation [165], synonym of converter's volume. [166] reports a reduction of the installed capacitance up to 40% with a proper circulating current injection which is significant in terms of capital expenditure (CAPEX).

Another approach is to suppress them, as it is supposed to minimize RMS arm-currents [166]. In this case, a circulating current suppression controller (CCSC) may be necessary [167][168]. The notations of Figure 1.10 have been retained, the terms (2.8) are introduced to implement the control loops:

$$\begin{array}{l} v_{sum,i}(t) = \frac{v_{ui}(t)+v_{li}(t)}{2},\ i \in \{a,b,c\} \\ v_{diff,i}(t) = \frac{-v_{ui}(t)+v_{li}(t)}{2},\ i \in \{a,b,c\} \\ i_{sum,i}(t) = \frac{i_{ui}(t)+i_{li}(t)}{2},\ i \in \{a,b,c\} \\ i_{diff,i}(t) = \frac{i_{ui}(t)-i_{li}(t)}{2},\ i \in \{a,b,c\} \end{array} \tag{2.8}$$

where $i_{sum,i}$ contains a third of the DC link current plus the circulating current of phase i, $i_{diff,i}$ is half the grid current of phase i and $v_{diff,i}$ is the pole-to-ground voltage of phase i. Consequently, this transformation, though simple, allows a separate management of AC and DC quantities. Since this is a three-phase system with positive and zero sequence components, the use of dq0 transformation is especially relevant [169]. The equations (2.9) are obtained:

$$\begin{cases} L_{eq}\frac{di_{diff,d}}{dt}(t) = L_{eq}\omega_0 i_{diff,q}(t) + v_{diff,d}(t) - v_{sd}(t) \\ L_{eq}\frac{di_{diff,q}}{dt}(t) = -L_{eq}\omega_0 i_{diff,d}(t) + v_{diff,q}(t) - v_{sq}(t) \end{cases} \tag{2.9}$$

The resulting output-current controller is shown in Figure 2.20, decoupling terms are necessary to independently regulate $i_{diff,d}$ and $i_{diff,q}$. A bandwidth of 30 Hz is sufficient to obtain a satisfactory dynamic response, leading to the coefficients of (2.10). The inductance L_g, including the cables and the leakage inductance of the converter transformers, must be considered as well as L_{arm} since it affects the dynamic of the AC grid currents. The parameters of the PI controller are calculated as follows:

$$\begin{cases} T_{id} = \frac{10}{\omega_{id}} \\ K_{id} = L_{eq}\omega_{id}, \text{ with } L_{eq} = L_{arm} + 2L_g \end{cases} \tag{2.10}$$

For each arm of each phase, duty-cycles are calculated by dividing the reference voltages $v^*_{ul,abc}$ by the nominal DC link voltage, V_{DC}, using the formula (2.11):

$$\alpha_{ul,abc}(t) = \frac{v^*_{ul,abc}(t)}{V_{DC}} \tag{2.11}$$

Also called "direct voltage control", this strategy provides asymptotic stability of the arm energies [170][171]. However, it introduces circulating currents in the converter because the total capacitor-voltage has a ripple at both grid-frequency f_0 and twice grid-frequency. Consequently, the CCSC has to be implemented. The second-order harmonic is suppressed as it is the most significant. On the whole, the first unwanted harmonic appears at four times the grid frequency, its influence is not meaningful.

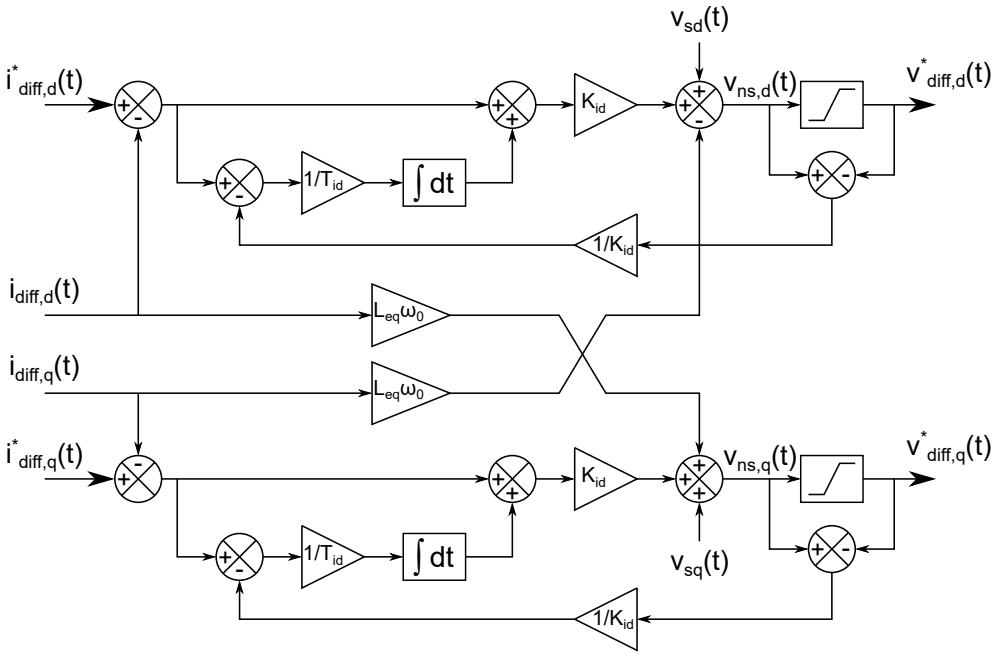


Figure 2.20: Schematic of the output-current controller; first inner control loop

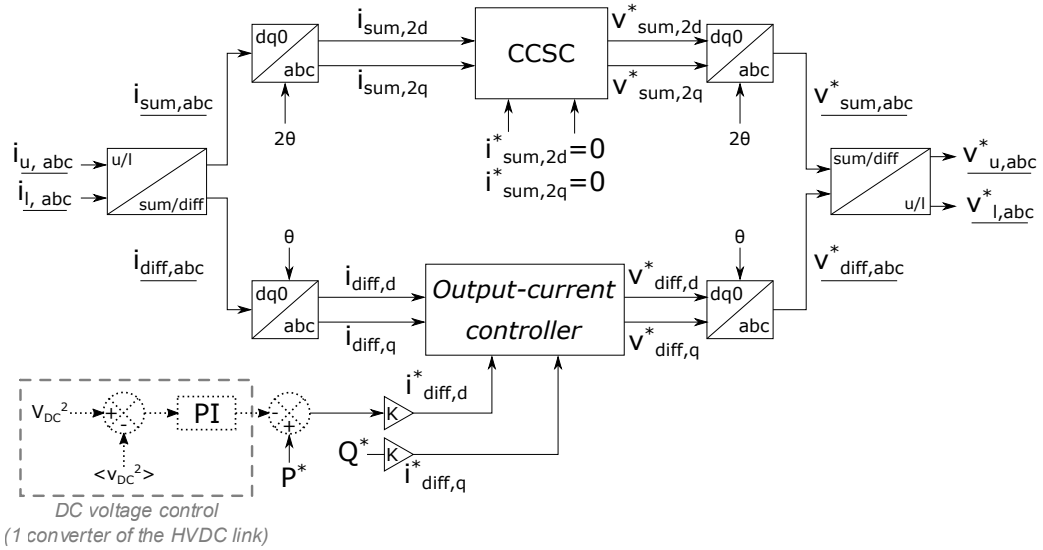


Figure 2.21: Overall schematic of the inner control loops with DC voltage mode control (1 converter of the HVDC link)

The implementation of the inner control loops is represented in Figure 2.21. It should be noted that the CCSC is based on a dq0 transformation at 2θ, since it works on the second

harmonic of the arm-currents. Outer control includes at least a DC voltage mode control, that must be enabled for one converter of the HVDC link, whereas the other converter manages the active power flow [172]. Droop control strategies which affect reactive power injection, the DC link voltage, the active power and the AC grid voltages have not been considered, because they are too specific to local standards and requirements. Besides, most of them are irrelevant for the assessment of power losses and for the study of fault scenario. Detailed information about droop control for HVDC converter-stations are provided in [33].

2.4.2 Multilevel modulation strategy

2.4.2.1 Existing multilevel modulation strategies and related issues

Multilevel modulation methods have known a significant development along with the multilevel converters. Typically four families can be retained [173]:

- Space vector based algorithms;
- Carrier-based Pulse Width Modulation (PWM);
- Nearest-Level Control (NLC) or nearest-level modulation;
- Staircase modulation or Selective Harmonic Elimination (SHE).

The selection of a multilevel modulation method must respond to the specific needs and constraints of the application. The case of the MMC for HVDC applications is singular, due to its large number of levels that easily exceeds a hundred. Consequently, the reduction in THD of AC quantities is not a critical concern, as explained in 1.2.3. On the other hand, real-time implementation of the modulation strategy is pointed out as an issue [174], since its time complexity depends on the number of SMs per arm. This first observation shows that staircase modulation is penalized, since it lies in nonlinear equations, whose solutions must generally be pre-calculated to allow real-time operation [175][176]. Space vector based techniques have no particular interest compared to temporal approaches, the direct management of redundancies being too cumbersome to be relevant [177].

Carrier-based PWM methods allow an operation at constant switching frequency, and lead to a reduction in THD of AC grid side voltages and currents. Their performances mainly depend on the redundancy management. Figure 2.22 presents the two-step control of the arm-voltages. The modulation strategy mainly defines the arm-voltage waveform, whereas the redundancy management system aims to balance the SM voltages.

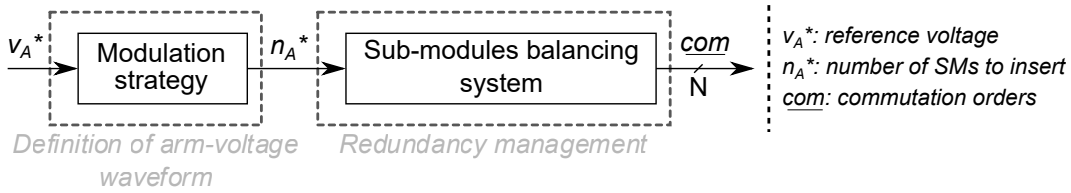


Figure 2.22: Control of the arm-voltages in an MMC having a large number of levels divided into two steps

Individual SM balancing is an efficient, though basic, approach where all the SM voltages are individually controlled [167][169]. It only applies to Phase-Shifted Carrier PWM (PSC-PWM) methods. On the other hand, sorting algorithms exhibit better performances and are not limited to PSC-PWM. For both techniques, switching frequencies inferior to 100 Hz are reachable [138]. Nevertheless, it has been reported that switching frequencies that are integer multiples of the

grid frequency prevent any cell balancing with PSC-PWM: sideband harmonics interact with the process [178]. Moreover, under three times the grid frequency the capacitor-voltage ripple is erratic; which may represent a tough constraint for the design of the converter if the switching frequency is not properly chosen.

NLC provides more flexibility as the switching frequency is not fixed, it is inherently defined by the sorting algorithm. Yet, a certain number of levels is required for this modulation method to be efficient. In this study case, N reaches a few hundreds so this requirement is fulfilled, the resulting THD is not significantly increased compared to PWM methods. The sampling frequency f_s must be properly chosen, then the criterion (2.12) is retained [179] to keep single-level transitions between two consecutive samples:

$$f_s > N\pi f_0 \tag{2.12}$$

A wide range of sorting algorithms for NLC have been proposed in the literature, for instance predictive algorithms may provide a satisfactory trade-off between the capacitor-voltage ripple and the switching frequency [139]. Tolerance band algorithms are also attractive as they provide a way to set the maximum capacitor-voltage ripple, which also influences the switching frequency [140]. [142] proposes a similar approach by introducing a maintaining factor. Furthermore, it has been shown that switching instants could be concentrated near zero-current crossings with cell tolerance band methods, leading to a major reduction of the switching losses [180].

Tolerance band methods are very promising but the selection of the tolerance band themselves is not trivial: a strategy for dynamic operation including reactive power injection has been proposed by [181] but it increases the overall complexity of the control. A more practical approach is to modify the width of the tolerance band to control the switching frequency [182], leading to a single parameter to handle. Nevertheless, these techniques rely on the hypothesis that the average SM voltage is known, and remains unchanged: the calculations presented in Appendix A show that the average SM voltage is expected to vary with the reactive power. Since tolerance bands should be symmetrical to obtain an optimized operation, it can be concluded that the selection of the tolerance bands is harder than expected.

The generic control of the arm-voltages based on NLC is presented in Figure 2.23. The sorting algorithm generally requires real-time quantities such as the SMs voltages $(v_{SM})_{i\in[1,N]}$ and the arm-current i_A.

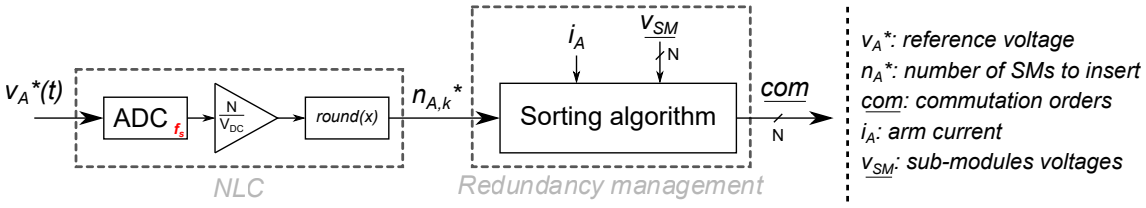


Figure 2.23: Control of the arm-voltages in an HVDC-MMC with NLC+sorting algorithm, NLC comprises an Analog-to-Digital Converter (ADC) and a round function (round)

2.4.2.2 Practical constraints regarding the semiconductor devices

Additional constraints related to the semiconductor devices must be considered to definitively select the modulation strategy. The most important is that IGCTs, as well as all other semiconductor devices, have an intrinsic dynamic at turn-on and turn-off which induces minimum on-time $t_{ON,min}$ and minimum off-time $t_{OFF,min}$. In the case of the IGCT, the clamp circuit affects this dynamic as well. Then, a minimum delay between two commutations, i.e the minimum

pulse width at a given state $T_{PW,min}$ is defined for a given set of semiconductor devices. The modulation strategy must respect this minimum duration between two commutations occurring in the same SM. $T_{PW,min}$ is estimated to be 50 μs at this step for IGCT [67]. This value is further discussed thereafter.

PWM methods with a sorting algorithm According to the previous observations PWM methods remain attractive, especially with a sorting algorithm. Duty-cycles are generally limited by boundaries, typically $T_{PW,min}f_{sw}$ and 1-$T_{PW,min}f_{sw}$ to ensure the minimum pulse width aforementioned. Yet, a SM is not assigned to a duty-cycle any more, which can potentially lead to the violation the minimum delay between two commutations. As shown in Fig. 2.24, if no sorting operation is done during the circled instants the same SM switches twice within a short duration, potentially inferior to $T_{PW,min}$. As a consequence the sorting algorithm must at least record the last commutation instants of all the SMs to avoid this critical phenomenon.

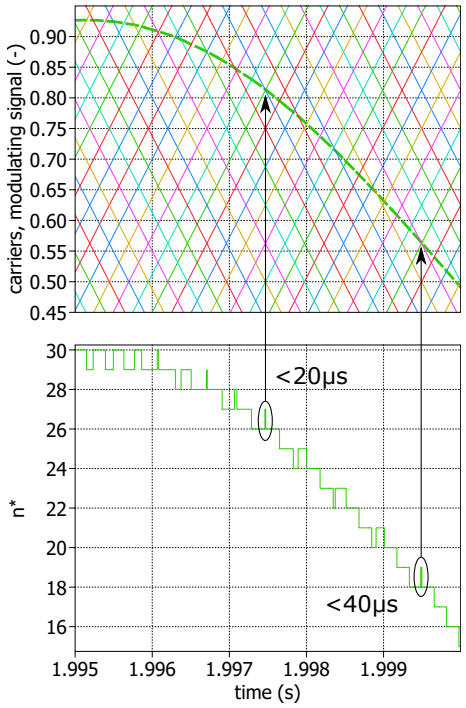


Figure 2.24: MMC with 32 SMs using PSC-PWM; carriers, modulating signal and resulting number of SMs to insert

NLC with a sorting algorithm The minimum pulse width is naturally respected with NLC as soon as the sampling frequency f_s is low enough: no commutation can occur between two successive sampling instants which simplifies the protection of the semiconductor devices.

The reduction of the switching frequency is another issue, pointed out as a relevant way to decrease the semiconductor power-loss in the literature for HVDC-MMC applications [173][182]. Switching frequencies as low as 50 Hz, i.e. the grid frequency, have been reported [183]. Moreover, it allows to select semiconductors with lower on-state losses (and higher switching losses), thus decreasing the power losses even more [184]. On the other hand, the reduction of the switching frequency generally leads to a rise in the peak-to-peak capacitor-voltage ripple. This is an important drawback, since it either implies an increase in the converter's volume as explained in 2.2.1.1, or a reduction of the SMs' lifetime according to the developments of 2.2.2.1. Therefore, the trade-off between the capacitor-voltage ripple, introduced by the sorting algorithm, and the

switching frequency must be properly handled for all the operating conditions of the converter. According to the analysis made in 2.4.2.1, cell tolerance bands methods are among the most suitable solutions, but dynamic operation is more complicated.

2.4.2.3 Considerations regarding the sorting algorithm retained

A new sorting algorithm, developed in the scope of this PhD thesis, is used to address the aforementioned concerns: simple dynamic operation and low frequency operation with a reasonable capacitor-voltage ripple. It is tuned to obtain a switching frequency varying from 75 Hz to 130 Hz, with a capacitor-voltage ripple lower than 17% when the power varies from ±50 MW to ±1 GW, considering an energy stored in the converter of 45.5 kJ/MVA. These operating conditions are supposed to favour IGCTs, in the meantime they remain reasonable: operation at grid-frequency has been avoided since it seriously penalizes converter's volume. The capacitor-voltage ripple complies with the initial expectations of 2.2.1.1. This sorting algorithm is currently the subject of a patent application, the details of its implementation cannot be disclosed at the time of writing.

2.5 Conclusion

Throughout this second chapter, the design of an HVDC-MMC using IGCT-based SMs has been carried out, including many considerations: MMC's properties and operation but also internal SM failures and reliability. The ARCP circuit has been identified as a relevant auxiliary circuit for IGCTs to reduce the power losses and the volume, compared to the traditional solution consisting of a clamp circuit and a di/dt choke. The modelling of the protection equipment as well as the HVDC cables has been presented. Simulations have shown that the design and the sizing of the SMs depend on the circuit-breakers, the initial cost of DCCBs is counterbalanced by the possibility to use devices with higher power densities, reducing the volume and the cost of the SMs. However, the ICCT of the DCCB must be mastered as it significantly affects the thermal stresses of the semiconductor devices.

In terms of control, NLC has come out as the most relevant modulation strategy due to its simplicity and its flexibility. The possibility to reduce switching frequency with a reduced computation complexity is crucial for HVDC systems, to allow switching losses reduction and real-time operation. The next chapter focuses on the modelling of the converter-station to efficiently calculate the power losses of the semiconductor devices, which implies a multi-physical approach.

Chapter 3

Electro-thermal modelling of the HVDC-MMC

3.1 Electrical model of the MMC

Several models exist to study the behaviour of the MMC. It is necessary to select the most suitable in terms of computation time, accuracy, and ease of implementation to perform an efficient power-loss analysis.

3.1.1 Detailed model (DM)

3.1.1.1 Presentation

The more immediate way to model the MMC is to represent all the SMs with discrete semiconductor devices, and eventually additional elements in the SM such as a parallel resistor to model internal losses [33]. Such a model has various names in the literature such as Detailed Model (DM) [49], instantaneous model [123] or SM-level switched model [33]. It is by definition the most accurate model at the converter level, and is presented in Figure 3.1. It is assumed that switches are ideal, i.e. lossless during on-state and commutations. So, in the specific case of the IGCT, the di/dt choke and the clamp circuit must not be represented. The drawing of the full circuit, including N SMs per arm, is not appropriate as it is not flexible. The concept of vectorization figures out this issue, allowing a parametric definition of the number of SMs per arm.

Such a representation is not relevant as soon as a large number of SMs is present in the converter, the number of discrete semiconductor devices in the converter being equal to 24N. The state-space system becomes enormous, typically leading to durations of calculation about a day with 128 SMs per arm on a desktop computer, for a few seconds of simulations only.

3.1.1.2 Comparison of NLC and PSC-PWM

The running of the DM is limited because of the consequent computation time and the important quantity of RAM. Typically, the converter-stations cannot be simulated with a number of SMs exceeding 128 with NLC, and 64 with PWM. According to 2.2.2.2, there is no match with traditional DC link voltages and standard semiconductor voltage ratings, thus it is decided to apply a scaling factor to the reference configuration V_{DC}=±320 kV/N=256. The SM capacitance is calculated to keep the total energy stored in the converter, expressed in kJ/MVA, identical for the different DC link voltages. The characteristics of the converter-stations for the two modulation strategies are presented in Table 3.1. A Reduced Switching-Frequency (RSF)

algorithm is used with PSC-PWM as described in [141], whereas NLC is combined with a sorting algorithm as described in 2.4.2.3. The two modulation strategies operate at 107±1 Hz, allowing for a comparison with similar operating conditions.

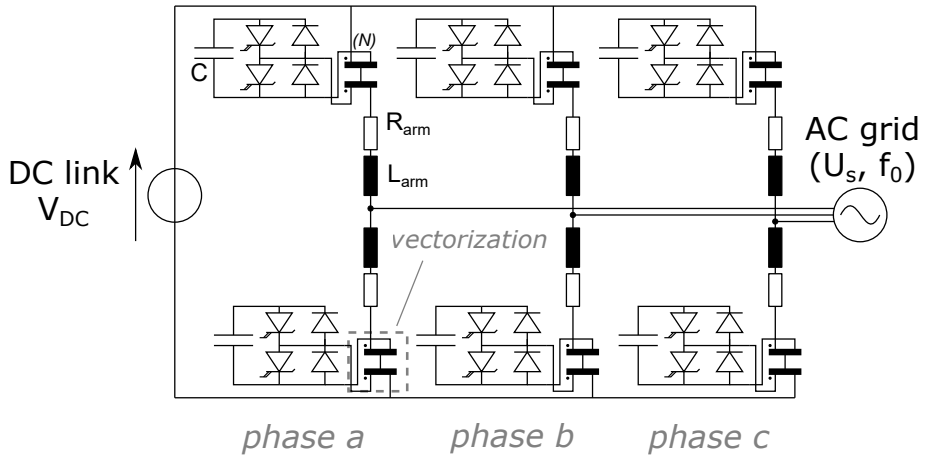
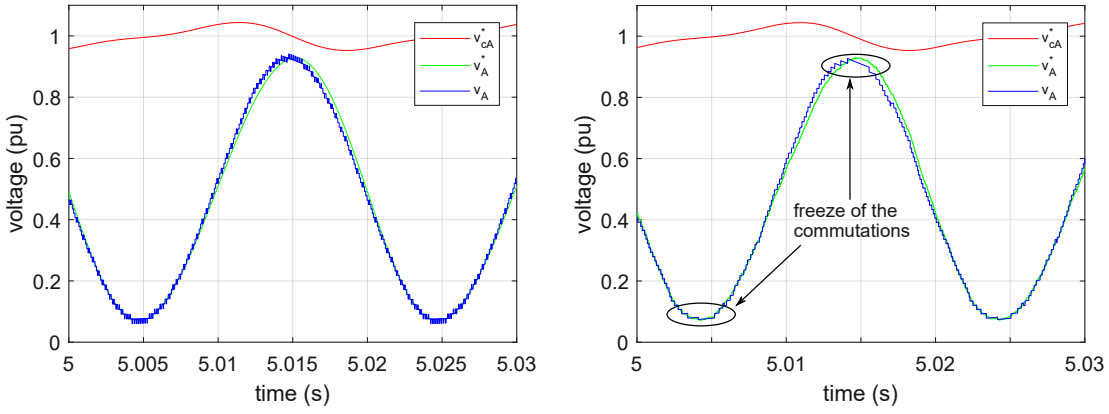


Figure 3.1: Detailed model of the MMC with half-bridge SMs using vectorization

Modulation	P	V_{DC}	N	U_s	C	L_{arm}
NLC	250 MW	±160 kV	128	166 kV	3.14 mF - 54 kJ/MVA	51.5 mH
PSC-PWM	125 MW	±80 kV	64	83 kV	6.28 mF - 54 kJ/MVA	25.7 mH

Table 3.1: Main characteristics of the converter-stations retained, for the comparison between NLC and PSC-PWM



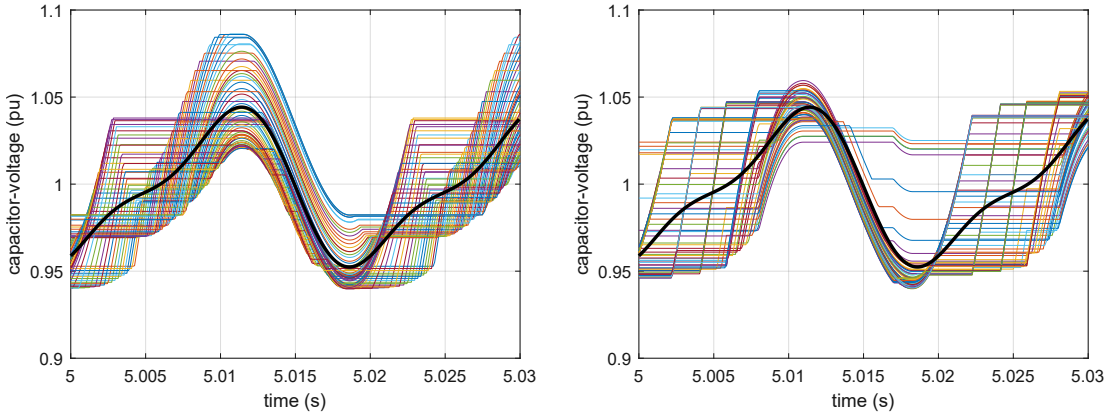
(a) PSC-PWM with RSF algorithm (b) NLC

Figure 3.2: Arm-voltage v_A, sum capacitor-voltage v_{cA} and reference arm-voltage v^*_A for PSC-PWM and NLC

Arm-voltage and sum capacitor-voltage Figure 3.2(a) shows that the arm-voltage v_A is consistent regarding the limits of operation at full power, it evolves between 0 and the sum capacitor-voltage v_{cA}. PWM can be observed, especially at the voltage peaks where it ensures an accurate reproduction of the desired voltage. The reference arm-voltage is distorted compared to the effective arm-voltage, because of the CCSC and the direct voltage control, as developed

in 2.4.1.

Then, Figure 3.2(b) points out that NLC leads to a faithful representation of the arm-voltage, especially between 0.4 and 0.6 pu. On the other hand, NLC provides a poor approximation of arm-voltage at the peaks: ideally NLC delivers a constant voltage when the reference is constant, on the contrary of PWM. Regarding the sorting algorithms, it can be observed on Figure 3.2(b) that the voltage intervals are slightly different due to the different capacitor-voltage ripples. The behaviour of NLC close to voltage peaks has a negative impact, as it introduce low-frequency harmonics with located distortion. Nevertheless, the freeze of commutations at the voltage peaks also coincide with the current peaks when no reactive power is injected, thus it potentially leads to a reduction of switching losses.



(a) PSC-PWM with RSF algorithm (b) NLC with sorting algorithm

Figure 3.3: Capacitor-voltages v_{ci}, $i \in [1, N]$, for NLC and PSC-PWM with RSF algorithm, P=1 pu; the average sum-capacitor voltage has been represented in black

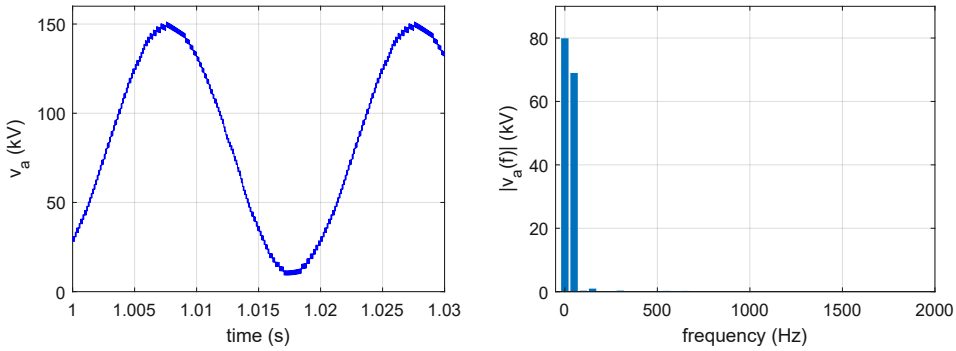
Capacitor-voltages Figure 3.3 shows the differences induced by the two sorting algorithms, with their respective modulation strategies. For P=1 pu and Q=0 MVAR, the total capacitor-voltage ripple is the smallest for the sorting algorithm implemented with NLC, 12.1%, compared to 14.6% with the RSF algorithm. Nevertheless, this property cannot be guaranteed for all the operating points of the converter.

3.1.2 Averaged model (AVM)

Normal operation Considering more than a hundred levels, the output waveforms of the DM are smooth, the modulation of the arm-voltages is hardly visible on the waveforms. Even the corresponding low-frequency spectrum cannot reveal the presence of a modulating signal, as shown in Figure 3.4. This observation leads to a first conclusion: an arm containing N SMs behaves as a continuous controlled voltage source.

According to this assumption, an arm can be replaced by a single equivalent SM, whose capacitance is $C_e = \frac{C}{N}$, providing an instantaneous voltage αv_c: this is an averaged model of a chopper generalized to N series-connected SMs. After applying it to the six arms of the converter, an Averaged Model (AVM) of the MMC [123], also called arm-level averaged model [33] or average-value model [49], is obtained, as represented in Figure 3.5. The computation time is estimated to a few seconds for the same simulation duration, approximately 40 000 times faster than the DM with N=128. Moreover, the AVM has a significant benefit: its computation time

is independent of the number of levels, so the reduction of the computation time is guaranteed, even for a higher number of levels.



(a) Waveform of the arm-voltage

(b) Spectrum of the arm-voltage, 40 first harmonics

Figure 3.4: Waveforms and spectrum of an arm-voltage with 64 SMs per arm, V_{DC}=±80 kV, PSC-PWM

Averaged model for faulty operation The AVM previously presented is only valid during normal operation: as soon as a fault is detected, controllable devices are blocked which invalidates the model. Actually, only the two diodes can potentially conduct during this phase, so the SM has a non-linear behaviour. Based on 2.1.1 and Figure 3.5, the model presented in Figure 3.6 can be deduced, where v' and i_c follow the relations (3.1). CE corresponds to an enabling signal, changed from 1 to 0 when the controllable devices are opened after fault detection. This model has been used to establish the results presented in 2.3.2 and 2.3.3.

$$\begin{cases} \text{if } CE = 1 \text{ (closed switch), } v' = \alpha V_c \text{ and } i_c = \alpha i' \\ \text{if } CE = 0 \text{ (open switch), } v' = V_c \text{ and } i_c = i' \end{cases} \tag{3.1}$$

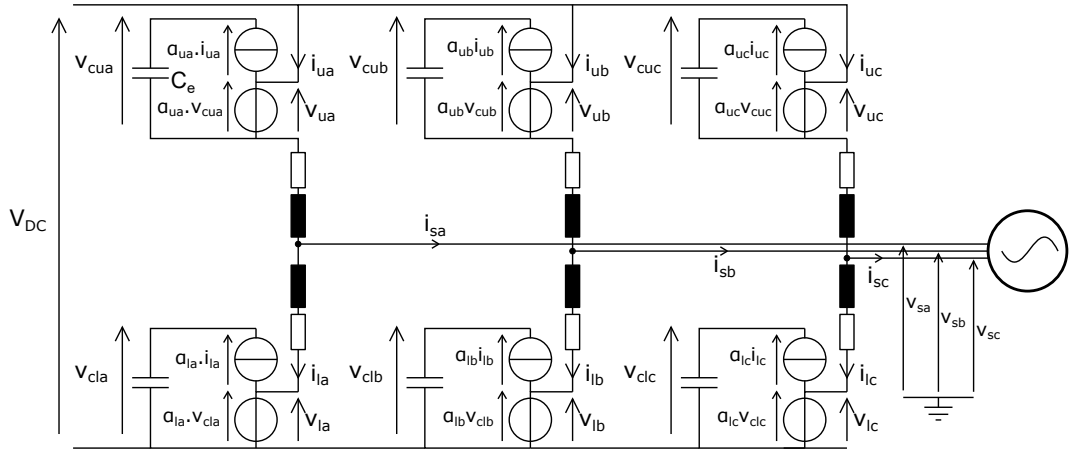


Figure 3.5: Averaged model of the MMC with half-bridge SMs

3.1.3 Comparison between the DM and the AVM

Based on the considerations mentioned in 3.1.1.2, the characteristics of the converter-stations for this study are presented in Table 3.2. The model reduction presented in 3.1.2 must lead to

a relative error as low as possible, between the AVM and the DM, to be valid. For reasons that are developed later in the chapter, the reference arm-voltage v^*_A and the arm-current i_A are important quantities that must be correctly reproduced by the AVM.

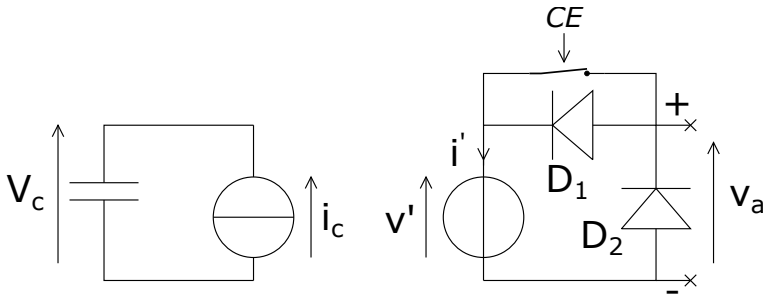
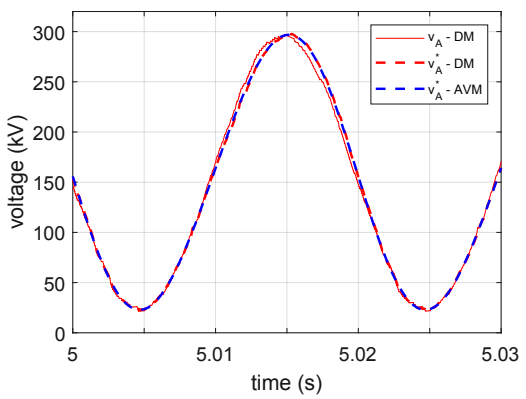


Figure 3.6: AVM of an arm with half-bridge SMs for normal and faulty operation, CE=1 during normal operation (closed switch)

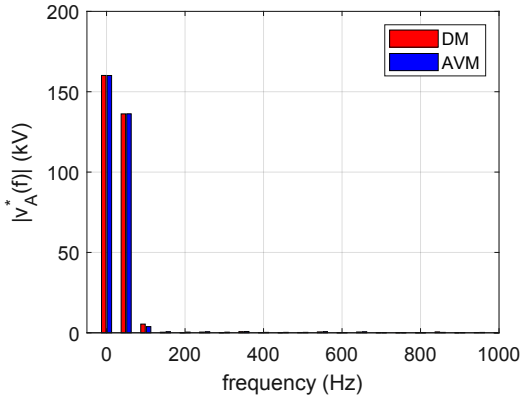
Power	V_{DC}	N	U_s	C	L_{arm}
250 MW	±160 kV	128	166 kV	6.28 mF (54 kJ/MVA)	51.5 mH

Table 3.2: Main characteristics of the converter-stations, with a scaling factor of 2, retained to compare the DM and the AVM

Then, Figure 3.7(a) shows that the AVM model generates a reference arm-voltage very similar to the arm-voltage obtained with the DM, despite the drastic differences between the two models. A tiny distortion can be observed, the spectrum of the two waveforms shown on Figure 3.7(b) unveils a slight difference between the second-order harmonics, which is not meaningful.



(a) Waveforms of v_A with the DM, the AVM and v^*_A with the DM

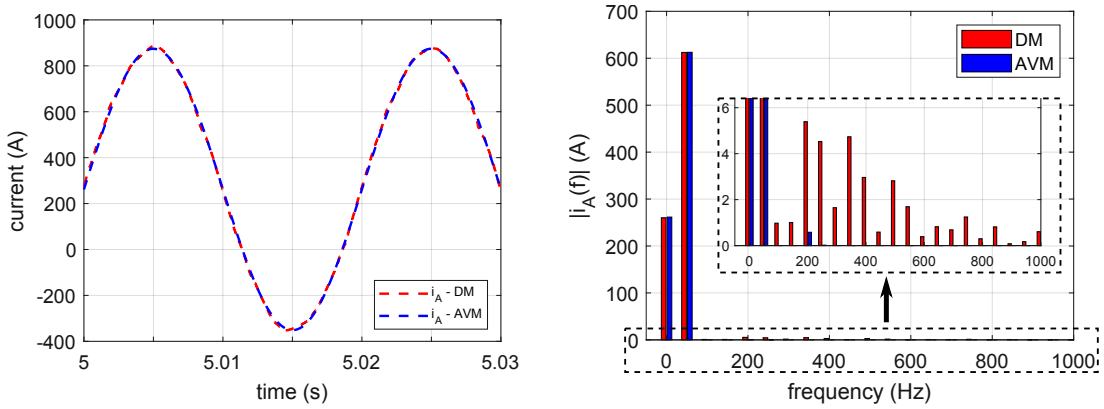


(b) Spectrum of v^*_A with the DM and the AVM

Figure 3.7: Waveforms and spectrum of v_A and v^*_A

Similar observations can be made from Figure 3.8(a), the DM shows a slight deformation close to the peak currents, whereas the AVM does not: this phenomenon is due to the modulation strategy. The harmonic content of the arm-current from the DM, presented in Figure 3.8(b), is much richer than the spectrum obtained with the AVM. Indeed, many low-frequency harmonics

are present from the 4^{th} to the 20^{th}. Yet, this difference is not problematic since the amplitude of the corresponding harmonics is negligible, inferior to 1% of the fundamental. It can be concluded, from the analysis of Figure 3.7 and Figure 3.8, that the AVM provides waveforms with a meaningless modelling error, compared to the DM.



(a) Waveforms of i_A with the DM and the AVM

(b) Spectrum of i_A with the DM and the AVM

Figure 3.8: Waveforms and spectrum of i_A

3.2 Electro-thermal model of the sub-modules

Due to the large number of SMs, traditional models do not calculate power losses for every single SM [185, 186], which leads to an approximate result. Since the ratio between switching frequency and grid frequency is low, the dispersion of on-state and switching losses among the cells of the same arm can become significant. Consequently, a few SMs will experience more thermal stresses than expected with these models, which is unacceptable when it comes to estimating maximum junction temperatures for instance.

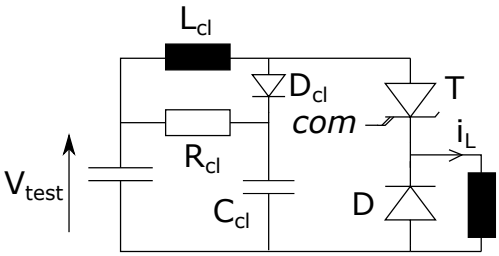
Furthermore, most models presented in the literature do not take into account this electro-thermal coupling and simply assume a constant junction temperature [187, 79]. However, consideration of the junction temperature is crucial, as specified in IEC 62751-2, since semiconductor power losses are highly dependent on temperature. Turn-on and turn-off losses can vary from 10% to 40% between 25°C and 125°C for IGBTs, depending on the technology and the packaging. It is common to consider the highest junction temperature to estimate power losses, but to ensure their safe operation, the devices operate at a lower junction temperature, whereby the losses are no longer the same [188]. Moreover, considering that IGBTs/IGCTs and diodes are thermally independent of each other is not strictly correct depending on the arrangement of these two parts. Both belong to the same packaging for devices such as the IEGT and more generally wire-bonded IGBT modules, while the same physical area of silicon is used for RC-IGCT [189] and BIGT [64]. It implies that calculations must consider at some point a relation between diode losses and IGBT/IGCT losses. Consequently, the purpose is to develop a model, that involves the junction temperatures of the semiconductors, with a fast computation time.

3.2.1 Measurement of the semiconductors' characteristics

The test system is shown in Figure 3.9(a). Inside the test system, the Device Under Test (DUT) is preheated in order to measure electrical characteristics at a specific junction temperature, $T_{j,DUT}$, up to 200°C. The DUT is inserted in the test system and clamped to its nominal

mounting force. Depending on the DUT, i.e. IGCT or diode, the electrical circuit is reconfigured to obtain the simplified schematic of Figure 3.9(b). Reconfiguration switches, protections and auxiliary systems (for charging the DC bus for instance) have not been represented. The clamp circuit is inserted at the back of the test system (many clamp circuits are pre-assembled as plug-in units for easy insertion and removal). The DC bus is charged to the nominal voltage, V_{test}, which corresponds to the voltage at which the DUT is supposed to be turned on and off. The double-pulse method must be repeated for each operating point. If the DUT is a diode, dI_r/dt, reverse-recovery current and reverse-recovery charge are automatically obtained through signal processing of diode current during turn-off. On-state, turn-on and turn-off losses are obtained using a double-pulse method, as presented in Figure 3.10.

(a) Picture of the test system for IGCTs and diodes at Hitachi ABB Power Grids, Semiconductors



(b) Equivalent circuit for the DUT (IGCT or diode)

Figure 3.9: Test system with its electrical schematic at Hitachi ABB Power Grids, Semiconductors

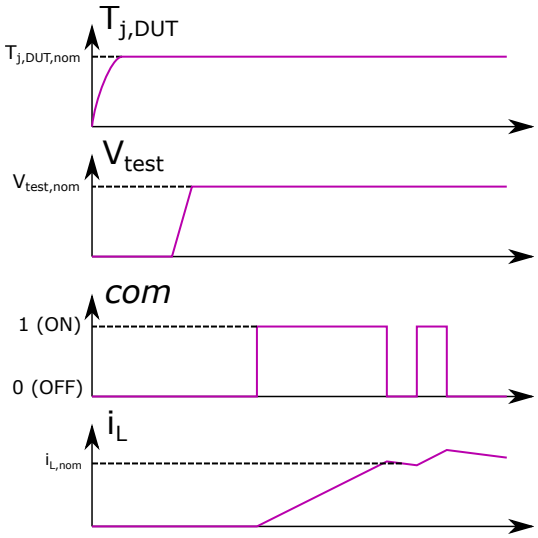


Figure 3.10: General waveforms of double-pulse method for testing of power semiconductors; time scale is not respected (self-heating of the DUT during the short current pulse is deemed negligible)

Asymmetric IGCTs (A-IGCTs) of different voltage classes (4.5, 6.5 and 10 kV), their respective free-wheeling diodes and reverse conducting IGCTs (4.5, 6.5 and 10 kV) have been electrically characterized for static and dynamic losses, Table 3.3 and Table 3.4 present all the semiconductors retained. To achieve a precise loss-model, the measurements have been

conducted at junction temperatures of 25°C, 75°C, 125°C and 140°C (when reachable). The dynamic characterization has been carried out for different voltages, covering the full capacitor-voltage ripple of an SM, and also different currents and clamp-circuits. Several devices with different charge-carrier lifetime-treatments have been measured to select the optimal device per application regarding the compromise between static and dynamic losses. For instance, Table 3.3 proposes 4 IGCTs with the same voltage rating and the same silicon area, having different best-suited switching frequencies. This compromise is particularly interesting to study, since it leads to an optimisation of the converter's efficiency without modifying either the topology or the control of the converter itself.

Part number	**Type**	**Designation**	**max. T_j**	**best-suited f_{sw}**
5SHY 40L4511	asymmetric	A-IGCT 1 4.5 kV	140°C	high
5SHY 35L4510	asymmetric	A-IGCT 2 4.5 kV	140°C	medium
5SHY 55L4500	asymmetric	A-IGCT 3 4.5 kV	140°C	low
5SHY 55L45xx	asymmetric	A-IGCT 4 4.5 kV	140°C	very low
5SHX 36L4520	reverse-conducting	RC-IGCT 1 4.5 kV	125°C	medium
5SHX 35L4521	reverse-conducting	RC-IGCT 2 4.5 kV	125°C	low
5SHX 22L6511	reverse-conducting	RC-IGCT 1 6.5 kV	140°C	low
5SHY 17L9000	asymmetric	A-IGCT 1 10 kV	115°C	medium
5SHY 17L90xx	asymmetric	A-IGCT 2 10 kV	115°C	very low
5SHX 20L8500	reverse-conducting	RC-IGCT 1 10 kV	125°C	low

Table 3.3: List of the IGCTs characterized and retained for the power-loss analysis

Part number	**Designation**	**max. T_j**	**best-suited f_{sw}**
5SDF 20L4520	diode 1 4.5 kV	140°C	medium
5SDF 28L4520	diode 2 4.5 kV	140°C	low
5SDF xL9000	diode 1 10 kV	125°C	medium
5SDF xL90xx	diode 2 10 kV	125°C	very low

Table 3.4: List of the discrete press-pack diodes retained for the power-loss analysis

The use of measured characteristics stored in look-up tables greatly enhances the accuracy of the calculations, compared to the traditional second-order approximations used for on-state and switching losses. The on-state voltage (respectively the switching energy) is obtained by interpolation of the two closest on-state voltages (respectively the two closest switching energies). The number of points forming the static and the dynamic characteristics for each device has been reported in Table 3.5.

3.2.2 Electro-thermal models for the semiconductors

The thermal modelling of semiconductors is not straightforward: multiple materials with different properties must be considered. Besides, contact resistances are also involved and depend on the mounting pressure [70]. Theoretically, the most comprehensive approach consist in a 3-D finite-element method. However, the resulting computation time is also the highest. Furthermore, the whole geometry of the device must be reproduced to obtain accurate results. Thus, model reduction is deemed necessary. The use of thermal RC models is more suited, as it drastically simplifies the geometry. Only the most significant thermal interfaces are retained, which makes the model easily adaptable to different complexity levels. This modelling technique has

also been retained by PLECS to enhance the calculation of power losses for static converters. For IGCTs, this model has proven to be accurate [93], where the RC parameters have been determined from the geometry of the different elements forming the device.

Designation	**Number of points per characteristic**	
	Static	Dynamic
A-IGCT 1 4.5 kV	44	96
A-IGCT 2 4.5 kV	44	96
A-IGCT 3 4.5 kV	44	96
A-IGCT 4 4.5 kV	44	96
A-IGCT 1 10 kV	8	12
A-IGCT 2 10 kV	8	12
diode 1 4.5 kV	40	112
diode 2 4.5 kV	40	112
diode 1 10 kV	14	24
diode 2 10 kV	14	24
RC-IGCT 1 4.5 kV	44(GCT) + 40(diode)	72(GCT) + 84(diode)
RC-IGCT 2 4.5 kV	44(GCT) + 40(diode)	72(GCT) + 84(diode)
RC-IGCT 1 6.5 kV	44(GCT) + 40(diode)	76(GCT) + 80(diode)
RC-IGCT 1 10 kV	21(GCT) + 21(diode)	36(GCT) + 45(diode)

Table 3.5: Number of points forming the static and the dynamic characteristics of each device

3.2.2.1 Asymmetric IGCT and diode

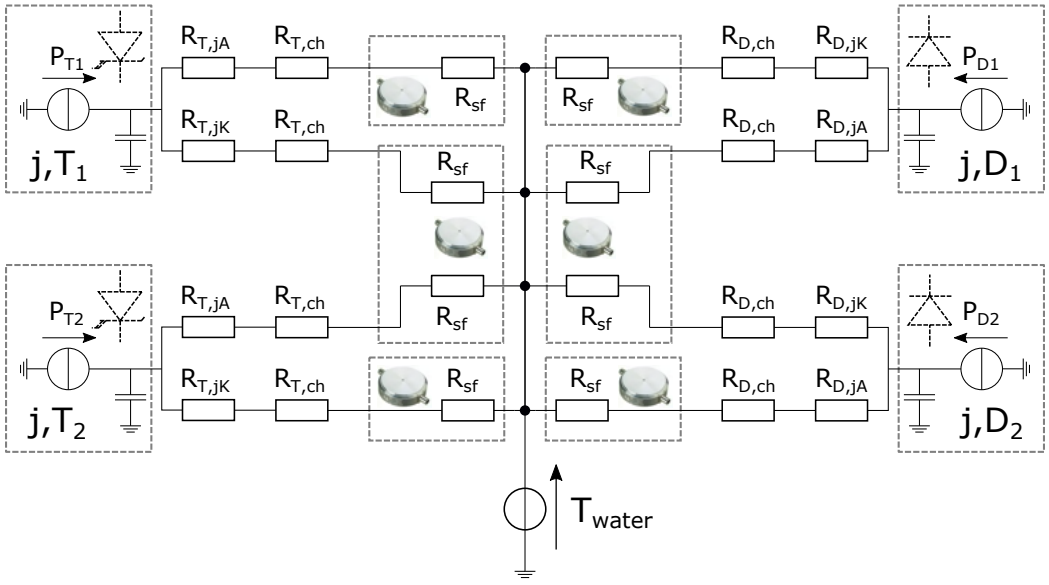


Figure 3.11: Thermal model for a chopper SM with two IGCTs and two diodes

The thermal modelling of an asymmetric IGCT, associated to a discrete diode, depends on the mechanical mounting. It is assumed that two independent stacks are built: one stack contains three cold plates and two IGCTs, as presented in 1.3.3, and the other one contains the two diodes instead of the two IGCTs. Figure 3.11 shows the model of two stacks. The first assumption that has been made is that the water temperature T_{water} is constant. In reality,

the outlet temperature is always slightly superior to the inlet temperature for each cold plate. This property is further discussed and exploited in the fifth chapter. Moreover, the middle cold plate that evacuates heat by its two contact surfaces has been modelled as two independent contact surfaces, since the single-face thermal resistance is often given in the data-sheets. The most significant interfaces of the devices are junction-to-anode and junction-to-cathode, then case-to-heatsink, which applies to both anode and cathode, corresponds to a contact resistance. Conduction is dominant from junction to heatsink, then forced convection with water is much more efficient than natural convection with ambient atmosphere. The parameters of this thermal circuit, for 4.5 kV asymmetric IGCTs and diodes, are given in Table 3.6.

Designation	Value	Description
$R_{T,jA}$	15.2 K/kW	between junction and anode, IGCT
$R_{T,jK}$	19.3 K/kW	between junction and cathode, IGCT
$R_{D,jK}$	12.9 K/kW	between junction and cathode, diode
$R_{D,jA}$	11.2 K/kW	between junction and anode, diode
$R_{T,ch}$	6.0 K/kW	between IGCT and cold-plate, single-face contact
$R_{D,ch}$	6.0 K/kW	between diode and cold-plate, single-face contact
R_{sf}	17.0 K/kW	between contact surface and water, single-face cooling, 3 L/min

Table 3.6: Parameters of the thermal circuit with 4.5 kV asymmetric IGCTs and diodes, and a water-flow rate of 3 L/min

3.2.2.2 RC-IGCT

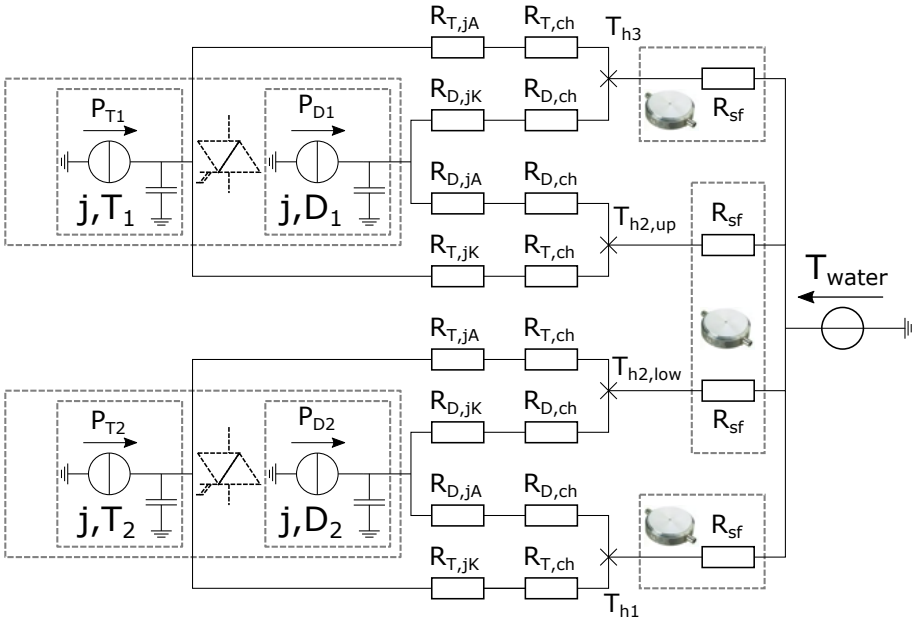


Figure 3.12: Thermal model for a stack of two RC-IGCTs

The thermal modelling of a RC-IGCT is different: there is internal cross-coupling between diode part and GCT part, since they are both on the same wafer. The modelling of these cross-coupling is complex, because the thermal resistances have to be accurately calculated to clearly distinguish it. Hence, internal cross-coupling has been neglected as shown in Figure 3.12, where it has been assumed that the thermal flux from diode and GCT parts to the heatsink are

independent. Such a hypothesis is pessimistic for the estimation of the maximum junction temperature, because in practice internal cross-coupling reduces the equivalent resistance between junction and water. The parameters of this thermal circuit, for 4.5 kV RC-IGCTs, are given in Table 3.7.

Designation	Value	Description
$R_{T,jA}$	18.8 K/kW	between junction and anode, GCT part
$R_{T,jK}$	26.6 K/kW	between junction and cathode, GCT part
$R_{D,jK}$	25.0 K/kW	between junction and cathode, diode part
$R_{D,jA}$	31.8 K/kW	between junction and anode, diode part
$R_{T,ch}$	10.2 K/kW	between GCT part and cold-plate, single-face contact
$R_{D,ch}$	14.4 K/kW	between diode part and cold-plate, single-face contact
R_{sf}	17.0 K/kW	between contact surface and water, single-face cooling, 3 L/min

Table 3.7: Parameters of the thermal circuit with 4.5 kV RC-IGCTs, and a water-flow rate of 3 L/min

3.2.2.3 Press-pack IGBT, BIGT and IEGT

The electrical model of the MMC-HVDC and the thermal model used for IGCT are easily transposable to the other semiconductor devices, seen in 1.3.1. For comparative purposes with existing and relevant technological solutions, three other kind of semiconductors are considered for the power-loss analysis of the fourth chapter: PPI, BIGT and IEGT. It has to be reminded that the thermal model of these semiconductors relies on data-sheet information. So, static and dynamic characterisation contain much less points than in the case of the IGCTs and their related diodes, where specific and extended characterizations have been carried out in the scope of the PhD thesis. Consequently, the results are potentially less accurate, and cannot be experimentally confirmed. The thermal models for these three types of semiconductors are presented in Appendix B.

3.2.3 External arm for power-loss calculation

Limitation of the AVM Table 3.8 summarizes the different targets of each model: the AVM is capable of reproducing the waveforms of the MMC, as well as the DM. Yet, semiconductor losses cannot be calculated with the AVM alone: as previously presented in Figure 3.5, there are no switches any more in this model. It implies that another model dedicated to power-loss calculation must run in addition to the AVM. Meanwhile, it has been demonstrated that among the N SMs of the same arm, the distribution of on-state and switching losses can have a non-negligible standard deviation due to the low-frequency operation of the MMC-HVDC [190]. As a consequence, it is mandatory to calculate the power losses of the N SMs to obtain consistent results.

Then, an external arm is introduced in addition to the AVM, as presented in Figure 3.13. This arm aims to accurately reproduce the capacitor voltages $\underline{v_{SM}}$, and the commutation orders $\underline{com}$, necessary to calculate the power losses of the devices $T^i{}_1$, $T^i{}_2$, $D^i{}_1$, and $D^i{}_2$, $i \in [1, N]$. Even though 4N devices have been reintroduced in the simulation model, the resulting computation time is not comparable to the one of the DM. Indeed, there is no coupling between the AVM and the external arm because the AVM is standalone, besides the N SMs operate like N independent choppers. These two properties are supposed to significantly reduce the model's computation time.

In the DM and the AVM, arm-energy balancing is automatic for the reasons developed in 2.4.1. Nevertheless, this property is lost with the external arm, because the current that flows through it is generated by a different model, continuous. Consequently, a manual arm-energy balancing is required: the total energy of the arm is calculated from the N capacitor-voltages $\underline{v_{SM}}$ and compared to the nominal average arm-energy e_{c0} of the AVM, to provide an arm-current $i_{A,mod}$ that keeps the arm-energy constant in steady-state. This arm balancing strategy remains valid as long as $|i_{A,mod} - i_A|$ is not meaningful compared to i_A, typically less than 10 A.

Modeling of...	DM	AVM
...switching transients	no	no
...semiconductor losses	yes	**no**
...SMs balancing	yes	no
...modulation strategy	yes	no
...fault operation	yes	possible
...inner control loops	yes	yes
...voltage and power control	yes	yes

Table 3.8: Features of the DM and the AVM

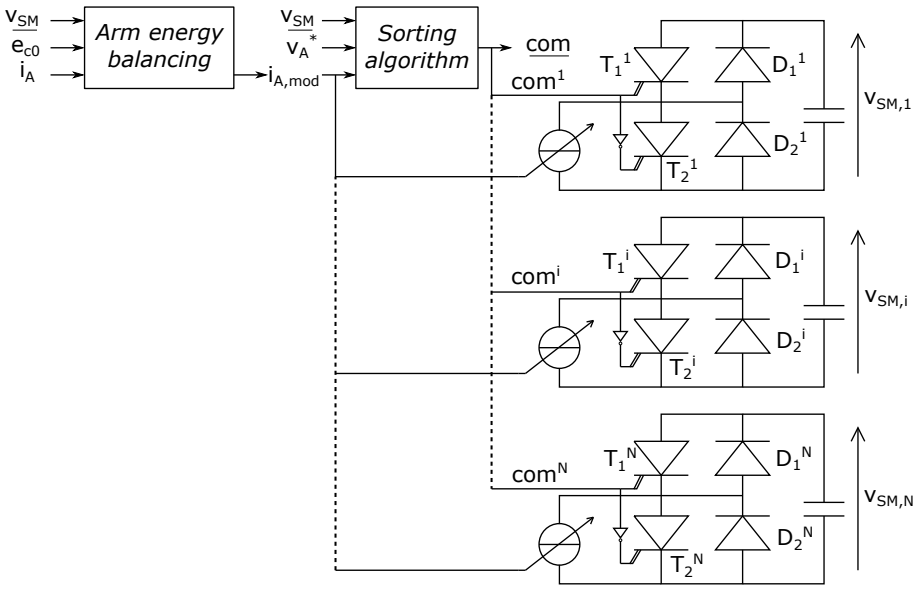


Figure 3.13: External arm, with N half-bridge SMs, to complete the AVM

3.2.4 Clamp circuit and di/dt snubber

Presentation, waveforms and energy losses The clamp circuit and the di/dt choke in an IGCT-based chopper have been presented in 1.3.3.3; and it has been mentioned in 2.1.3 that the clamp circuit dissipates energy when it is triggered. As these power losses result from the use of IGCTs, it is important to consider them and to identify the factors that influence them.

It comes out that the clamp circuit, as represented in Figure 3.14, is triggered by two distinct events, both leading to a current flow through $R_{cl,i}$ [100]:

- When T^i_2 turns off, the di/dt choke initially contains no energy. Because $i_{T2,i}$ decreases, $i_{D1,i}$ increases, inducing a negative di/dt through $L_{cl,i}$ ($v_{lcl,i}<0$), then a charging of the

clamp capacitor $C_{cl,i}$ and a positive current flowing through $R_{cl,i}$, as presented in Figure 3.15, $i \in [1, N]$.

- When D^i_1 turns off, the snubber remains inactive as long as $v_{lcl,i}>0$, i.e. as long as $i_{D1,i}$ decreases. However, the reverse recovery of D^i_1 leads to an excess of energy stored in the di/dt choke. Then, the decrease of the current $i_{lcl,i}$ triggers the clamp circuit, as presented in Figure 3.16, $i \in [1, N]$.

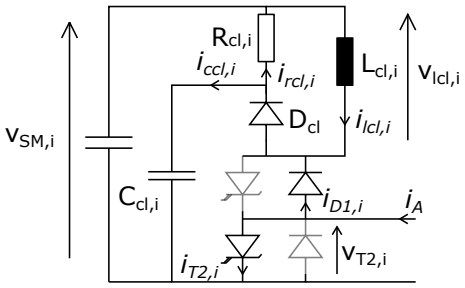
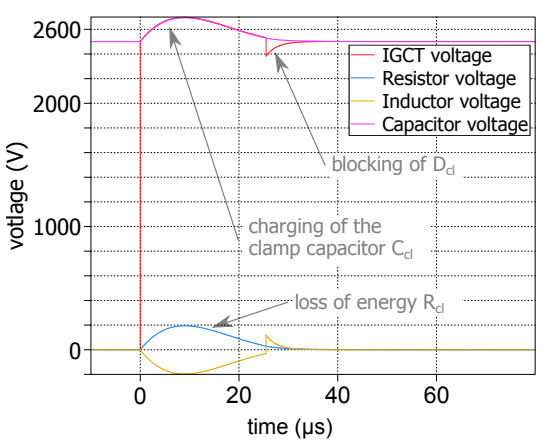
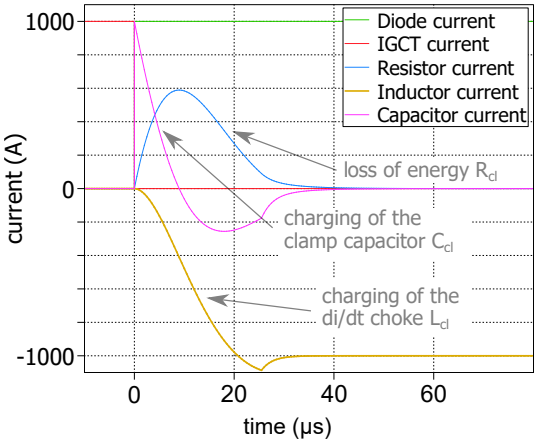


Figure 3.14: Clamp circuit with di/dt choke in the i^{th} SM of a given arm, $i \in [1, N]$

It is also important to observe in Figure 3.16(a) that when D^i_1 starts to turn off, the di/dt choke takes over the whole SM voltage, which drastically reduces IGCT turn-on losses. To represent the waveforms shown in Figure 3.15 and Figure 3.16, IGCT has been modelled as an ideal switch. Besides, $R_{cl,i}$=0.33 Ω, $L_{cl,i}$=3 μH, $C_{cl,i}$=20 μF and diode D^i_1: 5SDF 28L4520 have been considered, $i \in [1, N]$.



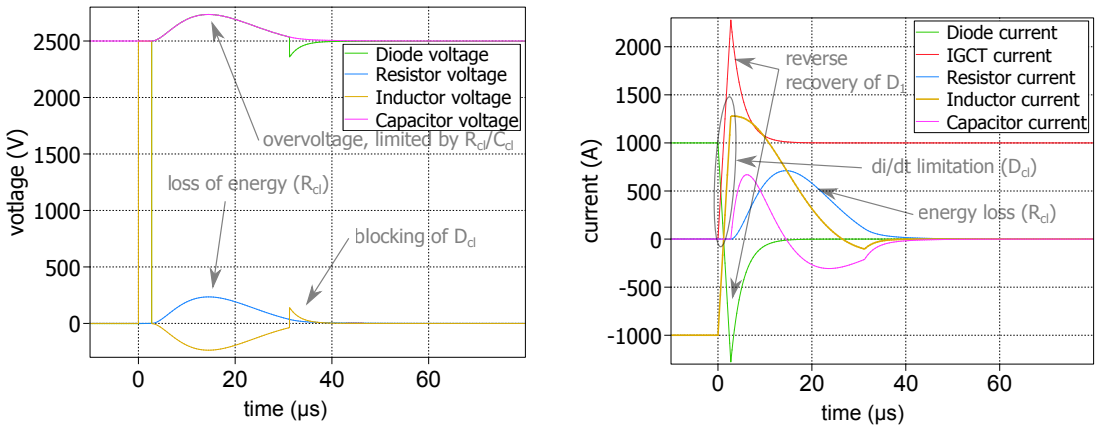
(a) $v_{T2,i}$, $v_{rcl,i}$, $v_{lcl,i}$ and $v_{ccl,i}$



(b) $i_{T2,i}$, $i_{D1,i}$, $i_{rcl,i}$, $i_{lcl,i}$ and $i_{ccl,i}$

Figure 3.15: Waveforms during T^i_2 turn-off: diode D^i_1 (green), IGCT T^i_2 (red), resistor $R_{cl,i}$ (blue), di/dt choke $L_{cl,i}$ (yellow) and clamp capacitor $C_{cl,i}$ (magenta), $i \in [1, N]$

On the necessity of a look-up table It has been proposed to calculate the snubber energy losses with the expressions of the energy stored in the di/dt choke [191]. Nevertheless, the accuracy of this approach has never been proven. On the other hand, the calculation of the energy losses using the waveforms is potentially closer to the reality. Yet, the integration of this circuit's model with the models presented in 3.1.2 and 3.2.3 is not straightforward, because it operates with very small time-constants, typically 1-10 μs, whereas they are higher for the AVM (1-100 ms) and the external arm (10 μs-1 ms). Consequently, a significant increase of the



(a) v_{T2}, $v_{rcl,i}$, $v_{lcl,i}$ and $v_{ccl,i}$ (b) $i_{T2,i}$, $i_{D1,i}$, $i_{rcl,i}$, $i_{lcl,i}$ and $i_{ccl,i}$

Figure 3.16: Waveforms during D^i_1 turn-off: diode D^i_1 (green), IGCT T^i_2 (red), resistor $R_{cl,i}$ (blue), di/dt choke $L_{cl,i}$ (yellow) and clamp capacitor $C_{cl,i}$ (magenta), $i \in [1, N]$

simulation time is expected if the clamp circuit is directly integrated into the existing model, composed of the AVM and the external arm.

In this way, the solution that has been retained is to separately run the model including the clamp circuit, in order to build a look-up table for all the reachable operating conditions of the SM. Afterwards, a look-up table can be loaded for any model, whatever its properties, thus ensuring that the computation time is not deteriorated. Another benefit is that for a given clamp circuit, the same look-up table is used for multiple simulations of converter's operation, which leads to a significant gain of time in the long run. Figure 3.17 proposes an overview of this approach. It can be noticed that during the simulation of the converter's operation, the losses calculation is based on a look-up table.

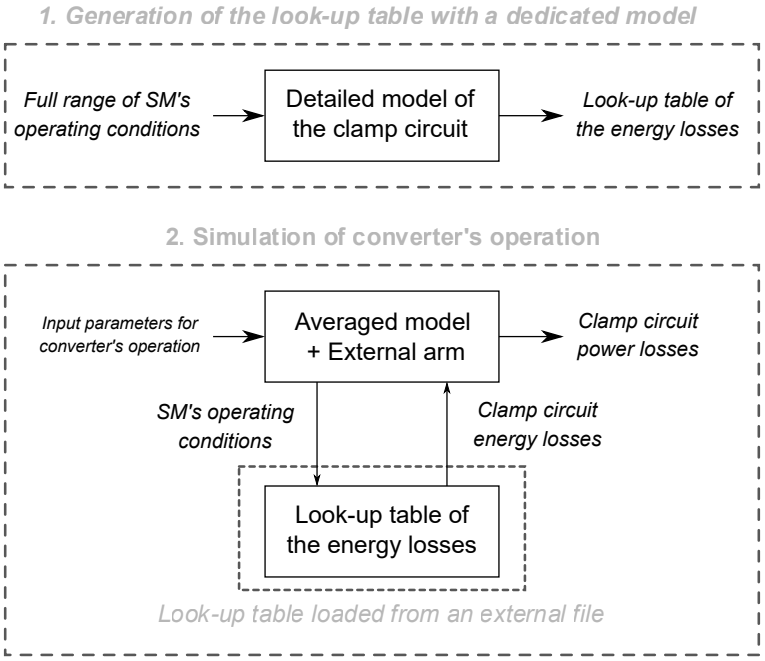


Figure 3.17: Generation and practical use of the look-up table containing the energy losses of the clamp circuit

Factors influencing the clamp circuit energy losses To be both accurate and fast, the look-up table must consider the correct number of input parameters, which corresponds to the "SM's operating conditions" defined in Figure 3.17. Firstly, the look-up table is defined for a single set of components R_{cl}, L_{cl}, C_{cl} and D_{cl}. Then, the arm-current i_A is the primary input parameter since it defines the amount of magnetic energy stored during IGCT turn-off. Another quantity that must be considered is the reverse recovery current I_{rr}: during diode turn-off an excessive amount of energy, proportional to I_{rr}^2, is briefly stored in the di/dt choke then dissipated by the clamp resistor. However, I_{rr} is not naturally available in the main model: it is more convenient to calculate it in the model dedicated to the clamp circuit.

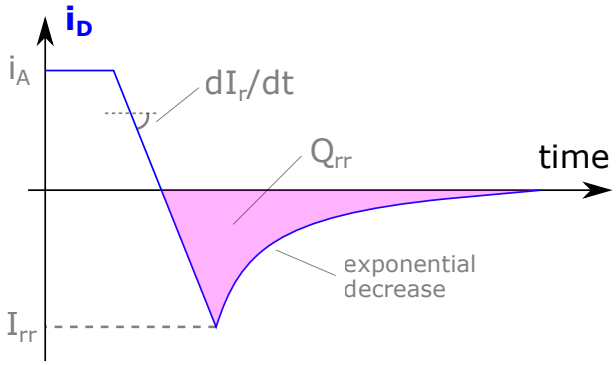


Figure 3.18: Modelling of a diode reverse recovery and notations

The model of reverse recovery in [192] is retained. It requires I_{rr}, the reverse recovery charge Q_{rr}, and the di/dt at turn-off dI_r/dt at a given arm-current i_A, as defined in Figure 3.18, to calculate the model parameters of the diode. It can be noticed that the relation between I_{rr}, Q_{rr}, dI_r/dt and i_A intrinsically depends on the diode. Moreover, dI_r/dt is proportional to the SM voltage V_{SM}, so V_{SM} must be the second input parameter of the look-up table. Consequently, the waveforms shown in Figure 3.16 can be reproduced for a given arm-current, SM voltage and diode part number.

Another important input parameter is the junction temperature of the main diode, involved in the commutation process, $T_{D,j}$, as it affects the relation between I_{rr}, Q_{rr} and i_A. Table 3.9 provides the relative evolution of these three quantities with the junction temperature, it points out the important variations that occurs: +45% for the reverse recovery current and +159% for the reverse recovery charge. Hence, $T_{D,j}$ is used as a third parameter, to adapt the intrinsic parameters of the diode along with i_A and V_{SM}. A model of the clamp circuit, considering the three input parameters, is implemented with the simulation software PLECS. A script is used to modify the input parameters in the beginning of each simulation, and to recalculate the intrinsic parameters of the main diodes.

$T_{D,j}$	dI_r/dt (pu)	Q_{rr} (pu)	I_{rr} (pu)
25°C	1	1	1
75°C	0.99	1.45	1.13
125°C	0.98	2.26	1.37
140°C	1.00	**2.59**	**1.45**

Table 3.9: Relative evolution of the reverse recovery current I_{rr} and the reverse recovery charge Q_{rr} with the junction temperature $T_{D,j}$ from experimental measurements, V_{SM}=2500 V and i_A=1500 A, diode 5SDF 20L4520

3.3 Implementation of the electro-thermal model with MATLAB

3.3.1 Motivations

The full model composed of the AVM of 3.1.2, the external arm of 3.2.3 and the electro-thermal model of the semiconductors of 3.2.2, has been implemented on the simulation software PLECS. Approximately 20 min are necessary to simulate the few seconds of operation necessary to reach the thermal steady-state, with the same computer as in 3.1.1 and for the same number of levels. It is a significant improvement and it makes the estimation of power losses accessible. Yet, the connection of offshore wind-farms is particular, as the transmitted power depends on the wind-speed. It means that the converter-stations must experience many operating conditions, due to the natural variations of wind-speed. Consequently, a large number of operating conditions have to be simulated, to reproduce the profile mission of the offshore wind-farms. This observation leads to another conclusion: a further reduction of the model's computation time is required to reproduce the mission profile as precisely as possible, in a given time interval. To figure it out, the AVM, the external arm and the electro-thermal model of the semiconductors have been implemented with MATLAB, which aims to accelerate the calculations through different techniques.

In the current model and especially after the simplification of the AVM, the external arm is the slowest part: it requires small time-steps, because of the large number of commutations. Since the maximum time-step is the sampling period $\frac{1}{f_s}$, one way to reduce the computation time is to use a fixed time-step, equal to the sampling period. Then, simulation issues have been encountered with PLECS: the simulation software does not provide consistent results because of the sorting algorithm. Using a variable-time step, PLECS generates approximately 4 time-steps per sampling period, whereas only one should be enough. Another limitation of PLECS is the thermal modelling, that cannot be vectorized. This concept, mentioned in 3.1.1, is powerful due to the large number of levels. Without it, the full implementation of the thermal models presented in 3.2.2 is not possible. On the other hand, MATLAB allows to represent the state-variables of all the SMs in matrices, thus performing fast matrix calculations.

3.3.2 Simplification of the AVM with analytic expressions

The AVM of the converter is a simplified version of the DM, leading to a continuous model with a reduced number of components which can be analytically described. As presented in 3.2.3, only three quantities from the AVM are required: the arm-current i_A, the reference arm-voltage v^*_A and the average arm-energy e_{c0} of a given phase. The use of analytic expressions provides more flexibility, as it reduces the interactions with the simulation software and MATLAB. Appendix A presents the necessary equations and the different steps leading to the expression of i_u, v^*_u and e_{cu0} in steady-state, considering the upper arm of any phase, the result being similar with any lower arms.

3.3.3 Structure of the simulation tool

The model is implemented with MATLAB and simulated with a fixed time-step, Figure 3.19 provides an overview of the resulting simulation tool. In terms of structure, it can be noticed that the electrical waveforms are calculated prior to the main calculation loop, which is only dedicated to simulate the external arm and the thermal circuit. The simulation tool has three initial steps:

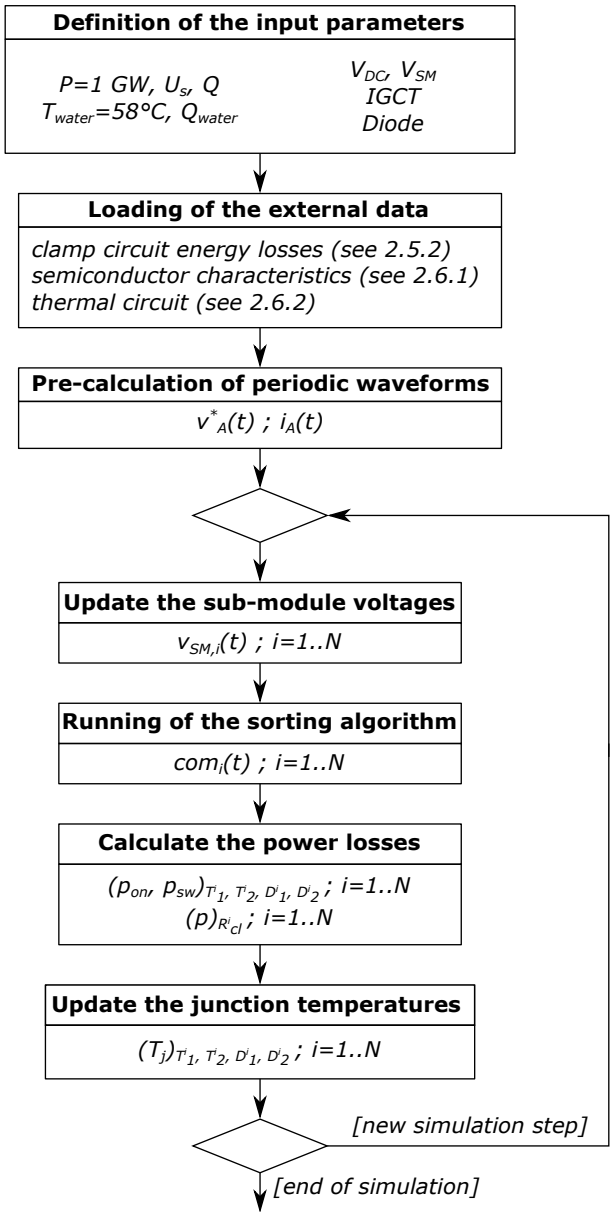


Figure 3.19: Flowchart of the simulation tool implemented with MATLAB

Definition of the input parameters The converter is defined from the main electrical quantities such as active and reactive powers, DC link voltage and AC grid voltage. The thermal circuit is also concerned, the water temperature T_{water}, as defined in 3.2.2, and the water flow are selected. Regarding the devices, the relation between the DC link voltage, the SM voltage V_{SM} and the semiconductor voltage rating follows the principles developed in 2.2.2.2.

Loading of the external data The simulation tool loads external data such as the clamp circuit energy losses, which are gathered in look-up tables as seen in 3.2.4, but also the static and dynamic characteristics of the semiconductor devices as described in 3.2.1. The thermal circuit is also loaded, it comprises the thermal resistances that are inherent to the semiconductors used.

Pre-calculation of the periodic waveforms The simplified averaged model, as described in 3.3.2, and based on the analytic expressions of Appendix A, is implemented.

Afterwards, the scripts enters the main calculation loop, which includes four major steps:

Update of the SM voltages The capacitor-voltages $v_{SM,i}(t)$ of the N SMs are calculated, using an forward Euler approximation:

$$v_{SM,i}(t_k) = v_{SM,i}(t_{k-1}) + \frac{1}{C} i_A(t_{k-1}),\ i \in [1, N] \tag{3.2}$$

Running of the sorting algorithm The sorting algorithm is run, using the capacitor-voltages updated during the same time-step. It generates the new commutation orders, $(com_i(t))_{i\in[1,N]}$

Calculation of the power losses This step gathers the calculation of on-state losses, switching losses and clamp circuit power losses. For the i_{th} SM, the commutation order $com_i(t_k)$ and the arm-current i_A are used to identify the devices that conduct or switch: this technique reduces the number of operations to perform. For on-state losses, (3.3) is used to calculate the voltage drop at given junction temperature and arm-current:

$$\begin{aligned} &v_{on}(T_j, i_A) = (1 - a_l - a_m + a_l a_m) v_{on,table}(l, m) + \\ &(a_l - a_l a_m) v_{on,table}(l+1, m) + \\ &(a_m - a_l a_m) v_{on,table}(l, m+1) + \\ &a_l a_m v_{on,table}(l+1, m+1) \end{aligned} \tag{3.3}$$

(3.3) corresponds to a bilinear interpolation of the look-up table $v_{on,table}$, with the notations defined in Figure 3.20. The same principle is applied to approximate switching losses and clamp circuit power losses, with an additional dimension due to the SM voltage dependency; bilinear interpolations turn into trilinear interpolations.

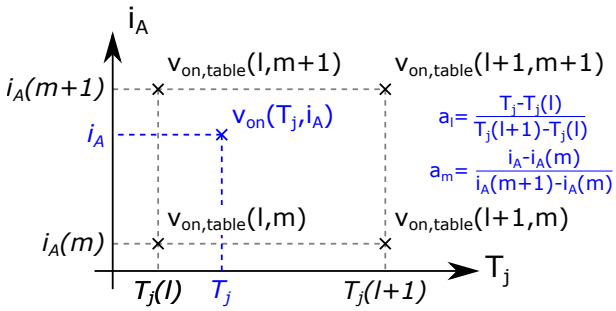


Figure 3.20: Bilinear interpolation of the on-state voltage with the simulation tool; notations

Update of the junction temperatures The thermal model consisting of an RC network is turned into a first-order relation between power losses and junction temperature, allowing a calculation of junction temperatures with forward Euler approximation.

Other features Arm-energy balancing is performed as presented in 3.2.3. In the end of each simulation, the capacitor-voltages, the power losses, the junction temperatures and the average switching frequency are saved within a single datafile, which facilitates the post-processing.

3.3.4 Performances and validation of the simulation tool

It is possible to consider the actual ratings of the converter-stations, without applying a scaling factor, as presented in Table 3.10.

Power	V_{DC}	N	U_s	C	L_{arm}
1 000 MW	±320 kV	256	333 kV	10.2 mF (45.5 kJ/MVA)	63.5 mH

Table 3.10: Main characteristics of the converter-stations considered for the validation of the simulation tool

3.3.4.1 Evolution of the average arm-energy

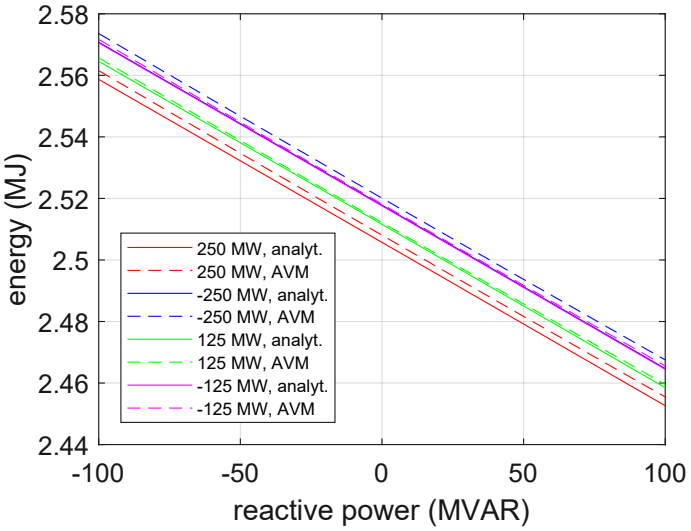


Figure 3.21: Evolution of the average arm-energy e_{c0} with the reactive power, for different active powers, using the AVM and the analytic expression

The external arm, introduced in 3.2.3, requires arm-energy balancing, as well as the simulation tool implemented with MATLAB. For given operating conditions, the average arm-energy must be equal to e_{c0} to have a consistent operation. Yet, it has been proven through the analytic developments of Appendix A that e_{c0} is different from $\frac{1}{2}C_e V_{DC}^2$. Besides, it varies with the passive elements of the model. To validate this expression, the analytic evolution of the average arm-energy has been represented in Figure 3.21 with the evolution obtained from the AVM. It can be observed that at a given power, the variation is not negligible as it can reach 2.5% of the nominal arm-energy. This difference leads to balancing issues if the value of e_{c0} is assumed constant. It can be observed that the analytic expression provides an accurate estimation of e_{c0} for the different active and reactive powers: the maximum relative error remains inferior to 0.15%. Figure 3.22 confirms these observations, the analytic estimation of the average arm-energy e_{c0} is accurate since it leads to a negligible arm-current deviation with the simulation tool, inferior to 1 A: arm-energy balancing is properly carried out.

3.3.4.2 Distribution of power losses in an arm and average power losses

As explained in 3.2.3, the semiconductor devices experience various electrical stresses: the N devices $(T_1^i)_{i\in[1,N]}$ exhibit different on-state losses and switching losses. This phenomenon is negligible, as soon as the modulating frequency, here 50 Hz, is much lower than the carrier frequency or more generally the average switching frequency. A factor 20 is deemed sufficient. Nevertheless, these conditions are not met with an HVDC-MMC, because the average switching frequency is only 1-4 times larger than the modulating frequency.

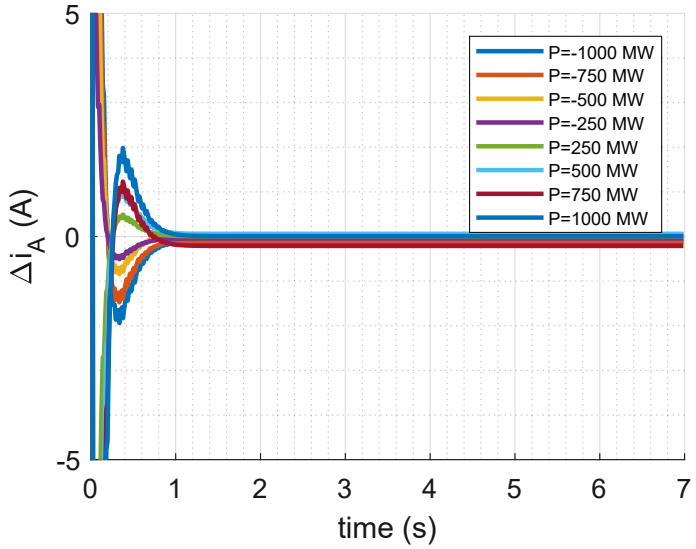
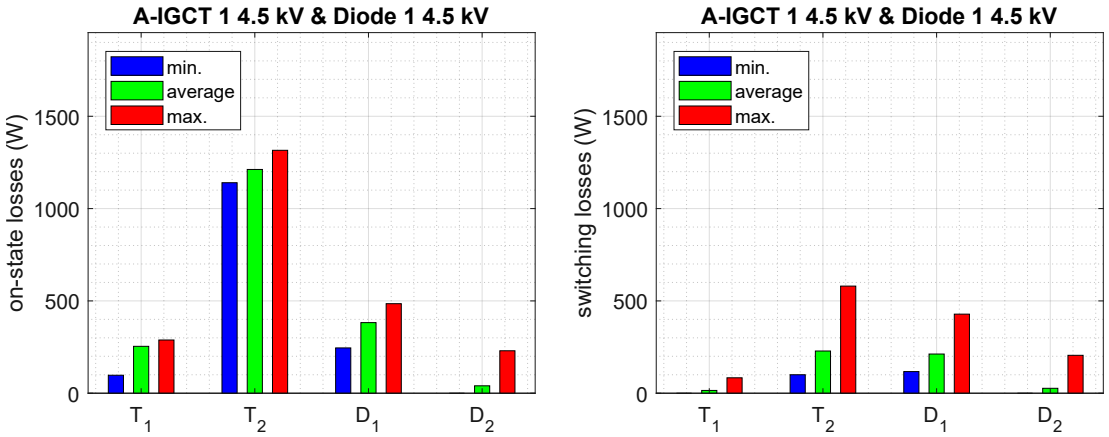


Figure 3.22: Evolution of the arm-current deviation $\Delta i_A = i_{A,mod} - i_A$, to ensure arm-energy balancing with the simulation tool



(a) Minimum, average and maximum on-state losses of $(T_1^i)_{i\in[1,N]}$, $(T_2^i)_{i\in[1,N]}$, $(D_1^i)_{i\in[1,N]}$ and $(D_2^i)_{i\in[1,N]}$

(b) Minimum, average and maximum switching losses of $(T_1^i)_{i\in[1,N]}$, $(T_2^i)_{i\in[1,N]}$, $(D_1^i)_{i\in[1,N]}$ and $(D_2^i)_{i\in[1,N]}$

Figure 3.23: Minimum, average and maximum on-state losses and switching losses of $(T_1^i)_{i\in[1,N]}$, $(T_2^i)_{i\in[1,N]}$, $(D_1^i)_{i\in[1,N]}$ and $(D_2^i)_{i\in[1,N]}$

Figure 3.23 points out the consequences of this particular mode of operation: the deviation between the minimum power losses and the maximum power losses is significant. It demonstrates that for low switching frequencies, all the SMs of the arm must be considered to calculate the power losses with a reasonable accuracy. Consequently, the average on-state losses and the average switching losses per device are retained as the most relevant quantities, leading to the representation of Figure 3.24.

3.3.4.3 Extraction of the junction temperature

Significant variations between minimum and maximum power losses are not reported on the junction temperatures; Figure 3.25(a) shows that the deviation is limited to a few hundreds of

millidegrees. This result is positive as it demonstrates that the semiconductors endure similar thermal stresses, which avoid premature ageing and permanent thermal cycling of the components. The calculation of the junction temperatures, based on RC networks, has a time-constant as shown in Figure 3.25(b). This time-constant is necessary to avoid non-realistic variations of the junction temperatures over a grid period. It implies that steady-state must be reached to retrieve consistent junction temperatures: Figure 3.25(b) proves that the duration of simulation is sufficient.

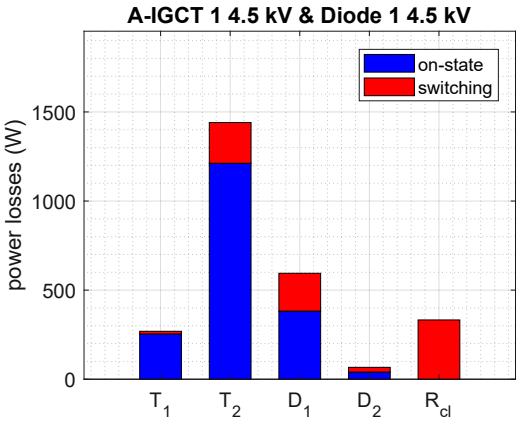
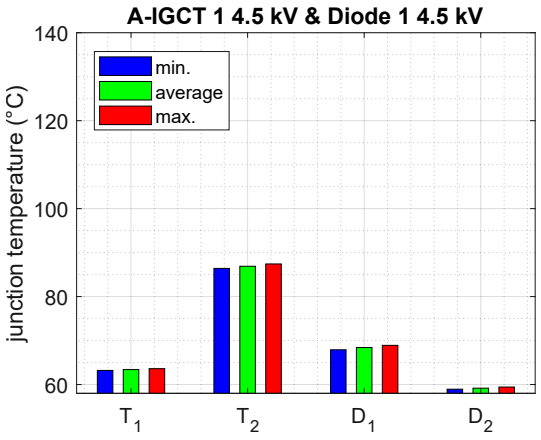
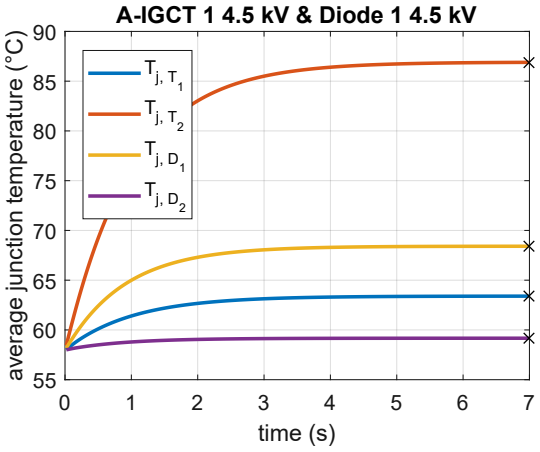


Figure 3.24: Average power losses of $(T_1^i)_{i\in[1,N]}$, $(T_2^i)_{i\in[1,N]}$, $(D_1^i)_{i\in[1,N]}$ and $(D_2^i)_{i\in[1,N]}$



(a) Minimum, average and maximum junction temperatures of $(T_1^i)_{i\in[1,N]}$, $(T_2^i)_{i\in[1,N]}$, $(D_1^i)_{i\in[1,N]}$ and $(D_2^i)_{i\in[1,N]}$



(b) Temporal evolution of the average junction temperatures T_{j,T_1}, T_{j,T_2}, T_{j,D_1} and T_{j,D_2}, obtained with the simulation tool

Figure 3.25: Minimum, average and maximum junction temperatures of $(T_1^i)_{i\in[1,N]}$, $(T_2^i)_{i\in[1,N]}$, $(D_1^i)_{i\in[1,N]}$ and $(D_2^i)_{i\in[1,N]}$, and temporal evolution of the average junction temperatures

Figure 3.26 provides an overview of the thermal stresses experienced by the semiconductors. In rectifier operation (P<0), the diodes $(D_2^i)_{i\in[1,N]}$ conduct the arm-current at low duty-cycle, i.e. when it is close to its maximum, which increases both on-state and switching losses, so T_{j,D_2} is the highest junction temperature. On the other hand, in inverter operation (P>0), the device T_{j,T_2} conduct the arm-current at low duty-cycle, i.e. when it is close to its maximum, which increases both on-state and switching losses, so T_{j,T_2} is the highest junction temperature.

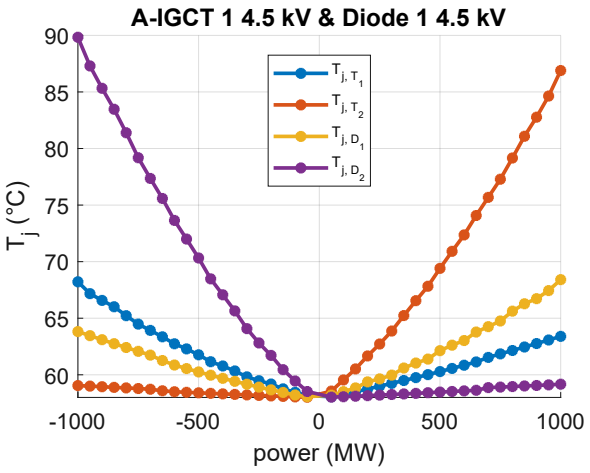


Figure 3.26: Evolution of the average junction temperatures T_{j,T_1}, T_{j,T_2}, T_{j,D_1} and T_{j,D_2} with the transmitted power, Q=0

3.3.5 Conclusions regarding the simulation tool implemented with MATLAB

The simulation tool is able to provide all the necessary quantities, electrical and thermal, within 30 seconds. It is 40 times faster than the original solution, composed of the AVM of 3.1.2 with the external arm of 3.2.3. Meanwhile, the accuracy of the simulation tool is excellent: a comparison of the power losses and the switching frequency with the original model has shown a modelling error lower than 0.5%, which is admissible regarding the gain of computation time. Therefore, the simulation tool is retained to proceed to the power-loss analysis of next chapter.

3.4 Conclusion

A focus has been made on converter modelling. The general DM is not suitable to carry out a power-loss analysis due to its unreasonable computation complexity. On the other hand, the AVM is much faster with a negligible error modelling. To build an accurate electro-thermal model of the SMs, experimental measurements have been realized on the semiconductor devices, in a way that facilitates a parametric approach. Currents, junction temperatures and SM voltages have been selected according to the converter design, as presented in the second chapter. The cooling system has been modelled using RC networks, allowing a simpler implementation of the multi-physical model.

The modelling of the SM has been pushed forward with an electro-thermal model of the clamp circuit, inherent to the use of IGCT. A detailed model considering the thermal stress endured by the diodes has been developed to provide accurate clamp circuit power losses, valid for a wide range of operating conditions. The concept of external arm, in addition to the AVM, has been introduced to accelerate the calculation of the power losses with a simulation software. Yet, the resulting computation time has come to be too large. An integration with MATLAB has been carried out to speed up the previous model even more, and to implement the thermal model with more accuracy. The operation of the corresponding simulation tool has been validated, including the execution of the sorting algorithm along with the calculation of power losses and the junction temperatures. With an acceleration factor of 40, the simulation tool provides all the necessary quantities to perform a thermal design of the semiconductor devices with the cooling system.

The results of this chapter, leading to the development of the simulation tool, are the cornerstone that can lead to a relevant power-loss analysis: accuracy and speed have been kept in the multi-physical model, where a limited number of simplifying hypotheses have been formulated. The fourth chapter is dedicated to the power-loss analysis of the semiconductor devices introduced in this chapter, for the converter-stations whose design has been presented in the second chapter.

Chapter 4

Power-loss analysis in the HVDC converter-stations

4.1 Modelling of the offshore wind park

4.1.1 Problematic, approach

The electro-thermal model of the SMs developed in the third chapter, based on the design proposed in the second chapter, allows to calculate the power losses of the two converter-stations for any operating conditions. Yet, the very same operating conditions depend on the power produced by all the WTGs of the offshore wind park(s), connected to the HVDC link at every instant. Furthermore, the wind is an intermittent source of energy: the power production significantly varies over time, due to the evolution of the meteorological conditions. Consequently, the calculations of the power losses must cover all the reachable operating conditions of the two converter-stations, defined by the characteristics of the offshore wind-park(s).

The key quantity to observe is the wind-speed measured in the axis of the WTGs, since it is responsible for the variations of the operating conditions. Typically, two approaches can be distinguished to describe the operating conditions of the converter-stations:

1. A temporal approach, where a "mission profile" is defined, based on experimental measurements of wind-speeds on the field. The evolution of the wind-speed with time allows to calculate the temporal evolution of the power losses of the two converter-stations. Assuming a sufficient time span, the power losses can be averaged to obtain an accurate estimation of the efficiency, only valid for the given mission profile.

2. A statistical approach, which also requires experimental measurements of wind-speeds on the field. From the mission profile, the occurrence of each wind-speed is used to define a probability, leading to a probability density function describing the evolution of the wind-speed in the frequency domain.

The second approach is more common for wind energy [193]. The wind-speeds are assimilated to an existing probability density function, thus allowing to describe the evolution of the wind-speeds with only a few parameters.

4.1.2 Statistical distribution of the wind-speeds

A two-parameter Weibull distribution is selected: though limited compared to four and five parameter distributions, the two-parameter Weibull distribution is a simple way to model the

distribution of wind-speeds [194]. The corresponding probability density function is given by (4.1):

$$f(v) = \frac{K}{A}\left(\frac{v}{A}\right)^{K-1} e^{-\left(\frac{v}{A}\right)^{K}} \tag{4.1}$$

where K=2.2 and A=10.57 m.s^{-1} have been retained [195]. K is the shape factor and A the scale factor. The corresponding function is shown in Figure 4.1. The dots represent the sampling of the function retained to approximate it: the step is not linear since it is based on the wind turbine power curve, introduced hereinafter.

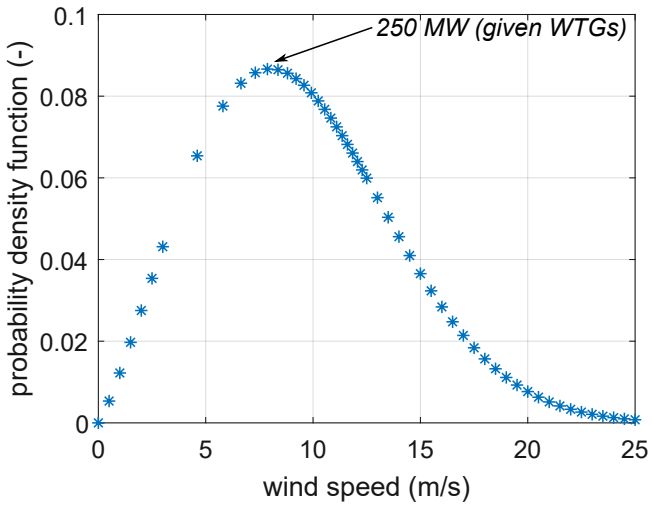


Figure 4.1: Probability-density function considered to assess the power losses in the two terminal-converters of the HVDC link

4.1.3 Wind turbine power curve

The second step is to link the wind-speed, given by the statistical distribution of Figure 4.1, with the power generated by the offshore wind park(s). The corresponding characteristic depends on many parameters such as the wind turbine's aerodynamic properties, the electromechanical energy conversion system, cut-in and cut-off wind-speeds. Cut-in and cut-off wind-speeds are typically 3 m.s^{-1} and 25 m.s^{-1}, respectively [196]. Many mathematical models exist, based on the characteristics provided by wind turbine manufacturers [197]. A cubic approximation with a saturation at maximum power has been retained [198], normalized by the maximum power of the HVDC link, i.e. 1 GW, as shown in Figure 4.2. A spacing of 5% of the maximum power is chosen between two successive samples. This approach though simple remains relevant. Besides, it is independent from the number and the arrangement of the offshore wind park(s) with their corresponding WTGs.

4.1.4 Calculation of the averaged power losses

An averaged quantity X, obtained from a given function x(v) depending on the wind-speed v, is given by:

$$X = \int_0^{+\infty} x(v)f(v)dv, \text{ where } \int_0^{+\infty} f(v)dv = 1 \tag{4.2}$$

where x can represent the on-state losses or the switching losses of any device, the clamp circuit power losses or simply the power produced by the offshore wind park(s). Then, it is not possible to have a continuous representation of x, as it is obtained from a finite number of simulations:

x is discrete. Therefore, the integral formulation of (4.2) is turned into a sum, thanks to a trapezoidal approximation:

$$X \approx \sum_{k=1}^{+\infty} \frac{1}{2} \left(x_k f(v_k) + x_{k-1} f(v_{k-1}) \right) (v_k - v_{k-1}) \tag{4.3}$$

(4.3) can be reduced to a finite sum: as explained in 4.1.3, a cut-off wind-speed 25 m.s^{-1} has been retained. It implies that the production stops if the wind-speed comes to exceed this upper boundary. Moreover, the energy production is null below the cut-in wind-speed, which leads to the following simplification:

$$X \approx \sum_{k=1}^{M} \frac{1}{2} \left(x_k f(v_k) + x_{k-1} f(v_{k-1}) \right) (v_k - v_{k-1}) \tag{4.4}$$

where M is the number of points from 3 m.s^{-1} to 25 m.s^{-1}, as presented in Figure 4.1 and Figure 4.2. Twenty operating conditions are simulated, which produces M=45. It leads to an average power production of the offshore wind park(s) equal to 468 MW, i.e. a capacity factor of 46.8%, which is consistent with existing systems [195, 198].

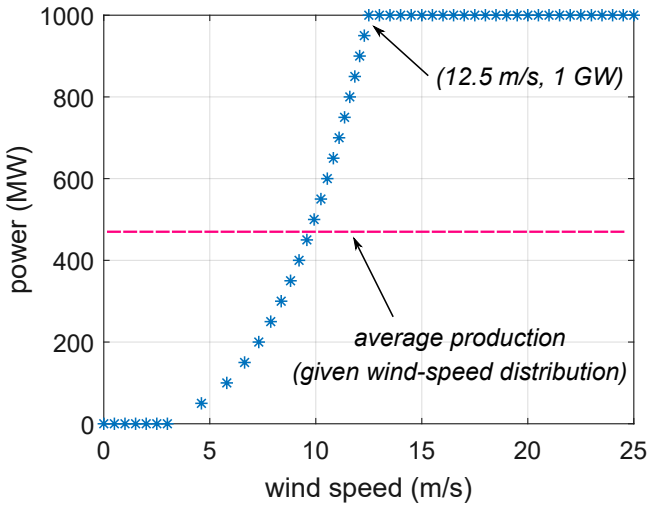


Figure 4.2: Wind turbine power curve normalized by the maximum power of the HVDC link, i.e. relation between the power produced by the offshore wind park(s) and the wind-speed

4.1.5 Parameters of the converter-stations

Table 4.1 presents the electrical and thermal parameters retained for the study. It is based on the considerations aforementioned in 1.1.3 regarding the modulation index and the reactive power, 2.2.1 regarding the energy stored in the converter and the arm inductance, and 2.2.2.2 regarding the DC link voltage and the number of SMs per arm. The modulation index of the offshore HVDC converter-station is constant and equal to 0.85. However, the modulation index of the onshore HVDC converter-station, operating as a rectifier, must be variable according to the grid codes: ±5% of the nominal modulation index is retained from TenneT's grid code [24]. Third-harmonic voltage injection, which consists in increasing the maximum modulation index from 1 to $2/\sqrt{3}$, has not been carried out. This choice implies that the arm-currents are approximately 10% higher, leading to a more restrictive design of the converter. Consequently, for a DC link voltage of ±320 kV, the whole P-Q profile must be reachable for a grid voltage U_s from

Name	Symbol	Value
Maximum power	P_{max}	±1 000 MW
DC link voltage	V_{DC}	from ±320 kV to ±600 kV
Number of SMs per am	N	from 137 to 256
Modulation index	m_a	from 0.8 to 0.9
Maximum reactive power	Q_{max}	±400 MVAR (inverter only)
Energy stored in a converter	-	45.5 kJ/MVA
Cooling water temperature	T_{water}	58°C
Water flow	Q_{water}	3 L/min

Table 4.1: Electrical and thermal parameters of the converter-stations using IGCTs

313 kV to 352 kV, between the onshore HVDC converter-station and the converter transformers.

Regarding the water cooling of the semiconductors, an ambient temperature of 50°C is assumed, with a rise in the cooling water of 8°C according to Hitachi ABB. The water flow must be specified, as it defines the value of the thermal resistance R_{sf}, introduced in 3.2.2. Then, a vacuum brazed cold plate from DAU is retained, which has a single-face thermal resistance of 17 K/kW.

4.2 Power losses of the HVDC stations, V_{DC} fixed

As presented in Table 4.2, the voltage V_{DC} is set to ±320 kV, whereas the number of SMs decreases with the semiconductor voltage rating. This first comparative study focuses on the currently available technologies of XLPE cables for such projects, allowing a nominal DC link voltage of 320 kV per pole. The increase in semiconductor voltage rating reduces the number of devices, but it necessarily increases both on-state and switching losses: a trade-off has to be found.

V_{DC}	±320 kV	±320 kV	±320 kV
V_{DRM} (kV)	4.5	6.5	10
min. N	256	178	137

Table 4.2: Different numbers of SMs per arm for the same DC link voltage and different semiconductor voltage ratings, according to 2.2.2.2

4.2.1 10 kV IGCTs

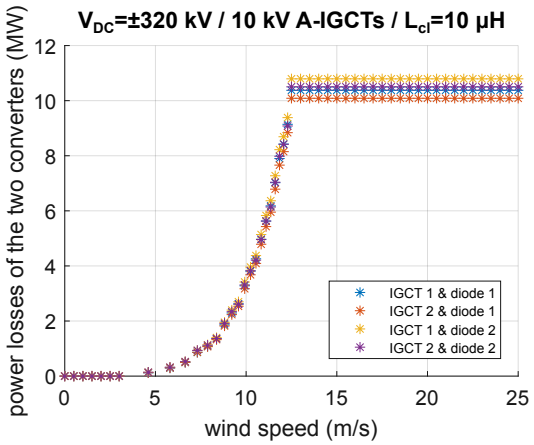
Table 4.3 regroups the 10 kV devices retained for the power-loss analysis, already introduced in 3.2.1. Since devices with low on-state losses have high switching losses, the devices of Table 4.3 are sorted according to their switching capabilities. It means that the device with the highest number is best suited for low frequency operation, i.e. it has the lowest on-state losses of the available devices. On the other hand, the device with the lowest number (A-IGCT 1 10 kV and diode 1 10 kV in Table 4.3) is better suited for high switching frequency. This allows the comparison of similar semiconductors with identical voltage ratings, to study the consequences of different trade-offs between on-state losses and switching losses. This concept is developed in [199], it is directly linked with the technology curve of the devices. IGCTs with different properties are obtained depending on the irradiation level used for carrier life-time control.

Consequently, "high" designates devices with a high irradiation, "medium" corresponds to a moderate irradiation level, and "very low" is equivalent to an un-irradiated device.

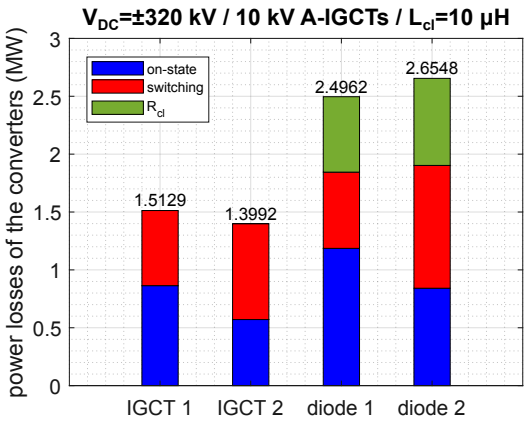
Part number	Designation	max. T_j	best-suited f_{sw}
5SHY 17L9000	A-IGCT 1 10 kV	115°C	medium
5SHY 17L90xx	A-IGCT 2 10 kV	115°C	very low
5SHX 20L8500	RC-IGCT 1 10 kV	125°C	low
5SDF xL9000	diode 1 10 kV	125°C	medium
5SDF xL90xx	diode 2 10 kV	125°C	very low

Table 4.3: Reminder - list of the 10 kV devices characterized and retained for the power-loss analysis

4.2.1.1 10 kV asymmetric devices



(a) Evolution of the power losses with the wind-speed, for the given wind turbine power curve of Figure 4.2 and for different 10 kV asymmetric devices



(b) Averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, for different 10 kV asymmetric devices

Figure 4.3: Evolution of the power losses with the wind-speed and averaged power losses of the two converter-stations, for different 10 kV asymmetric devices, with V_{DC}=±320 kV

The power losses of both converter-stations are calculated for the different wind-speeds, leading to the results of Figure 4.3(a). Power losses stay constant from 12.5 m.s^{-1} to 25 m.s^{-1}, because the converter-stations transfer the maximum power of 1 GW, according to the characteristic of Figure 4.2. The power losses depend on the semiconductors used. It appears that the couple IGCT 2/diode 1 minimizes the power losses at full power. Nevertheless, it is mandatory to consider the statistical distribution of wind-speeds to conclude.

Afterwards, the calculation steps from 4.1.4 are applied. The power losses are represented per device (IGCT/diode) and per nature (on-state/switching) in Figure 4.3(b), for each possible couple of devices listed in Table 4.3. It must be noted that on-state (or switching) losses of a given device regroups on-state (or switching) losses of the 12N devices per converter-station, since there are two identical devices per SM, which means that the 24N devices of the two converter-stations are taken into account.

The trade-off between on-state losses and switching losses can be clearly observed; however, it leads to different conclusions. Concerning IGCTs, IGCT 2 is the best choice which demonstrates that a device with a "very low" best-suited switching frequency f_{sw} is relevant. On the other hand, diode 1, which has a "medium" best-suited f_{sw}, minimizes the power losses. The switching losses are more significant for the diode, which requires a device with a higher best-suited f_{sw}. Moreover, the poor switching performances of diode 2 increases the clamp circuit power losses as well, due to the rise in the reverse-recovery current I_{rr} (for the reasons presented in 3.2.4). The couple IGCT 2/diode 1 still comes out as the best choice of semiconductors, leading to 3.89 MW power loss, averaged by considering a given wind-speed distribution. It corresponds to an efficiency of 99.53% for the rectifier and an efficiency of 99.63% for the inverter; these figures are based on an average power production of 468 MW, without considering the other sources of power losses in the converter-stations. At this stage, the results show that 10 kV IGCTs with discrete diodes embody a potential technological solution to equip such HVDC converter-stations. They benefit from reasonable power losses, and offer a drastic reduction of the number of SMs.

The electro-thermal model developed combined with the statistical description of the wind-speeds unveil that the selection of the best semiconductors is meaningful: a comparison between the best couple, IGCT 2/diode 1, and the worst couple, IGCT 1/diode 2, shows a difference of energy loss equal to 2.4 GWh per year of exploitation.

4.2.1.2 10 kV reverse-conducting devices

The 10 kV RC-IGCT has an insufficient SOA for the operating conditions defined: the maximum controllable turn-off current, 1800 A, is exceeded at full power and maximum reactive power. It is studied in the next section, where the arm-currents are lower.

4.2.2 4.5 kV IGCTs

Part number	Designation	max. T_j	best-suited f_{sw}
5SHY 40L4511	A-IGCT 1 4.5 kV	140°C	high
5SHY 35L4510	A-IGCT 2 4.5 kV	140°C	medium
5SHY 55L4500	A-IGCT 3 4.5 kV	140°C	low
5SHY 55L45xx	A-IGCT 4 4.5 kV	140°C	very low
5SDF 20L4520	diode 1 4.5 kV	140°C	medium
5SDF 28L4520	diode 2 4.5 kV	140°C	low
5SHX 36L4520	RC-IGCT 1 4.5 kV	125°C	medium
5SHX 35L4521	RC-IGCT 2 4.5 kV	125°C	low

Table 4.4: Reminder - list of the 4.5 kV devices characterized and retained for the power-loss analysis

4.2.2.1 4.5 kV asymmetric devices

4.5 kV devices are more common in the field of HVDC-VSC systems, since 4.5 kV IGBTs equip several HVDC converter-stations. The devices from Table 4.4 are considered in Figure 4.4. IGCT 2 comes out as the best IGCT. Besides, an interesting phenomenon must be noticed: this device has a "medium" best-suited f_{sw}, whereas the IGCTs next to it have a "high" and a "low" best-suited f_{sw}. It confirms that the use of 4.5 kV IGCTs is relevant for this application, this observation would not have been possible with a comparison involving less than three IGCTs.

The two diodes exhibit similar performances, despite a different distribution between on-state losses and switching losses. The best couple, IGCT 2/diode 1, leads to 3.58 MW power loss, which is inferior to the previous results with the 10 kV devices. It can be concluded at this stage that the use of high-performance devices in great number overtakes the use of high-voltage devices in reduced number, regarding the efficiency of the system, for this specific study case.

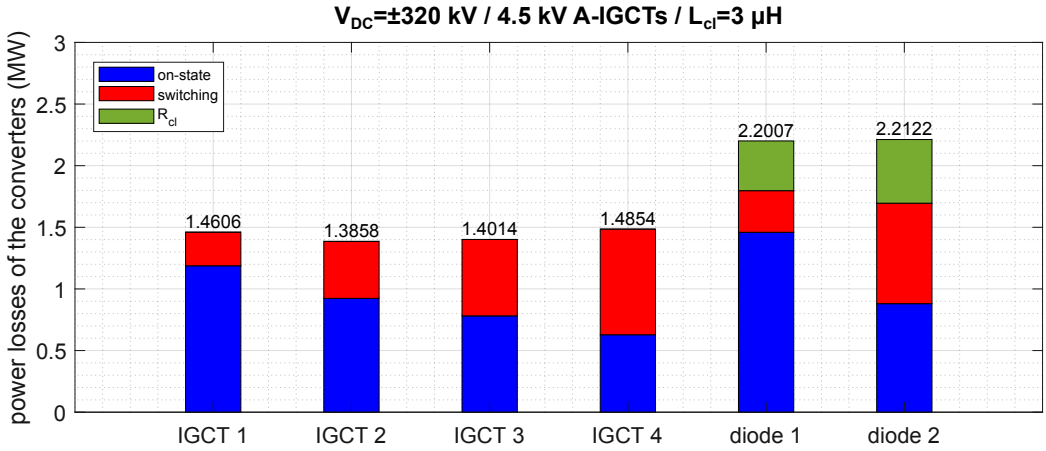


Figure 4.4: Averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, for different 4.5 kV asymmetric devices, with V_{DC}=±320 kV

4.2.2.2 4.5 kV reverse-conducting devices

The power losses of the RC-IGCTs from Table 4.4 are presented in Figure 4.5. RC-IGCT 2 exhibits the best performances. The differences between the two RC-IGCTs are mainly due to the GCT part: the reduction of the GCT on-state losses obtained with RC-IGCT 2 is important. 3.69 MW of power losses are obtained, which is not a significant increase compared to the 4.5 kV asymmetric devices. On the other hand, the gain in terms of CAPEX and volume is meaningful.

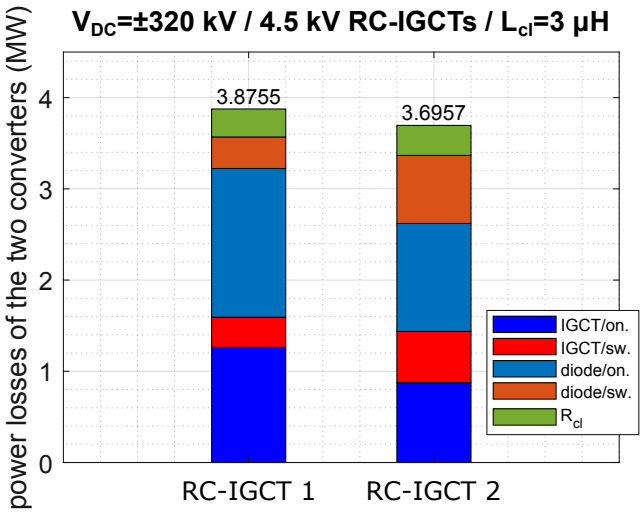


Figure 4.5: Averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, for different 4.5 kV RC-IGCTs, with V_{DC}=±320 kV

4.2.3 6.5 kV RC-IGCT

The distribution of on-state and switching losses is balanced for the 6.5 kV RC-IGCT as presented in Figure 4.6, but on-state losses remain slightly superior to switching losses. IGCT losses and diodes losses are also balanced, which shows that this RC-IGCT is well designed for MMC applications. The total power losses reaches 3.72 MW, which is slightly superior to the best 4.5 kV RC-IGCT.

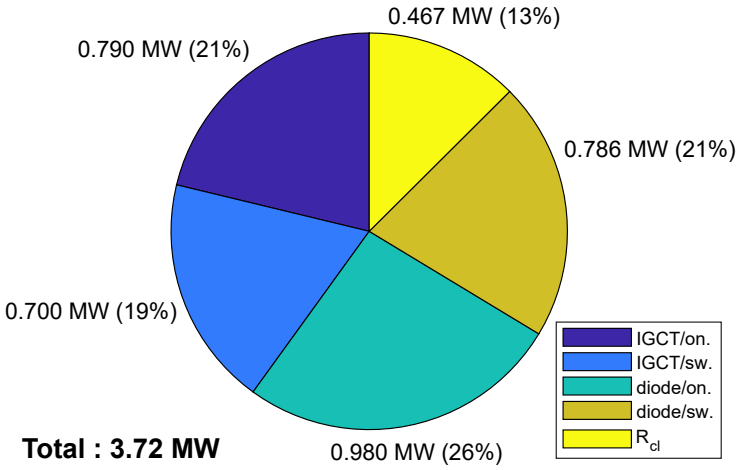


Figure 4.6: Pie chart (camembert) representing the distribution of the averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, for the 6.5 kV RC-IGCT, and with V_{DC}=±320 kV

4.2.4 Summary for constant voltage, V_{DC}=±320 kV

The power losses aforementioned have been gathered in Table 4.5 and separated in accordance with their origin (IGCT, diode or R_{cl}). Only the best couples of devices (IGCT/diode) and the best RC-IGCTs have been retained for each voltage rating. On the whole, all the solutions exhibit comparable performances: the maximum difference of power losses, which is between the 4.5 kV asymmetric devices and the 10 kV asymmetric devices, is equal to 310 kW, i.e. less than 9%. Regarding the asymmetric IGCTs, the 4.5 kV IGCTs and the 10 kV IGCTs present similar power losses, respectively 1.38 MW and 1.39 MW. Yet, clamp circuit power losses are increased by more than 50% due to the higher di/dt inductance L_{cl}. All these solutions lead to an efficiency superior to 99.5% for the rectifier and 99.6% for the inverter according to Table 4.6, this asymmetry is due to the high current stress of the diodes in the rectifier.

4.2.4.1 Thermal stress and voltage rating, limits of a study at constant DC link voltage

The junction temperatures for the critical operating conditions have been reported in Table 4.7. The diodes experience higher thermal stress in the offshore converter-station (rectifier), whereas the IGCTs experience higher thermal stress in the onshore converter-station (inverter). The junction temperatures remain low for 4.5 kV asymmetric devices; besides, these devices have a maximum junction temperature of 140°C. A reduction of the water flow could be considered to reduce the size of the cooling system. For instance, Q_{water}=2 L/min instead of Q_{water}=3 L/min would reduce the necessary hydraulic power by at least 33%. In addition, a further reduction is

expected due to the decrease in pressure drop in the hydraulic circuit.

Type	**V_{DC}**	**N**	**power losses (MW)**			
	kV		IGCT	R_{cl}	diode	total
A-IGCT 4.5 kV	±320	256	1.38	0.40	1.79	**3.58**
A-IGCT 10 kV	±320	137	1.39	0.65	1.84	3.89
RC-IGCT 4.5 kV	±320	256	1.43	0.33	1.92	3.69
RC-IGCT 6.5 kV	±320	178	1.49	0.46	1.76	3.72

Table 4.5: Power losses per origin (IGCT/diode/R_{cl}) of the two converter-stations, for the best solution related to each semiconductor voltage rating, and for each type of device (asymmetric/reverse-conducting), V_{DC} fixed

Type	**V_{DC}**	**N**	**η (%)**	
	kV		rectifier	inverter
A-IGCT 4.5 kV	±320	256	99.57	99.65
A-IGCT 10 kV	±320	137	99.53	99.63
RC-IGCT 4.5 kV	±320	256	99.57	99.63
RC-IGCT 6.5 kV	±320	178	99.58	99.62

Table 4.6: Efficiency of each converter-station of the HVDC link, for the best solution related to each semiconductor voltage rating, and for each type of device (asymmetric/reverse-conducting), V_{DC} fixed

Type	**V_{DC}**	**N**	**rectifier, P=-1 GW**		**inverter, P=1 GW**	
	kV		m_a=0.85, Q_{inv}=0 MVAR		m_a=0.8, Q_{inv}=±400 MVAR	
			IGCT	diode	IGCT	diode
A-IGCT 4.5 kV	±320	256	70.5°C	90.3°C	89.3°C	72.6°C
A-IGCT 10 kV	±320	137	95.2°C	**127°C**	**134°C**	94.5°C
RC-IGCT 4.5 kV	±320	256	78.5°C	114°C	101°C	94.9°C
RC-IGCT 6.5 kV	±320	178	91.7°C	134°C	126°C	109°C

Table 4.7: Junction temperatures of each device for the critical operating conditions of each converter-station, for the best solution related to each semiconductor voltage rating, and for each type of device (asymmetric/reverse-conducting), V_{DC} fixed

Regarding the 4.5 kV RC-IGCT, the diode part reaches 114°C in the rectifier at full power, for a maximum junction temperature of 125°C. The thermal stress is much more important than with the asymmetric devices, despite their similar power losses. The 6.5 kV RC-IGCT experiences a similar issue: its diode part and its GCT part respectively reach 134°C and 126°C, thus approaching the maximum junction temperature (140°C). These two RC-IGCTs are the most relevant solutions in terms of CAPEX, since all the capabilities of the installed silicon area are exploited.

It comes out that the junction temperatures of the 10 kV asymmetric devices exceed the maximum ratings, i.e. 115°C for the IGCTs and 125°C for the diodes. Beyond the important thermal stress experienced by the 10 kV devices, the switching frequency plays an important

role. When the modulation index m_a decreases and when reactive power is injected, the switching frequency is increased by the sorting algorithm to limit the capacitor-voltage ripple. This is why the switching frequency is equal to 124 Hz in the rectifier with m_a=0.85 and without reactive power, whereas it reaches 152 Hz in the inverter with m_a=0.8 and Q_{inv}=400 MVAR. The results regarding the 10 kV asymmetric devices demonstrate that the minimum modulation index and the range of reactive powers are crucial parameters, for the selection of the semiconductor devices. It also throws light on the drastic difference between the thermal stresses during the critical operating conditions.

The share of switching losses increases with the voltage rating; it approaches 50% of the total losses with the 6.5 kV devices and the 10 kV devices. This observation underlines the growing interest in investigating soft switching for these high-voltage devices. However, regarding this first comparative study, different factors have been ignored:

- THD varies with the number of SMs, which implies that the configuration based on N=256 SMs per arm has lower THD than the one with N=137 SMs per arm. This can be mitigated by the fact that as long as standards are respected, a further reduction of THD has no real interest.

- Mechanical, electrical and hydraulic assembly is more complex with N=256 SMs per arm. So, the reduction of N is attractive: converter material and assembly costs are intrinsically related to the number of SMs.

4.3 Power losses of the HVDC stations, N=256 sub-modules fixed

This second comparative study aims to address the limitations of the previous comparative study. The number of levels is kept constant, equal to 256, but with higher voltage devices while keeping system power constant, and allowing system voltage to increase as presented in Table 4.8. Then:

- DC voltage can reach ±600 kV between pole and ground, i.e. 1200 kV between poles, which would require cable technologies that are almost ready to be commercialised.
- For a given power, the increase in V_{DC} reduces load current, and consequently SM power-losses are reduced.
- The study does not directly compare semiconductors with different voltage ratings, but rather different technological solutions, where the number of components and the physical volume remain almost identical.

This study aims to forecast the future developments of HVDC systems, operating at higher DC link voltages. It can be seen that the current trend is to increase SM voltage: there is no incentive to increase the number of SMs per arm (which is already considerable), since THD is low enough to eliminate filter requirements [21]. In recent years, power semiconductors with voltage ratings exceeding 4.5 kV have become available such as the 6.5 kV BIGT [64]. Besides, 6.5 kV IGBT power modules with current ratings of around 1000 A are offered by manufacturers. The IGCT leads the way with the 6.5 kV RC-IGCT and the 10 kV IGCT as presented in 1.3.3, thus proposing a wide range of semiconductor voltage ratings. It should be noted that the results of the first study related to the 4.5 kV devices remain unchanged, since V_{DC} and N are identical.

$\mathbf{V_{DC}}$	±320 kV	±460 kV	±600 kV
$\mathbf{V_{DRM}}$ **(kV)**	4.5	6.5	10
min. N	256	256	256

Table 4.8: Different DC link voltages for a fixed number of SMs per arm, for the different semiconductor voltage ratings, regarding the developments of 2.2.2.2

4.3.1 6.5 kV RC-IGCT

Considering Figure 4.7, the distribution of the power losses of the 6.5 kV RC-IGCT remains similar to the one observed in Figure 4.6. However, the rise in the DC link voltage, at constant power, is beneficial for the converter-stations since the power losses are reduced to 3.50 MW.

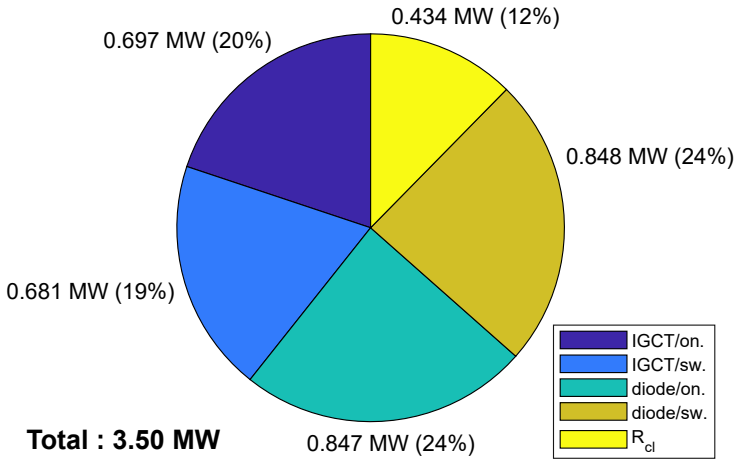


Figure 4.7: Pie chart (camembert) representing the distribution of the averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, and for the 6.5 kV RC-IGCT, with 256 sub-modules per arm

4.3.2 10 kV IGCTs

4.3.2.1 10 kV asymmetric devices

Figure 4.8 shows that the reduction of the arm-currents modifies the distribution between on-state losses and switching losses, compared to Figure 4.3(b). Switching losses exceeds on-state losses for IGCT 2 and diode 2, representing more than 60% of the total losses. IGCT 2/diode 1 is still the best couple; furthermore, the power losses are decreased to 3.36 MW. This result is due to the reduction of on-state losses, since these evolve non-linearly with the current. On the contrary, increasing the number of sub-modules increases the power losses of an MMC arm in an almost linear way.

4.3.2.2 10 kV RC-IGCT

The 10 kV RC-IGCT, which cannot be used with V_{DC}=±320 kV at the full power of ±1 GW, is compatible with a higher voltage application due to the smaller thermal stress. Figure 4.9 shows a similarity with the 10 kV asymmetric devices, switching losses have a significant weight in the distribution of the power losses that is close to 50%. In the end, 3.96 MW of power loss are obtained, leading to the lowest efficiency for the two converter-stations. Nonetheless, this solution is very attractive as it minimizes CAPEX due to a lighter design of the SMs.

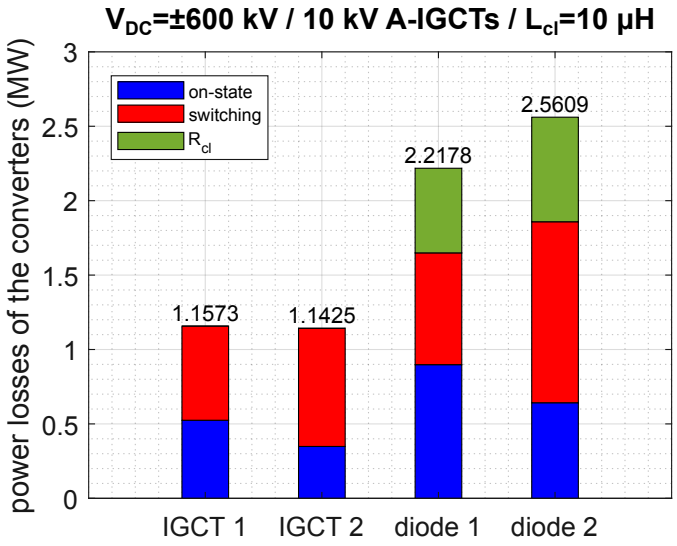


Figure 4.8: Averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, and for the 10 kV asymmetric devices listed in Table 4.3, with 256 sub-modules per arm

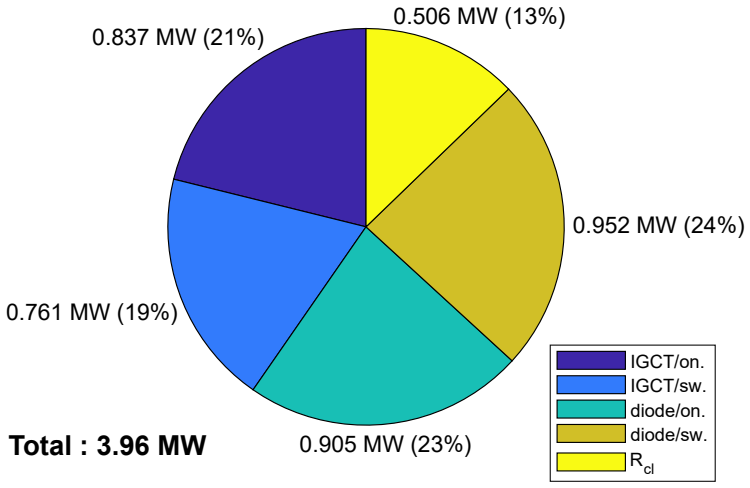


Figure 4.9: Pie chart (camembert) representing the distribution of the averaged power losses of the two converter-stations, for the given wind-speed distribution of Figure 4.1, for the 10 kV RC-IGCT, with 256 sub-modules per arm

4.3.3 Summary for constant number of SMs, N = 256

Table 4.9 shows that, on the contrary of the first comparative study, asymmetric 4.5 kV IGCTs do not turn out to be the best choice. Increased DC link voltages are promising as they decrease arm-currents, thus favouring 6.5 kV and 10 kV devices, at constant power. Consequently, asymmetric 10 kV devices exhibit the best performances, offering a power loss reduction by 6.1% compared to the asymmetric 4.5 kV devices. Among the reverse-conducting devices, the 6.5 kV RC-IGCT comes out as the best trade-off. As shown in Table 4.10, the 10 kV RC-IGCT leads to the worst efficiency despite the reduction of the arm-currents.

The origins of the power losses unveil that the clamp circuit power losses increase with the voltage rating. The main reason is that the di/dt limiting inductance must be increased with

the voltage rating, because the maximum allowable di/dt during diode reverse recovery is more or less constant. Clamp circuit power losses represent 11% of the total power losses for the 4.5 kV asymmetric devices, whereas they embody more than 16% of the total power losses for the 10 kV asymmetric devices. As in the case of the first comparative study, it comes out that soft switching circuits could benefit to the 6.5 kV devices and the 10 kV devices; but not only because of the switching losses. Clamp circuit power losses are strongly correlated with the SM voltage, which limits the performances of high-voltage IGCTs.

Type	$\mathbf{V_{DC}}$ kV	**N**	**power losses (MW)**			
			IGCT	R_{cl}	diode	total
A-IGCT 4.5 kV	±320	256	1.38	0.40	1.79	3.58
A-IGCT 10 kV	±600	256	1.14	0.56	1.65	**3.36**
RC-IGCT 4.5 kV	±320	256	1.43	0.33	1.92	3.69
RC-IGCT 6.5 kV	±460	256	1.37	0.43	1.69	**3.50**
RC-IGCT 10 kV	±600	256	1.60	0.50	1.85	3.96

Table 4.9: Power losses per origin (IGCT/diode/R_{cl}) for the two converter-stations, for the best solution related to each semiconductor voltage rating, and for each type of device (asymmetric/reverse-conducting), N fixed

Type	$\mathbf{V_{DC}}$ kV	**N**	η (%)	
			rectifier	inverter
A-IGCT 4.5 kV	±320	256	99.57	99.65
A-IGCT 10 kV	±600	256	99.59	99.68
RC-IGCT 4.5 kV	±320	256	99.57	99.63
RC-IGCT 6.5 kV	±460	178	99.60	99.64
RC-IGCT 10 kV	±600	256	99.56	99.58

Table 4.10: Efficiency of each converter of the HVDC link, for the best solution related to each semiconductor voltage rating, and for each type of device (asymmetric/reverse-conducting), N fixed

Type	$\mathbf{V_{DC}}$ kV	**N**	**rectifier, P=-1 GW** m_a=0.85, Q_{inv}=0 MVAR		**inverter, P=1 GW** m_a=0.8, Q_{inv}=±400 MVAR	
			IGCT	diode	IGCT	diode
A-IGCT 4.5 kV	±320	256	70.5°C	90.3°C	89.3°C	72.6°C
A-IGCT 10 kV	±600	256	74.5°C	89.2°C	91.6°C	79.3°C
RC-IGCT 4.5 kV	±320	256	78.5°C	114°C	101°C	94.9°C
RC-IGCT 6.5 kV	±460	256	79.6°C	107°C	100°C	95.3°C
RC-IGCT 10 kV	±600	256	81.9°C	115°C	107°C	102°C

Table 4.11: Junction temperatures of each device for the critical operating conditions of each converter, for the best solution related to each semiconductor voltage rating, and for each type of device (asymmetric/reverse-conducting), N fixed

The thermal stresses of 6.5 kV devices and 10 kV devices are lower than previously, according to Table 4.11. The highest junction temperature is reached by the diode part of the 10 kV RC-IGCT in the rectifier. The 10 kV asymmetric devices operate with a temperature rise inferior

to 35°C, which shows that a 10 kV A-IGCT-based SM is a suitable solution regarding electrical and thermal stresses. Even the 10 kV RC-IGCT could be considered, the junction temperature being always 10°C below its maximum junction temperature, 125°C.

4.4 Comparison with other semiconductors, V_{DC} fixed

4.4.1 Context and limits

The electro-thermal models along with the sizing methods of the HVDC converter-stations can be applied to estimate the power losses of the two HVDC stations using other semiconductor devices. According to the observations made in the first chapter in 1.3, the most suitable technological solutions have been gathered in Table 4.12. IGBT is mainly represented throughout the indirect pressure PPIs and the indirect pressure press-pack BIGT from Hitachi ABB, and the wire-bonded IGBT module from Mitsubishi. Two IEGT devices from Toshiba are also considered.

Part number	Designation	max. T_j
5SNA 2000K450300	StakPak 1 4.5 kV	125°C
5SNA 2000K451300	StakPak 2 4.5 kV	125°C
5SNA 3000K452300	StakPak 3 4.5 kV	125°C
CM1500HC 90XA	IGBT power module 4.5 kV	150°C
5SJA 2000L520300	BIGT 1 5.2 kV	125°C
5SJA 3000L520300	BIGT 2 5.2 kV	125°C
ST1500GXH24	IEGT 1 4.5 kV	125°C
ST2000GXH31	IEGT 2 4.5 kV	125°C

Table 4.12: List of the other semiconductors, non characterized, considered for the power-loss analysis

It has to be reminded that the accuracy of the electro-thermal models relies on the experimental measurements realized with all the IGCTs aforementioned, dedicated static and dynamic characteristics being used, as explained in 3.2.1. This is not the case for the semiconductor devices in Table 4.12, since they are modelled using data-sheet information only. Furthermore, experimental validation of the electro-thermal model, as presented in the fifth chapter for IGCTs, has not been carried out. Consequently, the comparison between IGCTs and the other semiconductor devices remains limited.

4.4.2 Results

The power-loss analysis presented in Table 4.13 highlights a contrast regarding the power losses in IGCT-based SMs. Press-pack diodes and diode parts of the RC-IGCTs systematically exhibit higher power losses than the diode dies integrated into IGBT power modules. On the other hand, discrete IGCTs and GCT parts of the RC-IGCTs dissipate less power than the other IGBT/IEGT devices. IGCTs lead to a reduction of the power losses superior to 0.22 MW compared to the IGBT/IEGT devices, considering the clamp circuit power losses. Without the clamp circuit power losses, the gain is superior to 0.57 MW, i.e. approximately 0.06% of the average power generated, which is significant.

Regarding the diodes, two considerations must be kept in mind. Diodes used with asymmetric IGCTs are realized on a wafer. Similarly, in the case of RC-IGCT they are integrated on the

IGCT wafer. This is not the case for IGBT power modules and IEGTs, where multiple diode dies are connected in parallel. Consequently, the physical structure of the diode is different, and the current density may differ between the wafer and the diode dies, which can lead to meaningful differences in terms of performances. Secondly, the IGCT turns on like a thyristor as explained in the first chapter, which leads to negligible turn-on losses because the voltage has almost entirely fallen before the current starts to rise. However, this behaviour tends to increase diode turn-off losses: the intrinsic characteristics of the controllable device affect the switching losses of the diode.

Type	**N**	**power losses (MW)**				η (%)	
		turn-off device	R_{cl}	diode	total	rectifier	inverter
A-IGCT 4.5 kV	256	**1.38**	**0.40**	**1.79**	*3.58*	99.57	99.65
RC-IGCT 4.5 kV	256	**1.43**	**0.33**	**1.92**	3.69	99.57	99.63
StakPak 1 4.5 kV	256	2.25 (no snubber)		1.28	*3.53*	99.63	99.60
StakPak 2 4.5 kV	256	2.21 (no snubber)		1.53	3.74	99.60	99.59
StakPak 3 4.5 kV	256	**2.00 (no snubber)**		1.42	*3.42*	99.63	99.63
IGBT power module 4.5 kV	256	**2.12 (no snubber)**		1.54	*3.66*	99.61	99.60
BIGT 1 5.2 kV	221	2.49 (no snubber)		1.67	4.17	99.56	99.54
BIGT 2 5.2 kV	221	2.27 (no snubber)		1.64	3.91	99.59	99.57
IEGT 1 4.5 kV	256	2.22 (no snubber)		1.63	3.85	99.58	99.59
IEGT 2 4.5 kV	256	2.09 (no snubber)		1.44	*3.53*	99.60	99.63

Table 4.13: Power losses per origin (turn-off device/diode/R_{cl}), and efficiency of each converter of the HVDC link for the different semiconductors, for the wind turbine power curve of Figure 4.2 and the wind-speed distribution of Figure 4.1, V_{DC}=±320 kV fixed

4.4.3 Conclusions

The comparison between IGCTs and other semiconductor devices throw light on their interest for HVDC applications. The IGCT alone allows a reduction of the power losses larger than 28% compared to the IGBT. Nevertheless, IGCTs affect the dynamic of the diodes in their commutation cells, thus increasing diode turn-off losses. The clamp circuit also has a contribution, though limited, that reduces the gap between IGCT and IGBT/IEGT devices. Consequently, soft switching circuits such as the ARCP circuit presented in 2.1.3.2, would be especially beneficial, as they would imply the suppression of the clamp circuit power losses and a drastic reduction of switching losses.

4.5 Conclusion of the power-loss analysis

Throughout an extensive modelling of the HVDC link, from the electro-thermal model of the SMs to the consideration of an intermittent power production of the offshore wind parks, several conclusions can be formulated regarding existing IGCTs and prospective IGCT-based solutions. IGCT is a relevant device for the considered application, as on-state and switching losses are low, leading to a moderate thermal stress. Besides, RC-IGCTs are very promising as they allow a clear reduction of converter's volume and converter's cost, at the price of a slight increase in the power losses. 10 kV IGCTs do not have sufficient current ratings for 1 GW HVDC stations yet, but they would allow an improvement of the converter's efficiency at higher DC link voltages. In the meantime, using 10 kV IGCTs can reduce the number of necessary SMs by 47%, compared to the traditional SMs based on 4.5 kV devices, thus simplifying converter's assembly and reducing part count. 4.5 kV IGCTs can be dedicated to higher power systems, involving

powers of around 1.5 GW according to the results of the power-loss analysis.

Soft switching circuits have come out as a meaningful option, especially for 6.5 kV IGCTs and 10 kV IGCTs, for different reasons:

- Switching loss reduction is harder as the semiconductor voltage rating increases, as the intrinsic modifications of the IGCT wafer necessarily increase on-state losses. Soft switching circuits could overcome this issue, which would leave the possibility to optimize high-voltage IGCTs for low on-state losses.
- Clamp circuit power losses steadily increase with the SM voltage, even in the second comparative study where the arm-currents decrease with the SM voltage itself. This source of power losses would be suppressed with an ARCP circuit.
- Diode turn-off losses are potentially higher within an IGCT-based commutation cell than within an IGBT-based commutation cell due to the behaviour of the devices during turn-on. An ARCP circuit could also reduce these switching losses, thus enhancing the performances of the overall IGCT-based SM.

The next chapter focuses on the experimental realization and the testing of IGCT-based SMs, equipped with a dedicated instrumentation, to estimate the semiconductor power losses and to analyse the behaviour of the semiconductors during commutations.

Chapter 5

Realization and testing of IGCT-based sub-modules

Throughout the second and the third chapter, IGCT-based converter-stations have been proposed, with dedicated models to accurately estimate the SM power losses. The fourth chapter has pointed out the relevance of IGCTs for grid-connection of offshore wind-farms. However, these studies raise some issues, such as the practical realization of IGCT-based sub-modules. The power-loss analysis, though based on the experimental static and dynamic characteristics of the semiconductors, relies on hypotheses inherent to the electro-thermal model that must be validated. The dynamic behaviour of IGCT is a pending issue, as it influences the switching losses as well as the clamp circuit power losses: the impact of the parasitic elements, that have not been considered in the simulation models, remains unknown at this stage.

The fifth and last chapter aims to address these concerns, focusing on a laboratory-scale experiment. Considering that a single converter-arm contains more than a hundred SMs, the whole converter-station cannot be reproduced. A much simpler solution has been selected, allowing for the test of semiconductor devices at their nominal electrical and thermal ratings, with a dedicated test bench.

5.1 Design of the test bench

5.1.1 Constraints, topology and electrical ratings

5.1.1.1 Overview of the electrical circuit and principle of operation

Introduction Because of the real current ratings and voltage ratings of an MMC SM, it is not possible to use a single commutation cell: it would be necessary to dissipate a huge power. Thus, an opposition method has been chosen to overcome this issue [200]. This approach is especially relevant to test medium-power and high-power electrical systems, as well as to carry out semiconductor characterization. The opposition method generally requires a duplicate of the system to test. Then, the two systems are connected in a way that the total power provided by the test bench's power supply is equal to the internal losses. In the scope of the PhD thesis, two half-bridge choppers are connected to the same DC bus, whereas their outputs are linked with an intermediate inductor which aims at ensuring a periodic energy exchange between the two commutation cells. Figure 5.1 shows an overview of the test bench considered for the experiments.

Challenges The main purpose of the test bench is to reproduce realistic operating conditions for the semiconductor devices. In the case of IGCTs, electrical and thermal stresses must be as

close as possible of the ones seen in the previous chapter. According to Figure 5.1, it implies that the DC bus voltage must be equal to the SM voltage V_{SM}. Based on 2.2.2.1, it can be concluded that the test bench must be sized to withstand at least a DC bus voltage of 4700 V, to be able to test the IGCTs with the highest voltage ratings.

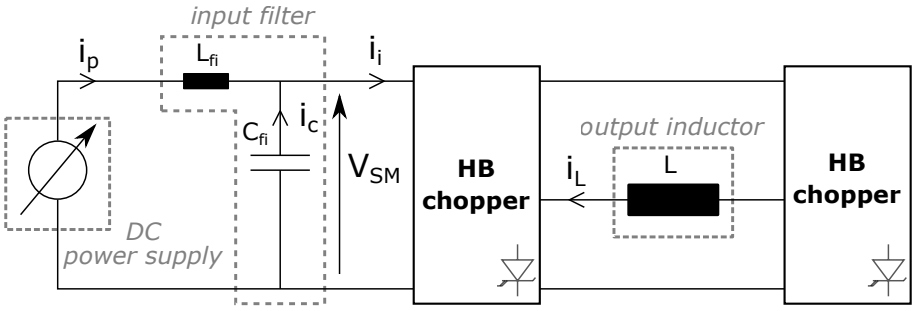


Figure 5.1: Principle of a test bench using opposition method; V_{SM} is the sub-module voltage and by extension the DC bus voltage of the test bench

In the meantime, it can be noticed that the current flowing through the inductor i_L, also called output current, is the direct image of the arm-current i_A from the point of view of the semiconductor devices. Based on the previous simulations, a maximum RMS current of 1200 A and a peak current of more than 2000 A are expected. Therefore, all the electrical connections must withstand important thermal stresses.

As it has been seen in the fourth chapter, the relevant IGCTs have a voltage rating going from 4.5 kV to 10 kV, so the test bench must comply with a wide range of voltages. Furthermore, the current ratings are necessarily more important with the 4.5 kV devices than with the 10 kV devices. Logically, the test bench must be designed for the maximum voltage and the maximum current, which is unfavourable because these two maximum ratings are not supposed to be simultaneously met. Consequently, two configurations are foreseen:

1. A “low voltage” configuration for 4.5 kV IGCTs, where the current rating of the test bench is maximized.

2. A “high voltage” configuration for 6.5 kV IGCTs and 10 kV IGCTs, where the voltage rating of the test bench is maximized.

More details about these two configurations are given in this section, as well as the resulting consequences on the test bench’s design.

The output current i_L must have the same electrical characteristics as an arm-current would have in a converter-station. Even though it is theoretically possible to reach the same RMS and peak values, the output voltage is a three-level waveform which necessarily leads to an important harmonic distortion. The only solution to significantly reduce the harmonic distortion is to increase the switching frequency. However, this is not desirable, because, as it has been seen in the fourth chapter, the most relevant IGCTs are optimized for a given pair current/switching frequency. Therefore, the switching frequency is imposed by the operating conditions of the converter. Consequently, low-order harmonics within the output current must be tolerated, in order to keep the switching frequency low enough.

Operation of the two commutation cells Since IGCTs are tested with free-wheeling diodes, at least one clamp circuit with a di/dt choke is necessary. If a single clamp circuit is used, a

minimum duration between two commutations must be respected, as explained in 1.3.3.3, even if the commutations do not occur in the same commutation cell. Using two clamp circuits allows the operation of the two commutation cells to be completely decoupled. In other words, the power losses inherent in the operation of each commutation cell are separated, rather than being combined in a single clamp circuit. Consequently, two clamp circuits with two di/dt chokes have been considered for the test bench.

Input current and considerations regarding the design of the test bench The power transferred to the commutation cells and the output inductor can be expressed:

$$P_t(t) = V_{SM} i_i(t) \tag{5.1}$$

where $i_i(t)$ is the input current of the commutation cells as shown in Figure 5.1. It is assumed that V_{SM} is constant, the residual voltage ripple behind the second-order filter (shown in Figure 5.1) is not considered here. Neglecting the power losses of all the elements, for this calculation only, the power transferred to the commutation cells is equal to the instantaneous power received by the output inductor:

$$P_t(t) \approx \frac{1}{2} L \frac{d\left(i_L(t)\right)^2}{dt} \tag{5.2}$$

The ideal output current i_L contains only two components, then:

$$i_L(t) = \frac{I_{DC}}{3} + \frac{\sqrt{2}}{2} I_s \sin(\omega_0 t) \tag{5.3}$$

where I_{DC} is the DC link current, and I_s the RMS value of the AC-side currents. This equivalence, between the output current i_L and the arm-currents of a converter-station, is discussed later. It leads to the following expression of the input current $i_i(t)$:

$$i_i(t) \approx \frac{L\omega_0}{V_{SM}} \left(\frac{\sqrt{2} I_{DC} I_s}{6} \cos(\omega_0 t) + \frac{I_s^2}{4} \sin(2\omega_0 t) \right) \tag{5.4}$$

(5.4) shows that the input current contains significant harmonics at f_0 and $2f_0$: this is problematic, because DC power supplies are generally not able to provide such harmonics. This is why an input filter is mandatory, to ensure a proper operation of the commutation cells and the DC power supplies. It should be reminded that $i_i(t)$ normally contains a continuous component that is due to the power losses, which has been ignored in order to simplify the calculations.

5.1.1.2 DC power supply, input filter and output inductor

Output inductor The selection of the output inductor primarily affects the output current. However, this is not the main criterion retained to select the output inductor: because of the low switching frequency operation, the harmonic distortion is necessarily high. A more relevant concern is the harmonic content of the input current $i_i(t)$. According to (5.4), the two low-frequency harmonics are proportional to the inductance L. Since these two components have to be attenuated, the amplitudes of the harmonics affects the volume and the cost of the input filter. It can be concluded that a reduction of the output inductance directly leads to a more compact input filter, which is a more effective strategy than increasing it to obtain a slight improvement of the harmonic content of the output current. At EDF R&D Les Renardières, the available inductors with the most suitable electrical ratings are air-core inductors of 2.0 mH/660 A, with a series resistance of 7.4 mΩ at 50 Hz and ambient temperature. To withstand 1200 Arms, at least two inductors in parallel are necessary, and a third inductor in parallel has been added to decrease the volume of the input filter as aforementioned. It leads to an equivalent inductance of 670 μH.

DC power supply According to the principle of the opposition method, the DC power supply must be designed to provide the total amount of power losses: it includes the semiconductor power losses, the clamp circuit power losses, but also the copper losses of the inductors. A simpler model than the one presented in the third chapter has been used, based on the simulation software PLECS, to estimate the maximum power losses of the whole test bench.

Semiconductors	Max. voltage	Max. power consumption	Max. current
4.5 kV devices	2800 V	26 kW	10.4 A
6.5 kV devices	4000 V	33.5 kW	9.3 A
10 kV devices	5300 V	<40 kW	<8.6 A

Table 5.1: Maximum ratings of the DC power supply to test 4.5 kV, 6.5 kV and 10 kV devices

According to Table 5.1, a 5300 V/10.4 A DC supply would be necessary assuming a rectangular v-i characteristic. Nevertheless, DC power supplies with such ratings are uncommon due to the limited number of applications. Therefore, it has been decided to use two DC power supplies, with the capability to operate together either in series or in parallel depending on the semiconductors to test. Two 3 kV/10 A DC power supplies (TSD-3000-9.6 from Magna-Power) are suitable and provide a comfortable safety margin regarding the electrical ratings.

Input filter The first purpose of the input filter is to attenuate the low-frequency currents absorbed by the circuit. A general formulation of the problem for the first-order and the second-order harmonics is represented in Figure 5.2, where the DC power supply behaves like a simple conductor. The transfer functions of the circuit are:

$$\begin{cases} \frac{\underline{i_p}}{\underline{i_i}} = \frac{1}{1-L_{fi}C_{fi}\omega^2} \\ \\ \frac{\underline{v_{cf}}}{\underline{i_i}} = -\frac{L_{fi}\omega j}{1-L_{fi}C_{fi}\omega^2} \end{cases} \tag{5.5}$$

Based on (5.5), two criteria are formulated to obtain the minimum values of L_{fi} and C_{fi}:

1. A maximum peak-to-peak current ripple Δi_p, determined by the limitations of the DC power supply.
2. A maximum peak-to-peak capacitor-voltage ripple Δv_{Cf}.

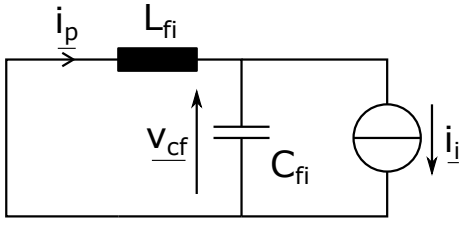


Figure 5.2: Equivalent circuit to design the input L-C filter

Four 480 mH/5.5 A iron-core inductors and four 1.4 mF/3500 V film capacitors have been selected to meet the requirements. As it can be seen, a single capacitor cannot withstand the DC bus voltage to test 6.5 kV devices or 10 kV devices at the nominal voltage, so it is necessary to associate two of them in series. On the other hand, the four capacitors must be connected in parallel when 4.5 kV devices are tested, to comply with the aforementioned criteria.

5.1.1.3 Low voltage and high voltage configurations

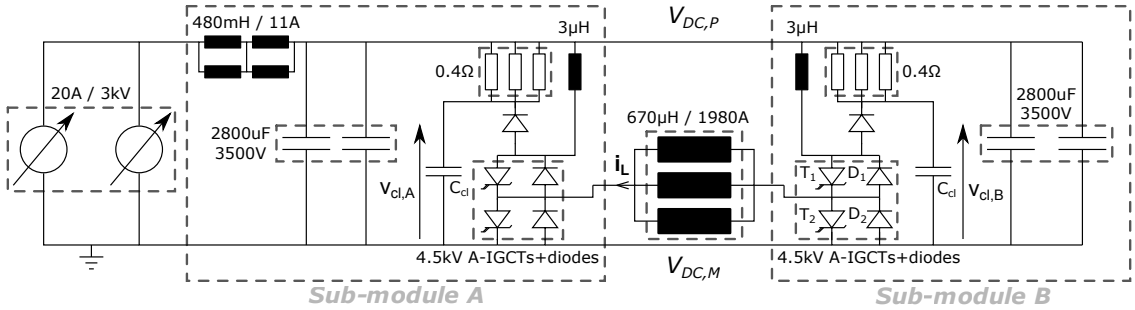


Figure 5.3: "Low voltage" configuration of the test bench, dedicated to the testing of 4.5 kV devices

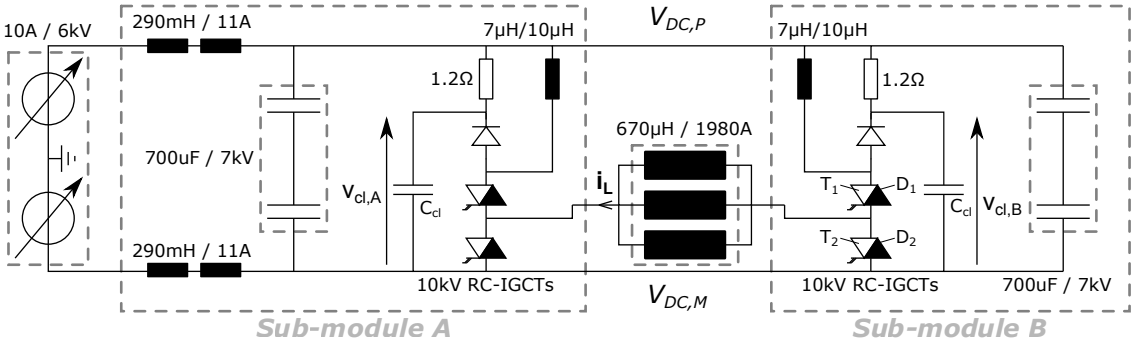
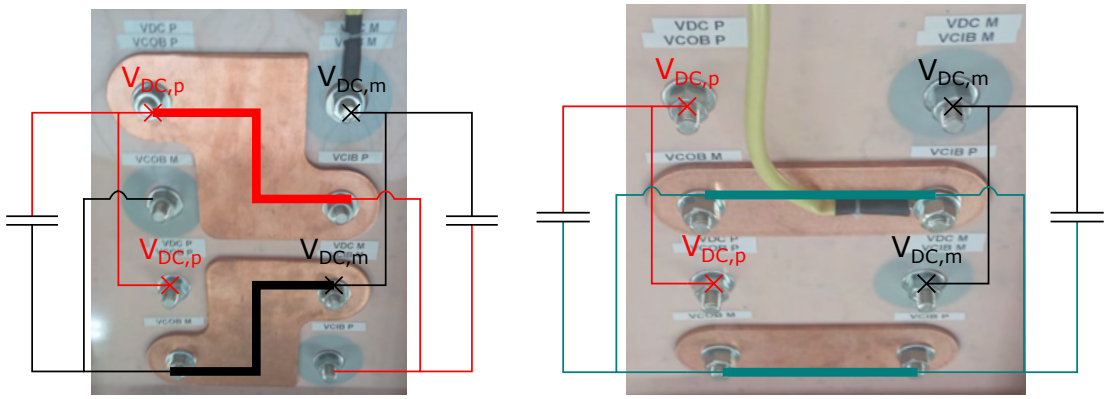


Figure 5.4: "High voltage" configuration of the test bench, dedicated to the testing of 6.5 kV and 10 kV devices

Based on Figure 5.1 and the previous observations, Figure 5.3 shows the configuration retained to test 4.5 kV IGCTs, whereas Figure 5.4 shows the alternative configuration for 6.5 kV devices and 10 kV devices. Since the capacitors are not connected in the same way in the two configurations, a reconfigurable coupling system composed of copper parts has been designed as shown in Figure 5.5.

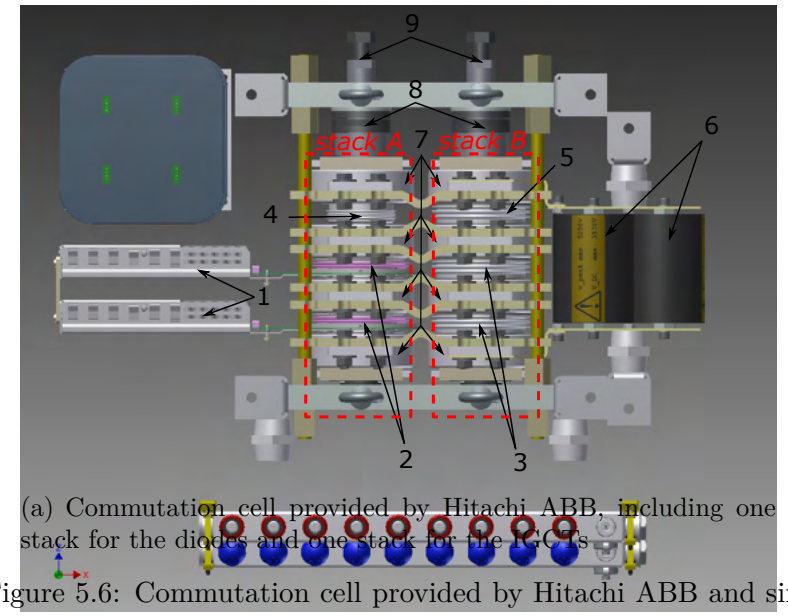


(a) "Low voltage" configuration (b) "High voltage" configuration

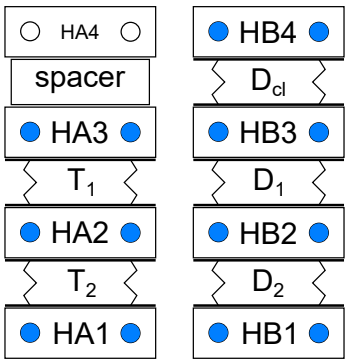
Figure 5.5: Coupling of the capacitors in each sub-module for the two possible configurations of the test bench

The capacitor bank is divided into two parts to be equally shared by each half-bridge chopper: two independent sub-modules are formed thanks to this transformation. The inductors of the input filter are embedded in the sub-module A for integration purposes. The choice of using two DC supplies allows to create a neutral point connected to the ground when the two DC power supplies are connected in series. It divides the pole-to-ground voltage by two in the whole test bench, thus reducing insulation requirements for the "high voltage" configuration.

5.1.1.4 IGCT-based half-bridge choppers



(a) Commutation cell provided by Hitachi ABB, including one stack for the diodes and one stack for the IGCTs



(b) Simplified schematic of the stacks A and B

Figure 5.6: Commutation cell provided by Hitachi ABB and simplified schematic of the stacks A and B

Mechanical clamping of the semiconductor devices IGCTs as well as all press-pack devices require a proper mechanical clamping. A given force must be applied with an uniform pressure distribution to ensure both electrical and thermal contacts. Hitachi ABB provides recommendations to safely mount its devices [201]. The semiconductor devices have been provided within their stacks by Hitachi ABB. Figure 5.6(a) shows two stacks gathered in the same mechanical structure, forming the commutation cell. Stack A is composed of two IGCTs (2) with their gate units (1), with four additional cold plates (7) to ensure a double-side water cooling. (4) is a spacer that aims to keep the two stacks aligned: one of the cold plate is useless. In Stack B, there are the two diodes D_1 and D_2 (3), the clamp diode D_{cl} (5) and four cold plates (7). Belleville springs (8) allow to easily adjust the mounting force of the stack with the screws (9). Figure 5.6(b) proposes a simplified schematic of the two stacks.

Clamp circuit and di/dt snubber The clamp capacitor bank (6) is composed of five 4 uF/3 kV film capacitors from AVX, leading to an adjustment range from 4 uF to 20 uF with multiple intermediate values. About the clamp resistors, three values are desired: 0.4 Ω, 0.6 Ω and 1.2 Ω, with a maximum power dissipation of 1400 W, to allow operation at higher switching frequency, up to 300 Hz. Three water-cooled clamp resistors of 1.2 Ω (969 W-L from EBG) have been selected for each sub-module: it is possible to obtain 0.4 Ω and 0.6 Ω with parallel associations. Furthermore, this choice allows to reconfigure the clamp circuit without modifying the hydraulic circuit.

The di/dt chokes have been custom-made to get at least two inductance values for each semiconductor voltage rating: 3 μH/850 A, 7 μH/850 A and 10 μH/770 A air-core inductors from Transrail Boige & Vignal have been used. Iron-core inductors have been avoided, because of the harmonic content of the output current i_L. The corresponding low-frequency harmonics could have led to additional iron losses and eventually saturation issues. On the other hand, air-core solutions provide a constant inductance, independently of the harmonic content of the output current, at the price of a higher volume.

5.1.1.5 Overview of the water cooling system

Multiple constraints have been considered to design the water cooling system. For environmental reasons, a closed-loop circuit has been preferred to traditional solutions where the water is simply "lost". Due to the mechanical clamping of the semiconductors, shown in 5.1.1.4, the cold plates are not electrically isolated from the semiconductor devices. It implies that the water flowing into the cold plates has a non-null potential. It also comes out that because of its ions, water has a relatively low impedance, leading to a current flow through the piping. This phenomenon is deemed concerning above 1 kV, but many parameters such as the section and the length of the piping elements affect it. Since a maximum voltage of 5300 V is considered, the water must be deionized to avoid consequent electrical disturbances. Furthermore, two independent departures are foreseen to ensure an equal distribution of the water flows in the two sub-modules. Figure 5.7 shows the resulting water cooling system, which is composed of two hydraulic circuits:

1. A primary circuit using a water-glycol mix, which evacuates the heat from the water/water exchanger to the water/air exchanger.
2. A secondary circuit using deionized water, in contact with the cold plates of the test bench. The heat is extracted from the semiconductor devices and the clamp resistors to the water/water exchanger.

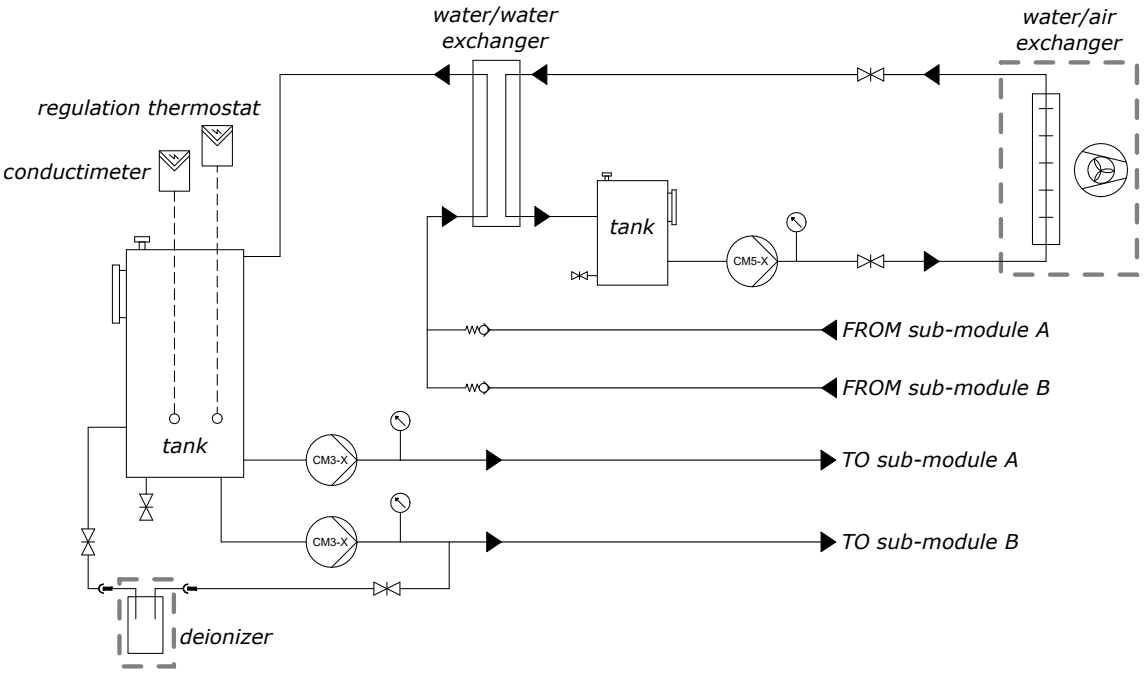


Figure 5.7: Hydraulic schematic of the water cooling system, connected to the two sub-modules of the test bench

The water cooling system has been designed and assembled by Eurodifroid. It features a maximum thermal power of 18 kW, a maximum ambient temperature of 40°C and a maximum water

temperature in the secondary circuit of 60°C to comply with the operating conditions of the test bench.

5.1.2 Measurements

The test bench is designed to embed two kind of measurements: thermal measurements to apply a calorimetric method, and electrical measurements to calculate the switching losses of the semiconductors. This concept can be also applied to the clamp circuit, as it is detailed later in the chapter.

5.1.2.1 Electrical measurements

Switching losses are calculated by measuring simultaneously the voltage and the current of the same semiconductor with a differential voltage probe and a Rogowski coil. The specifications of the corresponding probes are given in Appendix C. Both voltage and current probes exhibit a bandwidth larger than 10 MHz and a rise time lower than 15 ns, which is deemed sufficient to accurately acquire IGCT waveforms. The maximum di/dt is expected during diode turn-off, and cannot exceed 940 A/μs due to the operating conditions of the commutation cells. Since the Rogowski coil can acquire a peak di/dt of 40 kA/μs, the acquisition of the current transients must be accurate. Two oscilloscopes with a bandwidth of 200 MHz are used, point-to-point waveforms can be retrieved with an USB interface. Waveforms are averaged with the oscilloscope, using the last 16 sweeps.

The estimation of a given turn-off energy E_{sw} is obtained by integration:

$$E_{off} = \int_{t_1}^{t_2} v(t)i(t)dt \tag{5.6}$$

Where t_1 and t_2 define the integration interval. To obtain a consistent estimation, two criteria must be met: $v(t_1) = 0$ with $v(t)$ constant before the beginning of the commutation, and $i(t_2) = 0$ with $i(t)$ constant from the end of the commutation. In practice, it requires an integration interval as small as possible, and the introduction of offsets V_0 and I_0 to easily extract the switching energy. Besides, voltage and current are not continuous, which leads to the following formula, based on the Tustin (trapezoidal) approximation:

$$E_{off} \approx \sum_{k=2}^{N_{12}} \frac{1}{2} \left[(v_k - V_0)(i_k - I_0) + (v_{k-1} - V_0)(i_{k-1} - I_0) \right] (t_k - t_{k-1}) \tag{5.7}$$

where N_{12} is the number of points comprised in the interval $[t_1, t_2]$, and t_k the time at index k. The offsets V_0 and I_0 are calculated with the following formula:

$$V_0 = \frac{1}{N_{cal}} \sum_{k=1}^{N_{cal}} v_k \text{ and } I_0 = \frac{1}{N_{cal}} \sum_{k=N_{12}-N_{cal}+1}^{N_{12}} i_k \tag{5.8}$$

where N_{cal} defines a calibration interval to accurately calculate the offsets V_0 and I_0. These formulas are implemented in a script to automatically retrieve the switching energies, but the integration interval remains manually defined for each commutation to maximize the accuracy. This routine is extended to turn-on waveforms. Furthermore, it is also applicable to the electrical waveforms of the clamp resistor during commutations.

5.1.2.2 Thermal measurements and design of the hydraulic circuit

The calorimetric method lies in the following relation, linking the power losses P_{cp} of a cold plate, fully evacuated by the water at a constant water flow Q_{water}, with the difference of temperature

between the water outlet and the water inlet ΔT_{cp}, called "temperature rise of the cold plate" thereafter:

$$P_{cp} = \rho c_P Q_{water} \Delta T_{cp} \tag{5.9}$$

where the water has a density ρ and a specific heat capacity c_P. By definition, flow-meters and two temperature probes per cold plate are necessary. The expected pressure drop per cold plate, including the piping, is about 2 bar: since there are seven cold plates per sub-module, the cold plates are associated in parallel to limit the maximum pressure in the water circuit. Figure 5.8 shows the resulting design of the hydraulic circuits for the two sub-modules, which is asymmetric: only sub-module B is fitted with all the necessary sensors to calculate the power losses. On the other hand, sub-module A is only equipped with one flow-meter and two temperature probes, to monitor its operation. Two remarks can be done regarding the location of the sensors:

- One temperature probe is common to all the cold plates, a single water inlet temperature is retrieved.
- A single flow-meter is used for all the cold plates, it is assumed that the water flow is equally shared between the seven paths.

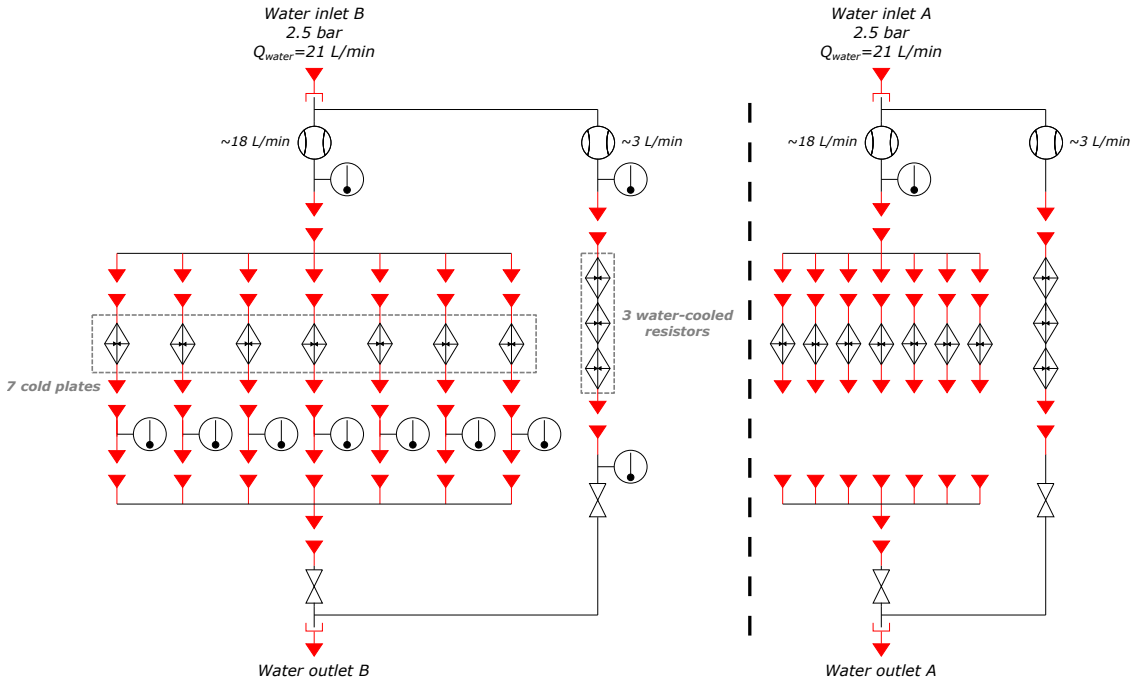


Figure 5.8: Hydraulic circuit of the two sub-modules

The characteristics of the sensors are given in Appendix C. It has come out that the interchangeability tolerance of the temperatures probes introduces an additional error. It can be removed by measuring the initial temperature difference before turning on the DC power supplies, $\Delta T_{cp}(0\ V, 0\ A)$, for each cold plate. Then, this quantity is subtracted to $\Delta T_{cp}(V, i)$, measured during the operation of the test bench. Consequently, the following quantity is systematically considered to estimate the power losses:

$$\Delta T_{cp,final}(V, i) = \Delta T_{cp}(V, i) - \Delta T_{cp}(0\ V, 0\ A) \tag{5.10}$$

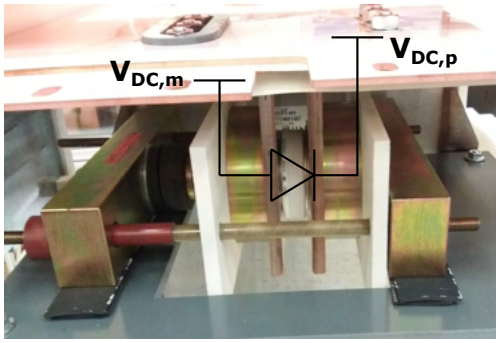
Temperatures and water flows are averaged over 12 samples (2 min), to attenuate eventual disturbances.

5.1.3 Control and protections

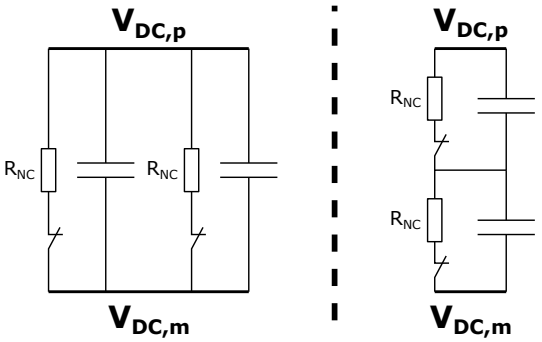
A Boombox from Imperix has been retained to monitor the test bench. This rapid control prototyping platform natively embed PWM outputs, analog inputs, and a Matlab/Simulink interface to easily implement the control of a converter, with the necessary protections. A LEM sensor is used to acquire the output current (its characteristics are given in Appendix C).

5.1.3.1 Protection of the test bench

Due to the important voltage reachable on the DC bus, security rules and exploitation instructions apply to the test bench to ensure the safety of the people. Dedicated protection systems have been designed to meet these requirements.



(a) Free-wheeling diode that avoids polarity reversal on the DC bus of the test bench



(b) DC bus discharge system with the "low voltage" configuration (left) and the "high voltage" configuration (right)

Figure 5.9: Free-wheeling diode and discharge system for the DC bus, ensuring passive and active protection of the test bench

Protection of the DC bus against short-circuit In case of semiconductor failure, the DC bus may see a short-circuit. This fault case is critical because it would induce a consequent discharge of energy, stored in the capacitor bank. Even with the di/dt chokes which would limit the fault current, a peak current superior to 100 kA is expected with a resonant voltage on the DC bus, inducing thermal and mechanical stresses able to damage all the components of the test bench. For this worst-case scenario, a free-wheeling diode has been mounted on the DC bus. The purpose of this diode is to conduct when the DC bus voltage becomes inferior to zero, which is supposed to avoid a voltage reversal, thus protecting the DC power supplies. The corresponding diode is shown in Figure 5.9(a).

DC bus discharge system Even if a fault scenario is detected, the opening of the IGCTs and the disconnection of the DC power supplies remain insufficient. A significant energy remains stored in the capacitor bank, able to damage material or to hurt people. Consequently, this energy must be discharged as soon as a fault scenario occurs. It is done thanks to a discharge system composed of normally closed contactors in series with resistors, as presented in Figure 5.9(b). R_{NC}=10 kΩ is selected to ensure a full discharge of the DC bus in less than a minute. The contactors are mandatory because the corresponding discharge resistors would dissipate too much power in steady-state: in case of fault scenario, they are inserted.

Interlock between the DC power supplies and the Boombox Many software protections are implemented on the Boombox, which leads to the opening of the IGCTs if an unexpected

behaviour is observed: this is the safest strategy to protect the IGCTs against turn-off failure. Yet, this is not sufficient because the DC power supplies remain in operation by default. To address this issue, an interlock signal is sent by the Boombox to the dedicated inputs of the DC power supplies. If an user-defined fault case is detected, the DC power supplies are disconnected from the test bench thanks to the dry contacts of the DC outputs.

5.1.3.2 Architecture of the output-current controller

As explained in 5.1.1.1, the output current i_L necessarily has an important harmonic distortion. The simplest solution to control the output current, implemented in a first approach, is a proportional-integral (PI) controller. Nevertheless, because of the small bandwidth of the control loop, the relation between the amplitude of the output current and the reference current varies with the operating conditions.

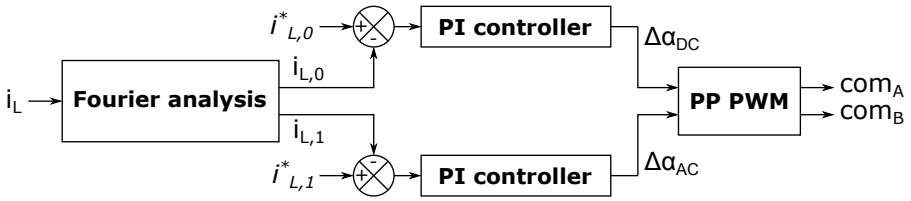


Figure 5.10: Overview of the output-current controller

A more comprehensive approach consists in controlling the harmonics of the output current: the continuous and the grid-frequency components are the most important quantities to monitor. Figure 5.10 presents this principle, 180 samples at a sampling frequency of 9 kHz are processed by discrete filters to calculate the average output current, $i_{L,0}$, and the fundamental of the output current, $i_{L,1}$. These two quantities lead to the calculation of the duty-cycles $\Delta\alpha_{DC}$ and $\Delta\alpha_{AC}$ that are processed to reproduce a programmed pattern (PP) of the output current, based on PWM.

Figure 5.11 presents the programmed pattern of i_L for f_{sw}=150 Hz, where $\Delta\alpha = \alpha_B - \alpha_A$ is the difference of duty-cycles between the two commutation cells. The sign of $\Delta\alpha$ changes twice per grid-period, i.e. two times every three periods of the carrier. This concept, though straightforward, requires a perfect synchronization between the generation of the programmed pattern and the FPGA. So, the timer of the carrier's clock has been retrieved from the FPGA in order to change the duty-cycles at the right times. The resulting output-current controller is still based on a carrier, since it simplifies the generation of the dead-times. Besides, it allows the generation of the programmed pattern with the digital signal processor, easily programmable with the Matlab/Simulink interface.

5.1.4 Overview of the test bench

A side view of one of the two sub-modules is presented in Figure 5.12; the control room is shown in Figure 5.13. The computer-aided design of the two sub-modules has been realized by Jean-Marc Blaquière, design engineer at LAPLACE Laboratory. He has also contributed to the design of the hydraulic circuit, the assembly of the two sub-modules and the first tests to ensure the proper operation of the whole system.

5.2 Power-loss analysis with the 4.5 kV A-IGCTs

The IGCT 5SHY 55L4500 and the diode 5SDF 28L4520 have been retained. The conditions of operation of these devices during the measurements are presented in Table 5.2.

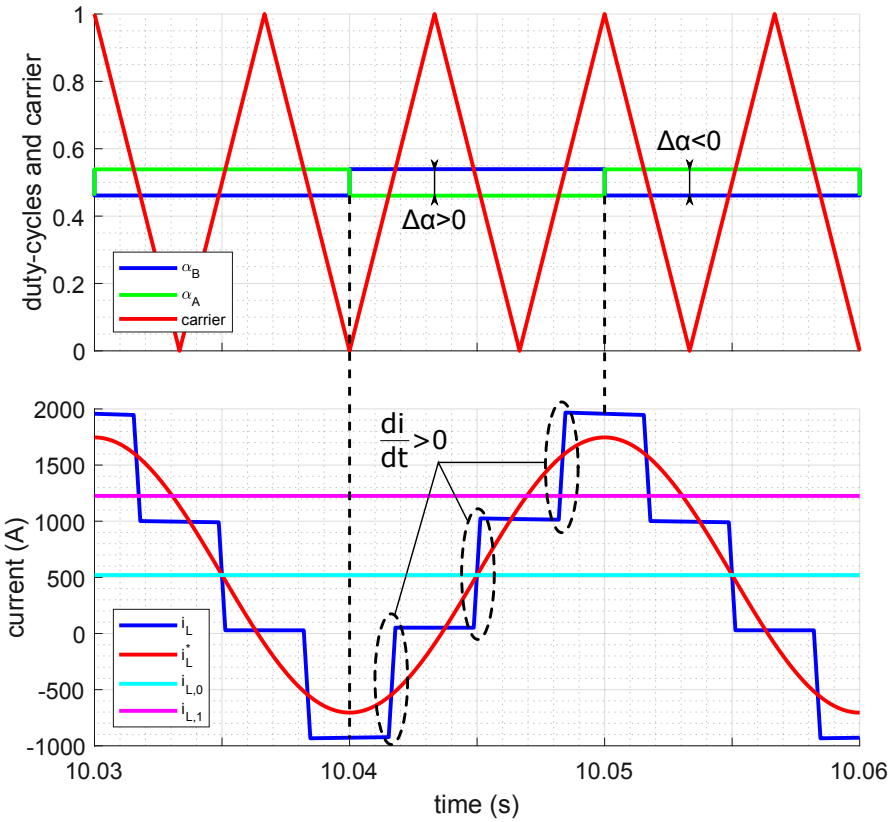


Figure 5.11: Programmed pattern of the output current for a switching frequency of 150 Hz: duty-cycles, carrier, output current i_L, continuous and grid-frequency components of the output current $i_{L,0}$ and $i_{L,1}$

Designation	Notation	Value/Range	Comments
SM voltage	V_{SM}	$[2200\ V, 2800\ V]$	voltage ripple $< 4\%$
DC current	i_L	$[-1200\ A_{DC}, 1200\ A_{DC}]$	minimum current: 200 A_{DC}
MMC-like current	i_L	$[210\ A_{rms}, 1160\ A_{rms}]$	$[\pm 430\ A_{pk}, \pm 2270\ A_{pk}]$
Switching frequency	f_{sw}	$[150\ Hz, 300\ Hz]$	-
di/dt choke	L_{cl}	$3\ \mu$H	-
clamp resistor	R_{cl}	$0.4\ \Omega$	3 resistors in parallel
clamp capacitor	C_{cl}	$20\ \mu$F	5 capacitors in parallel

Table 5.2: Conditions of operation of the asymmetric 4.5 kV semiconductor devices during the tests

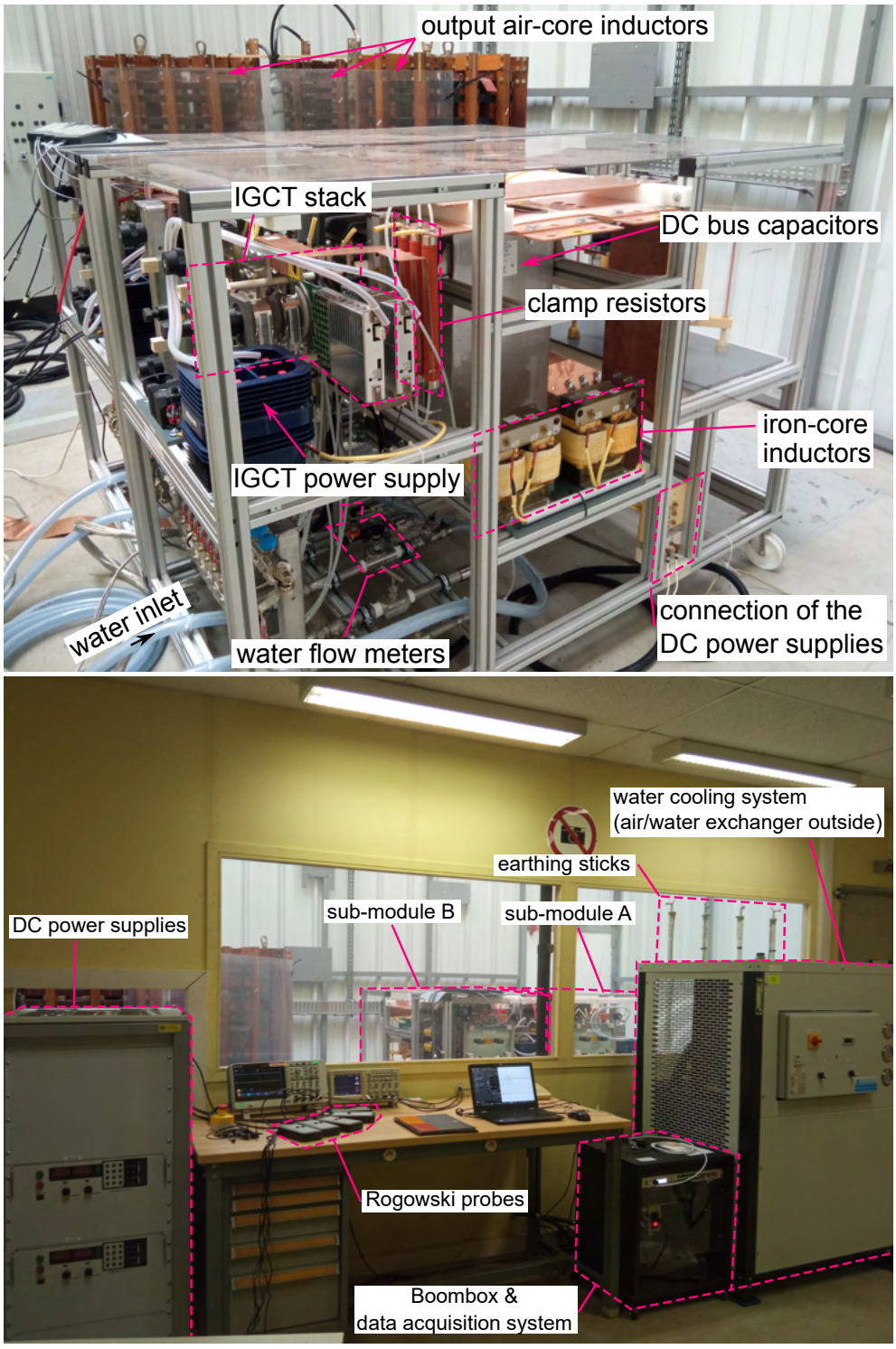


Figure 5.13: Control room

5.2.1 DC output current

The first tests have been performed with a DC output current. It allows to validate the proper operation of the semiconductor devices and to easily calculate the switching losses with the electrical measurements.

5.2.1.1 Switching waveforms

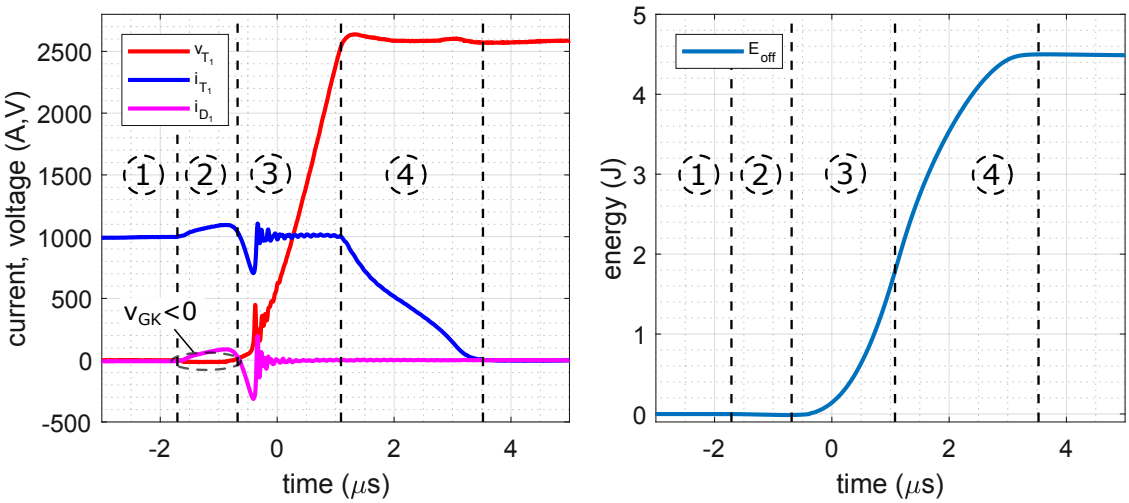


Figure 5.14: IGCT turn-off waveforms under 2500 V/1000 A: IGCT current i_T (blue), IGCT voltage v_T (red) and anti-parallel diode current i_D (magenta); and turn-off energy E_{off}

IGCT turn-off The left plot of Figure 5.14 shows the waveforms during IGCT turn-off, which can be divided into four phases. Initially, when i_T=1000 A, the anode-cathode voltage v_{AK}=v_T is very low since it is equal to the on-state voltage. The second phase starts when the turn-off process is initiated: the commutation order falls down to zero, then the gate unit applies a negative gate-cathode voltage v_{GK}=-20 V to deviate the anode current from the cathode to the gate. Since the PNP transistor is saturated, v_{AK} becomes negative, which explains the small voltage dip that is observed in the second phase. During this phase, the lower PN junction of the IGCT is blocking. However, due to the negative gate-cathode voltage, the anti-parallel diode is forward-biased. Consequently, i_D rises during the second phase, at a rate determined by v_{GK} and the stray inductance L_D, as defined in Figure 5.15. Assuming L_D=50 nH and v_{GK}=-20 V, the maximum di/dt that can occur is 400 A/μs. The effective di/dt is smaller because of the forward voltage of the diode at turn-on.

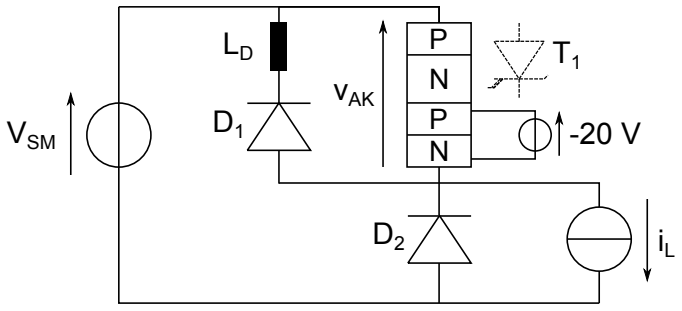


Figure 5.15: Schematic of the commutation cell during the first three phases of IGCT turn-off

An important remark is that the current that flows into the diode also flows into the IGCT, it only circulates between T_1 and D_1. When the cathode current has entirely been deviated to the gate, the anode-cathode voltage must rise: only the PNP transistor with an open base remains. In the third phase, D_1 goes through a reverse-recovery, the corresponding current flows into T_1. The anode-cathode voltage continuously rises at rate larger than 1200 V/μs, until reaching the nominal voltage V_{SM}. The fourth phase is marked by the decrease in the anode current i_T, while the anode-cathode voltage is maximum. The shape of the current waveform is specific to IGCT. i_T falls from 1000 A to 0 A within 3 μs. This commutation is a hard turn-off, which

draws a rectangular trajectory in the i-v plane of the IGCT. The selection of the dead-time is based on the longest IGCT turn-off duration: after observing IGCT turn-off with various DC output currents, a dead-time of 10 μs has been retained.

The right plot of Figure 5.14 shows the resulting turn-off energy, where the four phases previously defined have been reported. It can be observed that the second phase does not generate energy losses: the unexpected circulation of current between the switches T_1 and D_1 does not lead to additional losses, since it occurs when the anode-cathode voltage v_{AK} is null. Only the second part of the third phase and the fourth phase are responsible for the energy losses.

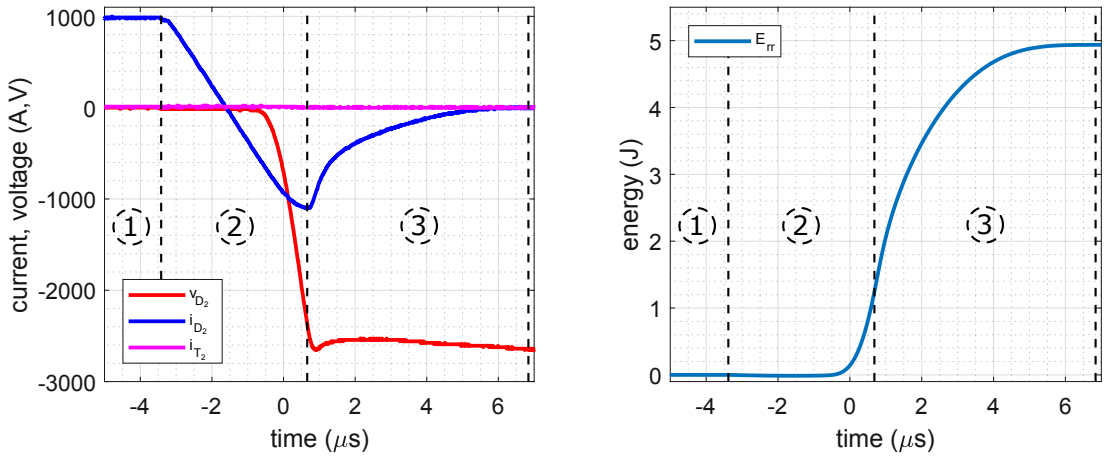


Figure 5.16: Diode turn-off waveforms under 2500 V/1000 A: diode current i_D (blue), IGCT voltage v_T (red) and anti-parallel IGCT current i_T (magenta); and diode turn-off energy E_{rr}

Diode turn-off The left plot of Figure 5.16 shows D_2's turn-off under 2500 V, divided into three phases. Initially equal to the arm-current, the diode current i_D falls with a regular slope, determined by the value of the di/dt choke and the sub-module voltage V_{SM}. In the end of the second phase, the anode-cathode voltage starts to rise, to reach sub-module voltage, approximately when i_D=-I_{rr}. Afterwards, the diode current exponentially increases and reaches zero, ending the diode turn-off.

5.2.1.2 Switching energies, comparison with the available characteristics

Diode turn-off energy The diode turn-off energies are presented in Figure 5.17 along with the measurements from the double-pulse tests (used for the electro-thermal models). It can be noticed that the two series of measurements provide similar results. Nevertheless, the diode turn-off energies are overestimated with the measurements from the double-pulse tests. This is mainly due to the value of the di/dt choke: the total inductance is increased by the stray inductance of connection between the di/dt choke itself and the stacks, $L_{\sigma,con}$, as presented in Figure 5.18.

The analysis of the diode's reverse-recovery unveils a total inductance of 4.2 μH, whereas the di/dt limiting inductance is equal to 3.41 μH. Considering a parasitic inductance of the commutation cell of 129 nH, obtained with FEM simulations, the stray inductance of connection $L_{\sigma,con}$ is equal to 660 nH. It leads to a reduction of the di/dt of more than 20%. Then, the diode turn-off energies for a di/dt choke of 4.5 μH are also considered in the right plot of Figure 5.17 (in magenta). It comes out that the diode turn-off energies, measured on the test bench, exceed

the theoretical results, obtained with a di/dt choke of 4.5 μH, for currents larger than 800 A. It is explained by the junction temperature of the diode, that progressively increases with the current in the operating conditions of the test bench, whereas it is constant with the double-pulse method. Consequently, a model considering the evolution of the power losses with the junction temperature is mandatory to accurately foresee the evolution of the power losses in steady-state.

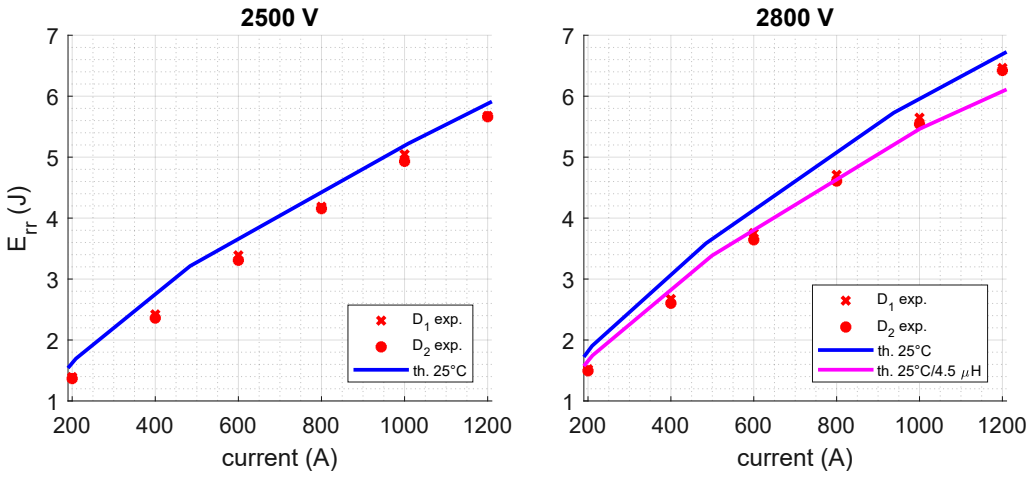


Figure 5.17: Evolution of the diode turn-off energy with the current under V_{SM}=2500 V and V_{SM}=2800 V, experimental results and "theoretical" results, based on the measurements with the double-pulse method at 25°C; and diode turn-off energies for a di/dt choke of 4.5 μH under V_{SM}=2800 V (magenta)

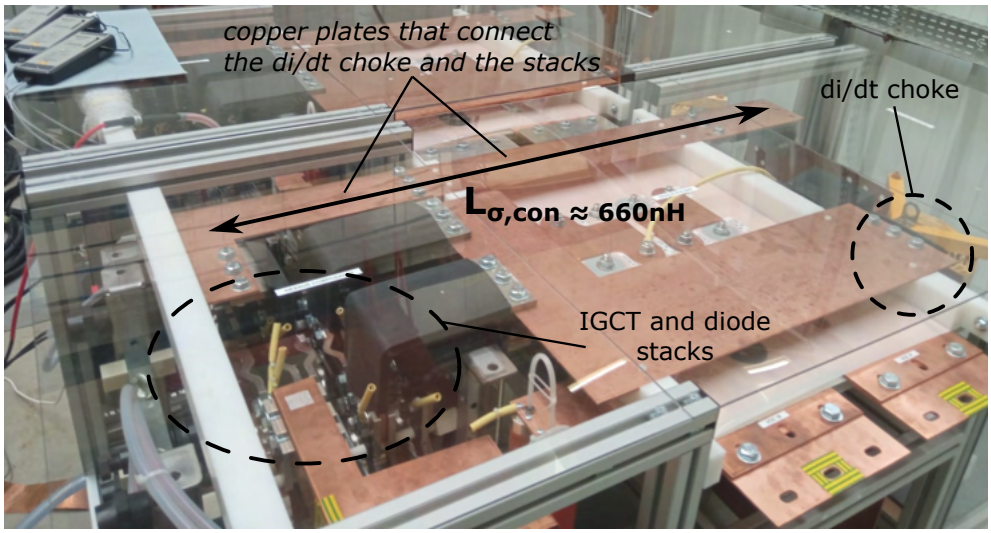


Figure 5.18: Top view of the test bench, and location of the parts responsible for the additional inductance in the commutation cell

IGCT turn-off energy The IGCT turn-off energies measured with the test bench are also consistent with the measurements obtained with the double-pulse method, as presented in Figure 5.19. The power losses are slightly lower than the expectations, which can be explained by the stray inductance of the commutation cell, $L_{\sigma,cell}$. Independently from the di/dt choke, it is the stray inductance between the IGCT and the clamp capacitor C_{cl}. The measurements

with the double-pulse method have been carried out with a stray inductance of 325 nH, whereas the test bench has a stray inductance estimated to 129 nH. It is known to decrease the IGCT turn-off losses, because of the reduction of the parasitic overvoltages.

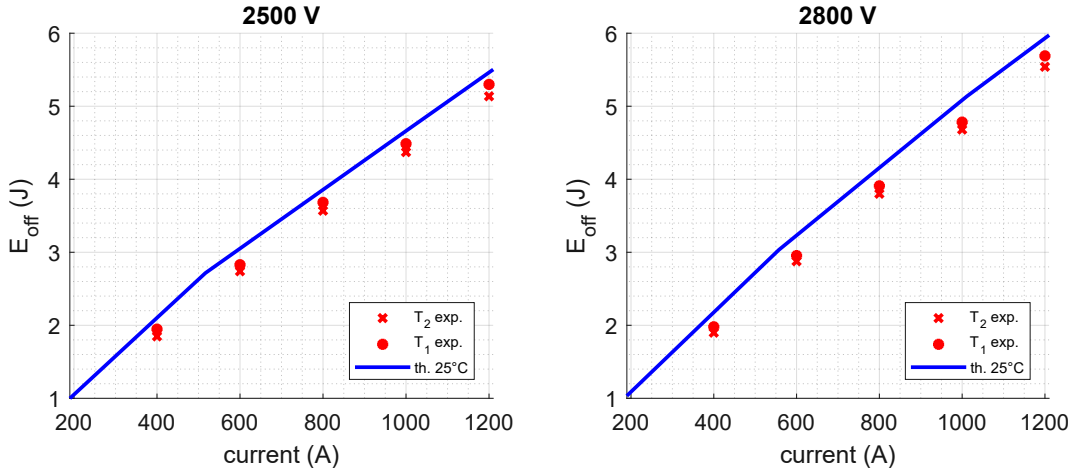


Figure 5.19: Evolution of the turn-off energy with the current under V_{SM}=2500 V and V_{SM}=2800 V, experimental results and "theoretical" results, based on the measurements with the double-pulse method at 25°C

Conclusion regarding the switching energies Figure 5.20 presents the two parasitic inductances among the commutation cells. The stray inductance of connection $L_{\sigma,con}$ is added to the existing di/dt choke L_{cl} in the test bench, which affects diode turn-off losses. On the other hand, the parasitic inductance $L_{\sigma,cell}$ mainly influences IGCT turn-off losses. $L_{\sigma,cell}$ value is much smaller than L_{cl}, so it has a negligible influence on diode switching losses. The switching losses of the semiconductors are quite sensitive to these parasitic elements; for industrial applications $L_{\sigma,con}$ would be negligible due to the higher compactness of the sub-module. The evolution of the switching energies throws light on the electro-thermal coupling, inherent to the semiconductor devices, and confirms the interest in using the multi-physical model introduced in the third chapter.

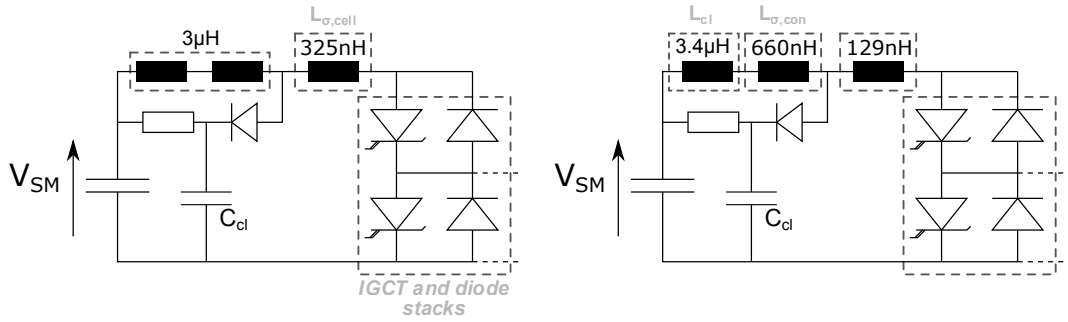
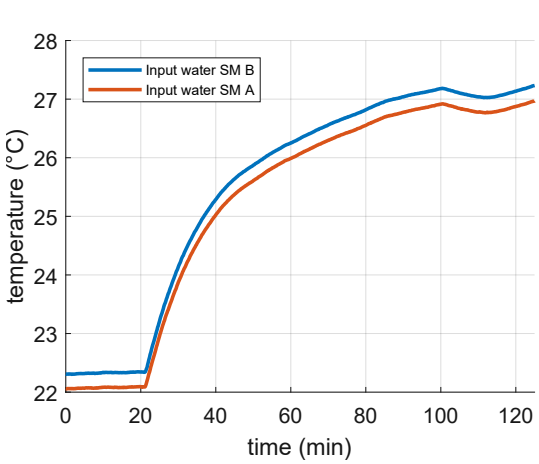


Figure 5.20: Parasitic elements in the commutation cell for the two systems: double-pulse test system (left) and actual test bench (right)

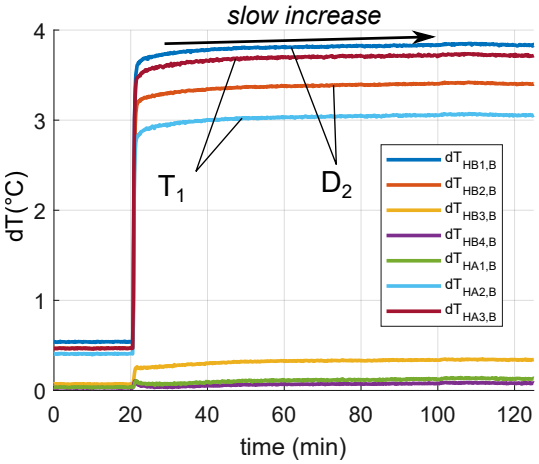
5.2.1.3 Thermal time-constants of the different components

Thermal measurements often have a non-negligible time-constant. Ideally, they must be read when the thermal equilibrium is reached. The thermal response of the water cooling system

has been observed during a sudden rise in the power dissipation. Initially, the operating conditions are V_{SM}=2200 V, i_L=100 A, with a switching frequency of 200 Hz. This initial state is maintained long enough to observe stable temperatures. Then, approximately at t=20 min, the reference current is increased from i_L=100 A to i_L=800 A, the temperatures of the input water for the two sub-modules are presented in Figure 5.21(a). The inlet water temperatures are directly related to the power losses: for a relative variation of 700 A at 2200 V/200 Hz, the temperatures are approximately increased by 5°C. From t=100 min, the temperatures decrease and finally stabilize, because the water cooling system is designed to limit the difference of temperature between the primary circuit and the secondary circuit. A time-constant of 25 min is obtained for the water cooling system, which requires about 80 min to reach the equilibrium point.



(a) Step response of the water cooling system



(b) Temperature rise (ΔT_{cp}) of the cold plates of SM B

Figure 5.21: Step response of the water cooling system and temperature rise (ΔT_{cp}) of the cold plates

Even though the water cooling system has an important time-constant, the temperature rise of the different cold plates stabilizes much faster, as shown in Figure 5.21(b). The temperature rise of a given cold plate, as a difference of two temperatures, has a time-constant about a few minutes. This quantity matters, because as explained in 5.1.2.2 it is proportional to the power losses extracted from the cold plate. After the quick step of temperature, it can be observed that ΔT_{cp} slowly increase over time. Actually, the rise in the water temperature slightly influences on-state and switching losses. Finally, a minimum time interval of 20 min is observed between two successive measurements.

5.2.1.4 Decoupling of the thermal measurements

The thermal measurements do not directly provide the semiconductor power losses, but the power losses extracted from the cold plates. Figure 5.6(b) from 5.1.1.4 points out the problematic: each device shares at least one cold plate with another device. It means that the relation between the power evacuated by the cold plates and the semiconductor losses is not straightforward. The following equation can be formulated, based on the notations introduced in Figure 5.6(b):

$$P_{T_1} + P_{T_2} = P_{HA1} + P_{HA2} + P_{HA3} \tag{5.11}$$

With a DC output current the coupling issues disappear, because either P_{T1} or P_{T2} is null. However, both IGCTs dissipate energy during normal operation, which requires a decoupling

method to obtain the power losses per device. Figure 5.22 shows the model of the stack retained for the study, which implies:

$$A.\begin{pmatrix} P_{HA1} \\ P_{HA2} \\ P_{HA3} \end{pmatrix} = \begin{pmatrix} P_2 \\ P_1 \\ P_1 + P_2 \end{pmatrix}, \text{ with } A = \begin{pmatrix} 1 + \frac{R_{22}}{R_{2i}} & -\frac{R_{hi}}{R_{2i}} & 0 \\ 0 & -\frac{R_{hi}}{R_{1i}} & 1 + \frac{R_{11}}{R_{1i}} \\ 1 & 1 & 1 \end{pmatrix} \tag{5.12}$$

The matrix A is inverted, to proceed to an identification of the thermal resistances. Then, two specific operating conditions are relevant to retrieve the five parameters of the model:

1. $P_{T1}>0$ and $P_{T2}=0$, giving two independent equations;
2. $P_{T1}=0$ and $P_{T2}>0$, giving also two independent equations.

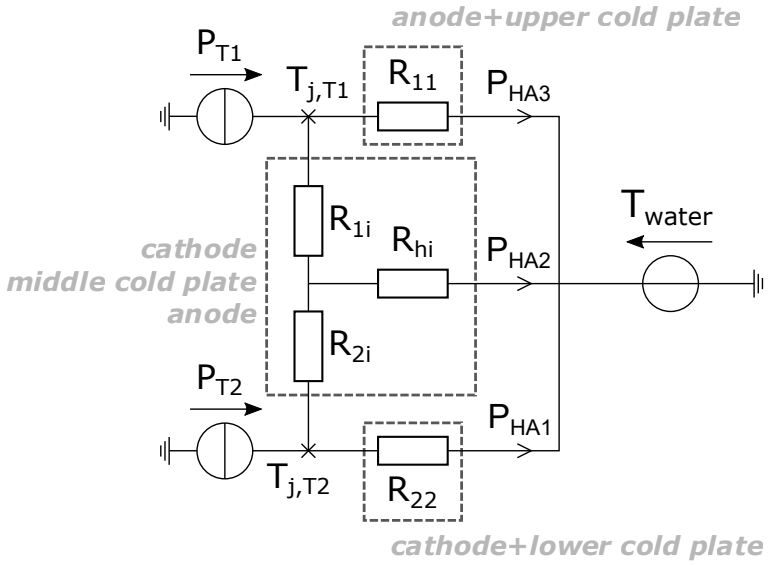


Figure 5.22: Equivalent thermal model of the IGCT stack (stack A)

The last thermal resistance must be fixed. Ten measurements are considered to identify the parameters of the model, under 2800 V/150 Hz, with DC output currents from ±400 A to ±1200 A, and a step of 200 A. It finally leads to the expression of P_{T1} and P_{T2}:

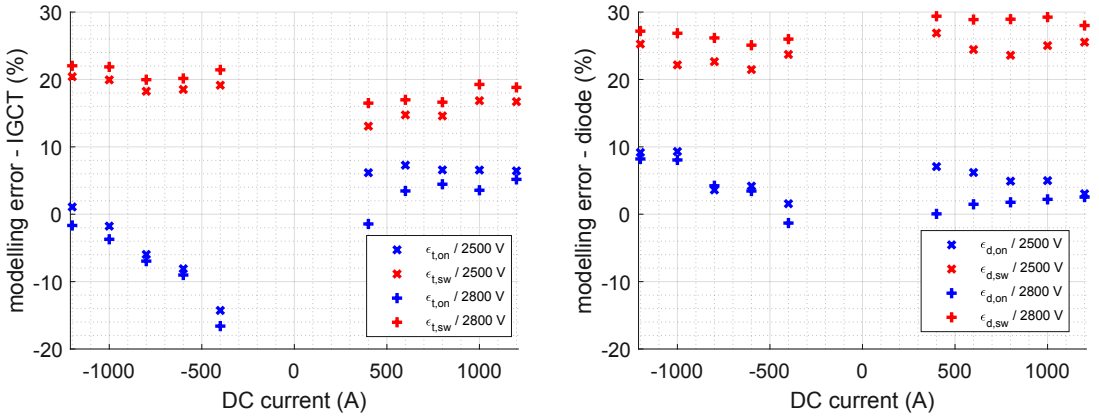
$$\begin{cases} P_{T_1} = 1.96P_{HA3} - 0.11P_{HA2} \\ P_{T_2} = 2.30P_{HA1} - 0.094P_{HA2} \end{cases} \tag{5.13}$$

This decoupling method, for an IGCT, could not be identically applied to the diode stack. Because of the clamp diode D_{cl}, the model of the diode stack is more complex than that of the IGCT stack, so the identification process should be reconsidered.

5.2.1.5 Comparison of the semiconductor power losses with the simulation results

Separation of on-state and switching losses Since the total power losses are obtained with the thermal measurements, and the switching losses are calculated from the switching waveforms, the on-state losses can be estimated by difference of these two terms. Then, on-state losses and switching losses can be individually compared to the simulation results. Figure 5.23 shows the estimation error ϵ, in percent, per device and per type of losses, for V_{SM}=2500 V and V_{SM}=2800 V.

As observed in 5.2.1.2, the switching energies are overestimated for both IGCT and diode, due to the different stray inductances and the higher di/dt limiting inductance. This difference is more pronounced for the diodes, as the switching waveforms are very sensitive to the value of the di/dt choke L_{cl}. The estimation error remains stable, from 25% to 30% for the diodes and from 10% to 25% for the IGCTs, for a wide range of DC currents and for the two SM voltages. Therefore, the sensitivity of the modelling error to the main electrical quantities is low.



(a) IGCTs (b) Diodes

Figure 5.23: Estimation error (%) of IGCT on-state losses $\epsilon_{t,on}$, IGCT turn-off losses $\epsilon_{t,sw}$, diode on-state losses $\epsilon_{d,on}$ and diode turn-off losses $\epsilon_{d,sw}$, with V_{SM}=2500 V and V_{SM}=2800 V; DC current from ±200 A to ±1200 A and f_{sw}=150 Hz

The assessment of on-state losses is less biased, the modelling error evolves from -20% to 10% for IGCTs and from -5% to 10% for diodes. The uncertainty is necessarily increased, because on-state losses require both thermal and electrical measurements: the measurement errors add up. According to Appendix C, the measurement error is 3.3% for the calorimetric method and 1.2% for the electrical measurements. Consequently, an error of 4.5% is introduced by the measuring instruments.

Total power losses per device Total power losses are also overestimated due to the overestimation of the switching losses, as presented in Figure 5.24 and Figure 5.25. The modelling error is lower than 20% for diodes and lower than 13% for IGCTs. In absolute terms, it corresponds to a maximum deviation of 210 W for IGCTs and 340 W for diodes, at the maximum DC current and an SM voltage of 2800 V. These results prove the reliability of the electro-thermal model to estimate the semiconductor power losses, as long as the inductances of the commutation cells are known. Otherwise, a safety margin is mandatory to avoid an underestimation of the power losses, which would be more concerning.

5.2.1.6 Assessment of the clamp circuit power losses

The electro-thermal model also includes the clamp circuit, whose power losses are inherent to the use of free-wheeling diodes with IGCTs. In the literature, the clamp circuit power losses are traditionally approximated by the following formula:

$$\begin{cases} P_{R_{cl},on} \approx \frac{1}{2} L_{cl} I_{rr}^2 f_{sw} \\ P_{R_{cl},off} \approx \frac{1}{2} L_{cl} i_A^2 f_{sw} \end{cases} \tag{5.14}$$

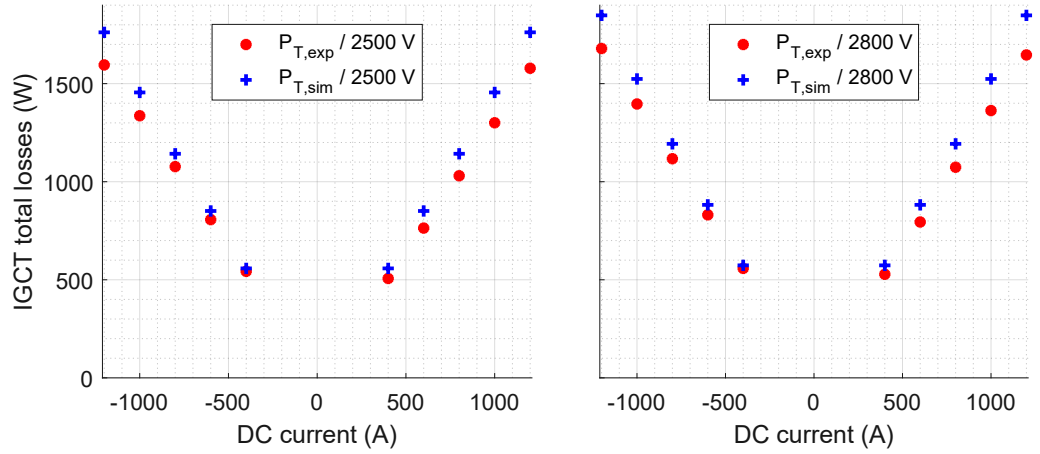


Figure 5.24: IGCT total power losses, with V_{SM}=2500 V and V_{SM}=2800 V; DC current from ±200 A to ±1200 A and f_{sw}=150 Hz

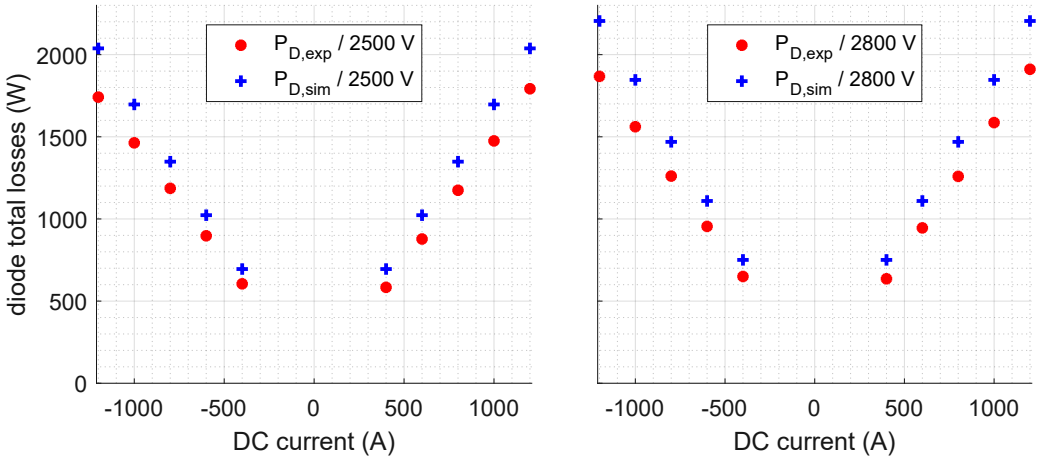


Figure 5.25: Diode total power losses, with V_{SM}=2500 V and V_{SM}=2800 V; DC current from ±200 A to ±1200 A and f_{sw}=150 Hz

These formula are compared to the experimental measurements and the simulation results, as shown in Figure 5.26. It can be noticed that the model of the clamp circuit provides a consistent evolution of the power losses with the DC current, for the two SM voltages. The estimation error of the electro-thermal model, regarding the clamp circuit, evolves between -5% and 15%. On the other hand, the energy-based approach leads to a significant overestimation of the power losses, with a corresponding error of 48% under 400 A/2500 V. At maximum current, the error remains superior to 20%, which shows that the analytic expressions are only relevant to get an upper bound of the power losses, as their accuracy is very limited.

During the study, it has been noted that the assessment of the clamp circuit power losses is very sensitive to the reverse-recovery current I_{rr} of D_1 and D_2. Then, the reverse-recovery current has to be accurately known, especially at low currents where its influence is significant. This point is further discussed later in the chapter.

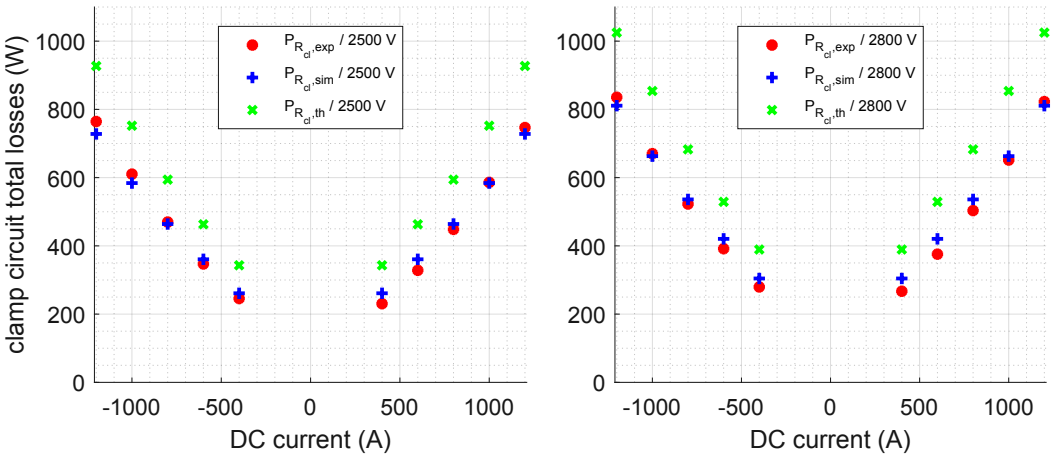


Figure 5.26: Clamp circuit power losses obtained from thermal measurements, simulation results and analytic expressions, with V_{SM}=2500 V and V_{SM}=2800 V; DC current from ±200 A to ±1200 A and f_{sw}=150 Hz

5.2.1.7 Estimated junction temperatures, conclusions regarding the electro-thermal model

The junction temperature is estimated with the electro-thermal, assuming a constant water temperature, in Figure 5.27. In practice, the water temperature varies as observed in 5.2.1.3. It points out that the semiconductor devices have been tested for a wide range of thermal stresses, with a variation of junction temperature larger than 40°C. Thus, it validates the accuracy of the electro-thermal model for the very same operating conditions.

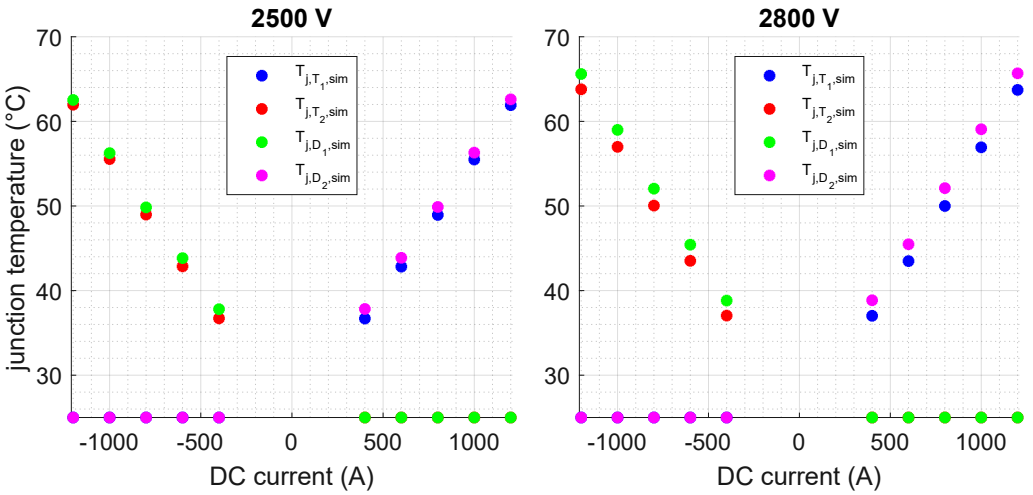


Figure 5.27: Junction temperatures calculated with the electro-thermal model for a constant water temperature T_{water}, with V_{SM}=2500 V and V_{SM}=2800 V; DC current from ±200 A to ±1200 A and f_{sw}=150 Hz

5.2.2 Calibration of the thermal measurements - semiconductor power losses

The calorimetric method lies in the hypothesis that the power losses are evacuated by the water flowing through the cold plates. In practice, this is false because of the heat exchange with the

surrounding air of the different parts. A critical issue is the tubes in which the outlet water flows: the heat exchange with the surrounding air leads to a drop in the water temperature between the cold plate and the temperature probes. This phenomenon is presented in Figure 5.28. To limit this phenomenon as much as possible, the tube length between the outputs of the cold plates and the temperature probes has been minimized. Besides, the use of 6 mm tubes limits convection. To conclude regarding the efficiency of these precautions, a calibration of the thermal measurements is necessary.

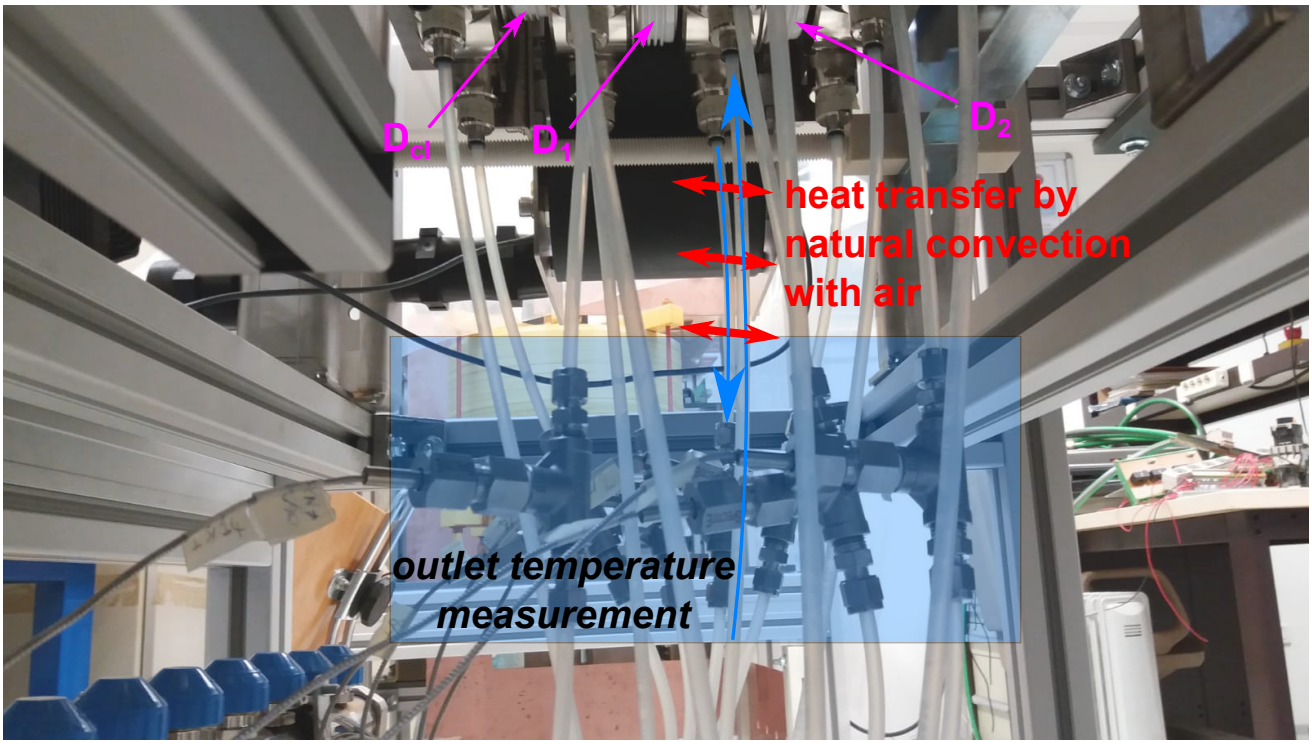


Figure 5.28: Cold plates, tubes and temperatures probes of SM B; heat loss between the outputs of the cold plates and the temperature probes may be problematic

Currently, only switching losses can be obtained through electrical measurements: on-state losses are deduced from the thermal measurements. In steady-state, the only way to measure on-state losses with a satisfactory accuracy is to use a voltmeter with a range of a few volts. Consequently, the existing high-voltage low-current DC power supplies of the test bench are replaced with a high-current, low-voltage DC power supply, as presented in Figure 5.29. The purpose is to validate the accuracy of the thermal measurements, thanks to a comparison with reliable electrical measurements.

Figure 5.30(a) shows that the two methods provide similar results, over the full range of DC currents. To quantify the difference between the electrical measurements and the calorimetric method, the coefficient β is introduced:

$$\beta = \frac{P_{elec}}{P_{th}} \tag{5.15}$$

β is the ratio between the power losses obtained with the electrical measurements and the power losses obtained with the calorimetric method. It is equal to 1, if there is no heat loss between the inputs and outputs of the cold plates. Nevertheless, according to the previous observations, this coefficient is necessarily larger than 1. Its evolution, presented in Figure 5.30(b), unveils

that β evolves between 1.02 and 1.07 for the two IGCTs, so convection effects with ambient air are negligible. Hence, it has been deemed irrelevant to multiply the power losses obtained with the coefficient β. Indeed, nothing but the maximum error of measurement of the flow-meter is $\pm 3\%$, as reported in Appendix C.

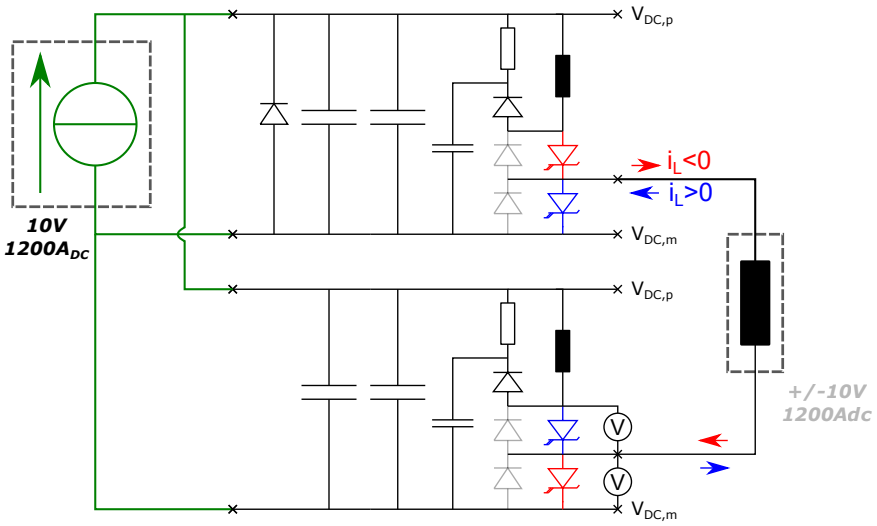
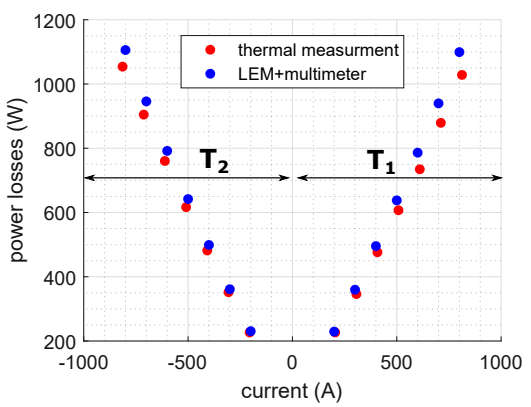
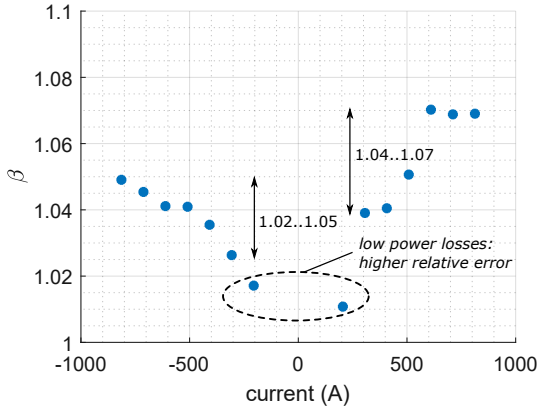


Figure 5.29: Special configuration to calibrate the thermal measurements, the output current is equal to the current of the DC power supply



(a) Power losses obtained using the calorimetric method and the electrical measurements (LEM+voltmeter)



(b) Evolution of β

Figure 5.30: Comparison between the thermal measurements and electrical measurements, without switching; DC current from -800 A_{DC} to 800 A_{DC}

5.2.3 MMC-like output current

The definition and the control of the MMC-like current for the test bench have been presented in 5.1.3.2. Since the output current is a complex signal, it is defined by different quantities such as its RMS value and its peak value, as in the case of Table 5.2. Another possibility, that has been retained, is to use the *equivalent DC link current* $i_{DC,eq}$, which is equal to three times the average output current, according to the properties of MMCs. This quantity allows to easily transpose the results obtained on the test bench to a real converter-station. The equivalence

for a few DC link currents is presented in Table 5.3. Besides, the arm-currents obtained for different equivalent DC link currents are shown in Figure 5.31.

$\mathbf{i_{DC,eq}}$/ $\mathbf{V_{DC}}$	±320 kV	±525 kV	±600 kV
100 A	64 MW	105 MW	120 MW
500 A	320 MW	525 MW	600 MW
1000 A	640 MW	1050 MW	1200 MW
1500 A	960 MW	1575 MW	1800 MW

Table 5.3: Relation between the equivalent DC link current, the DC link voltage and the power of the converter-station

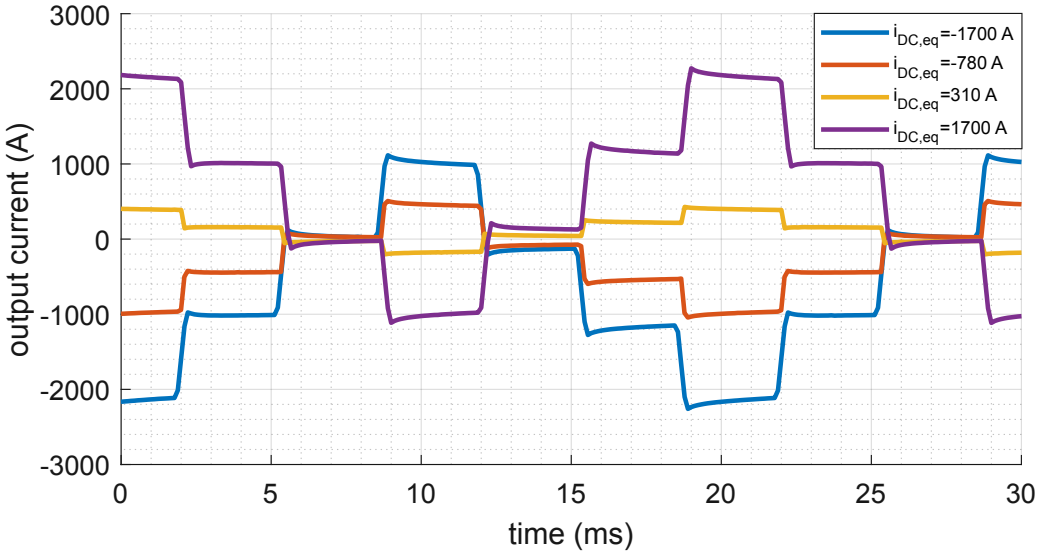


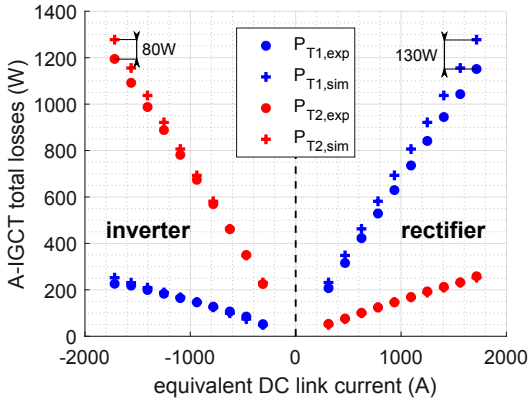
Figure 5.31: Output current measured for different operating conditions and corresponding $i_{DC,eq}$, V_{SM}=2500 V and f_{sw}=150 Hz

5.2.3.1 Comparison of the power losses with the simulation results

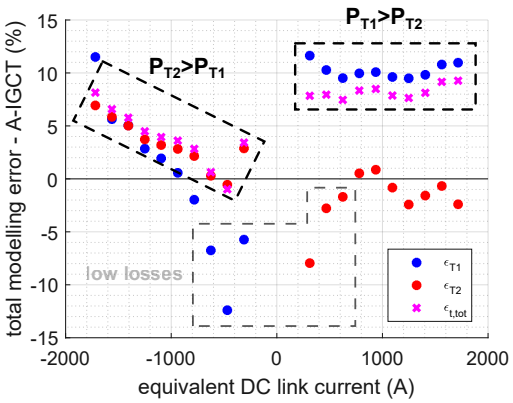
Validation of the decoupling method The decoupling issue, raised in 5.2.1.4, can only be observed when the upper and the lower IGCTs dissipate power, i.e. only when the sign of the current regularly changes. The decoupling relations (5.13) are applied to the power losses per cold plate P_{HA1}, P_{HA2}, and P_{HA3}, related to the IGCT stack. Figure 5.32(a) shows that the decoupling model provides consistent results over a wide range of power. Besides, Figure 5.32(b) shows that the decoupling model error is much smaller that the electro-thermal model error. Consequently, the decoupling approach applied to double-side cooled press-pack devices is relevant.

Conclusions For an equivalent DC link current up to 1710 A, under a constant switching of 150 Hz and a SM voltage of 2500 V, IGCTs and diodes exhibit a junction temperature lower than 55°C according to the thermal model. It corresponds to a rise in the junction temperature lower than 30°C. The semiconductor losses reach a maximum of 2650 W in the SM, plus 830 W of power losses in the clamp resistor R_{cl}, for an equivalent power of the converter-station of 1.1 GW, considering a DC link voltage of ±320 kV, according to Table 5.3. It implies a relative energy loss of 0.48% per converter-station. Consequently, this sub-module is perfectly compatible with

the constraints of the full-scale system, providing a high efficiency with low thermal stress for the semiconductor devices.



(a) Power losses of the two IGCTs for an MMC-like current; equivalent DC link current from -1715 A to 1715 A, V_{SM}=2500 V, f_{sw}=150 Hz



(b) Estimation error (%) of P_{T_1} and P_{T_2}, including the electro-thermal model error and the decoupling model error, and total estimation error (%) including only the electro-thermal model error

Figure 5.32: Power losses of the T_1 and T_2 with an MMC-like current and estimation error (%) after decoupling the thermal measurements

5.3 Power-loss analysis with the 10 kV RC-IGCTs

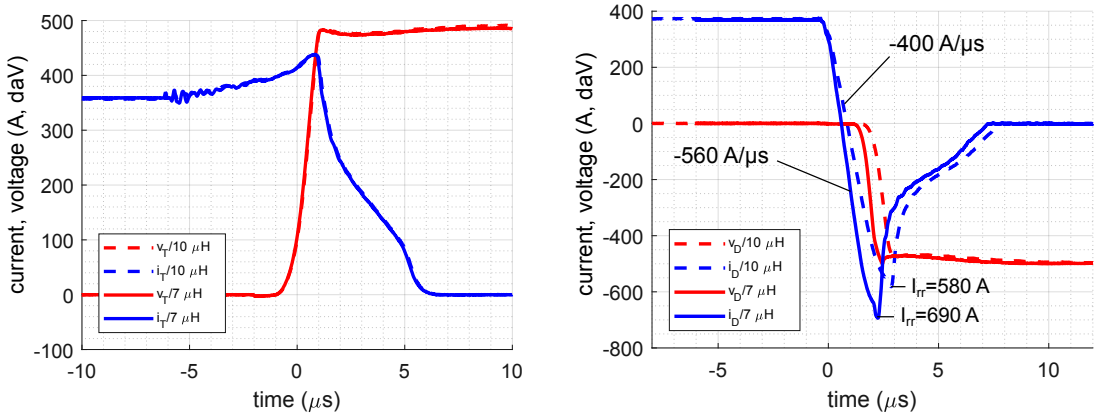
Designation	Notation	Value	Comments
SM voltage	V_{SM}	4700 V	voltage ripple $< 1.5\%$
		constant	
DC current	i_L	$[-400\ A_{DC}, 400\ A_{DC}]$	minimum current: 150 A_{DC}
MMC-like current	i_L	$[120\ A_{rms}, 510\ A_{rms}]$	$[\pm 260\ A_{pk}, \pm 1070\ A_{pk}]$
Switching frequency	f_{sw}	150 Hz	-
di/dt choke	L_{cl}	10 μH, 7 μH	-
clamp resistor	R_{cl}	1.2 Ω	1 resistor
clamp capacitor	C_{cl}	4 μF	4 capacitors in series/parallel

Table 5.4: Conditions of operation of the 10 kV RC semiconductor devices during the tests

High-voltage IGCTs have been identified as very promising devices, as they allow a reduction of the number of sub-modules with a meaningless increase in the power losses. In the meantime, reverse-conducting solutions enhance the compactness of the converter and its reliability, which are precious features in the field of offshore HVDC. In the fourth chapter, the IGCT 5SHX 20L8500 has shown limited current rating compared to the other devices. However, it benefits from all the advantages aforementioned. Currently, it is the reverse-conducting device having the highest voltage rating on the market, which can lead to a new range of applications for IGCTs. Its conditions of operation in the test bench are summarized in Table 5.4. As this device requires a SM voltage of 4700 V, the test bench has been modified to adopt the "high voltage" configuration, as presented in 5.1.1.3.

5.3.1 DC output current

5.3.1.1 Switching waveforms for different di/dt chokes



(a) Turn-off; GCT part (b) Turn-off; diode part

Figure 5.33: Switching waveforms of the RC-IGCT 5SHX 20L8500, V_{SM}=4700 V, i_L=400 A and two different di/dt chokes; L_{cl}=10 μH and L_{cl}=7 μH

Figure 5.33(b) shows the turn-off of the diode part for two di/dt chokes. For an output current of 400 A, the reverse-recovery current reaches respectively 1.45 pu and 1.72 pu with L_{cl}=10 μH and L_{cl}=7 μH. Because of the excessive impact of the recovery process, the diode part must be designed to ensure soft reverse-recovery and reduced switching losses at voltages as high as 5.3 kV [149]. The dynamic behaviour of the diode is different from previously observed (see Figure 5.16), in order to limit the turn-off losses as much as possible. The di/dt inductance hardly affect IGCT turn-off during the current fall; however, it influences the overvoltage that follows. The turn-off duration is longer than with the 4.5 kV asymmetric devices, so the dead-time has been increased from 10 μs to 15 μs.

5.3.1.2 Switching energies for different di/dt chokes and comparison with the available characteristics

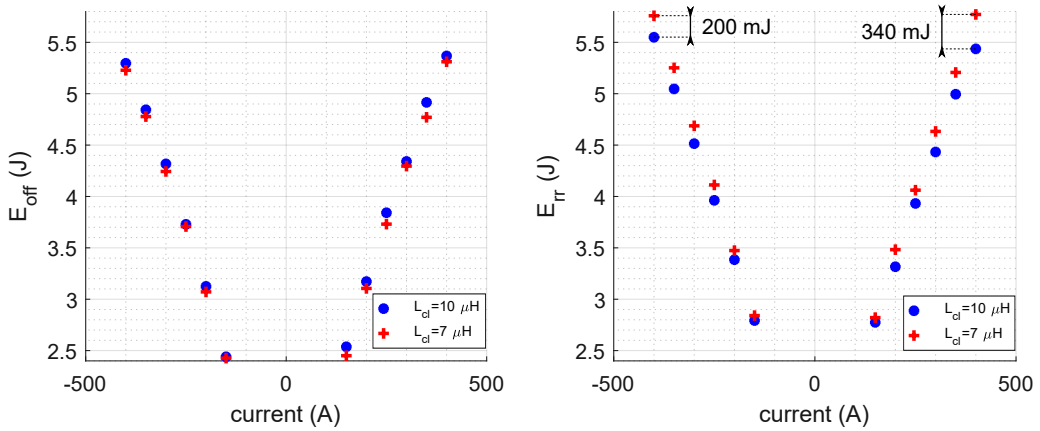
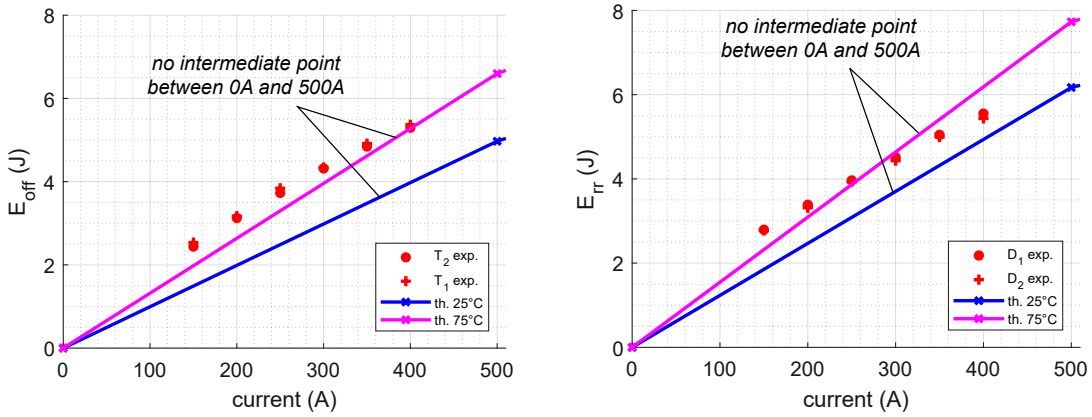


Figure 5.34: Turn-off energies of GCT and diode parts, for L_{cl}=10 μH (blue) and L_{cl}=7 μH (red), V_{SM}=4700 V

Figure 5.34 allows to quantify the influence of the di/dt choke: as expected GCT turn-off losses are hardly affected. On the other hand, diode turn-off losses increase when L_{cl} decreases;

a rise of about 5% can be noticed at the maximum output DC current. Despite poorer performances, reducing L_{cl} also reduces the volume of the clamp circuit. Furthermore, it may decrease clamp circuit power losses: this assumption is investigated later in the chapter.



(a) Turn-off energies, GCT part

(b) Turn-off energies, diode part

Figure 5.35: Evolution of the turn-off energies with V_{SM}=4700 V and L_{cl}=10 μH, electrical measurements with the test bench and "theoretical" results obtained from the double-pulse method

The evolution of the dynamic characteristics, shown in Figure 5.35, raises an issue. Due to the limited current rating of the RC-IGCT in steady-state, the DC output current is lower than the smallest current at which the device has been characterized with the double-pulse method, i.e. 500 A. As a consequence, the approximation of the dynamic characteristic is poor between 0 and 500 A, which explains that most of the experimental points are outside the expected boundaries. This issue also implies that the switching losses of the 10 kV RC-IGCT, assessed in the fourth chapter, have potentially been underestimated. It is worth mentioning that the static characteristics are not concerned, as the on-state voltages have been measured for currents as low as 100 A.

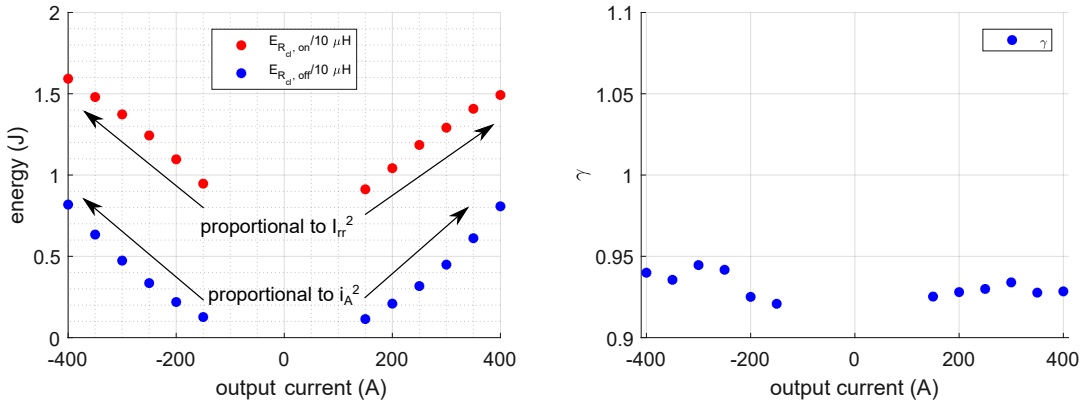
5.3.1.3 Calibration of the thermal measurements - clamp circuit power losses

As in the case of the semiconductors, clamp circuit power losses are measured using the calorimetric method. The influence of the convective heat exchange of the piping with ambient air, between the outlet of the water-cooled resistor and the temperature probe, is unknown. Consequently, a calibration of the clamp circuit power losses has been considered as well, based on the considerations and the approach of 5.2.2. A specificity of the clamp circuit is that the clamp resistor only dissipates energy during commutations. Then, it is possible to obtain the total power losses of the clamp circuit with a single voltage probe (and/or a current probe), assuming that the power losses of the diode D_{cl} and the power losses of the di/dt choke are negligible.
As explained in the third chapter, 3.2.4, the clamp resistor dissipates energy during IGCT turn-off and IGCT turn-on, for distinct reasons. During IGCT turn-off, an excess of energy $\frac{1}{2}L_{cl}i_A^2$ must be evacuated, whereas an additional energy $\frac{1}{2}L_{cl}I_{rr}^2$ is stored in the di/dt choke during diode turn-off, occuring at IGCT turn-on. This analysis is the origin of the analytic expressions (5.14). Thanks to the electrical measurements, these two sources of energy losses can be separated, as presented in Figure 5.36(a). It points out that the reverse-recovery current significantly influences the clamp circuit power losses, its contribution being especially dominant at low current. On the other hand, $E_{Rcl,off}$ has a higher contribution when the current increases, since the ratio $\frac{I_{rr}}{i_A}$ progressively decreases. From these energies, the power losses of the clamp

resistor $P_{R_{cl},elec}$ are calculated, and the factor γ is defined:

$$\gamma = \frac{P_{R_{cl},elec}}{P_{R_{cl},th}} \tag{5.16}$$

where $P_{R_{cl},th}$ corresponds to the power losses of the clamp resistor, calculated using the calorimetric method. According to Figure 5.36(b), γ is stable but remains inferior to 1. It implies that the power losses are underestimated with the electrical measurements, which is unusual. Some sources of inaccuracies can explain this result, for instance the error of the flow-meter (see Appendix C), which is not negligible in this case. The average value of γ, about 0.93, is close enough to 1 to be accepted. Nevertheless, the thermal measurements are not adjusted: the most pessimistic result is kept.



(a) Clamp resistor energy losses during IGCT turn-off $E_{Rcl,\,off}$ and during IGCT turn-on $E_{Rcl,\,on}$, with V_{SM}=4700 V

(b) Evolution of the factor γ with the output current, V_{SM}=4700 V and f_{sw}=150 Hz

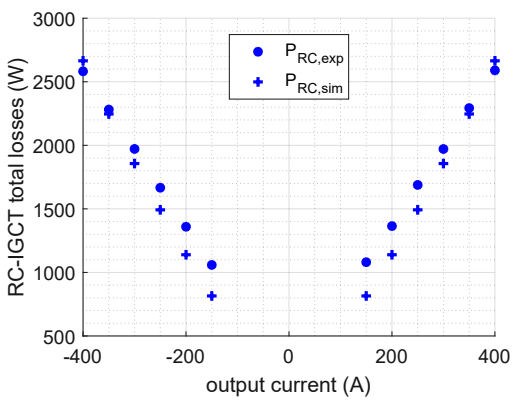
Figure 5.36: Clamp resistor energy losses during IGCT turn-off and IGCT turn-on, and evolution of the factor γ with the output current, V_{SM}=4700 V

5.3.1.4 Comparison of the semiconductor power losses with the simulation results

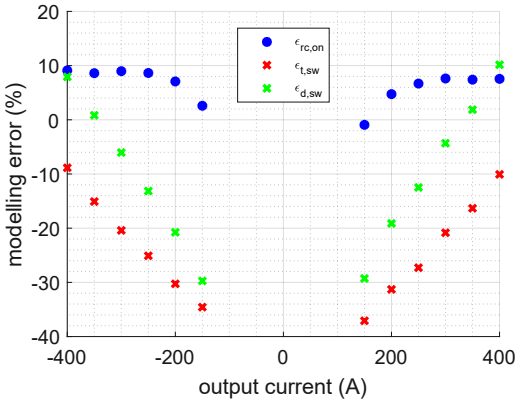
Figure 5.37(a), presenting the power losses of the two RC-IGCTs, indicates that the simulation results are quite accurate regarding the total power losses. However, the separation of the power losses per type, shown in Figure 5.37(b), unveils that switching losses are significantly underestimated, due to the aforementioned issue. On the other hand, on-state losses are accurately predicted, the estimation error typically varies between -2% and 10%. Consequently, a dynamic characterization at low current of the RC-IGCT would be mandatory to properly describe its behaviour over a wider range of operating conditions.

5.3.1.5 Assessment of the clamp circuit power losses

The assessment of the clamp circuit power losses is less accurate than previously: Figure 5.38 shows a difference from -15% to 20% between the thermal measurements and the simulation results. As mentioned in 5.3.1.1, the diode part of the RC-IGCT has been designed to minimize the turn-off losses, thus modifying the dynamic of recovery, i.e. the shape of the current waveform during turn-off. This phenomenon, not considered within the model of the clamp circuit, may explain this estimation error. A more complex model of the reverse-recovery would be necessary, considering the intrinsic parameters of the diode, to enhance the electro-thermal model of the clamp circuit.



(a) Total losses of the two RC-IGCTs, one operates only as a "GCT" whereas the other one operates only as a diode



(b) Estimation error (%) of RC-IGCT on-state losses $\epsilon_{rc,on}$, GCT turn-off losses $\epsilon_{t,sw}$ and diode turn-off losses $\epsilon_{d,sw}$

Figure 5.37: Evolution of the power losses of the two RC-IGCTs with the output current and relative estimation error, V_{SM}=4700 V, f_{sw}=150 Hz, and L_{cl}=10 μH

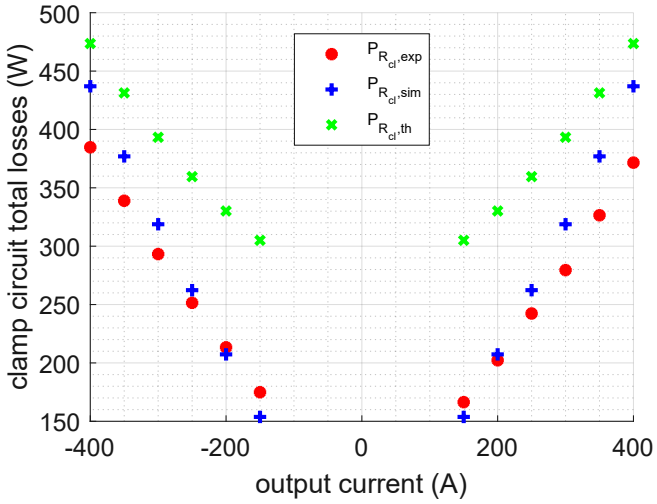


Figure 5.38: Evolution of the clamp circuit power losses with the output current: thermal measurements, simulation results and analytic expression, V_{SM}=4700 V and f_{sw}=150 Hz

5.3.2 MMC-like output current

5.3.2.1 IGCT turn-off

As in the case of the 4.5 kV devices, the output current is controlled to obtain an MMC-like current: DC and grid-frequency components are automatically adjusted to reproduce the arm-current of a real converter-station. As mentioned in Table 5.4, this mode of operation allows to reach a peak current larger than ±1 kA, as presented in Figure 5.39. It can be concluded that the operation of the RC-IGCTs comply with the expectations. Figure 5.40 focuses on the moment when T_2 turns off (the same conditions are reproduced for T_1 turn-off). The turn-off at 1050 A is performed by T_1, whereas the turn-off at -1050 A is performed by T_2: the resulting turn-off energies are almost identical, about 9.10 J. This value is consistent, since the expected values are 8.75 J @4700 V/1000 A/25°C with a di/dt choke of 7 μH, and 10.7 J @4700 V/1000 A/25°C with a di/dt choke of 10 μH. This comparison could not be performed in 5.3.1.2, due to the lack of points in the dynamic characteristic of the device under 500 A.

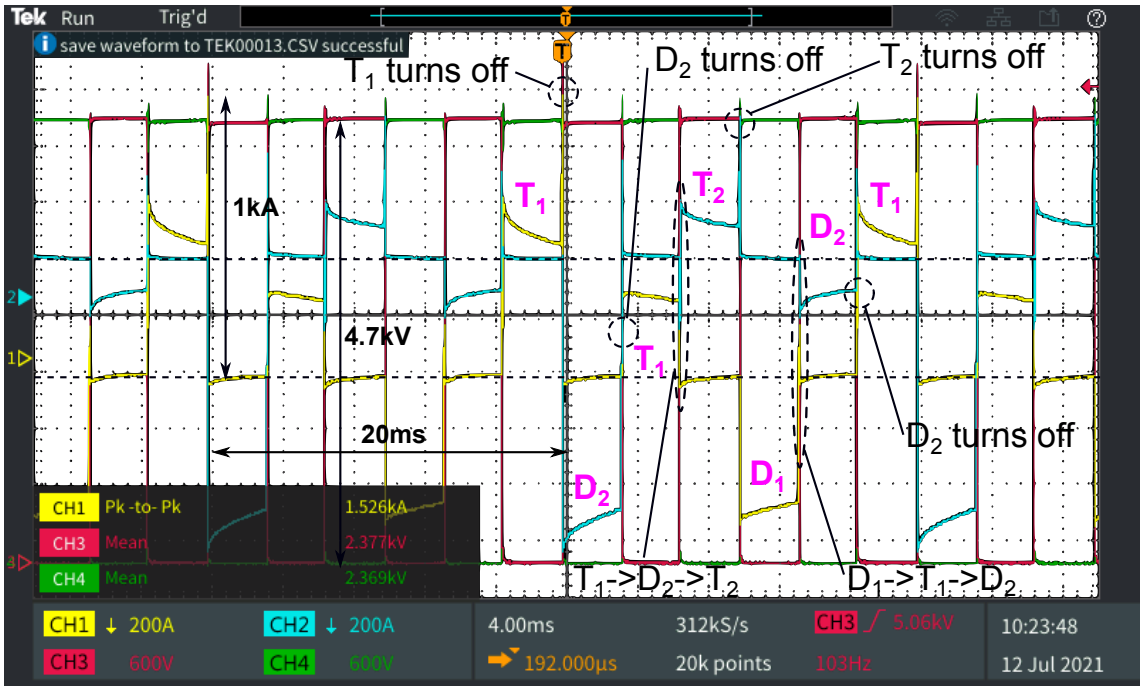


Figure 5.39: i_{T1} (yellow), i_{T2} (blue), v_{T1} (red) and v_{T2} (green) for an equivalent DC link current of 750 A, V_{SM}=4700 V, f_{sw}=150 Hz

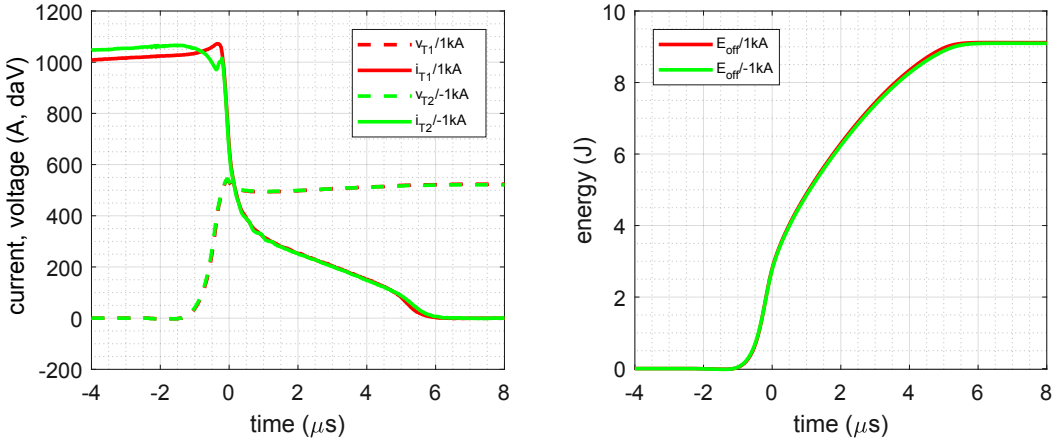


Figure 5.40: GCT turn-off at 4700 V/±1050 A with a steady-state current of 510 A_{rms}, L_{cl}=7 μH (left), and resulting turn-off energy

5.3.2.2 Dynamics of the clamp circuit

Figure 5.41 presents a GCT turn-off and a diode turn-off at the maximum reachable currents with the MMC-like current, respectively 1050 A and 330 A, as suggested by Figure 5.39. An important concern is the time interval during which the clamp circuit operates, since it defines the minimum pulse width duration of the SM. As explained in the second chapter, in 2.4.2.2, a minimum pulse width of 50 μs has been deemed sufficient for IGCTs. The two commutations presented in Figure 5.41 unveil that the clamp circuit carries out a full cycle of operation within 30 μs, which is lower than the minimum pulse width $T_{PW,min}$ retained in the previous chapters. The maximum voltage is 5450 V, a relative overvoltage of 16% is acceptable as it does not endanger the MTTF of the semiconductors. Since both the total turn-off duration and the overvoltages are satisfactory, it can be concluded that the design of the clamp circuit meets the

requirements of a MMC sub-module.

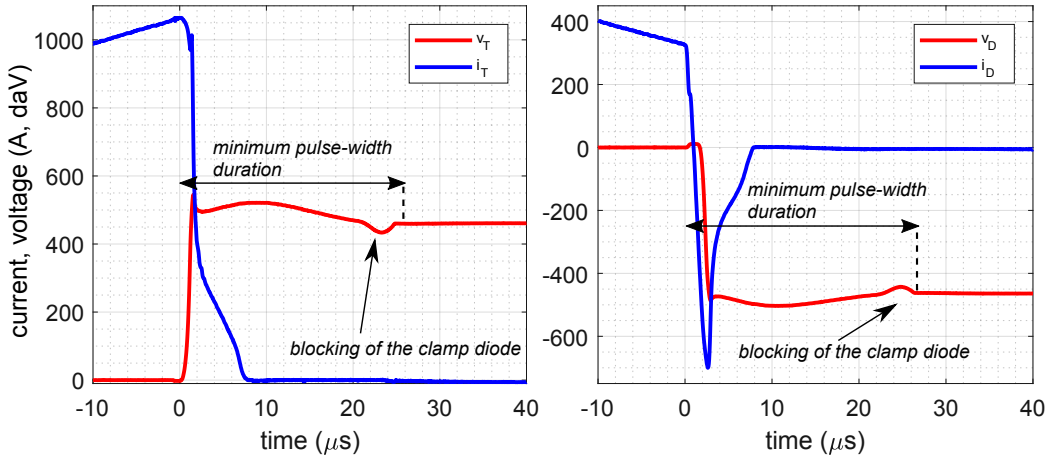


Figure 5.41: GCT part turn-off at 4700 V/±1050 A (left), and a diode part turn-off at 4700 V/±330 A (right)

5.3.2.3 Comparison of the power losses with the simulation results

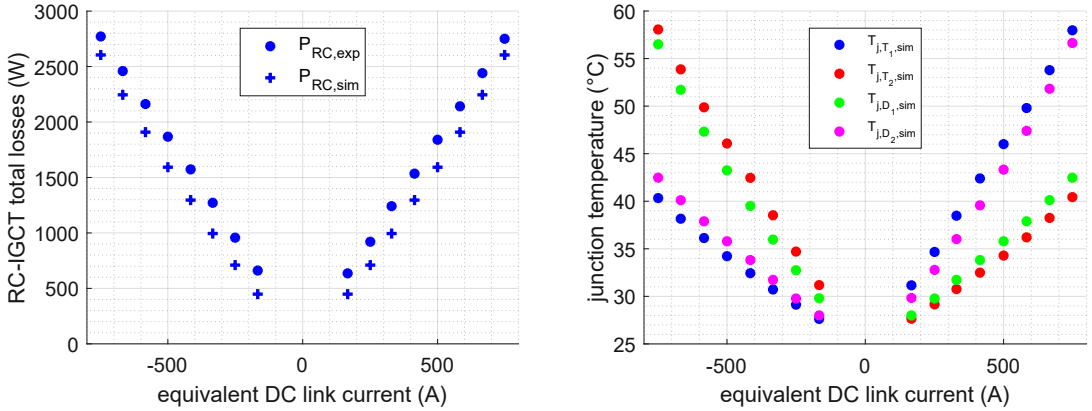
The underestimation of the switching losses at low currents is still visible in Figure 5.42(a). Yet, the electro-thermal model is accurate for high-power operation: the modelling error is lower than 10% when the total power losses exceed 2000 W. The simulation results unveil that the junction temperatures evolve between 25°C and 60°C, which is a sufficient range to validate the model. In the meantime, the maximum junction temperature does not rise above T_{water}+35°C. The 10 kV RC-IGCTs experience suitable thermal stress for an equivalent DC link current up to ±750 A, corresponding to a transmitted power of ±480 MW according to Table 5.3.

5.3.2.4 Influence of the di/dt inductance L_{cl}

As observed in 5.3.1.2, the reduction of the di/dt limiting inductance is supposed to increase the diode turn-off losses, even though the reverse-recovery is slightly faster. The power losses of the sub-module for two different di/dt chokes, L_{cl}=10 μH and L_{cl}=7 μH, in the case of an MMC-like current, have been reported in Figure 5.43. For a di/dt choke of 10 μH, the contribution of clamp power losses to total power losses increases with the equivalent DC link current: it is 11% at 250 A, reaching 16% at 750 A.

The semiconductors losses are slightly higher with L_{cl}=7 μH than with L_{cl}=10 μH, because of the diode turn-off losses. However, the clamp circuit power losses are significantly reduced, by 20% for an equivalent DC current of 250 A, and by 30% for an equivalent DC current of 750 A. This gain is due to the smaller amount of energy stored. Besides, the reduction is more significant at high current, because the contribution of the clamp circuit power losses due to IGCT turn-on (i.e. diode turn-off) decreases with increasing currents, as observed in Figure 5.3.1.3. Consequently, the minimization of the di/dt choke is especially attractive at high currents.

At the scale of an IGCT-based SM, the reduction of the clamp circuit power losses overtakes the rise in the diode turn-off losses. Moreover, it also leads to a more compact design of the commutation cell. Nevertheless, L_{cl} must be high enough to ensure a reasonable level of reliability, as the rise in the di/dt affects the failure rate of the diode part (see 1.3.1.3). Therefore, it represents an efficient strategy to enhance the performances of IGCT-based SMs, as long as the failure rate of the diode is properly handled.



(a) Power losses of the two RC-IGCTs for an MMC-like current, V_{SM}=4700 V, f_{sw}=150 Hz, L_{cl}=10 μH

(b) Estimated junction temperatures for an MMC-like current, V_{SM}=4700 V, f_{sw}=150 Hz

Figure 5.42: Evolution of the power losses of the two RC-IGCTs with the equivalent DC link current and estimated junction temperatures (simulations), V_{SM}=4700 V and f_{sw}=150 Hz

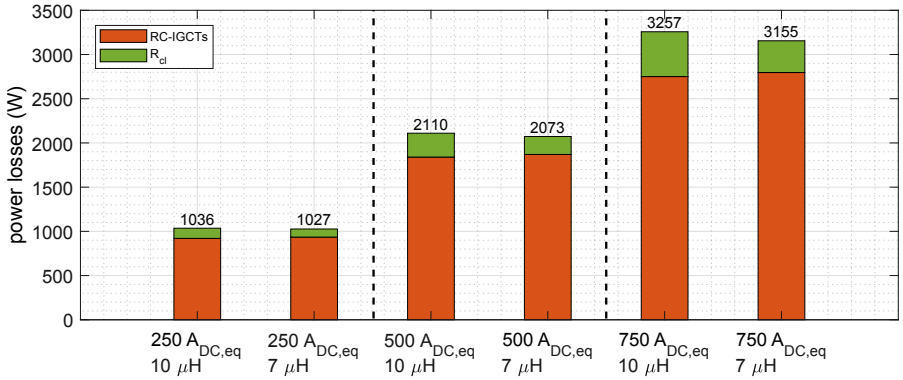


Figure 5.43: Evolution of semiconductors power losses and clamp circuit power losses with the equivalent DC link current, for two different di/dt chokes L_{cl}, V_{SM}=4700 V and f_{sw}=150 Hz

5.3.2.5 Conclusions

The 10 kV RC-IGCT offers promising performances, beyond its high voltage rating. A wide range of operating conditions has been validated for a switching frequency of 150 Hz, i.e. the maximum switching frequency considered in the fourth chapter. A transmitted power close to 500 MW, under a ±320 kV DC link voltage, could be obtained in HVDC converter-stations, up to 900 MW under a ±600 kV DC link voltage. The electro-thermal model have provided consistent results compared to the experimental measurements, especially regarding the clamp circuit power losses. Commutations, including the dynamic of the clamp circuit, are fast enough to comply with the constraints inherent to the traditional control strategies for high-power MMCs. The maximum di/dt allowed by the diode part is a crucial rating, as it influences the volume of the SM and the distribution of power losses between the diode part itself and the clamp resistor.

5.4 Conclusion of the experiments

The opposition method applied to MMC SMs has proven to be relevant in order to analyse steady-state operation of IGCT, along with its clamp circuit. Calorimetric method and waveforms obtained during commutations allow for the separation of on-state and switching losses, providing a way to select the best semiconductor devices on the technology curve. Thanks to a rapid prototyping controller and a LEM current sensor, an output current with the same characteristics as an arm-current in actual HVDC converter-stations can be reproduced. With a voltage rating up to 5 kV and current ratings up to 1200 A_{rms}/2500 A_{pk}, the test bench designed and assembled in the scope of the PhD thesis allows for the testing of semiconductors for equivalent powers up to 1.1 GW, considering ±320 kV XLPE cables.

The electro-thermal models presented in the third chapter have exhibited a satisfactory accuracy, with an estimation error of about 10%. However, it has been observed that the stray inductances of the commutation cell significantly affect switching losses. The new approach, considered to estimate the clamp circuit power losses, has proven to be much more accurate than the traditional energy-based formula. It comes out that clamp circuit power losses are smaller in reality, compared to analytic calculations.

4.5 kV asymmetric devices have important current ratings, even at the maximum current capabilities of the test bench it is estimated that the junction temperatures have not exceeded 70°C. These devices are naturally designed for higher power operation, potentially 1.5 GW or even more. 10 kV RC-IGCTs are more relevant for powers lower than 1 GW, under a DC link voltage of ±320 kV, in the moment, due to their higher on-state and switching losses. A maximum turn-off current of 1050 A has been reached in steady-state, for a maximum rating of 1800 A.

The di/dt choke L_{cl} has been experimentally identified as a key factor, involved in the design of IGCT-based SMs: the reduction of L_{cl} is favourable in terms of efficiency and volume. However, the resulting performances are mitigated by the tough trade-off between on-state and switching losses for high voltage IGCTs. Even with a switching frequency of 150 Hz, switching losses are almost equal to on-state losses. In this context, soft switching circuits would be especially relevant: the ARCP circuit presented in 2.1.3.2 could significantly reduce the overall power losses of the SM, for a lighter design.

Conclusion and outlook

Overall conclusion

The work carried out during this PhD thesis has shown that efficient and promising technological solutions exist to connect remote offshore wind-parks to the onshore grid. IGCTs anticipate the current trend, where transmitted powers are increasing along with the connection voltages, while offering a reduced level of losses. These features support the progressive reduction of LCOE regarding offshore wind energy, paramount to favour the expansion of renewable energy sources.

A state of the art has been presented in the first chapter, to understand the main issues related to grid-connection of offshore wind-farms. Among the static converters for HVDC power transmission, VSC technology has come out as a relevant solution. MMCs, in particular, offer many features to facilitate the development of HVDC links in remote or isolated areas. IGCTs show attractive performances and properties in the field of HVDC. With 10 kV devices and 6 inch versions, they reach voltage and current ratings superior to IGBT's.

The second chapter has dealt with the design of the HVDC link, including the two converter-stations and the sub-modules inside them. With IGCTs, the protection strategy of a SM can be simplified, especially because of its SCFM and the di/dt choke of the clamp circuit. The ARCP, which aims to replace the RCD snubber, is a promising soft switching circuit with a reduced volume and a low complexity. Regarding control aspects, NLC is more suitable than PWM due to the inherent minimum pulse width it introduces. Besides, it offers a high degree of flexibility to dynamically adapt the switching frequency, and the possibility to reduce switching losses thanks to dedicated sorting algorithms.

Considering electrical quantities and the properties of the water cooling circuit, a power-loss model has been proposed in the third chapter. The successive steps of simplification of the MMC's topology have been presented, oriented towards a reduction of the computation time. A new approach, to estimate the power losses of the clamp circuit, has been introduced. The different models have been gathered in a single simulation tool, implemented with MATLAB, able to provide all the state-space variables of the converter-station, including the power losses and the junction temperatures of the 24N semiconductor devices, within 30 seconds.

A power-loss analysis of the HVDC converter-stations has been performed in the fourth chapter, considering the intermittent energy production of offshore wind-farms. 4.5 kV asymmetric IGCTs have shown reduced power losses and reduced thermal stress. RC-IGCTs have come out as an attractive trade-off considering efficiency, volume and cost issues. 6.5 kV IGCTs and 10 kV IGCTs offer a clear advantage as they allow a reduction of the number of SMs in

the converter-stations, even though their potential is limited by their switching losses and the clamp circuit power losses.

The fifth chapter has focused on an experimental validation of the hypotheses and the models formulated in the previous chapters. The high current capability of the 4.5 kV IGCTs has been confirmed, for a wide range of operating conditions, inherent to the converter-stations. Power losses have been measured throughout different instruments and different methods. Besides, calibration protocols have been carried out to ensure the exactness of the results. Estimation errors regarding switching losses have been obtained; the main factors influencing them have been identified for IGCTs and diodes. The accuracy of the power-loss models, developed in the third chapter, has been validated for different voltages, currents, switching frequencies, and a variable junction temperature, during steady-state operation. 10 kV RC-IGCTs have unveiled important power losses, but a sufficient SOA to safely operate in steady-state with a SM voltage of 4700 V, a switching frequency of 150 Hz, and currents larger than 500 A_{rms}/1 000 A_{peak}.

Future work

The work in this PhD thesis has brought to light many areas of interest, to enhance the performances of the sub-modules. Regarding efficiency and volume, the reduction of the di/dt limiting inductance is beneficial: diodes withstanding a high di/dt, i.e. larger than 5 kA/μs, are relevant with IGCTs. Such diodes already exist as discrete devices, but the integration into an RC-IGCT would contribute even more to enhance sub-module's compactness.

Regarding high-voltage IGCTs, switching losses and clamp circuit power losses have a significant contribution to the total level of power losses. In the meantime, the ARCP circuit introduced in the second chapter has come out as a potential alternative to the traditional clamp circuit. For a similar volume and reliability, switching losses can be drastically reduced and clamp circuit power losses would no longer exist with an ARCP circuit. Therefore, ARCP circuit testing with 6.5 kV IGCTs and 10 kV IGCTs would be relevant, in order to compare the two designs and to conclude regarding the potential of soft switching circuits with high-voltage IGCTs.

Volume constraints have not been considered in the scope of this PhD thesis, since the SMs assembled have been especially designed for power-loss measurement and laboratory testing, with the capability to be reconfigured. The design of an IGCT-based sub-module, oriented towards industrial applications, could unveil issues or, on the contrary, additional advantages compared to IGBTs.

Bibliography

[1] European Commission. *An EU Strategy to harness the potential of offshore renewable energy for a climate neutral future*. 2020. URL: https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=COM%7B%5C%%7D3A2020%7B%5C%%7D3A741%7B%5C%%7D3AFIN%7B%5C&%7Dqid=1605792629666 (visited on 07/19/2021).

[2] The White House. *FACT SHEET: Biden Administration Jumpstarts Offshore Wind Energy Projects to Create Jobs*. 2021. URL: https://www.whitehouse.gov/briefing-room/statements-releases/2021/03/29/fact-sheet-biden-administration-jumpstarts-offshore-wind-energy-projects-to-create-jobs/ (visited on 07/19/2021).

[3] R. J. Barthelmie et al. "Meteorological aspects of offshore wind energy: Observations from the Vindeby wind farm". In: *Journal of Wind Engineering and Industrial Aerodynamics* 62.2-3 (1996), pp. 191–211. ISSN: 01676105. DOI: 10.1016/S0167-6105(96)00077-3.

[4] S. A. Hsu. "Models for estimating offshore winds from onshore meteorological measurements". In: *Boundary-Layer Meteorology* 20.3 (1981), pp. 341–351. ISSN: 00068314. DOI: 10.1007/BF00121378.

[5] European Environment Agency. *Europe's onshore and offshore wind energy potential*. Tech. rep. 6. Copenhagen: European Environment Agency, 2009. DOI: 10.2800/11373.

[6] Working Group B4.55 CIGRE. *HVDC Connection of Offshore Wind Power Plants*. 2015. URL: https://e-cigre.org/publication/619-hvdc-connection-of-offshore-wind-power-plants (visited on 04/19/2019).

[7] EDP Energias de Portugal. *Floating offshore wind-power generating platform*. 2018. URL: https://www.edp.com/en/innovation/windfloat (visited on 07/19/2021).

[8] Marie-Laure Guillerminet et al. *Couts des énergies renouvelables en France édition 2016*. Tech. rep. ADEME, 2016. URL: https://www.ademe.fr/sites/default/files/assets/documents/couts%7B%5C_%7Denergies%7B%5C_%7Drenouvelables%7B%5C_%7Den%7B%5C_%7Dfrance%7B%5C_%7Dedition2016v1.pdf.

[9] Ana Fernández-Guillamón et al. "Offshore wind power integration into future power systems: Overview and trends". In: *Journal of Marine Science and Engineering* 7.11 (2019). ISSN: 20771312. DOI: 10.3390/jmse7110399.

[10] ABB. *ABB Review - 60 years of HVDC*. Tech. rep. Zurich: ABB Technology Ltd., 2014. URL: https://library.e.abb.com/public/aff841e25d8986b5c1257d380045703f/140818%20ABB%20SR%2060%20years%20of%20HVDC%7B%5C_%7D72dpi.pdf.

[11] C. Bartzsch et al. "HVDC LCC Technology Developments to facilitate Integration of Bulk Wind Power Resources". In: *HVDC and Power Electronics International Colloquium*. Agra, 2015.

[12] Working Group 04 of Study Committee 14. *Compendium Of HVDC Schemes Throughout The World*. Tech. rep. CIGRE, 1987. URL: https://e-cigre.org/publication/003-compendium-of-hvdc-schemes-throughout-the-world.

[13] ENTSO-E. *HVDC Mass Impregnated (MI) cables*. 2021. URL: https://www.entsoe.eu/Technopedia/techsheets/hvdc-mass-impregnated-mi-cables (visited on 06/07/2021).

[14] ENTSO-E AISBL. *Offshore Transmission Technology*. Tech. rep. ENTSO-E, 2011, pp. 1–44. URL: https://eepublicdownloads.entsoe.eu/clean-documents/pre2015/publications/entsoe/SDC/European%7B%5C_%7Doffshore%7B%5C_%7Dgrid%7B%5C_%7D-%7B%5C_%7DOffshore%7B%5C_%7DTechnology%7B%5C_%7D-%7B%5C_%7DFINALversion.pdf.

[15] ENTSO-E. *HVDC Cross-linked Polyethylene (XLPE) cables*. 2021. URL: https://www.entsoe.eu/Technopedia/techsheets/hvdc-xlpe-cross-linked-polyethylene (visited on 06/07/2021).

[16] Anders Gustafsson et al. *The new 525 kV extruded HVDC cable system*. Tech. rep. ABB Grid Systems, 2014. URL: https://resources.news.e.abb.com/attachments/published/12792/en-US/D6D3A232A090/The-new-525-kV-extruded-HVDC-cable-system-White-PaperFINAL.pdf.

[17] K Koyama et al. "Total System Development on Innovative and Large Scaled HVDC Cable System towards Expanded Installation of Large Offshore Wind Farms". In: *CIGRE 2020*. Paris, 2020.

[18] TenneT. *Information for cable suppliers 525 kV HVDC XLPE*. 2019. URL: https://www.tennet.eu/our-grid/offshore-grid-netherlands/information-for-cable-suppliers-525-kv-hvdc-xlpe/ (visited on 06/07/2021).

[19] Prysmian. *Extruded Cables for HVDC Power Transmission*. Tech. rep. Milan: Prysmian, 2020. URL: https://www.prysmiangroup.com/sites/default/files/business%7B%5C_%7Dmarkets/markets/downloads/datasheets/BR%7B%5C_%7DHVDC%7B%5C_%7D2018%7B%5C_%7Drev12%7B%5C_%7D%7B%5C_%7D0.pdf.

[20] NKT Group GmbH. *640 kV XLPE HVDC cable system*. Tech. rep. Cologne: NKT, 2017. URL: https://nkt.widen.net/content/74qakygsgk/pdf/640kV-XLPEHV%7B%5C_%7DHV%7B%5C_%7DDS%7B%5C_%7DEN.pdf?u=gj0n1y.

[21] P. Labra Francos et al. "INELFE – Europe's first integrated onshore HVDC interconnection". In: *2012 IEEE Power and Energy Society General Meeting*. 2012, pp. 1–8. DOI: 10.1109/PESGM.2012.6344799.

[22] Paola Bresesti et al. "HVDC Connection of Offshore Wind Farms to the Transmission System". In: *IEEE Transactions on Energy Conversion* 22.1 (Mar. 2007), pp. 37–43. ISSN: 0885-8969. DOI: 10.1109/TEC.2006.889624.

[23] I Arrambide, I Zubia, and I Zamora. "VSC-HVDC technology on power systems and offshore wind farms integration". In: *Electrical Engineering Electronic Journal (EEEJ)* 1.3 (2016), pp. 43–47.

[24] TenneT TSO GmbH. *Requirements for Offshore Grid Connections in the Grid of TenneT TSO GmbH*. Tech. rep. Bayreuth: TenneT, 2012, pp. 1–14. URL: https://www.tennet.eu/fileadmin/user%7B%5C_%7Dupload/The%7B%5C_%7DElectricity%7B%5C_%7DMarket/German%7B%5C_%7DMarket/Grid%7B%5C_%7Dcustomers/tennet%7B%5C_%7Dtso%7B%5C_%7Dgmbh-asn-eng%7B%5C_%7D21122012%7B%5C_%7Dfinal%7B%5C_%7D1%7B%5C_%7D.pdf.

[25] TenneT. *Converter - "Sockets" at sea and on land*. 2021. URL: https://www.tennet.eu/our-grid/offshore-projects-germany/our-technology/converter/ (visited on 07/15/2021).

[26] Haseeb Ahmad, Steven Coppens, and Bahri Uzunoglu. "Connection of an Offshore Wind Park to HVDC Converter Platform without Using Offshore AC Collector Platforms". In: *2013 IEEE Green Technologies Conference (GreenTech)*. IEEE, Apr. 2013, pp. 400–406. ISBN: 978-0-7695-4966-8. DOI: 10.1109/GreenTech.2013.68.

[27] Jiuping Pan et al. "DC Connection of Offshore Wind Power Plants without Platform". In: *13th Wind Integration Workshop*. Berlin, 2014, pp. 1–6. URL: https://abblibrary.s3.amazonaws.com/public/b33fd96a874651a8c1257d97002b7f31/DC%20Connection%20of%20Offshore%20Wind%20Power%20Plants.pdf.

[28] Roland Ryndzionek and Łukasz Sienkiewicz. "Evolution of the HVDC link connecting offshore wind farms to onshore power systems". In: *Energies* 13.8 (2020). ISSN: 19961073. DOI: 10.3390/en13081914.

[29] CIGRE Working Group B4.57. *Guide for the Development of Models for HVDC Converters in a HVDC Grid*. Tech. rep. Paris: CIGRE, 2014. URL: https://e-cigre.org/publication/604-guide-for-the-development-of-models-for-hvdc-converters-in-a-hvdc-grid.

[30] M Vardikar et al. "Overview and Key Features of +/- 320 kV, 2x1000 MW Pugalur-Trichur VSC HVDC Link". In: *CIGRE India 2019* 8.2 (2019).

[31] Sébastien Dennetière et al. "Modeling of Modular Multilevel Converters for the France-Spain link". In: *International Conference on Power Systems Transients*. Vancouver, 2013, pp. 1–7.

[32] Kurt Friedrich. "Modern HVDC PLUS application of VSC in Modular Multilevel Converter topology". In: *IEEE International Symposium on Industrial Electronics*. 2010. ISBN: 9781424463916. DOI: 10.1109/ISIE.2010.5637505.

[33] Kamran Sharifabadi et al. *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. Chichester: John Wiley & Sons, 2016. ISBN: 978-1-118-85156-2.

[34] Michael Bahrman and Brian Johnson. "The ABCs of HVDC transmission technologies". In: *IEEE Power and Energy Magazine* 5.2 (Mar. 2007), pp. 32–44. ISSN: 1540-7977. DOI: 10.1109/MPAE.2007.329194.

[35] European Commission. *Network code on requirements for grid connection of generators*. Tech. rep. Brussels: ENTSO-E, 2016. URL: https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=OJ:JOL%7B%5C_%7D2016%7B%5C_%7D112%7B%5C_%7DR%7B%5C_%7D0001.

[36] Nikolas Flourentzou, Vassilios G. Agelidis, and Georgios D. Demetriades. "VSC-based HVDC power transmission systems: An overview". In: *IEEE Transactions on Power Electronics* (2009). ISSN: 08858993. DOI: 10.1109/TPEL.2008.2008441.

[37] Antony James Beddard. "Factors Affecting the Reliability of VSC-HVDC for the Connection of Offshore Windfarms". PhD thesis. University of Manchester, 2014, pp. 1–305.

[38] Oluwafemi E Oni, Innocent E Davidson, and Kamati N I Mbangula. "A Review of LCC-HVDC and VSC-HVDC Technologies and Applications". In: *IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*. Florence, 2016, pp. 1–7. ISBN: 9781509023202. DOI: 10.1109/EEEIC.2016.7555677.

[39] S K Chaudhary, R Teodorescu, and P Rodriguez. "Wind Farm Grid Integration Using VSC Based HVDC Transmission-An Overview". In: *2008 IEEE Energy 2030 Conference*. Atlanta: IEEE, 2008. DOI: 10.1109/ENERGY.2008.4781061.

[40] B. Gemmell et al. "Prospects of multilevel VSC technologies for power transmission". In: *2008 IEEE/PES Transmission and Distribution Conference and Exposition*. IEEE, Apr. 2008, pp. 1–16. ISBN: 978-1-4244-1903-6. DOI: 10.1109/TDC.2008.4517192.

[41] J. Arrillaga, Y. H. Liu, and N. R. Watson. *Flexible Power Transmission: The HVDC Options*. John Wiley & Sons, 2007. ISBN: 9780470056882. DOI: 10.1002/9780470511862.

[42] Anton Lesnicar and Rainer Marquardt. "An innovative modular multilevel converter topology suitable for a wide power range". In: *2003 IEEE Bologna Power Tech Conference Proceedings*. Bologna: IEEE, 2003. ISBN: 0780379675. DOI: 10.1109/PTC.2003.1304403.

[43] Rainer Marquardt and Anton Lesnicar. "New Concept for High Voltage – Modular Multilevel Converter". In: *PESC 2004 - Aachen* (2004). DOI: 10.1109/PTC.2003.1304403.

[44] Justin Gerdes. *Siemens Debuts HVDC PLUS with San Francisco's Trans Bay Cable*. Tech. rep. HVDC. San Fransisco: Siemens, 2011.

[45] A. L.P. De Oliveira et al. "Prospects of Voltage-Sourced Converters (VSC) applications in DC transmission systems". In: *2010 IEEE/PES Transmission and Distribution Conference and Exposition: Latin America (T&D-LA)*. IEEE, 2011, pp. 491–495. ISBN: 9781457704871. DOI: 10.1109/TDC-LA.2010.5762927.

[46] Alberto Persico et al. "IFA2 - HVDC goes compact with Hybrid PASS420 modules and GIB connections". In: *2019 AEIT HVDC International Conference (AEIT HVDC)*. Ed. by IEEE. Florence: IEEE, 2019, pp. 1–6. ISBN: 9781728120713. DOI: 10.1109/AEIT-HVDC.2019.8740612.

[47] Kalle Ilves et al. “On energy storage requirements in modular multilevel converters”. In: *IEEE Transactions on Power Electronics* 29.1 (2014), pp. 77–88. ISSN: 08858993. DOI: 10.1109/TPEL.2013.2254129.

[48] Markus Billmann, Otto Kreutzer, and Martin Nagelmüller. “Modular Multilevel Submodules for Converters, from the State of the Art to Future Trends”. In: *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Nurember, 2018.

[49] Jaime Peralta et al. “Detailed and Averaged Models for a 401-Level MMC–HVDC System”. In: *IEEE Transactions on Power Delivery* 27.3 (July 2012), pp. 1501–1508. ISSN: 0885-8977. DOI: 10.1109/TPWRD.2012.2188911.

[50] Michael M. C. Merlin et al. “The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability”. In: *IEEE Transactions on Power Delivery* 29.1 (Feb. 2014), pp. 310–317. ISSN: 0885-8977. DOI: 10.1109/TPWRD.2013.2282171.

[51] Michaël M.C. Merlin and Tim C. Green. “Cell capacitor sizing in multilevel converters: Cases of the modular multilevel converter and alternate arm converter”. In: *IET Power Electronics* 8.3 (2015), pp. 350–360. ISSN: 17554543. DOI: 10.1049/iet-pel.2014.0328.

[52] Deepak Tiku. “dc Power Transmission: Mercury-Arc to Thyristor HVdc Valves”. In: *IEEE Power and Energy Magazine* 12.2 (2014), pp. 76–96. ISSN: 15407977. DOI: 10.1109/MPE.2013.2293398.

[53] Jan Vobecký. “Design and Technology of High-Power Silicon Devices”. In: *18th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2011*. Gliwice: IEEE, 2011, p. 702. ISBN: 9781457703041.

[54] Silverio Alvarez Hidalgo. “Characterisation of 3.3kV IGCTs for Medium Power Applications”. PhD thesis. Institut National Polytechnique de Toulouse, 2005, pp. 1–217.

[55] Philippe Leturcq. “Composants semi-conducteurs de puissance bipolaires. Partie 2”. In: *Techniques de l’ingénieur Conversion de l’énergie électrique* TIP301WEB.ref. article : d3107 (2001). DOI: 10.51257/a-v1-d3107.

[56] Steffen Bernet. “Recent developments of high power converters for industry and traction applications”. In: *IEEE Transactions on Power Electronics* 15.6 (2000), pp. 1102–1117. ISSN: 08858993. DOI: 10.1109/63.892825.

[57] Gunnar Asplund, Kjell Eriksson, and Kjell Svensson. “DC Transmission based on Voltage Source Converters”. In: *CIGRE SC14 Colloquium in South Africa*. 1997.

[58] Steffen Bernet et al. “Comparison of high-power IGBT’s and hard-driven GTO’s for high-power inverters”. In: *IEEE Transactions on Industry Applications* 35.2 (1999), pp. 487–495. ISSN: 00939994. DOI: 10.1109/28.753645.

[59] David Weiss et al. “IGCT-based modular multilevel converter for an AC-AC railway power supply”. In: *PCIM Europe 2017 - International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2017, pp. 1–8. ISBN: 9783800744244.

[60] Philippe Ladoux, Nicola Serbia, and Eric Carroll. “On the Potential of IGCTs in HVDC”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 3.3 (2015), pp. 780–793. ISSN: 2168-6777. DOI: 10.1109/JESTPE.2015.2429116.

[61] Markus Billmann and Herbert Gambach. “Explosion proof housings for IGBT module based high power inverters in HVDC transmission application”. In: *PCIM 2009*. Nuremberg, 2009, pp. 352–357. ISBN: 978-3-8007-3158-9.

[62] Simon Eicher et al. “4.5kV press pack IGBT designed for ruggedness and reliability”. In: *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.* Seattle: IEEE, 2004, pp. 1534–1539. ISBN: 0780384865. DOI: 10.1109/IAS.2004.1348674.

[63] Heng Wang et al. “The New High Reliable Press Pack IGBT for Modular Multilevel Converter in VSC-HVDC Applications”. In: *2020 4th International Conference on HVDC, HVDC 2020*. Ed. by IEEE. Xi’an, 2020, pp. 14–19. ISBN: 9781728175935. DOI: 10.1109/HVDC50696.2020.9292741.

[64] Liutauras Storasta et al. “The next generation 6500V BIGT HiPak modules”. In: *PCIM Europe* (2013), pp. 337–344.

[65] Regina Gao. “HVDC & FACTS - Development & Project Update (ABB)”. In: *EPRI Workshop*. Palo Alto, 2019.

[66] Tianyu Wei et al. "Experimental evaluation of IGCT converters with reduced di/dt limiting inductance". In: *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*. 2018. ISBN: 9781538611807. DOI: 10.1109/APEC.2018.8341248.

[67] Thomas Setz, Vasilis Kappatos, and Matthias Lüscher. *Applying IGCTs*. Tech. rep. Lenzburg: ABB Switzerland Ltd Semiconductors, 2016. URL: https://library.e.abb.com/public/bf8c3766e36244cc93dfaab1e92e6636/Applying%20IGCTs%7B%5C_%7D5SYA%202032-04-16-06-2016.pdf.

[68] Jan Vobecký et al. "Large Area Fast Recovery Diode with Very High SOA Capability for IGCT Applications". In: *PCIM Europe 2011*. Nuremberg, 2011, pp. 1–7.

[69] H. E. Gruening. "High performance low cost MVA inveters realised with Integrated Gate-Commutated Thyristors (IGCT)". In: *EPE*. Trondheim, 1997, pp. 1–5.

[70] Hervé Feral. "Modélisation des couplages électrothermo-fluidiques des composants en boîtier press-pack. Application à l'Integrated Gate Commutated Thyristor 4,5kV - 4kA". PhD thesis. Institut National Polytechnique de Toulouse, 2005, pp. 1–164.

[71] P.K. Steimer et al. "IGCT-a new emerging technology for high power, low cost inverters". In: *IAS '97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting*. Vol. 2. IEEE, 1997, pp. 1592–1599. ISBN: 0-7803-4067-1. DOI: 10.1109/IAS.1997.629064.

[72] H. Yamada et al. "GTO thyristor applications for HVDC transmission systems". In: *IEEE Transactions on Power Delivery* 5.3 (1990), pp. 1327–1335. ISSN: 0885-8977. DOI: 10.1109/61.57974.

[73] Hironobu Kon et al. "The 4500 V-750 A planar gate press pack IEGT". In: *Proceedings of the 10th International Symposium on Power Semiconductor Devices and ICs*. Kyoto: IEEE, 1998, pp. 81–84. DOI: 10.1109/ISPSD.1998.702638.

[74] Yoshimasa Sato. "Novel IEGT based Modular Multilevel Converter for New Hokkaido-Honshu HVDC Power Transmission". In: *Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. Vienna: IEEE, 2020, pp. 1–4. ISBN: 9781728148366. DOI: 10.1109/ISPSD46842.2020.9170200.

[75] Toshiba. "TOSHIBA IEGT & Application in VSC-HVDC". In: *AEIT HVDC Conference 2021*. 2021.

[76] Eugen Wiesner and Kenji Hataori. "3.3 kV Full SiC MOSFETs – Towards High-Performance Traction Inverters". In: *Bodo's Power Systems* (2018), pp. 22–25. URL: https://www.mitsubishichips.eu/wp-content/uploads/2018/11/Bodos-Power-Systems%7B%5C_%7D18-01%7B%5C_%7DMitsubishi-Electric-Semiconductor.pdf.

[77] Christina Dimarino et al. "10 kV, 120 A SiC MOSFET modules for a power electronics building block (PEBB)". In: *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*. IEEE, 2014, pp. 55–58. ISBN: 9781479954933. DOI: 10.1109/WiPDA.2014.6964623.

[78] Sachin Madhusoodhanan et al. "Comparative evaluation of 15 kV SiC IGBT and 15 kV SiC MOSFET for 3-phase medium voltage high power grid connected converter applications". In: *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*. Milwaukee: IEEE, 2016, pp. 1–8. ISBN: 9781509007370. DOI: 10.1109/ECCE.2016.7854933.

[79] Biao Zhao et al. "A More Prospective Look at IGCT: Uncovering a Promising Choice for dc Grids". In: *IEEE Industrial Electronics Magazine* 12.3 (2018), pp. 6–18. ISSN: 1932-4529. DOI: 10.1109/MIE.2018.2855216.

[80] Michael J Rogers, Eric R Motto, and Mark Steiner. "Performance Comparison 300 A/1700 V Si IGBT of State-of-the-Art and SiC MOSFET Power Modules". In: *IEEE Power Electronics Magazine* 7.3 (2020), pp. 44–51. DOI: 10.1109/MPEL.2020.3011776.

[81] Joseph Fabre et al. "Characterization and Implementation of Resonant Isolated DC/DC Converters for Future MVdc Railway Electrification Systems". In: *IEEE Transactions on Transportation Electrification* 7.2 (2021), pp. 854–869. ISSN: 23327782. DOI: 10.1109/TTE.2020.3033659.

[82] Dimosthenis Peftitsis et al. "High-power modular multilevel converters with SiC JFETs". In: *IEEE Transactions on Power Electronics* 27.1 (2012), pp. 28–36. DOI: 10.1109/TPEL.2011.2155671.

[83] Thomas Lagier, Philippe Ladoux, and Piotr Dworakowski. “Potential of silicon carbide MOSFETs in the DC/DC converters for future HVDC offshore wind farms”. In: *IET High Voltage* 2.4 (2017), pp. 233–243. ISSN: 2397-7264. DOI: 10.1049/hve.2017.0070.

[84] Jacobs Keijo. “Silicon-Carbide-Based High-Voltage Submodules for HVDC Voltage-Source Converters”. PhD thesis. KTH Royal Institute of Technology, 2020. ISBN: 9789178736782.

[85] S. Ryu et al. “15 kV N-GTOs in 4H-SIC”. In: *Materials Science Forum*. Vol. 963. 2019, pp. 651–654. ISBN: 9783035713329. DOI: 10.4028/www.scientific.net/MSF.963.651.

[86] Rasmus Orndrup Nielsen et al. “Efficiency and cost comparison of Si IGBT and SiC JFET isolated DC/DC converters”. In: *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*. 2013, pp. 695–699. ISBN: 9781479902248. DOI: 10.1109/IECON.2013.6699219.

[87] Amol Deshpande and Fang Luo. “Practical Design Considerations for a Si IGBT + SiC MOSFET Hybrid Switch: Parasitic Interconnect Influences, Cost, and Current Ratio Optimization”. In: *IEEE Transactions on Power Electronics* 34.1 (2018), pp. 724–737. ISSN: 08858993. DOI: 10.1109/TPEL.2018.2827989.

[88] Peter Steimer et al. “IGCT technology baseline and future opportunities”. In: *2001 IEEE/PES Transmission and Distribution Conference and Exposition*. Atlanta: IEEE, 2001, pp. 1182–1187. ISBN: VO - 2. DOI: 10.1109/TDC.2001.971429.

[89] Steffen Bernet et al. “Design and Characteristics of 10 kV IGCTs”. In: *EPE 2003*. Toulouse, 2003, pp. 1–10. ISBN: 9075815077.

[90] Tobias Wikstrom et al. “The 150 mm RC-IGCT: A device for the highest power requirements”. In: *Proceedings of the International Symposium on Power Semiconductor Devices and ICs* (2014), pp. 91–94. ISSN: 10636854. DOI: 10.1109/ISPSD.2014.6855983.

[91] Martin Arnold et al. “High Temperature Operation of HPT + IGCTs”. In: *PCIM Europe 2011*. Nuremberg, 2011, pp. 1–6. ISBN: 9783800733446.

[92] J. Vobecky et al. “Local lifetime control for enhanced ruggedness of HVDC thyristors”. In: *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs*. IEEE, 2018, pp. 156–159. ISBN: 9781538629260. DOI: 10.1109/ISPSD.2018.8393626.

[93] Chaoqun Xu et al. “Full-Time Junction Temperature Extraction of IGCT Based on Electrothermal Model and TSEP Method for High-Power Applications”. In: *IEEE Transactions on Industrial Electronics* 68.1 (2021), pp. 47–58. ISSN: 15579948. DOI: 10.1109/TIE.2019.2962423.

[94] S Linder et al. “A new range of reverse conducting gate-commutated thyristors for high voltage, medium power applications”. In: *Proceedings of the 7th European Conference on Power Electronics and Applications (EPE)*. Trondheim, 1997, pp. 1–8.

[95] Dragan Stamenkovic et al. “Soft Switching Behavior of IGCT for Resonant Conversion”. In: *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)* (2019), pp. 2714–2719. DOI: 10.1109/APEC.2019.8722039.

[96] Felix Mathis et al. *Applying IGCT gate units*. Tech. rep. Lenzburg: ABB Switzerland Ltd. Semiconductors, 2017, pp. 1–14. URL: https://search.abb.com/library/Download.aspx?DocumentID=5SYA2031%7B%5C&%7DLanguageCode=en%7B%5C&%7DDocumentPartId=%7B%5C&%7DAction=Launch.

[97] Tobias Thurnherr et al. “Static frequency converters for railway power supply based on IGCT high power semiconductors”. In: *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management* (2020), pp. 1–8.

[98] Bjorn Odegard et al. “Rugged MMC converter cell for high power applications”. In: *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*. Karlsruhe: IEEE, Sept. 2016, pp. 1–10. ISBN: 978-9-0758-1524-5. DOI: 10.1109/EPE.2016.7695417.

[99] Zilang Hu et al. “An Aging-Degree Evaluation Method for IGBT Bond Wire with Online Multivariate Monitoring”. In: *Energies* 12.20 (2019). ISSN: 19961073. DOI: 10.3390/en12203962.

[100] Sanchit Singh. *IGCT Transient Analysis and Clamp Circuit Design for VSC valves*. Tech. rep. Stockholm: Royal Institute of Technology (KTH), 2012. URL: https://www.diva-portal.org/smash/get/diva2:583522/FULLTEXT01.pdf.

[101] Tobias Wikstroem et al. "94 mm Reverse-Conducting IGCT for High Power and Low Losses Applications". In: *PCIM Asia 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Shanghai: VDE, 2017. ISBN: 9783800744299.

[102] Umamaheswara Vemulapati et al. "Recent advancements in IGCT technologies for high power electronics applications". In: *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*. 2015, pp. 1–10. ISBN: 9789075815221. DOI: 10.1109/EPE.2015.7311740.

[103] Thomas Stiasny et al. "Experimental results of a Large Area (91mm) 4.5kV "Bi-mode Gate Commutated Thyristor" (BGCT)". In: *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Nuremberg: VDE, 2016, pp. 917–923. ISBN: 9783800741861.

[104] Bjoern Oedegard et al. *An Application-Specific Asymmetric IGCT*. Tech. rep. ABB Semiconductors AG, 2001.

[105] Björn Backlund et al. *Failure rates of IGCTs due to cosmic rays*. Tech. rep. Lenzburg: ABB Power Grids Semiconductors Ltd., 2014, pp. 1–5. URL: https://search.abb.com/library/Download.aspx?DocumentID=5SYA2046%7B%5C&%7DLanguageCode=en%7B%5C&%7DDocumentPartId=%7B%5C&%7DAction=Launch.

[106] Frans Dijkhuizen and Staffan Norrga. "Fault tolerant operation of power converter with cascaded cells". In: *EPE Journal* 23.1 (2013), pp. 21–26. DOI: 10.1080/09398368.2013.11463842.

[107] Bjorn Jacobson et al. "VSC-HVDC Transmission with Cascaded Two-Level Converters". In: *CIGRE* (2010).

[108] Siemens. *Fact Sheet - BorWin2 HVDC Platform*. 2015. URL: https://assets.new.siemens.com/siemens/assets/api/uuid:2c208787-94c1-42aa-a344-725ac2787dd4/factsheet-borwin2-en.pdf.

[109] Siemens. *Fact Sheet: BorWin3 grid connection system*. 2020. URL: https://assets.new.siemens.com/siemens/assets/api/uuid:dcc4289e-9325-4daf-9b29-f60e8ff3c194/Factsheet-BorWin3-en.pdf.

[110] Hitachi ABB Power Grids. *HVDC Light ® - The original VSC technology*. Tech. rep. 2020, pp. 1–16. URL: https://search.abb.com/library/Download.aspx?DocumentID=POW0027%7B%5C&%7DLanguageCode=en%7B%5C&%7DDocumentPartId=%7B%5C&%7DAction=Launch.

[111] Orestes Macchione. "HVDC & FACTS Projects Update (Siemens)". In: *ERPI*. Palo Alto, 2019.

[112] André Bodin. "HVDC Light ® - A Preferable Power Transmission System for Renewable Energies". In: *Proceedings of the 2011 3rd International Youth Conference on Energetics (IYCE)*. IEEE, 2011, pp. 1–4.

[113] Til Kristian Vrana and Sintef Energi. "Review of HVDC component ratings: XLPE cables and VSC converters". In: *2016 IEEE International Energy Conference (ENERGYCON)*. 2016, pp. 1–6. ISBN: 9781467384636. DOI: 10.1109/ENERGYCON.2016.7514045.

[114] N M Macleod et al. "Tres Amigas : an innovative HVDC link between three asynchronous AC networks". In: *SCB4 Colloquium 2011*. Paris: CIGRE, 2015, pp. 1–8.

[115] Urban Wijk, Jonas Lindgren, and Johan Winther. "Dolwin1 - Further Achievements in HVDC Offshore Connections". In: *EWEA Offshore 2013*. Frankfurt, 2013, pp. 1–6. URL: https://library.e.abb.com/public/0817901b2514978ec1257c3000435c3a/DolWin1%20further%20achievements%20in%20HVDC%20offshore%20connections.pdf.

[116] Siemens. *Fact Sheet - HelWin1 HVDC Platform*. 2015.

[117] Siemens. *Fact Sheet - SylWin1 HVDC Platform*. 2015.

[118] Siemens. *Fact Sheet - HelWin2 HVDC Platform*. 2015.

[119] Alfons Benzinger. *Siemens Energy delivers technology for seventh offshore wind farm connection in the North Sea*. 2020. URL: https://press.siemens-energy.com/global/en/pressrelease/siemens-energy-delivers-technology-seventh-offshore-wind-farm-connection-north-sea (visited on 06/09/2021).

[120] Magnus Callavik, Peter Lundberg, and Ola Hansson. *NORDLINK - Pioneering VSC-HVDC interconnector between Norway and Germany*. Tech. rep. March. ABB Power Systems, Grid Systems, 2015, pp. 1–6. URL: https://library.e.abb.com/public/aaa99cf7067cd258c1257e0d002c9a7b/Nordlink%20White%20Paper%20from%20ABB.pdf.

[121] Alireza Nami et al. "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities". In: *IEEE Transactions on Power Electronics* 30.1 (2015), pp. 18–36. ISSN: 08858993. DOI: 10.1109/TPEL.2014.2327641.

[122] Rainer Marquardt. "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-bus-applications". In: *The 2010 International Power Electronics Conference - ECCE ASIA*. Ed. by IEEE. Sapporo, 2010, pp. 502–507. ISBN: 9781424453955. DOI: 10.1109/IPEC.2010.5544594.

[123] Nicola Serbia. "Modular Multilevel Converters for HVDC power stations". PhD thesis. Institut National Polytechnique de Toulouse, 2014, pp. 1–152.

[124] Alireza Nami et al. "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVDC transmission systems". In: *2015 17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015*. Geneva, 2015, pp. 1–10. ISBN: 9789075815221. DOI: 10.1109/EPE.2015.7309391.

[125] T Jonsson et al. "Converter Technologies and Functional Requirements for Reliable and Economical HVDC Grid Design". In: *2013 CIGRE Canada Conference*. Calgary: CIGRE, 2013.

[126] Yeqi Wang and Rainer Marquardt. "Future HVDC-Grids employing Modular Multilevel Converters and Hybrid DC-Breakers". In: *15th European Conference on Power Electronics and Applications (EPE)*. Lille: IEEE, 2013, pp. 1–8. DOI: 10.1109/EPE.2013.6631861.

[127] B Jacobson et al. "HVDC with voltage source converters and extruded cables for up to +/-300 kV and 1000 MW". In: *CIGRE* (2006).

[128] Paolo Bordignon et al. "HV submodule technology based on press pack IGBT for largest scale VSC-HVDC application". In: *12th IET International Conference on AC and DC Power Transmission (ACDC 2016)*. Beijing: IET, 2016, pp. 1–6. DOI: 10.1049/cp.2016.0397.

[129] Paolo Bordignon et al. "Modular multilevel converter in HVDC systems under fault conditions". In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. Lille: IEEE, 2013, pp. 1–10. ISBN: 9781479901166. DOI: 10.1109/EPE.2013.6634467.

[130] Huifeng Chen et al. "Design and testing of the World's first single-level press-pack IGBT based submodule for MMC VSC HVDC applications". In: *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*. Montreal: IEEE, 2015, pp. 3359–3366. ISBN: 9781467371506. DOI: 10.1109/ECCE.2015.7310134.

[131] Jiapeng Liu et al. "A Novel Controlled Punch-through IGCT for Modular Multilevel Converter with Over- Voltage Bypass Function". In: *IEEE Transactions on Power Electronics* 36.7 (2021), pp. 8280–8290. DOI: 10.1109/TPEL.2020.3046679.

[132] Kihyun Lee and Yongsug Suh. "Flyback-type di/dt Snubber for 10kV IGCT in MV Wind Turbines". In: *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*. Pittsburgh: IEEE, 2014, pp. 4591–4598. ISBN: 9781479956982. DOI: 10.1109/ECCE.2014.6954029.

[133] Siamak Shirmohammadi and Yongsug Suh. "Cascaded Snubber Scheme using Flyback Type Transformer for 10kV IGCT Applications". In: *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*. Busan: IEEE, 2019, pp. 1688–1695. DOI: 10.23919/ICPE2019-ECCEAsia42246.2019.8797360.

[134] R. W. De Doncker and J. P. Lyons. "The auxiliary resonant commutated pole converter". In: *Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting*. Vol. 2. Seattle: IEEE, 1990, pp. 1228–1235. ISBN: 0879425539. DOI: 10.1109/IAS.1990.152341.

[135] Nils Soltau et al. "Ensuring soft-switching operation of a three-phase dual-active bridge DC-DC converter applying an auxiliary resonant-commutated pole". In: *2014 16th European Conference on Power Electronics and Applications*. Lappeenranta: IEEE, 2014, pp. 1–10. ISBN: 9781479930159. DOI: 10.1109/EPE.2014.6910857.

[136] Johannes Voss, Jochen Henn, and Rik W. De Doncker. "Control Techniques of the Auxiliary-Resonant Commutated Pole With Special Regards on the Dual-Active Bridge DC-DC Converter". In: *CPSS Transactions on Power Electronics and Applications* 3.4 (2018), pp. 352–361. DOI: 10.24295/CPSSTPEA.2018.00034.

[137] Steffen Bernet and Matthias Lüscher. "IGCTs in Soft Switching Power Converters". In: *EPE*. Lausanne, 1999, pp. 1–11.

[138] Arman Hassanpoor et al. "Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application". In: *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*. Montreal: IEEE, 2012, pp. 388–393. ISBN: 9781467324212. DOI: 10.1109/IECON.2012.6388789.

[139] Kalle Ilves et al. "Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor voltages". In: *IEEE Transactions on Power Electronics* 30.1 (2015), pp. 440–449. ISSN: 08858993. DOI: 10.1109/TPEL.2014.2308018.

[140] Arman Hassanpoor et al. "Tolerance Band Modulation Methods for Modular Multilevel Converters". In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. Lille: IEEE, 2013, pp. 1–10. DOI: 10.1109/EPE.2013.6632010.

[141] Qingrui Tu, Zheng Xu, and Lie Xu. "Reduced Switching-frequency modulation and circulating current suppression for modular multilevel converters". In: *IEEE Transactions on Power Delivery* 26.3 (2011), pp. 2009–2017. ISSN: 08858977. DOI: 10.1109/TPWRD.2011.2115258.

[142] Minyuan Guan, Zheng Xu, and Hairong Chen. "Control and modulation strategies for modular multilevel converter based HVDC system". In: *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*. Melbourne: IEEE, 2011, pp. 849–854. ISBN: 978-1-61284-972-0. DOI: 10.1109/IECON.2011.6119421.

[143] Marcin Zygmanowski, Boguslaw Grzesik, and Radoslaw Nalepa. "Capacitance and inductance selection of the modular multilevel converter". In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. Lille: IEEE, 2013, pp. 1–10. ISBN: 9781479901166. DOI: 10.1109/EPE.2013.6634446.

[144] Steffen Rohner et al. "Analysis and Simulation of a 6 kV, 6 MVA Modular Multilevel Converter". In: *2009 35th Annual Conference of IEEE Industrial Electronics*. IEEE, 2009, pp. 225–230. ISBN: 978-1-4244-4648-3. DOI: 10.1109/IECON.2009.5414775.

[145] Kalle Ilves et al. "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters". In: *IEEE Transactions on Power Electronics* 27.1 (2012), pp. 57–68. ISSN: 08858993. DOI: 10.1109/TPEL.2011.2159809.

[146] Qingrui Tu et al. "Parameter design principle of the arm inductor in modular multilevel converter based HVDC". In: *2010 International Conference on Power System Technology*. Hangzhou: IEEE, 2010, pp. 1–6. ISBN: 9781424459407. DOI: 10.1109/POWERCON.2010.5666416.

[147] Philipp Ruffing et al. "Fault current control methods for multi-terminal DC systems based on fault blocking converters". In: *The Journal of Engineering* 2018.15 (2018), pp. 871–875. DOI: 10.1049/joe.2018.0228.

[148] Tim Augustin et al. "Transient behaviour of VSC-HVDC links with DC breakers under faults". In: *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*. Warsaw: IEEE, 2017, pp. 1–10. ISBN: 978-90-75815-27-6. DOI: 10.23919/EPE17ECCEEurope.2017.8099248.

[149] Umamaheswara Reddy Vemulapati et al. "10 kV RC-IGCT and Fast Recovery Diode : with an Improved Technology Trade-off Performance". In: *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Online: VDE, 2021, pp. 1–6. ISBN: 9783800755158.

[150] Rainer Marquardt. "Modular Multilevel Converter topologies with DC-Short circuit current limitation". In: *8th International Conference on Power Electronics - ECCE Asia*. Jeju: IEEE, 2011, pp. 1425–1431. ISBN: 9781612849560. DOI: 10.1109/ICPE.2011.5944451.

[151] Y Jiang-Häfner and M. Manchen. "Stability Enhancement and Blackout Prevention by VSC Based HVDC". In: *CIGRE*. Bologna, 2011.

[152] Kenichiro Sano and Masahiro Takasaki. "A Surgeless Solid-State DC Circuit Breaker for Voltage-Source-Converter-Based HVDC Systems". In: *IEEE Transactions on Industry Applications* 50.4 (2014), pp. 2690–2699. ISSN: 0093-9994. DOI: 10.1109/TIA.2013.2293819.

[153] Dragan Jovcic and Bin Wu. "Fast fault current interruption on high-power DC networks". In: *IEEE PES General Meeting*. Minneapolis: IEEE, 2010, pp. 1–6. ISBN: 978-1-4244-6549-1. DOI: 10.1109/PES.2010.5589953.

[154] Jared Candelaria and Jae-Do Park. "VSC-HVDC system protection: A review of current methods". In: *2011 IEEE/PES Power Systems Conference and Exposition*. Phoenix: IEEE, 2011, pp. 1–7. ISBN: 978-1-61284-789-4. DOI: 10.1109/PSCE.2011.5772604.

[155] J.-M. Meyer and A. Rufer. "A DC Hybrid Circuit Breaker With Ultra-Fast Contact Opening and Integrated Gate-Commutated Thyristors (IGCTs)". In: *IEEE Transactions on Power Delivery* 21.2 (Apr. 2006), pp. 646–651. ISSN: 0885-8977. DOI: 10.1109/TPWRD.2006.870981.

[156] Mian Wang et al. "A Review on AC and DC Protection Equipment and Technologies : Towards Multivendor Solution". In: *Proc. Cigre 2017 Canada*. Winnipeg, 2017, pp. 1–11.

[157] Anshuman Shukla and Georgios D. Demetriades. "A Survey on Hybrid Circuit-Breaker Topologies". In: *IEEE Transactions on Power Delivery* 30.2 (Apr. 2015), pp. 627–641. ISSN: 08858977. DOI: 10.1109/TPWRD.2014.2331696.

[158] W. Leterme et al. "Classification of Fault Clearing Strategies for HVDC Grids". In: *CIGRE*. Lund, 2015, pp. 1–10.

[159] Volker Hinrichsen. *Metal-Oxide Surge Arresters in High-Voltage Power Systems*. Tech. rep. Berlin: Siemens AG, 2012, pp. 1–128. URL: https://assets.siemens-energy.com/siemens/assets/api/uuid:2ded5619-b9b1-4a28-ae11-d0742992f5da/e50001-g630-h197-x-4a00-ableiterhandbuch-teil-1-a4.pdf.

[160] Willem Leterme, Jef Beerten, and Dirk Van Hertem. "Nonunit protection of HVDC grids with inductive DC cable termination". In: *IEEE Transactions on Power Delivery* 31.2 (2016), pp. 820–828. ISSN: 08858977. DOI: 10.1109/TPWRD.2015.2422145.

[161] Salvatore D'Arco, Jon Are Suul, and Jef Beerten. "Analysis of accuracy versus model order for frequency-dependent Pi-model of HVDC cables". In: *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*. Trondheim: IEEE, 2016, pp. 1–8. ISBN: 9781509018154. DOI: 10.1109/COMPEL.2016.7556700.

[162] Julian Andres Suarez Diaz. "Étude et modélisation des interactions électriques entre les engins et les installations fixes de traction électrique 25kV/50Hz". PhD thesis. Institut National Polytechnique de Toulouse, 2014, pp. 1–143.

[163] Hermann W. Dommel. "Digital Computer Solution of Electromagnetic Transients in Single-and Multiphase Networks". In: *IEEE Transactions on Power Apparatus and Systems* PAS-88.4 (1969), pp. 388–399. DOI: 10.1109/TPAS.1969.292459.

[164] Matthias K. Bucher and Christian M. Franck. "Contribution of fault current sources in multiterminal HVDC cable networks". In: *IEEE Transactions on Power Delivery* 28.3 (2013), pp. 1796–1803. ISSN: 08858977. DOI: 10.1109/TPWRD.2013.2260359.

[165] P Bordignon et al. "Effects of the 2nd order harmonic leg current in a MMC converter". In: *EPE*. Lappeenranta: IEEE, 2014, pp. 1–10. DOI: 10.1109/EPE.2014.6911029.

[166] Stefan P. Engel and Rik W. De Doncker. "Control of the Modular Multi-Level Converter for minimized cell capacitance". In: *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*. Birmingham, 2011, pp. 1–10. ISBN: 9781612841670.

[167] Ming Zhang et al. "Circulating Harmonic Current Elimination of a CPS-PWM-Based Modular Multilevel Converter With a Plug-In Repetitive Controller". In: *IEEE Transactions on Power Electronics* 29.4 (2014), pp. 2083–2097. ISSN: 0885-8993. DOI: 10.1109/TPEL.2013.2269140.

[168] Kalle Ilves et al. "Circulating current control in modular multilevel converters with fundamental switching frequency". In: *Proceedings of The 7th International Power Electronics and Motion Control Conference*. Harbin: IEEE, June 2012, pp. 249–256. ISBN: 978-1-4577-2085-7. DOI: 10.1109/IPEMC.2012.6258844.

[169] Hirofumi Akagi, Shigenori Inoue, and Tsurugi Yoshii. "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration". In: *IEEE Transactions on Industry Applications* 43.4 (2007), pp. 1041–1049. DOI: 10.1109/TIA.2007.900487.

[170] Lennart Harnefors et al. "Dynamic Analysis of Modular Multilevel Converters". In: *IEEE Transactions on Industrial Electronics* 60.7 (2013), pp. 2526–2537. ISSN: 0278-0046. DOI: 10.1109/TIE.2012.2194974.

[171] Wei Huang Huang et al. "Stability analysis of Modular Multilevel Converter using Nearest Level Modulation". In: *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*. Florence: IEEE, 2016, pp. 2582–2587. ISBN: 9781509034741. DOI: 10.1109/IECON.2016.7793018.

[172] Thomas LAGIER. "Convertisseurs continu-continu pour les réseaux d'électricité à courant continu". PhD thesis. Institut National Polytechnique de Toulouse, 2010, pp. 1–234.

[173] Leopoldo G. Franquelo et al. "The age of multilevel converters arrives". In: *IEEE Industrial Electronics Magazine* 2.2 (2008), pp. 28–39. ISSN: 19324529. DOI: 10.1109/MIE.2008.923519.

[174] Marcelo A. Perez et al. "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters". In: *IEEE Transactions on Power Electronics* 30.1 (2015), pp. 4–17. DOI: 10.1109/TPEL.2014.2310127.

[175] Fainan Hassan, Will Crookes, and Roger Critchley. "Optimized stair-case modulation for modular grid connected converters". In: *2010 IEEE International Symposium on Industrial Electronics*. IEEE, 2010, pp. 3820–3825. ISBN: 978-1-4244-6390-9. DOI: 10.1109/ISIE.2010.5637498.

[176] Qiang Li, Zhiyuan He, and Guangfu Tang. "Investigation of the Harmonic Optimization Approaches in the New Modular Multilevel Converters". In: *2010 Asia-Pacific Power and Energy Engineering Conference*. Chengdu: IEEE, 2010, pp. 1–6. ISBN: 978-1-4244-4812-8. DOI: 10.1109/APPEEC.2010.5449299.

[177] José Rodríguez, Jih Sheng Lai, and Fang Zheng Peng. "Multilevel inverters: a survey of topologies, controls, and applications". In: *IEEE Transactions on Industrial Electronics* 49.4 (2002), pp. 724–738. ISSN: 02780046. DOI: 10.1109/TIE.2002.801052.

[178] Kalle Ilves et al. "Analysis and Operation of Modular Multilevel Converters With Phase-Shifted Carrier PWM". In: *IEEE Transactions on Power Electronics* 30.1 (2015), pp. 268–283. ISSN: 08858993. DOI: 10.1109/TPEL.2014.2321049.

[179] Qingrui Tu and Zheng Xu. "Impact of sampling frequency on harmonic distortion for modular multilevel converter". In: *IEEE Transactions on Power Delivery* 26.1 (2011), pp. 298–306. ISSN: 0885-8977. DOI: 10.1109/TPWRD.2010.2078837.

[180] Arman Hassanpoor et al. "Optimization-based cell selection method for grid-connected modular multilevel converters". In: *IEEE Transactions on Power Electronics* 31.4 (2016), pp. 2780–2790. ISSN: 0885-8993. DOI: 10.1109/TPEL.2015.2448573.

[181] Arman Hassanpoor, Alireza Nami, and Staffan Norrga. "Tolerance Band Adaptation Method for Dynamic Operation of Grid-Connected Modular Multilevel Converters". In: *IEEE Transactions on Power Electronics* 31.12 (2016), pp. 8172–8181. ISSN: 0885-8993. DOI: 10.1109/TPEL.2016.2521480.

[182] Sascha Kubera, Rodrigo Alvarez, and Jorg Dorn. "Control of switching frequency for modular multilevel converters by a variable hysteresis band modulation". In: *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*. Karlsruhe: IEEE, 2016, pp. 1–7. ISBN: 9789075815245. DOI: 10.1109/EPE.2016.7695697.

[183] Kalle Ilves et al. "A new modulation method for the modular multilevel converter allowing fundamental switching frequency". In: *IEEE Transactions on Power Electronics* 27.8 (2012), pp. 3482–3494. ISSN: 0885-8993. DOI: 10.1109/TPEL.2012.2185832.

[184] Davin Guedon et al. "Use of IGCTs in Modular Multilevel Converters for HVDC Link: Influence of the Modulation Method on the Efficiency". In: *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)* (2019), pp. 773–779. DOI: 10.23919/ICPE2019-ECCEAsia42246.2019.8797134.

[185] Phil S. Jones and Colin C. Davidson. "Calculation of power losses for MMC-based VSC HVDC stations". In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. Lille: IEEE, 2013, pp. 1–10. ISBN: 9781479901166. DOI: 10.1109/EPE.2013.6631955.

[186] Martin Buschendorf, Jens Weber, and Steffen Bernet. "Comparison of IGCT and IGBT for the use in the modular multilevel converter for HVDC applications". In: *International Multi-Conference on Systems, Signals & Devices*. Chemnitz: IEEE, 2012, pp. 1–6. ISBN: 9781467315906. DOI: 10.1109/SSD.2012.6198118.

[187] Arman Hassanpoor, Staffan Norrga, and Alireza Nami. "Loss evaluation for modular multilevel converters with different switching strategies". In: *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*. Seoul: IEEE, 2015, pp. 1558–1563. ISBN: 978-8-9570-8254-6. DOI: 10.1109/ICPE.2015.7167984.

[188] Tomas Modeer, Hans-Peter Nee, and Staffan Norrga. "Loss comparison of different submodule implementations for modular multilevel converters in HVDC applications". In: *EPE Journal (European Power Electronics and Drives Journal)* 22.3 (2012), pp. 32–38. DOI: 10.1080/09398368.2012.11463829.

[189] Peter K. Steimer, David Weiss, and Bjorn Odegard. "Robust, Low-Loss RCIGCT Technology and MV Applications". In: *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*. Busan: IEEE, 2019, pp. 1703–1708. ISBN: 9788957083130. DOI: 10.23919/ICPE2019-ECCEAsia42246.2019.8796873.

[190] Davin Guédon et al. "IGCTs in HVDC Systems : Analysis and Assessment of Losses Modular multilevel converter". In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. Nuremberg: VDE, 2019, pp. 1–8. ISBN: 9783800749386.

[191] Biao Zhao et al. "Practical Analytical Model and Comprehensive Comparison of Power Loss Performance for Various MMCs based on IGCT in HVDC Application". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 7.2 (2018), pp. 1071–1083. ISSN: 2168-6777. DOI: 10.1109/JESTPE.2018.2871191.

[192] Alan Courtay. "MAST Power Diode and Thyristor Models Including Automatic Parameter Extraction". In: *SABER User Group Meeting*. Brighton, 1995, pp. 1–10. URL: https://cds.cern.ch/record/291468/files/cn-95-016.pdf.

[193] J.F. Manwell, J.G. McGowan, and A.L. Rogers. *Wind Energy Explained: Theory, Design and Application (Second Edition)*. John Wiley & Sons, 2009, pp. 1–705. ISBN: 9780470015001.

[194] Eugene C. Morgan et al. "Probability distributions for offshore wind speeds". In: *Energy Conversion and Management* 52.1 (2011), pp. 15–26. ISSN: 01968904. DOI: 10.1016/j.enconman.2010.06.015.

[195] B. H. Bulder et al. *Quick scan wind farm efficiencies of the Borssele location*. Tech. rep. Petten: ECN, 2014, pp. 1–34. URL: https://publicaties.ecn.nl/PdfFetch.aspx?nr=ECN-E--14-050.

[196] GE. *GE's Haliade 150-6MW*. 2016. URL: https://www.ge.com/renewableenergy/sites/default/files/2020-01/wind-offshore-haliade-wind-turbine.pdf (visited on 10/22/2019).

[197] Alhassan Ali Teyabeen, Fathi Rajab Akkari, and Ali Elseddig Jwaid. "Power Curve Modelling for Wind Turbines". In: *2017 UKSim-AMSS 19th International Conference on Computer Modelling & Simulation (UKSim)*. Cambridge: IEEE, 2018, pp. 179–184. ISBN: 9781538627358. DOI: 10.1109/UKSim.2017.30.

[198] Thomas Ackermann. *Wind Power in Power Systems*. John Wiley. John Wiley & Sons, 2005, pp. 1–745. ISBN: 9780470974162.

[199] Munaf Rahimo et al. "Optimization of high voltage IGCTs towards 1V on-state losses". In: *PCIM Europe 2013* (2013), pp. 613–620. ISSN: 21913358.

[200] François Forest et al. "Use of opposition method in the test of high-power electronic converters". In: *IEEE Transactions on Industrial Electronics* 53.2 (2006), pp. 530–541. ISSN: 02780046. DOI: 10.1109/TIE.2006.870711.

[201] Evgeny Tsyplakov, Toni Schweizer, and Björn Backlund. *Mechanical clamping of press-pack high power semiconductors*. Tech. rep. ABB Switzerland Ltd Semiconductors, 2016. URL: https://library.e.abb.com/public/541a627680f848b48ff4547b226df547/Mechanical%20clamping%20of%20press-pack%7B%5C_%7D%205SYA%202036-04.pdf.

Appendix A

Analytic expressions of the electrical waveforms

A.1 Arm-voltage $v_u(t)$

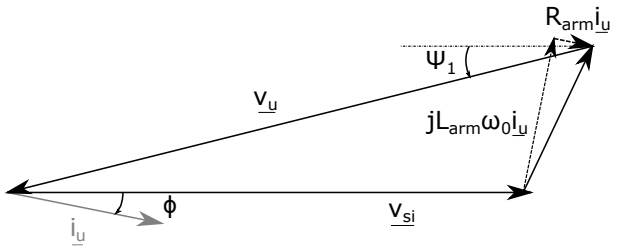


Figure A.1: Fresnel diagram for the upper arm of a given phase

The upper arm-current has the well-known expression:

$$\boxed{i_u(t) = \frac{I_{DC}}{3} + \frac{I_s}{\sqrt{2}}\sin(\omega_0 t - \varphi)} \tag{A.1}$$

In this equation the DC link current I_{DC} is unknown at this stage, it is expressed later. Considering the voltage drop due the inductor as well as its resistance as presented in Figure A.1, the upper arm-voltage of a given phase $v_u(t)$ has the expression:

$$v_u(t) = \frac{V_{DC}}{2} - R_{arm}\frac{I_{DC}}{3} - v_{u1}\sin(\omega_0 t + \psi_1) \text{ with :} \tag{A.2}$$

$$\begin{cases} v_{u1}^2 = \left(m_a\frac{V_{DC}}{2}\right)^2 + \frac{I_s^2}{2}\left((R_{arm}^2 + (L_{arm}\omega_0)^2) + m_a V_{DC}\frac{I_s}{\sqrt{2}}\left(R_{arm}\cos(\varphi) + L_{arm}\omega_0\sin(\varphi)\right)\right. \\ \cos(\psi_1) = \frac{1}{v_{u1}}\left(m_a\frac{V_{DC}}{2} + \frac{I_s}{2}(R_{arm}\cos(\varphi) + L_{arm}\omega_0\sin(\varphi))\right) \\ \sin(\psi_1) = \frac{I_s}{\sqrt{2}v_{u1}}\left(L_{arm}\omega_0\cos(\varphi) - R_{arm}\sin(\varphi)\right) \end{cases} \tag{A.3}$$

The second-order harmonic of $v_u(t)$ is neglected because a CCSC is used as described in 2.4.1; otherwise another modelling approach would have been necessary as the one proposed in [123]. v_{u1} evolves with the phase angle φ because of the natural voltage drop in the arm-inductor L, it defines the P-Q plane of the converter: when v_{u1} increases $v_u(t)$ may reach either 0 or $v_{cu}(t)$, which corresponds to the converter's limit of operation.

A.2 DC link current I_{DC}

It is assumed that the AC grid currents are controlled, then the DC link current is slightly higher than expected to counterbalance the power losses in the converter, modelled by the arm-resistances R_{arm}:

$$V_{DC}I_{DC} = \sqrt{3}U_s I_s \cos(\varphi) + 6R_{arm}I_u^2 \tag{A.4}$$

It leads to the new expression of I_{DC}:

$$I_{DC} = \frac{3V_{DC}}{4R_{arm}}\left(1 - \sqrt{1 - \frac{8R_{arm}P}{3V_{DC}^2}\left(1 + \frac{R_{arm}P}{3V_{DC}^2}\left(\frac{2}{m_a\cos(\varphi)}\right)^2\right)}\right) \tag{A.5}$$

(A.5) is replaced into (A.1) to have the final expression of the arm-current.

A.3 Arm-energy $E_{cu}(t)$

The energy variation over a grid period can be obtained from the expressions of $v_u(t)$ and $i_u(t)$:

$$P_{cu}(\theta) = v_u(t)i_u(t) \tag{A.6}$$

where $P_u(t)$ is the instantaneous power provided by the arm; i.e. the N capacitors of the sub-modules. As a consequence, the energy variation over a grid period is:

$$\Delta E_{cu}(t) = -\frac{V_{DC}I_s}{2\sqrt{2}\omega_0}\cos(\theta-\varphi) + \frac{v_{u1}I_{DC}}{3\omega_0}\cos(\omega_0 t + \psi_1) + \frac{v_{u1}I_s}{4\sqrt{2}\omega_0}\sin(2\omega_0 t + \psi_1 - \varphi) \tag{A.7}$$

Then this expression can be rewritten:

$$E_{cu}(t) = e_{cu0} - e_{cu1}sin(\theta+\beta_1) + \underbrace{\frac{v_{u1}I_s}{4\sqrt{2}\omega_0}}_{e_{cu2}}\sin(2\omega_0 t + \underbrace{\psi_1 - \varphi}_{\beta_2}) \text{ with:} \tag{A.8}$$

$$\begin{cases} e_{cu1}^2 = \left(\left(\frac{V_{DC}}{2} - R_a\frac{I_{DC}}{3}\right)\frac{I_s}{\sqrt{2}\omega_0}\right)^2 + \left(v_{u1}\frac{I_{DC}}{3\omega_0}\right)^2 - \\ \left(\frac{V_{DC}}{2} - R_{arm}\frac{I_{DC}}{3}\right)\frac{2I_s v_{u1}I_{DC}}{3\sqrt{2}\omega_0^2}\cos(\varphi+\psi_1) \\ \\ \cos(\beta_1) = \frac{1}{e_{cu1}}\left(\left(\frac{V_{DC}}{2} - R_{arm}\frac{I_{DC}}{3}\right)\frac{I_s}{\sqrt{2}\omega_0}\sin(\varphi) + v_{u1}\frac{I_{DC}}{3\omega_0}\sin(\psi_1)\right) \\ \sin(\beta_1) = \frac{1}{e_{cu1}}\left(\left(\frac{V_{DC}}{2} - R_{arm}\frac{I_{DC}}{3}\right)\frac{I_s}{\sqrt{2}\omega_0}\cos(\varphi) - v_{u1}\frac{I_{DC}}{3\omega_0}\cos(\psi_1)\right) \end{cases} \tag{A.9}$$

The arm-energy can be also be expressed from the sum capacitor-voltage $v_{cu}(t)$:

$$E_{cu}(t) = \frac{1}{2}C_e v_{cu}^2(t),\ C_e = \frac{C}{N} \tag{A.10}$$

$v_{cu}(t)$ is decomposed as:

$$v_{cu}(t) = v_{cu0} - v_{cu1}\sin(\omega_0 t + \beta_1') - v_{cu2}\sin(2\omega_0 t + \beta_2') \tag{A.11}$$

By replacing (A.11) into (A.10), the following equations are obtained by identification with (A.8):

$$\begin{cases} e_{cu0} \approx \frac{1}{2}C_e\left(v_{cu0}^2 + \frac{1}{2}v_{cu1}^2\right) \\ e_{cu1}\sin(\theta+\beta_1) = C_e v_{cu0}v_{cu1}\sin(\theta+\beta_1') - C_e v_{cu1}v_{cu2}\cos(\theta+\beta_2'-\beta_1') \end{cases} \tag{A.12}$$

The product $v_{cu0}v_{cu1}$ is much greater than $v_{cu1}v_{cu2}$, so

$$\begin{array}{l} e_{cu1}\sin(\theta+\beta_1) \approx C_e v_{cu0}v_{cu1}\sin(\theta+\beta_1') \text{ and } \beta_1 \approx \beta_1' \\ \Rightarrow \boxed{e_{cu1} \approx C_e v_{cu0}v_{cu1}} \end{array} \tag{A.13}$$

A.4 Average sum capacitor-voltage v_{cu0}

The relation between the reference arm-voltage $v^*_u(t)$, the sum capacitor-voltage $v_{cu}(t)$ and the arm-voltage $v_{cu}(t)$ is:

$$v_u(t) = v_{cu}(t)\frac{v_u^*(t)}{V_{DC}} \tag{A.14}$$

$v_u(t)$ is known from Eq. (A.2). $v_{cu}(t)$ in expressed in Eq. (A.11), the terms being partly identified in Eq. (A.12) and Eq. (A.13), however the DC component is still unknown. $v^*_u(t)$ can be approximated as:

$$v_u^*(t) = \frac{V_{DC}}{2} - v_{u1}^* \sin(\omega_0 t + \delta_1) \tag{A.15}$$

It has to be noticed that $v^*_u(t)$ necessarily contains a second-order harmonic but it is neglected. By replacing (A.15) into (A.14):

$$v_u(t) = \frac{1}{V_{DC}}\left(v_{cu0} - v_{cu1}\sin(\theta+\beta_1) - v_{cu2}\sin(2\theta+\beta_2')\right)\left(\frac{V_{DC}}{2} - v_{u1}^*\sin(\theta+\delta_1)\right) \tag{A.16}$$

Using the expression (A.2) of $v_u(t)$:

$$\begin{cases} \frac{V_{DC}}{2} - R_a\frac{I_{DC}}{3} = \frac{1}{2}v_{cu0} + \frac{v_{u1}^* v_{cu1}}{2V_{DC}}\cos(\delta_1 - \beta_1) \\ \\ v_{u1}sin(\theta+\psi_1) = \frac{v_{cu0}v_{u1}^*}{V_{DC}}\sin(\theta+\delta_1) + \frac{1}{2}v_{cu1}\sin(\theta+\beta_1) \end{cases} \tag{A.17}$$

so, from the second equation of (A.17):

$$\begin{cases} \cos(\delta_1) = \frac{V_{DC}}{v_{cu0}v_{u1}^*}\left(v_{u1}\cos(\psi_1) - \frac{1}{2}v_{cu1}\cos(\beta_1)\right) \\ \\ \sin(\delta_1) = \frac{V_{DC}}{v_{cu0}v_{u1}^*}\left(v_{u1}\sin(\psi_1) - \frac{1}{2}v_{cu1}\sin(\beta_1)\right) \end{cases} \tag{A.18}$$

and from the first equation in Eq. (A.17):

$$\frac{V_{DC}}{2} - R_a\frac{I_{DC}}{3} = \frac{1}{2}v_{cu0} + \frac{v_{u1}^* v_{cu1}}{2V_{DC}}\left(\cos(\delta_1)\cos(\beta_1) + \sin(\delta_1)\sin(\beta_1)\right) \tag{A.19}$$

So, it is possible to replace $\cos(\delta_1)$ and $\sin(\delta_1)$ by the expressions of Eq. (A.18), yielding after simplification:

$$\frac{1}{2}v_{cu0}^2 - \left(\frac{V_{DC}}{2} - R_a\frac{I_{DC}}{3}\right)v_{cu0} + \frac{v_{cu1}v_{u1}}{2}\cos(\psi_1 - \beta_1) - \frac{1}{4}v_{cu1}^2 = 0 \tag{A.20}$$

The term k_{cu1} is introduced into (A.13) to approximate v_{cu1}:

$$v_{cu1} = \underbrace{\frac{e_{cu1}}{C_e V_{DC}}}_{k_{cu1}}\frac{1}{\frac{v_{cu0}}{V_{DC}}} \approx k_{cu1}\left(2 - \frac{v_{cu0}}{V_{DC}}\right) \tag{A.21}$$

Thus, by replacing into (A.20):

$$\left(\frac{1}{2} - \frac{k_{cu1}^2}{4V_{DC}^2}\right)v_{cu0}^2 + \left(-\frac{V_{DC}}{2} + R_{arm}\frac{I_{DC}}{3} + \frac{k_{cu1}^2}{V_{DC}} - \frac{k_{cu1}v_{u1}}{2V_{DC}}\cos(\psi_1 - \beta_1)\right)v_{cu0} + \left(k_{cu1}v_{u1}\cos(\psi_1 - \beta_1) - k_{cu1}^2\right) = 0 \tag{A.22}$$

Therefore:

$$\Delta = \left(-\frac{V_{DC}}{2} + R_{arm}\frac{I_{DC}}{3} + \frac{k_{cu1}^2}{V_{DC}} - \frac{k_{cu1}v_{u1}}{2V_{DC}}\cos(\psi_1 - \beta_1)\right)^2 - \left(2 - \frac{k_{cu1}^2}{V_{DC}^2}\right)\left(k_{cu1}v_{u1}\cos(\psi_1 - \beta_1) - k_{cu1}^2\right) \quad \text{(A.23)}$$

which leads to the following expression of v_{cu0}:

$$v_{cu0} = \frac{1}{1 - \frac{k_{cu1}^2}{2V_{DC}^2}}\left(\frac{V_{DC}}{2} - R_{arm}\frac{I_{DC}}{3} - \frac{k_{cu1}^2}{V_{DC}} + \frac{k_{cu1}v_{u1}}{2V_{DC}}\cos(\psi_1 - \beta_1) + \sqrt{\Delta}\right) \quad \text{(A.24)}$$

A.5 Reference arm-voltage $v^*_u(t)$

Using (A.12) and the notation k_{cu1} as in (A.21), it is possible to obtain the final expression of e_{cu0}:

$$\boxed{e_{cu0} = \frac{1}{2}C_e\left(v_{cu0}^2 + \frac{1}{2}\left(\frac{k_{cu1}V_{DC}}{v_{cu0}}\right)^2\right)} \quad \text{(A.25)}$$

Then the sum capacitor-voltage $v_{cua}(t)$ is expressed using (A.8), (A.13) and (A.25):

$$v_{cu}(t) = \sqrt{\frac{2}{C_e}\left(e_{cu0} - e_{cu1}\sin(\omega_0 t + \beta_1) + e_{cu2}\sin(2\omega_0 t + \beta_2)\right)} \quad \text{(A.26)}$$

Consequently (A.2) and (A.26) are replaced into (A.14) to obtain $v^*_u(t)$:

$$\boxed{v_u^*(t) = V_{DC}\frac{v_u(t)}{v_{cu}(t)}} \quad \text{(A.27)}$$

Appendix B

Thermal model of PPI, BIGT and IEGT

B.1 Press-pack IGBT

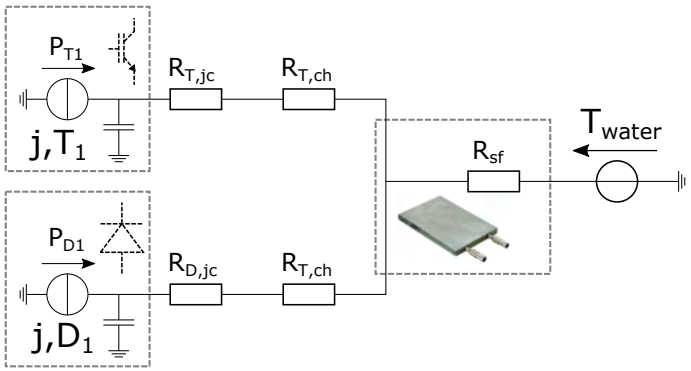


Figure B.1: Thermal model of a press-pack IGBT

PPI is designed for single-side cooling, with the base plate acting as the collector. Even if the IGBT and the diode are in the same module, coupling effects are meaningless because of the physical separation between the chips.

B.2 Bi-mode IGBT

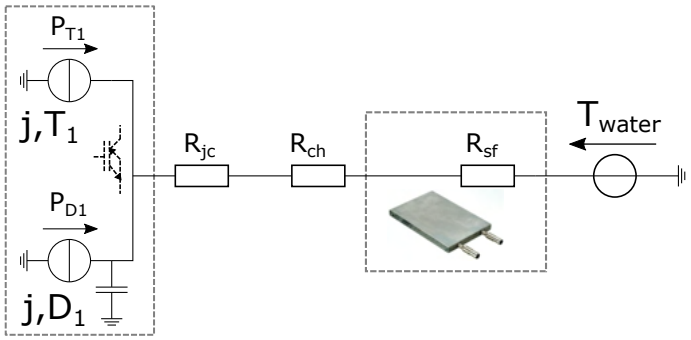


Figure B.2: Thermal model of a BIGT, IGBT and diode parts physically share the share junction

B.3 Injection-enhanced gate transistor

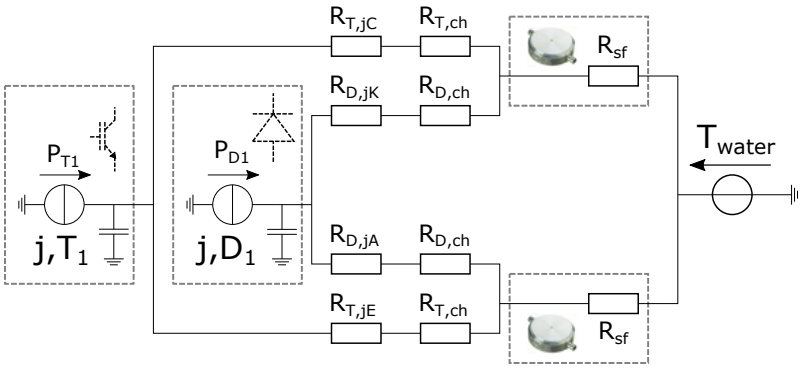


Figure B.3: Thermal model of double-side cooled IEGT

Appendix C

Instruments, sensors and probes of the test bench

Name	Designation	Main characteristics
Keysight DAQ972A	data acquisition system	3 slots for channel multiplexer modules 22-bit internal digital multimeter
Keysight DAQ901A	20-channel multiplexer module	20 channel multiplexer +2 channels for current measurements
B-Box 3.0	rapid control prototyping platform	16 PWM outputs 16 bits / 500 ksps ADCs
PULML30.241	AC-DC power supply	output voltage 24 V max. output current 1.3 A
PULML15.241	AC-DC power supply	output voltage 24 V max. output current 0.6 A
GIS40 - 35AD	AC-DC power supply for IGCTs	100 W per output channel input voltage 230 V
TDS2024B	analogue oscilloscope	200 MHz, 2 GS/s
TBS2204B	numeric oscilloscope	200 MHz, 2 GS/s

Table C.1: List of instruments

Name	Designation	Max. rating	Max. error
LEM LTC 1000-SF/SP8	current transducer	3000 Apk	±0.8%
LEM DVM 4200	voltage transducer	6000 Vpk	±0.4%
Kobold DRG 1520 G6 L303/C	water flow meter	45 L/min	±3%
Kobold DPL 1V15 G4 L303/C	water flow meter	6 L/min	±2.5%
TCSA class A PT100	temperature probe	250°C	±0.13%
CWT 30	Rogowski transducer	6000 Apk	±1%
TT-SI 9010A	differential voltage probe	7000 V	±2%

Table C.2: List of sensors and probes