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ORIGINAL RESEARCH PAPER

An improved asymmetrical multi-level inverter topology with boosted output voltage and reduced components count

M Saad Bin Arif[1,4] | **Uvais Mustafa**[1] | **Marif Daula Siddique**[2] | **Shahbaz Ahmad**[1] | **Atif Iqbal**[2] | **Ratil Hasnat Ashique**[3] | **Shahrin bin Ayob**[4]

[1] Department of Electrical Engineering, Z. H. College of Engineering and Technology, AMU, Aligarh, India

[2] Department of Electrical Engineering, Qatar University, Doha, Qatar

[3] Department of Electrical Electronics Engineering, Green University Bangladesh, Dhaka, Bangladesh

[4] Power Engineering Department, School of Electrical Engineering, UTM, Johor, Malaysia

Correspondence
Prof. Atif Iqbal (DSc, Poland, PhD, UK), Vice-Chair IEEE Qatar Section, Department of Electrical Engineering, Qatar University, PO Box 2713, Doha, Qatar.
Email: atif.iqbal@qu.edu.qa

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Abstract

This paper presents an improved Multi-level Inverter topology utilizing the concept of boosting-capacitor and two DC sources with reduced switches count for generating 17-level output. The topology employs 10 unidirectional switches including one bidirectional switch. Comparison with other recent topologies shows that the proposed topology employs a reduced number of devices and better performance. The topology combines the modularity of H-Bridge with the boosting capacity of the switched capacitor topology. Special care is taken while designing the switching strategy for voltage balancing of the capacitors. The authors also have generalized the topology to produce 'n' level output. Relevant expressions are also formed and reported. Experimental validation, as well as simulation, is performed, and results are verified. Nearest level control is used as the modulation technique.

1 | INTRODUCTION

In recent years, the use of renewable energy resources has shifted the attention of researching community towards fast and effective power conversion techniques due to the growing concern over the environment. Multi-level inverters (MLI) have emerged as an effective, practical and feasible option for improved and high-power quality power conversion [1]. They produce stepped output voltage waveform through several DC source(s), switching them in a particular manner with power conductor switches [2, 3]. The stepped voltage waveform has several advantages like reduced switching stress, increased waveform quality in terms of reduced total harmonic distortion (THD), better electromagnetic consistency, lower switching and conduction losses and improved efficiency [4, 5]. Owing to these advantages, MLI has found application in several sectors such as micro-grid [6], distributed generation [7, 8], power systems [9, 10], reactive power compensation and AC drives as well in high voltage direct current (HVDC) applications [11]. Some of the earliest work on multi-level inverters is covered by Lai and Peng in [12].

The earliest work for asymmetrical inverters can be traced back to Manjrekar et al. [13, 14]. In their work, the authors proposed a new binary method of choosing the magnitude of DC sources for Cascaded H-Bridge topology. The number of output levels showed a dramatic rise with the same number of components as compared to the symmetrical counterpart. The author is [15] proposed a novel topology to produce stepped output; it employed a principal DC source bus and the rest of the DC buses were capacitor banks. The converter control algorithm stabilized the voltage across capacitors. This topology offered a reduction in devices, but it required a complex algorithm for voltage balancing. In [16], the author proposed another novel topology that employed a single DC source and three capacitors to produce seven-level output. The topology is suitable for solar PV-grid applications. Although the topology offers an

advantage in requiring only a single DC source, it suffers from a higher total component count. Babaei et al. [17] proposed another capacitor-based asymmetrical topology. The topology offered better performance in THD and employed lesser components and increased the output level considerable. Still, it suffered from the voltage balancing issue for the capacitors. The topology required special attention for capacitor balancing, thus increasing the complexity of the control algorithm.

Gautam et al. [18] proposed another hybrid topology which employed two DC sources with capacitors. The number of capacitors depends on the output level required. The topology offered fundamental switching, equal power sharing among the cells, but it required the switches of different power ratings; also, the capacitors balancing of voltage needed, making the control algorithm complex. Jain and Sonti [19] presented another topology specifically for solar PV-based applications. The topology utilized an equal number of DC sources and capacitors. The topology offered reduced conduction losses as the number of switches in conduction path are reduced and lower common-mode current making it highly suitable for solar PV applications [20]. Apart from these, many different works are proposed in the literature for asymmetric and symmetric topologies employing capacitor banks [21, 22]. This paper has exploited the switch capacitor circuit's boosting capability and the flexible nature of H-Bridge inverter. In the proposed topology, two DC sources and three capacitors so placed between two Half-Bridge to maintain the modularity of H-Bridge and reduce the switching stress on each Half-Bridge switch. The proposed topology has added advantage that it produces inherent negative levels, thus reducing the switching stress and the device count and cost.

The basic cell of the proposed asymmetric topology produces 17-level output in an asymmetric configuration; nevertheless, the basic cells can be cascaded to produce n-level output, thus retaining the modularity. The basic cell employs two DC sources and is utilized in 2:3 ratio of magnitudes. The topology can be used in symmetric manner, also where both the DC sources are of equal magnitude. In that case, the topology offers 13-level output. The novelty of the work lies in the fact that the topology combines the advantages of H-Bridge with those of boosting voltage by incorporating a switched capacitor circuit. The topology is very much suitable for grid-tied applications and solar PV system applications as it has reduced components counts and can be easily extended to the three-phase structure. The novelty of the work and the critical points of the proposed topology can be summarized in the following points:

(a) The proposed topology offers voltage boosting with $1.6V_{in}$ gain in the asymmetric configuration.
(b) The capacitors are self-balanced because of the utilization of the redundant states in switching.
(c) The capacitor size is small, thus making it feasible.
(d) The topology offers 17-level output thus reducing the THD in the output. The output can be directly fed to the grid as the IEEE standard is met to cut the cost of the filter, making it even more feasible.

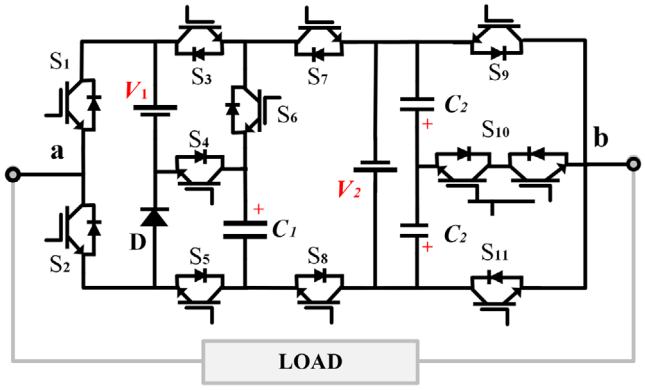


FIGURE 1 Basic cell of the proposed topology

(e) The topology utilizes a lesser number of components to produce 17-level output making it suitable for renewable energy application.

The proposed topology is suitable for interfacing different renewable energy sources with the utility grid due to its advantages like lower harmonics, lower components and economically feasible operation. The output from various renewable sources is predominantly DC. For the solar PV, the output supplied by the MPPT serves as the DC link. A DC–DC converter can be used to form the appropriate DC link of required magnitude. These DC links are fed as input to the proposed inverter and converted into AC with low harmonics. The output of the multilevel inverter can be controlled through the current controller. This is done in order to control the active and reactive power flow.

The paper is organized as follows: Section 2 discusses the topology and its working; the switching table is explained, and all the necessary calculations are performed. Section 3 deals with the generalization of the basic cell through cascading. All the necessary equations are formed. In Section 4, the simulation results of the basic cell are shown and discussed. Section 5 deals with the experimental validation of the proposed topology. Section 6 discusses the results and compares the topology in terms of components used with other topologies, and finally, the paper is concluded in Section 7.

2 | TOPOLOGY DESCRIPTION

The proposed topology is depicted in Figure 1. The magnitudes of the two DC sources can be symmetric and asymmetric in magnitude. In asymmetric combination, DC sources are in 2:3 ratio producing 17-level output voltage. Ten unidirectional switches are employed along with a single bidirectional switch. The unidirectional switch means two-quadrant operation while the bidirectional switch is a four-quadrant switch. Both the insulated gate bipolar transistors (IGBTs) of the bidirectional switch can be fed through a single gate driver circuit. The topology makes the use of boosting voltage capacity of switched capacitor topology. It is possible because of the isolated nature

TABLE 1 Different switching and capacitor charging states during one complete cycle

Modes of operation	Switching states of the switches											Source combination	Capacitor (C_1) state
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}		
Mode 8 (+)	1	0	0	1	0	0	0	1	1	0	0	$V_2 + V_{C1} + V_1$	Discharging
Mode 7 (+)	1	0	0	1	0	0	0	1	0	1	0	$V_2 + V_{C1} + V_{C2}$	Discharging
Mode 6 (+)	1	0	0	1	0	0	0	1	0	0	1	$V_2 + V_{C1}$	Discharging
Mode 5 (+)	1	0	0	0	1	0	0	1	1	0	0	$V_2 + V_1$	–
Mode 4 (+)	1	0	1	0	1	1	0	1	0	1	0	$V_2 + V_{C2}$	–
Mode 3 (+)	1	0	1	0	1	1	0	1	0	0	1	V_2	–
Mode 2 (+)	0	1	1	0	1	1	0	1	1	0	0	V_1	Charging
Mode 1 (+)	0	1	1	0	1	1	0	1	0	1	0	V_{C2}	Charging
Mode zero	0	1	0	0	1	0	0	1	0	0	1	0	Charging
Mode zero	1	0	1	0	0	0	1	0	1	0	0	0	Charging
Mode 1 (−)	1	0	1	0	0	0	1	0	0	1	0	$-V_{C2}$	Charging
Mode 2 (−)	1	0	1	0	0	0	1	0	0	0	1	$-V_1$	Charging
Mode 3 (−)	0	1	0	0	1	1	1	0	1	0	0	$-V_2$	–
Mode 4 (−)	0	1	0	0	1	1	1	0	0	1	0	$-(V_2 + V_{C2})$	–
Mode 5 (−)	0	1	0	0	1	1	1	0	0	0	1	$-(V_2 + V_1)$	–
Mode 6 (−)	0	1	1	1	1	0	1	0	1	0	0	$-(V_2 + V_{C1})$	Discharging
Mode 7 (−)	0	1	1	1	1	0	1	0	0	1	0	$-(V_2 + V_{C1} + V_{C2})$	Discharging
Mode 8 (−)	0	1	1	1	1	0	1	0	0	0	1	$-(V_2 + V_{C1} + V_1)$	Discharging

of the capacitor C_1. The modified switching strategy keeps the capacitor C_1 charged to $3V_d$ voltage level. Through proper switching, this can be exploited to boost the voltage by operating $3V_d$ DC source in series with the C_1. Where V_d is equals to one step of the voltage in the output staircase waveform. The DC voltage source V_2 is required to control the charging of C_2 and C_2'. Although it is possible to charge the C_2 and C_2' through the V_1 utilizing the redundant state switching strategy, that approach will reduce the output levels. Hence, to make the C_2 and C_2' independent of V_1, the second DC Source V_2 is used, which will increase the output levels. Thus, the topology is a hybrid amalgamation of H-Bridge and switched capacitor, retaining all the positive characteristics of both configurations. The modularity of H-Bridge and the boosting of the voltage level of switched capacitor, are incorporated in this topology. In the following section, operation of the basic circuit producing 17-level output is discussed in detail.

Table 1 shows the switching configuration for the various output voltage level. Current flow path and modes of operation during one complete cycle is shown in Figure 2. The zero levels can be produced in two states, giving the redundant states, which helps in capacitor voltage balancing. The first positive voltage is generated by turning on switches S_2, S_{10}, S_8 and S_5. This combination brings the capacitor C_2' into the conduction path and delivers the V_d level at the output. During this period, S_3 and S_6 switches are also turned on to charge the capacitor C_1 to $3V_d$.

Similarly, $2V_d$ are generated by bringing both the capacitors C_2 and C_2' into the conduction path. This is done by turning on S_2, S_9, S_8 and S_5. Again, S_3 and S_6 are turned on to exploit the circuit's redundancy and charge the capacitor C_1. $3V_d$ can be generated in two ways, either by bringing the $3V_d$ DC source into the conduction path or by bringing the capacitor C_1 which is charged to $3V_d$ into the circuit, thus providing further redundant states. To keep the voltage balanced across capacitor C_1, the $3V_d$ DC source is utilized to produce the output level by turning on the switches S_1, S_{11}, S_8 and S_5. Also, S_3 and S_6 are also turned on to keep the capacitor C_1 charged. To produce the $4V_d$, the capacitor C_1 or the DC source with $3V_d$ magnitude can be utilized. The DC source with $3V_d$ magnitude is again preferred, and the capacitor C_1 is kept charged while bringing the $3V_d$ DC source and the capacitor C_2' into the conduction path. For $5V_d$ output level, the $3V_d$ DC source, as well as both the capacitors (C_2 & C_2'), is brought into the conduction path by turning on S_1, S_9, S_8 and S_5. For $6V_d$ output level, both the $3V_d$ DC source and the capacitor C_1 are turned by switching the S_1, S_{11}, S_4 and S_8. For $7V_d$ output level, an additional capacitor C_2' is also brought into the conduction path in addition to the previous combination. Finally, for $8V_d$, all the three capacitors and the $3V_d$ DC source are brought into conduction path by turning on S_1, S_9, S_4 and S_8.

During the negative cycle, there is no redundant path for the capacitor charging. For $-V_d$, switches S_1, S_{10}, S_3 and S_7 are turned on, bringing the C_2 into conduction path and the direction of current is reversed. For $-2V_d$, both the capacitors C_2 and C_2' are brought into the reverse conduction path by turning on S_1, S_{11}, S_3 and S_7. Capacitor C_1 produces $-3V_d$ across the load. Again for $-4V_d$, capacitors C_1 and C_2 are brought into reverse conduction path in series by turning on S_2, S_{10}, S_6, S_5 and S_7. $-5V_d$ is produced by bringing all the three capacitors

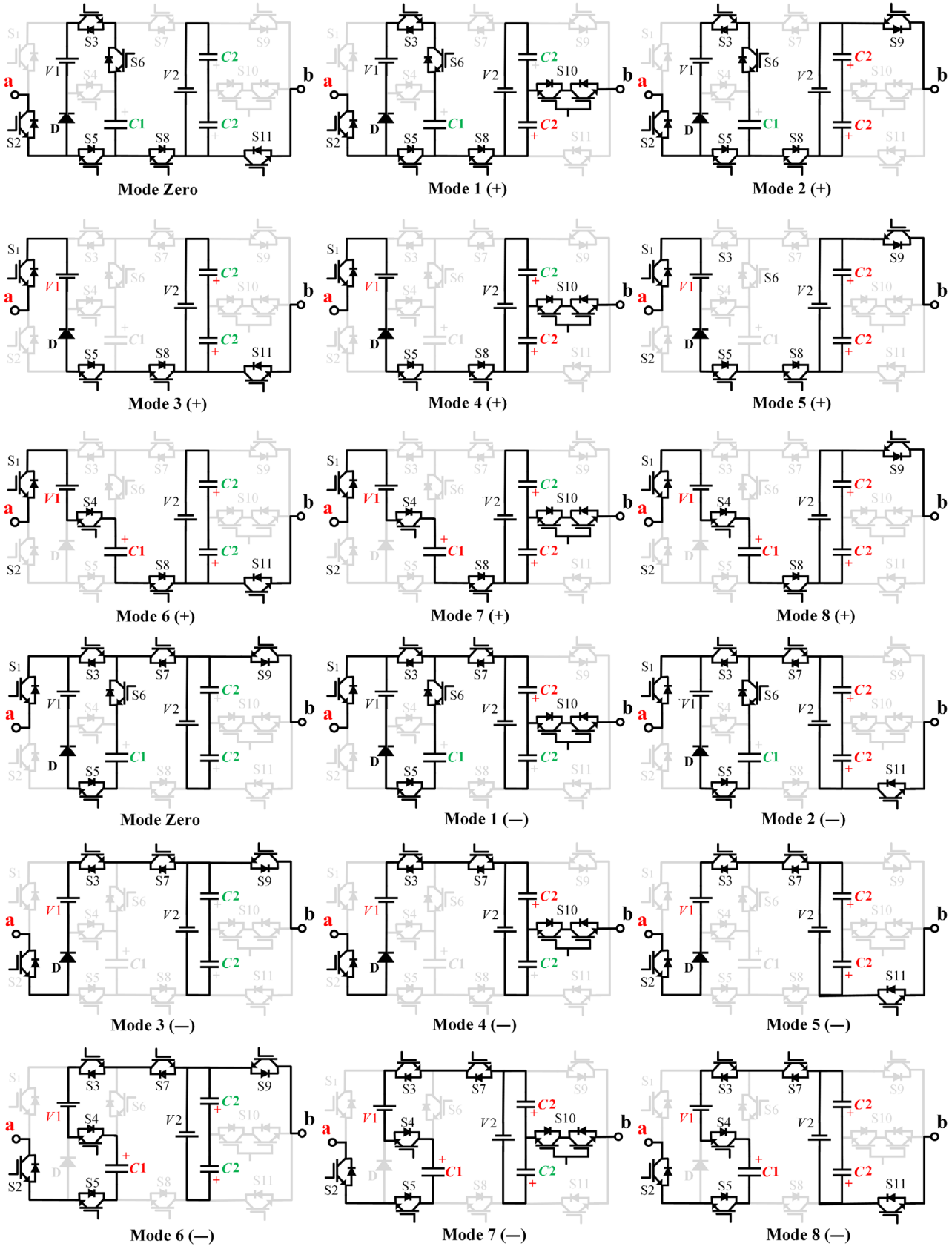


FIGURE 2 Modes of operation during one complete cycle

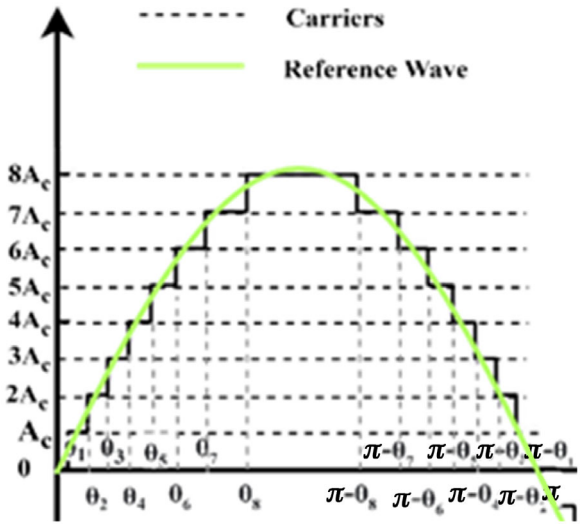


FIGURE 3 17 Level voltage waveform and switching scheme

into series. This is done by switch combination S_2, S_{11}, S_6, S_5 and S_7. For $-6V_d$ both the $3V_d$ DC source and the capacitor C_1 are made to act in series in reverse conduction path. For $-7V_d$, an additional capacitor C_2 is also brought in series with the previous combination. Finally, for $-8V_d$, all the capacitors and $3V_d$ source are put in series in reverse conduction path by turning on S_2, S_{11}, S_3, S_4, S_5 and S_7.

Table 1 shows the switching strategy as well as the capacitor C_1 charging and discharging states. Since the other two capacitors, i.e. C_2 and C_2' are continuously connected across the DC source, they are constantly in a charged state. However, capacitor C_1 is isolated and therefore, requires proper charge balancing attention. To maintain adequate charge balancing for C_1, the author has modified the switching strategy to provide the redundant states for capacitor charging.

2.1 | Capacitor sizing

The size of the capacitor plays a vital role in determining the feasibility of the converter. The size of the capacitor depends upon the energy handled by the capacitor in one complete cycle. Considering Table 1 of the switching and Figure 3 which shows the 17-level output and the switching strategy, it can be seen that for capacitor C_1, the maximum discharging time is from θ_6 to π-θ_8. Similarly, C_2 discharges for positive half cycle, i.e. (π–0) and C_2' acts complimentary to the C_2 because of their series connection and charge balance, thus C_2' discharges for the negative half cycle (2π-π). Since the capacitor C_1 involves most complex equations, the capacitor balancing process is shown for C_1. For C_2 and C_2', the process remains the same.

For the discharging period of capacitor C_1, the change in charge is given by:

$$\Delta Q_1 = \int_{\theta_6}^{\pi-\theta_8} \frac{i_L}{\omega} d(\omega t), \tag{1}$$

where i_L represents the load current. Based on the modulation index, both θ_6 and θ_8 can be calculated as follows:

$$\theta_6 = \frac{\sin^{-1}(6A_c/2A_{\text{ref}})}{2\pi f_{\text{ref}}} \tag{2}$$

$$\theta_8 = \frac{\sin^{-1}(8A_c/2A_{\text{ref}})}{2\pi f_{\text{ref}}} \tag{3}$$

Further considering a purely resistive load of resistance R, the maximum charge ripple ΔQ_1 is calculated by the following equation:

$$\Delta Q_1 = \frac{8v_d}{2\pi f_s R}(\pi - \theta_8 - \theta_6) = \frac{4v_d}{\pi f_s R}(\pi - \theta_8 - \theta_6), \tag{4}$$

where f_s is the switching frequency, and $8V_d$ is the maximum voltage that appears across load R. Now for capacitor C_1, the maximum voltage ripple can be calculated by Equation (5). The capacitor's optimum size is calculated by using (6). Using the same procedure, the capacitor size is calculated for C_2 and C_2'.

$$\Delta V_{\text{rip}} = \frac{4v_d}{\pi f_s R C_1}(\pi - \theta_8 - \theta_6), \tag{5}$$

$$opt.C_1 = \frac{4v_d}{\pi f_s R \Delta V_{\text{rip}}}(\pi - \theta_8 - \theta_6). \tag{6}$$

2.2 | Capacitor balancing

To analyse the two series capacitors' voltage balancing across the DC source, that part of the topology is explored separately and shown in Figure 4(a). The voltage balancing of capacitors depends upon the average power during the various intervals [23, 24]. The typical current and voltage waveforms of this part is also shown in Figure 4(b) and it shows that the current waveforms in 0–π interval and then π–2π interval are the same. For the interval $\alpha_1 - \alpha_2$, the waveform follows the same pattern as it follows in $[(\pi + \alpha_1) - (\pi + \alpha_2)]$. The same is true for the rest of the intervals. This is because of equal capacitance ($C_1 = C_2$), both capacitors are initially charged to an equal voltage value, i.e. $V_2/2$. The switching is designed in such a way that if for $\alpha_1 - \alpha_2$, capacitor C_1 is utilized then for the interval $[(\pi + \alpha_1) - (\pi + \alpha_2)]$, C_2 will be utilized. This process is validated as for the positive half cycle, and the lower capacitor is made to come in the current path. In contrast, for the negative half cycle, the uppermost capacitor is made into the current path. Thus, in light of Figure 4 and the above discussion, the following equations hold truth:

$$\int_{\alpha_1}^{\alpha_2} [i_o(t)v_o(t).\, d\omega t = \int_{\pi+\alpha_1}^{\pi+\alpha_2} [i_o(t).v_o(t).d\omega t] \tag{7}$$

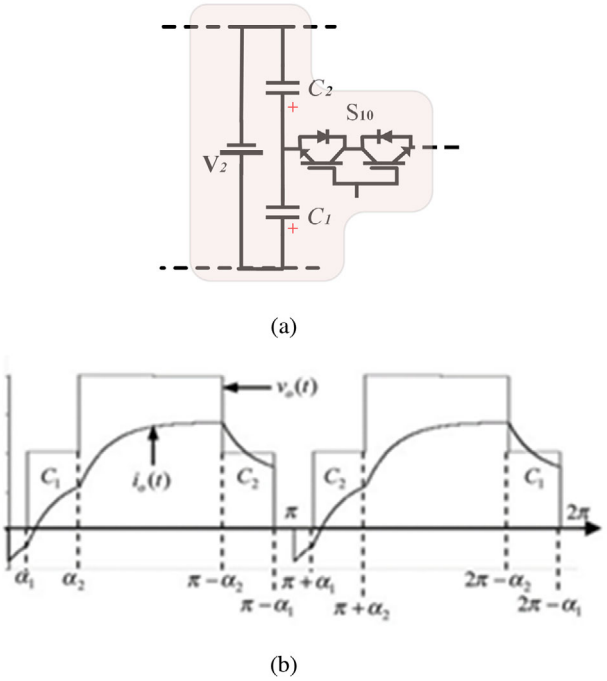


FIGURE 4 DC source with series capacitors. (a) Basic cell of DC source with series capacitors, (b) Series capacitors voltage and current [17]

and

$$\int_{\pi-\alpha_2}^{\pi-\alpha_1} [i_o(t)v_o(t).d\omega t] = \int_{2\pi-\alpha_2}^{2\pi-\alpha_1} [i_o(t).v_o(t).d\omega t]. \quad (8)$$

For the above equations, it should be noted that v_o and i_o represent the voltage and current waveform corresponding to the cell shown in Figure 4(a) only and does not mean the output voltage and current of the converter. Thus, the average power during the various intervals remains same and maintaining the voltage across the capacitors. During the interval $[(\pi-\alpha_1)-\pi]$, the current falls to zero as the capacitors are cut off from the current path. This describes the voltage balancing for the series capacitors with a DC source acting independently. This whole arrangement of DC source with series capacitors is utilized with a switched capacitor, this does not change the working of the series capacitors, only as the levels in voltage are increased because of the previously switched capacitor, Equations (7) and (8) still holds thus maintaining the voltage balance.

2.3 | Inrush current control

In one complete cycle, the switched capacitor, C_1 is charged and discharges several times. The inrush charging current is mainly determined by the gap between the charging voltage and the initial capacitor voltage at the time of charging and on the circuit parameters of the charging loop. Figure 5 depicts the simplified charging loop.

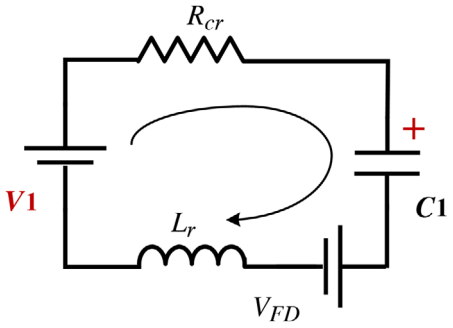


FIGURE 5 Simplified charging loop for switch capacitor

For the sake of reliability and protection, the maximum difference between the charging voltage, i.e. V_1 and the capacitor (C_1) voltage is seen. The maximum gap between these two will draw the maximum possible inrush current. This maximum gap occurs when the first charging begins, and the difference is $3V_d$. The following expression can approximate this gap:

$$\Delta V_{\max} = \frac{3V_d}{C_1 f_{\text{ref}} R}. \quad (9)$$

The approximate peak value of charging current then can be found as:

$$I_{\text{Charging\_max}} \approx \frac{\Delta V_{\max}}{r_{cr}} = \frac{3V_d}{r_{cr} C_1 f_{\text{ref}} R}, \quad (10)$$

where $R_{cr} = r_{cr}$ is the total parasitic resistance of all the charging loop components V_{FD} is the lumped forward drop of all the charging loop components. This maximum inrush charging current can be handled by inserting a small inductance L_r in the charging loop. L_r can be modelled based on maximum inrush charging current. It acts as a short circuit during the steady-state operation and protects against the maximum charging current during the transients. It reduces peak of inrush charging current and provides *di/dt* protection. To avoid any negative impact, this inductance value is kept reasonably small and set below 1 μH.

2.4 | Total standing voltage (TSV) calculation

TSV is an important aspect while deciding the switch ratings. It refers to the maximum voltage the switch has to bear during its blocking state. From the circuit, it is clear that the switches S_1, S_2, S_6, S_8 and S_{10} have to bear maximum of $3V_d$ voltage. This can be verified by applying the Kirchhoff's voltage law in their respective loop. Meanwhile, the switches S_7, S_{11} and S_9 have to bear the maximum stress of $5V_d$ as capacitor C_2, and DC source with magnitude $2V_d$ both lie in their respective loop. And S_3, S_4 and S_5 have to bear the lowest stress of V_d. Thus, three categories of switches are required in terms of their standing voltage rating, i.e. V_d, $3V_d$ and $5V_d$.

$$\text{Category 1}: V_{S9} = V_{S10} = V_{S11} = V_d, \quad (11)$$

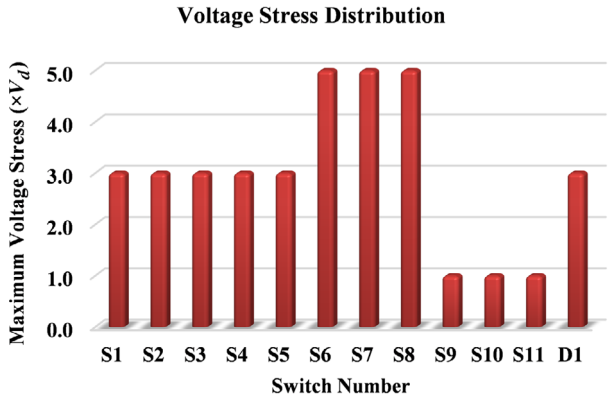


FIGURE 6 Voltage stress distribution of various switches

$$\text{Category 2}: V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = 3V_d, \quad (12)$$

$$\text{Category 3}: V_{S6} = V_{S8} = V_{S7} = 5V_d. \quad (13)$$

Also, the diode D_1 has to withstand maximum stress of $3V_d$.

$$\begin{aligned}&\text{Total Standing Voltage (TSV)}\\&= (3 \times V_d) + (6 \times 3V_d) + (3 \times 5V_d)\\&= 3V_d + 18V_d + 15V_d\\&= 36V_d. \end{aligned} \quad (14)$$

Sometimes, per-unit TSV, which is the ratio of TSV and the maximum output voltage, is also calculated. In this case,

$$\begin{aligned}\text{Per Unit TSV, TSV (pu)} &= \text{TSV}/(\text{Peak Output Voltage})\\&= 36V_d/8V_d\\&= 4.5\text{pu}. \end{aligned} \quad (15)$$

The voltage stress distribution on various switches is shown in Figure 6.

3 | CASCADED STRUCTURE

The basic structure of a cell produces 17-level output; however, the topology can be extended by cascading different cells to produce a higher number of levels. For generalization, a number of cells are cascaded together. The different characteristics associated with the cascaded structure are shown below in terms of equations. For 'k' cells cascaded together:

$$\text{Number of DC sources required, } N_{DC} = 2k, \quad (16)$$

$$\text{Number of capacitors required, } N_C = 3k \quad (17)$$

$$\text{Number of switches required, } N_{sw} = 11k \quad (18)$$

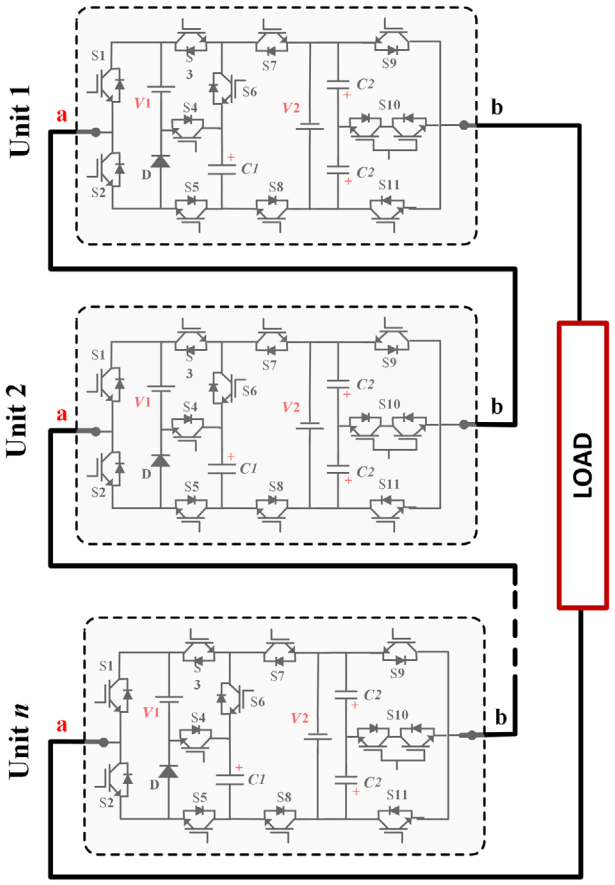


FIGURE 7 Extended n-level structure

$$\text{Number of gates required, } N_G = 11k \quad (19)$$

$$\text{Number of diodes required, } N_D = k \quad (20)$$

$$\text{Number of IGBT required, } N_{IGBT} = 12k \quad (21)$$

$$\text{Number of output level produced, } N_L = 16k + 1 \quad (22)$$

$$\text{TSV(pu)} = 4.5k. \quad (23)$$

Apart from these equations, the relationship between N_L, N_{DC} and N_{sw} can also be formulated as below:

$$N_{DC} = (N_L - 1)/8, \quad (24)$$

$$N_{sw} = 3(N_L - 1)/16. \quad (25)$$

Figure 7 depicts the generalized structure of the topology utilizing different cells cascaded together.

4 | RESULTS AND DISCUSSION

A basic cell of the topology proposed and discussed above produces 17 levels in asymmetric DC sources combination and 13 levels in symmetric mode. The converter is controlled using

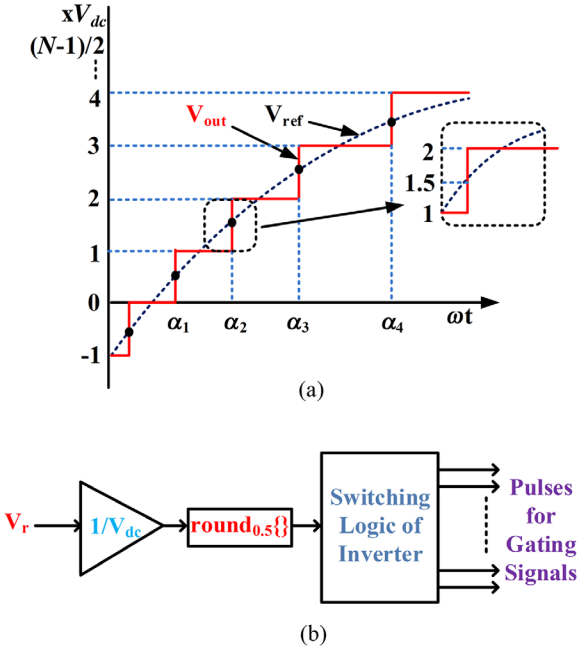


FIGURE 8 NLC switching technique

nearest level control (NLC)-based switching. Figure 8 shows the application of NLC switching technique. The switching table is depicted in Table 1. Simulation analysis and hardware validated of both the topologies has carried out and discussed in the following sections.

4.1 | Simulation analysis

The basic cell is simulated in MATLAB/Simulink environment. The simulation is performed for constant and varying load conditions to check the static and dynamic performance of the proposed topology. The values used for C_1 and C_2 in the simulation are 2.2 mF each. For symmetric operating, the value of the DC sources are $V_1 = V_2 = 150$ V whereas for asymmetric operation, the DC sources are $V_1 = 150$ V and $V_2 = 100$ V.

Figure 9(a) shows the output voltage and the current waveform for constant *RL* load for symmetrical configuration, thus producing 13-level output. Figure 9(b) depicts the output voltage and current waveforms for 17-level output. The load is specified to be 100 Ω + 80 mH in both cases. The harmonic analysis is also shown alongside. The THD in the output voltage is 4.85% for 17-level output with all the individual harmonics being less than 5%. For 13-level output, the output voltage offers 6.37% THD.

4.2 | Experimental validation

The inverter prototype is prepared in the laboratory to confirm and validate the performance and operation of the topology. Table 2 specifies the various characteristics of the components used. The output waveform shows the stable voltage levels

TABLE 2 Specifications of the hardware used

Parameters/Device	Value/Part number
IGBT switches	G60N100
Capacitors	450 V, 2200 μF
FPGA Vertix-5	(XC5VLX50T)
V_1,	80 V, 80 V (for 13 levels)
V_2	120 V, 80 V (for 17 levels)
R load	150 Ω, 75 Ω
L load	120 mH

are produced. The current drawn by the load is also depicted to confirm the proper working of the topology. Figure 10 illustrates the output voltage and current waveform for symmetrical configuration, i.e. for 13-level output while Figure 11 deals with the asymmetrical configurations, i.e. 17-level output. Figure 10 depicts the experimental validation for the symmetrical operation of the proposed topology. It produces 13-level output which can be seen in the Figures 10(a) and (b) depicts the output voltage and current for *R* (150 Ω) and *RL* (150 Ω and 120 mH) load, respectively. The current waveform is slightly lagging due to the lagging power factor of the load in Figure 10(b). Figure 10(c) shows the dynamic operation by changing the load from infinite (no load), to 150 Ω and then to 75 Ω. It can be seen that the envelope of current waveform goes on increasing as the load is decreased while the voltage waveform remains unchanging. Figure 10(d) shows the effect of change of the power factor of the load. As the power factor is changed from the lagging to unity, the current waveform is changed accordingly. The transition is smooth without any oscillation or current spike.

Figure 11 deals with the results obtained for asymmetrical operation of the topology, and it can be seen that the topology produces 17-level output. Figure 11(a) depicts the output voltage and current for *RL* load, while Figure 11(b) shows the change in the load power factor. Again, it can be noticed that the transition in the current waveform is without any disturbance. Thus, the operation of the topology in both modes is validated through the experimental setup.

5 | POWER LOSS ANALYSIS

The power losses associated with the switches involved are important as the converter's efficiency depends upon the losses. There are mainly two types of losses associated with a switch, conduction loss and switching loss. Since a power, the electronic switch includes both transistor and diode, the conduction loss across both is calculated as follows [25–27]:

$$p_{c,T}(t) = [V_T + R_T i^{\beta}(t)]\, i(t), \tag{26}$$

$$p_{c,D}(t) = [V_D + R_D i^{\beta}(t)]\, i(t), \tag{27}$$

where *T* and *D* in the subscript represent Transistor and Diode, respectively, V_T and V_D are the voltages drop across the

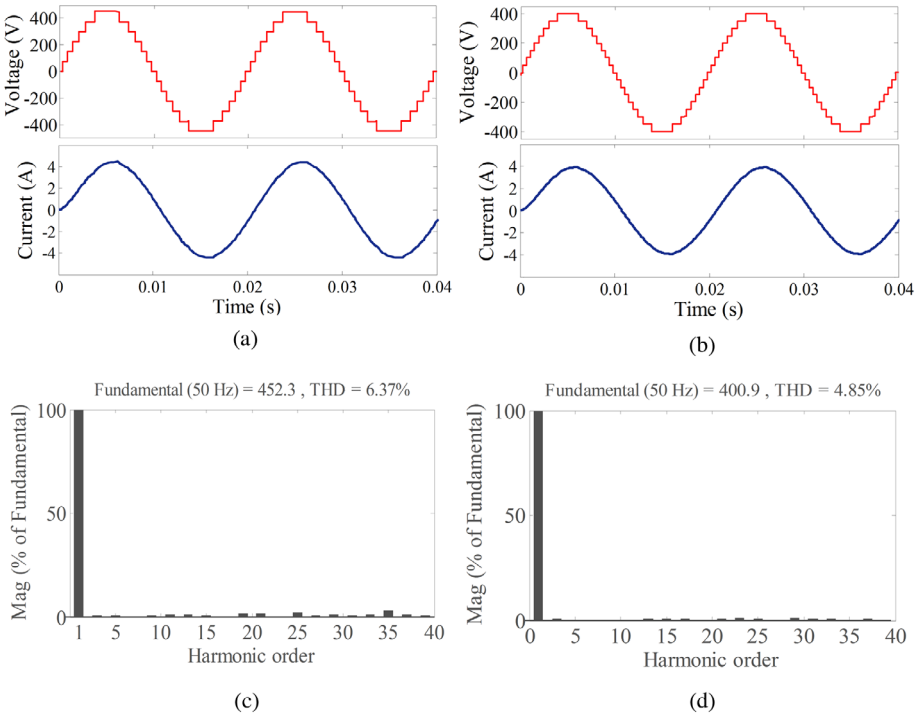


FIGURE 9 Output voltage, load current and voltage THD for 13-level and 17-level topology with constant RL load. (a) For 13-level topologies, (b) For 17-level topology, (d) THD in voltage 13-level topology, (d) THD in voltage 17-level topology

Transistor and Diode during the conduction period, R_T and R_D represent the conduction resistance, $i(t)$ is the current flowing through switch during the conduction period while β is a constant related to the Transistor specifications and can be noted down from the Datasheet. The total conduction losses of a switch are the sum of the two equations above. The average conduction loss of a converter depends upon the number of transistors and diodes conducting at an instant. Considering N_T transistors and N_D diodes are conducting at an instant t, then the average conduction loss will be

$$P_c = \frac{1}{2\pi}\int_0^{2\pi}\left[N_T(t)\,p_{c,T}(t) + N_D(t)\,p_{c,D}(t)\right]dt. \tag{28}$$

The switching losses are calculated based on energy loss. These include turn-off losses and turn-on losses and can be calculated as described in [8]:

$$\begin{aligned} E_{\text{off},k} &= \int_0^{t_{\text{off}}} v(t)\,i(t)\,dt \\ &= \int_0^{t_{\text{off}}}\left[\left(\frac{V_{\text{sw},k}}{t_{\text{off}}}t\right)\left(-\frac{I}{t_{\text{off}}}(t-t_{\text{off}})\right)\right]dt \\ &= \frac{1}{6}V_{\text{sw},k}It_{\text{off}}. \end{aligned} \tag{29}$$

Similarly,

$$\begin{aligned} E_{\text{on},k} &= \int_0^{t_{\text{on}}} v(t)\,i(t)\,dt \\ &= \int_0^{t_{\text{on}}}\left[\left(\frac{V_{\text{sw},k}}{t_{\text{on}}}t\right)\left(-\frac{I'}{t_{\text{on}}}(t-t_{on})\right)\right]dt \\ &= \frac{1}{6}V_{\text{sw},k}I't_{\text{on}}, \end{aligned} \tag{30}$$

Where $E_{\text{off},k}$ and $E_{\text{on},k}$ are the energy loss during the turn-off and turn-on period of the switch k, t_{off} and t_{on} are the turn-off and turn-on time while t is the time period, I is the current through the switch just before turning off and I' is the current through the switch just after turning it on, $V_{\text{sw},k}$ is the voltage of the switch after it is turned off. The power loss due to switching transitions in one complete cycle can be written as:

$$P_{\text{sw}} = f\sum_{k=1}^{N_{\text{switch}}}\left(\sum_{i=0}^{N_{\text{on},k}}E_{\text{on},ki} + \sum_{i=0}^{N_{\text{off},k}}E_{\text{off},ki}\right), \tag{31}$$

where f is the fundamental frequency, $N_{\text{on},k}$ and $N_{\text{off},k}$ are the number of times kth switch turn-on or turn-off in one fundamental cycle. Finally, total losses are given as:

$$P_{\text{total loss}} = P_c + P_{\text{sw}}. \tag{32}$$

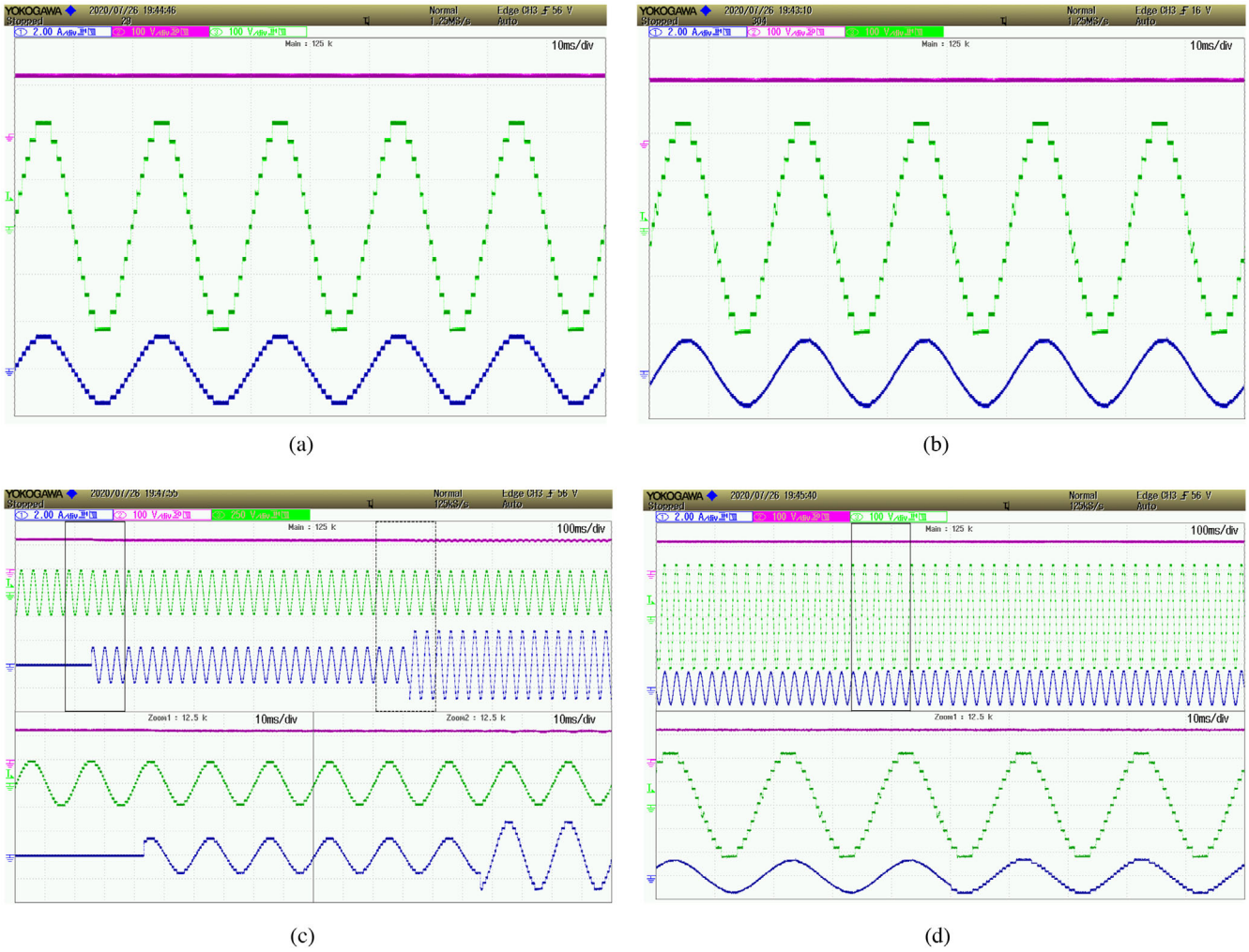


FIGURE 10 Output voltage, load current and capacitor voltage of the proposed 13-level topology. (a) Waveforms with fixed *R* load, (b) Waveforms with fixed *RL* load, (c) Waveforms with varying *R* Load, (d) Waveforms with varying load power factor

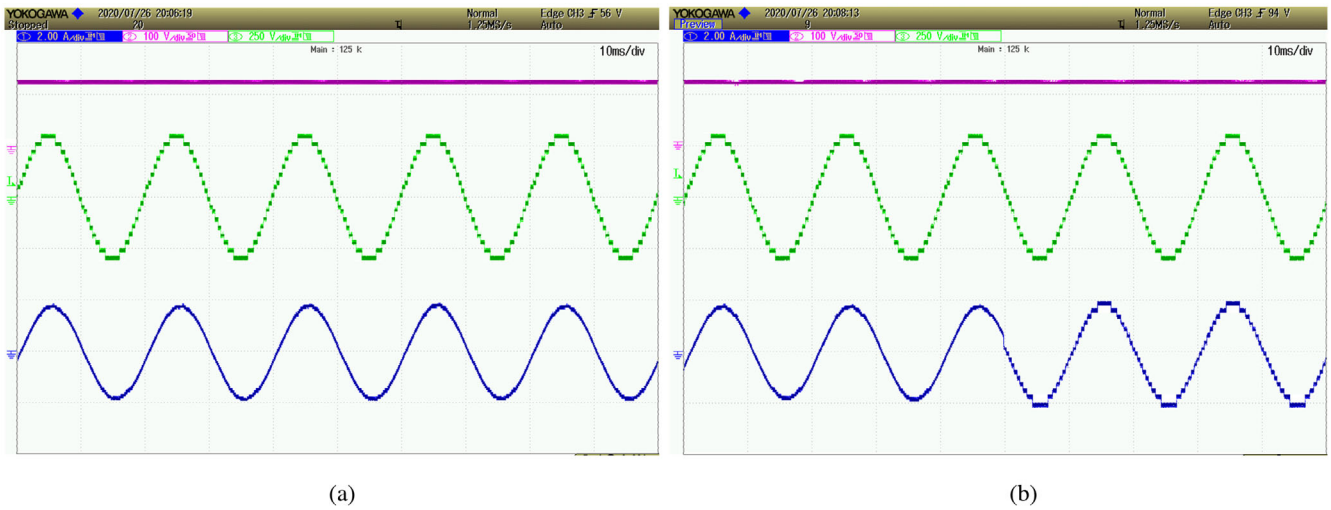


FIGURE 11 Output voltage, load current and capacitor voltage of the proposed 17-level topology. (a) Waveforms with fixed *RL* load, (b) Waveforms with varying load power factor

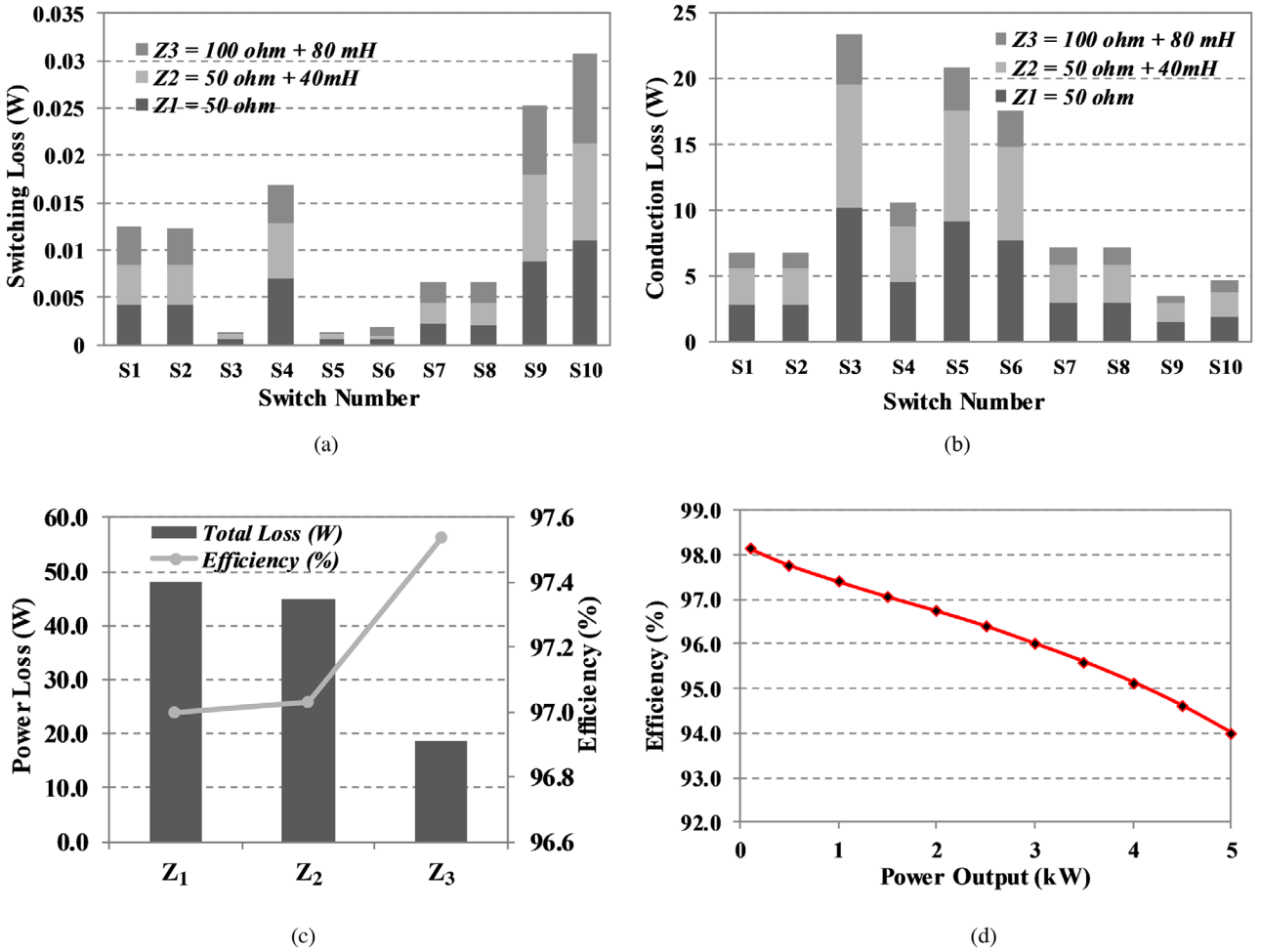


FIGURE 12 Results obtained from the power loss analysis of the proposed inverter topology. (a) Switching losses, (b) Conduction losses, (c) Total loss with efficiency, (d) Efficiency versus power output

To check the performance of the topology, power losses are calculated at three different loads which are specified as $Z_1 = 50\ \Omega$, $Z_2 = 50\ \Omega + 40$ mH and $Z_3 = 100\ \Omega + 80$ mH. Figures 12(a) and (b) depict the switching and conduction losses in the topology for both the three loads, respectively. Moreover, total power loss with the efficiency variation is also shown for all the three loads in Figure 12(c). Efficiency versus power output curve is depicted in Figure 12(d).

6 | COMPARATIVE ANALYSIS AND DISCUSSION

The following section validates the proposed topology by comparing the other topologies present in the literature. Since the different topologies produce different levels, it is not fair to compare them straightforward. To do a fair comparison, authors have added N_L/N_{IGBT} ratio. The other parameters used are N_{gd} (No. of gate drivers), N_{DC} (No. of DC source used), N_L (No. of levels generated), N_{IGBT} (No. of IGBT used), N_{C} (No. of capacitor used), TSV_{pu} (total standing voltage) and MBV_{pu} (maximum blocking voltage) and the boosting capability of the topology. The comparison is made in the following subsections.

6.1 | Number of levels versus number of IGBT

For the comparison purpose, N_L/N_{IGBT} ratio is included by the author. This ratio gives insight into the cost-effectiveness of the topology. Higher the N_L/N_{IGBT} ratio, fewer would IGBTs used, and higher would be the output levels. Thus, better quality output with a lower number of IGBTs and more feasible the topology is. Some of the topologies utilize bidirectional switches. The N_{IGBT} and N_{gd} are different as a bidirectional switch combines two IGBTs but fed by single gate driver. Based on the above table, it can be seen that the proposed topology has 1.42 N_L/N_{IGBT} ratio. Topologies present in [31] and [35] have higher N_L/N_{IGBT} ratios, but they utilize many DC sources and have no boosting capability. Topology in [32] has the lowest N_L/N_{IGBT} ratio while the proposed topology has second-best ratio among the topologies included above. Thus, based on the above discussion, it is clear that the proposed topology is feasible for renewable energy applications.

TABLE 3 Comparison with other topologies

Topology	N_{DC}	N_L	N_{IGBT}	N_L/N_{IGBT}	N_{gd}	N_C	TSV_{pu}	MBV_{pu}	Boosting
[28]	4	17	16	1.06	14	8	4.00	0.375	No
[29]	4	17	12	1.42	09	0	6.00	1	No
[30]	4	17	12	1.42	10	0	5.50	1.67	No
[31]	4	15	10	1.50	8	0	4.57	1	No
[32]	4	09	11	0.82	11	0	6.75	1	No
[33]	1	09	12	0.75	12	3	6.50	1	No
[34]	2	13	14	0.93	11	2	5.33	1	Yes
[35]	4	17	10	1.70	10	0	4.00	0.75	No
[P]	**2**	**17**	**12**	**1.42**	**11**	**2**	**4.50**	**0.625**	**Yes**

6.2 | Number of levels versus number of DC sources

The number of DC sources play an important role in the application feasibility of the topology. Higher the number of DC sources, more would the cost and voltage stress on the switches. From Table 3, [33] has the lowest number of DC sources. It only utilizes a single DC source but produces nine-level output with no boosting capability and utilizing three capacitors. The proposed topology utilizes only two DC sources and gives 17-level output; thus, it is clear that the proposed topology offers a feasible option for better power quality.

6.3 | Number of levels versus TSV_{pu} and MBV_{pu}

TSV (pu) is an important aspect while determining the feasibility of a topology as it is an indirect measurement of the rating of the IGBTs used. Higher the TSV_{pu}, more would be the rating and cost of the IGBT. The proposed topology has 4.5 pu of TSV. The topology in [28] has the best TSV_{pu} of 4 only, but it requires a higher number of DC sources. Among the 17-level topologies, the proposed topology offers relatively good TSV. Figure 13(a) shows the graphical comparison of TSVs. Another critical parameter is MBV_{pu}. It is the representation of the average blocking capability required for a switch in the topology. Lower the value of MBV_{pu}, better it is. From the above table and discussion, it can be seen that the proposed topology has the best MBV_{pu} among all the work discussed. It signifies that on average a switch in proposed topology has to withstand the stress of only 0.675 pu. Thus, from the above discussion, it can be concluded that based on the MBV_{pu} and TSV_{pu}, the proposed topology offers good performance.

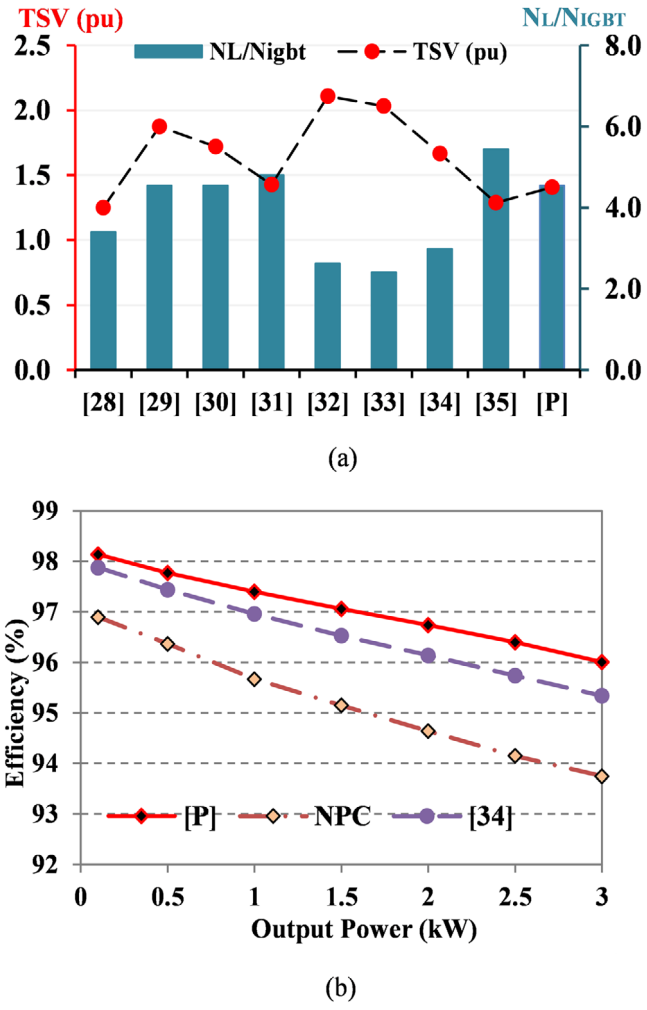
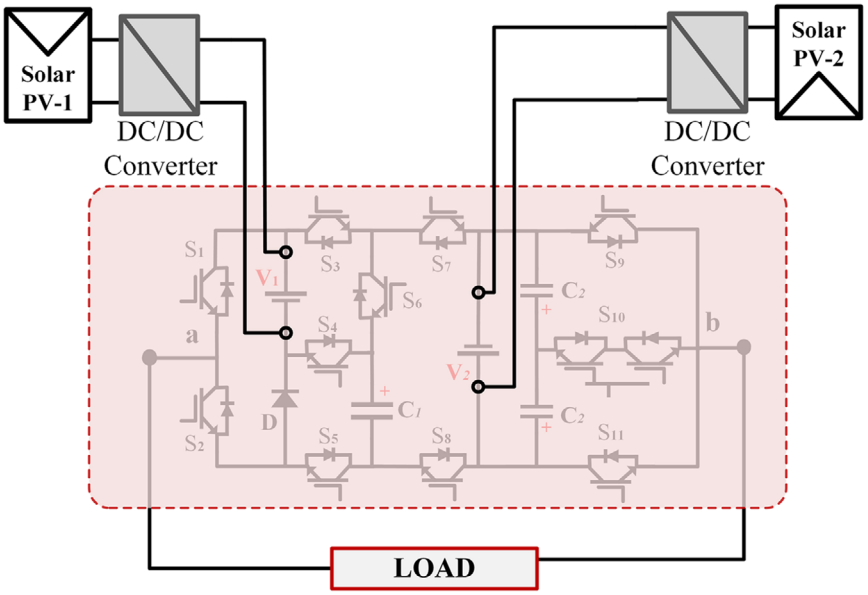


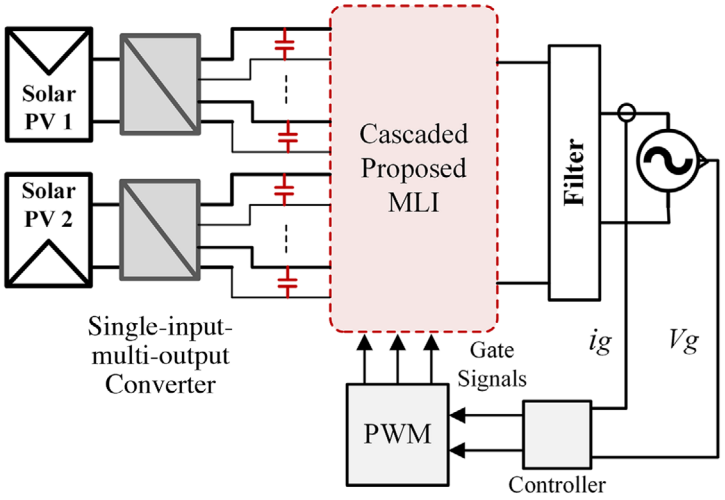
FIGURE 13 Comparison with other similar topologies. (a) TSV (pu) and NL/NIGBT, (b) Efficiency (%) vs Output Power (kW)

6.4 | Comparison based on boosting capability

The boosting capability of a topology means that its peak value of output voltage is greater than the total supplied DC voltage. The ratio of $V_{o,peak}/V_{in,dc}$ is termed as the boosting gain. The proposed topology has 1.6 gain in the output voltage. Only one other topology [34] has the boosting capability, but it utilizes 14 IGBTs to produce 13-level output. Moreover, it has higher TSV_{pu} and MBV_{pu} then the proposed topology. Thus, the proposed topology offers boosted output with reduced TSV_{pu} and lower number of DC sources.



(a) Application of Single cell configuration



(b) Application of Cascaded Configuration

FIGURE 14 Proposed topology implementing single-input multiple-output DC–DC converters. (a) Application of Single cell configuration, (b) Application of Cascaded Configuration

6.5 | Comparison based on efficiency

For efficiency comparison, thermal modelling of the proposed and other compared topologies has been done in PLECS software. Figure 13(b) depicts the efficiency versus rated output power curve of the proposed topology and capacitor-based conventional topology, i.e. NPC and the topology presented in [34] at the same peak voltage at the output. It can be seen that the proposed topology performs better in terms of efficiency. Thus, the proposed topology is efficient and has a lower number of sources suitable for renewable energy applications.

Thus, considering the comparative study above and the experimental as well as simulation analysis, following remarks regarding the problems solved by the proposed topology can be made:

(a) The multi-level inverter's first and foremost problem is the trade-off between the better waveform, i.e. higher output levels and the lower device count. The proposed topology offers 17-level output with a lower number of devices used. As shown in Table 3, the topology offers 1.54 N_L/N_{sw} ratio.

(b) Due to the voltage boosting ability, the topology reduces the number of DC sources required to produce a higher output.

(c) The capacitors utilized are of smaller size and does not require any extra sensor to maintain the voltage stability; thus, control complexity is reduced.

Although there are various applications suitable for multi-level inverters such as Electric Vehicles [36], integration of solar

panels into utility grid with MLI acting as interface [8] etc, considering the discussion above it is safe to say that the proposed topology is suitable for renewable energy applications, especially solar PV-based applications. Since the proposed topology is asymmetric, one of the main disadvantages is that it requires a large variety of DC sources in cascaded structures. A single cell, it utilizes two DC sources of different magnitudes. Two PV panels with MPPT can be used as two isolated DC sources for a single cell. In case the topology is utilized in cascaded structure, or a modular structure, a single input, multi-output DC–DC converters can be used to provide different sources of the same magnitude. This will require two DC–DC converters with multiple outputs to act as two different sources of magnitudes for different cascaded cells of the proposed topology. Figure 14 depicts the application of the proposed topology in single-cell operation and cascaded structure utilizing multiple output DC–DC converter.

7 | CONCLUSION

This paper presents a new and improved topology to produce the 17-level boosted output with a gain of 1.6 in asymmetric mode. The topology offers lower TSV_{pu} as well as utilizes a lower number of switches. The topology uses 11 switches with one switch being of bidirectional blocking and bidirectional conducting operation. The topology employs two DC sources in 2:3 ratio for asymmetric configuration along with three capacitors. The topology can also be used in the symmetric structure at the cost of a lower number of levels, i.e. producing 13-level output. The capacitor helps boost the number of levels through various combinations by a factor of 1.5 in symmetric mode and a factor of 1.6 in asymmetric DC combinations. The performance of the topology is proved to be satisfactory in static as well as in dynamic conditions. Experimental validation is done using the developed prototype. The promising results are obtained in the experimental setup. The topology is compared with other topologies to confirm the effectiveness and assert that the topology is suitable for the various medium- and high-power applications.

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ORCID

Marif Daula Siddique https://orcid.org/0000-0002-0799-500X
Shahbaz Ahmad https://orcid.org/0000-0001-5322-9835
Atif Iqbal https://orcid.org/0000-0002-6932-4367

REFERENCES

1. Rodriguez, J., Jih, S.L., Fang, Z.P.: Multilevel inverters: A survey of topologies, controls, and applications. IEEE Trans. Ind. Electron. 49(4), 724–738 (2002)
2. Raman, S.R., et al.: Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution. IEEE Trans. Power Electron. 33(7), 5937–5948 (2018)
3. Ding, K., Cheng, K.W.E., Zou, Y.P.: Analysis, of an asymmetric modulation method for cascaded multilevel inverters. IET Power Electron. 5(1), 74–85 (2012)
4. Pereda, J., Dixon, J.: Cascaded multilevel converters: Optimal asymmetries and floating capacitor control. IEEE Trans. Ind. Electron. 60(11), 4784–4793 (2013)
5. Farokhnia, N., et al.: Minimization of total harmonic distortion in a cascaded multilevel inverter by regulating of voltages DC sources. IET Power Electron. 5(1), 106–114 (2012)
6. Raman, S.R., Ye, Y., Cheng, K.W.E.: Switched-capacitor multilevel inverters for high frequency AC microgrids. In: Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC (Institute of Electrical and Electronics Engineers Inc.), pp. 2559–2564 (2017)
7. Ye, Z., Jain, P.K., Sen, P.C.: Circulating current minimization in high-frequency AC power distribution architecture with multiple inverter modules operated in parallel. IEEE Trans. Ind. Electron. 54(5), 2673–2687 (2007)
8. Mustafa, U., et al.: Efficiency improvement of the solar PV-system using nanofluid and developed inverter topology. Energy Sources Part A 1–17 (2020)
9. Romero-Cadaval, E., et al.: Power injection system for grid-connected photovoltaic generation systems based on two collaborative voltage source inverters. IEEE Trans. Ind. Electron. 56(11), 4389–4398 (2009)
10. Turner, R., Walton, S., Duke, R.: Stability and bandwidth implications of digitally controlled grid-connected parallel inverters. IEEE Trans. Ind. Electron. 57(11), 3685–3694 (2010)
11. Peng, W., Ye, Y., Jiang, B.: Cost-effective solution of EV motor driver based on asymmetric cascaded multilevel inverters. In: 7th International Conference on Power Electronics Systems and Applications-Smart Mobility, Power Transfer & Security (PESA), IEEE (2017)
12. Lai, J.-S., Peng, F.Z.: Multilevel converters—A new breed of power converters. IEEE Trans. Ind. Appl. 32(3), 509–517 (1996)
13. Manjrekar, M.D., Lipo, T.A.: A hybrid multilevel inverter topology for drive applications. In: APEC'98 Thirteenth Annual Applied Power Electronics Conference and Exposition, IEEE (1998)
14. Manjrekar, M.D., Steimer, P.K., Lipo, T.A.: Hybrid multilevel power conversion system: A competitive solution for high-power applications. IEEE Trans. Ind. Appl. 36(3), 834–841 (2000)
15. Ounejjar, Y., Al-Haddad, K., Gregoire, L.-A.: Packed U cells multilevel converter topology: Theoretical study and experimental validation. IEEE Trans. Ind. Electron. 58(4), 1294–1306 (2010)
16. Ebrahimi, J., Babaei, E., Gharehpetian, G.B.: A new multilevel converter topology with reduced number of power electronic components. IEEE Trans. Ind. Electron. 59(2), 655–667 (2011)
17. Babaei, E., Kangarlu, M.F., Sabahi, M.: Extended multilevel converters: An attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters. IET Power Electron. 7(1), 157–166 (2014)
18. Gautam, S.P., Kumar, L., Gupta, S.: Hybrid topology of symmetrical multilevel inverter using less number of devices. IET Power Electron. 8(11), 2125–2135 (2015)
19. Jain, S., Sonti, V.: A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems. IEEE Trans. Ind. Electron. 64(4), 2865–2875 (2016)
20. Peng, W., et al.: Seven-level inverter with self-balanced switched-capacitor and its cascaded extension. IEEE Trans. Power Electron. 34(12), 11889–11896 (2019)
21. Mustafa, U., et al.: Single phase seven-level inverter topology with single DC source and reduce device count for medium and high power

applications. In: Innovations in Power and Advanced Computing Technologies (i-PACT), IEEE (2019)
22. Ye, Y., et al.: A step-up switched-capacitor multilevel inverter with self-voltage balancing. IEEE Trans. Ind. Electron. 61(12), 6672–6680 (2014)
23. Alishah, R.S., et al.: A new generalized cascade multilevel converter topology and its improved modulation technique. Int. J. Circuit Theory Appl. (2020). https://doi.org/10.1002/cta.2880
24. Alishah, R.S., et al.: New high step-up multilevel converter topology with self-voltage balancing ability and its optimization analysis. IEEE Trans. Ind. Electron. 64(9), 7060–7070 (2017)
25. Aalami, M., et al.: Ladder-switch based multilevel inverter with reduced devices count. In: 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), IEEE (2020)
26. Masoudinia, F., et al.: New basic unit and cascaded multilevel inverters with reduced power electronic devices. Int. J. Electron. 107(7), 1177–1194 (2020)
27. Tackie, S.N., Babaei, E.: Modified topology for three-phase multilevel inverters based on a developed H-Bridge inverter. Electronics 9(11), 1848 (2020)
28. Jagabar Sathik, M., et al.: A new generalized switched diode multilevel inverter topology with reduced switch count and voltage on switches. Int. J. Circuit Theory Appl. 48, 619–637 (2020)
29. Samadaei, E., et al.: A square T-type (ST-Type) module for asymmetrical multilevel inverters. IEEE Trans. Power Electron. 33(2), 987–996 (2018)
30. Alishah, R.S., et al.: A new general multilevel converter topology based on cascaded connection of submultilevel units with reduced switching components, DC sources, and blocked voltage by switches. IEEE Trans. Ind. Electron. 63(11), 7157–7164 (2016)
31. Kakar, S., et. al., New asymmetrical modular multilevel inverter topology with reduced number of switches. IEEE Access 9, 27627 (2021). https://doi.org/10.1109/ACCESS.2021.3057554
32. Babaei, E., Laali, S., Bayat, Z.: A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. IEEE Trans. Ind. Electron. 62(2), 922–929 (2014)
33. Sandeep, N., Yaragatti, U.R.: Operation and control of an improved hybrid nine-level inverter. IEEE Trans. Ind. Appl. 53(6), 5676–5686 (2017)
34. Samadaei, E., Kaviani, M., Bertilsson, K.: A 13-levels module (K-type) with two DC sources for multilevel inverters. IEEE Trans. Ind. Electron. 66(7), 5186–5196 (2018)
35. Siddique, M.D., et al.: A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress. Int. Trans. Electr. Energy Syst. 30(2), 1–21 (2020)
36. Pereda, J., Dixon, J.: High-frequency link: A solution for using only one DC source in asymmetric cascaded multilevel inverters. IEEE Trans. Ind. Electron. 58(9), 3884–3892 (2011)

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