IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received January 10, 2021, accepted January 31, 2021, date of publication February 5, 2021, date of current version February 19, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3057554

New Asymmetrical Modular Multilevel Inverter Topology With Reduced Number of Switches

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This work was supported in part by the Ministry of Higher Education Malaysia (MOHE) and Universiti Teknologi Malaysia through the UTM Encouragement Research (UTMER) under Grant 19J28. The APC for this article is funded by the Qatar National Library, Doha, Qatar.

ABSTRACT In this article, a new single-phase multilevel inverter is introduced with a reduced number of power switches and reduced voltage stress on power switches. The proposed topology consists of four input dc sources and nine semiconductor switches (eight unidirectional and one bidirectional switch). The topology can be used for asymmetrical voltage source configuration to generate seventeen voltage levels. The extended topology is constructed by a series connection of the topology circuit to produce higher voltage levels with less voltage stress on the switches without modifying the existing structure. Comparison is made with traditional and recently introduced topologies based on the number of power switches, dc sources, total blocking voltage of switches, and gate driver circuits, to prove the proposed topology's superiority. A simple nearest level modulation has been deployed as the switching scheme. Validation on the viability of the proposed topology has been carried out through simulation and hardware experimental setup.

INDEX TERMS Asymmetrical configuration, modular multilevel inverter (MLI), nearest level control (NLC), total harmonics distortion (THD).

I. INTRODUCTION

In recent years, the power industry demanded high and quality power in the megawatts range. This motivated researchers to introduce a new breed of power inverters to attain a high-quality output voltage. The classical two-level inverter is not suitable for high power since it needs to withstand high voltage stress. Moreover, its high dv/dt and di/dt introduces high electromagnetic interference (EMI) to the whole system. The introduction of multilevel inverter MLI technology overcame the limitations of the two-level inverter. MLIs are one of the most popular technologies used in power systems to improve the performance of Photovoltaic (PV) systems, electric vehicles (EVs), FACTS devices, HVDC systems, adjustable-speed drives, wind turbine, Static VAR Compensations, active power filters, and other medium and high power applications [1]–[5].

The associate editor coordinating the review of this manuscript and approving it for publication was Inam Nutkani.

Multilevel inverters are explored and grown at a much higher rate in recent times. However, this technology is still under research and development, and new multilevel inverters circuit topologies have been presented in recent times [6], [7]. A multilevel inverter's basic idea is to generate a staircase AC voltage waveform near sinusoidal shape by utilizing several semiconductor power switches connected to dc input voltage sources. Multilevel inverter topologies have paid much attention recently due to decreased power ratings of the switches, better harmonics performance, and decreased electromagnetic interference that can be realized by generating staircase voltage waveform near to sinusoidal shape.

There are three well known traditional multilevel inverter topologies; cascaded H-bridge (CHB) MLI topology, Neutral-point clamped (NPC) [8], and flying-Capacitor (FC) [9]. The multilevel inverters (MLI) concept was first introduced in the 1970s by Baker and Bannister [10]. It describes a converter topology that can produce multilevel voltage waveform from several H-Bridge units connections

with separate dc voltage sources. Compared to NPCMLI and FCMLI, CHBMLI uses fewer power semiconductor switches, highly modular in structure, and simple control can be implemented. Flying capacitors and clamping diodes are not required in this MLI topology. NPC topology requires additional clamping-diodes and, the unequal voltage balancing of the series-connected input capacitors is problematic. FC MLI is an alternative topology to NPC. However, it requires a large number of power switches and storage capacitors when the number of voltage levels are increased.

The classical MLI topologies have their own merits and drawbacks. However, the main drawback of classical inverter topologies is that the number of device count increases significantly as the output voltage levels increase. Therefore, the system can be costly, bulky, and complicated to control. Recently, different multilevel inverter topologies have been proposed by researchers to solve and mitigate the problems associated with conventional MLIs. They mainly focused on utilizing less the number of semiconductor devices, gate driver circuits, dc sources, increased voltage levels, less harmonic distortion, and decreased blocking voltage of switches.

Based on the magnitude of dc voltage sources, MLIs can be classified as symmetrical and asymmetrical configurations. Identical dc sources are employed in symmetrical MLIs, whereas asymmetrical MLIs use dc voltage sources with unequal values. Among them, asymmetric MLI topologies are attracting the great attention of researchers. This configuration's main benefit is using lesser active and passive components to achieve high output levels. Many topologies are recently developed based on the optimal utilization of unequal dc sources by the least number of power components [11]–[30].

In [13], the topology uses a trinary sequence of asymmetric dc-source value is introduced. The MLI is designed and implemented with symmetric and asymmetric configurations. The inverter requires a smaller number of switches due to the addition and subtraction of input dc sources. However, this structure utilizes many different voltage-rated switches and an H-bridge inverter with high voltage stress on power switches. Besides, various voltage source algorithms have been presented to calculate the magnitude of input dc sources. A new inverter based on the switched diode concept is presented in [14]. The basic unit comprises a discrete diode, dual sources, and a single switch. The advantage of this topology is to utilize diodes, which leads to a reduction of switch count. However, as the voltage levels increase, it is necessary to have many input dc voltage sources.

The structures developed in [11]–[16] have used the H-bridge inverters as a polarity changer to obtain the output terminal's voltage waveform. However, the total standing voltage is high due to the utilization of the H-bridge. Therefore, the high voltage stress across H-bridge switches increases the total standing voltage, limiting their high-power medium-voltage applications.

The problem mentioned above has been solved in [17]–[29], where the MLIs are developed without using H-bridge that inherently produces both positive and negative voltage levels.

The topologies presented in [17]–[21] are examined with extended structures of basic units. These topologies can be extended with basic units for higher voltage levels, but the maximum total standing voltages (TSV) on the switches is still high.

Modular based topologies [24]–[29] are evolved to reduce voltage stress and total standing voltage of the topology with inherent polarity voltage changer. In [26], two modular topologies are introduced to generate high voltage levels with reduced power switches. The inverter uses eight switches and four input dc sources, in an asymmetric operation sequence and generates 13-levels. The topology introduced in [27] is an improved version of the former topology, where two T-type back-to-back inverters are connected across four semiconductor switches. The inverter uses 12 power switches and four input dc sources to synthesize 17L voltage waveform at the output; dc sources are selected in trinary sequence. At least two power switches have to bear the peak of the output voltage in these above topologies. Although these topologies generate a high number of voltage levels with fewer dc-sources, the number of power switches is relatively high. Another 7L topology based on a T-type inverter is proposed in [28]. The proposed inverter connects two T-type inverters using cross-connected power switches. The inverter is suggested for low power applications only. The maximum blocking voltage stress on the cross-connected switches is also high.

Hence, this study is focused on designing an asymmetric topology by making a trade-off between voltage stress on switches, the number of switches, voltage levels, and system structure complexity. In this work, 17-level circuit topology is proposed to produce all voltage levels with uniform step size utilizing fewer power switches. The proposed inverter is designed using MATLAB/Simulink software with simulations and verified by experimental results at inductive load. The presented topology is also compared with traditional MLIs and other recently introduced MLIs to show its performance. Its structure and operating principle are addressed in Section II. A comparative study of the proposed inverter against other topologies is carried out in section III. In section IV, the simulation and experimental results are presented. Finally, the conclusion is presented in Section V.

II. PROPOSED MODULAR MLI

The basic unit of the proposed inverter circuit is depicted in Fig.1. It consists of four input dc voltage sources with one bi-directional power switch and eight unidirectional power switches. The unidirectional switch is comprised of a power IGBT/MOSFET and an anti-parallel diode. In contrast, the bidirectional power switch comprises two power IGBTs/MOSFETs, two anti-parallel diodes, and a gate-driver circuits. The purpose of anti-parallel diodes is to pass current in both directions, and voltage can be blocked in one direction. The magnitude of the first two input dc voltage sources

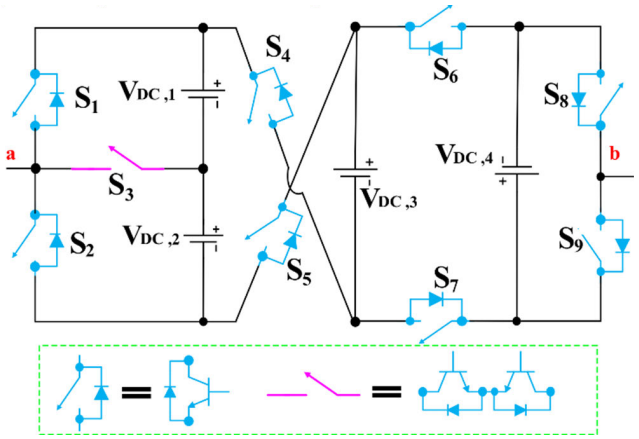

FIGURE 1. The basic unit of the proposed MLI topology.

are selected as $1V_{DC}$ each, and the other two dc sources have the magnitude of $3V_{DC}$ each. The proposed inverter is very suitable for some applications, including Stand-alone Photovoltaic (PV) systems and battery energy storage systems (BESS). The Stand-alone PV systems are specially used in areas with no access or are not easily accessible to an electric grid. In many stand-alone photovoltaic systems, batteries are utilized for energy-storage purposes. Batteries are often used in PV systems to store energy produced by the PV array during daytime and supply it to electrical loads as needed. For BESS application using the proposed inverter circuit, the battery cells can be connected in parallel and series combinations to form battery packs, to get the desired voltage and current.

The basic unit of the proposed topology can generate seventeen voltage levels if the dc voltage sources are selected as:

$$V_{DC,1} = V_{DC,2} = 1V_{DC} \tag{1}$$

$$V_{DC,3} = V_{DC,4} = 3V_{DC} \tag{2}$$

According to this configuration, the basic unit can generate 17L of 0V, $\pm 1V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, $\pm 7V_{dc}$, and $\pm 8V_{dc}$ in output with a step size of V_{dc}. Table 1 tabulates the switching states for proposed 17-level MLI, while Fig. 2 explains the proposed 17-level MLI modes during a positive cycle. Blue dotted lines indicate the current-carrying paths during each operation. Table 1 shows the switching states of 17-level MLI. It can be observed that for some voltage states, the proposed topology contains switching redundancies.

The basic unit of the proposed inverter structure can be connected in cascade to increase the number of voltage steps. Fig.3 shows the generalized inverter circuit for higher output voltage levels. The cascaded structure can generate a higher number of voltage steps with a suitable selection of input sources in asymmetric mode. The number of power switches, total standing voltage, dc-links, and gate-driver circuit can be calculated using formulae in Table 2, where, 'n' represents the number of the basic units.

TABLE 1. Switching states for 17-level proposed MLI.

No	Switches state									V_0
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	
1	0	0	1	0	1	1	0	1	0	
2	0	1	0	1	0	0	1	1	0	
3	1	0	0	0	1	1	0	1	0	
4	0	0	1	1	0	0	1	1	0	
5	1	0	0	1	0	0	1	1	0	
6	0	1	0	0	1	0	1	0	1	
7	0	0	1	0	1	0	1	0	1	$4V_{DC}$
8	1	0	0	0	1	0	1	0	1	$5V_{DC}$
9	0	1	0	0	1	0	1	1	0	$6V_{DC}$
10	0	0	1	0	1	0	1	1	0	$7V_{DC}$
11	1	0	0	0	1	0	1	1	0	$8V_{DC}$
11	1	0	0	1	0	0	1	0	1	
12	0	1	0	0	1	1	0	1	0	
13	0	0	1	1	0	0	1	0	1	
14	1	0	0	0	1	1	0	0	1	
14	0	1	0	1	0	0	1	0	1	
15	0	0	1	1	0	0	1	1	0	
16	0	1	0	0	1	1	0	1	1	
17	1	0	0	1	0	1	0	1	0	
18	0	0	1	1	0	1	0	1	0	-4 V_{DC}
19	0	1	0	1	0	1	0	1	0	-5V_{DC}
20	1	0	0	1	0	1	0	0	1	-6V_{DC}
21	0	0	1	1	0	1	0	0	1	-7 V_{DC}
22	0	1	0	1	0	1	0	0	1	-8 V_{DC}

For cascaded connection of the basic units the dc voltage sources are selected as:

$$V_{DC1,n} = V_{DCn,2} = 1V_{DC} \tag{3}$$

$$V_{DC3,n} = V_{DC4,n} = 3V_{DC} \tag{4}$$

The maximum output voltage for proposed can be expressed as:

$$V_{o,max} = \pm\left(\frac{N_L - 1}{2}\right) \tag{5}$$

Total blocking voltage (TBV) of the power switches is also an essential parameter in deciding the multilevel inverter cost. The inverter topology cost can be reduced by reducing the semiconductor switches' total blocking voltage [27]. The blocking voltage or standing voltage of power device is

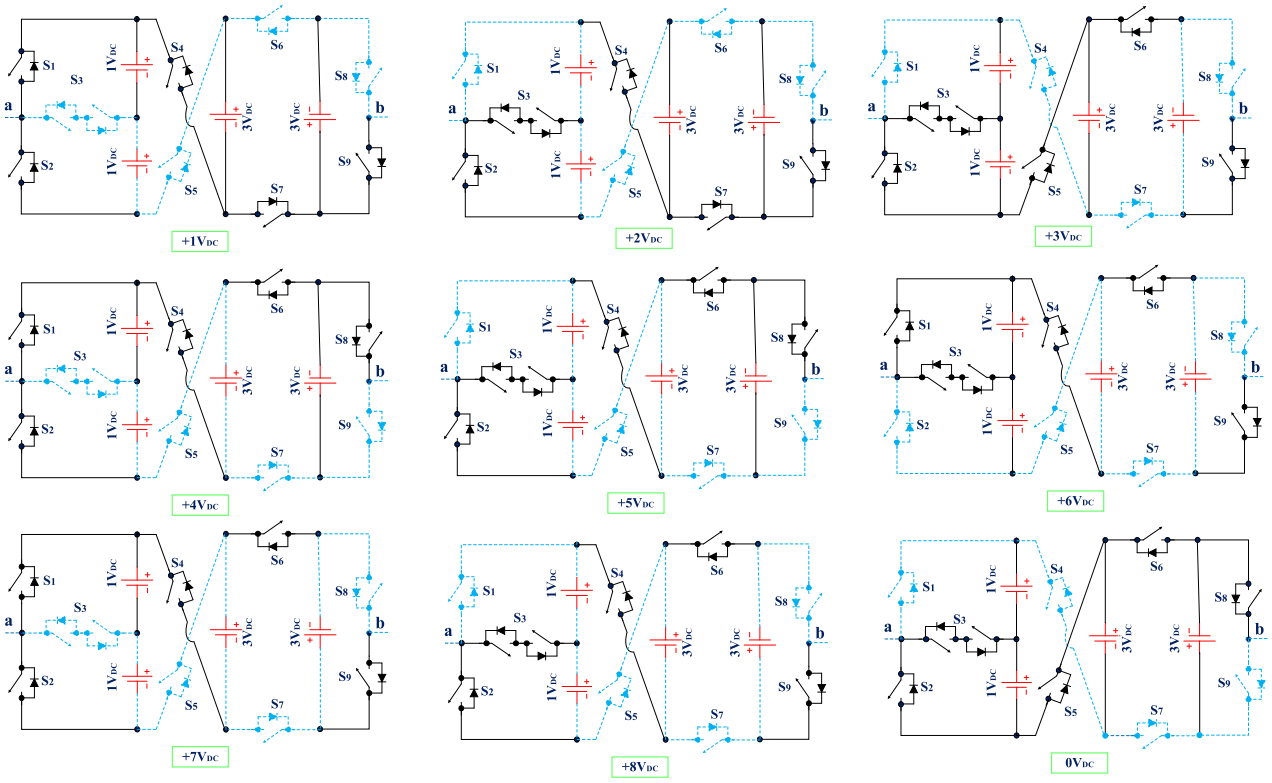

FIGURE 2. Modes of operation during positive half-cycle.

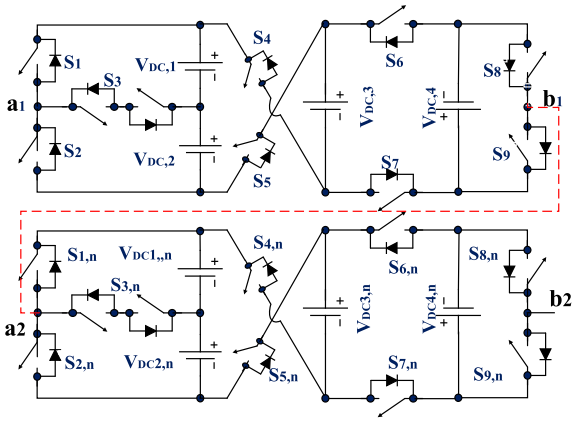

FIGURE 3. Generalized structure of the inverter.

defined as the maximum voltage stress on it during the off state.

TBV calculation is explained from Fig.2, taking the blocking voltage of S_2 as an example. The peak voltage blocking capability of S_2 is determined at $V_o = 2V_{DC}$ or $3V_{DC}$ or $5V_{DC}$ or $8V_{DC}$ or $-6\ V_{DC}$. In all of these voltage levels, S_2 is in the off state. Therefore, $V_{DC,1}$ and $V_{DC,2}$ apply blocking voltage on S_2. Similarly, the peak voltage stress across power switches of the inverter is achieved as follows;

$$V_{S1} = V_{DC,1} + V_{DC,1} = 1V_{DC} + 1V_{DC} = 2V_{DC}$$
$$(\text{At, } V_o = 6V_{DC} \text{ or } -2V_{DC} \text{ or } -3V_{DC})$$

TABLE 2. Various parameters for proposed MLI topologies.

	Parameters	Based on basic units	Based on voltage levels
1	voltage levels	16n+1	N_L
2	power switches	10n	$5(N_L-1)/8$
3	gate-drivers	9n	$9(N_L-1)/16$
4	diodes	10n	$5(N_L-1)/8$
5	dc-links	4n	$(N_L-1)/8$
6	TBV	33n	$2.0625(N_L-1)$

$$V_{S2} = V_{DC,1} + V_{DC,1} = 1V_{DC} + 1V_{DC} = 2V_{DC}$$
$$(\text{At, } V_o = 2V_{DC} \text{ or } 3V_{DC} \text{ or } 5V_{DC} \text{ or } 8V_{DC} \text{ or } -6V_{DC})$$
$$V_{S3} = V_{DC,1} = 1V_{DC}$$
$$(\text{At, } V_o = -3V_{DC} \text{ or } 5V_{DC} \text{ or } 8V_{DC} \text{ or } -6V_{DC})$$
$$V_{S4} = V_{DC,1} + V_{DC,1} + V_{DC,3}$$
$$= 1V_{DC} + 1V_{DC} + 3V_{DC} = 5V_{DC}$$
$$(\text{At, } V_o = 7V_{DC} \text{ or } 8V_{DC})$$
$$V_{S5} = V_{DC,1} + V_{DC,1} + V_{DC,3}$$
$$= 1V_{DC} + 1V_{DC} + 3V_{DC} = 5V_{DC}$$
$$(\text{At, } V_o = -7V_{DC} \text{ or } -8V_{DC})$$
$$V_{S6} = V_{DC,3} + V_{DC,4} = 3V_{DC} + 3V_{DC=}6V_D$$
$$(\text{At, } V_o = 6V_{DC} \text{ or } 7V_{DC} \text{ or } 8V_{DC})$$

$$V_{S7} = V_{DC,3} + V_{DC,4} = 3V_{DC} + 3V_{DC=}6V_D$$
$$(\text{At, } V_o = -6V_{DC} \text{ or } -7V_{DC} \text{ or } -8V_{DC})$$
$$V_{S8} = V_{DC,4} = 3V_{DC}$$
$$(\text{At, } V_o = -1V_{DC} \text{ or } -3V_{DC} \text{ or } 5V_{DC})$$
$$V_{S9} = V_{DC,4} = 3V_{DC}$$
$$(\text{At, } V_o = 1V_{DC} \text{ or } 3V_{DC} \text{ or } -5V_{DC})$$
$$TBV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} + V_{S8} + V_{S9} = 33V_{DC}$$

The power losses of semiconductor switches are the sum of conduction losses and switching losses. The power loss calculation procedure demonstrated in [16] can be conveniently considered for the proposed topology. Conduction losses are defined as the losses due to voltage drop in semiconductor devices when they conduct current during their on-states. Conduction losses are obtained by multiplying $V_{on,y}(t)$ and I(t) of the semiconductor device during on-state.

$$P_{C,y}(t) = V_{on,y}(t) \times I(t) \tag{6}$$

where 'y' is the semiconductor switching device, $V_{on,y}$ (t) is the voltage drop of 'y' in on-state. The I(t) is the current conducting through 'y'. The power loss during on-state can be achieved

$$P_{C,G} = [V_{on,G} + R_{on,G}.I^{\beta}(t)]I(t) \tag{7}$$

$$P_{C,D} = [V_{on,D} + R_{on,D}.I(t)]I(t) \tag{8}$$

Here, 'G' is IGBT, 'D' is an anti-parallel diode and 'β' is a constant factor depending on the specification of IGBT. The $V_{on,G}$ and $V_{on,D}$ are the on-state voltage drops of IGBT and diode. $R_{on,G}$ and $R_{on,D}$ are the on-state resistances of IGBT and anti-parallel diode, respectively. General formula for calculating IGBT and anti-parallel diode average conduction losses is:

$$P_{C,G} = u(t)\left[\frac{1}{2\pi}\int_0^{2\pi} V_{on,G}I + R_{on,G}I^{\beta}(t)\right]d(\omega t) \tag{9}$$

$$P_{C,D} = v(t)\left[\frac{1}{2\pi}\int_0^{2\pi} V_{on,D}\cdot I + R_{on,D}\cdot I^{\beta}(t)\right]d(\omega t) \tag{10}$$

In the above equations, P_C is the total power loss. Here, u(t) is the number of semiconductor switches, and v(t) is the number of anti-parallel diodes in the direction of conducting current path.

Hence, total conduction losses for the proposed inverter can be expressed as

$$P_C = P_{C,G} + P_{C,D} \tag{11}$$

Switching loss in the semiconductor device is the power dissipated during switches turn-on and turn-off states. Switching loss is determined for IGBTs and diodes as follows:

$$E_{on} = f\int_0^{t_{on}} v(t)i(t)d(t) \tag{12}$$

$$E_{on} = f_s\int_0^{t_{on}}\left[\left(\frac{V_{sw}}{t_{on}}t\right)\left(-\frac{t-t_{on}}{t_{on}}I\right)\right]dt = \frac{V_{sw}*I*t_{on}}{6T} \tag{13}$$

$$E_{off} = f_s\int_0^{t_{off}} v(t)i(t)d(t) \tag{14}$$

$$E_{off} = f_s\int_0^{t_{off}}\left[\left(\frac{V_{sw}}{t_{off}}t\right)\left(-\frac{t-t_{off}}{t_{off}}I\right)\right]dt = \frac{V_{sw}*I*t_{off}}{6T} \tag{15}$$

Here, f_s, I, v_{sw}, t_{on}, and t_{off} are the fundamental switching frequency, the current through semiconductor device before turning off and after turning on, the off-state voltage of the device and on-state and off-state of the power devices, respectively.

The total switching loss during one period is:

$$P_{sw} = f_s \times \sum_i^{N_{sw}} (E_{on,i} + E_{off,i}) \tag{16}$$

The total power losses and efficiency of the proposed asymmetric inverter are calculated

$$P_T = P_C + P_{sw} \tag{17}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_T} \tag{18}$$

Here, P_{out} and P_{in} are the output and input power of the inverter.

III. COMPARATIVE STUDY

In this part, a comparison is made to show the superiority of the proposed MLI topology over the traditional inverter structures such as CHBMLIs, FCMLIs, NPCMLIs, and recently introduced reduced component count topologies having similar structures. A comparative analysis is carried out based on voltage levels in terms of semiconductor switches, dc-links, the total standing voltage on switches, sources (N_y) and gate driver circuits. Table 3 shows different parameters in terms of voltage levels for comparison with different MLI topologies.

Power switches are the most dominant part of multilevel inverters. Increasing the count of power switches, the cost and size of the inverter circuit also increases. The increase in the count of power switches thus leads to the complex control of the circuit. Fig. 4(a) compares the count of utilized semiconductor switches for the proposed MLI topology and other topologies. This comparison confirms that the proposed MLI structure uses less amount of semiconductor switches than other topologies. It can reduce the overall system cost and complexity. The number of used switches is smaller in [24], [28], [29] than the proposed topology. Whereas [13], [16] uses H-bridge, the high voltage stress across H-bridge switches increases the total standing voltage. However, the total voltage standing in the proposed inverter topology is less than these topologies. Therefore, the proposed MLI topology's installation space and cost will be reduced compared to other MLIs.

Total blocking voltage (TBV) of the switches for the proposed multilevel inverter is compared in Fig. 4(b), with

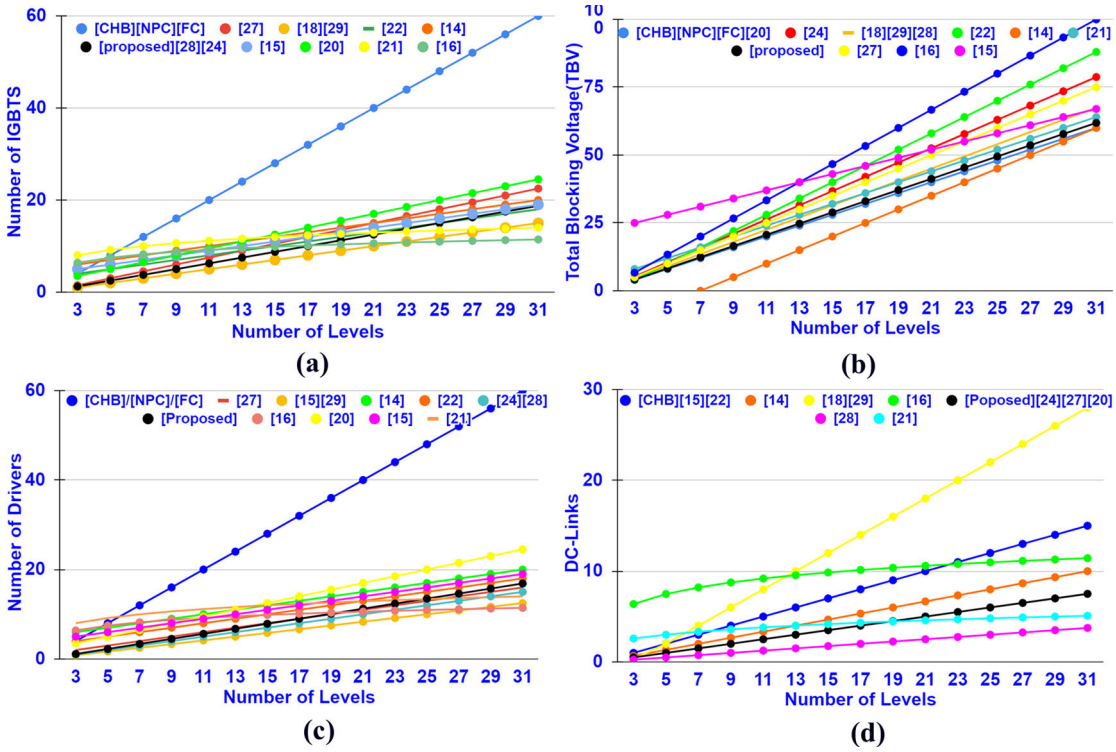

FIGURE 4. Comparison of proposed inverter topology with other topologies, (a) power IGBTs, (b) TBV, (c) gate-driver circuits, (d) DC-Links against the number of levels.

traditional and other recent inverter topologies. It is shallow compared to most topologies, but traditional MLI topologies have small TBV compared to the proposed inverter. However, traditional inverter topologies have a significantly higher number of required switches for generating the same voltage levels than the proposed topology. The proposed inverter requires ten switches and has a standing voltage of $33V_{DC}$ producing 17 voltage levels at the output. The traditional MLIs need 32 switches and have a standing voltage of $32V_{DC}$. There is a minor difference in TBV, but a reduced number of required switches in the proposed topology shows its superiority over other inverter topologies.

From Fig. 4(c), it is evident from the comparison that the proposed topology requires fewer gate drivers than other topologies, as mentioned earlier. As each power switch needs a separate gate driver circuit, the number of gate drivers equals the total number of switches. The number of gate drivers required in topologies [18], [29] is the same as in the proposed topology, but it has high TBV compared to the proposed topology. The use of bidirectional power switches can reduce gate driver circuits, as these switches require only one gate driver circuits. However, the cost of inverter also increases with the increase in gate drivers.

Fig. 4(d) depicts the comparison of the number of dc-links in the proposed MLI topology and other topologies. Neutral point clamped and capacitor clamped MLI topologies uses only one dc-link; therefore, a comparison is made with topologies require more than one dc-links. This comparison confirms that the proposed MLI structure uses less number of dc-links than other topologies. Hence, it can reduce the overall system cost and complexity. The proposed topology uses the same number of dc-links as topologies [19], [24], [27].

As it is clear from the comparison mentioned above, the proposed MLI has good performance compared to the traditional and recently introduced inverter topologies. The comparisons above show the remarkable advantages of the proposed inverter topology in reducing the numbers of required power IGBTs, total blocking voltage of the power switches, diodes, driver circuits, dc-links, and the amount of the blocked voltage by the power switches. These dominant advantages can lead to minimizing the total cost and installation space of the MLI topology.

IV. SIMULATION AND EXPERIMENTAL RESULTS ANALYSIS

The Nearest level Control (NLC) modulation technique [31] is used to generate the switching pulses for gate drivers to drive the power switches. NLC modulation technique is recommended since the number of required voltage levels generated by inverter topology is high. Moreover, the nearest level Control (NLC) method is easy compared with other fundamental switching frequency techniques. Fig.5 shows the NLC method waveform synthesis and control diagram. In this technique, the closest voltage level to the reference voltage (V_{ref}) is first selected. The closest voltage level can be generated by comparing the inverter output voltage with reference sinusoidal voltage (V_{ref}) to produce proper switching signals. Nearest voltage level can be generated using the

TABLE 3. Comparison of proposed inverter topology with other topologies.

References	Switches	Drivers	Diodes	N_v	Dc links	TSV	Negative levels
CHB	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	1	$(N_L-1)/2$	$2(N_L-1)$	With H-Bridge
FC	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	1	1	$2(N_L-1)$	Inherent
NPC	$2(N_L-1)$	$2(N_L-1)$	(N_L+1)	1	1	$2(N_L-1)$	Inherent
2015[18]	$(N_L-1)/2$	$5(N_L-1)/12$	$(N_L-1)/2$	2	$(N_L-1)/6$	$9(N_L-1)/4$	Inherent
[24]2017	$5(N_L-1)/8$	$(N_L-1)/2$	$5(N_L-1)/8$	2	$(N_L-1)/4$	$2.625((N_L-1)$	Inherent
[27] 2017	$3(N_L-1)/4$	$(N_L+1)/2$	$3(N_L-1)/4$	2	$(N_L-1)/4$	$5(N_L-1)/2$	Inherent
[29]2018	$(N_L-1)/2$	$5(N_L-1)/12$	$(N_L-1)/2$	2	$(N_L-1)/6$	$9(N_L-1)/4$	Inherent
[28]2019	$5(N_L-1)/8$	$(N_L-1)/2$	$5(N_L-1)/8$	2	$(N_L-1)/8$	$9(N_L-1)/4$	Inherent
[22]2020	$(N_L+5)/2$	$(N_L+5)/2$	$(N_L-3)/2$	1	$(N_L-1)/2$	$3(N_L-1)-2$	Inherent
[21]2020	$[2\ln(N_L+1)]/\ln 2+2$	$[2\ln(N_L+1)]/\ln 2$	$[2\ln(N_L+1)]/\ln 2$	2	$\ln(N_L+3)/\ln 2$	$2(N_L+1)$	Inherent
[14]2020	$(N_L-1)/2+5$	$(N_L-1)/2+5$	$(N_L-1)/2+5$	1	(N_L-3)	$(5N_L-7)/2$	Inherent
[16]2020	$3[\mathrm{Log}_4^{(NL+1/)}+4]$	$3[\mathrm{Log}_4^{(NL+1/)}+4]$	$6[\mathrm{Log}_4^{(NL+1/)}+4]$	2	$3[\mathrm{Log}_4^{(NL+1/)}+4]$	$20(N_L-1)-6$	With H-Bridge
[20]2020	$3[(N_L-1)/4]+2$	$3[(N_L-1)/4]+2$	$(N_L-1)/4$	1	$(N_L-1)/4$	$2(N_L-1)$	Inherent.
[15] 2020	$[(N_L-1)/2]+4$	$[(N_L-1)/2]+4$	$[(N_L-1)/2]+4$	1	$(N_L-1)/2$	$3[(N_L-1)/2]+22$	With H-Bridge
Proposed	**$5(N_L-1)/8$**	**$9(N_L-1)/16$**	**$5(N_L-1)/8$**	**2**	**$(N_L-1)/4$**	**$2.0625(N_L-1)$**	**Inherent.**

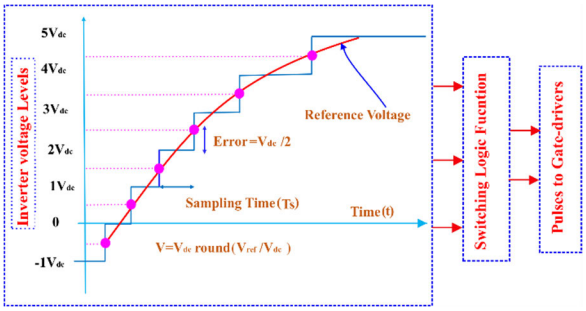

FIGURE 5. Nearest level control waveform synthesis.

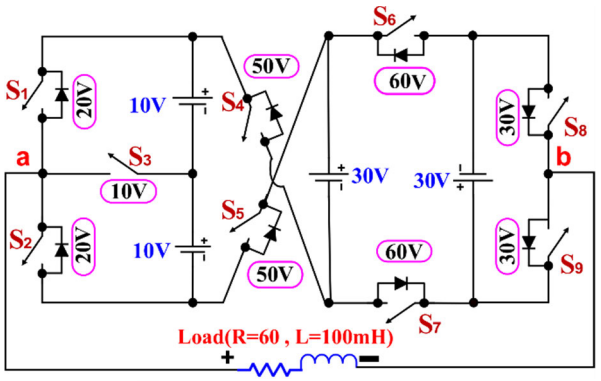

FIGURE 6. Experimental circuit diagram of the 17L inverter topology.

formula as;

$$\text{Nearest voltage level} = \frac{1}{V_{DC}} \times \text{round}(V_{ref}) \qquad (19)$$

Here, V_{DC} represents the voltage difference between the two levels. So, the round function is applied to this value to determine the VDC's integer's closest value. Finally, these values are compared with their associated levels. Table 1. NLC technique can generate low THD for the same number of output voltage levels and low switching losses due to low commutations per cycle. This method's main drawback is that it cannot be used with low levels because it cannot eliminate specific harmonics. Hence it is preferable to use this method in inverters with the increased number of voltage levels.

The performance of the inverter is examined with a laboratory prototype, as shown in Fig. 6. For the seventeen-level asymmetrical configuration simulation, the input dc sources used are $V_{DC,1} = V_{DC,2} = 10V$, and $V_{DC,3} = V_{DC,4} = 30V$. Fig.7 depicts the voltage and current waveforms at inductive-load (R = 60Ω, L = 100mH) and their corresponding harmonics spectrum. THD is 2.77% for output voltage, and output current is 0.70%, as shown in Fig. 8. The harmonics spectrum of voltage proved that each harmonic present's magnitude is below 5%, which meets IEEE519 standards (the total THD magnitude should be equal to or less than 7% and the THD magnitude of order harmonic should be equal to or less than 5%).

Experimental tests have been conducted, and results are obtained for a 17-level prototype to validate the simulation results. The experimental setup of 17-level of proposed MLI is shown in Fig. 9. The real-time interface controller dSPACE-DS1104 has been used for hardware implementation to generate switching signals, as shown in Fig.10.

IGBTs IRGP35B60PDPBF (with a built-in internal diode) models are used as semiconductor switches. In the laboratory

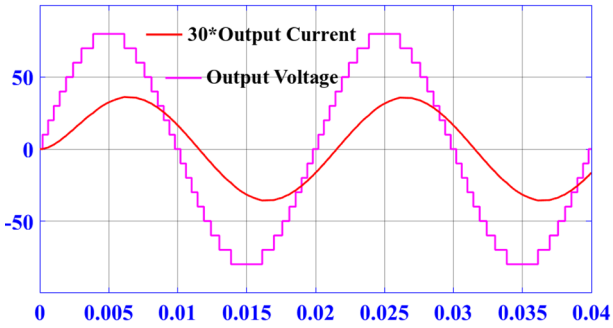

FIGURE 7. Simulation results for 17-level inverter with load (R = 60Ω, L = 100mH), (a) Output voltage, (b) Output current.

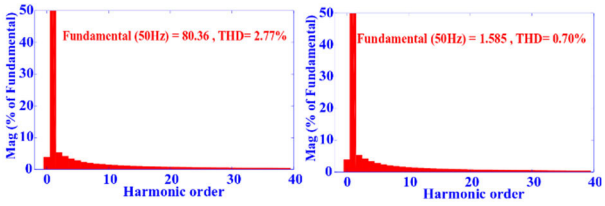

FIGURE 8. Harmonic spectrums (a), Voltage harmonic spectrum, (c) Current harmonic spectrum.

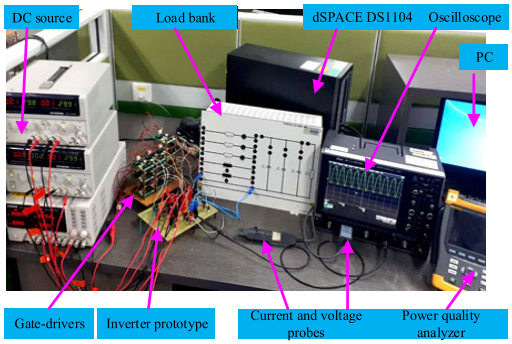

FIGURE 9. Experimental prototype 17-level inverter.

FIGURE 10. Switching pulses for IGBTS.

setup, the adjustable dc power supplies have been used as input sources. A magnitude of $V_{DC,1} = V_{DC,2} = 10V$, and $V_{DC,3} = V_{DC,4} = 30V$ are selected for 17-level inverter operation the load values considered are R = 35Ω and

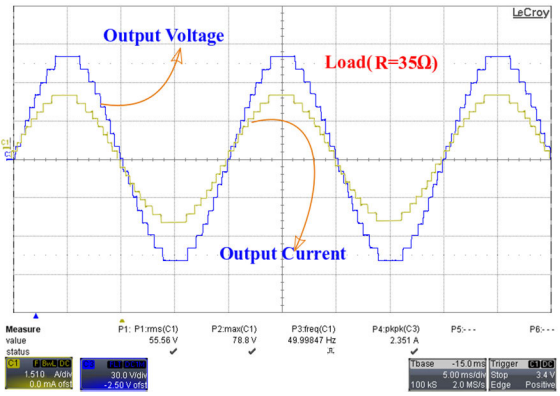

FIGURE 11. Experimental results for a 17-level inverter with load (R = 35Ω) (a) Output voltage, (b) Output current.

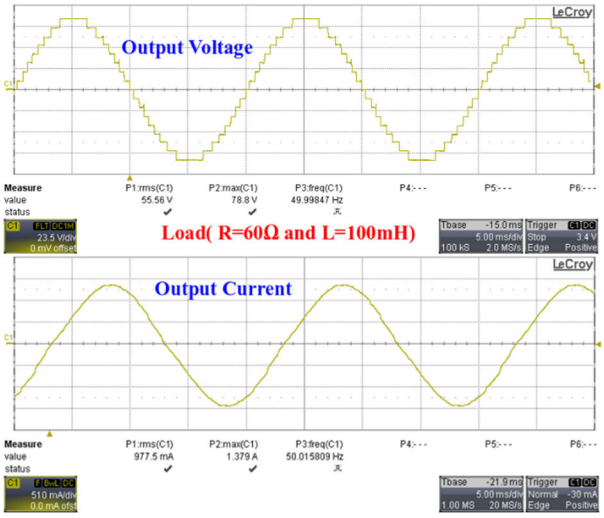

FIGURE 12. Experimental results for 17-level inverter with load (R = 60Ω, L = 100mH) (a) Output voltage, (b) Output current.

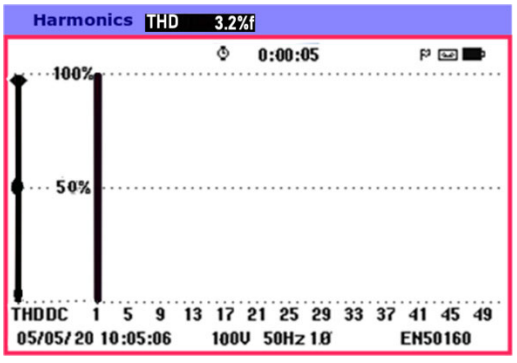

FIGURE 13. Output Voltage harmonic spectrum.

(R = 60 Ω, L = 100mH). The voltage and current waveforms at pure resistive load are shown in Fig.11. While, Fig.12 illustrates the voltage and current waveforms of the proposed 17-level with inductive load at 50 Hz, and the frequency spectrum is shown in Fig. 13. Voltage waveform THD is 3.2%, and output current waveform THD is 0.4%. The RMS value of output voltage is 55.46 V, and the current is 0.9 A. Maximum amplitude of the voltage is 78.9 V, and the current is 1.38 A. The 'Y' axis of voltage is 23.5V/div,

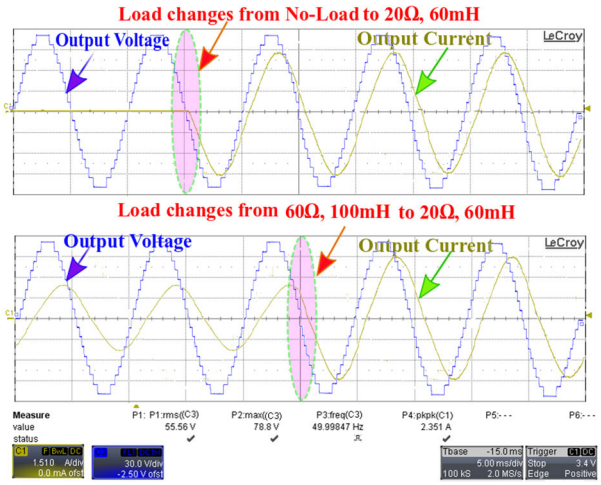

FIGURE 14. Transient-state response with change of load from,(a) No-load to R = 20 Ω, L = 60mH. (b) R = 60 Ω, L = 100mH to R = 20 Ω, L = 60mH.

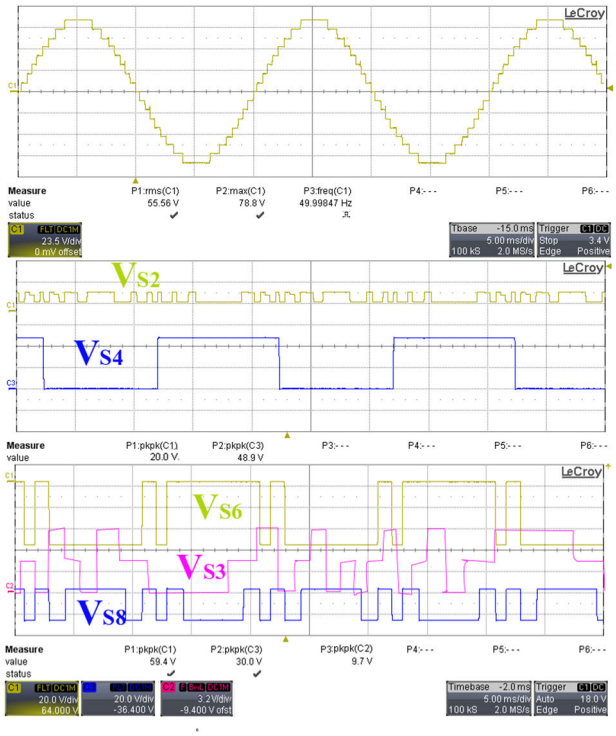

FIGURE 15. Experimental Blocking voltages across power IGBTs.

'Y' axis of the current waveform is 510mA/div, and the 'X' axis is 50Hz per cycle.

Further, the transient response of the inverter is tested with sudden load variations. Fig. 14 depicts the sudden load variations from no-load to (20Ω, 60mH) and from (60Ω, 100mH) to (20Ω, 60mH). The load current gradually changes as the load changes. In both cases, it is clear from the experimental results that the proposed topology keeps each output voltage level unchanged and remains in steady-state. Fig. 15 shows the voltage stress across different switches of the inverter. The blocking voltage (voltage stress) of switches S_6 and S_7 is 60V. The pattern of blocking voltage waveform of switches

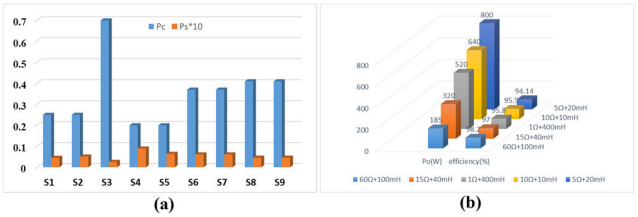

FIGURE 16. Power loss analysis (a) power loss distribution (b) efficiency with different loading conditions.

S_1 and S_2 with magnitude 20V. The least blocking voltage across bidirectional power switch S_3 is 10V. The voltage stress across power switches (S_3, S_4) and (S_8, S_9) is 50V and 30V, respectively. The proposed inverter's power losses and efficiency are determined numerically based on experimental results at different output powers, as shown in Fig.16. The parameters considered for power loss calculation are; V_{SW} = 1.85 V, R_{SW} = 84mΩ, V_{DF} = 1.3V, R_D = 4.3mΩ, t_{on} = 8ns, t_{off} = 130ns, β = 1. It should be noted that IRGP35B60PDPBF_IGBTs are used for power loss calculations. The conduction and switching losses in the topology are calculated for each switch. From that, the cumulative loss for all the switches is obtained. The conduction and switching losses loss obtained using (9) and (16) are 0.089 W and 3.16 W, respectively. Hence, the total power loss is equal to 3.25 W. To investigate the feasibility of proposed inverter; the power loss analysis is performed at various power loads such as 185W, 360W, 734W as depicted in Fig. 16(b). The peak efficiency is 98.2% at load voltage of 78.8 V and power load of 185 W. The inverter efficiency drop is due to higher conduction losses (I^2r losses) in the inverter's different elements.

V. CONCLUSION

This research work proposed a new single-phase MLI topology. The primary objective of introducing the proposed MLI is to use reduced power electronics components to produce higher voltage levels with low voltage rated power switches. The topology can generate seventeen voltage levels under asymmetric source configuration. The inverter topology can be connected in cascade to increase voltage steps with lower power components and lower voltage stress on power components. The proposed inverter's main feature is that it can generate all voltage steps without utilizing an H-bridge inverter. Therefore, semiconductor components having low voltage ratings can be utilized in this topology and make it very suitable for higher voltage applications. The proposed topology is also compared with traditional MLIs and other recently introduced MLIs in terms of the number of power switches, total blocking voltage, dc-links, and the number of gate driver's circuits to show its performance. The comparative study shows that this MLI topology uses fewer power switches than other topologies and low voltage-rated switches. Simulation and prototype results validate the feasibility of the proposed MLI circuit

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