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WORD COUNT 4903
TIME SUBMITTED 23-SEP-2021 11:59AM
PAPER ID 76940838

International Journal of Electrical and Computer Engineering (IJECE)
Vol. 10, No. 4, August 2020, pp. 3988~3998
ISSN: 2088-8708, DOI: 10.11591/ijece.v10i4.pp3988-3998

Dual output DC-DC quasi impedance source converter

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Article Info

Article history:

Received Jan 30, 2020
Revised Mar 5, 2020
Accepted Mar 15, 2020

Keywords:

Bidirectional
Buck-boost converters
Converters
Double output
Quasi-Z-source
Z-source

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ABSTRACT

A double output port DC-DC quasi impedance source converter (q-ZSC) is proposed. Each of the outputs has a different voltage gain. One of the outputs is capable of bidirectional (four-quadrant) operation by only varying the duty ratio. The second output has the gain of traditional two-switch buck-boost converter. Operation of the converter was verified by simulating its responses for different input voltages and duty ratios using MATLAB SIMULINK software. Its average steady-state output current and voltage values were determined and used to determine the ripples that existed. These ripples are less than 5% of the average steady-state values for all the input voltage and duty ratio ranges considered.

1. INTRODUCTION

Use of renewable-energy (RE) generation systems has been dramatically increasing due to environmental effects and the exhaustion of fossil fuels [1]. The major RE sources are photovoltaic (PV) energy, wind power, and fuel cells (FC). The outputs of these RE sources are unregulated, thus require power converters such as DC-DC converters for regulation [2–8]. Functions of these DC-DC converters include regulating the variable output voltages to a given set point to charge the energy storage systems (ESSs) [4], charging and discharging of batteries or other energy storage systems (ESSs) [9], stepping up/down of voltages in fuel cell electric vehicles (FCEVs) [5] and powering DC loads or inverters.

Impedance source converters (ISCs or ZSCs) [10] are types of power converters capable of AC-AC, AC-DC, DC-AC and DC-DC conversion. They couple converter's main circuit by using an impedance network to its input power source and provide other exclusive features [11, 12]. ISCs permit shoot-through (ST) in voltage-fed ISCs without causing over-current for voltage boosting by allowing short-circuiting of their output terminal [13]. They permit open-circuit (OC) in current-fed ISCs by allowing interruption of current for current boosting without causing over-voltage [14]. Turning ON switches of a H-bridge's common leg simultaneously results in ST while turning them ON triggers OC [6].

Inductors are used during ST to store energy that is released later during other modes [15]. ISCs are robust because they could be controlled by PWM signals with or without OC and/or ST modes. Q-ZSCs [16] are class of ISCs obtained by swapping switches and inductors to remedy some limitations of ZSCs. However,

limitations like discontinuous input current and high voltage stress on switches are still common in some q-ZSC topologies. Incorporating OC modes into the switching signals could reduce switching stress [3].

Q-ZSC application was extended to DC-DC application by taking the output across one of the capacitors [17]. However, [18–20] took their outputs across a switch in what is called pulse-width modulated DC-DC ISCs. M. Ado et al [11] and [21] later proposed additional topology each to form an additional class [22]. M. Ado et al [23] extended the family of DC-DC q-ZSCs from two classes to three and from four members to six. Each of the classes has two members and a unique voltage gain. Although some of the proposed topologies are capable of four-quadrant (bidirectional) energy transfer, they all have single input and single output (SISO) voltages.

This paper presents a DC-DC q-ZSC topology with a single input voltage source and dual output voltage ports as shown in Figure 1. The two outputs have different voltage gains. The significance of having different voltage gains is that two different output voltages could be obtained simultaneously. The operation of the proposed converter was verified by simulating its response in MATLAB SIMULINK. The verification involved simulating its response at different input voltages (V_g) and duty ratios (D). The average steady-state output current (I_O) and voltages (V_O) of each simulation was determined and analyzed. Ripple ratios for these average voltages and currents were determined and compared with theoretical values. The comparison showed that the average voltages were above 89% of the theoretical values.

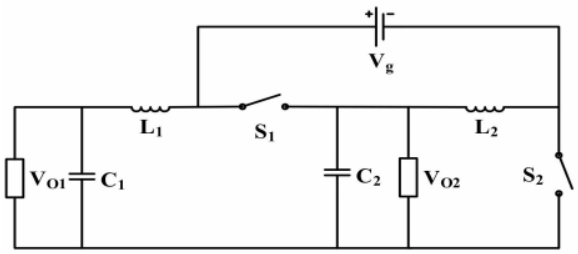


Figure 1. Topology of proposed converter

2. CIRCUIT ANALYSIS

For easy analysis, the circuit is operated based on two operating modes. The modes are obtained by complementary switching of the converter's switches S_1 and S_2.

2.1. Mode I

During this operating mode, S_1 is turned ON while S_2 is turned OFF as shown in Figure 2a. The circuit equations during this mode are:

$$V_{L1} = V_{C2} - V_{C1} \tag{1}$$

$$V_{L2} = V_g \tag{2}$$

2.2. Mode II

During this operating mode, S_1 is turned OFF while S_2 is turned ON as shown in Figure 2b. The circuit equations during this mode are:

$$V_{L1} = V_g - V_{C1} \tag{3}$$

$$V_{L2} = V_{O2} \tag{4}$$

Applying volt-second balance on L_1 yields

$$DV_{C2} - DV_{C1} + V_g - V_{C1} - DV_g + DV_{C1} = 0 \tag{5}$$

Applying volt-second balance on L_2 yields

$$DV_g + V_{C2}(1-D) = 0 \tag{6}$$

Simplifying (6) shows that

$$V_{C2} = -\frac{D}{1-D}V_g \tag{7}$$

Substituting (7) into (5) and simplifying yields

$$V_{C1} = \frac{1-2D}{1-D} \tag{8}$$

From Figure 1, V_{O1} is in parallel with C_1, thus

$$V_{C1} = V_{O1} \tag{9}$$

Also from Figure 1, V_{O2} is in parallel with C_2, thus

$$V_{C2} = V_{O2} \tag{10}$$

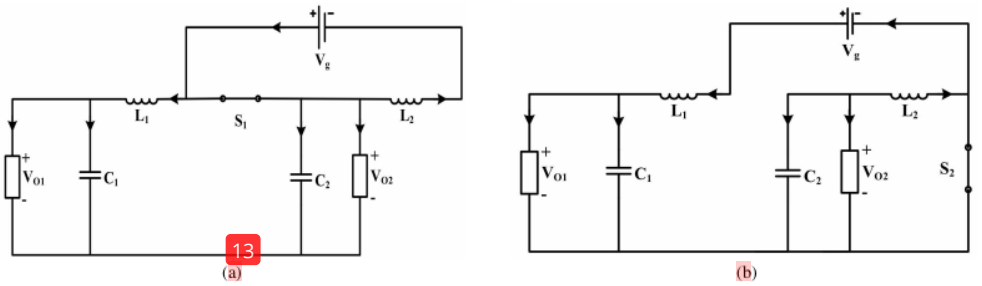


Figure 2. Equivalent circuit of the proposed converter during (a) mode I, (b) Mode II

2.3. First output (V_{O1})

The expression for V_{O1} is obtained by substituting (9) into (8) as

$$V_{O1} = \frac{1-2D}{1-D} \times V_g \tag{11}$$

The gain of this output is

$$A_1 = \frac{V_{O1}}{V_g} = \frac{1-2D}{1-D} \tag{12}$$

2.4. Second output (V_{O2})

The expression for V_{O2} is obtained by substituting (10) into (7) as

$$V_{O2} = \frac{-D}{1-D} \times V_g \tag{13}$$

The gain of this output is

$$A_2 = \frac{V_{O2}}{V_g} = \frac{-D}{1-D} \tag{14}$$

A plot comparing the two different outputs of the converter V_{O1} and V_{O2} against duty ratio (D) is shown in Figure 3. The following can be deduced from Figure 3:

(a) Both the two outputs are capable of stepping up (boosting) or stepping down (bucking) the input voltage as D is varied from 0 to 1. However, the buck operation in V_{O2} is inverted.
(b) As D is varied from 0 to 0.5, the two outputs are less than or equal to the input voltage magnitude
(c) For V_{O2}, varying the output from 0.5 to 1 results in boost operation
(d) For V_{O1}, varying D from 0.5 to 0.667 results in inverted buck (stepping down) operation before achieving inverted boost operation from 0.667 to 1
(e) Two different buck operations could be achieved from V_{O1} namely: positive buck (from D = 0 to 0.5) and negative buck (from D = 0.667 to 1)
(f) The positive and negative buck operation implies bidirectional buck capability [23, 17]. The bidirectional buck capability means that during the negative buck, energy is transferred from source to V_{O1} while during the positive buck, it could be transferred from V_{O1} to source [17] at lower voltage magnitude.

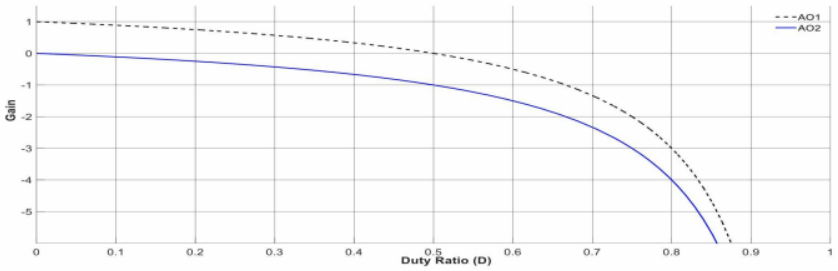


Figure 3. Comparison of voltage gains of the converter's two outputs against duty ratio (D)

3. VERIFICATION

Operation of the converter was verified by simulating a specifically designed prototype using MATLAB SIMULINK.

3.1. Components selection

The design equations of DC-DC q-ZSC derived in [24] and presented here as (15) through (18) were used to determine the components values for a prototype. The specifications for the prototype are given in Table 1.

$$C_1 = \frac{D(1-D)I_O}{V_\Delta(1-2D)fV_g} \tag{15}$$

Where I_O is the output current, f is the minimum operating frequency, V_Δ is the voltage ripple ratio, V_g is the input voltage.

$$C_2 = \frac{2(1-D)I_O}{V_\Delta f V_g} \tag{16}$$

$$L_1 = \frac{DV_g}{fI_\Delta I_O} \tag{17}$$

Where I_Δ is the current ripple ratio.

$$L_2 = \frac{D(D-1)V_g}{f(D+1)I_\Delta I_O} \tag{18}$$

Table 1. Design specifications

Parameter	Minimum	Maximum
Input Voltage (V_g)	10 V	15 V
Output Current (I_O)	0.4 A	2 A
Switching Frequency (f)	100 kHz	
Max Duty Ratio (D)	0.7	

3.2. Component values

3.2.1. Capacitor 1 (C_1)

$$C_1 = \frac{D_{max}(1 - D_{max})I_{O,max}}{(1 - 2D_{max})f_{min}V_{\Delta}V_{g,min}} \tag{19}$$

$I_{O,max}$ is the maximum output current, f_{min} is the minimum frequency, V_{Δ} is the voltage ripple ratio, $V_{g,min}$ is the minimum input voltage.

$$C_1 = \frac{0.72 \times (1 - 0.72) \times 2}{1 - (2 \times 0.72) \times 100 \times 10^3 \times 0.2 \times 10} F = 4.52\ \mu F \tag{20}$$

3.2.2. Capacitor 2 (C_2)

$$C_2 = \frac{2(1 - D_{max})I_{O,max}}{f_{min}V_{\Delta}V_{g,min}} \tag{21}$$

$$C_2 = \frac{2 \times (1 - 0.72) \times 2}{100 \times 10^3 \times 0.2 \times 10} F = 5.6\ \mu F \tag{22}$$

$$L_1 = \frac{D_{max}V_{g,max}}{f_{min}I_{\Delta}I_{O,min}} \tag{23}$$

Where $V_{g,max}$ is the maximum input voltage, I_{Δ} is the current ripple ratio and $I_{O,min}$ is the minimum output current.

$$L_1 = \frac{0.72 \times 15}{100 \times 10^3 \times 0.2 \times 0.4} H = 1.35\ mH \tag{24}$$

$$L_2 = \frac{D_{max}(1 - D_{max})V_{g,max}}{(D_{max} + 1)f_{min}I_{\Delta}I_{O,min}} \tag{25}$$

$$L_2 = \frac{0.72 \times (1 - 0.72) \times 15}{(0.72 + 1) \times 100 \times 10^3 \times 0.2 \times 0.4} H = 87.9\ \mu H \tag{26}$$

The components values found in (20), (22), (24) and (26) implies the use of asymmetric components [25, 6, 3]

3.3. Simulations and methods

The components values obtained in (20), (22), (24) and (26) as shown in Table 2 were used to simulate the response of the proposed converter. This simulation was in order to verify the ideal operation of the converter. Thus, ideal components were used and parasitic resistances were neglected.

A load with resistance of 20 Ω was connected to the first output (output 1) to consume a voltage V_{O1}. Also, another load with resistance of 20 Ω was connected to the second output (output 2) to consume a voltage V_{O2} as shown in Figure 1. To analyze the response of the converter at various input voltages (V_g) and duty ratios (D), parametric sweep of V_g and D for 10 V ≤ V_g ≤ 15 V with step size of 1 V and 0 ≤ D ≤ 0.7 with step size of 0.1 respectively. This implies that the converter's response was simulated for all possible operating voltages and duty ratios based on the design specifications and step size.

Some selected steady-state responses of the converter at minimum and maximum input voltages and duty ratios are shown in Figure 4a through Figure 5b. Since steady-state values of DC-DC converters contain

ripples that are dependent of switching frequency and values of the reactive components due to charging and discharging, average values of the converter's steady-state output voltages and currents V_{O1}, V_{O2}, I_{O1} and I_{O2} for every given V_g and D were determined. Plots of these average output voltages and currents against D are shown in Figure 6a and 6b respectively.

The ripples in the output voltages and currents determined using Equation (27) where A is the voltage or current, $A_\Delta(\%)$ is the ripple ratio in percentage, A_{max} is the steady-state maximum value of the signal, A_{min} is its minimum and A_{av} is its average value.

$$A_\Delta(\%) = \frac{A_{max} - A_{min}}{2 \times A_{av}} \times 100 \tag{27}$$

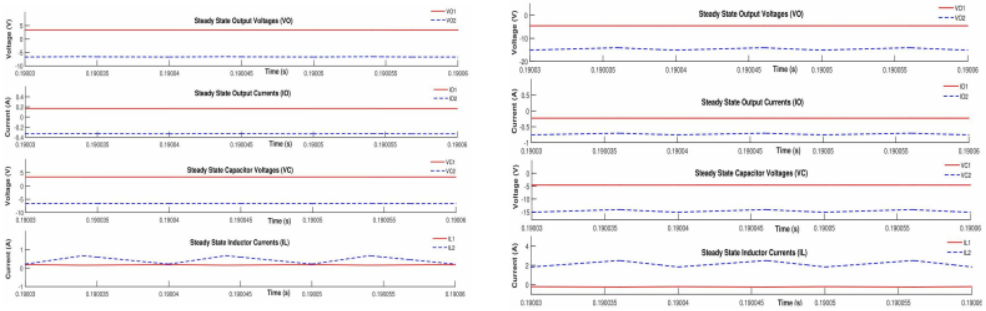
The values of output voltages and currents along with their ripple values $V_{O1\Delta}(\%)$, $V_{O2\Delta}(\%)$, $I_{O1\Delta}(\%)$ and $I_{O2\Delta}(\%)$ for 10 V $\leq V_g \leq$ 15 V and $0.3 \leq D \leq 0.7$ are presented in Table 3 through Table 8. $0.3 \leq D \leq 0.7$ was considered because the efficiency of complementary switched converters reduces when operated outside this range [22, 12, 19]. A significance of the the ripple ratio is to measure the appositeness of the adapted design equations. This is because very low ripple indicates overvalue while very high ripple indicates undervalue of reactive component.

Table 2. Summary of components values

Component	Value	Unit
C_1	4.52	μF
C_2	5.6	μF
L_1	1350	μH
L_2	87.9	μH
R_{O1}	20	Ω
R_{O2}	20	Ω

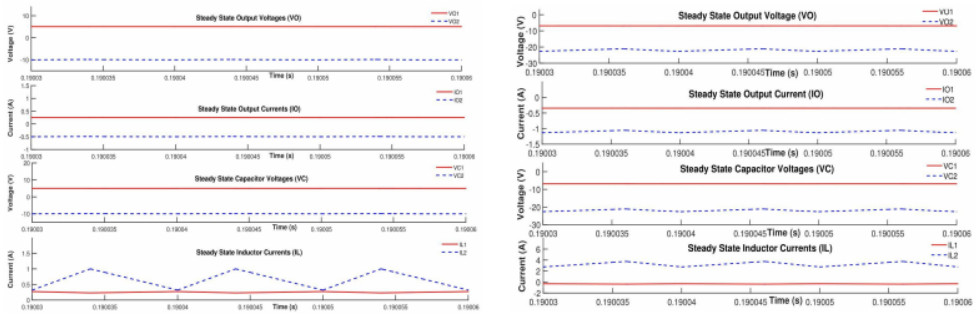
4. RESULTS AND DISCUSSION

Results of the proposed converter's response for some selected steady-state responses of the converter at minimum and maximum input voltages and duty ratios are shown in Figure 4a through Figure 5b. Figure 4a and Figure 4b both show its response at $V_g = 10$ but $D = 0.4$ and 0.6 respectively while Figure 5a and Figure 5b both show its response at $V_g = 15$ but $D = 0.4$ and 0.6 respectively. Table 3, 4, 5, 6, 7 and Table 8 show the average output voltages and currents along with their percentage ripples.



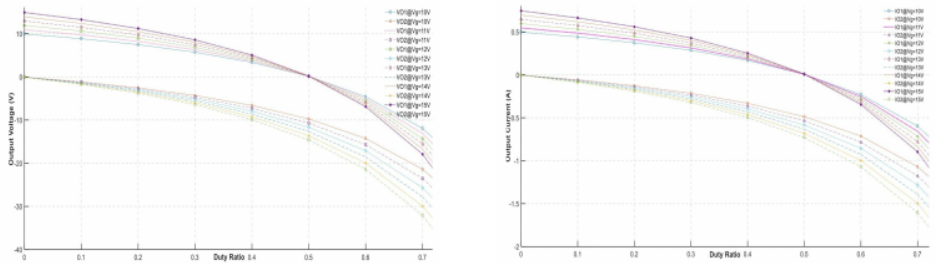
(a) (b)

Figure 4. Steady state simulation response of the proposed converter showing output and capacitor voltages, output and inductor currents for (a) $V_g = 10$ V and $D = 0.4$ (b) $V_g = 10$ V and $D = 0.6$



(a) (b)

Figure 5. Steady state simulation response of the proposed converter showing output and capacitor voltages, output and inductor currents for (a) $V_g = 15$ V and D = 0.4 (b) $V_g = 15$ V and D = 0.6



(a) (b)

Figure 6. Plots of the proposed converter's steady state average (a) Output voltages against duty ratio for different input voltages (b) Output currents against duty ratio for different input voltages

Table 3. Average output voltages and currents of the proposed converter with their percentage ripples at $V_g = 10$ V with D varied from 0.3 to 0.7

$V_g = 10$ V								
D	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	$V_{1\Delta}(\%)$	$V_{2\Delta}(\%)$	$I_{1\Delta}(\%)$	$I_{2\Delta}(\%)$
0.3	5.714	-4.2822	0.2857	-0.2141	0.0465	-0.8322	0.0465	-0.8322
0.4	3.3671	-6.6146	0.1684	-0.3307	0.0444	-0.9026	0.0444	-0.9026
0.5	0.1266	-9.7351	0.0063	-0.4868	3.9975	-2.2408	3.9975	-2.2408
0.6	-4.5964	-14.266	-0.2298	-0.7133	-0.0994	-3.6016	-0.0994	-3.6016
0.7	-11.942	-21.393	-0.5971	-1.0697	-0.0420	-4.9488	-0.0420	-4.9488

Table 4. Average output voltages and currents of the proposed converter with their percentage ripples at $V_g = 11$ V with D varied from 0.3 to 0.7

$V_g = 11$ V								
D	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	$V_{1\Delta}(\%)$	$V_{2\Delta}(\%)$	$I_{1\Delta}(\%)$	$I_{2\Delta}(\%)$
0.3	6.2853	-4.7104	0.31426	-0.2355	0.0465	-0.8322	0.0465	-0.8322
0.4	3.7038	-7.2761	0.1852	-0.3638	0.0444	-0.9026	0.0443	-0.9026
0.5	0.1392	-10.71	0.0070	-0.5355	3.9987	-2.2405	3.9987	-2.2405
0.6	-5.0561	-15.693	-0.2528	-0.7846	-0.0994	-3.6016	-0.0994	-3.6016
0.7	-13.136	-23.532	-0.6568	-1.1766	-0.0420	-4.9488	-0.0420	-4.9488

Table 5. Average output voltages and currents of the proposed converter with their percentage ripples at $V_g = 12$ V with D varied from 0.3 to 0.7

	V_g = 12 V							
D	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	$V_{1\Delta}(\%)$	$V_{2\Delta}(\%)$	$I_{1\Delta}(\%)$	$I_{2\Delta}(\%)$
0.3	6.8567	-5.1389	0.3428	-0.2569	0.0465	-0.8322	0.0465	-0.8322
0.4	4.0405	-7.9376	0.2020	-0.3969	0.0444	-0.9026	0.0443	-0.9026
0.5	0.1518	-11.684	0.0076	-0.5842	3.9987	-2.2405	3.9987	-2.2405
0.6	-5.5157	-17.119	-0.2758	-0.8560	-0.0994	-3.6016	-0.0994	-3.6016
0.7	-14.33	-25.672	-0.7165	-1.2836	-0.0420	-4.9488	-0.0420	-4.9488

Table 6. Average output voltages and currents of the proposed converter with their percentage ripples at $V_g = 13$ V with D varied from 0.3 to 0.7

	V_g = 13 V							
D	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	$V_{1\Delta}(\%)$	$V_{2\Delta}(\%)$	$I_{1\Delta}(\%)$	$I_{2\Delta}(\%)$
0.3	7.4282	-5.5669	0.3714	-0.2783	0.0464	-0.8323	0.0464	-0.8323
0.4	4.3772	-8.599	0.2187	-0.4300	0.0444	-0.9026	0.0444	-0.9026
0.5	0.1645	-12.658	0.0082	-0.6329	3.9987	-2.2405	3.9987	-2.2405
0.6	-5.9754	-18.546	-0.2998	-0.9273	-0.0994	-3.6016	-0.0994	-3.6016
0.7	-15.525	-27.811	-0.7762	-1.3906	-0.0420	-4.9488	-0.0420	-4.9488

Table 7. Average output voltages and currents of the proposed converter with their percentage ripples at $V_g = 14$ V with D varied from 0.3 to 0.7

	V_g = 14 V							
D	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	$V_{1\Delta}(\%)$	$V_{2\Delta}(\%)$	$I_{1\Delta}(\%)$	$I_{2\Delta}(\%)$
0.3	7.9997	-5.9951	0.4000	-0.2998	0.0464	-0.8322	0.0464	-0.83217
0.4	4.7139	-9.2605	0.2357	-0.4630	0.0443	-0.9026	0.0443	-0.9026
0.5	0.1772	-13.629	0.0089	-0.6815	3.9975	-2.2408	3.9975	-2.2408
0.6	-6.435	-19.973	-0.3218	-0.9986	-0.0994	-3.6016	-0.0994	-3.6016
0.7	-16.719	-29.95	-0.8360	-1.4975	-0.0420	-4.9488	-0.0420	-4.9488

Table 8. Average output voltages and currents and their percentage ripples of the proposed converter at $V_g = 15$ V with D varied from 0.3 to 0.7

	V_g = 15 V							
D	V_{01} (V)	V_{02} (V)	I_{01} (A)	I_{02} (A)	$V_{1\Delta}(\%)$	$V_{2\Delta}(\%)$	$I_{1\Delta}(\%)$	$I_{2\Delta}(\%)$
0.3	8.5711	-6.4233	0.4286	-0.3212	0.0465	-0.8323	0.0465	-0.8323
0.4	5.0506	-9.922	0.2525	-0.4961	0.0444	-0.9026	0.0444	-0.9026
0.5	0.19	-14.603	0.0095	-0.7301	3.9975	-2.2408	3.9975	-2.2408
0.6	-6.8947	-21.399	-0.3447	-1.07	-0.0994	-3.6016	-0.0994	-3.6016
0.7	-17.913	-32.09	-0.8957	-1.6045	-0.0420	-4.9488	-0.0420	-4.9488

Plots of these average output voltages and currents against D are shown in Figure 6a and 6b respectively. Results of Figure 4a through Figure 5b confirmed the operation of the proposed converter. As presented in [17], the output voltage and current of port 1 (V_{O1} and I_{O1} are bipolar; positive for $D < 0.5$ and inverted for $D > 0.5$). This is captured in (9), with the V_{O1} expected to be null at $D = 0.5$. However as shown in Table 3 through Table 8, V_{O1} at $D = 0.5$ is slightly greater than 0 (zero) with its magnitude proportional to the V_g as shown in Figure 7. All these values are 1.27 % of the corresponding V_g.

The ripples for output port 1 ($V_{1\Delta}(\%)$ and $I_{1\Delta}(\%)$) presented in Table 3 through Table 8 are minimal except at D = 0.5, where it is maximum at 4 % due to the ideal 0 (zero) output. The ripples for output port 2 are significantly higher than the corresponding ones for output 1. Reasons for the wide variation in the ripple ratio are:

(a) The design equations used to determine the components values are not specifically derived for the proposed converter but for a related topology with a single output in which the output was taken from port 2.
(b) The components used for C_1 and L_1 are oversized because the design equations were not specifically derived for this converter.

The plots of average output voltages and currents of the proposed converter's simulation responses against duty ratio for different input voltages shown in Figure 6a and Figure 6b respectively show that the shape of the plot is identical with the theoretical gain curve of the converter shown in Figure 3. The average output voltages of output port 1 are about 89.56% to 101% of the theoretical value for $0.3 \leq \mathrm{D} \leq 0.7$ except at $\mathrm{V_g} = 15$ V where it is 96% to 108.2%. For port 2, $\mathrm{V_{O2}}$ is 91.7% to 99.9% of the theoretical value with the ratio proportional to D. It is important to note that in some cases the simulation output for some parameters are above or very close to the theoretical ideal values as seen above. This is due to the effect of dead-time/OC that exists in the switching signal [6].

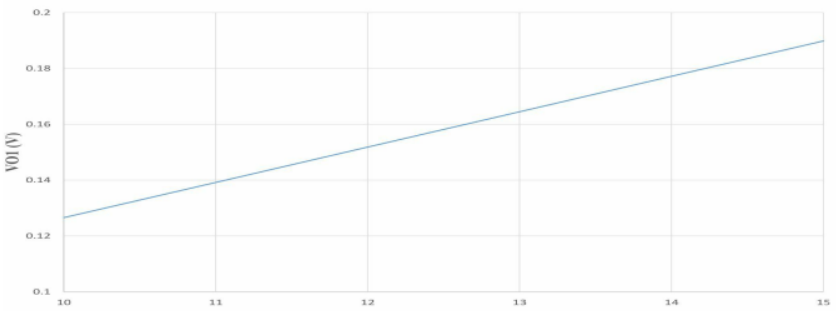


Figure 7. Plot of $\mathrm{V_{O1}}$ at $\mathrm{D} = 0.5$ against $\mathrm{V_g}$

5. CONCLUSION

A q-ZSC with two outputs has been proposed. The gain of each output has been derived. The operations of the converter was simulated at different input voltages and duty ratios using MATLAB SIMULINK. The average steady-state output current and voltages of each simulation was determined, analyzed and their ripple ratios determined. Comparison of the average output voltages of the two outputs show agreement with the theoretical outputs given by their ideal gain equations. The ripples present in all the outputs of the proposed converter were lower than 5%.

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