Alexandria Engineering Journal (2021) 60, 1067–1083

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Development of Modular DC-DC Converters for Low-Speed Electric Vehicles Fast Chargers

Mena ElMenshawy [a,*], Ahmed Massoud [b]

[a] Department of Electrical Engineering, Qatar University, Doha 2713, Qatar
[b] Department of Electrical Engineering, Qatar University, Doha 2713, Qatar

Received 5 May 2020; revised 16 July 2020; accepted 7 October 2020
Available online 10 November 2020

KEYWORDS

Dual Active Bridge;
Full-Bridge;
Input-Series Input-Parallel Output-Series Output-Parallel Multimodule Converters;
Fast Charging;
Output Current Sharing;
Input Voltage Sharing;
Reflex Charging

Abstract To increase the utilization of Low-Speed Electric Vehicles (LS-EVs), rapid recharging of the EV's battery pack turn out to be essential. This permits reduced charging times, greater vehicle utility, and broader adoption of LS-EVs. This paper presents a modular Input-Series Output-Parallel (ISOP) DC-DC converter for LS-EVs fast chargers. A generalized small-signal analysis applicable for any multimodule connection (Input-Series Input-Parallel Output-Series Output-Parallel (ISIP-OSOP) is introduced. The employed topology is a multimodule DC-DC converter based on Dual Active Bridge (DAB). Nonetheless, a single bridge is utilized at the primary side, and the modularity concept is applied to the high-frequency transformer and the second bridge where the connection of the modules is ISOP. In the presented system, 3-modules are employed where each module is rated at 1.5kWto achieve the desired power rating, which is 4.5kW. The charging process is achieved from a single-phase outlet. However, due to the high output current, a modular approach is required to avoid high losses. Uniform power-sharing is achieved through a direct output current sharing control, ensuring stability without the need for input voltage sharing loops, unlike the conventional ISOP converters. This is due to the fact that the proposed configuration uses only a single capacitor at the input side, avoiding the inherent instability problem caused by the output current sharing control. The controller is examined using a 3-module ISOP DC-DC converter, where the controlled current is following the reflex charging algorithm. Simulation results using the Matlab/Simulink platform are provided to elucidate the presented concept considering parameter mismatches, where the input voltage and the output current are equally shared among the three modules.

1. Introduction

Low-Speed Electric Vehicles (LS-EVs) are zero-emission EVs that are commonly used in suburban areas, airports, retirement communities, sports complexes, country clubs, vacation resorts, and golf courses. LS-EVs operate over short distances and primarily run on batteries. Nowadays, LS-EVs such as

* Corresponding author.
E-mail addresses: me1203675@student.qu.edu.qa (M. ElMenshawy), ahmed.massoud@qu.edu.qa (A. Massoud).
Peer review under responsibility of Faculty of Engineering, Alexandria University.

https://doi.org/10.1016/j.aej.2020.10.031

golf carts are powered by a sealed lead-acid battery pack. This is due to the cost advantage of the lead-acid battery when compared to other batteries. The LS-EVs recharging process is typically done via a standard single-phase outlet [1]. Such a process takes more than eight hours. Accordingly, the fast charging of the battery pack is necessary to increase the LS-EVs utilization and to attain wide acceptance by the public. To achieve that, one approach is to invest in fast recharging stations infrastructure. Accordingly, the main aim of this paper is to develop a modular DC-DC converter for LS-EVs fast chargers.

Currently, most EVs chargers consist of the AC-DC conversion stage and the DC-DC conversion stage. In [2], a bidirectional fast charging system control strategy consisting of two cascaded stages has been proposed, where two Dual Active Bridges (DABs) are connected in parallel at the battery side. The aim of the proposed strategy in [2], is to deal with higher power levels and reduced component stresses. However, in [3], an isolated DAB-based single-stage AC-DC converter has been presented. The charger in [3], contains a single stage that includes the PFC and ensures ZVS over the full load range. A variable switching frequency and single-phase modulation control are proposed using one stage and resulted in higher efficiency and higher power density. In [4], an architecture for multi-megawatt power transfer for an extreme fast-charging infrastructure has been introduced. This is meant to charge several EVs simultaneously in 15 min. An architecture that makes use of the DC-DC converters partial rated power to charge the individual EVs has been presented in [4]. In [5], two DC-DC converters topologies for off-board EV chargers have been presented. Moreover, isolated and non-isolated topologies appropriate for off-board EVs chargers are analyzed and compared with a power rating of 40kW/200V. These topologies are half-bridge LLC converter, interleaved buck converter, and full-bridge phase-shift converter. It is concluded from [4], that the LLC provides the highest efficiency and lowest cost. However, based on the load profile, efficiency may decrease. It is also concluded that the interleaved buck converter is a promising candidate if isolation is not required since it provides a low current ripple that would improve the battery lifetime. Fast charging techniques, including traditional and advanced charging techniques, have been discussed in [5]. The conventional charging techniques are Constant-Current Constant-Voltage (CC-CV) and Multistage Constant-Current Constant-Voltage (MCC-CV) [5]. MCC-CV has been proposed in [6] to increase the battery acceptance rate. The stated charging traditional methods do not have the capability of transferring high power. Accordingly, advanced charging techniques are used to achieve better results. The advanced charging techniques are CC-CV method with negative pulses and variable frequency pulse charge. Such charging methods are utilized to increase charging acceptance [6,7].

A safe charge and discharge process should be guaranteed in the DC-DC converter stage. In which, proper measures shall be taken to prevent battery degradation resulting in battery shorter lifetime expectation. In other words, voltage levels should be within acceptable limits, and the charging current should not affect the integrity of the battery. Moreover, galvanic isolation should be taken into consideration for safety issues. The DC-DC converters topologies presented in this section are the two-level DAB converters and multimodule converters.

The most critical parameters in the requirements for designing an EV battery charger are power density, efficiency, cost, and galvanic isolation [8]. Increasing the switching frequency would reduce the size and cost of the passive elements. However, increasing the switching frequency would increase the switching losses. Accordingly, soft switching techniques and resonant topologies are usually employed in such applications to increase the switching frequency without sacrificing the efficiency of the power stage. Another requirement that is necessary for the EV charger system is to select a topology that can control the high current at the output side. Also, to electrically isolate the grid from the vehicles, galvanic isolation is required [8]. This can be done by employing a high-frequency transformer.

The DAB DC-DC converter is a topology that can be used for low and high-power applications [9,10]. It is commonly used in EV charger applications [11–19]. The DAB configuration, shown in Fig. 1, consists of two active bridges that are connected via a medium/high-frequency AC transformer. DAB can be constructed using a single-phase bridge or a three-phase bridge depending on the design criteria [20]. The 2L-DAB shown in Fig. 1 usually operates in a square wave mode [21,22]. The intermediate transformer leakage inductance limits the maximum power flow and is used as the energy transferring element [23]. The steady-state operation, including the switching modes for the 2L-DAB, has been discussed in [24–28]. This topology is capable of bidirectional power flow that can be achieved by controlling the phase shift between the two bridges and the magnitude of the output voltage per bridge [22]. The switches can be switched at ZVS and/or Zero Current Switching (ZCS. Accordingly, switching losses are reduced, and the power efficiency is increased. However, ZVS operation (i.e., soft switching features) is not ensured at light load. In other words, the conventional DAB soft-switching region is limited to a narrow output voltage range. However, in EV battery charger applications, the converter may be operating at light loading for a period of time. Therefore, to achieve high efficiency, ZVS should be maintained with a wide load range. Accordingly, several control strategies have been proposed to increase the soft-switching range and reduce the transformer current. In addition, a high conversion ratio can be obtained by choosing the transformer turns ratio [21].

To enhance the DAB soft-switching range, several Resonant DAB (R-DAB) topologies have been proposed [9,29–43]. One of the resonant topologies that have gained much attention due to its low resonant network component when applied with the DAB converter is the Series R-DAB (SR-DAB). In this topology, an extra capacitor is only required. As mentioned in [44], SR-DAB is usually modulated through a frequency modulation scheme. However, to modulate the power transfer, an extensive switching frequency range is required, which causes difficulties in the filter and control

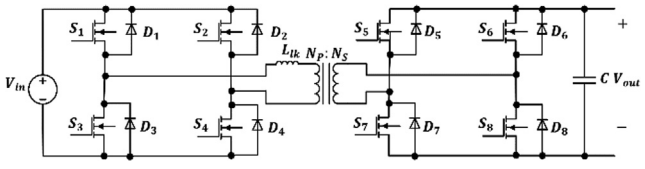

Fig. 1 DAB converter circuit diagram.

design. Phase modulation for SR-DAB has been proposed in [35–38].

In [29,44], a frequency modulated CLLC-R-DAB has been proposed. In this topology, the converter can operate over a considerable variation of the input voltage while maintaining soft-switching capability. A smaller switching frequency range is used to modulate the CLLC-R-DAB converter when compared to SR-DAB. In [39,45], a DAB with a tuned LCL network has been proposed. It has been shown that the bridge current magnitude is reduced when operated at the LCL network tuned frequency. This minimized the high-frequency link conduction losses and enhanced the utilization of the semiconductor devices in both full bridges. In [46], a DAB with a tuned CLLC structure has been proposed to increase the power density of the converter in [39,46]. The proposed topology in [47], reduced the required number of magnetic components and the transformer magnetizing inductance while maintaining similar operating characteristics as the LCL-DAB topology.

Through the modular design of DAB, easier scalability of the system can be obtained. In addition, through inserting redundant modules, system reliability is achieved. The possible architectures of connecting multiple DAB units are classified into four main categories which are: Input-Series Output-Series (ISOS), Input-Parallel Output-Parallel (IPOP), Input-Series Output-Parallel (ISOP), Input-Parallel Output-Series (IPOS) [48,49].

Fig. 2 shows multimodule DC-DC converters with some of its possible configurations that can be employed in EV charger applications. In this converter, each Sub-Module (SM) operates at a single module rated voltage and contributes with a fraction of the total output power. Accordingly, such converters can operate with a higher switching frequency without facing challenges in their design and without sacrificing conversion efficiency [50]. This DC-DC converter is based on the modular structure and can offer unidirectional or bidirectional power flow according to the technical requirements of the application. In this arrangement, extra control techniques are required to ensure equal voltage and/or current sharing among the SMs. However, the converter shown in Fig. 2(b) based on FB topology experiences some drawbacks. Firstly, the diodes in the rectifier stage are exposed to high reverse recovery currents in high-power applications. In addition, this converter suffers from a limited ZVS range [29,50,51]. However, several solutions have been suggested in [29,51,52] to reduce the high reverse recovery current. In Fig. 2(e), the FB converters adjust their frequency according to the AC link resonant frequency to generate across the primary and secondary winding of the transformer voltage waveform that has a sinusoidal behavior. This would enable the switching devices to operate near to the ZCS [50].

The presented work in this paper focuses on modular power converters for LS-EVs fast chargers. Modular power converters are scalable and can provide a ride-through capability, redundancy, and easy maintenance [53]. In this paper, a DC-DC converter for LS-EVs fast chargers is proposed. Different DC-DC converters are reviewed for EVs applications. However, the focus will be on multimodule power converters since higher switching frequency can be achieved and hence reduced weight and size. Moreover, through the employment of soft switching techniques, the losses of the converter are reduced, and thereby, higher efficiency can be achieved. To develop the small-signal analysis for the proposed fast charger DC-DC converter, a generalized small-signal analysis applicable for Input-Series Input-Parallel Output-Series Output-Parallel (ISIP-OSOP) is developed to study the dynamic performance of multimodule DC-DC converters. This is achieved by study-

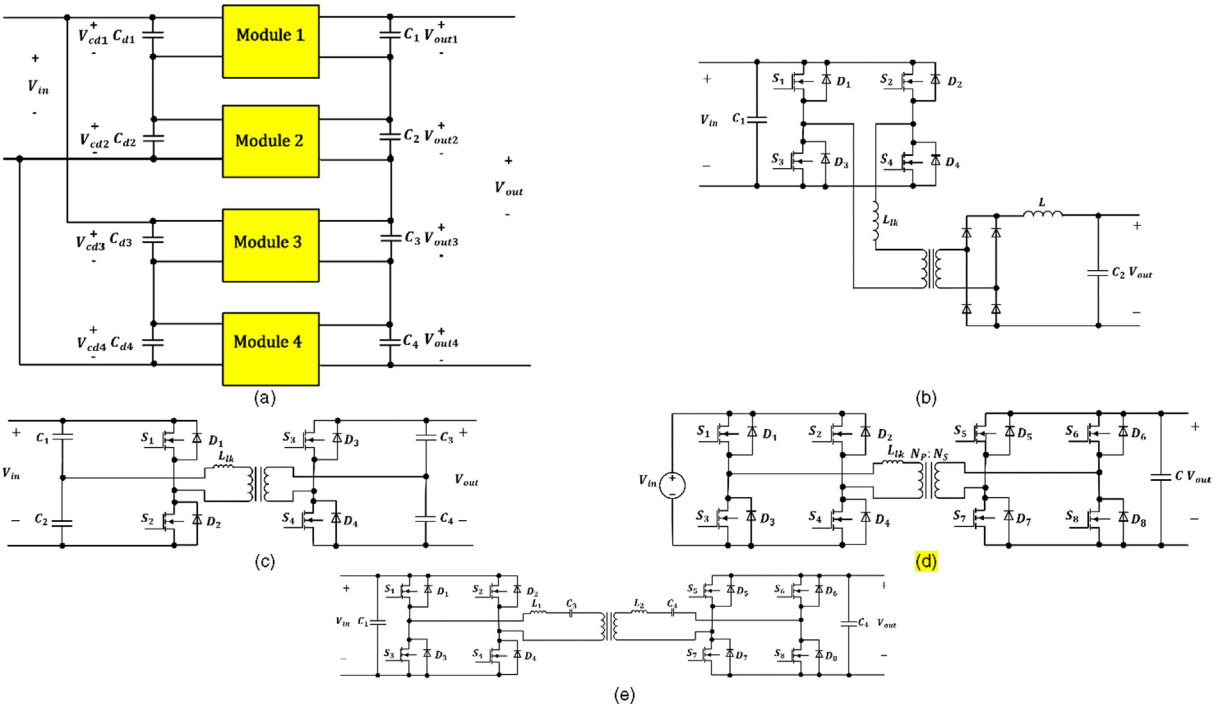

Fig. 2 Multimodule DC-DC converter possible configurations; (a) Generic multimodule DC-DC converter; (b) FB circuit configuration; (c) HB circuit configuration; (d) DAB circuit configuration; (e) DAB DC-DC converter-based resonant topology.

ing the small-signal analysis of Full-Bridge Phase-Shift (FB-PS) DC-DC converter, 2-module Input-Parallel Output-Series (IPOS), 3-module Input-Series Output-Parallel (ISOP), and 4-module Input-Series Input-Parallel Output-Series (ISIPOS) presented in [54,55,48,56–58], respectively. After deriving the generalized model, the model is verified with the multimodule configurations presented in [48,57,55]. Accordingly, the generalized model is used to derive the small-signal model for the proposed ISOP DC-DC converter. Furthermore, the control of the proposed ISOP DC-DC converter is studied to guarantee equal distribution of power among the modules.

The main contribution of the paper can be summarized as follows:

- A modular DC-DC converter for LS-EVs fast chargers is proposed. The proposed configuration is ISOP DC-DC converter, where the control of the proposed converter can be achieved via direct Output Current Sharing (OCS) control that can achieve OCS as well as Input Voltage Sharing (IVS) without the need for IVS control loops. In other words, the control of the proposed configuration can be achieved via OCS, where the instability problem associated with the conventional ISOP converters controlled via direct OCS [48] is avoided. This is due to the fact that the proposed configuration contains only a single capacitor at the input side, unlike the conventional ISOP DC-DC converters presented in [56].
- A generalized model for the multimodule ISIP-OSOP DC-DC converter, which is used to derive the small-signal analysis of the proposed ISOP fast charger DC-DC converter, is provided.
- The control scheme of the proposed DC-DC converter to achieve equal power-sharing between the modules is provided considering parameter mismatch to elucidate the presented concept.

This paper is structured such that: Section 2 presents a generalized small-signal model for ISIP-OSOP multimodule power converter. Section 3 presents the proposed ISOP fast charger DC-DC converter circuit diagram and the small-signal model. Section 4 discusses the control strategy for the proposed ISOP DC-DC converter based on constant current control considering parameter mismatch and reflex charging algorithm for lead-acid batteries. Finally, the conclusion is presented in Section 5.

2. Generalized small signal analysis for dual series/parallel Input-Output (ISIP-OSOP) DC-DC converter

One of the attractive DC-DC converters used in fast charging EVs applications and can provide bidirectional power flow is the multimodule DC-DC converters-based DAB topology [53,59,60]. Several research studies have presented the small-signal analysis for modular power converters. In [61], the small-signal modeling for ISOS DC-DC converters has been studied. However, in [48,56,57,55], the control strategy with the small-signal modeling for the ISOP, ISIPOS, and IPOS have been studied, respectively. The selected topology is the multimodule DC-DC converter DAB. However, only a single bridge is employed at the primary side, and the modularity concept will be applied to the high-frequency transformer and the second bridge where the connection of the modules is ISOP, as shown in Fig. 3. In this section, the small-signal modeling presented in [48,54–58] is expanded to include a generalized small-signal analysis applicable for ISIP-OSOP configuration.

2.1. ISIP-OSOP generic DC-DC converter circuit diagram

The ISIP-OSOP generic DC-DC converter configuration shown in Fig. 4, consists of *n*isolated units that are connected in series and/or parallel at the input side, and in series and/or parallel at the output side, as presented in Fig. 4.

By ensuring Input Current Sharing (ICS) and IVS, the input current per unit is $\frac{I_{in}}{\boldsymbol{\alpha}}$, and the input voltage per unit is $\frac{V_{in}}{\boldsymbol{\beta}}$. In which, I_{in} is the input current and V_{in} is the input voltage of the ISIP-OSOP DC-DC converter, and $\boldsymbol{\alpha}$ is the number of modules connected in parallel, and $\boldsymbol{\beta}$ is the number of modules connected in series at the input side. Similarly, by ensuring OCS and Output Voltage Sharing (OVS), the output current per unit is $\frac{I_o}{\boldsymbol{a}}$, and the output voltage per unit is $\frac{V_o}{\boldsymbol{b}}$. In which I_o is the output current and V_o is the output voltage of the ISIP-OSOP DC-DC converter, and $\boldsymbol{a}$ is the number of modules connected in parallel, and $\boldsymbol{b}$ is the number of modules connected in series at the output side.

2.2. ISIP-OSOP DC-DC converter small signal analysis

Using the model presented in [55], and expanding the study of the presented multimodule DC-DC converters presented in [48,55–58] the small-signal model for the ISIP-OSOP converter presented in Fig. 5 is derived. It is worth mentioning that the red colored symbols reflect the parameters defined for the input side while the blue colred symbols reflect the parameters defined for the output side. This is done to diffrentiate between the input side and the output side in the small signal analysis.

Since the input current and voltage per unit is $\frac{I_{in}}{\boldsymbol{\alpha}}$ and $\frac{V_{in}}{\boldsymbol{\beta}}$, respectively, and the output current and voltage per unit is $\frac{I_o}{\boldsymbol{a}}$ and $\frac{V_o}{\boldsymbol{b}}$, respectively. Therefore, the load resistance per unit is $\boldsymbol{b}$ R. Accordingly, $\widehat{d}_{ij}$ and $\widehat{d}_{vj}$ which are the effect of changing the filter inductor current and the effect of changing the input voltage on the duty cycle modulation, as well as I_{eq} can be presented as [48,55,56]:

$$\hat{d}_{ij} = -\frac{4\boldsymbol{\beta} L_{lk} f_s}{K V_{in}} i_{Lj}, \qquad j = 1,2,\ldots,n \tag{1}$$

where $K = N\_P/N\_S$ is the turns ratio of the intermediate transformer.

Eq. (1) can be modified as:

$$\hat{d}_{ij} = -\frac{\boldsymbol{\beta} K R_d}{V_{in}} i_{Lj}, \qquad j = 1,2,\ldots,n \tag{2}$$

where $R_d = \frac{4L_{lk}f_s}{k^2}$.

$$\hat{d}_{vj} = \frac{4\boldsymbol{\beta}\boldsymbol{b} L_{lk} f_s D_{eff}}{\boldsymbol{a} k^2 R V_{in}} \hat{v}_{cdj}, \qquad j = 1,2,\ldots,n \tag{3}$$

Eq. (3) can be modified as:

$$\hat{d}_{vj} = \frac{\boldsymbol{\beta}\boldsymbol{b} R_d D_{eff}}{\boldsymbol{a} R V_{in}} \hat{v}_{cdj}, \qquad j = 1,2,\ldots,n \tag{4}$$

$$I_{eq} = \frac{\boldsymbol{b} V_{in}}{\boldsymbol{\beta}\boldsymbol{a} K R} \tag{5}$$

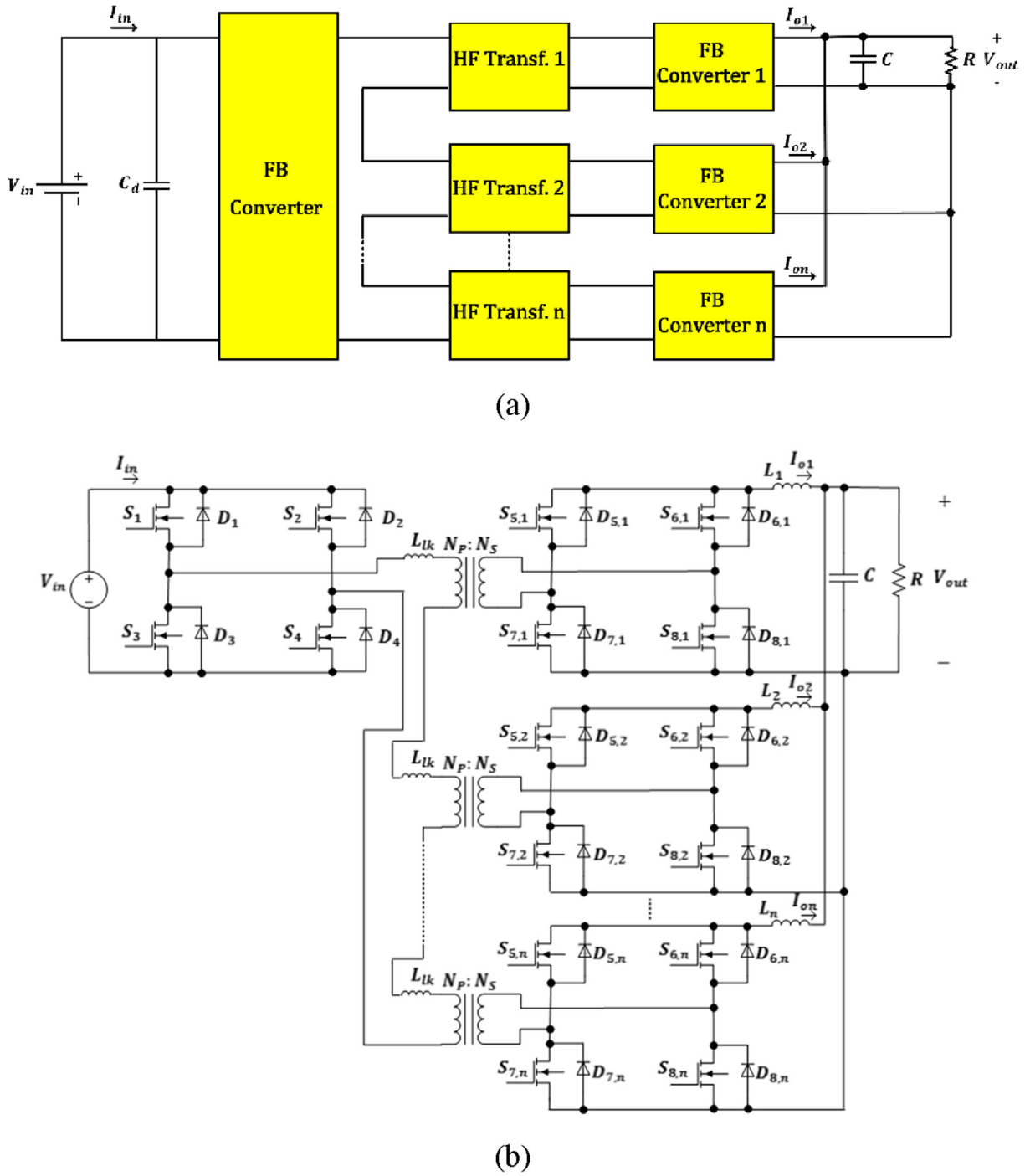

Fig. 3 Proposed fast charger DC-DC converter circuit diagram; (a) DC-DC converter overall configuration, (b) DC-DC converter detailed configuration.

Eqs. (6) and (7) are obtained from Fig. 5:

$$\begin{cases} \frac{D_{eff}}{K}\hat{v}_{cd1} + \frac{V_{in}}{\beta K}(\hat{d}_{i1} + \hat{d}_{v1} + \hat{d}_1) = sL\hat{i}_{L1} + \hat{v}_{out1} \\ \frac{D_{eff}}{K}\hat{v}_{cd2} + \frac{V_{in}}{\beta K}(\hat{d}_{i2} + \hat{d}_{v2} + \hat{d}_2) = sL\hat{i}_{L2} + \hat{v}_{out2} \\ \vdots \\ \frac{D_{eff}}{K}\hat{v}_{cdn} + \frac{V_{in}}{\beta K}(\hat{d}_{in} + \hat{d}_{vn} + \hat{d}_n) = sL\hat{i}_{Ln} + \hat{v}_{outn} \end{cases} \tag{6}$$

$$\begin{cases} \hat{i}_{L11} + \hat{i}_{L21} + \cdots + \hat{i}_{La1} = \frac{sC}{sR_cC+1}\hat{v}_{out1} + \frac{\hat{v}_{out}}{R} \\ \hat{i}_{L12} + \hat{i}_{L22} + \cdots + \hat{i}_{La2} = \frac{sC}{sR_cC+1}\hat{v}_{out2} + \frac{\hat{v}_{out}}{R} \\ \vdots \\ \hat{i}_{L1b} + \hat{i}_{L2b} + \cdots + \hat{i}_{Lab} = \frac{sC}{sR_cC+1}\hat{v}_{outn} + \frac{\hat{v}_{out}}{R} \end{cases} \tag{7}$$

Based on the feature of modularity, it is assumed that all the modules are identical to simplify the small-signal model.

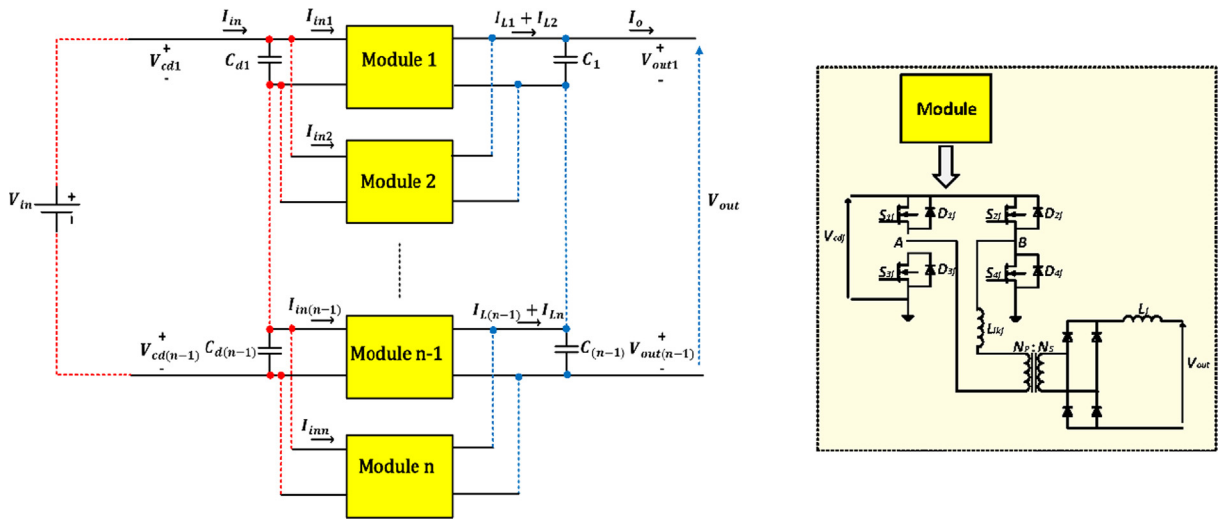

Fig. 4 Generalized multimodule DC-DC converter circuit diagram.

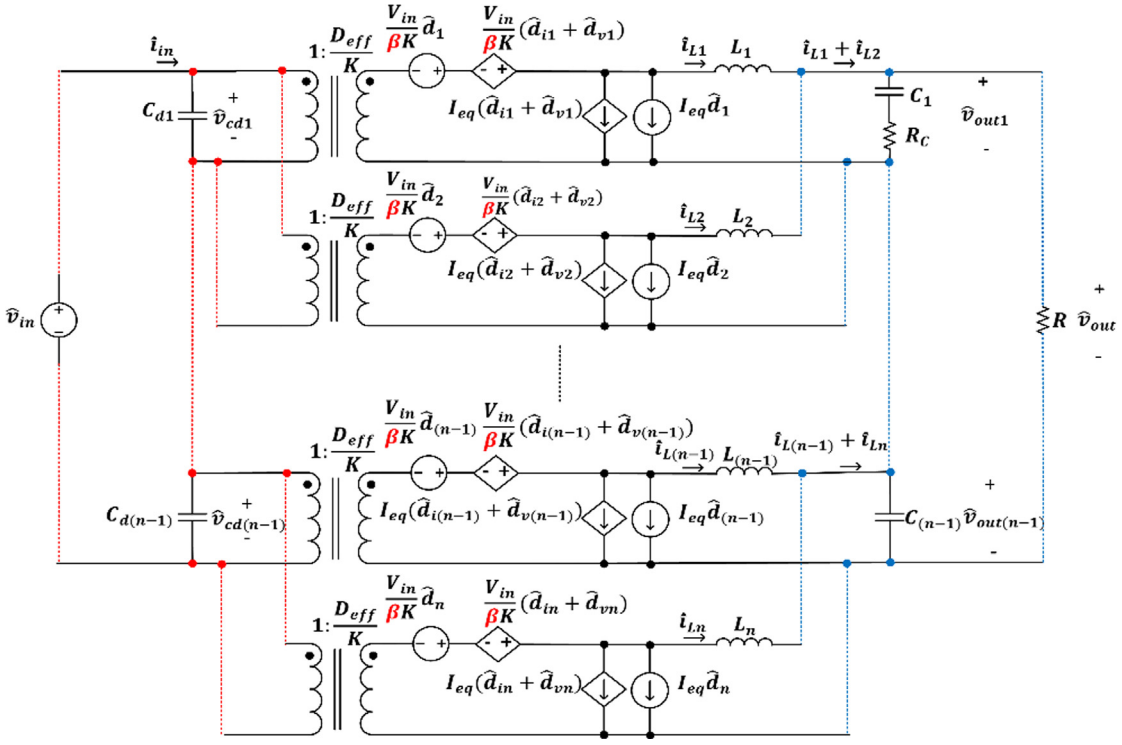

Fig. 5 *n*-module ISIP-OSOP DC-DC converter small-signal model.

Adding equations in (7):

$$\sum_{i=1}^{a}\sum_{j=1}^{b}\hat{\imath}_{Lij} = \frac{sC}{sR_cC+1}\hat{v}_{out} + \frac{b\hat{v}_{out}}{R} \tag{8}$$

Eq. (8) can be written as:

$$\sum_{i=1}^{a}\sum_{j=1}^{b}\hat{\imath}_{Lij} = \hat{v}_{out}\left(\frac{sRC + sbR_cC + b}{R(1+sR_cC)}\right) \tag{9}$$

However, the ESR can be neglected compared to the load.

Defining the summation terms of the module's input and output voltage appearing after summing up equations in (6):

$$\sum_{j=1}^{n}\hat{v}_{cdj} = \gamma\hat{v}_{in} \tag{10}$$

where

$\gamma = 1$, if all the modules at the input side are connected in series.

$\gamma = \alpha$, if all the modules at the input side are connected in parallel or if the modules at the input side are connected in both; series and parallel.

$$\sum_{j=1}^{n}\hat{v}_{outj} = c\hat{v}_{out} \tag{11}$$

where

$c = 1$, if all the modules at the output side are connected in series.
$c = a$, if all the modules at the output side are connected in parallel or if the modules at the output side are connected in both; series and parallel.

2.2.1. Control-to-output voltage transfer function

This transfer function is obtained by adding up equations in (6), assuming $\hat{v}_{in} = 0$, and $\hat{d}_k = 0$, where $k = 1, 2, \cdots, n$and $k \neq j$, and substituting (2), (4), (9), (10), and (11).

Adding equations in (6):

$$\frac{D_{eff}}{K}\sum_{j=1}^{n}\hat{v}_{cdj} + \frac{V_{in}}{\beta K}\left(\sum_{j=1}^{n}\hat{d}_{ij} + \sum_{j=1}^{n}\hat{d}_{vj} + \sum_{j=1}^{n}\hat{d}_j\right) = sL\sum_{j=1}^{n}\hat{\imath}_{Lj} + \sum_{j=1}^{n}\hat{v}_{outj} \tag{12}$$

$$\frac{D_{eff}}{K}\sum_{j=1}^{n}\hat{v}_{cdj} + \frac{V_{in}}{\beta K}\left(\sum_{j=1}^{n} -\frac{\beta K R_d}{V_{in}}\hat{\imath}_{Lj} + \sum_{j=1}^{n}\frac{\beta b R_d D_{eff}}{aRV_{in}}\hat{v}_{cdj} + \hat{d}_1\right) = sL\sum_{j=1}^{n}\hat{\imath}_{Lj} + \sum_{j=1}^{n}\hat{v}_{outj} \tag{13}$$

$$\frac{D_{eff}}{K}\gamma\hat{v}_{in} + \frac{V_{in}}{\beta K}\left(\sum_{j=1}^{n} -\frac{\beta K R_d}{V_{in}}\hat{\imath}_{Lj} + \frac{\beta b R_d D_{eff}}{aRV_{in}}\gamma\hat{v}_{in} + \hat{d}_1\right) = sL\sum_{j=1}^{n}\hat{\imath}_{Lj} + c\hat{v}_{out} \tag{14}$$

Rearranging (14) results in (15).

$$G_{vd} = \frac{\hat{v}_{out}}{\hat{d}_j} = \frac{\frac{V_{in}}{\beta K}(1 + sR_cC)}{s^2LC\left(1 + \frac{bR_c}{R}\right) + s\left(\frac{bL}{R} + R_dC\left(1 + \frac{bR_c}{R}\right) + cR_cC\right) + \frac{bR_d}{R} + c} \tag{15}$$

2.2.2. Control-to-Filter inductor current transfer function

This transfer function can be obtained using (9) to find the following equation:

$$\hat{v}_{out} = \frac{R(1 + sR_cC)}{sRC + sbR_cC + b}\sum_{i=1}^{a}\sum_{j=1}^{b}\hat{\imath}_{Lij} \tag{16}$$

Substituting (16) in (14), and assuming $\hat{v}_{in} = 0$, and $\hat{d}_k = 0$, where $k = 1, 2, \cdots, n$and $k \neq j$.

$$\frac{V_{in}}{\beta K}\hat{d}_1 - R_d\sum_{j=1}^{n}\hat{\imath}_{Lj} = sL\sum_{j=1}^{n}\hat{\imath}_{Lj} + \frac{cR(1 + sR_cC)}{sRC + sbR_cC + b}\sum_{j=1}^{n}\hat{\imath}_{Lj} \tag{17}$$

Rearranging (17) results in (18) seen at the bottom of the page.

$$G_{id} = \frac{\hat{\imath}_L}{\hat{d}_j} = \frac{\frac{V_{in}}{\beta K}(b + sRC + sbR_cC)}{R\left(s^2LC\left(1 + \frac{bR_c}{R}\right) + s\left(\frac{bL}{R} + R_dC\left(1 + \frac{bR_c}{R}\right) + cR_cC\right) + \frac{bR_d}{R} + c\right)} \tag{18}$$

2.2.3. Output impedance

As studied in [48,56], the output impedance of the ISIP-OSOP converter can be obtained by modifying Eq. (7) as follows:

$$\begin{cases} \hat{\imath}_{L11} + \hat{\imath}_{L21} + \cdots + \hat{\imath}_{La1} + \hat{\imath}_{out} = \frac{sC}{sR_cC + 1}\hat{v}_{out1} + \frac{\hat{v}_{out}}{R} \\ \hat{\imath}_{L12} + \hat{\imath}_{L22} + \cdots + \hat{\imath}_{La2} + \hat{\imath}_{out} = \frac{sC}{sR_cC + 1}\hat{v}_{out2} + \frac{\hat{v}_{out}}{R} \\ \vdots \\ \hat{\imath}_{L1b} + \hat{\imath}_{L2b} + \cdots + \hat{\imath}_{Lab} + \hat{\imath}_{out} = \frac{sC}{sR_cC + 1}\hat{v}_{outn} + \frac{\hat{v}_{out}}{R} \end{cases} \tag{19}$$

Summing equations in (19):

$$\sum_{i=1}^{a}\sum_{j=1}^{b}\hat{\imath}_{Lij} = \frac{sC}{sR_cC + 1}\hat{v}_{out} + \frac{b\hat{v}_{out}}{R} - b\hat{\imath}_{out} \tag{20}$$

Accordingly, (7) is modified as follows:

$$\sum_{i=1}^{a}\sum_{j=1}^{b}\hat{\imath}_{Lij} = \hat{v}_{out}\left(\frac{sRC + sbR_cC + b}{R(1 + sR_cC)}\right) - b\hat{\imath}_{out} \tag{21}$$

This transfer function is found by assuming $\hat{v}_{in} = 0$, and $\hat{d}_j = 0, j = 1, 2, \cdots, n$, adding all equations in (6-6), and substituting (2), (4), (10), (11), and (21).

$$\frac{V_{in}}{\beta K}\left(-\frac{\beta K R_d}{V_{in}}\right)\sum_{j=1}^{n}\hat{\imath}_{Lj} = sL\sum_{j=1}^{n}\hat{\imath}_{Lj} + c\hat{v}_{out} \tag{22}$$

$$-R_d\left(\hat{v}_{out}\left(\frac{sRC + sbR_cC + b}{R(1 + sR_cC)}\right) - b\hat{\imath}_{out}\right) = sL\left(\hat{v}_{out}\left(\frac{sRC + sbR_cC + b}{R(1 + sR_cC)}\right) - b\hat{\imath}_{out}\right) + c\hat{v}_{out} \tag{23}$$

Rearranging (23) would result in (24).

$$Z_{out} = \frac{\hat{v}_{out}}{\hat{\imath}_{out}} = \frac{b(R_d + sL)(1 + sR_cC)}{s^2LC\left(1 + \frac{bR_c}{R}\right) + s\left(\frac{bL}{R} + R_dC\left(1 + \frac{bR_c}{R}\right) + cR_cC\right) + \frac{bR_d}{R} + c} \tag{24}$$

2.2.4. Converter gain

The gain of the converter is found by assuming $\hat{d}_j = 0, j = 1, 2, \cdots, n$, adding all equations in (6), and substituting (2), (4), (9), (10) and (11) in the added equation.

$$\frac{D_{eff}}{K}\sum_{j=1}^{n}\hat{v}_{cdj} + \frac{V_{in}}{\beta K}\left(\sum_{j=1}^{n} -\frac{\beta K R_d}{V_{in}}\hat{\imath}_{Lj} + \sum_{j=1}^{n}\frac{\beta b R_d D_{eff}}{aRV_{in}}\hat{v}_{cdj}\right) = sL\sum_{j=1}^{n}\hat{\imath}_{Lj} + \sum_{j=1}^{n}\hat{v}_{outj} \tag{25}$$

$$\frac{D_{eff}}{K}\gamma\left(1 + \frac{bR_d}{aR}\right)\hat{v}_{in} = (sL + R_d)\left(\hat{v}_{out}\left(\frac{sRC + sbR_cC + b}{R(1 + sR_cC)}\right)\right) + c\hat{v}_{out} \tag{26}$$

Rearranging (26) would result in (27).

$$G_{vg} = \frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{\frac{D_{eff}}{K}\gamma\left(1 + \frac{bR_d}{aR}\right)(1 + sR_cC)}{s^2LC\left(1 + \frac{bR_c}{R}\right) + s\left(\frac{bL}{R} + R_dC\left(1 + \frac{bR_c}{R}\right) + cR_cC\right) + \frac{bR_d}{R} + c} \tag{27}$$

3. Fast charger DC-DC converter with ISOP connection

The same analysis carried out in the previous section is expanded considering modular structures ISOP based FB-PS DC-DC converter. However, the modular manner will be applied only on the high-frequency transformer and the second FB converter. The analysis carried out in this paper is not restricted to unidirectional power flow and can be applied for bidirectional power flow.

3.1. Proposed Fast Charger ISOP DC-DC converter circuit

As introduced in Section 2, the proposed converter shown in Fig. 3 consists of multiple high-frequency transformers as well as FB converters connected in series and parallel at the input and the output, respectively. Considering 3-module ISOP DC-DC converter and by ensuring equal IVS and OCS, the input voltage per unit is $\frac{V_{in}}{3}$, and the output current per unit is $\frac{I_o}{3}$. In which, V_{in} and I_o are the input voltage and the output

current of the converter, respectively. Each module is rated at $1.5kW$,and to achieve the desired power rating, which is $4.5kW$, three modules are connected in series at the input side and connected in parallel at the output side are required. According to the mentioned specifications at the input side, a single FB converter that can handle the input current$14A$ is employed. However, due to the high output current $94A$, a modular approach is required to avoid high losses and achieve the highest efficiency.

As mentioned in Section 1, the steady-state analysis for a DAB DC-DC converter has been presented in [24], showing the equivalent circuit at each operating mode. The same behavior is expected using the presented power converter since the converter is based on DAB topology. The equivalent circuit at each operating mode is shown in Fig. 6, indicating at each mode the corresponding period for the reflex charging.

3.2. Fast charger ISOP DC-DC converter small signal analysis

Using the analysis provided [55], the small-signal model for the proposed converter presented in Fig. 7 is derived. In which, it is assumed that all the units are ideal.

Since the input voltage per unit is $\frac{V_{in}}{3}$, and the output current per unit is $\frac{I_o}{3}$, therefore, the load resistance per unit is $3R$. Accordingly, the values for the six parameters that are previously defined are known and shown in Table 1.

Substituting the six parameters with their values in Eqs. (15), (18), (24), and (27) would result in the transfer functions presented in Table 2.

However, the first two transfer functions which are the control-to-output voltage and control-to filter inductor current are found assuming that $\widehat{d}_k = 0$, where $k = 1, 2, \cdots, n$ and $k \neq j$. In other words, these two transfer functions are found with respect to the effect of the duty cycle perturbation of only one module. However, since only one module is available at the primary side, the duty cycle perturbation $\widehat{d}_1$ will appear three times. Therefore, $G_{vd} = \frac{\widehat{v}_{out}}{3\widehat{d}_1}$ and $G_{id} = \frac{\widehat{i}_L}{3\widehat{d}_1}$. Accordingly, Table 2 is updated, resulting in Table 3.

To study the behavior of the converters when its parameters such as the transformer leakage inductance, switching frequency, and the load resistance are varied. The term $\frac{R_d}{R}$ is varied because it includes the effect of L_{lk},f_s, and R, as shown in Section 2. The converter presented in this paper is designed considering that the term $\frac{R_d}{R} = 0.25$. Accordingly, the impact of this term is studied with a variation of up to $\pm 100\%$ of the designed value.

Fig. 8 presents the effect of changing the term $\frac{R_d}{R}$ from 0 to 0.5 on the frequency response of the proposed control-to-output voltage of the fast charger 3-module ISOP DC-DC converter. It can be noticed that the term $\frac{R_d}{R}$ affects the system damping (increasing the term $\frac{R_d}{R}$, increases the system's damping and vice versa). Furthermore, the term $\frac{R_d}{R}$is equivalent to the quality factor where a lower quality factor ensures a higher output voltage

4. Power sharing in the ISOP fast charger DC-DC converter

Since modules in practical applications are not identical, any mismatch in the parameter values can cause unequal power distribution among the modules. Consequently, the voltage of a single module is unbalanced; in addition, modules that are heavily loaded are thermally overstressed [57]. Accordingly, a control scheme that ensures uniform power-sharing among the modules is required to achieve reliable operation for the ISIP-OSOP DC-DC converter. For instance, if the connection is ISOP as in [60], then a control scheme that ensures IVS and OCS is required. However, if the connection is ISIPOS as delivered in [56], then a control scheme that ensures IVS, ICS, and OVS is required.

Since the proposed converter is connected in series and parallel at the input and output sides, respectively, a control scheme that ensures IVS and OCS is required. In this section, a control scheme for an active power balancing between the modules is addressed for the 3-module ISOP DC-DC converter.

Assuming the modules presented in Fig. 3 are lossless; the input and output power relationship of each module can be expressed as:

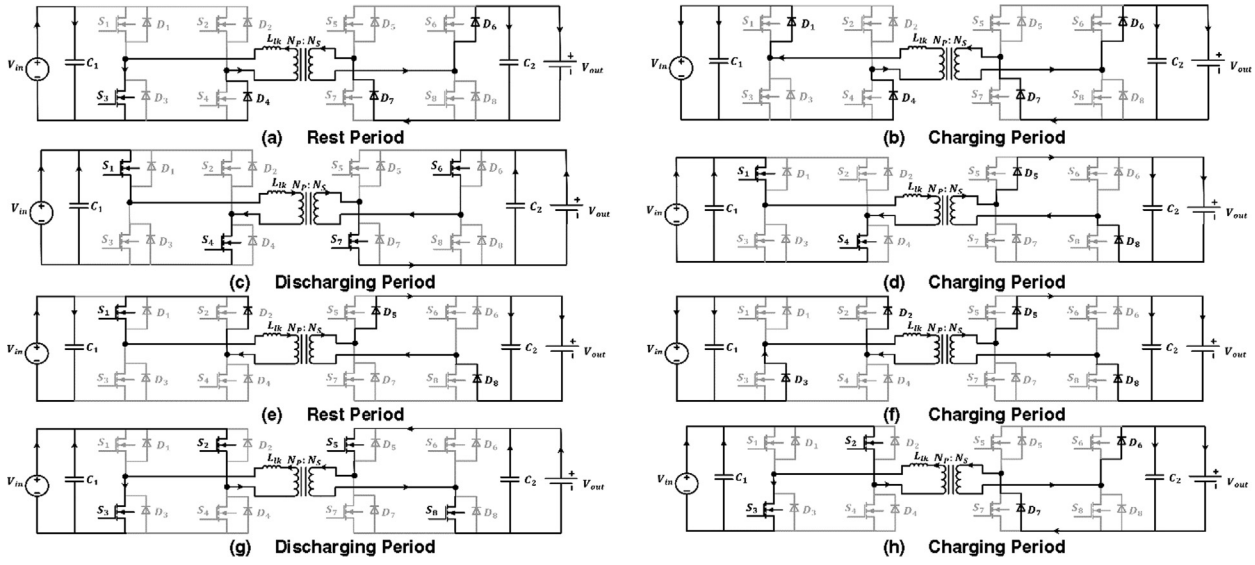

Fig. 6 Operation modes for DAB converter.

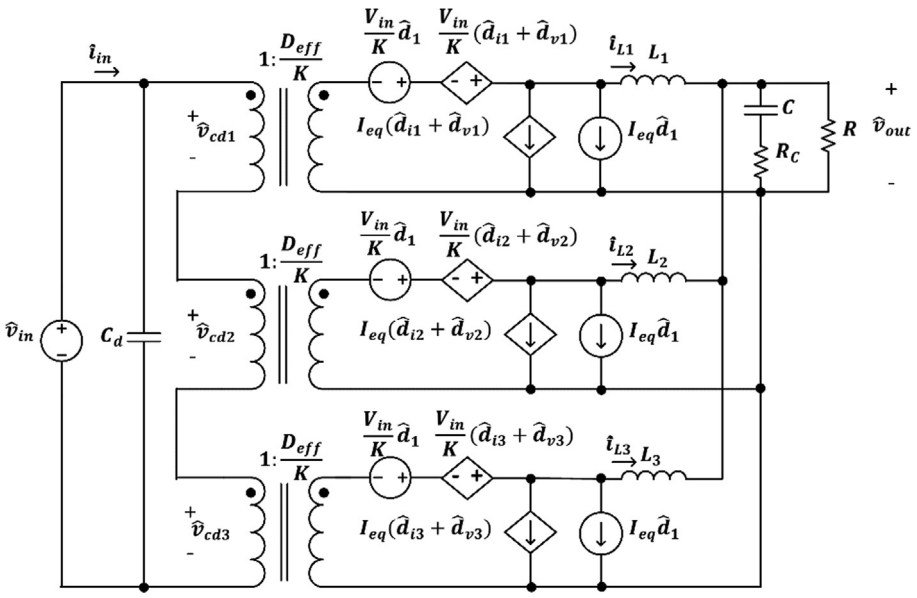

Fig. 7 Proposed ISOP DC-DC converter small-signal model.

Table 1 Values for the Six Parameters for the proposed ISOP Fast Charger DC-DC Converter.

Defined Variables		
Input Side	α	1
	β	3
	γ	1
Output Side	a	3
	b	1
	c	3

Table 2 Transfer functions for 3-module ISOP DC-DC converter.

Transfer functions for 3-module ISOP DC-DC converter	
G_{vd}	$\frac{\frac{V_{in}}{3K}(1+sR_cC)}{s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3}$
G_{id}	$\frac{\frac{V_{in}}{3K}(1+sRC+sR_cC)}{R\left(s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3\right)}$
Z_{out}	$\frac{(R_d+sL)(1+sR_cC)}{s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3}$
G_{vg}	$\frac{\frac{D_{eff}}{K}\left(1+\frac{R_d}{3R}\right)(1+sR_cC)}{s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3}$

$$\begin{cases} V_{cd1}I_{in} = V_{out}I_{out1} \\ V_{cd2}I_{in} = V_{out}I_{out2} \\ V_{cd3}I_{in} = V_{out}I_{out3} \end{cases} \tag{28}$$

where V_{cd1}, V_{cd2}, and V_{cd3} are the DC input voltages across the transformer windings for module 1 and 2 and 3 respectively, I_{out1}, I_{out2} and I_{out3} are the output currents for modules 1, 2, and 3 respectively, I_{in} and V_{out} are the input voltage and the output voltage for the three modules.

Table 3 Updated Transfer functions for 3-module ISOP DC-DC converter.

Transfer functions for 3-module ISOP DC-DC converter	
G_{vd}	$\frac{\frac{V_{in}}{K}(1+sR_cC)}{s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3}$
G_{id}	$\frac{\frac{V_{in}}{K}(1+sRC+sR_cC)}{R\left(s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3\right)}$
Z_{out}	$\frac{(R_d+sL)(1+sR_cC)}{s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3}$
G_{vg}	$\frac{\frac{D_{eff}}{K}\left(1+\frac{R_d}{3R}\right)(1+sR_cC)}{s^2LC\left(1+\frac{R_c}{R}\right)+s\left(\frac{L}{R}+R_dC\left(1+\frac{R_c}{R}\right)+3R_cC\right)+\frac{R_d}{R}+3}$

If OCS is accomplished, meaning that $I_{out1} = I_{out2} = I_{out3}$, therefore, according to (28), the following equation is obtained.

$$V_{cd1}I_{in} = V_{cd2}I_{in} = V_{cd3}I_{in} \tag{29}$$

It can be concluded from (29) that $V_{cd1} = V_{cd2} = V_{cd3}$, meaning that if OCS is achieved among the three modules, IVS sharing is also achieved.

Alternatively, if IVS is achieved, meaning that $V_{cd1} = V_{cd2} = V_{cd3} = \frac{V_{in}}{3}$, therefore, according to (28), the following equation is obtained.

$$V_{out}I_{out1} = V_{out}I_{out2} = V_{out}I_{out3} \tag{30}$$

It can be concluded from (30) that $I_{out1} = I_{out2} = I_{out3}$, meaning that if IVS is achieved among the three modules, OCS is also achieved. Consequently, to recognize output side control, an output voltage control for the overall converter

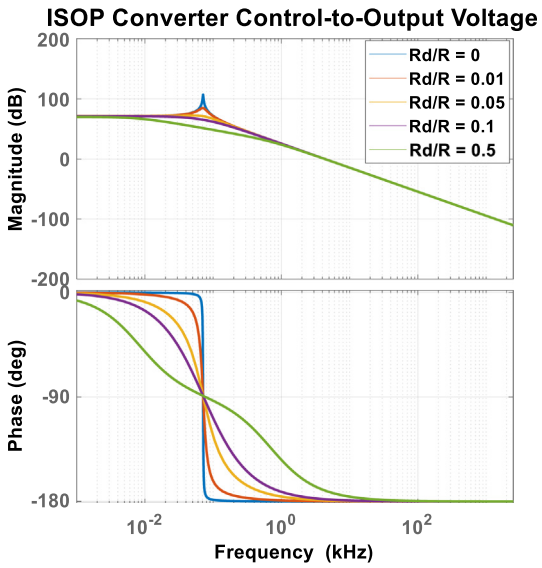

Fig. 8 Effect of varying $\frac{R_d}{R}$.

as well as output current controller per unit are dedicated; to ensure stable operation for the parallel-connected modules. To achieve uniform power distribution, the output voltage control, in addition to the overall control scheme, is described where the small-signal analysis derived in the previous section is used and will be further illustrated.

The effect of changing the filter inductor current and the effect of changing the input voltage on the duty cycle modulation which are $\widehat{d}_{ij}$ and $\widehat{d}_{vj}$, respectively as well as I_{eq} are updated according to the parameters listed in Table 2.

$$\widehat{d}_{ij} = -\frac{12L_{lk}f_s}{KV_{in}}\widehat{i}_{Lj}, j = 1,2,3 \tag{31}$$

Eq. (31) can be written as follows by substituting R_d which is previously defined in Section 2.

$$\widehat{d}_{ij} = -\frac{3KR_d}{V_{in}}\widehat{i}_{Lj}, j = 1,2,3 \tag{32}$$

$$\widehat{d}_{vj} = \frac{4L_{lk}f_sD_{eff}}{k^2RV_{in}}\widehat{v}_{cdj}, j = 1,2,3 \tag{33}$$

A similar step can be done with (33):

$$\widehat{d}_{vj} = \frac{R_dD_{eff}}{RV_{in}}\widehat{v}_{cdj}, j = 1,2,3 \tag{34}$$

$$I_{eq} = \frac{V_{in}}{9KR} \tag{35}$$

The following equations for the proposed ISOP DC-DC converter are obtained from Fig. 7:

$$\begin{cases} \frac{D_{eff}}{K}\widehat{v}_{cd1} + \frac{V_{in}}{3K}\left(\widehat{d}_{i1} + \widehat{d}_{v1} + \widehat{d}_1\right) = sL\widehat{i}_{L1} + \widehat{v}_{out} \\ \frac{D_{eff}}{K}\widehat{v}_{cd2} + \frac{V_{in}}{3K}\left(\widehat{d}_{i2} + \widehat{d}_{v2} + \widehat{d}_1\right) = sL\widehat{i}_{L2} + \widehat{v}_{out} \\ \frac{D_{eff}}{K}\widehat{v}_{cd3} + \frac{V_{in}}{3K}\left(\widehat{d}_{i3} + \widehat{d}_{v3} + \widehat{d}_1\right) = sL\widehat{i}_{L3} + \widehat{v}_{out} \end{cases} \tag{36}$$

$$\begin{cases} \frac{K}{D_{eff}}\left(\widehat{i}_{in} - sC_d\widehat{v}_{in}\right) = I_{eq}\left(\widehat{d}_{i1} + \widehat{d}_{v1} + \widehat{d}_1\right) + \widehat{i}_{L1} \\ \frac{K}{D_{eff}}\left(\widehat{i}_{in} - sC_d\widehat{v}_{in}\right) = I_{eq}\left(\widehat{d}_{i2} + \widehat{d}_{v2} + \widehat{d}_1\right) + \widehat{i}_{L2} \\ \frac{K}{D_{eff}}\left(\widehat{i}_{in} - sC_d\widehat{v}_{in}\right) = I_{eq}\left(\widehat{d}_{i3} + \widehat{d}_{v3} + \widehat{d}_1\right) + \widehat{i}_{L3} \end{cases} \tag{37}$$

$$\sum_{j=1}^{3}\widehat{v}_{cdj} = \widehat{v}_{in} \tag{38}$$

$$\sum_{j=1}^{3}\widehat{i}_{Lj} = \frac{\widehat{v}_{out}}{\left(R_c + \frac{1}{sC}\right)//R} \tag{39}$$

$$\sum_{j=1}^{3}\widehat{i}_{Lj} = \widehat{v}_{out}\left(\frac{sRC + sR_cC + 1}{R(1 + sR_cC)}\right) \tag{40}$$

The main objective for the ISOP control is to ensure equal power-sharing between the modules, such that IVS and OCS are achieved. Several control strategies are proposed to achieve IVS and OCS; one of these schemes is the common duty ratio that achieves stable operation for the ISOP converter [48]. However, proper IVS and OCS cannot be obtained due to parameter mismatch. Another control scheme that has been implemented in [62] is the input voltage feedforward charge control for two modules. However, the module's input voltage, as well as the input current, are sensed. A control scheme consisting of 3 loops has been implemented in [63,64]. These control strategies achieve IVS for the ISOP converter, where IVS control loops are required. Such techniques are classified as voltage mode control. On the other hand, the current control loop technique that is established via direct feedback of the module's output current to its corresponding current loop is commonly utilized for IPOP converters [65]. However, in ISOP converters, direct OCS control leads to system instability. Consequently, uniform power-sharing in ISOP converter systems is usually studied via directing the IVS control. Nevertheless, in [66], a stable current mode control termed as cross feedback control has been studied to achieve OCS among the modules and automatically ensuring IVS without the need for IVS control loops. In other words, a Cross-Feedback OCS (CFOCS) for ISOP has been presented in [66] to ensure both equal IVS and OCS. The presented control strategy in [66] has a fault-tolerant feature even when introducing a mismatch in the module's parameters. Besides, the output voltage regulation for the converter is simplified.

As mentioned earlier, several research studies employed voltage mode control techniques for conventional ISOP DC-DC converters because of the inherent instability for the direct OCS control. However, due to the proposed configuration shown in Fig. 3, which consists of only one single driving capacitor at the input side, the instability problem caused by the direct OCS control is avoided. Accordingly, in this paper, the control technique presented in Fig. 9 is the direct OCS control scheme. The OCS control consists of one outer output current loop and three inner current loops. The output current loop generates the common reference to the three inner current loops, where the current feedback for the individual module is its output current and not the summation of the other two output currents as presented in [66] since the proposed ISOP configuration would lead to a stable control scheme through the direct OCS control.

4.1. Output Current Sharing Control (OCS) for a 3-module ISOP

Lead-acid batteries are extensively used in LS-EVs applications because of their low-cost benefits. However, lead-acid batteries are accompanied with some disadvantages that limit their utilization in further commercial applications. These shortcomings can be highlighted in: lengthy charging process and lifetime that tends to be lower than other batteries [67]. Consequently, charging algorithms that attain fast charging and prolong the lifetime of the battery are necessary. Constant-Current Constant-Voltage (CC-CV) scheme is one of the traditional charging schemes used to charge the battery. However, this scheme results in a lengthy charging process, low efficiency, and overheating.

Since this paper mainly focuses on DC-DC converters for fast chargers, it should be noted that as the charging rate increases, the battery can be exposed to overcharging or overheating. This threatens the lifetime of the battery. Accordingly, it is crucial to terminate the charging process once the battery is fully charged to avoid overcharging the battery. Therefore, the control scheme designed for the presented power converter is current-controlled, considering a reflex charging technique that is termed as burp charging or negative pulse charging. Such an algorithm offers significant advantages that can be highlighted in: shortening the charging time and lowering the rise in temperature. Generally, the reflex charging technique consists of 3 charging sequences, which are: a positive charging pulse, a rest period where no charging occurs, and a negative charging pulse or a discharge pulse [67]. Accordingly, the designed control scheme is based on controlling the output current of the proposed ISOP DC-DC converter such that the output current profile is based on reflex charging, as seen in Fig. 9.

Fig. 9 presents the OCS control scheme for the proposed 3-module ISOP DC-DC converter. In which it consists of an outer current loop and another three inner current loops. The reference signal $\widehat{i}_{ref}$ is provided to the individual current loops by the output current loop. It can be noticed from the control structure shown in Fig. 9 that the current feedback of module 1 is its output current, and this is also applied to modules 2 and 3. In steady-state conditions, all the current feedbacks follow the common reference $\widehat{i}_{ref}$ provided by the output current loop with zero static errors. Consequently, the following equation is obtained:

$$\widehat{i}_{ref} = \widehat{i}_{L1} = \widehat{i}_{L2} = \widehat{i}_{L3} \tag{41}$$

From the KVL equation presented in Eq. (36), the control-to-output current can be found. This is done by substituting (32), (34), and substituting $\widehat{v}_{out}$ in terms of $\sum_{j=1}^{3} \widehat{i}_{Lj}$ as well as setting $\widehat{v}_{cdj} = 0$. By doing so, the following equation is obtained:

$$\begin{cases} \left(sL + R_d + \frac{R}{sRC+1}\right)\widehat{i}_{L1} + \frac{R}{sRC+1}\widehat{i}_{L2} + \frac{R}{sRC+1}\widehat{i}_{L3} = \frac{V_{in}}{3K}\widehat{d}_1 \\ \frac{R}{sRC+1}\widehat{i}_{L1} + \left(sL + R_d + \frac{R}{sRC+1}\right)\widehat{i}_{L2} + \frac{R}{sRC+1}\widehat{i}_{L3} = \frac{V_{in}}{3K}\widehat{d}_1 \\ \frac{R}{sRC+1}\widehat{i}_{L1} + \frac{R}{sRC+1}\widehat{i}_{L2} + \left(sL + R_d + \frac{R}{sRC+1}\right)\widehat{i}_{L3} = \frac{V_{in}}{3K}\widehat{d}_1 \end{cases} \tag{42}$$

Eq. (42) can be represented in a matrix form such that:

$$\begin{bmatrix} a(s) & b(s) & b(s) \\ b(s) & a(s) & b(s) \\ b(s) & b(s) & a(s) \end{bmatrix} = \begin{bmatrix} \frac{V_{in}}{3K} \\ \frac{V_{in}}{3K} \\ \frac{V_{in}}{3K} \end{bmatrix} \widehat{d}_1 \tag{43}$$

where $a(s) = sL + R_d + \frac{R}{sRC+1}$ and $b(s) = \frac{R}{sRC+1}$.

From (43), the control-to-output current transfer function is obtained as follows:

$$\widehat{i}_{Lj} = \frac{V_{in}A(s)}{B(s) - \frac{2RV_{in}}{B(s)}}\widehat{d}_1, j = 1, 2, and 3 \tag{44}$$

where

$$A(s) = s^2LRC + s(L + R_dRC) + R_d + 2R \tag{45}$$

$$B(s) = 3K\left(\begin{matrix} s^3L^2RC + s^2\left(L^2 + 2LR_dRC\right) + s\left(2LR_d + 3LR + R_d^2RC\right) \\ +R_d^2 + 3R_dR \end{matrix}\right) \tag{46}$$

The relation between the individual module input voltage and the output currents can be found using the KCL equation presented in (37). This is done by equating the first two equations in (37) and substituting (32), (34), and (35) such that:

$$\frac{V_{in}}{9KR}\left(-\frac{3KR_d}{V_{in}}\widehat{i}_{L1} + \frac{R_dD_{eff}}{RV_{in}}\widehat{v}_{cd1} + \widehat{d}_1\right) + \widehat{i}_{L1} = \frac{V_{in}}{9KR}\left(\begin{matrix} -\frac{3KR_d}{V_{in}}\widehat{i}_{L2} + \frac{R_dD_{eff}}{RV_{in}}\widehat{v}_{cd2} \\ +\widehat{d}_1 \end{matrix}\right) + \widehat{i}_{L2} \tag{47}$$

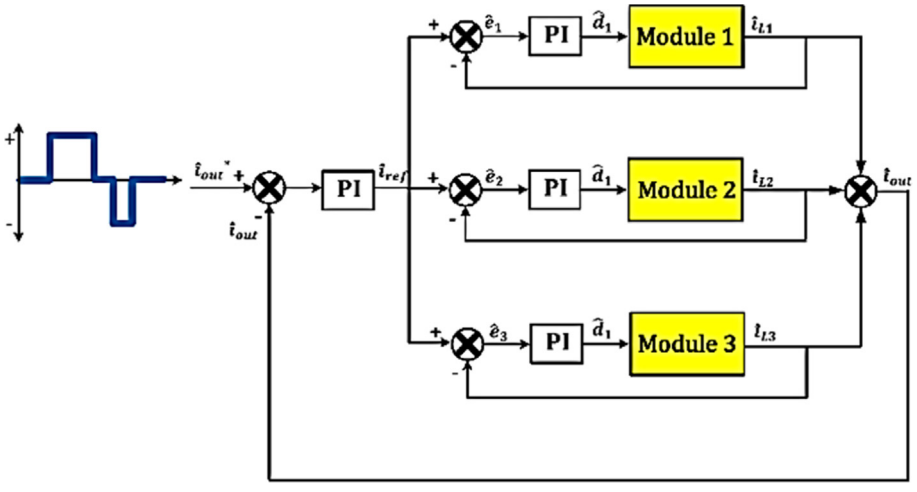

Fig. 9 OCS control scheme for the proposed 3-module ISOP.

Further simplification for (47) would result in (48).

$$\left(1-\frac{R_d}{3R}\right)\hat{i}_{L1}+\frac{R_dD_{eff}}{9KR^2}\hat{v}_{cd1}=\left(1-\frac{R_d}{3R}\right)\hat{i}_{L2}+\frac{R_dD_{eff}}{9KR^2}\hat{v}_{cd2} \quad (48)$$

From (48), the following is obtained:

$$y(\hat{v}_{cd2}-\hat{v}_{cd1})=x\left(\hat{i}_{L2}-\hat{i}_{L1}\right) \quad (49)$$

where $x=\left(1-\frac{R_d}{3R}\right)$ and $y=-\frac{R_dD_{eff}}{9KR^2}$.

From (49), $\hat{v}_{cd2}$ can be found such that:

$$\hat{v}_{cd2}=\hat{v}_{cd1}+\frac{x}{y}\left(\hat{i}_{L2}-\hat{i}_{L1}\right) \quad (50)$$

Eq. (50) can be generalized as:

$$\hat{v}_{cdj}=\hat{v}_{cd1}+\frac{x}{y}\left(\hat{i}_{Lj}-\hat{i}_{L1}\right), j=1,2,and3 \quad (51)$$

Setting $\hat{v}_{in}=0$, and substituting (51) in (38):

$$\sum_{j=1}^{3}\hat{v}_{cd1}+\frac{x}{y}\left(\hat{i}_{Lj}-\hat{i}_{L1}\right)=0 \quad (52)$$

$$3\hat{v}_{cd1}-3\frac{x}{y}\hat{i}_{L1}+\sum_{j=1}^{3}\frac{x}{y}\hat{i}_{Lj}=0 \quad (53)$$

Therefore,

$$\hat{v}_{cd1}=\frac{x}{y}\hat{i}_{L1}+\frac{x}{3y}\sum_{j=1}^{3}\hat{i}_{Lj} \quad (54)$$

Substituting (54) in (51) result in:

$$\hat{v}_{cdj}=\frac{x}{y}\hat{i}_{Lj}+\frac{x}{3y}\sum_{j=1}^{3}\hat{i}_{Lj}, j=1,2,and3 \quad (55)$$

Presenting (55) in a matrix form result in:

$$\begin{bmatrix}\hat{v}_{cd1}\\ \hat{v}_{cd2}\\ \hat{v}_{cd3}\end{bmatrix}=\begin{bmatrix}\frac{2x}{3y} & \frac{-x}{3y} & \frac{-x}{3y}\\ \frac{-x}{3y} & \frac{2x}{3y} & \frac{-x}{3y}\\ \frac{-x}{3y} & \frac{-x}{3y} & \frac{2x}{3y}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{i}_{L3}\end{bmatrix} \quad (56)$$

To study the fluctuation in the individual module's input voltage due to disturbances, it is assumed that $\hat{v}_{in}=0$, where the perturbation in $\hat{v}_{cdj}, j=1,2,and3$ is analyzed due to the disturbance in the load current.

According to the OCS control scheme block diagram shown in Fig. 9, perturbations in the load currents can be written as:

$$\begin{cases}\hat{i}_{L1}=G_{iLd}G_{PI}\left(\hat{i}_{ref}-\hat{i}_{L1}\right)\\ \hat{i}_{L2}=G_{iLd}G_{PI}\left(\hat{i}_{ref}-\hat{i}_{L2}\right)\\ \hat{i}_{L3}=G_{iLd}G_{PI}\left(\hat{i}_{ref}-\hat{i}_{L3}\right)\end{cases} \quad (57)$$

where; G_{iLd} is the control-to-output current transfer function and G_{PI} is the PI controller transfer function.

Substituting (57) in (56) would give:

$$\hat{v}_{cd1}=\frac{x}{3y}G_{iLd}G_{PI}\left(-2\hat{i}_{L1}+\hat{i}_{L2}+\hat{i}_{L3}\right) \quad (58)$$

where the term $-2\hat{i}_{L1}$ can be written as $\hat{i}_{L1}-3\hat{i}_{L1}$. Accordingly, the following generalized equation is obtained.

$$\hat{v}_{cdj}=\frac{x}{3y}G_{iLd}G_{PI}\left(-3\hat{i}_{Lj}+\hat{i}_{out}\right), j=1,2,and3 \quad (59)$$

It can be seen from the OCS control scheme block diagram that the inner feedbacks track the common reference signal $\hat{i}_{ref}$ provided by the outer output voltage loop such that: $\hat{i}_{ref}=\hat{i}_{L1}=\hat{i}_{L2}=\hat{i}_{L3}$. Furthermore, according to Eq. (59), the following is obtained.

$$\hat{v}_{cd1}=\hat{v}_{cd2}=\hat{v}_{cd3}=\frac{\hat{v}_{in}}{3}=0 \quad (60)$$

Consequently, it can be concluded from (60) that the fluctuation in the input voltage per module is unaffected and kept equal to zero even when the load current changes.

4.2. Simulation results

To offer a uniform power distribution among the modules, a dedicated power balancing control is indispensable. In this subsection, the controller is tested through a 3-module ISOP DC-DC converter rated at 4.5kW and a supply voltage of 340V. In which, parameter mismatch is introduced as presented in Table 4. In other words, to test the controller's power balancing capability when handling uncertainties, the component parameters per unit are purposely assumed to be different.

Talking about the simulation results, the control scheme presented in Fig. 9 is examined by burp charging. It can be observed from Fig. 10 that the power-sharing controller presented in Fig. 9 compensates the negative influences resulting from the system parameters mismatch. In which, the modular input voltages and the modular output currents are equally sharing among the three modules. It can be noted that the output current of the proposed DC-DC converter tracks the reference signal applied. Consequently, it can be concluded that the control scheme is reliable and achieves equal power distribution between the modules.

Fig. 11 shows the results for the output currents as well as the input voltages where the balancing concept is disabled at 0.5*s*. The system is simulated considering parameter mis-

Table 4 System parameters used in simulation.

Parameters	1st Module	2nd Module	3rd Module
Overall converter rated power	4.5kW		
Rated power per unit	1.5kW		
Total supply voltage	340V		
Input voltage per unit	113.3V		
Total output voltage	48V		
Output voltage per unit	48V		
Total number of units	3		
Turns ratio	1.89 : 1	1.79 : 1	1.69 : 1
Leakage inductance	1.1431μH	1.025μH	0.914μH
Effective duty cycle	0.8	0.759	0.717
Filter inductor	50mH	60mH	60mH
Filter capacitance	300μF		
Load resistance	0.512Ω		
Switching frequency	100kHz		

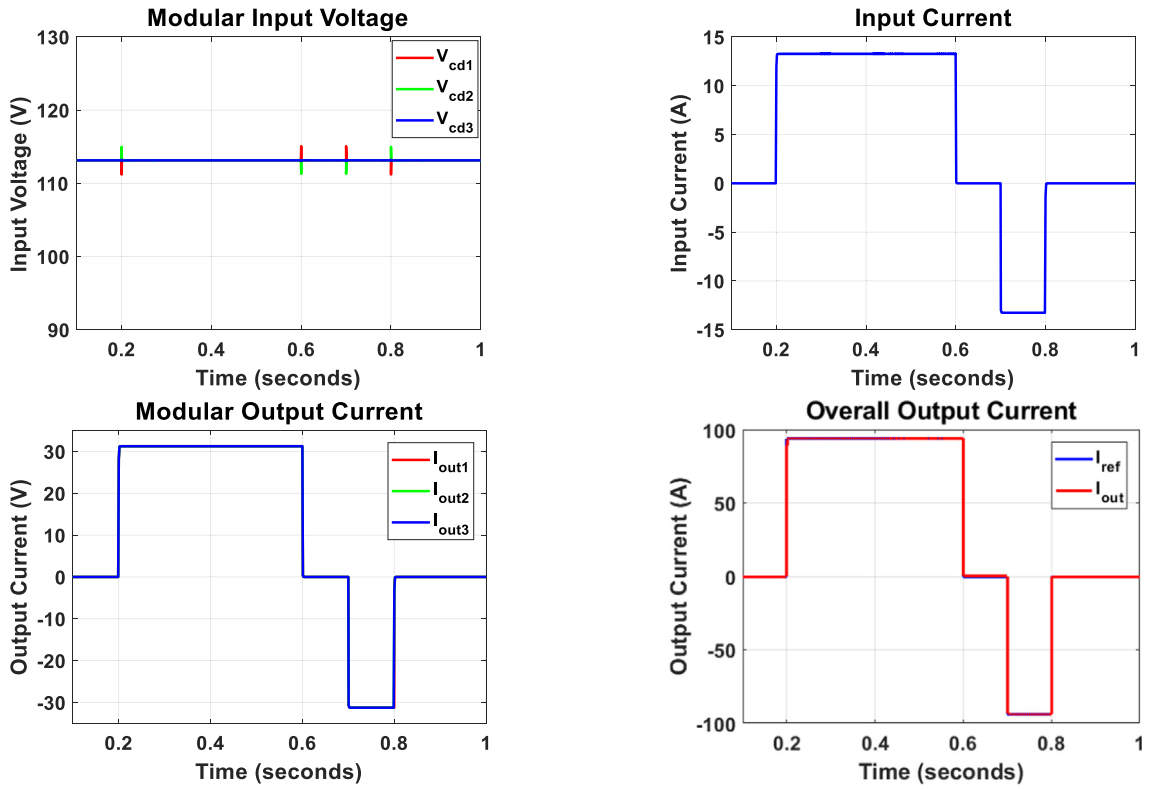

Fig. 10 Simulation Results.

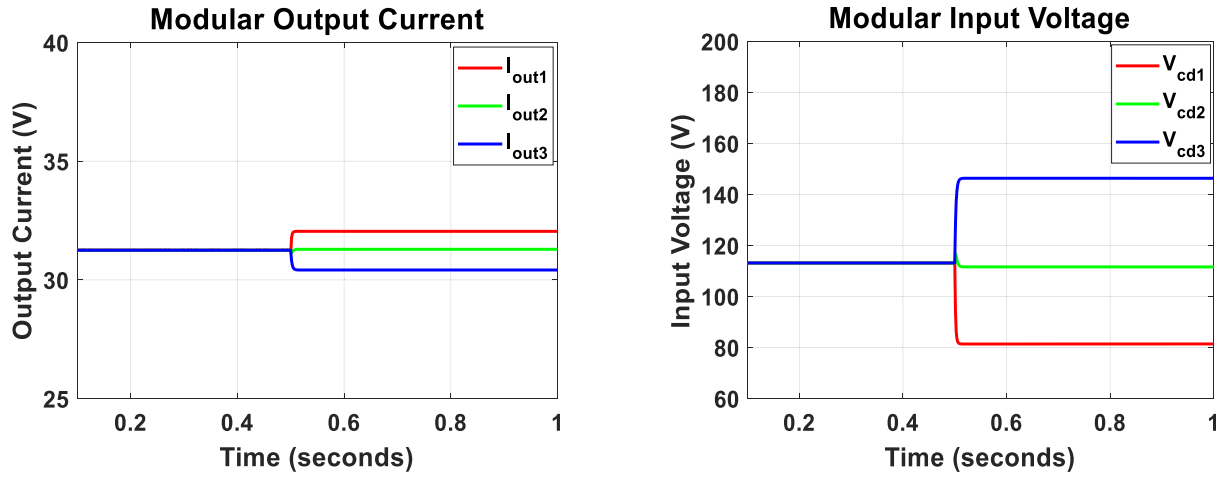

Fig. 11 Modular output currents and modular input voltages from balanced to unbalanced conditions.

match. It can be seen that the output currents, as well as the output voltages, are equally shared among the three modules up to 0.5*s*. However, after deactivating the PI controllers designed to ensure both input voltage and output current sharing, the input voltages, as well as the output currents, diverge.

To validate the operation of the power converter using software simulations and to verify the correctness of the derived small-signal model of the converter, especially under the transient conditions, a Simulink model for the 3-module ISOP DC-DC converter-based DAB topology has been conducted. Parameter mismatch presented in Table 4 and circuit parasitics, including the transformers leakage resistance, filer inductance leakage resistance, and the MOSFET and internal diode resistances, are taken into consideration in the simulated model. The control scheme shown in Fig. 9 is applied to the simulated converter, and the results are shown in Fig. 12. It is clearly shown from Fig. 12 that the modular output currents are equally shared among the three modules and that the total output current follows the reference current.

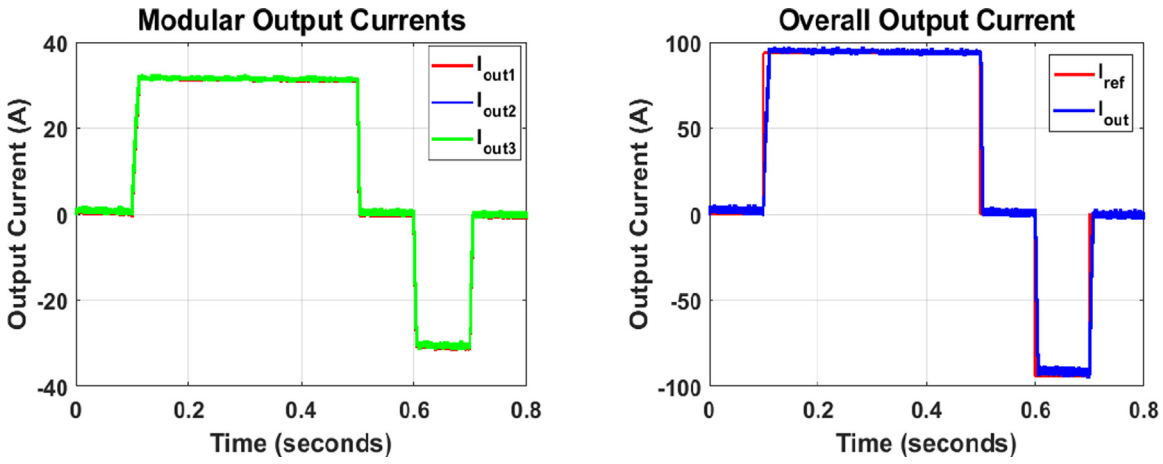

Fig. 12 Three-module ISOP DC-DC converter based DAB topology simulation results.

5. Conclusion

The main contribution of this paper is to develop a DC-DC converter for LS-EVs fast chargers. Achieving this would reduce the charging time and allow for wide LS-EVs adoption. The paper focuses on multimodule DC-DC converters for LS-EVs fast chargers due to the fact that modular power converters offer easy maintenance, redundancy, and scalability. In addition, the higher switching frequency can be achieved in the AC link, which results in weight and size reduction. Moreover, through the employment of soft switching techniques, the losses of the converter are reduced. Hence, higher efficiency can be achieved. In this regard, a generalized small-signal analysis applicable for ISIP-OSOP is provided to assist in the control design of the DC-DC converter system. The proposed DC-DC converter to achieve a fast charging process is a multimodule DC-DC converter based DAB. Three-modules are employed where each module is rated at 1.5kWto achieve the desired power rating, which is 4.5kW. Assuming that the recharging process is done from a $240VAC$ single-phase outlet and according to the mentioned specifications at the input side, a single FB converter that can handle the input current is employed. However, due to the high output current, a modular approach is required to avoid high losses and achieve the highest efficiency. In other words, the modular power stage connection based on the conventional DAB DC-DC converter is ISOP. However, the input specifications can be achieved by only one converter, and due to the high output current at the output side, more than one converter is required to avoid high power losses and achieve high efficiency. Hence, only one bridge is used at the primary side, and the modularity concept is applied to the high-frequency transformer and the second bridge.

The dynamic behavior of the multimodule converters is studied using the small-signal analysis to develop a generalized dual series/parallel input-output dual active bridge small-signal model. After deriving the generalized small-signal modeling for the ISIP-OSOP DC-DC converter, the analysis is used to study and derive the small-signal analysis for the proposed ISOP DC-DC converter and thereby designing the converter's controller and achieving equal power-sharing between the modules. To study the performance of the converter when its parameters are varied. The term $\frac{R_d}{R}$ varied, where increasing $\frac{R_d}{R}$, increases the system's damping coefficient.

Due to the configuration of the proposed DC-DC converter, equal power-sharing is achieved through a direct output current sharing control, ensuring stability without the need for input voltage sharing loops, unlike the conventional ISOP converters. This is because the proposed configuration uses only a single capacitor at the input side, avoiding the inherent instability problem caused by the output current sharing control. The control of the proposed converter is simulated to ensure the effectiveness of the presented control under parameter mismatch. The controller is tested with burp charging using a 3-module ISOP power converter rated at 4.5kW. Simulation results show that the modular input voltage and the modular output current are equally shared among the three modules.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

This publication was made possible by NPRP grant NPRP (10-0130-170286) from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

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Mena S. ElMenshawy received the B.Sc. and MSc degrees in Electrical Engineering from Qatar University, Qatar, in 2016 and 2019, respectively. She worked as a Graduate Assistant at Qatar University from 2016 to 2018. She is currently working as Research Assistant at Qatar University. Her research interests include power electronics, renewable energy, energy management, and power systems.

Ahmed M. Massoud (SM' 11) received the B. Sc. (first-class honors) and M.Sc. degrees in Electrical Engineering from Alexandria University, Egypt, in 1997 and 2000, respectively, and the Ph.D. degree in Electrical Engineering from Heriot-Watt University, Edinburgh, U.K., in 2004. He is currently a Professor at the Department of Electrical Engineering, College of Engineering, Qatar University. His research interests include power electronics, energy conversion, renewable energy, and power quality. He holds five U.S. patents. He published more than 100 journal papers in the fields of power electronics, energy conversion, and power quality.