Impact of Work Function Tunability on Thermal and RF Performance of P-type Window Based Junctionless Transistor

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Abstract. *The choice of gate metal technology for junctionless transistors needs to have diverse characteristics as metals have distinct work functions and hence, they show incompatibility while tailoring threshold of the device. In such a scenario, bimetallic stacked gate can be a promising candidate to present wide range of tunable work functions required for nano-regime junctionless transistors. This paper explores the electronic phenomena occurring at metal-metal interface and the impact of Platinum (Pt)/Titanium (Ti) bimetallic stacked gate-based work function tunability on the RF and thermal performances of p-type window-based Silicon on Insulator Junctionless Transistor (SOI JLT) using numerical simulator SILVACO ATLAS. The parameters considered for performance evaluation are ON-state current (I_{ON}), OFF-state current (I_{OFF}), I_{ON}/I_{OFF} ratio, transconductance (g_m), cutoff frequency (f_T), Transconductance Frequency Product (TFP), Intrinsic Gate Delay (IGD), intrinsic gain (A_V), and Global Device Temperature (GDT). The g_m, f_T, TFP, A_V and GDT improve for modified over conventional in the ON state at higher work function, while IGD improves at lower work function. The improvements of 11.7 % and 2.21 % are obtained in maximum g_m and f_T, respectively, for modified transistor over conventional. The findings suggest that bimetallic stacked gate modified SOIJLT is a better option than conventional for low-power RF application.*

Keywords

Bimetallic stacked gate, Junctionless Transistor (JLT), Radio Frequency (RF), Silicon-on-Insulator (SOI), thermal performance and tunable work function.

1. Introduction

Miniaturization of MOS devices faces major challenges such as Short Channel Effects (SCEs) in the nanoscale regime [1]. Downscaling of inversion mode FET devices has led to creation of effects like hot carrier effect, Drain-Induced Barrier Lowering (DIBL), poor subthreshold swing, etc. inside the device due to which performance has degraded [1]. Ultra-shallow junction is one of the solutions for SCEs in the inversion mode devices but is very complex and difficult from fabrication cost and process points of view [2]. Therefore, in 2010, researchers came up with a new device, popularly known as "Junctionless FET (JLFET)" or "gated resistor", as a plausible solution to inversion mode devices [3]. It is heavily doped semiconductor device with source, channel, and drain and all three are doped with the same uniform doping type and same concentration [3]. Hence, there is no p-n junction existing inside the semiconductor device. The operation of this gated resistor shifts from volume depletion (of channel region in OFF state) into partial depletion and subsequently

in flat band condition and accumulation region with the application of gate voltage [3].

Work function is considered as one of the important parameters for the selection of gate metal material. The gate electrode work function is utilized as an efficient tool to turn off the JLFETs by accomplishing volume depletion in the OFF state [4]. As the active layer in JLFET is heavily doped, the full depletion is achieved in JLFET at $V_{GS} = 0$ V. A gate electrode with a high work function (>= 5.1 eV) is required for n-JLFETs, while one with low work function (<= 4.1 eV) is required for p-JLFETs [4]. This is in direct contrast to the work function requirements of conventional FET devices [5]. Interestingly, a suitable range of work functions (5.0 eV to 5.3 eV), also termed as work function window, has been suggested to obtain optimum performance from junctionless transistor for low-power applications in a nanoscale regime [6]. The effect of single metals on RF performance of junctionless transistors has already been presented in [7].

The SOI JLTs (Silicon-on-Insulator Junctionless Transistors) have the planar architecture compatible with Complementary Metal Oxide Semiconductor (CMOS) technology, and they have a single top gate. The polysilicon gates have been replaced by the metal gates due to the poly-depletion effects and the penetration of dopants through the gate dielectric layer [8]. The available options of metals have different work functions which are suitable for n-type and p-type JLTs [9]. The benefit of polySi gate is that its effective work function (EWF or Φ_{meff}) could be modified depending on doping concentration, but the purest metals have inherent value, so their EWF cannot be modified [10]. If some metal has the required value of work function needed for the desired threshold voltage at gate, then there are problems with its thermal stability and adhesiveness to dielectric and semiconductor materials. To tailor the threshold voltage of the device, a strong approach is carried out when the gate material should have a tunable work function [5]. Therefore, gate metals with tunable work function are highly preferable for CMOS integration [11].

Various gate electrode technologies to achieve tunable work function have been investigated, such as metal silicides [12], metal nitrides [13], [14] and [15], binary metal alloys [16], [17], [18] and [19] and bimetal stacks [20], [21] and [22]. Among these, bimetallic stacked gate has shown a wider range of work function tunability and ease of deposition [20].

This paper aims to explore the electronic phenomena taking place at metal-metal interface. Then, the impact of Platinum (Pt)/Titanium (Ti) bimetallic stacked gate-based work function tunability is studied on the RF and thermal performance of p-type window-based SOI JLT. The parameters considered for performance evaluation are ON current (I_{ON}), OFF-state current (I_{OFF}), transconductance (g_m), cutoff frequency (f_T), Transconductance Frequency Product (TFP), Intrinsic Gate Delay (IGD), intrinsic gain (A_V), and Global Device Temperature (GDT). The remaining part of this paper is organized as follows: Sec. 2. explains the electronic phenomena taking place at the metal-metal interface. The proposed device structure, its process flow and its simulation methodology are discussed in Sec. 3. , Sec. 4. and Sec. 5. correspondingly. Section 6. discusses the simulation results of the proposed JLT transistor and compares the performance parameters with conventional JLT. Section 7. concludes the work.

2. Tunable Work Function Using Bimetallic Stacked Gate

In a bimetallic stacked gate, two different metals are grown over the gate dielectric sequentially in stacked manner, providing that bottom metal touching the dielectric should be much thinner than the top metal. Herein, the work function can be tuned to desired value by varying the bottom metal thickness, assuming that top metal is thick enough [20]. The effective work function value ranges between the work functions of two metals used.

The more accurate explanation of this work function tunability is based on quantum size effects as the thickness of the bottom metal decreases continuously [20]. The two isolated distinct metals possess the same vacuum level (E_{vac}) but their respective Fermi levels (E_{F1} for metal-1 and E_{F2} for metal-2) are different for them due to the varying of work function (Φ_m) from metal to metal [23], as shown in Fig. 1(a) [20]. It is assumed that metal-1 has lower work function than metal-2 ($\Phi_{m1} < \Phi_{m2}$).

Considering the sharp atomic profiles and no interdiffusion between the two metals, when two metals are in electrical contact with each other, an interface is formed in intimate contact. By virtue of chemical equilibrium, the chemical potential should be constant throughout the interface, which means that Fermi level of two metals should be constant at equilibrium near the interface [24].

Therefore, electrons will flow from lower work function of metal-1 to higher work function of metal-2 and increase the density of states, until Fermi level gets aligned and becomes the same for both metals (Fig. 1(b)). As a result, metal-1 is depleted of electrons and metal-2 has an excess of electrons. The concluding space charge, positive in metal-1 and negative in metal-

2, forms an interface dipole layer composed of positive ion cores (metal-1) and displaced free electrons (metal-2) [23]. The resulting potential distribution ($\Phi(x)$) and charge density ($\rho(x)$) is depicted in Fig. 1(b).

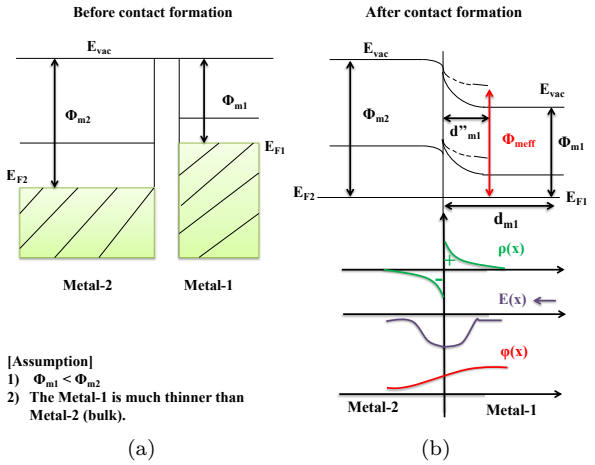


Fig. 1: Band structure of metal-metal interface (a) before contact formation and (b) after contact formation [20].

Due to dipole created, there lies an electric field ($E(x)$) which confirms that the vacuum level (E_{vac}) becomes sloppy in nature [24], as shown in Fig. 1(b). Because of 'screening' phenomena in metals, free electrons near charge in dipole distribution get polarized and redistribute to lower the energy of the system. The dipole width remains limited to a few Angstroms only. In the bulk region, this effect vanishes not abruptly but continuously. Hence, the position of Evac also changes continuously moving from interface to bulk and the separation of E_F (Fermi level) and E_{vac}) (vacuum level) attains constant value in the bulk of metal.

From Fig. 1(b), it is observed that in the case of thick metal-1 (thickness d_{m1}), the electron redistribution process (electron transfer from metal-1 to metal-2) will cause less change in electron density as compared to the bulk state in metal-1. Thus, in thick metal-1, junction depth will be shorter and, at gate dielectric, value of work function Φ_{m1} will appear. In the case of very thin metal-1 (thickness d''_{m1}), the electron density will be drastically reduced. Consequently, this will increase junction depth and a modified value of work function will appear on the gate dielectric ($\Phi_{m1} < \Phi_{meff}$) [20].

Some researchers have presented a model for band alignment for the multi-metal gated MOS structure [8]. An analytical model for the Effective Work Function (EWF) of a bimetallic stacked gate has been proposed [25]. According to this,

$$\Phi_{meff} = \frac{d_{m1}}{\tau}\Phi_{m1} + \left(1 - \frac{d_{m1}}{\tau}\right)\Phi_{m2}, \qquad (1)$$

where $0 < d_{m1} < \tau$. 'τ' is known as the transition length near the interface, which depends on the annealing conditions, and is the length over which the entire range of tunable work function is obtained, varying from work function of the first metal to that of the second metal. Here, Φ_{meff} is the effective work function, Φ_{m1} is work function of metal-1, Φ_{m2} is work function of metal-2 and dm1 is thickness of metal-1. This model considers no intermixing between the top metal and the gate dielectric and, hence, the bottom metal also serves as a barrier layer between the two. The analytical variation of bimetallic stacked gates such as Ti/Au and Ni/Au has been found to be in consistent with experimental results [10].

The relative order of metal layers profoundly affects the electrical behavior of transistors. If electrons are dominant in the gate structure, then the bottom metal having a lower Φ_m and top metal having a higher Φ_m will make improper arrangement as during the redistribution process bottom will become depleted of electrons, which will ultimately produce gate depletion effects, thus slowing down the switching speed of the transistor. But if order is reversed (top metal with low Φ_m and bottom metal with high Φ_m), electrons will accumulate in bottom metal, thus increasing the population density, which successively decreases gate depletion and increases the current drive and speed of transistor. The gate structure with dominant carriers as holes forms proper arrangement when bottom metal has low Φ_m while the top metal has high Φ_m [26].

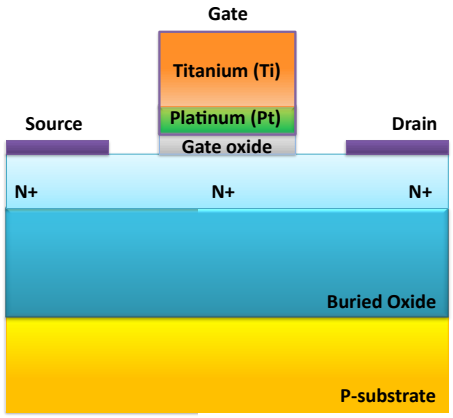
The Pt/Ti bimetallic stack is used in this work because it shows a wide EWF range varying from Ti (3.9 eV) to Pt (5.3 eV), nearly $\sim$ 1.4 eV and this range is obtained after 300 °C FGA annealing with $\tau \sim 6$ nm [27]. Due to the consideration of n-channel JLT here, Pt having a higher Φ_m has been placed at the bottom layer.

3. Device Structure & Specification

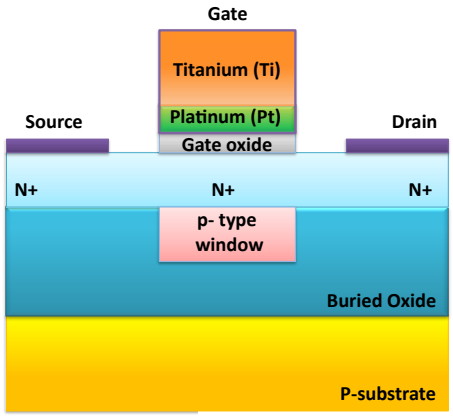
The cross-sectional views of the proposed bimetallic stacked gate-based conventional SOI JLT (BSG_CSJLT) and modified SOI JLT (BSG_MSJLT) device structures are shown in Fig. 2(a) and Fig. 2(b) respectively. The BSG_MSJLT has a planar SOI structure with source, drain, and channel doped with the same n-type impurity and concentration, thus eliminating metallurgical junctions like those that exist in conventional SOI-MOSFET.

In addition, a p-type window is opened in the buried oxide layer and is in vertical alignment with the channel and gate. The reason is that it will help to achieve full depletion and reduced OFF state leakage by reduc-

ing the effective channel thickness. The opened window has length 22 nm, i.e. the same as that of the channel. The structural parameters for designing the p-type window-based modified SOI JLT are tabulated in Tab. 1. It merits referencing that structural parameters of modified SOI JLT are carefully coordinated according to the description in [28]. The proposed modification to the gate electrode is implemented by stacking platinum (bottom metal) and titanium (top metal) over gate oxide. Titanium (Ti) has a fixed thickness of 30 nm while platinum (Pt) thickness is kept variable as it will help to tune the desired work function but is kept below the transition length ($\tau \sim 6$ nm) [27]. To analyze the impact on the performance parameters of the junctionless devices, the work function range considered is from 5.0 to 5.3 eV. The specifications for BSG_CSJLT are the same as those for BSG_MSJLT except that it does not have a p-type pocket window.



(a)



(b)

Fig. 2: Two-dimensional structures of (a) BSG_CSJLT and (b) BSG_MSJLT.

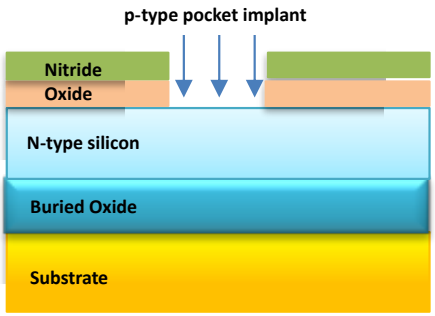
4. Process Flow

The process flow for fabricating the BSG_MSJLT is included in Fig. 3. To obtain the final structure of the proposed device, smart-cut technique [29] to generate a silicon film thickness of 10 nm is used and is followed by the stages as outlined.

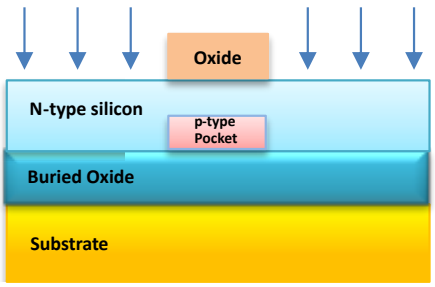
Low-dose Separation by Implanted Oxygen (SIMOX method) can be used to produce oxide on both sides of the doped pocket [30] and [31]. As demonstrated in Fig. 3, oxygen ions can be implanted with appropriate doses and optimal implant energies ($2.5 - 4.8 \cdot 10^{17}$ O^+ cm^{-2} at optimized implant energies of $70 - 140$ KeV) [31] and [32].

The formation of the gate can be carried out by sequentially depositing the two metals with different work functions over gate oxide using the E-beam evaporation method. Later, the gate stack is subjected to Forming Gas Anneal (FGA) after the plasma gate etch [27]. The annealing temperature decides the transition length formed at the contact of two metals, over which a tunable work function range is obtained.

(a) n-type doped top layer of SOI wafer.



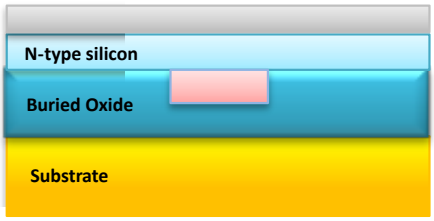
(b) Oxidation, Nitridation and etching gate to implant p-type pocket.



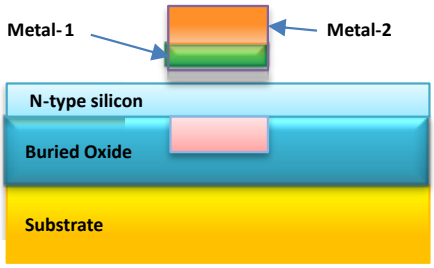
(c) Oxide realisation using low dosage SIMOX technique.

Tab. 1: Structural parameters considered for BSG_MSJLT device simulation.

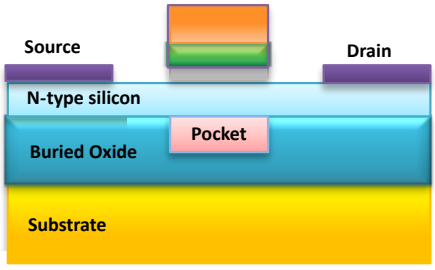
S. no.	Parameter name	Symbol	Parameter value	Unit
1	Gate length	L_g	22	nm
2	Channel thickness	t_{si}	10	nm
3	Gate oxide thickness (EOT)	t_{ox}	1	nm
4	Buried oxide thickness	t_{box}	80	nm
5	Gate work function	Φ_m	5, 5.1, 5.2 and 5.3	eV
6	Opened window thickness	T_{ow}	25	nm
7	Active region doping (n-type)	N_D	$1 \cdot 10^{19}$	cm^{-3}
8	Opened window doping (p-type)	N_{ow}	$1 \cdot 10^{13}$	cm^{-3}
9	Substrate doping (p-type)	N_A	$1 \cdot 10^{18}$	cm^{-3}



(d) Top layer gate oxidation.



(e) Sequential deposition of two distinct gate metals by E-beam evaporation followed by annealing.



(f) Source and Drain contact formation.

Fig. 3: Proposed process flow for fabricating BSG_MSJLT.

5. Simulation Environment and Methodology

The simulation of device structures and extraction of various parameters has been carried out using the SILVACO ATLAS-2D device simulator. To represent exact re-enactment, various physical models available in ATLAS 2D device simulator, which are essentially desired for deep submicron device simulation, have been employed [35]. The fermidirac statistics is used due to heavy doping in the channel region. The Energy Balance Transport model is enabled using hcte in the model statement, which sets the solution for electron and hole balance. In energy balance model: Poisson's equation, carrier continuity equations, and energy balance equations for mobile carriers are solved self-consistently. The self-heating equation is combined with the aforementioned equations to consider the heat generation within the device. Selberrher's impact ionization model is set using an impact selb statement. The lat. temp model is also initialized to account for solution of lattice energy balance equation. The required thermal boundary condition is included by defining a thermal contact at bottom of the device fixed at 300 K using the thermcontact statement. Various other physical models included are bgn to consider bandgap narrowing effects, bbt.std model to analyze the effects of band-to-band tunneling, cvt to incorporate mobility dependence on channel doping and both transverse and longitudinal electric fields, srh to include Shockley-Read- Hall recombination for the fixed minority carrier lifetime, and auger model to consider Auger recombinations.

The numerical method chosen is block newton to calibrate the device solutions for given bias voltages. To approve the SILVACO ATLAS tool, the simulation setup is calibrated with simulation results of [28] which are already calibrated with experimental results of [33].

6. Results and Discussion

The experimental and analytical variations of effective work function (Φ_{meff}) with changing thickness (d_{m1}) of bottom metal-1 platinum (Pt) are plotted in Fig. 4, considering the equivalent MOS capacitor structure (included in Fig. 4). Here, the transition length (τ) is considered to be 6 nm, obtained at 300 °C FGA (Forming Gas Anneal) condition [27]. It can be seen that the effective work function ranges from 3.9 eV (Ti only) to 5.3 eV (Pt only) for Pt thickness variation $0 < d_{m1} < 6$ nm [27]. Thus, a wide range of tunable work function ($\sim$ 1.4 eV) can be achieved with the Pt/Ti bimetallic stacked gate. The percentage difference between experimental and analytical EWF is

found to be a maximum of 6.68 %, which is very satisfactory (less than 10 %).

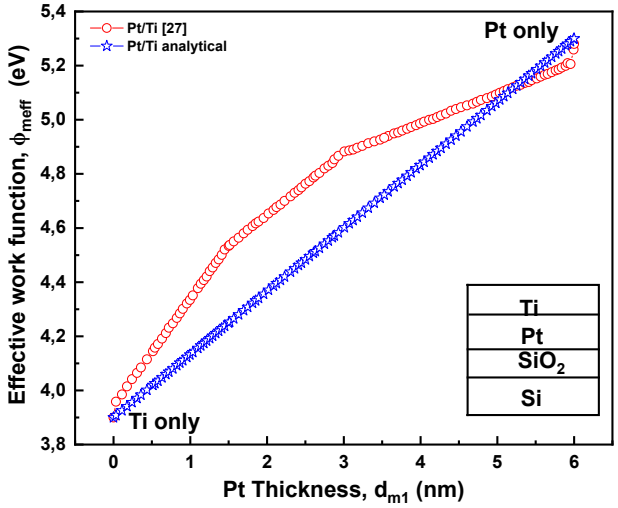
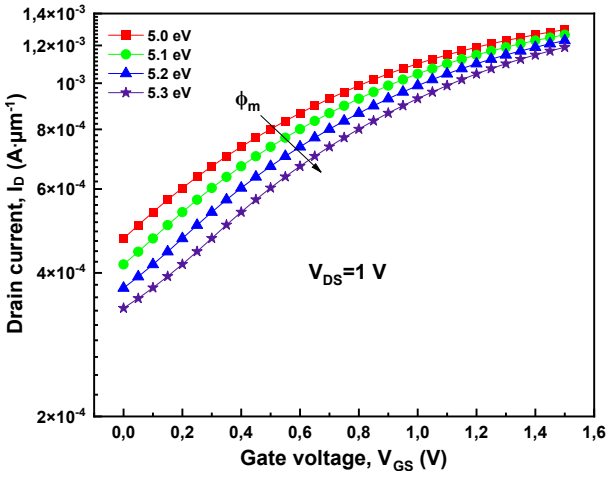


Fig. 4: The experimental and analytical variation of effective work function (Φ_{meff}) with platinum metal thickness (d_{m1}).

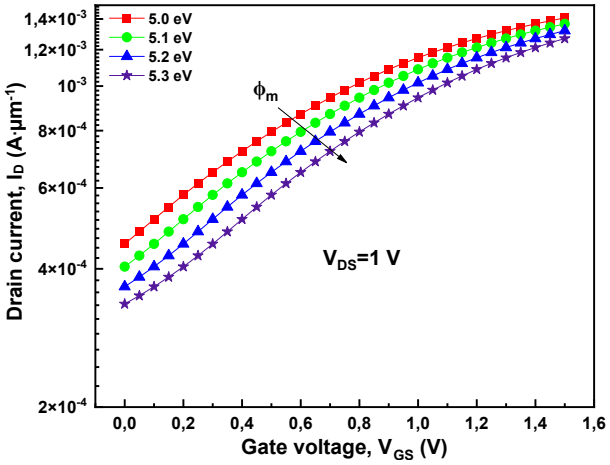
The role of gate metal work function in operating junctionless devices is very critical. The device performance is altered by the gate metal work function, since the flatband voltage varies linearly with work function. Normally, JLT is an ON device, so the channel should be fully depleted to stop conduction in the OFF state. With increasing gate metal work function, the threshold shifts towards positive value in n-channel JLT.

Figure 5 shows the transfer characteristics (I_D-V_{GS}) of SOI JLTs plotted on logarithmic scale. The OFF state is assumed to be at $V_{GS} = 0$ V and ON state at $V_{GS} = V_{DS} = 1$ V. The OFF-state current (I_{OFF}) decreases with increasing work function because increased Φ_m results in the reduction of minimum potential in the channel region, thus providing better supervision in OFF state. This effectively reduces static power dissipation inside the device. As observed from Fig. 5, the BSG_MSJLT shows lower leakage than the BSG_CSJLT, due to better depletion achieved in channel region owing to reduced channel thickness in the BSG_MSJLT. Table 2 clearly depicts this leakage current reduction improvement of BSG_MSJLT at each work function value. The basic weakness of SOI JLT is relatively low I_{ON}/I_{OFF} ratio and can be corrected by grading the drain doping level [34].

In the ON state, a reduction in ON current (I_{ON}) is observed at higher work function values as the presence of electrons in the channel is not eased at higher work function. Improved I_{ON} is obtained in BSG_MSJLT (Fig. 5(b)) over BSG_CSJLT (Fig. 5(a)) because of enhanced electron mobility due to mitigated lattice heating. Hence, the combined effect of lower I_{OFF} and higher I_{ON} increases the I_{ON}/I_{OFF} ratio of BSG_MSJLT more than that of BSG_CSJLT, as presented in Table 2. Thus, the relative switching power will always be greater than 1. The effect of higher Φ_m is more pronounced in I_{OFF} than in I_{ON}, hence, I_{ON}/I_{OFF} ratio also enhances at higher work function. This improvement nature is consistent with results of [2].



(a)



(b)

Fig. 5: Drain Current (I_{DS}) variation against gate voltage (V_{GS}) on logarithmic scale for (a) BSG_CSJLT and (b) BSG_MSJLT.

Figure 6 depicts transconductance (g_m) variation against gate voltage (V_{GS}) for different gate metal work functions at a drain voltage of 1 V. The transconductance (in Eq. (2)) behaviors at different work functions are very much similar to each other. The only difference is that the gate voltage at which maximum g_m appears shifts towards a positive voltage value with increasing work function. This gate voltage shift is explained by the linear dependence of flatband voltage on the work function. From Fig. 6, it is evident that in comparison to BSG_CSJLT (Fig. 6(a)), an improvement of 11.7 % is achieved in the maximum g_m for

BSG_MSJLT (Fig. 6(b)). This effect of work function on the maximum g_m of both devices is tabulated in Tab. 2.

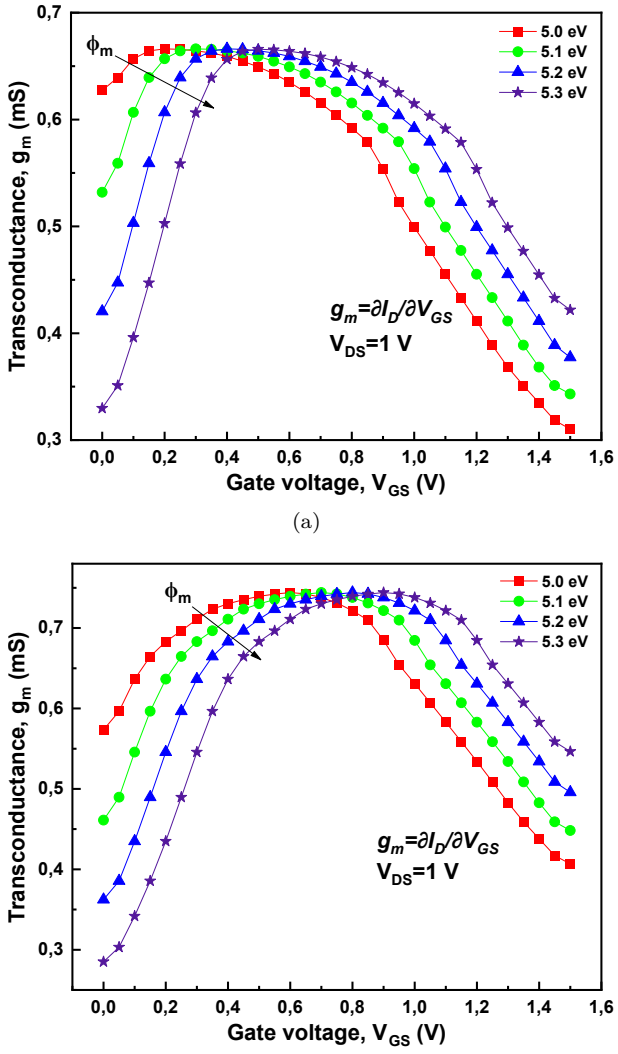


Fig. 6: Transconductance (g_m) variation against gate voltage (V_{GS}) for (a) BSG_CSJLT and (b) BSG_MSJLT.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{2}$$

Figure 7 shows output characteristics (I_D-V_{DS}) at different gate work functions for both devices. The gate voltage is varied from 0.5 V to 2 V with a step of 0.5 V. Higher work function results in a decreased ON-state current in the saturation region. At different gate voltages, the BSG_MSJLT (Fig. 7(b)) is driving larger amount of current than the BSG_CSJLT (Fig. 7(a)). This performance improvement is reflected at each work function value, thus, making the BSG_MSJLT more suitable for driving a larger amount of current even at smaller drain voltage (V_{DS}) than the BSG_CSJLT.

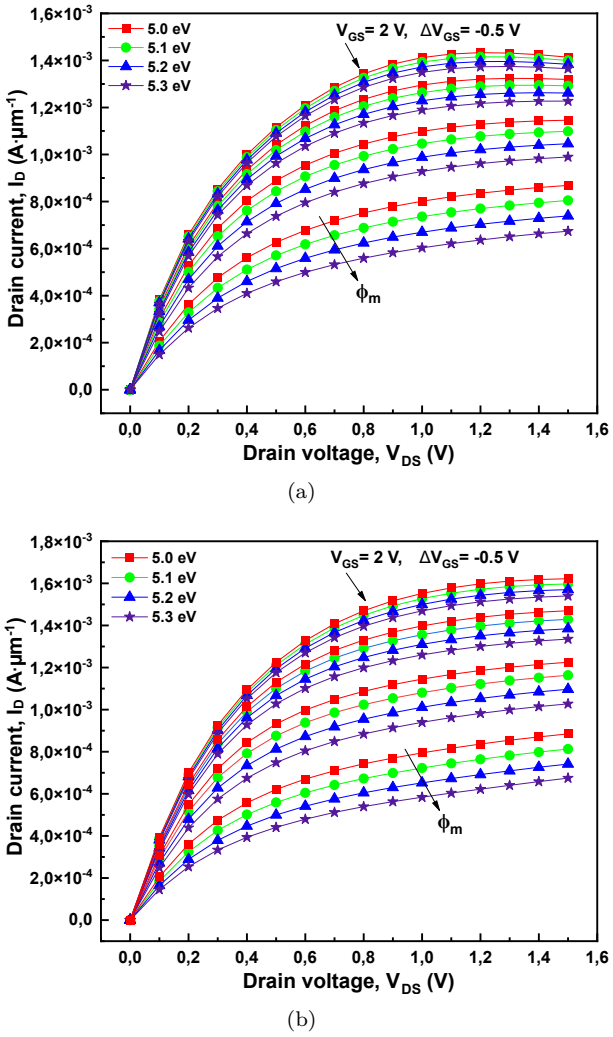


Fig. 7: Drain current (I_{DS}) variation against drain voltage (V_{DS}) for (a) BSG_CSJLT and (b) BSG_MSJLT.

Figure 8 shows the plots for gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) measured against the gate voltage at different work functions. It is obtained by performing small signal analysis with V_{DS} = 1 V and frequency of 100 MHz, after dc analysis. The capacitances increase with increase in gate voltage. No improvement was obtained in the capacitance values with increasing gate metal work function, only the position of occurrence has shifted towards positive gate voltage due to change in flatband voltage. In comparison, it is observed that at each gate work function value, C_{gd} is reduced for BSG_MSJLT (Fig. 8(b)) over that of BSG_CSJLT (Fig. 8(a)), but BSG_MSJLT shows increased C_{gs} over BSG_CSJLT. This is only due to the additional capacitive coupling effect arising between the gate and source terminal due to the p-n junction formed in the vertical direction of the n-type channel and p-type window.

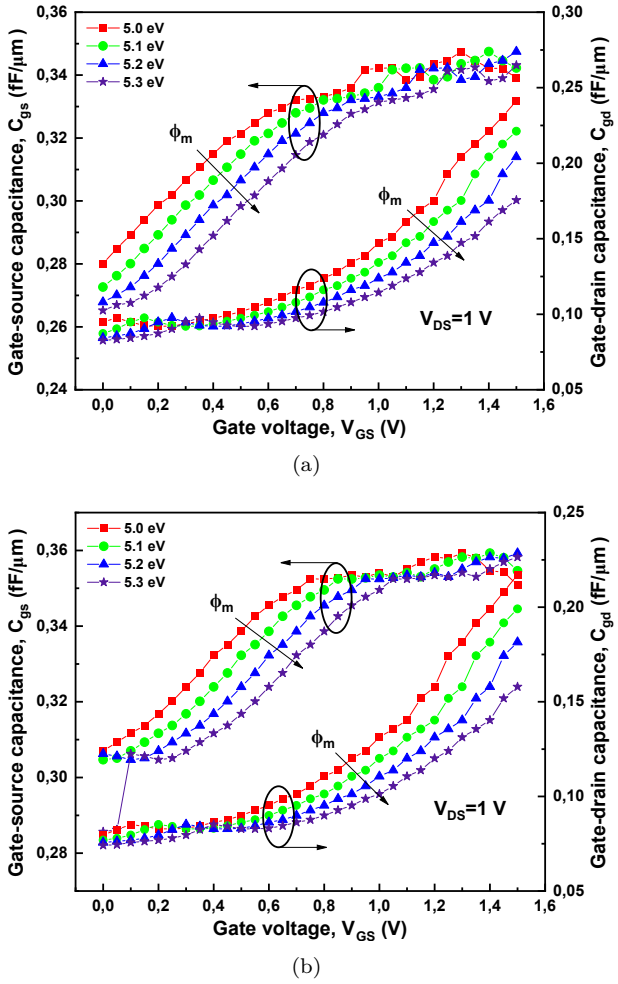


Fig. 8: Gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) measured against the gate voltage (V_{GS}) for (a) BSG_CSJLT and (b) BSG_MSJLT.

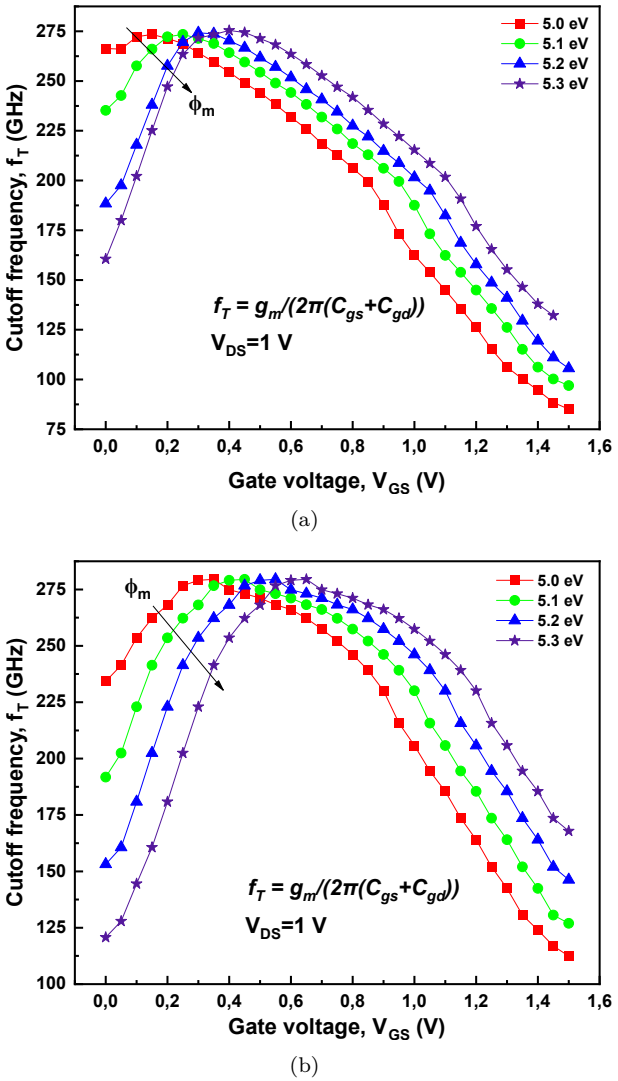


Fig. 9: Cutoff frequency (f_T) variation against gate voltage (V_{GS}) for (a) BSG_CSJLT and (b) BSG_MSJLT.

Figure 9 shows the effect of different gate work functions on cutoff frequency or transition frequency (f_T) of junctionless transistors. It is the frequency at which the device reflects unity gain. Hence, higher f_T is always desirable to suit for RF application. Also, the position of plot has shifted to more positive gate voltage with increasing work function due to increased device threshold.

As illustrated in Fig. 9(b), BSG_MSJLT shows a maximum f_T of 279.51 GHz, which is approximately 2.21 % improvement over the maximum f_T of 273.45 GHz shown by BSG_CSJLT (see Fig. 9(a) and Tab. 2). The increase in C_{gs} was compensated by increased g_m and decreased C_{gd} and BSG_MSJLT still manages to produce higher f_T.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{3}$$

Figure 10 shows Global Device Temperature (GDT) of both devices changing with drain voltage, with varying work function. Global temperature of device increases with increasing drain voltage as electron movement in the channel rises with V_{DS} due to which more thermal heat is transferred from carrier to the lattice. The GDT has decreased considerably with increasing work function value. The highest rise in temperature in BSG_MSJLT (Fig. 10(b)) at $V_{DS} = 1.5$ V and at $\Phi_m = 5.0$ eV is still less than 500 K, while GDT rises up to 600 K in BSG_CSJLT (Fig. 10(a)). Thus, it is evident that BSG_MSJLT greatly reduces the device thermal heating issue. This reduction in temperature is attained due to the insertion of lightly doped p-type window in BSG_MSJLT which facilitates dissipation of heat on increasing drain voltage.

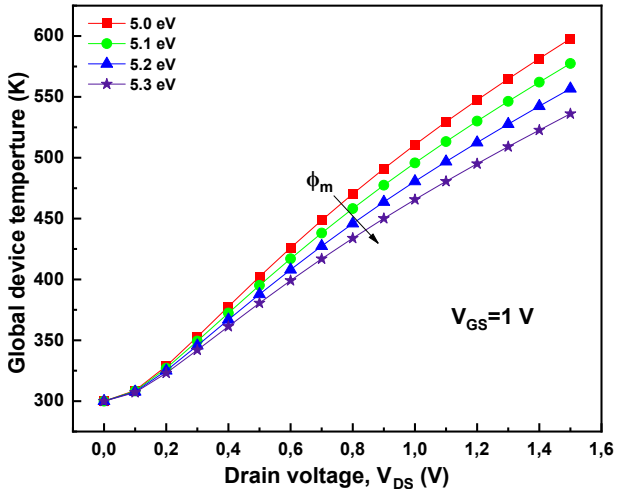
In Tab. 2, the proposed device BSG_MSJLT shows ON/OFF ratio better than BSG_CSJLT with open window doping ($N_{ow} = 1 \cdot 10^{13}$ cm^{-3}) but it is not ap-

Tab. 2: Performance comparisons of BSG_CSJLT, BSG_MSJLT and R_DGJLFET [6] in work function range from 5.0 eV to 5.3 eV.

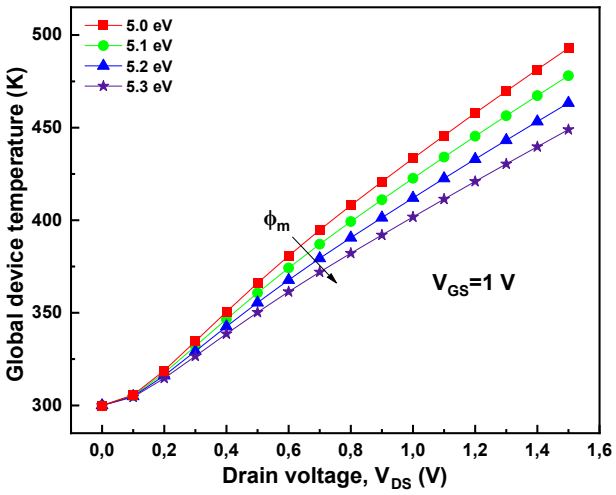
S. No.	Parameters	Work function							
		5.0 eV				5.1 eV			
		BSG_ CSJLT	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{13}$ cm^{-3})	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{20}$ cm^{-3})	R_DG JLFET [6]	BSG_ CSJLT	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{13}$ cm^{-3})	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{20}$ cm^{-3})	R_DG JLFET [6]
1	I_{OFF} (mA)	0.472	0.453	$8.41e^{-10}$	$1.1e^{-9}$	0.416	0.404	$1.5e^{-11}$	$3e^{-11}$
2	I_{ON} (mA)	1.098	1.152	0.387	1.09	1.046	1.087	0.221	0.859
3	I_{ON}/I_{OFF}	2.32	2.54	$7.15e^{8}$	$9.8e^{8}$	2.51	2.69	$1.4e^{10}$	$2.7e^{10}$
4	g_m (max) (mS)	0.666	0.744	1.83	~ 2.2	0.666	0.744	1.83	~ 2.2
5	f_T (max) (GHz)	273.45	279.51	751.03	-	273.45	279.51	751.03	-
S. No.	**Parameters**	**Work function**							
		5.2 eV				**5.3 eV**			
		BSG_ CSJLT	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{13}$ cm^{-3})	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{20}$ cm^{-3})	R_DG JLFET [6]	BSG_ CSJLT	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{13}$ cm^{-3})	BSG_ MSJLT ($N_{ow} = 1 \cdot 10^{20}$ cm^{-3})	R_DG JLFET [6]
1	I_{OFF} (mA)	0.371	0.367	$2.69e^{-11}$	$8.9e^{-13}$	0.337	0.335	$5.17e^{-12}$	$2.9e^{-14}$
2	I_{ON} (mA)	0.988	1.02	0.058	0.608	0.928	0.943	0.009	0.365
3	I_{ON}/I_{OFF}	2.66	2.77	$2.1e^{9}$	$6.7e^{11}$	2.75	2.81	$4.6e^{9}$	$1.2e^{13}$
4	g_m (max) (mS)	0.666	0.744	1.83	~ 2.2	0.666	0.744	1.83	~ 2.2
5	f_T (max) (GHz)	273.45	279.51	751.03	-	273.45	279.51	751.03	-

preciable due to very low value. However, by increasing the doping level of open window to $N_{ow} = 1 \cdot 10^{13}$ cm^{-3} [36], the ON/OFF ratio can be increased by manifolds even greater than 10^6, thus, maintaining the reliability of the device.

Table 3 summarizes the RF and thermal performance comparison between BSG_MSJLT and BSG_CSJLT. Various values of analog/RF parameters are calculated for different work functions in the ON state (at $V_{GS} = V_{DS} = 1$ V) using small signal ac analysis at 100 MHz.



(a)



(b)

Fig. 10: Global device temperature variation against drain voltage (V_{DS}) for (a) BSG_CSJLT and (b) BSG_MSJLT.

$$A_V = \left(\frac{g_m}{g_d}\right), \tag{4}$$

$$\text{TFP} = \left(\frac{g_m}{I_{DS}}\right) \cdot f_T, \tag{5}$$

$$\text{IGD} = \left(\frac{V_{DD}}{I_{ON}}\right) \cdot C_{gg}. \tag{6}$$

The transconductance (g_m) value is observed to increase with increasing work function in the ON state for both devices but g_m is always higher for BSG_MSJLT

Tab. 3: RF and thermal performance comparisons of BSG_CSJLT and BSG_MSJLT in the ON state ($VGS = VDS = 1$ V) in work function range from 5.0 eV to 5.3 eV.

S. No.	Parameters	Work function			
		5.0 eV		5.1 eV	
		BSG_CSJLT	BSG_MSJLT	BSG_CSJLT	BSG_MSJLT
1	g_m (mS)	0.499	0.631	0.554	0.685
2	f_T (GHz)	162.37	205.77	187.54	230.09
3	A_v	2.468	2.588	2.714	2.816
4	GDT (K)	510.68	433.35	495.73	422.65
5	TFP(GHz·V^{-1})	73.71	112.55	99.20	145.18
6	IGD (psec)	0.445	0.420	0.449	0.435
S. No.	Parameters	Work function			
		5.2 eV		5.3 eV	
		BSG_CSJLT	BSG_MSJLT	BSG_CSJLT	BSG_MSJLT
1	g_m (mS)	0.591	0.722	0.603	0.738
2	f_T (GHz)	201.55	246.14	215.42	257.41
3	A_v	2.868	2.967	2.90	3.043
4	GDT (K)	480.63	412.04	465.68	401.73
5	TFP(GHz·V^{-1})	120.52	174.02	139.80	201.29
6	IGD (psec)	0.462	0.455	0.480	0.477

than for BSG_CSJLT at the corresponding work function in the ON state. The carrier transport efficiency is improved with improvement in g_m, thus, making BSG_MSJLT preferable for low-voltage analog/RF applications. Similar trends have been observed with other analog/RF parameters, namely cutoff frequency (f_T), Transconductance Frequency Product (TFP), Intrinsic Gate Delay (IGD), and intrinsic gain (A_V).

The cutoff frequency f_T for BSG_MSJLT remains above 200 GHz in the ON state (see Tab. 3), for work function range of 5.0 eV–5.3 eV, while it drops below 200 GHz for lower work function in case of BSG_CSJLT. Hence, BSG_MSJLT is giving out higher f_T and, thus, it will achieve high gate controllability over the channel region. In the ON state, intrinsic gain (given by Eq. (4)) is maintained greater than 1 and thus, prominent amplification can still be achieved. Also, the A_V for BSG_MSJLT is higher than that of BSG_CSJLT at all corresponding work function values.

Table 3 also presents values of TFP calculated in ON state and formulated by Eq. (5). The power-bandwidth trade-off of a device is obtained from TFP and is also required in design of moderate speed circuits. TFP is found to be increasing with increasing work function which is self-explanatory because the individual effect of work function on f_T, g_m and I_{DS} together appears in TFP. BSG_MSJLT delivers larger TFP than the BSG_CSJLT, thus, increasing the applicability of BSG_MSJLT for RF domain.

The dynamic performance of the device is evaluated by the Intrinsic Gate Delay (IGD) and is formulated by Eq. (6). Lower work function helps to reduce the IGD. In Tab. 3, the minimum intrinsic gate delay of 0.42 psec has been achieved for BSG_MSJLT at 5.0 eV in the ON state, while it is 0.445 psec for BSG_CSJLT. Thus, BSG_MSJLT is relatively faster than BSG_CSJLT in the ON state. However, there is a trade-off between static and dynamic performance as higher work function causes lower OFF-state current and also leads to larger delays, thus degrading dynamic performance.

In Tab. 3, it can be seen that Global Device Temperature (GDT) also decreases with increasing work function in the ON state. BSG_MSJLT gives out reduced lattice heating with GDT of 401.73 K at 5.3 eV, while BSG_CSJLT produces a global temperature of 465.68 K.

7. Conclusion

The impact of work function tunability on thermal and RF performance of BSG_MSJLT has been explored and compared with the performance of BSG_CSJLT. High work function tuning has increased gate controllability in BSG_MSJLT and thus, I_{OFF} has reduced and better I_{ON}/I_{OFF} ratio is produced over BSG_CSJLT. Increasing work function has increased the parasitic capacitances. No effect has occurred on maximum value of g_m and f_T with changing work function. The C_{gd} has reduced, while C_{gs} has increased for BSG_MSJLT compared to BSG_CSJLT. However, an improvement of 11.7 % and 2.21 % is still obtained in maximum g_m and f_T respectively, in BSG_MSJLT over BSG_CSJLT. Higher work function has also mitigated thermal heating of both devices. Moreover, BSG_MSJLT has produced lower global device temperature as compared to BSG_CSJLT. The effect of work function tuning has also been investigated for ON state. It is found that at higher work function, g_m, f_T, TFP, A_V and GDT have improved, while IGD improves at lower work function. In the ON state, BSG_MSJLT has shown pronounced im-

provement over BSG_CSJLT. The least intrinsic delay is found to be 0.42 psec for BSG_MSJLT and 0.445 psec for BSG_CSJLT at 5.0 eV, BSG_MSJLT thus has maintained faster speed than BSG_CSJLT in the ON state. Thus, the concluding remark suggests that BSG_MSJLT is a better candidate than BSG_CSJLT for low-power RF application.

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Author Contributions

P.T., N.Y., M.D.G., and R.K.C. conceived and developed the study design, drafted the original study protocol, approved the final version of the study protocol and reviewed the article for publication. P.T. drafted the article for publication.

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