Capacitance Characteristics Behavior of 0.5 Order FC Using CFOA Based FC Multiplier

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Abstract. *This paper presents a method for capacitance scaling of Fractional Capacitor (FC) which is implemented using Current Feedback Operational Amplifiers (CFOA) based Capacitance Multipliers (C Multipliers). The circuit facilitates the change in FC value without changing component values in R-C network used for FC modelling or fabricating a new FC. The performance of the proposed circuit is examined for non ideal effects of CFOA. Effective impedance of scaled FC is examined through MATLAB simulations. The functionality of the realized scalers is verified using SPICE simulations where the FC is modelled using domino RC ladder network. Simulation results for impedance magnitude and phase responses are presented for various scaling factors and are compared with theoretical counterparts. The circuit application of proposed FC scaler is demonstrated through implementation of fractional order lossy and lossless integrators; and may be extended to fractional order filters, oscillators, controllers etc.*

Keywords

Capacitance Scaling, Current Feedback Operational Amplifier (CFOA), Capacitance Multipliers, Fractional Capacitor.

1. Introduction

Monolithic integration of circuits and systems has witnessed a tremendous boost due to continuous downsizing of device dimensions. Low frequency applications such as sensing and subsequent processing of biomedical signals and integration of loop filter used in Phase Locked Loop (PLL) could not be benefited from this as these require large value capacitors. Researchers, therefore, look for alternate schemes for placing a small capacitor on-chip and use a multiplier circuit. Gyrator, Generalized Impedance Converter (GIC), and Negative Impedance Converter (NIC) are also used for tuning of Capacitance multiplier (C multiplier) circuit. Such C multiplier circuits have been deployed for appropriate tuning of filters [1], [2], [3],[4], [5], [6], [7], [8], [9], [10], [11], [12] and [13] oscillators [14], PLLs [15] and series resonators [16]. Commercially available active elements such as Operational Transconductance Amplifier (OTA) [17], [18] and [19] and Op-amp [1] and [15] and AD 844 (CFOA) [20], and [21], [22] and [23] based C multipliers are reported in the literature.

Besides this, researchers are also focusing on fractional domain signal processing and generation applications especially in biomedical instrumentation and control systems. Analogous to capacitor in integer order circuits, the fractional order circuits use FC. The impedance of FC with Capacitance value (C_α) and non-integer order $(\alpha, 0 < \alpha < 1)$ is given by $(s^\alpha C_\alpha)^{-1}$.

In the available literature, the FCs is modelled using various structures [24] such as passive Resistor-Capacitor (RC) elements arranged in the form of semi-infinite tree, domino ladder, nested ladder, and symmetric network. Researchers have also explored FC emulators based on Metal Oxide Semiconductor/Complementary Metal Oxide Semiconductor (MOS/CMOS) [25] and OTA [26]. Few physical realizations of FC are also reported in [27], however, being in primitive stage these are not commercially available. The desired value of FC for given order α may be obtained by computing component (R and C) values [24] or bias currents and capacitor values [25] and [26] or by physical implementation of specific FC [27].

Tab. 1: Comparison on scaling methods of FC.

Ref.	Active element	No. of active elements	No. of passive element	FC	Solution	Additional circuit required	Experimental verification
[28]	Op-Amp	2	4	Electrolytic chemical process	GIC	No	Yes
[29]	Op-Amp	2	4	Domino ladder network	GIC	No	Yes
[30]	OTA	4	1	RC ladder network	IIMC	Impedance inverter	Yes
[31]	ECCII	3–4	3	RC ladder network	Synthetic inductor	Impedance inverter	No
[32]	CCII/ ECCII/ VGA	1/ 2/ 1	6	RC ladder network	FDNR	Impedance inverter	No
[33]	VCA	1	3	RC network	FDNR	Impedance inverter	No
[34]	OTA	4	0	RC network	Gyrator	Impedance inverter	No
[35]	OTA	17	5	Active simlation of RC network	SFG	No	No
Proposed	CFOA	1–2	2	RC ladder network	FC scaler	No	Yes

ECCII: Electronically Controllable CCII
VGA: Variable Gain Amplifier
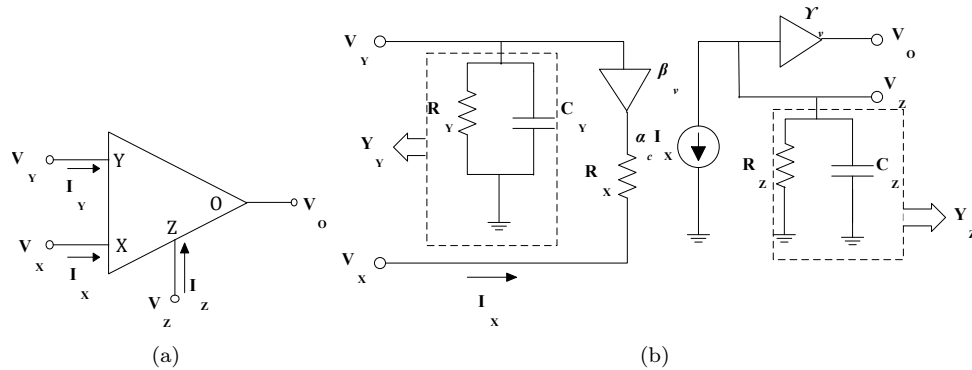VCA: Voltage Controlled Gain Amplifier
SFG: Signal Flow Graph

Fig. 1: (a) CFOA symbol and (b) its non-ideal model.

Any change in the FC value is a tedious task as it requires either recomputation of the component or bias current values or calls for a new physical realization. The capacitance scaling may be achieved using GIC [28] and [29] and Inverted Impedance Multiplier Circuit (IIMC) [30] topologies. These, however, use large number of passive elements and/or active blocks. Therefore, FC scaling through Capacitance multiplier (C multiplier) is examined in this work as an alternate solution and compared with other scaling methods having different forms of FC component Tab. 1.

This paper is organized as follows: Sec. 2. presents proposed CFOA based capacitance multiplier circuit having different form of scaling factors. It also includes investigation of impact of FC order and scaling factor of multiplier circuits on impedance values. The resulted impedances are also compared with unscaled normal capacitor. Section 3. illustrates non-ideal ef-

fect on Fractional Order (FO) capacitance scalers. The performances of realized scalers with applications are demonstrated by simulation and experimental results in Sec. 4. and Sec. 5. , respectively. Section 1. is the conclusion part.

2. CFOA Based C Multiplier Circuit

In this section, capacitance scaling of FC using CFOA based C multiplier circuits is presented. The symbol and equivalent non-ideal model of CFOA are shown in Fig. 1. Its terminal characteristics can be described by Eq. (1):

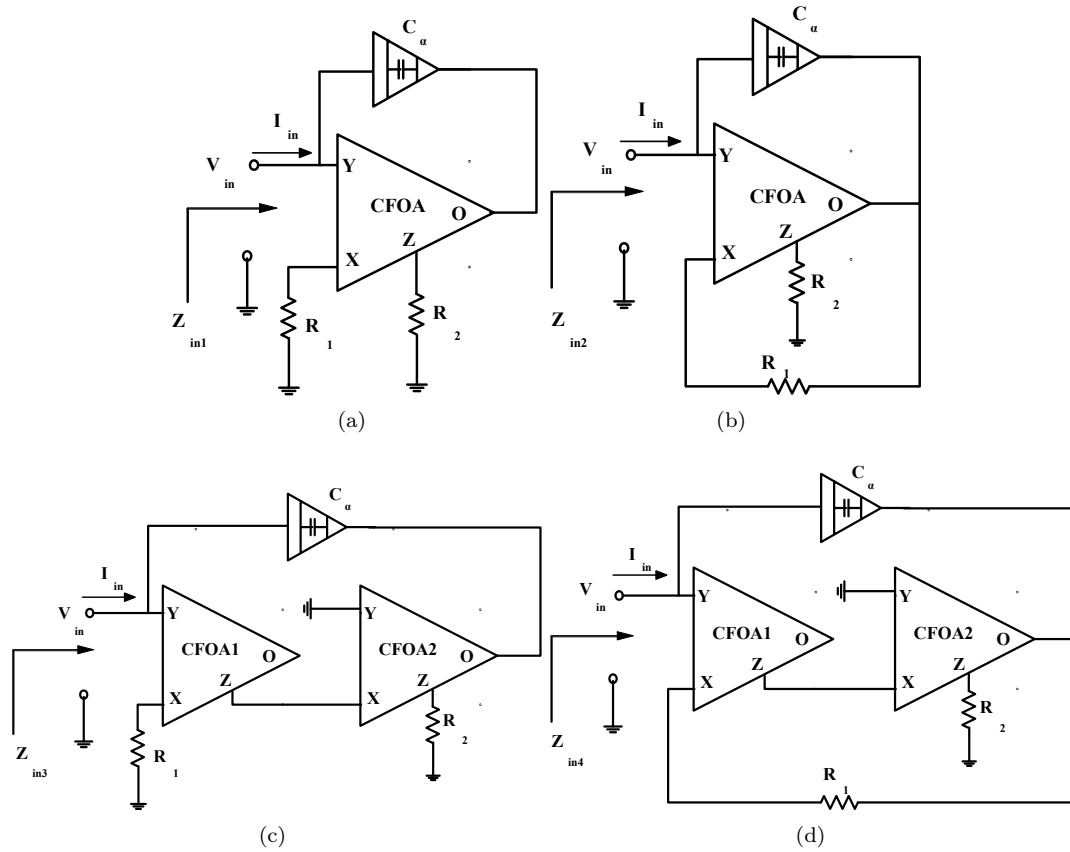$$I_Y = 0, \quad V_X = V_Y, \quad I_Z = I_X, \quad V_0 = V_Z, \quad (1)$$

Fig. 2: CFOA based FC scaling circuits.

where V_X, V_Y, V_Z, V_O and I_X, I_Y, I_Z, I_O correspond to voltages and currents at X, Y, Z, O-terminals, respectively. In practice, the terminal characteristics may deviate from Eq. (1) due to non-idealities which appear in form of tracking errors and parasitic elements. The modified terminal characteristics are given as:

$$
\begin{aligned}
I_Y &= \left(sC_Y + \frac{1}{R_Y}\right)V_Y = Y_Y V_Y, \\
I_Z &= \alpha_c I_X + \left(sC_Z + \frac{1}{R_Z}\right)V_Z = I_X + Y_Z V_Z, \quad (2) \\
V_X &= \beta_v V_Y + I_X R_X, \ V_0 = \gamma_v V_Z,
\end{aligned}
$$

where α_c, β_v, γ_v correspond to current and voltage transfer gains due to tracking errors. Parasitic elements appear in form of resistance R_X, parallel resistance capacitance combination $R_Y \ // \ C_Y$ and $R_Z \ // \ C_Z$ at terminals X, Y, and Z, respectively.

Figure 2 shows proposed CFOA based FC scaling circuits. The topologies in Fig. 2(a), Fig. 2(b), and Fig. 2(c) are realized by generalizing C multipliers reported in [23] while topology in Fig. 2(d) is obtained using topology reported in [36]. Routine analysis of the circuits in Fig. 2(a), Fig. 2(b), Fig. 2(c), and Fig. 2(d)

yields in the following impedance functions:

$$
Z_{in1}(s) = \frac{1}{s^\alpha \left(1 - \dfrac{R_2}{R_1}\right)C_\alpha}, \quad (3)
$$

$$
Z_{in2}(s) = \frac{\left(1 + \dfrac{R_2}{R_1}\right)}{s^\alpha C_\alpha}, \quad (4)
$$

$$
Z_{in3}(s) = \frac{1}{s^\alpha \left(1 + \dfrac{R_2}{R_1}\right)C_\alpha}, \quad (5)
$$

$$
Z_{in4}(s) = \frac{\left(1 - \dfrac{R_2}{R_1}\right)}{s^\alpha C_\alpha}, \quad (6)
$$

where order α of FC provides $-\alpha\pi \cdot 2^{-1}$ phase shift, therefore $\alpha = 0.5$ has $-45°$ phase shift.

Equations (3), Eq. (4), Eq. (5) and Eq. (6) show that FC is scaled by factors K_i ($i = 1, \ldots, 4$) where $K_1 = (1 - R_2 \cdot R_1^{-1})$, $K_2 = 1/(1 + R_2 \cdot R_1^{-1})$, $K_3 = (1 + R_2 \cdot R_1^{-1})$, and $K_4 = 1/(1 - R_2 \cdot R_1^{-1})$.

It may be observed that the impedance functions of realized scalers are majorly influenced by two factors

$$Z_{in1}(s) \mid_n = \frac{1}{Y_Y + s^\alpha C_\alpha \left[1 - \dfrac{\alpha_c \beta_v}{(R_1 + R_X)(G_2 + Y_Z)}\right]}, \tag{7}$$

$$Z_{in2}(s) \mid_n = \frac{1}{Y_Y + s^\alpha C_\alpha \left[1 - \dfrac{\alpha_c \beta_v \gamma_v}{(R_1 + R_X)(G_2 + Y_Z) + \alpha_c \gamma_v}\right]}, \tag{8}$$

$$Z_{in3}(s) \mid_n = \frac{1}{Y_{Y1} + s^\alpha C_\alpha \left[1 + \dfrac{\alpha_{c1}\alpha_{c2}\beta_{v1}}{(R_1 + R_{X1})(1 + R_{X2}Y_{Z1})(G_2 + Y_{Z2})}\right]}, \tag{9}$$

$$Z_{in4}(s) \mid_n = \frac{1}{Y_{Y1} + s^\alpha C_\alpha \left[1 + \dfrac{\alpha_{c1}\alpha_{c2}\beta_{v1}\gamma_{v2}}{(R_1 + R_{X1})(1 + R_{X2}Y_{Z1})(G_2 + Y_{Z2} - \alpha_{c1}\alpha_{c2}\gamma_{v2})}\right]}. \tag{10}$$

(i) α, and (ii) $R_2 \cdot R_1^{-1}$. To achieve higher scaling factor, larger resistor ratio $(R_2 \cdot R_1^{-1})$ is needed for topologies in Fig. 2(a) and Fig. 2(c) whereas similar results may be obtained by selecting $R_2 \cdot R_1^{-1}$ closer to unity for topology in Fig. 2(d). Further, all the topologies show an increasing trend in impedance for decreasing α ($\alpha < 1$) for fixed resistor ratio.

MATLAB simulations for change in impedance magnitude with respect to (w.r.t.) α and $(R_2 \cdot R_1^{-1})$ for circuits in Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d) are demonstrated in Fig. 3(a), Fig. 3(b), Fig. 3(c) and Fig. 3(d). It is useful to examine the effect of combined variation of α and $(R_2 \cdot R_1^{-1})$. The change in impedance magnitude value is calculated from its original impedance value and plotted against α and resistor ratio as shown in Fig. 3.

To examine the cumulative effect of variation of α and $R_2 \cdot R_1^{-1}$ on change in impedance magnitude, MATLAB simulations are carried out for circuits of Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d) and corresponding results are plotted in Fig. 3(a), Fig. 3(b), Fig. 3(c) and Fig. 3(d). Here % change of $|Z|$ is calculated from original value w.r.t. α and resistor ratio. The simulation results corroborate with the theoretical results. It may be noted that smaller α values have larger impact on impedance magnitude for a resistor ratio $R_2 \cdot R_1^{-1}$, i.e. close to unity for Fig. 2(a)/ much larger than unity for Fig. 2(b)/ negligible for Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d).

3. Non-Ideal Analysis of FC Scalers

To analyse the behaviour of proposed circuits in presence of CFOA non-idealities (Fig. 1(b)), the input

impedance functions of topologies of Fig. 2 are recomputed as Eq. (7), Eq. (8), Eq. (9) and Eq. (10), where subscript n corresponds to nonideal; and subscripts 1 and 2 with current transfer gain $(\alpha_{c_{1,2}})$, voltage transfer gains (β_v, γ_v); and parasitics, Y_Y, R_X, Y_Z correspond to CFOA1 and CFOA2.

It may be noted from the graphs in Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d) that Y-terminal of CFOA/CFOAs is either connected to input or to ground, therefore the performance remains unaltered due to parasitic associated with this terminal. The parasitic at X terminal of CFOA may be accommodated by adjusting the value of external resistor connected to it. The overall impact of CFOA parasitic elements on FC scaler behaviour may be ignored by considering the frequency of operation much below than parasitic pole associated with Z terminal. Therefore, $(K_i, i = 1, 2, 3, 4)$ for topologies of Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d) are recomputed as:

$$K_1 \mid_n = 1 - \alpha_c \beta v \frac{R_2}{R_1}, \tag{11}$$

$$K_2 \mid_n = \frac{1 + \left(\alpha_c \gamma_v - \alpha_c \beta_v \gamma_v \dfrac{R_2}{R_1}\right)}{1 + \alpha_c \gamma_v \dfrac{R_2}{R_1}}, \tag{12}$$

$$K_3 \mid_n = 1 + \alpha_{c1}\alpha_{c2}\beta v1 \frac{R_2}{R_1}, \tag{13}$$

$$K_4 \mid_n = \frac{1 - \left(\alpha_{c1}\alpha_{c2}\gamma_{v2} - \alpha_{c1}\alpha_{c2}\beta_{v1}\gamma_{v2} \dfrac{R_2}{R_1}\right)}{1 - \alpha_{c1}\alpha_{c2}\gamma_{v2} \dfrac{R_2}{R_1}}. \tag{14}$$

The parasitic effects of CFOA based FC multipliers (Fig. 2) are demonstrated using SPICE simulation results as shown in Fig. 5. The typical values of parasitic
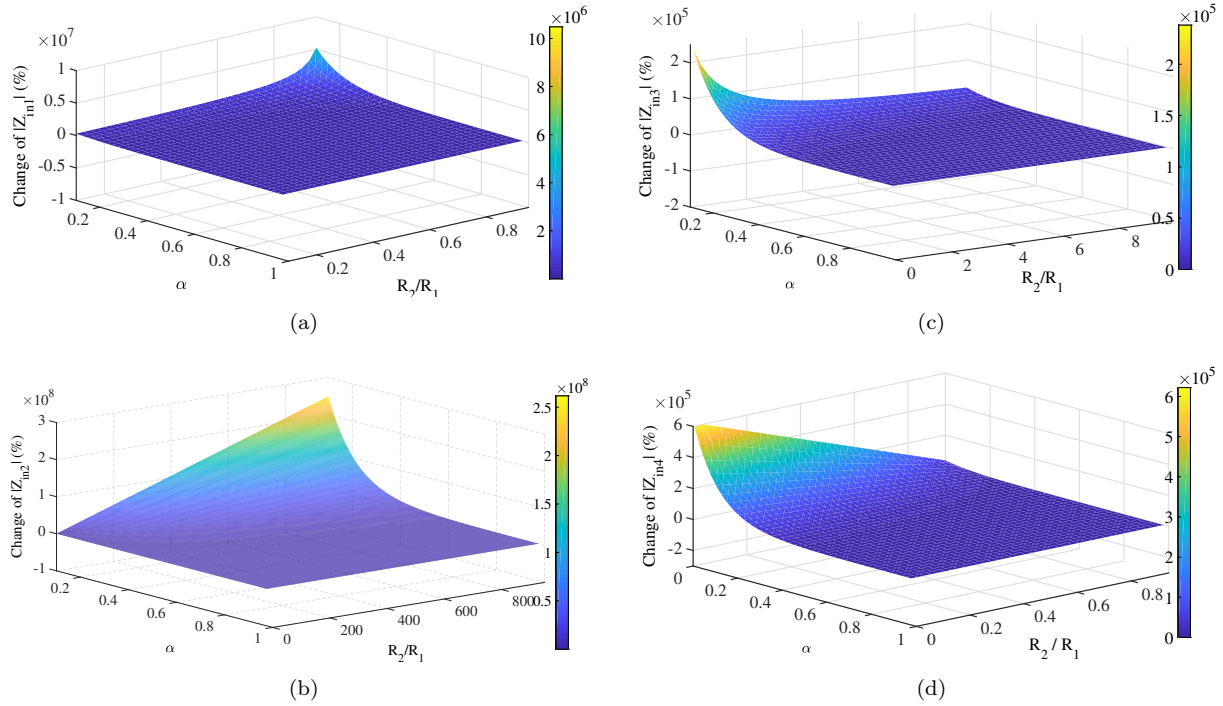
Fig. 3: Percent change in impedance magnitude with respect to α and $R_2 \cdot R_1^{-1}$.

impedances of CFOA are $R_x = 50$ Ω, $R_Y = 2$ MΩ, $C_Y = 2$ pF, $R_Z = 3$ MΩ, $C_Z = 4.5$ pF. It is clear that the parasitic element on X-terminal affects magnitude responses more with maximum errors of 3 dB, -1.18 dB and -4.14 dB for the circuits of Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d), respectively in the operational frequency range of α order FC while it produces -0.6 dB magnitude error with Y and Z-terminal parasitic elements of Fig. 2(b). The phase responses of FC multipliers as shown in Fig. 2(a) and Fig. 2(b) are more influenced by the parasitic of Z-terminal at lower frequency and Y-and X-terminals at higher frequency. Whereas the (Y-, X-) and (Y-, Z-) terminals parasitic elements have a few more effect on the phase responses of Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d), respectively.

4. Application and Simulation Results

The functionality of the realized scalers is verified using SPICE simulations using CFOA model [37]. The FC is implemented using infinite order domino RC ladder network truncated Fig. 4 to 12 blocks [38]. The component values of FC model having $\alpha = 0.5$ and $C_{\alpha=3.75}$ µF·s$^{-0.5}$ are $R_0 = 330$ kΩ, $R_1 = 82$ kΩ, $R_2 = 33$kΩ, $R_3 = 12$ kΩ, $R_4 = 4.7$ kΩ, $R_5 = 2$ kΩ, $R_6 = 736$ Ω, $R_7 = 270$ Ω, $R_8 = 120$ Ω, $R_9 = 47$ Ω, $R_{10} = 8.2$ Ω, $R_{11} = 18.2$ Ω, $C_0 = 4.7$ µF, $C_1 = 3.1$ µF,

$C_2 = 1$ µF, $C_3 = 470$ nF, $C_4 = 168$ nF, $C_5 = 68$ nF, $C_6 = 27$ nF, $C_7 = 10$ nF, $C_8 = 4.7$ nF, $C_9 = 1$ nF, $C_{10} = 2.2$ nF.
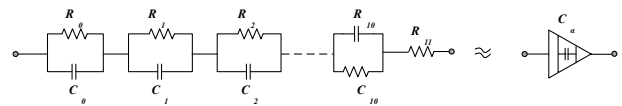

Fig. 4: Truncated RC domino ladder network realizing FC. [36]

Simulations are performed for different scaling factors for topologies in Fig. 2 for examining impedance magnitude and phase response and corresponding results are depicted in Fig. 6. The excitation voltage is set at 100 mV for the simulation results. The excitation voltage is set 100 mV for the simulation results. Table 2 enlists simulation setting for capacitance scaling factors and component settings used therein and performance of circuits. In the view of non-ideal effects of CFOA on the realized circuits, it may be observed that Fig. 2(b) and Fig. 2(c), have more linearity than Fig. 2(a) and Fig. 2(d). In Fig. 2(a) and Fig. 2(d), it increases the range of operation for lesser value of $R_2 \cdot R_1^{-1}$.

To illustrate the use of proposed scaler, CFOA based lossy/lossless integrator circuit is constructed as shown in Fig. 9. The notation $C_{\alpha eff}$ indicates the effective capacitance value of FC (that is $C_{\alpha eff} = K_i \cdot C_\alpha$). The transfer functions of lossy and lossless fractional
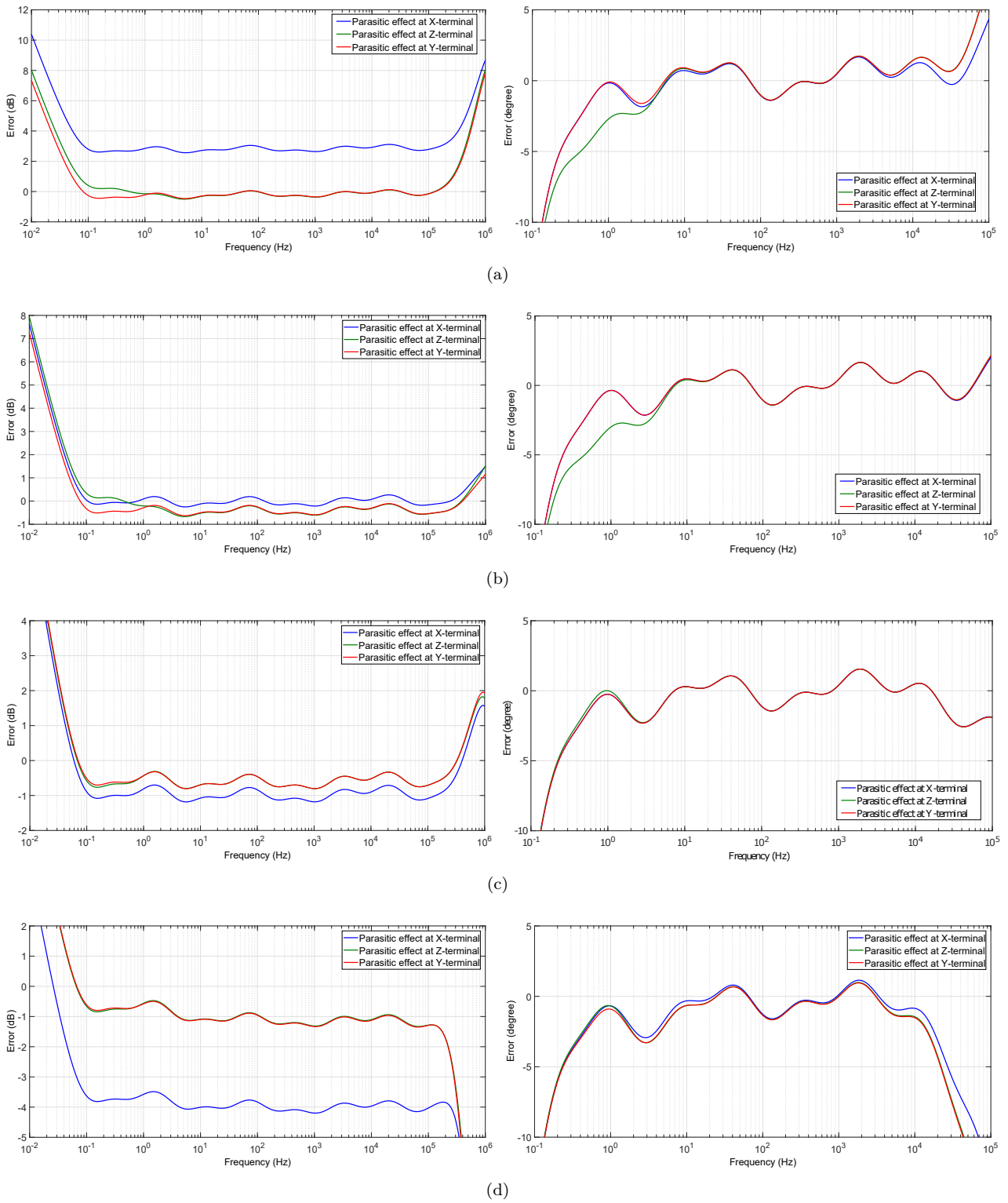
Fig. 5: The magnitude and phase errors for (a) Fig. 2(a), (b) Fig. 2(b), (c) Fig. 2(c) and (d) Fig. 2(d).
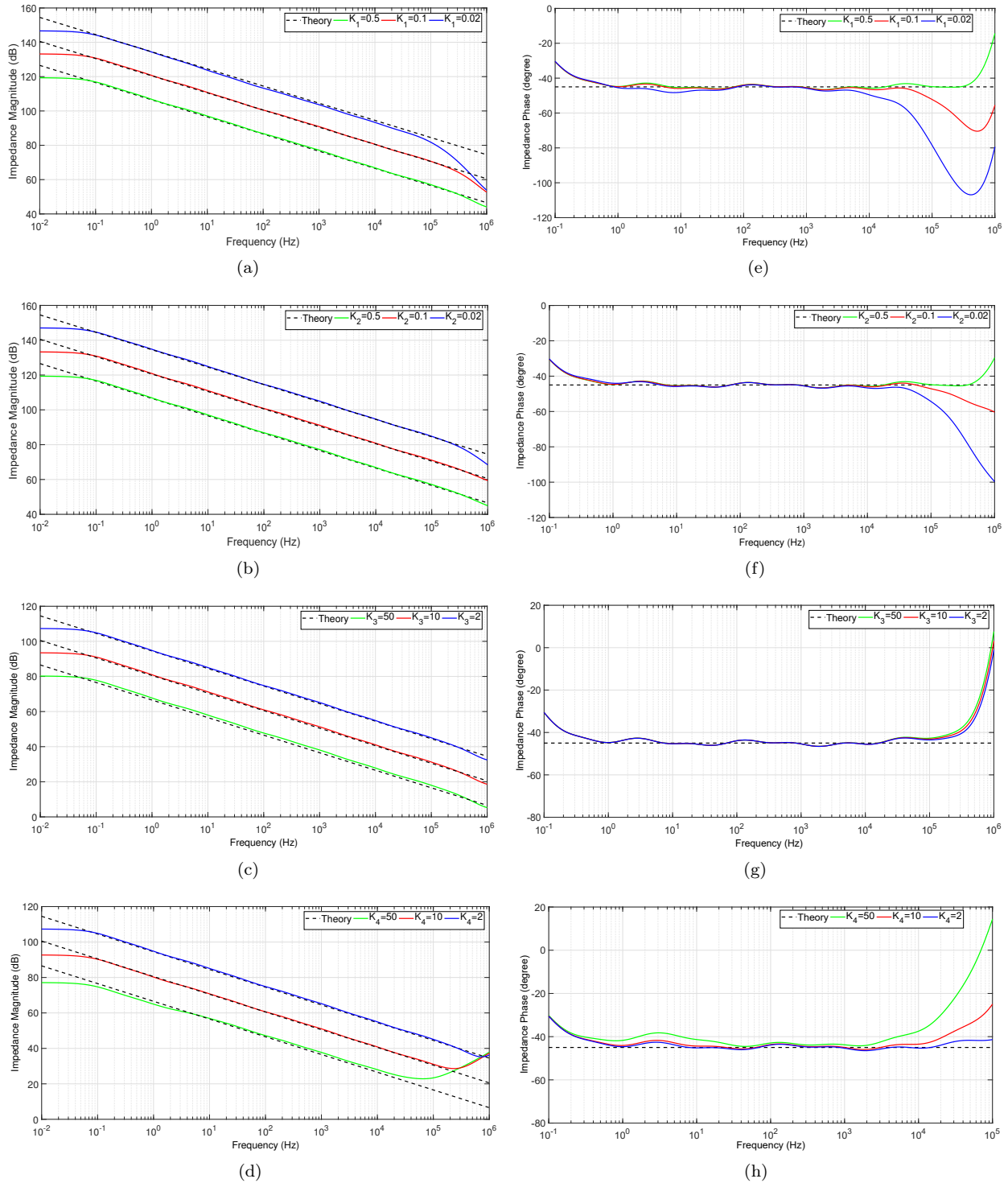
Fig. 6: Simulated impedance magnitude (a) – (d) and phase (e) – (h) responses for circuits of Fig. 2(a), Fig. 2(b), Fig. 2(c) and Fig. 2(d).
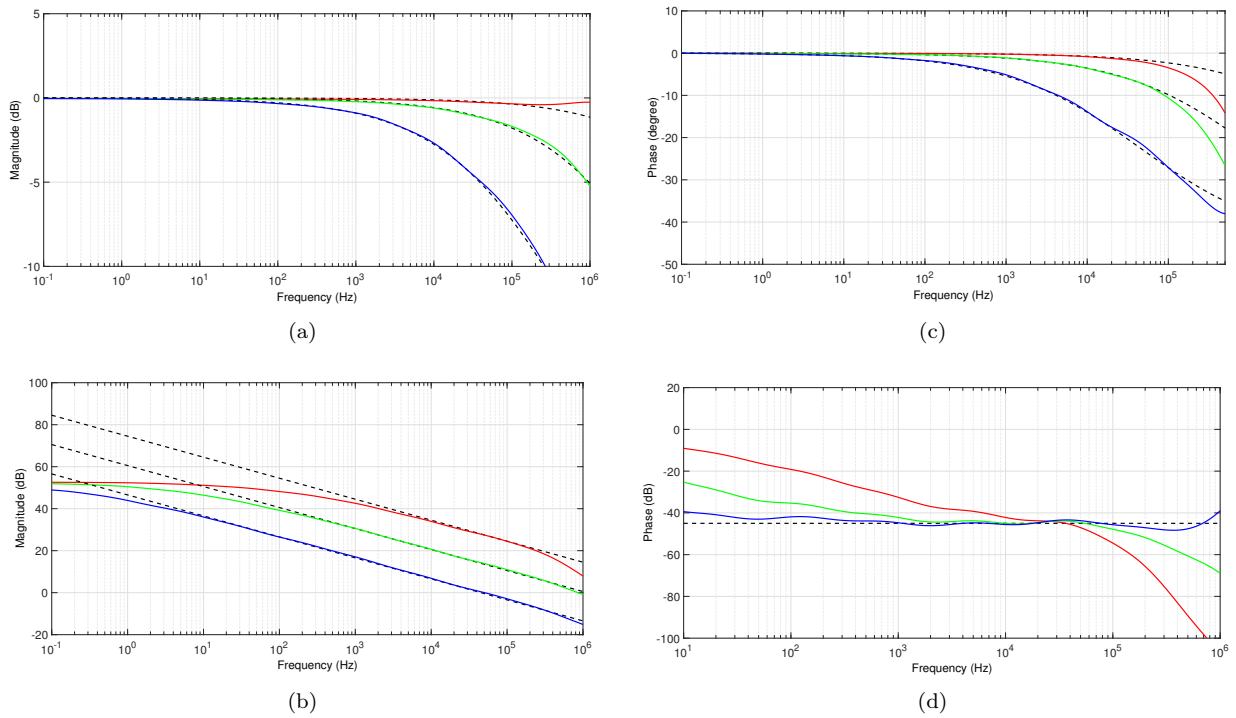
Fig. 7: Magnitude (a, b) and phase (c, d) responses of fractional lossy and lossless integrators for multiplication factor < 1.
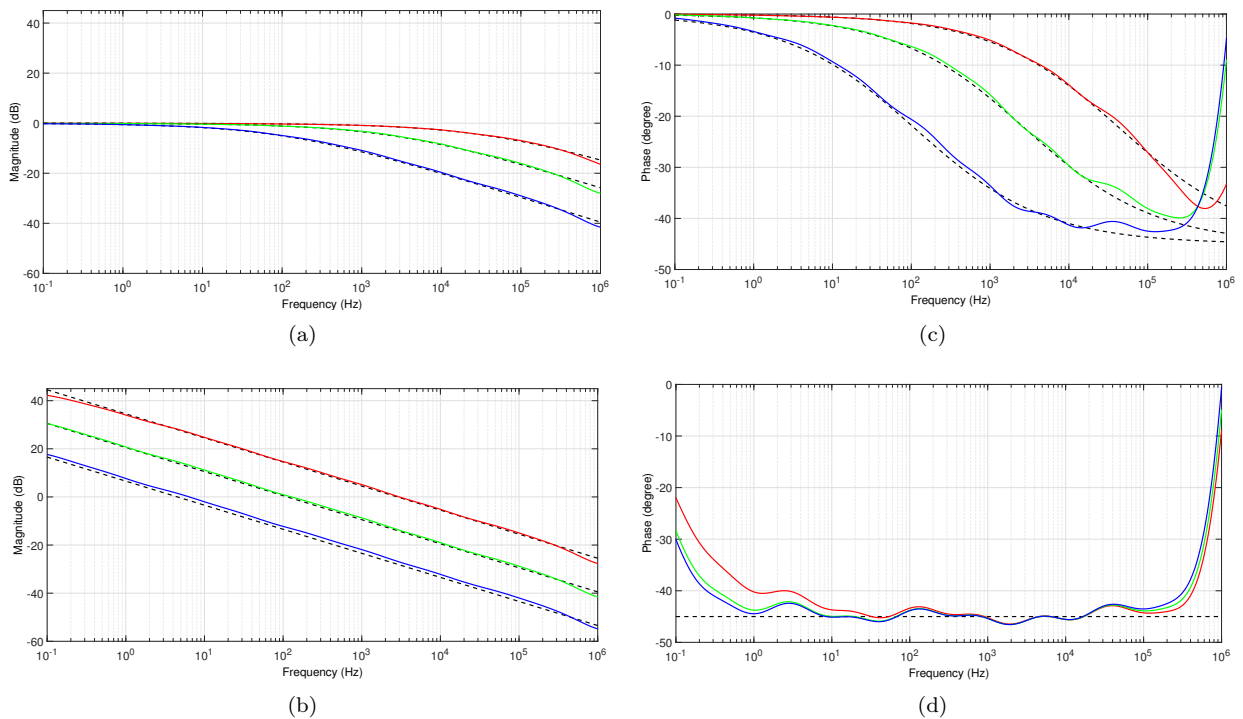

Fig. 8: Magnitude (a, b) and phase (c, d) responses of fractional lossy and lossless integrators for multiplication factor > 1.

Tab. 2: The components values and performance of FO capacitance scalers.

| Components setting and performance evaluation	Fig. 2(a)			Fig. 2(b)			Fig. 2(c)			Fig. 2(d)		
Multiplication factor	0.02	0.1	0.5	0.02	0.1	0.5	2	10	50	2	10	50
R_1 (kΩ)	1	1	1	1	1	1	1	1	1	1	1	1
R_2 (kΩ)	0.98	0.9	0.5	49	9	1	1	9	49	0.5	0.9	0.98
$(C_\alpha)_{eff} F(v/s^\alpha)$	75 n	0.375 μ	1.875 μ	75 n	0.375 μ	1.875 μ	7.5 μ	37.5 μ	187.5 μ	7.5 μ	37.5 μ	187.5 μ
Frequency range of magnitude response (Hz) (within 1.5 dB deviation)	0.05–50.1 k	0.04–330 k	0.042–588 k	0.046–392 k	0.042–1 Meg	0.042–935 k	0.04–625 k	0.04–676 k	0.04–741 k	0.042–970 k	0.052–218 k	1.4–14.8 k
Frequency range of phase response (Hz) (within 2.5° deviation)	13.3–6 k	0.44–53 k	0.43–426 k	0.57–44 k	0.45–107 k	0.42–525 k	0.4–202 k	0.4–154 k	0.4–120 k	0.44–28 k	4.6–14.5 k	19.5–3 k

(a)   (b)
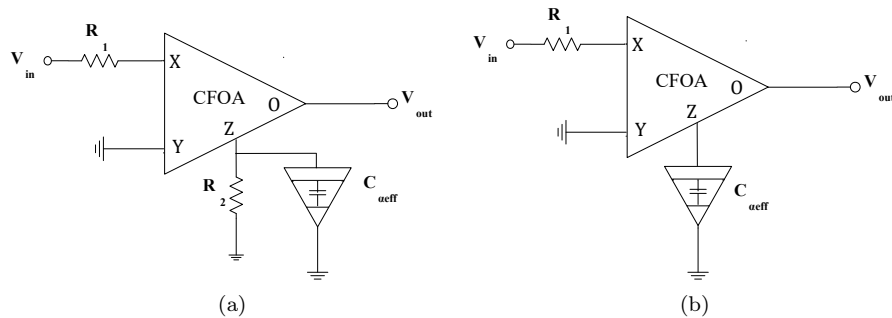
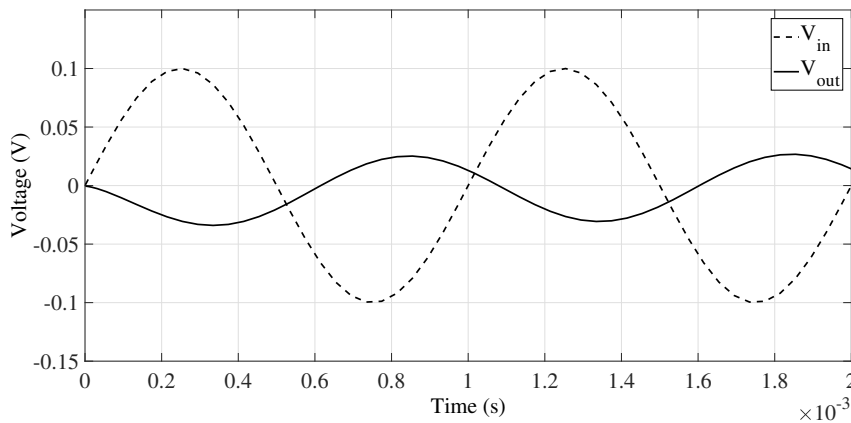**Fig. 9:** CFOA based fractional (a) lossy and (b) lossless integrators.

Fig. 10: Transient responses of fractional lossy integrator.

integrators can be expressed as follows:

$$T_{\text{lossy}}^\alpha = \frac{V_o(s)}{V_{in}(s)} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + s^\alpha R_2 C_{\alpha eff}}, \qquad (15)$$

$$T_{\text{lossless}}^\alpha = \frac{V_o(s)}{V_{in}(s)} = -\frac{1}{s^\alpha R_1 C_{\alpha eff}}. \qquad (16)$$

The simulated magnitude and phase responses of fractional order lossy/lossless integrators using 0.5 order FC scaler of Fig. 2(b) and Fig. 2(c) with scaling factors of (0.02, 0.1, 0.5) and (2, 10, 50) are depicted in Fig. 7 and Fig. 8, respectively. It may be observed that the simulated magnitude responses for lossy and lossless integrators follow theoretical values with deviations of (0.45 dB, 0.7 dB, 1.5 dB) and (0.6 dB, 0.8 dB, 1.5 dB) up to frequencies (478 kHz, 1.58 MHz, 2.7 MHz) / (380 kHz, 457 kHz, 1.7 MHz) and (1.5 kHz–346 kHz, 165 Hz–660 kHz, 2.8 Hz–891 kHz) / (410 kHz, 483 kHz, 1.7 MHz) for scaling factors (0.02, 0.1, 0.5) / (2, 10, 50), respectively. Further, phase deviations are well within 2.5° for frequencies up to (190 kHz, 200 kHz, 295 kHz) / (370 kHz, 280 kHz, 215 kHz) for lossy integrator and that for lossless integrator in the frequency range of (7.2 kHz–64 kHz, 1 kHz–94 kHz, 186 Hz–234 kHz) / (5.6 Hz–343 kHz, 3.3 Hz–278 kHz, 0.43 Hz–214 kHz). The transient response of fractional lossy integrator circuit is shown in Fig. 10 where input 100 mV amplitude and 1 kHz frequency sinusoidal signal is applied. The output is plotted for $K_3 = 10$, which verifies phase difference of $-5.5°$ closer to $-34°$ theoretical value.
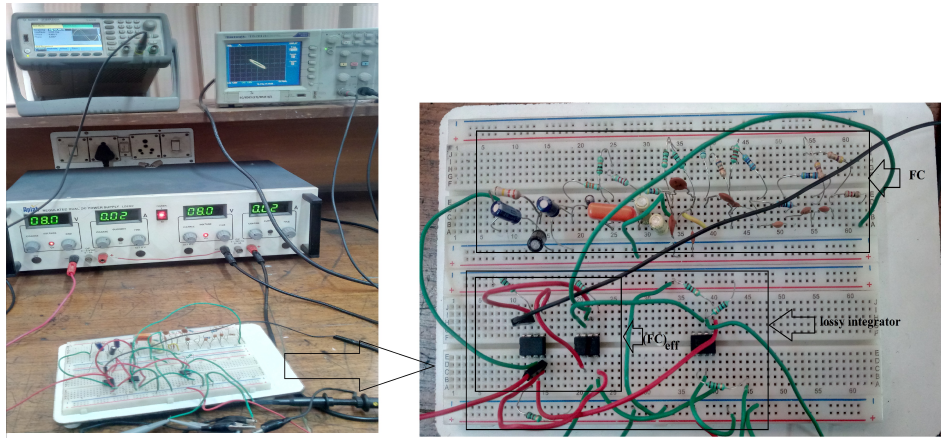
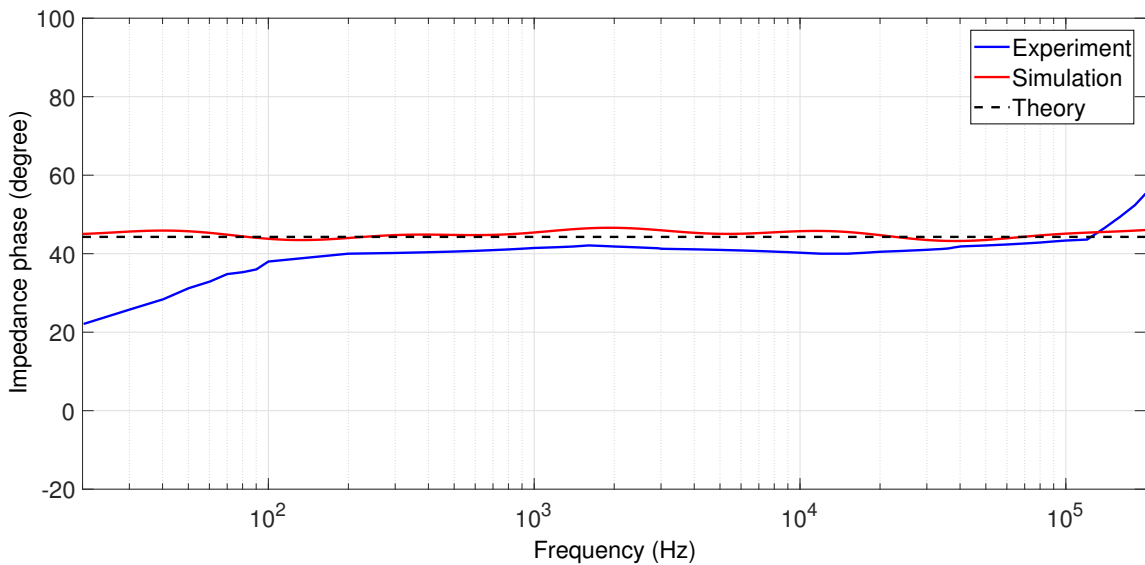**Fig. 11:** Experimental setup for FO lossy integrator circuit.

Fig. 12: Impedance phase response of 0.5 order FC.

5.   Experimental Verification

The realization of FC having α closed to 0.5 and $C_\alpha = 3.75$ µF/s^α using infinite RC ladder network is considered for experimental verification. The components values of ladder network (Fig. 4) are $R_0 = 330$ kΩ, $R_1 = 82$ kΩ, $R_2 = 33$ kΩ, $R_3 = 12$ kΩ, $R_4 = 4.7$ kΩ, $R_5 = 2$ kΩ, $R_6 = 736$ Ω, $R_7 = 270$ Ω, $R_8 = 120$ Ω, $R_9 = 47$ Ω, $R_{10} = 8.2$ Ω, $R_{11} = 18.2$ Ω, $C_0 = 4.7$ µF, $C_1 = 3.1$ µF, $C_2 = 1$ µF, $C_3 = 470$ nF, $C_4 = 168$ nF, $C_5 = 68$ nF, $C_6 = 27$ nF, $C_7 = 10$ nF, $C_8 = 4.7$ nF, $C_9 = 1$ nF, $C_{10} = 2.2$ nF. The impedance phase response of FC is plotted as shown in Fig. 12. The impedance phase value of FC (Fig. 4) is calculated with phase differences between FC and R_{11} using two voltage probes of oscilloscopes.

The experiment is performed using commercially available AD844AN (CFOA). The hardware setup for FO capacitance scalar, FC, and lossy integrator circuits

(Fig. 2(c), Fig. 5, and Fig. 6) is shown in Fig. 11. The approach to test the characteristics of Fig. 2(c) employing Fig. 9 is implemented for multiplication factor $K_3 = 3.2$ ($R_1 = 1$ kΩ and $R_2 = 2.2$ kΩ), order $\alpha = 0.5$ and capacitance $C_\alpha = 3.75$ µF/s^α of FC (the used component values as given in Sec. 4.).

The component values of lossy integrator ($R_1 = 0.22$ kΩ and $R_2 = 1$ kΩ) provides dc gain equals to 13.15 dB and its response is shown in Fig. 13. The performance is observed for sinusoidal input supply $V_{peak-peak} = 1$ V at 100 Hz, 1 kHz, and 10 kHz frequency points. Figure 13 also shows the responses of sinusoidal input and their Lissajous figures. The dc supply voltage in CFOA is fixed at ± 8 V. Moreover, Fig. 13 displays gain of 10 dB, 8 dB, 2.4 dB and phase of 1730, 1640, 1530 where calculated gain = 11.34 dB, 8.03 dB, 1.6 dB and phase = 1700, 159.10, 145.80 at corresponding 100 Hz, 1 kHz, 10 kHz frequency points. Thus, it can be stated that the experimental work verifies the theoretical study.
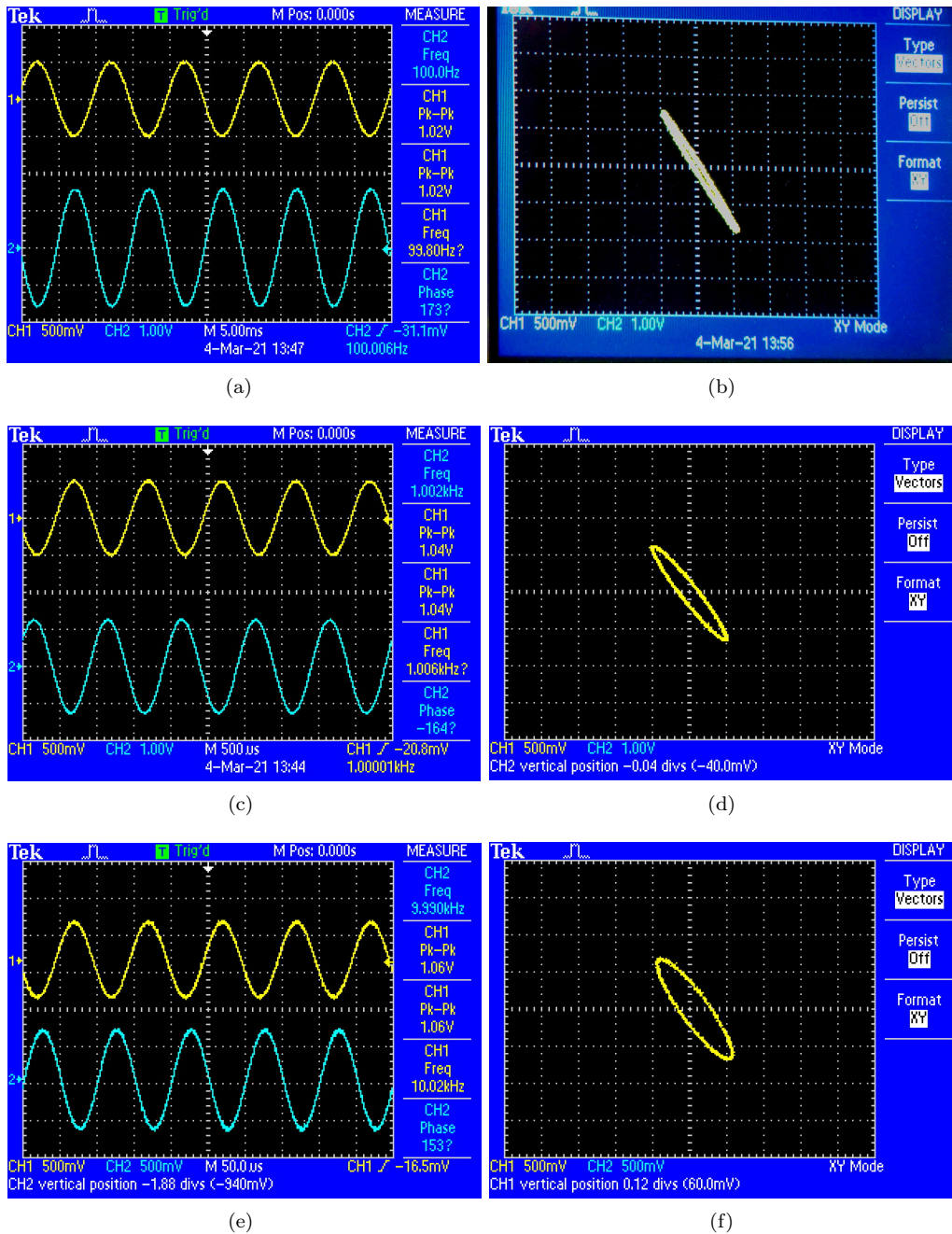
Fig. 13: Responses (channel 2) of Fig. 9 choosing dc gain = 13.15 dB for sinusoidal input (channel 1) at (a) 100 Hz, (c) 1 kHz, and (e) 10 kHz frequency points and (b, d and f) their Lissajous pattern.

6.   Conclusion

Four fractional capacitance scaler topologies obtained through generalization of CFOA based capacitance multipliers are presented in this paper. The effect of non idealities of CFOA on proposed scalers is investigated. Functionality of these scalers is tested through MATLAB and SPICE simulations for various scaling factors. The application of proposed scaler is illustrated through fractional order lossy and lossless integrators.

Author Contributions

R.V., N.P. and R.P. conceived of the presented idea. R.V. developed the theory and performed the computations. N.P. and R.P. verified the analytical methods. N.P. and R.P. encouraged R.V., to investigate practical application and supervised the findings of this work. All authors discussed the results and contributed to the final manuscript.

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