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Sub-10nm Transistors for Low Power Computing: Tunnel FETs and Negative Capacitance FETs

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SUB-10NM TRANSISTORS FOR LOW POWER COMPUTING: TUNNEL FETS AND NEGATIVE CAPACITANCE FETS

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Dedicated to my parents.

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SYMBOLS

I_D	Drain Current
V_{DD}	Supply Voltage
V_G	Gate voltage
C_{GS}	Gate-source Capacitance
C_{GD}	Gate-drain Capacitance
C_S	Substrate Capacitance
C_{OX}	Oxide Capacitance
k_B	Boltzmann Constant
T	Temperature
q	Charge
h	Planck's Constant
ϵ_o	Permittivity of free space
ϵ_{ox}	Oxide dielectric constant
ϵ	Electric field
E_o	Urbach parameter
A	Cross-sectional area
G^R	Retarded Green's function

ABBREVIATIONS

DG	Double-Gate
eDRAM	Embedded Dynamic Random Access Memory
Het-j TFET	Heterojunction Tunnel Field Effect Transistor
GC	Gain-cell
SRAM	Static Random Access Memory
SS	Subthreshold-Swing
TFET	Tunnel Field Effect Transistor
UTB	Ultra-Thin Body
NCFET	Negative-Capacitance Field Effect Transistor
FeFET	Ferroelectric Field Effect Transistor

ABSTRACT

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One of the major roadblocks in the continued scaling of standard CMOS technology is its alarmingly high leakage power consumption. Although circuit and system level methods can be employed to reduce power, the fundamental limit in the overall energy efficiency of a system is still rooted in the MOSFET operating principle: an injection of thermally distributed carriers, which does not allow subthreshold swing (SS) lower than 60mV/dec at room temperature. Recently, a new class of steep-slope devices like Tunnel FETs (TFETs) and Negative-Capacitance FETs (NCFETs) have garnered intense interest due to their ability to surpass the 60mV/dec limit on SS at room temperature. The focus of this research is on the simulation and design of TFETs and NCFETs for ultra-low power logic and memory applications.

Using full band quantum mechanical model within the Non-Equilibrium Greens Function (NEGF) formalism, source-underlapping has been proposed as an effective technique to lower the SS in GaSb-InAs TFETs. Band-tail states, associated with heavy source doping, are shown to significantly degrade the SS in TFETs from their ideal value. To solve this problem, undoped source GaSb-InAs TFET in an i-i-n configuration is proposed. A detailed circuit-to-system level evaluation is performed to investigate the circuit level metrics of the proposed devices. To demonstrate their potential in a memory application, a 4T gain cell (GC) is proposed, which utilizes the low-leakage and enhanced drain capacitance of TFETs to realize a robust and long retention time GC embedded-DRAMs. The device/circuit/system level evaluation of proposed TFETs demonstrates their potential for low power digital applications.

The second part of the thesis focuses on the design space exploration of hysteresis-free Negative Capacitance FETs (NCFETs). A cross-architecture analysis using HfZrOx ferroelectric (FE-HZO) integrated on bulk MOSFET, fully-depleted SOI-FETs, and sub-10nm FinFETs shows that FDSOI and FinFET configurations greatly benefit the NCFET performance due to their undoped body and improved gate-control which enables better capacitance matching with the ferroelectric. A low voltage NC-FinFET operating down to 0.25V is predicted using ultra-thin 3nm FE-HZO. Next, we propose one-transistor ferroelectric NOR type (Fe-NOR) non-volatile memory based on HfZrOx ferroelectric FETs (FeFETs). The enhanced drain-channel coupling in ultra-short channel FeFETs is utilized to dynamically modulate memory window of storage cells thereby resulting in simple erase-, program- and read-operations. The simulation analysis predicts sub-1V program/erase voltages in the proposed Fe-NOR memory array and therefore presents a significantly lower power alternative to conventional FeRAM and NOR flash memories.

1. INTRODUCTION

1.1 Overview of the Problem

Since the advent of integrated circuit (IC) technology, the electronics industry has seen a phenomenal and unabated growth. The secret to its success lies in the continued miniaturization of its computing elements, the transistors. For over past four decades, the incessant downscaling of the complementary metal-oxide-semiconductor (CMOS) transistors has fueled an era of electronics with unimaginable computing abilities. It has proven to be the most important achievement in the modern engineering history. The electronics industry has kept pace with the Moore's Law [1], roughly scaling down the gate-length of the transistor by *0.7*x every two years. Fig. 1.1 shows a graph of this historical trend for Intel Corporation processor chips [2].

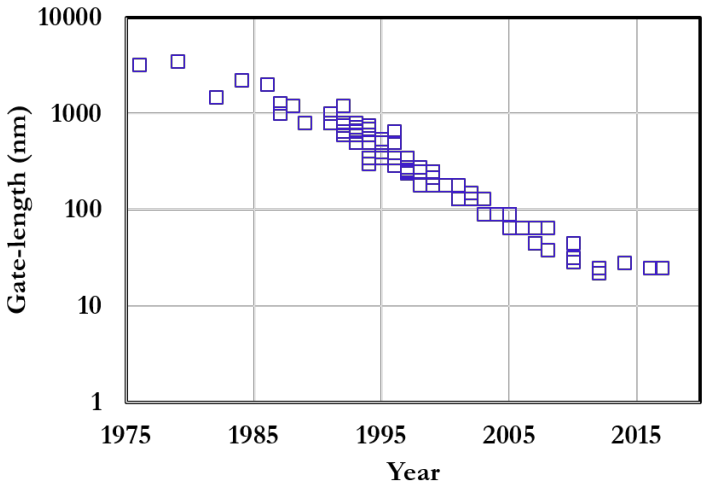

Fig. 1.1. The evolution of CMOS physical gate-length over past four decades.

Continuous down-scaling of transistors is paramount to maintaining this trend. From a manufacturing standpoint, this resulted in a lower cost per transistor in a

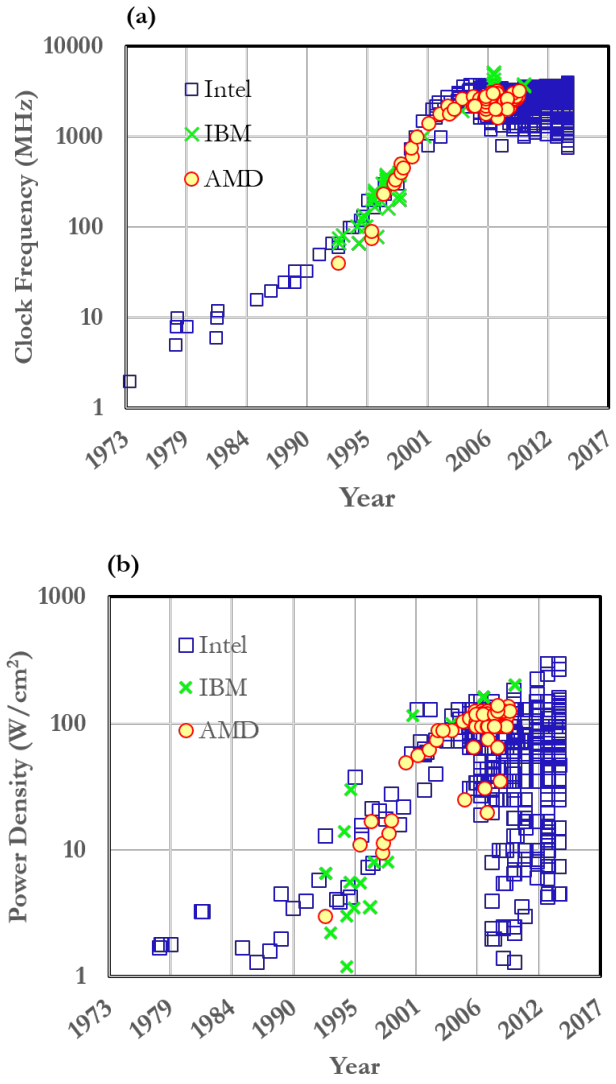

Fig. 1.2. The evolution of CMOS (a) Clock Frequency and (b) Power density over past four decades.

given chip area. However, since late 2000's, the gate-length hasn't reduced much and a flattening in the trend is seen at gate-lengths of around 25nm. In the conventional scaling era, the reduction in size of each transistor was accompanied by commensurate lowering of supply voltage and an increase in clock frequency and power density as shown in Fig.1.2(a) and Fig.1.2(b), respectively. However, in the late 2000's, con-

ventional scaling ended and the industry transitioned to a power constrained scaling era [3]. The power-consumption of a transistor is given by Eqn.1.1,

$$P = \alpha.f.C.V_{DD}^2 + V_{DD}.I_{Leak} \tag{1.1}$$

, where α is the activity factor, f is the switching frequency, V_{DD} is the supply voltage and I_{Leak} is the leakage current of the transistor. The quest for higher performance, i.e. an increase in operating frequency, resulted in power density shooting beyond 100W/cm^2, a magnitude similar to power density of a nuclear reactor [3]. Further increase in power density is unmanageable and greatly impacts the reliability and lifetime of transistors due to possibility of thermal damage. This, in turn, has led to saturation in clock frequency to around 3 GHz. Another reason for saturation in clock frequency is that the transistors themselves have not become significantly faster. The delay of a long-channel MOSFET is given by Eqn.1.2,

$$\tau = \frac{C.V_{DD}}{I_{ON}} \propto \frac{L^2.V_{DD}}{\mu(V_{DD} - V_{TH})^2} \tag{1.2}$$

, where L is the gate-length and μ is the mobility of carriers in the channel material. Modern high-performance devices leverage the high-mobility of III-V materials [4] or mobility-enhancements techniques such as strain-engineering [5, 6]. However, in a power-constrained era, any further reduction in gate-length or enhancement in clock-frequency has to be accompanied by a commensurate lowering of supply voltage, so that the power-density is kept in control. Lowering the supply-voltage, without compromising on the performance, requires a proportionate reduction in threshold voltage. But, this results in an exponential increase in the leakage current, which negatively impacts the second term in Eqn.1.1, i.e. the leakage power dissipation.

This claim is graphically justified in Fig. 1.3 where scaling the threshold voltage, without lowering the steepness from *off* to *on* state, results in an exponential increase in the OFF state leakage.

This factor, which measures the steepness from *off* to *on* state, is defined as subtheshold swing (SS) and quantifies the amount of voltage needed to change current

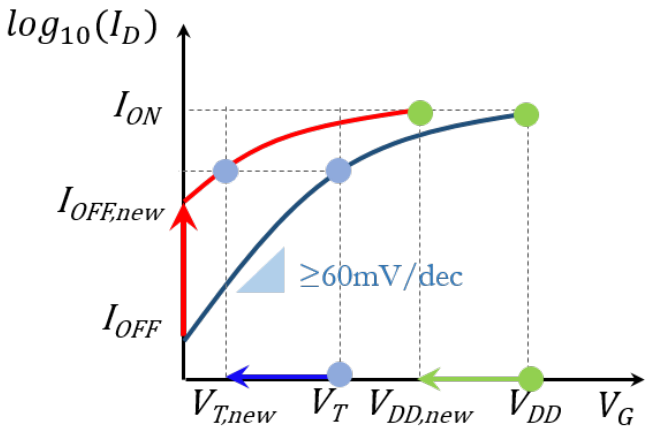

Fig. 1.3. I_{OFF} increases exponentially if V_T is reduced without reducing the sub-threshold swing.

by one order of magnitude. Mathematically, the fundamental lower limit of SS for a MOSFET can be formulated as follows:

$$SS = \left(\frac{\partial log I_D}{\partial V_G}\right)^{-1} = \frac{\partial V_G}{\partial \psi_s}\frac{\partial \psi_s}{\partial log I_D} = \left(1 + \frac{C_S}{C_{ox}}\right)\frac{kT}{q}ln10 \geq \left(\frac{kT}{q}ln10\right)\left(\quad (1.3)$$

where V_G is the gate-voltage, ψ_s is the surface-potential of the channel, C_S and C_{ox} are the semiconductor-channel and gate-oxide capacitance respectively. The first term on the right hand side of Eqn.1.3 signifies the coupling efficiency of the gate voltage to channel's surface potential, and is always greater than 1 for typical MOSFET operation. The second term denotes a factor associated with thermal (Boltzmann) distribution of carriers within the source of the MOSFET. At room temperature (300K), the minimum value of SS is therefore fundamentally limited to $ln(10)kT/q$ = 60 mV/dec.

1.2 Design Requirements for a New Transistor

It was highlighted in the previous section that the switching behavior of a MOSFET was limited to 60mV/dec due to carrier injection following Boltzmann statistics. As a result, a new switch with fundamentally different carrier injection mechanism

needs to be explored. This thesis explores two different post-CMOS devices as an alternative to overcome 60mV/dec barrier on subtheshold swing of MOSFETs, and thereby improve the energy efficiency of CMOS digital circuits: 1) Tunnel Field Effect Transistor (TFET), 2) Negative Capacitance Field Effect Transistor (NCFET).

The architecture of a TFET is exactly similar to a FinFET, however the source doped p-type, thereby making it an asymmetrical transistor. The major advantage of TFETs in comparison with the MOSFETs is that the reverse biased tunnel junction in the former eliminates the high-energy tails present in Fermi-Dirac distribution of electons in p+ source region and allows sub-60 mV/dec SS near the OFF state. It will be shown that by employing a GaSb-InAs TFET, the subthreshold swing can be reduced to $< 30mV/dec$, thus allowing supply voltage to be reduced to $\approx 0.25V$.

On the other hand, an NCFET consists of a ferroelectric deposited on the gate-stack of a conventional MOSFET. The operation of NCFET relies on the boosting of internal gate-voltage as a result negative capacitance offered by the ferroelectric. In other words, a negative capacitor in the gate-stack makes the net capacitance, looking into the gate, larger than the classical MOS capacitance. Thus, a lower voltage is required to induce a given amount of charge in the channel, than that required classically. This translates to a lower sub-threshold swing, thereby allowing the supply voltage to be reduced, while maintaining the same on- and off- currents of the transistor.

1.3 MOSFET vs. TFET vs NCFET

Fig. 1.4 shows the cross-sectional schematics of an n-MOSFET,n-TFET and n-NCFET respectively. The only structural difference in a TFET is asymmetrical doping of source and drain regions (p-i-n) as opposed to symmetrically doped source and drain regions (n-i-n) in a MOSFET. This seemingly trivial difference in the device structure, however, results in a completely different operating principle and accompanying physics in a TFET as described in the following section. The NCFET, on the

other hand, preserves the source-drain symmetricity of a MOSFET, however involves a layer of ferroelectric material deposited in gate stack of regular MOSFET as shown in Fig. 1.4(c).

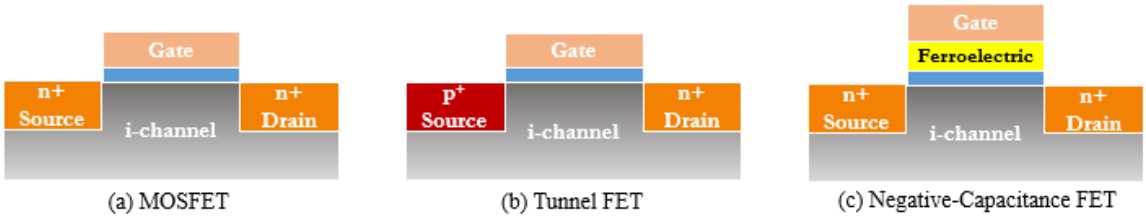

Fig. 1.4. Cross-sectional view of (a) n-MOSFET, (b) n-TFET (c) n-NCFET

1.3.1 Operating Principle of MOSFET

The operation of a MOSFET relies on modulation of the channel potential under the effect of gate-voltage which allows injection of carriers from the source into the channel region through a process called thermionic emission [7]. These carriers (electrons in the conduction band for n-MOSFET and holes in the valence band for p-MOSFET) are thermally distributed in the source region of the device according to Boltzmann distribution as shown in Fig.1.5. In the off-state, the potential barrier seen by the carriers from the source region is large, and the resulting off-state leakage current is small. As the gate-voltage is increased, the source-channel potential barrier reduces, resulting in an exponential increase in the injection of carriers from the source region into the channel. In the subthreshold region, the current is proportional to $e^{\frac{qV_{GS}}{mKT}}$, where $kT/q \approx 26mV$ at room temperature, and m is the body factor given by $\left(1+\frac{C_D}{C_{OX}}\right)$, where C_D and C_{OX} are depletion and oxide capacitances respectively. In the log scale, this appears as $m.60mV/dec$ as the subthreshold swing. In the superthreshold region, the channel is under strong inversion and the channel

capacitance greatly exceeds the oxide capacitance. This results in pinning of the surface potential and saturation of the drain-current.

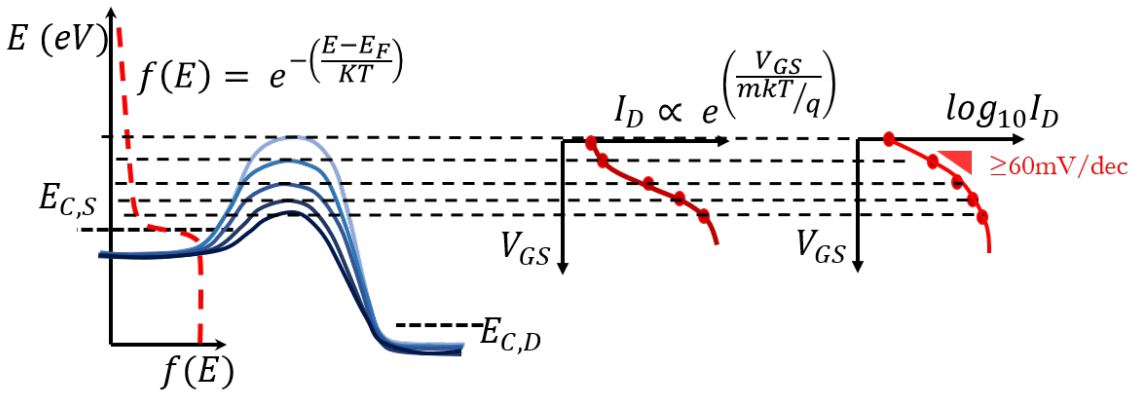

Fig. 1.5. (a) Conduction band-diagram along the channel of a n-channel MOSFET.The subthreshold swing is limited to 60mV/dec at room temperature.

1.3.2 Operating Principle of TFET

The operation of a TFET also relies on gate-voltage modulation of channel potential for the injection of carriers from source into the channel region. However, in contrast to an injection over the potential barrier (i.e. thermionic emission) in a MOSFET, the carriers are injected into the channel via a process called band-to-band tunneling (BTBT) as shown in Fig. 1.6.

The main advantage associated with BTBT is that the energy band gap of the p+ source cuts off the high-energy boltzmann tails of electrons (holes in the p-type source region). This lack of thermal dependence allows for subthreshold-swings lower than 60mV/dec even at room temperature. The resulting tunneling current can be expressed as [8]

$$I_{BTBT} = A\epsilon^2 exp\left[-\frac{B}{\epsilon}\right]\left(\tag{1.4}$$

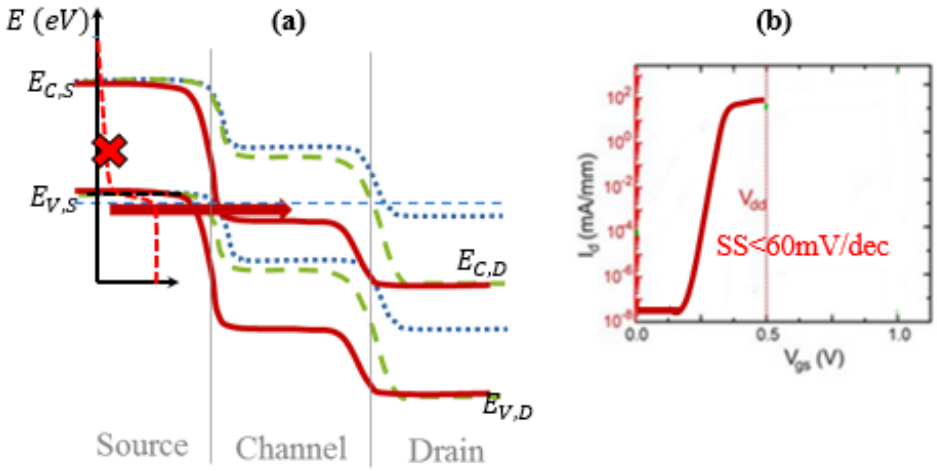

Fig. 1.6. (a) Energy band-diagram along the channel of a representative n-TFET. ON state is shown in solid red while the OFF states are shown in dashed blue and green. The Fermi-Dirac distribution is overlaid on the source Fermi level. In the ON state, the high-energy Fermi tail is cut-off by the bandgap resulting in extremely small leakage current. (b) TFETs can result in subthreshold-swing lower than MOSFET's thermal limit of 60mV/dec at room temperature.

where A and B are material dependent parameters, ϵ is the electric-field within the tunnel region. When a TFET is in the off-state, the p-i-n structure of TFET is reverse-biased and hence the diode leakage current comprises the dominant source of off-current, which is significantly smaller than the off-current of a MOSFET.

1.3.3 Operating Principle of NCFET

An NCFET consists of a ferroelectric material deposited on top of dielectric in the gate-stack of a MOSFET. A ferroelectric material is characterized by the presence of remnant polarization, $\pm P_R$, even in the absence of applied electric field. The polarization state can be switched via application of external electric field, greater than the critical value, E_C, also known as the coercive field of the ferroelectric. The ferroelectric behaves like a dielectric material in its stable states, however, exhibits negative capacitance, i.e. $dQ/dV < 0$, while traversing from one state to another.

A standalone ferroelectric is unstable in the negative capacitance region, however it can be stabilized when placed on top of dielectric, such that the overall capacitance of the system is always positive. In such a case, the voltage at the intermediate node is an amplified version of applied voltage.

The above property of internal voltage amplification is utilized in Negative-Capacitance FETs to lower the sub-threshold swing below the Boltzmann limit of 60mV/dec.

1.4 Organization of the Dissertation

This dissertation examines state-of-the-art steep slope transistors, particularly Tunnel FETs and Negative-Capacitance FETs at sub-10nm gate-lengths, for future low-power logic and memory applications. It is divided into six chapters which are as follows:

Chapter 1: Chapter 1 lays the background behind the search for a new transistor. It briefly describes the accompanying physics of two novel steep-slope devices: Tunnel FETs and Negative Capacitance FETs.

Chapter 2: This chapter describes the simulation framework used to simulate sub-10nm transistors in this research. We use an atomistic quantum device simulator based on tight-binding approach which solves Non-equilibrium Green's Function (NEGF) transport equation and Poisson's equation self-consistently to produce current-voltage and charge-voltage characteristics. These are then used to create look-up table based Verilog-A models to perform circuit simulations in HSPICE.

Chapter 3: This chapter describes the proposal of a sub-10nm doped-source underlapped GaSb-InAs TFET which exhibits lower subthreshold-swing compared to conventional p-i-n GaSb-InAs TFET.

Chapter 4: Chapter 4 investigates the detrimental impacts of band-tails, arising due to heavily doped source, on the subthreshold-swing of a TFET. To solve the problem, the intrinsic source TFET in an i-i-n configuration is proposed, which is immune to band-tail effects due to undoped source.

Chapter 5: In chapter 5, we discuss the applications of proposed TFETs in realizing an ultra-low power logic from a circuit-to-system level. A detailed circuit assessment of these devices is carried out at near-threshold voltages by synthesizing a LEON3 processor under varying interconnect scenarios. At near-threshold voltages and in the presence of moderate interconnect parasitics, TFET implementations were found to be preferable because of their ability to deliver similar performance as FinFETs while consuming nearly 50% lower power. Furthermore, to demonstrate their potential in a memory application, a 4T gain cell (GC) is proposed, which utilizes the low-leakage and enhanced drain capacitance of TFETs to realize a robust and long retention time GC embedded-DRAMs.

Chapter 6: In this chapter, we investigate the design space of hysteresis-free Negative Capacitance FETs (NCFETs) by performing a cross-architecture analysis using HfZrOx ferroelectric (FE-HZO) integrated on bulk MOSFET, fully-depleted SOI-FETs, and sub-10nm FinFETs. Our simulation analysis shows that FDSOI and FinFET configurations greatly benefit the NCFET performance due to their undoped body and improved gate-control which enables better capacitance matching with the ferroelectric. A low voltage NC-FinFET operating down to 0.25V is predicted using ultra-thin 3nm FE-HZO.

Chapter 7: In this final chapter, we propose one-transistor ferroelectric NOR type (Fe-NOR) non-volatile memory based on HfZrOx ferroelectric FETs (FeFETs). The enhanced drain-channel coupling in ultra-short channel FeFETs is utilized to dynamically modulate memory window of storage cells thereby resulting in simple

erase-, program- and read-operations. The simulation analysis predicts sub-1V program/erase voltages in the proposed Fe-NOR memory array and therefore presents a significantly lower power alternative to conventional FeRAM and NOR flash memories.

Finally, we summarize the work in *Chapter 8* and conclude the thesis by discussing ideas for future in *Chapter 9*.

2. SIMULATION OF SUB-10NM GATE LENGTH TRANSISTORS

2.1 Introduction

In the sub-10nm regime, the transistors operate near the ballistic limit, i.e the carriers traverse through the channel without undergoing scattering. In other words, the mean free path is larger than the dimension of the channel. In such a scenario, the device characteristics are essentially dictated by the quantum-mechanical effects, atomistic granularity of the nano-devices, two-dimensional electrostatics and the non-equilibrium carrier distribution. Traditional approaches based on continuum representation of underlying material become invalid. Hence, to accurately capture all atomistic quantum-mechanical effects, a rigorous physics-based device simulation is critical. This would also be helpful to quantitatively explain and even predict the experiments on nano-devices. In this chapter, we describe the simulation framework adopted to simulate sub-10nm Tunnel-FETs and Negative-Capacitance FETs. Particularly, we use a quantum mechanical device simulator, NEMO5 [9]. The device is described using atomistic tight-binding model and involves a self-consistent simulation of NEGF-transport and Poisson's electrostatics equation.

2.2 Overview of Tight-Binding NEGF Approach

The tight binding Non-Equilibrium Green's Function (NEGF) formalism is a quantum-mechanical method of computing charge density and transmission probability of carriers under arbitrary potential profile. Since the rigorous derivation of this NEGF formalism is available in literature [10–12], here we confine our discussion on key principles and applying them to examine carrier transport in nano-scale

transistors. In the NEGF solver, the device is represented by a nearest neighbor tight-binding Hamiltonian matrix, H, consisting of semi-empirical optimized parameters to reproduce the complete bulk band structure [13, 14]. For example in $sp3d5s^*$ tight-binding model, the basis function used to represent wave functions are constructed from outermost valence s, p (p_x, p_y, p_z), d ($d_{xy}, d_{yz}, d_{xz}, d_{x^2-y^2}, d_{z^2},$) and excited s ($s^*$) orbitals centered at cation and anion that constitute the primitive basis for the lattice.

2.3 Poisson's Equation

To compute the electrostatic potential, $\phi(x, y)$, the two-dimensional Poisson's equation is solved over a domain composed of source/drain extension, the channel region and the gate-oxide.

$$-\nabla^2\phi(x, y) = \frac{\rho(x, y)}{\epsilon_0\epsilon_r} \tag{2.1}$$

Here, ϵ_0 is the permittivity of air, ϵ_r is the dielectric constant of the region where (x, y) lies, and $\rho(x, y)$ is the net charge density at the point.

2.4 NEGF Transport Equations

The most important quantity to be computed in NEGF is the retarded Green's function, $G(E)$, also sometimes represented as $G^R(E)$. The simulation domain spans across source, channel and drain regions. The source and drain are assumed to be semi-infinite and at equilibrium, characterized by Fermi distributions, f_1 and f_2 respectively. The equations that are solved over the simulation domain are given below [15, 16]:

$$
\begin{aligned}
G(E) &= [EI - H - \Sigma_1 - \Sigma_2]^{-1} \\
\Gamma_{1,2}(E) &= i(\Sigma_{1,2} - \Sigma_{1,2}^{\dagger}) \\
\rho &= \frac{1}{2\pi} \iint (f_1 G\Gamma_1 G^{\dagger} + f_2 G\Gamma_2 G^{\dagger}) \\
T(E) &= Trace(\Gamma_1 G\Gamma_2 G^{\dagger}) \\
I &= \frac{-q}{h} \iint T(E)(f_1 - f_2)dE
\end{aligned}
\tag{2.2}
$$

The retarded Green's function, $G(E)$, is obtained from the Hamiltonian matrix, H, and the contact self-energy matrices $\Sigma_{1,2}$ expressed in the chosen atomic basis which constitutes the outermost atomic orbitals of the atoms, that form the device domain. It is worth noting that the matrix inversion is an expensive operation, specially if the size of Hamiltonian matrix is large (i.e. if the device itself is large). To relieve the computation burden, fast algorithms, such as Recursive Green's Function (RGF) [17, 18] are utilized to calculate only specific elements of G(E) that would be used in subsequent steps. The electrostatic potential, ϕ, calculated from the Poisson's equation as described in previous subsection, is added to the diagonal elements of the Hamiltonian. The diagonal entries are important because they represent the state density at each lattice point. Γ, which is defined in terms of the lead self-energies, physically denotes the electron exchange rates between the device active region and S/D reservoirs. Once the retarded Green's function is evaluated, charge density, ρ, transmission coefficient from source contact to drain contact, T, are computed using Γ and Fermi distribution functions, f. Finally, the net current is calculated by integrating transmission coefficient over energies as highlighted in Eqn.2.2.

2.5 Boundary Conditions

2.5.1 NEGF Equations

Open boundary conditions are assumed for the S/D contacts while a uniform potential profile in equilibrium is used to compute contact self-energy matrices $\Sigma_{1,2}$. The complete description of the self-energy calculation procedure can be found in [19].

2.5.2 Poisson's Equation

The Poisson's equation is solved on the entire domain, including the S/D regions, the channel and the gate-oxide. The applied gate potential is applied as Dirichlet boundary condition while Neumann type boundary condition is applied to source and drain contacts. The initial guess for charge density is computed through NEGF equations given by Eqn.2.2. Then, electrostatic potential and semi-classical charge density are evaluated using self-consistent iterations using Newton-Raphson method [20].

2.5.3 Computing Capacitance

When the convergence between Poisson's equation and NEGF is reached, NEMO5 dumps out current-voltage and charge-voltage characteristics for various applied biases. The gate, drain and source capacitances are thereby calculated from carrier densities using following equations:

$$\begin{aligned} C_G(V_{GS}, V_{DS}) &= \frac{Q(V_{GS}+\Delta V, V_{DS}) - Q(V_{GS}-\Delta V, V_{DS})}{2\Delta V} \\ C_D(V_{GS}, V_{DS}) &= \frac{Q(V_{GS}, V_{DS}+\Delta V) - Q(V_{GS}, V_{DS}-\Delta V)}{2\Delta V} \\ C_S(V_{GS}, V_{DS}) &= \frac{Q(V_{GS}+\Delta V, V_{DS}+\Delta V) - Q(V_{GS}-\Delta V, V_{DS}-\Delta V)}{2\Delta V} \end{aligned} \tag{2.3}$$

The capacitance between terminals can thereby be obtained by:

$$\begin{bmatrix} C_{GS} \\ C_{GD} \\ C_{DS} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} C_G \\ C_D \\ C_S \end{bmatrix} \tag{2.4}$$

Here, C_{GS}, C_{GD} and C_{DS} are gate-source capacitance, gate-drain capacitance and drain-source capacitance respectively. The resulting I-V and C-V characteristics are used to create look-up table based Verilog-A model to perform circuit simulations in HSPICE [21, 22].

3. SOURCE UNDERLAPPED GASB-INAS TFET

3.1 Introduction

The Tunneling Field Effect Transistor is of great interest for future logic applications due to its promise of enabling power-supply scaling to below 0.5V [23], [24]. The major advantage of TFETs in comparison with the metal-oxide semiconductor field-effect transistors (MOSFETs) is that the reverse biased tunnel junction in the former eliminates the high-energy tail present in the Fermi-Dirac distribution of the valence band electrons in the p+ source region and allows sub-60mV/dec SS near the OFF state. This allows TFETs to achieve, in principle, much higher $I_{ON} - I_{OFF}$ ratio over a specified gate voltage swing compared to MOSFETs, thus making them attractive for low-V_{DD} operation. With growing challenges in maintaining L_G scaling and device performance tradeoff, extending technology roadmap to sub-10 nm is becoming increasingly difficult with lateral devices. At such dimensions, vertical device architecture is advantageous for improving performance [25].

GaSb/InAs Het-j TFET is one of the leading TFET options because of the broken-gap band-alignment which results in high drive current [26]. In this chapter, we discuss our proposal of a GaSb/InAs DG n-TFET with an n+-doped underlap layer of InAs towards the source and compare it with conventional p-i-n GaSb/InAs DG n-TFET [26] at gate lengths of 9 nm (ITRS 2022 node) [27]. Using WKB approximation, we present a simple analytical formulation that supports the observed improvement in SS over a larger range of currents in the proposed device.

3.2 Device Structure and Simulation Approach

3.2.1 Device Structure

Vertically grown double-gate (DG) GaSb-InAs n-TFET with an intermediate n+-doped InAs layer between p+ GaSb-source and intrinsic InAs-channel is shown in Fig. 3.1(a). Similarly, a p-TFET that utilizes an intermediate p+-doped GaSb layer between n+-InAs source and intrinsic-GaSb channel is shown in Fig. 3.1(b).

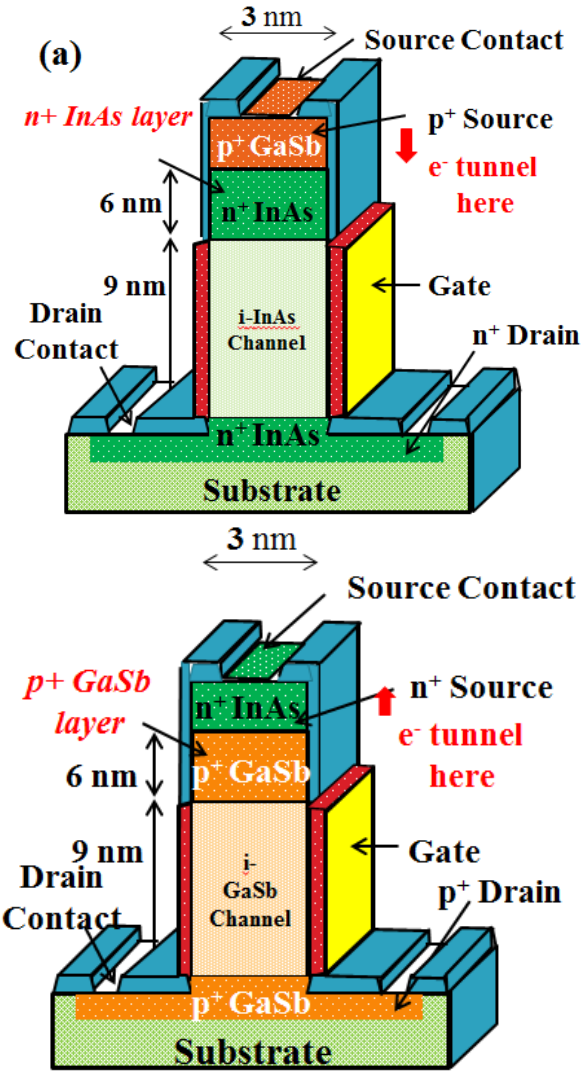

Fig. 3.1. Schematics of vertical (a) Underlapped n-TFET (b) Underlapped p-TFET. The configuration parameters are listed in Table 3.1.

The devices have a drawn gate-length of 9nm, and a source-side underlap of 6nm. Since, the devices are vertically grown, the underlap does not result in an increased footprint, as would be the case with underlapped quasi-planar FinFETs. The devices utilize 3 nm thick intrinsic body and 1.2 nm thick HfO_2 ($\epsilon_{ox} = 16$) gate dielectric. The other device parameters are listed in Table. 3.1. Abrupt doping profile has been assumed for simulations. The devices can be grown on GaSb using solid-source molecular-beam-epitaxy process [28] with in-situ source doping, thus realizing abrupt source-channel junctions, another important factor determining the performance of TFETs [29].

Table 3.1.
TFET Device Parameters

Quantity	**n-TFET**	**p-TFET**
$Gate - Length, L_G(nm)$	9	9
$S/DExtension, L_S, L_D(nm)$	30	30
$OxideThickness, T_{OX}(nm)$	1.2	1.2
$Fin - Thickness, T_{FIN}(nm)$	3	3
$N_A(cm^{-3})$	$4X10^{18}$	$1X10^{19}$
$N_D(cm^{-3})$	$1X10^{18}$	$4X10^{18}$
$N_{UNDERLAP}(cm^{-3})$	$1X10^{18}$	$1X10^{19}$
$DrainUnderlap, L_{DU}(nm)$	0	0
$SourceUnderlap, L_{SU}(nm)$	6	6
$\|V_{DD}\|$	0.5	0.5
$Gate - metalworkfunction, \Phi_g$	$4.7eV$	$5.0eV$

3.2.2 Device Simulation

The device simulations were performed using the quantum mechanical device simulator NEMO5 [9] as described in Chapter 2. We used $sp3s^*$ tight-binding model with spin-orbit coupling to solve two-dimensional NEGF transport equations coupled to Poisson electrostatics equation for simulating TFET I-V characteristics. Non-ideal effects like phonon and surface scattering, oxide-channel interfacial traps were ignored and ballistic operation was assumed. Gate-leakage current has been ignored in the simulations. The cross-sections used for simulations are shown in Fig. 3.2. For comparison against FinFETs, symmetrically-doped ($1\text{x}10^{20} cm^{-3}$) 9nm gate-length Si FinFETs, with 3nm fin-thickness, have been simulated using $sp3d5s^*$ tight-binding model without spin-orbit coupling. Note that the Si FinFETs are used only for comparison purposes to highlight the unique output- and CV-characteristics of TFETs in a circuit implementation and are not the goal of this work.

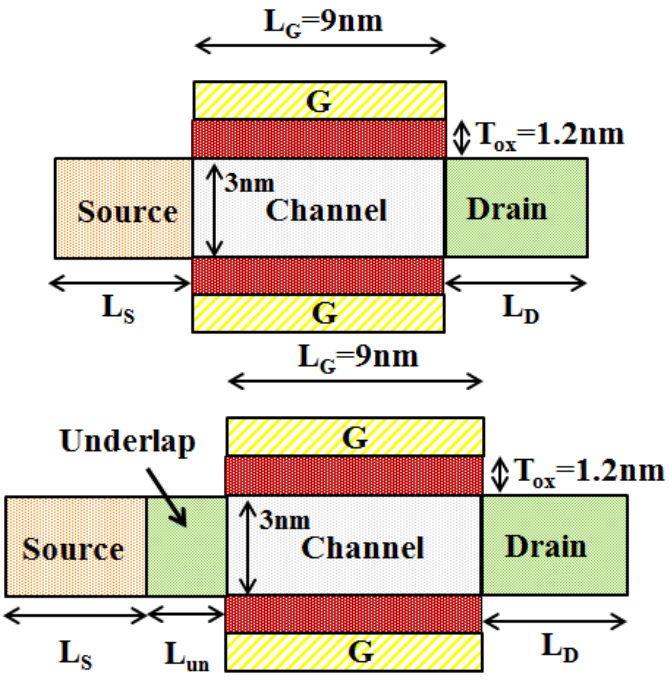

Fig. 3.2. Cross-sectional schematic of (a) Conventional TFET and Si-FinFET (b) Underlapped n-TFET used for 2D NEGF-Poisson simulations.

3.3 Current-Voltage Characteristics

3.3.1 Transfer Characteristics

A comparison of $I_D - V_{GS}$ characteristics of 6nm underlapped n/p TFETs and that of a non-underlapped, n/p TFET at V_{DS} of 0.5V is shown in Fig. 3.3.

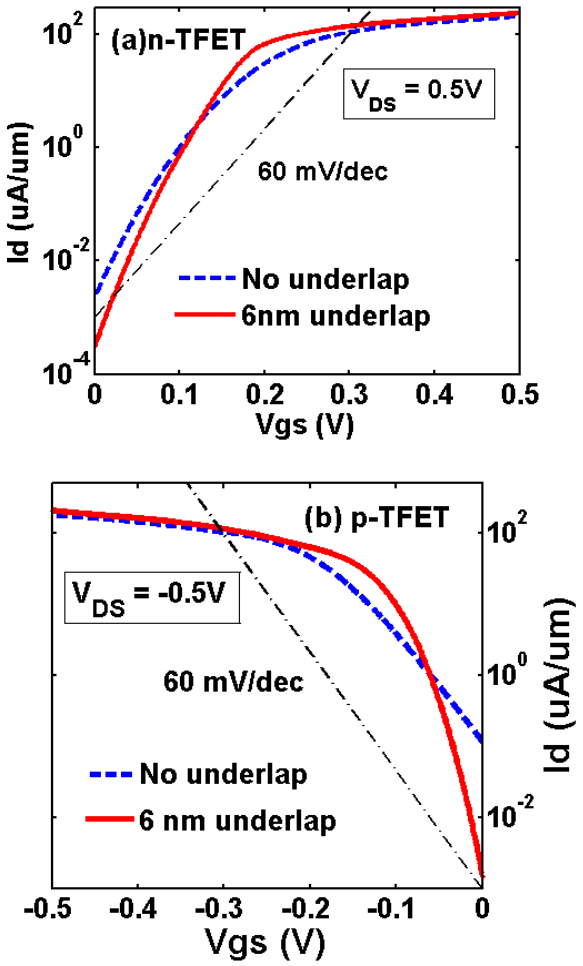

Fig. 3.3. I_D vs V_{GS} for non-underlapped and 6nm underlapped (a) n-TFET [30] (b) p-TFET [31]. Underlapped TFETs yield lower SS at low-voltages, thereby resulting in lower OFF currents while exhibiting same ON currents.

Underlapped n-TFET shows an I_{OFF} of $0.3nA/\mu m$ and I_{ON} of $235\mu A/\mu m$ (Fig. 3.3(a)), for gate-voltage swing of 0.5V. The effect of underlapping is much more pro-

nounced in p-TFET. As shown in Fig. 3.3(b), the off-current is lowered by around 50x in an underlapped p-TFET compared to non-underlapped p-TFET. The underlapped p-TFET shows off-current of $1.5nA/\mu m$ and on-current of $210\mu A/\mu m$. For the same gate voltage swing, a p-TFET without any underlap shows a much higher I_{OFF} of $100nA/\mu m$, thus making it unsuitable for low power applications. It is worthwhile mentioning that entire leakage current is due to direct source to drain tunneling. Other leakage components like trap-assisted tunneling (TAT) and Shockley Reed Hall recombination-generation (SRH) current have been ignored in these simulations due to unavailability of suitable models which can capture these phenomena within a full-band, wavefunction-based, ballistic transport treatment such as in NEMO5. However, the simulated TFET characteristics are expected to degrade if all such non-idealities could be taken into account. A comparison of the sub- threshold characteristics with respect to drive current, I_D, for both the devices is shown in Fig. 3.4. Underlapping in sub-10nm TFETs extends the sub-60 mV/dec SS to larger range of currents. Both n/p-type underlapped TFETs show sub-60 mV/dec SS for drain currents upto $10\mu A/\mu m$.

3.3.2 Output Characteristics - Comparison with FinFETs

The output characteristics of the TFETs and those of iso-gate length Si FinFETs, with gate-workfunction adjusted to obtain similar $V_T \approx 0.25V$ (defined here as V_{GS} at which $I_{DS} = 100\mu A/\mu m$) as TFETs, are shown in Fig. 3.5. The TFET has been upsized to 10 fins to plot both the curves on same scale, because the ON current in FinFETs is approximately 10x greater than TFETs. The excellent saturation of drain current emphasizes significantly lower DIBT (Drain Induced Barrier Thinning) in TFETs as compared to DIBL (Drain Induced Barrier Lowering) in the case of identically-sized FinFETs. This implies underlapped TFETs are more scalable than FinFETs beyond 9nm gate-length, however a different underlap length may be needed. Scaling the gate-length reduces gate-capacitance which improves delay

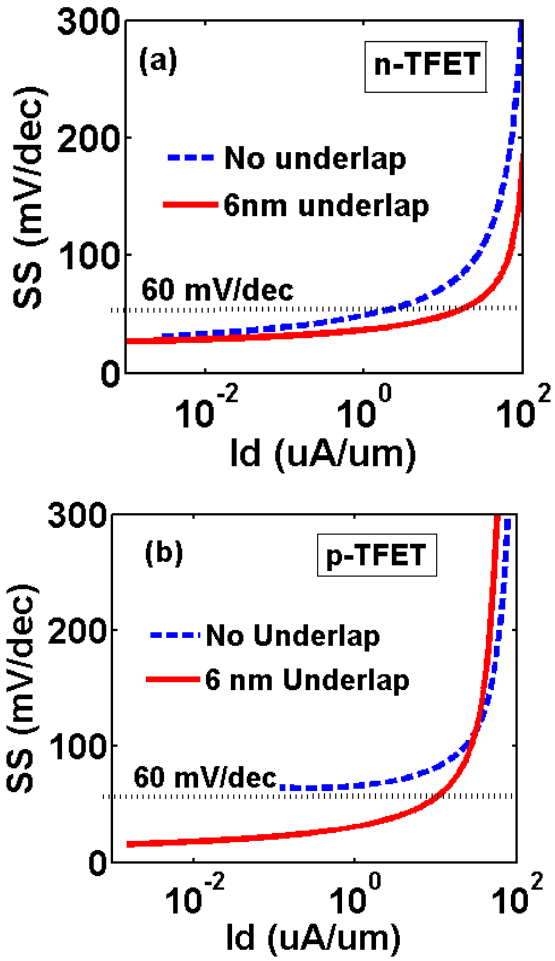

Fig. 3.4. SS vs I_D for non-underlapped and 6nm underlapped (a) n-TFET [30] (b) p-TFET [31].

of logic circuits. Near-ideal saturation of drain current also highlights much higher output-resistance which is paramount for small signal amplification. Another interesting observation is strong exponential dependence of drain-current with respect to V_{GS} at subthreshold voltages ($V_{GS} < 0.25V$) due to low SS while a near-linear dependence at super-threshold voltages in TFETs. This observation suggests that TFETs are more suitable for near-threshold logic applications.

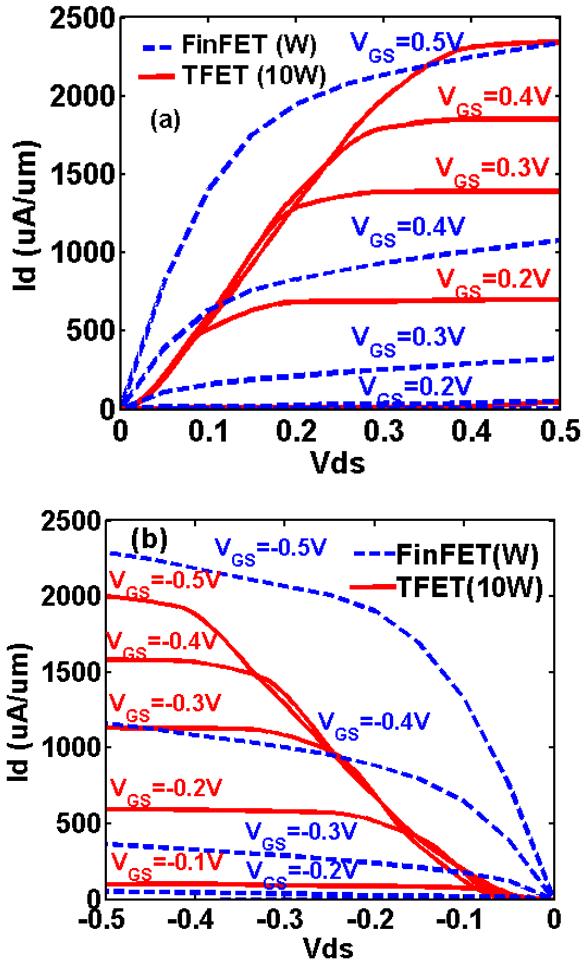

Fig. 3.5. Comparison of I_D versus V_{DS} characteristics for iso-gate length, L_G = 9 nm. (a) n-TFET and n-FinFET. (b) p-TFET and p-FinFET.

3.4 Analytical Explanation

The underlapped TFETs exhibit lower SS than non-underlapped TFETs. To understand this behavior, a plot of the band-diagrams and electron-density along the current-transport direction, near the center of the fin for non-underlapped and underlapped n-TFETs, at $V_{GS} = 0.1V$, is shown in Fig. 3.6 and Fig. 3.7 respectively. The effective channel tunnel barrier in n-TFET without any underlap (Fig. 3.6(a)) can be modelled as a right angled triangular barrier of width 9nm (gate length) as

shown in Fig. 3.6(b). The transport in an underlapped TFET is a two-step tunneling process: the standard broken-gap band-to-band tunneling followed by direct underlap-to-drain tunneling (like DSDT in a MOSFET) through the channel tunneling barrier. We achieve a low SS by engineering the second tunneling barrier. In a 6nm underlapped n-TFET, the presence of the n+ doped InAs underlap between source and channel modifies the tunneling barrier near the source and the resultant profile can be modelled as shown in Fig. 3.7(b), which is an isosceles triangular barrier. The presence of source-underlap creates a quantum wire-like environment for electrons in this region, due to confinement along current transport and fin-thickness direction. The low density of states resulting from quantization ensures that the underlapped region operates in quantum capacitance limit at the onset of tunneling thereby causing the subbands in this region to closely track the applied gate voltage due to fringe fields.

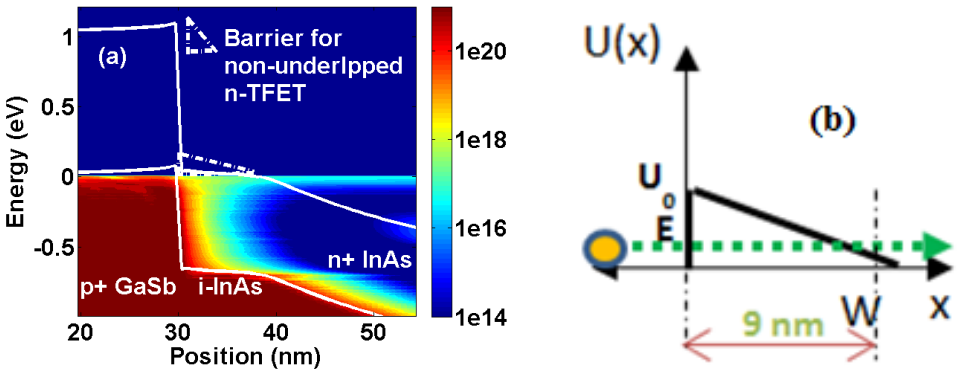

Fig. 3.6. Band diagram and energy resolved electron density for non-underlapped n-TFET at $V_{GS} = 0.1V$ [30]. (b) Right-angled triangle tunneling barrier model [30].

As V_{GS} increases, the bands continue to move down, causing the channel tunneling barriers effective width to reduce from both sides of the channel. This results in lower SS, as opposed to non-underlapped TFET where the tunneling barriers effective width changes only on the drain side. The WKB approximation [32] for the triangular

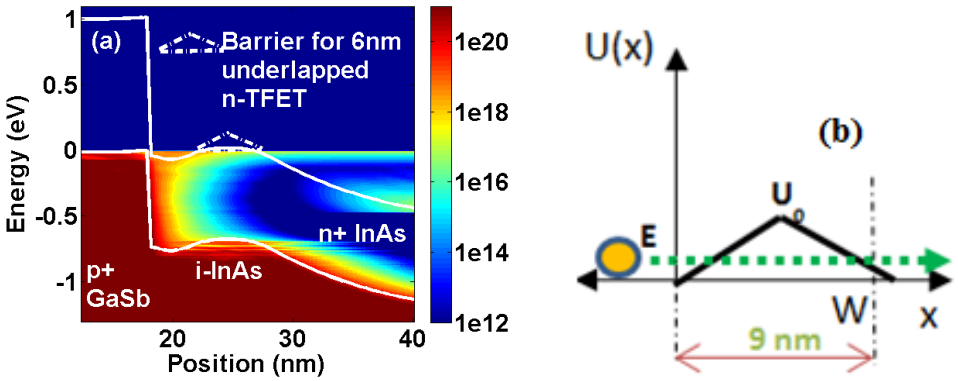

Fig. 3.7. Band diagram and energy resolved electron density for (a) 6nm-underlapped n-TFET at $V_{GS} = 0.1V$ [30]. (b) Isosceles triangle tunneling barrier model [30].

barrier shows that the transmission, $T(E)$, increases exponentially as the tunneling width decreases (Eqn. 3.1). The top of the barrier, U_O, is equally affected in both the devices for the same increase in gate voltage. The only differentiating factor between the two devices is the width of tunnel barrier, W, which is a function of gate voltage, V_{GS}. We collect all the common terms between the two devices in a constant term denoted by, α (Eqn. 3.2). The derivative of $log_{10}T(E)$ with respect to gate voltage determines the steepness of $I_D - V_{GS}$ curve, i.e. the SS.

$$T(E) \approx= e^{-2\int_{xo}^{W} \frac{\sqrt{2m}}{\hbar}\left[U_o\left(1-\frac{x}{W}\right)-E\right]^{\frac{1}{2}}dx} \tag{3.1}$$

$$T(E) \approx e^{-\left[\frac{4\sqrt{2m}}{3\hbar}\left(\frac{W}{U_o}\right)(U_o-E)^{\frac{3}{2}}\right]} \approx e^{-\alpha.W(V_{GS})} \tag{3.2}$$

$$\frac{\partial T(E)}{\partial V_{GS}} \approx -\alpha.e^{\alpha.W(V_{GS})}.\frac{\partial W(V_{GS})}{\partial V_{GS}} \approx -\alpha.T(E).\frac{\partial W(V_{GS})}{\partial V_{GS}} \tag{3.3}$$

$$SS^{-1} = \frac{\partial log_{10}(I_d)}{\partial V_{GS}} \propto \frac{\partial log_{10}(T(E))}{\partial V_{GS}} \approx -\alpha.\frac{\partial W(V_{GS})}{\partial V_{GS}} \tag{3.4}$$

Eqn. 3.4 shows that the SS is inversely proportional to rate of change of tunnel barrier width with respect to gate voltage. As the tunneling width changes on both

sides of the intrinsic-InAs channel barrier for underlapped device, we see a greater decrease in its tunneling barrier width compared to non-underlapped device for the same increase in gate voltage. Hence, the following relationship holds true:

$$\frac{\partial W(V_{GS})}{\partial V_{GS}}_{underlapped} > \frac{\partial W(V_{GS})}{\partial V_{GS}}_{non-underlapped} \tag{3.5}$$

As SS is inversely proportional to rate of decrease of tunneling barrier width with respect to applied voltage (Eqn.3.4), SS of the underlapped device is lower than that of conventional non-underlapped TFET. Similar discussion holds true for the observed

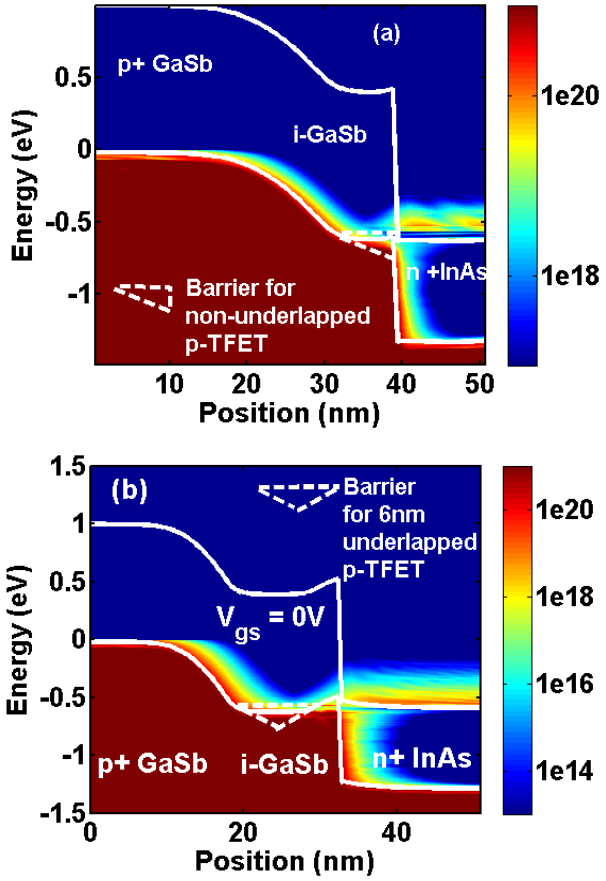

Fig. 3.8. Band diagram and energy resolved electron density for (a) Non-underlapped p-TFET [31]. (b) 6nm Underlapped p-TFET [31].

improvement in SS of underlapped p-TFET. Fig. 3.8(a) and Fig. 3.8(b) show the band-diagrams and respective barrier models which justify the claim.

3.5 Variation Analysis

With the scaling of the devices into sub-10nm scale, the effect of size/dopant variations on the device characteristics becomes increasingly important. Here, we present the impact of variations in length and doping of the underlapped region, fin-thickness and temperature on the device subthreshold characteristics.

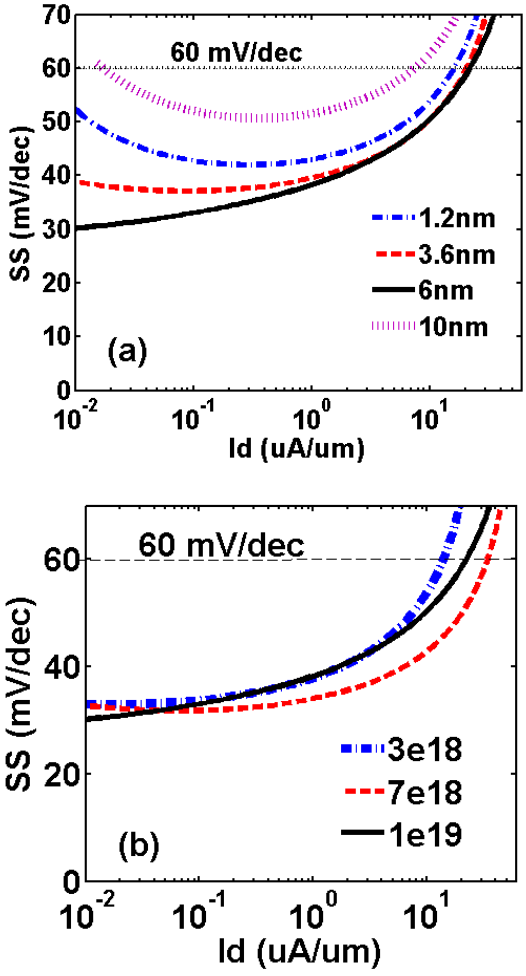

Fig. 3.9. SS vs. I_D for different lengths of underlap [30]. (b) SS vs. I_D for different doping values (in cm^{-3}) of underlap in n-TFET [30].

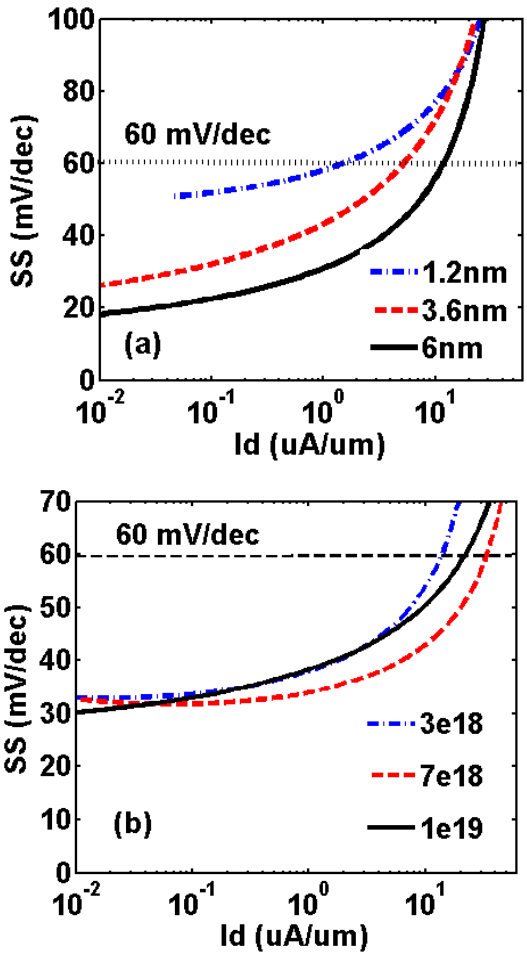

Fig. 3.10. SS vs. I_D for different lengths of underlap [31]. (b) SS vs. I_D for different doping values (in cm^{-3}) of underlap in p-TFET [31].

Fig 3.9(a) shows that SS becomes poorer with the reduction in the length of the underlap. A highly-scaled underlap might be insufficient to cause the potential energy dip near the source-channel interface which is central to achieving a low SS with source underlapped TFET, as explained in Section IV. Similarly, too long an underlap results in high density of states in the conduction band within the underlapped region, thereby resulting in poor SS and higher off-current due to conduction of carriers above the top of the channel barrier [30]. An optimal underlap length of 6 nm is seen to result in a symmetrical potential profile near both sides of the channel and desired subthreshold charateristics. SS is found to be fairly resistant to doping vari-

ations within the underlapped region as shown in Fig. 3.9(b). However, the doping should not be too high which would result in asymmetrical potential profile near the channel and hence degraded SS characteristics. Similar observations can be derived from variation plots of p-TFET as shown in Fig. 3.10.

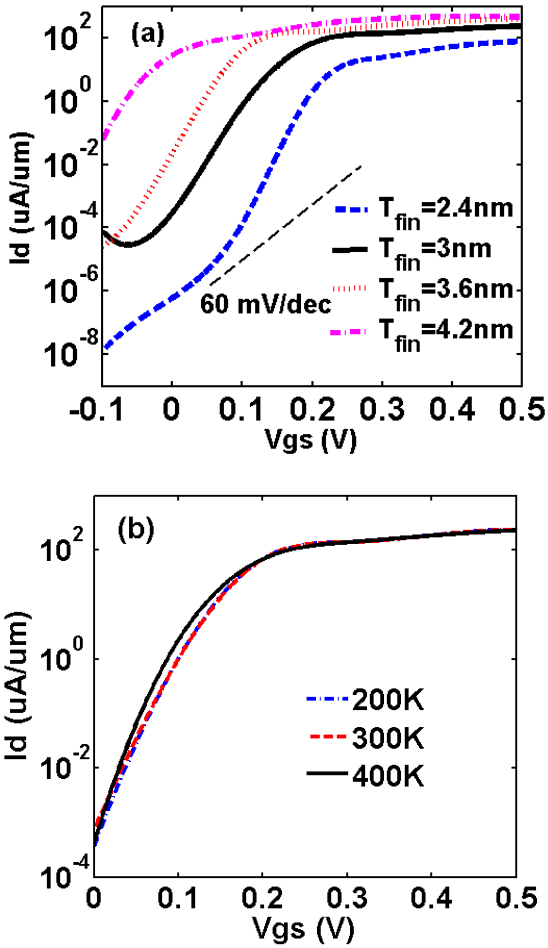

Fig. 3.11. I_D vs. V_{GS} of proposed n-TFET for varying (a) fin-thickness. (b) Temperature of operation.

The transfer characteristics for various fin-thicknesses are plotted in Fig. 3.11(a). As the channel thickness is reduced from 3nm to 2.4nm, a slight improvement in SS is observed as a result of better gate-control. However, due to reduction in number of

sub-bands, it can be seen that current drive capability reduces as the fin-thickness is reduced. Another interesting observation is the weak-dependence of SS with respect to fin-thickness. As the fin-thickness is increased to 4.2nm, sub-60 mV/dec SS is still maintained; however enhanced I_{OFF} is seen due to increased DSDT current. This behavior can be attributed to source-injection that remains independent of the electrostatics in the channel. The broken-gap tunnel junction remains in the ON-state while the gate-field only modulates the second tunnel barrier, i.e. the channel barrier thickness. III-V semiconductors, due to their low density of states, present lower channel capacitance compared to Si-FinFET counterparts (explained in Section VI). Hence, the channel potential closely tracks the gate-voltage even if the fin-thickness is relaxed. This observation supports experimental efforts to minimize gate oxide-channel and source-channel tunneling junction interface defects instead of geometry-scaling alone for successful sub-60mV/dec SS realization [33]. As with previous III-V TFETs, the sensitivity of Het-j TFET characteristics to gate-oxide thickness is found to be insignificant [26]. Fig. 3.11(b) corroborates the well-known weak-temperature dependence property of TFETs. As the tunneling current is independent of high-energy fermi-tails, the only temperature dependence comes from bandgap dependence on temperature. However, it should be noted that leakage current in experimental devices exhibit exponential dependence on temperature due to SRH-leakage (Shockley-Read-Hall) current [34], which is not accounted for in NEMO5.

3.6 Capacitance-Voltage Characteristics

Device capacitances play an important role in determining performance together with on-current. In this section, we present the C-V characteristics of source-underlapped TFETs and bring out essential differences against FinFETs. The methodology for extraction of C-V characteristics and generation of SPICE compatible look-up table models (used for circuit simulations in the next section) from the device simulations is summarized in Fig. 3.12.

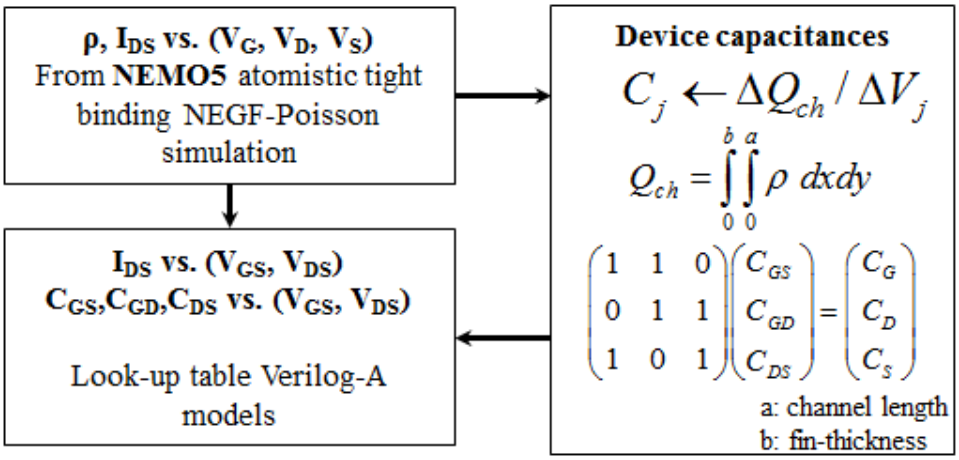

Fig. 3.12. Simulation flow for extraction of C-V characteristics used to develop look-up table based compact models for circuit simulations.

The capacitance versus voltage characteristics for source-underlapped GaSb-InAs n-TFET near the OFF and ON state is shown in Fig. 3.13(b). For comparison purposes, we also present 9nm gate-length n-FinFET C-V characteristics as shown in Fig. 3.13(a). In MOSFETs, both gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}) contribute equally toward inducing charge within the channel in the linear region whereas C_{GD} becomes negligible in saturation region due to higher potential barrier between the channel and drain. On the other hand, for TFETs, C_{GS} remains very small due to the presence of source-side tunnel barrier, whereas C_{GD} reflects the entire gate capacitance. This results in large Miller capacitance in source-underlapped TFETs, similar to conventional TFETs as has already been shown by Mookerjee et. al. [35]. This enhanced Miller capacitance effect in TFETs is known to result in large output voltage overshoot and undershoot peaks when input transitions from 0-1 and 1-0 V, respectively [35]. However, in a GaSb-InAs TFET, the low-density of states in InAs channel limits enhanced Miller capacitance and reliable circuit operation is achieved using GaSb-InAs TFETs as described in a circuit application in the next section. Also, the low- channel capacitance results in

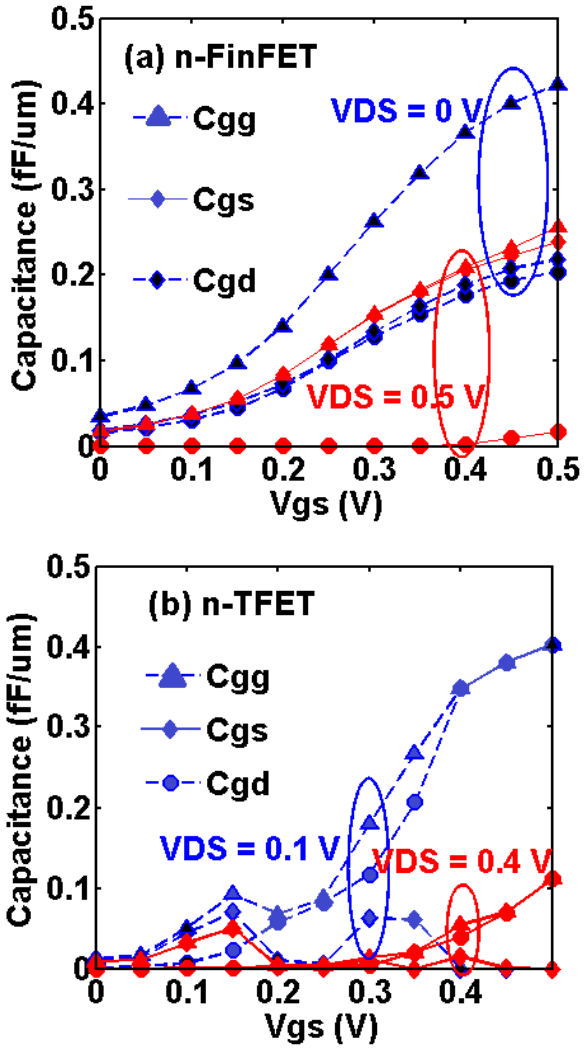

Fig. 3.13. C-V characteristics for (a) n-FinFET and (b)n-TFET.

reduced delay in III-V TFET based logic circuits in spite of their lower average drive currents, especially at near-threshold voltages of operation.

3.7 Conclusion

In this chapter, sub-10nm gate-length double-gate, vertically grown, n-type and p-type source underlapped heterojunction GaSb-InAs TFETs with superior subthreshold swings over conventional GaSb-InAs TFETs were investigated. A detailed pa-

rameter variation analysis shows that the device characteristics are fairly tolerant to minor fluctuations in underlap length and doping, while sub-60mv/dec SS can be maintained even when fin-thickness is relaxed upto 4.2nm. The source-underlapped TFETs exhibit enhanced Miller capacitance, similar to a non-underlapped TFET.

4. INTRINSIC SOURCE GASB-INAS TFET

4.1 Introduction

BAND-to-band tunneling field-effect transistors (TFETs) have emerged as leading contenders to outperform conventional CMOS by enabling supply voltage scaling due to its sub-60 mV/decade subthreshold swing (SS) [23,24,36,37]. TFETs based on both direct-gap (III-V) and indirect-gap (Si) semiconductors are being investigated theoretically and experimentally. Group IV materials such as Si [38], [32] and Ge [39], [40] exhibit smaller ON-currents due to low tunneling probability mainly resulting from their indirect bandgaps and wider tunnel barrier widths. Group III-V materials like InGaAs [41], InAs [42] and InSb [43] have higher ON-currents due to their narrower and direct bandgaps. The use of staggered-gap $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ [44] and broken-gap GaSb/InAs [21, 26, 30, 31] heterojunctions boosts the ON-current by reducing the tunneling distances.

Experimental investigation of Si TFETs [17-19] has been consistent with theoretical predictions [38], [32] i.e. they generally exhibit lower-ON currents. However, there exists a large gap between the theoretical and the experimental projections of III-V TFETs as shown in Fig.4.1. So far, a fabricated III-V TFET matching theoretical predictions of sub-60mV/dec SS over several orders of current [30], [26] has not been demonstrated. The successful demonstrations of subthermal SS have been performed by Dewey et. al. [45] using $In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ and Tomioka et. al [46] using the Si/InAs heterojunction in a nanowire geometry. Generally the ON-currents are in reasonable agreement with the theory; however a great disparity exists in experimental vs. simulated subthreshold characteristics. Some of the reasons for this include the non-idealities, like band-tail states associated with heavy source doping,

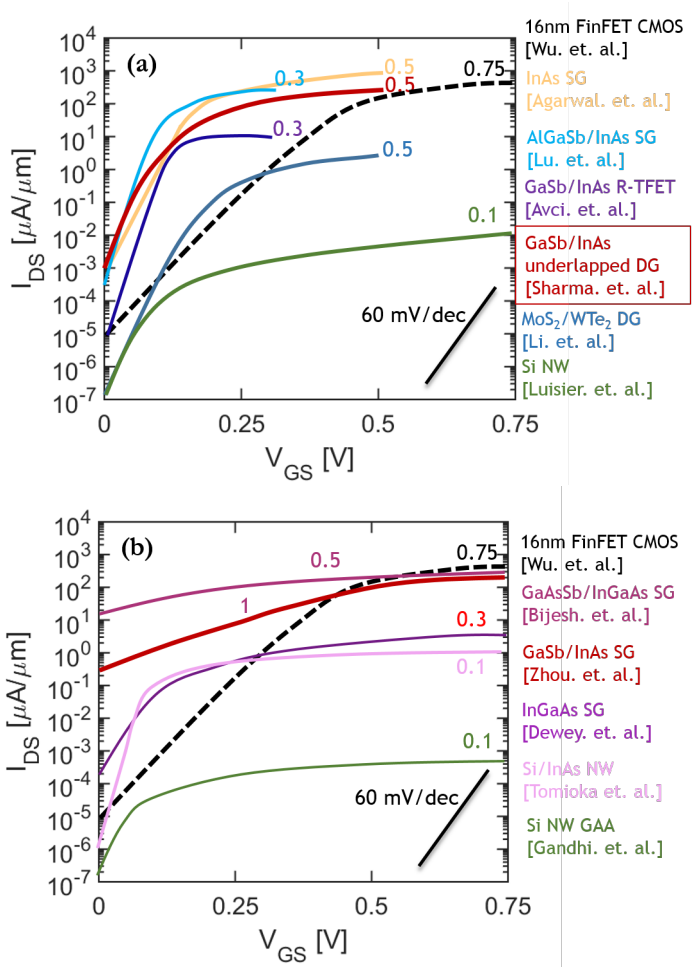

Fig. 4.1. Comparison of (a) Simulated (b) Experimental $I_D - V_{GS}$ characteristics for published n-channel TFETs. The curves are shifted to ensure that the region with steepest SS lies at origin.

trap-assisted tunneling, defects at high-k dielectric/semiconductor interface leading to enhanced Shockley-Read-Hall (SRH) leakage; all of which are generally neglected in simulations. Decoupling various non-idealities in search of the root-cause for degraded subthreshold-swing in experimental TFETs still remains a topic of intensive research. Khayer et. al. [47] first performed a simulation study on the band-tails in InSb nanowire, and showed that for channels $>$ 20nm, source band-tails can worsen the SS by almost 2x.

In this chapter, we report the effects of band-tails on the subthreshold characteristics of double-gate (DG) III-V tunnel-FETs based on GaSb/InAs broken-gap heterojunction. High source doping is required in TFETs to support high electric fields which are essential for achieving high drive currents. High doping is associated with band-tails that decay exponentially into the bandgap. Fig. 4.2. illustrates the density of states as a function of energy for a 3nm diameter GaSb nanowire doped p-type to $3x10^{19}cm^{-3}$, calculated using approach described in previou section. Away from the band edges, the band-tails decay in the bandgap as $e^{-\frac{|E-E_{C,V}|}{E_0}}$, where $E_{C,V}$ is the conduction (valence) band edge and E_0 is the Urbach parameter, which can be comparable to room temperature thermal energy, $k_BT = 26meV$ [47]. Thus, the decay of carrier density into the bandgap can be compared to the decay of carrier density above the band-edge due to thermal tail of the Fermi factor, which sets the ideal lower limit of 60mV/decade on SS in MOSFETs. However, in a TFET, it has not been experimentally shown that the band-tails would act in a similar way.

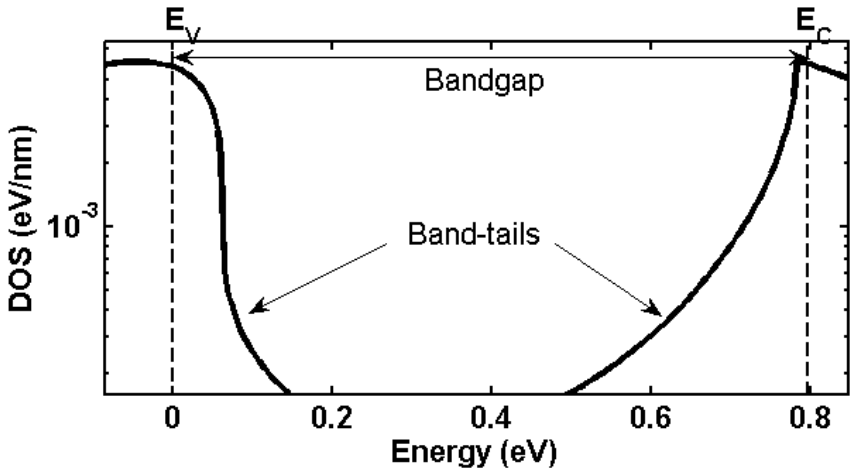

Fig. 4.2. Density of states as a function of energy of 3nm diameter of GaSb nanowire showing the exponentially decaying band-tails within the bandgap as $e^{-\frac{|E-E_{C,V}|}{E_0}}$, with E_C and E_V being the conduction band edge and valence band edge, respectively. In this case, $E_0 = k_BT$ and $N_A = 3\text{x}10^{19}cm^{-3}$.

In this work, using full band quantum mechanical model within Non-Equilibrium Greens Function (NEGF) formalism, we show that there can be a significant degradation of SS due to band-tail states within the bandgap. As a solution, we propose an intrinsic-source broken-gap TFET, which still achieves similar subthreshold characteristics and performance as a corresponding p-i-n TFET. We also study impacts of parameter variations in the new device.

4.2 Band-Tail Modeling

Band-tails result from geometrical and substitutional disorders as a consequence of heavy doping. We adopt a simple approach used by Khayer et. al. [47] which involves modification of self-energy that will reproduce the known exponential decay of the density of states into the bandgap within a few hundred millielectron volt of the band edges, which are energies of interest. A full-band, discretized, 8-band k.p model [48] is used within the Non-Equilibrium Greens Function formalism. The k.p Hamiltonian is implemented using finite difference method, hence the Hamiltonian accommodates for the effect of quantum confinement in the device bandstructure. Also the effect of doping and bandstructure discontinuity due to the heterostructure has been incorporated. The exponentially decaying band-tails in the source and drain regions result from the energy-dependent, diagonal, self-energy as in Eqn. 4.1 below.

$$\Sigma = \Sigma_O + \Sigma_R \tag{4.1}$$

$$\Sigma_R = -i\frac{\Gamma_i}{2}\delta_{i,j} \tag{4.2}$$

Here Σ_O is original self-energy matrix (without consideration of any band-tail effects), while the additional states within the bandgap arise from the doping dependent term Γ_i as defined in Eqn. 4.3 below.

$$\Gamma_i = \begin{cases} 0 & E < E_V \\ \Gamma_i^0 e^{-\frac{E-E_V}{E_O}} & E_V < E < \frac{E_C+E_V}{2} \\ \Gamma_i^0 e^{-\frac{E_C-E}{E_O}} & \frac{E_C+E_V}{2} < E < E_C \\ 0 & E > E_C \end{cases} \tag{4.3}$$

E_0 is temperature dependent term called Urbach parameter [49] which is used for defining the decay of band-tail and is usually determined by optical measurements. For GaSb, the typical value is experimentally observed as 0.15 eV at room temperature [50]. Note that the model introduces band-tails only in doped regions and does not account for any band-tails arising out of defects in intrinsic channel. In the ideal case, i.e. ignoring band-tail effects, $E_0 = 0$, which makes Γ_i for all energies. Hence, $\Sigma = \Sigma_O$ However, non-zero values of E_0 lead to band-tails into the band-gap; higher the value, lower the decay rate. The value of Γ_i^O depends mainly on doping density and for ultra-thin body (UTB) like structures, it can be defined as follows [51].

$$\Gamma_i^O = \frac{\pi N_A}{A} \quad \frac{q^2 L_D^2}{\epsilon} \Bigg)^2 . N_{1D}(E) \tag{4.4}$$

,where q is the magnitude of the electron charge, and $\hbar$ is the Plancks constant. $\epsilon = \epsilon_O.\epsilon_r$ with ϵ_O being the permittivity of free space and ϵ_r is the relative permittivity of the material where band-tails are under consideration. N_A is the doping density, A is the cross-sectional area, and $N_{1D}(E)$ is one-dimensional density of states. L_D is the screening length defined as [52]

$$L_D = \sqrt{\frac{\epsilon k_B T}{q^2 N_A}} \tag{4.5}$$

Here, k_B is the Boltzmann constant. For the ease of calculation of density of states, we assume that the density of states is equal density of electrons which can be calculated as follows:

$$N_e(E) = N_{1D}(E) = Trace(G^n)/2\pi = Trace(G^R \Sigma_S G^A)/2\pi \tag{4.6}$$

where G^R is the retarded Greens function and G^A is its complex conjugate transpose [52]. G^R is defined as [12]

$$G^R = [EI - H - \Sigma]^{-1} \tag{4.7}$$

The density of states as a function of energy calculated from Eqn. 4.6 for a 3nm diameter GaSb nanowire is shown in Fig. 4.2. The doping is set to 3x$10^{19} cm^{-3}$ while $E_0 = 26meV$.

By solving equations 4.4 and 4.6 self-consistently for doping density of $10^{19} cm^{-3}$ in the GaSb source, we have $\Gamma_i^0 \approx 75meV$, which is a reasonable value. The converged self-energy is used to solve two-dimensional NEGF transport equation coupled to Poisson electrostatics equation to obtain I-V characteristics. The k.p parameters for GaSb and InAs used in the TFET simulation are listed in Table 4.1. Due to unavailability of k.p paramaters for HfO_2 in literature, we assumed SiO_2 k.p parameters while using bandgap of 5.7 eV [53], electron affinity 2.25eV [54] and di-electric constant 16 [55] of HfO_2.

Fig. 4.3(a) plots the $I_D - V_{GS}$ characteristics of GaSb/InAs TFET for various source doping, when the Urbach factor is equal to thermal energy, $k_BT = 26meV$. Higher source doping leads to more states decaying into the band-gap which results in degraded SS. Fig. 4.3(b) shows $I_D - V_{GS}$ curves for a range of values of Urbach factor. It can be observed that even a small E_0 can significantly degrade the SS. For larger band-tails (higher values of E_0) the number of available states within the energy bandgap increases, which in turn, promotes larger tunneling currents in the

Table 4.1.
8 band k.p Parameters for InAs and GaSb [56]

Parameters	**n-TFET**	**p-TFET**	**Ankit**
$Luttinger Parameter, \gamma_1$	19.67	13.3	3.00
$Luttinger Parameter, \gamma_2$	8.37	4.4	0.55
$Luttinger Parameter, \gamma_3$	9.29	6.0	1.00
$Kane's Parameter, P_{cv}(eV)\gamma_3$	17.0	22.88	0.1
$Bandgap, E_G(eV)$	0.42	0.725	5.7(HfO_2)
$Effective mass, m_e^*$	0.023	0.042	0.2
$Spin Orbit coupling, \Delta_{so}(eV)$	0.38	0.76	0.044
$Valence Band offset, VBO(eV)$	-0.0733	0.6726	-3.9(HfO_2)

subthreshold region. For all cases, the off-currents for transport without band-tail consideration would be significantly lower because of lower SS.

4.3 Proposal of Intrinsic Source TFET

From the previous section, it is evident that band-tails arising from high source doping can be detrimental to subthreshold characteristics of a TFET. Electrically doping the source, a dominant method used to dope 2D material TFETs, could be an alternative to get rid of substitutional doping-dependent band-tails [57]. Electrical doping involves wrapping the source semiconductor with high workfunction metal to deplete it of electrons thereby realizing a p-type source. However, such an approach is experimentally challenging and the proximity between gate and source-metal contact will lead to deleterious coupling effects. In this section, we propose an intrinsic-source GaSb/InAs in an i-i-n configuration which achieves similar performance to that of a corresponding p-i-n TFET. The i-i-n TFET is free from band-tail effects and is

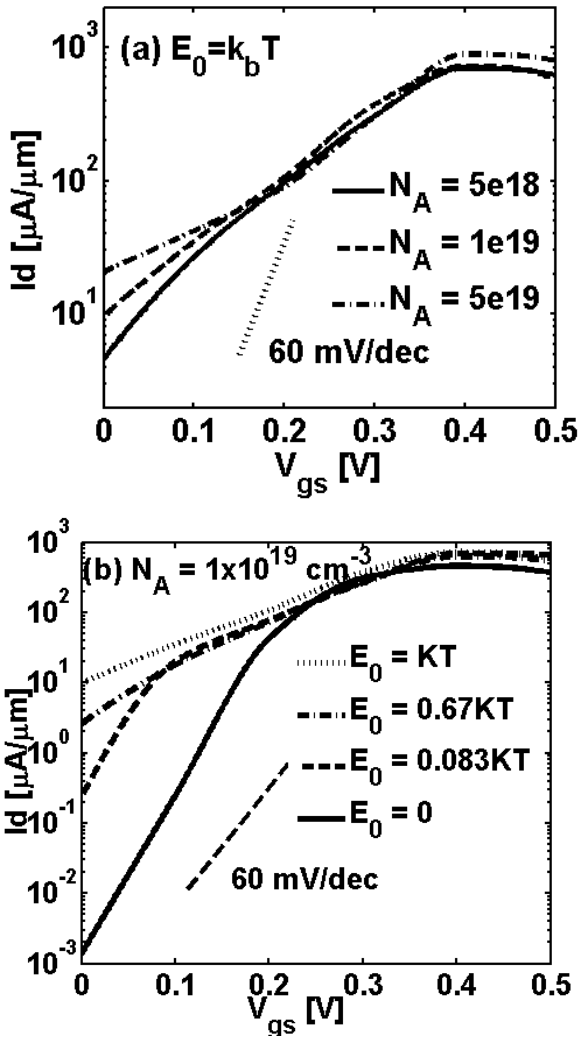

Fig. 4.3. $I_D - V_{GS}$ characteristics of double-gate GaSb/InAs TFET using k.p simulations for (a) A range of source-doping values when $E_0 = k_BT$. (b) A range of values of E_0 with band-tails considered in the source doped to $1\text{x}10^{19}cm^{-3}$.

compatible with existing fabrication techniques. The device structure and operating principle is explained in detail below.

4.3.1 Device Structure

The cross-sectional schematic of the proposed double-gate (DG) GaSb/InAs n-TFET with intrinsic-GaSb source is shown in Fig. 4.4.

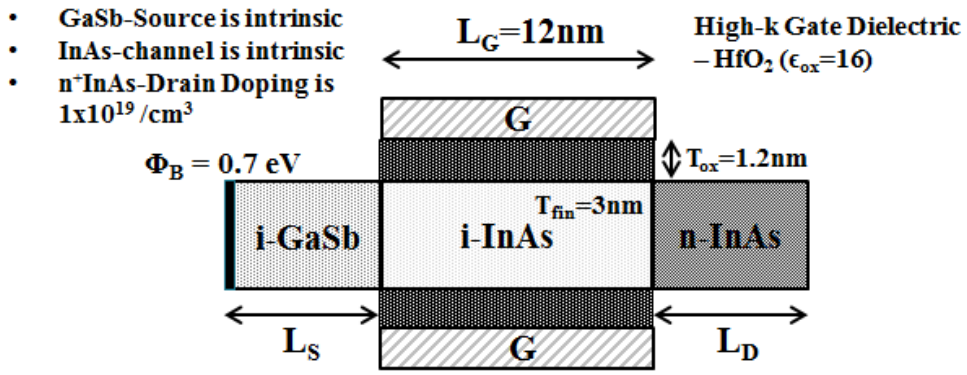

Fig. 4.4. Schematic of double-gate i-i-n TFET. The drawn gate-length is 12nm, fin-thickness is 3nm.

The TFET has a drawn gate-length of 12nm and a fin-thickness of 3nm. A high-k dielectric, HfO_2, with $\epsilon_{OX} = 16$, and physical thickness of 1.2nm is used. The low conduction band density of states in InAs leads to low channel capacitance, hence a relaxed oxide thickness of upto 2.4nm doesnt result in observable change in the device characteristics. The InAs channel is left intrinsic while the n^+-InAs drain doping is set to $1x10^{19} cm^{-3}$. Abrupt doping profile has been assumed for simulations. The devices can be grown on GaSb using solid- source molecular-beam-epitaxy [28] with in-situ source doping, thus realizing abrupt source-channel junctions. Such junctions play an important role in determining the performance of TFETs [29]. For realistic simulations, the interaction of intrinsic-GaSb source with the source metal contact needs to be carefully captured. It has been shown that fermi-level pinning in GaSb occurs near the valence band edge which leads to low Schottky barrier height for valence band electrons in most metal / p-type GaSb contacts [58].

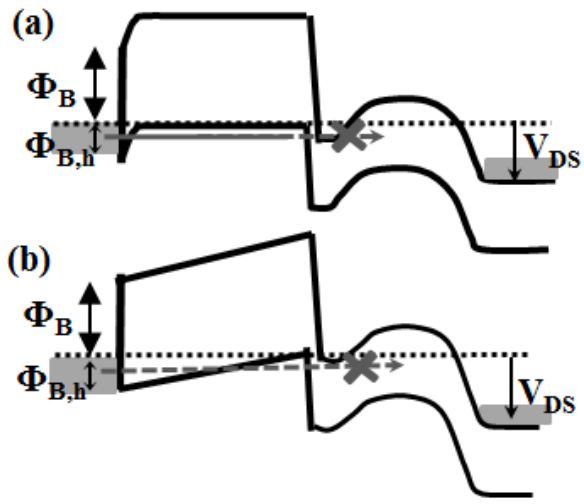

Fig. 4.5. Band-diagrams of (a) p-i-n TFET (b) i-i-n TFET in the OFF state. $\phi_{B,h}$ is the source-side schottky barrier for electrons in valence band.

Fig. 4.5(a) shows the band-diagram for p-i-n GaSb/InAs TFET in the OFF state. High p+-doping reduces the thickness of the barrier, $\phi_{B,h}$, which results in near-ohmic contact for valence band electrons in a p-i-n TFET. However, if the source is left intrinsic, the schottky barrier width is large and electrons within energy range from valence band edge of source to Fermi-level cannot participate in conduction as shown in Fig 4.5(b). For carriers below the valence band edge, there does not exist a barrier at metal contact-source interface, thereby leading to negligible contact resistance. Note, however, the channel barrier prevents their conduction in the OFF-state. It is also interesting to note that switching to intrinsic source doesnt add to significant series resistance in a TFET because the valence band electron density nearly equals the density of states within the valence band. This is in sharp contrast to an n-MOSFET, where reducing the doping proportionately reduces the conduction band electron density and hence the current.

4.3.2 Simulation Approach

The device simulations were performed using the quantum mechanical device simulator NEMO5 [9]. We used $sp3s^*$ tight-binding model with spin-orbit coupling to solve two-dimensional NEGF transport equations coupled to Poisson electrostatics equation for simulating TFET I-V characteristics. Non-ideal effects like phonon and surface scattering, oxide-channel interfacial traps were ignored and ballistic operation was assumed. The electrostatic potentials at the S/D contacts as well as gate contact were specified as boundary conditions. Gate-leakage current has been ignored in the simulations. To correctly capture the effects of Schottky barrier on transport, we assumed same tight-binding parameters for the metal as the source (GaSb in this case) and introduced a virtual metal conduction band edge $0.7eV$ above the Fermi energy of the metallic source contact, similar to approach discussed in [59]. A Schottky-barrier height, $\phi_{B,h}$, of $0.7eV$ (between GaSb conduction band and Fermi level) is assumed in simulations for conduction band electrons.

4.3.3 Simulation Results and Discussion

The $I_D - V_{GS}$ characteristics of intrinsic-source GaSb/InAs TFET is shown in Fig. 4.6(a). As shown in the figure, the intrinsic-source TFET achieves a minimum SS of 40 mV/decade. The gate-workfunction was set to $4.8eV$ to achieve off-current $\approx 1nA/\mu m$ for V_{DS}=0.5V, according to ITRS 2022 low-operating power specifications [27]. Fig. 4.6(b) shows the simulated band-diagram of the i-i-n TFET along the current transport direction, near the center of the fin, in the OFF (solid) and the ON (dashed) state. In the OFF-state, the channel presents a large tunneling barrier for the valence band electrons in the source, and the off-current is dictated by direct inter-band source to drain tunneling through the channel barrier. To illustrate further, Fig. 4.7 and Fig. 4.8 plot the energy-resolved carrier density and a corresponding energy-resolved current in the off-state and on-state respectively. The integral of energy-resolved current over entire energy range is equal to the net current

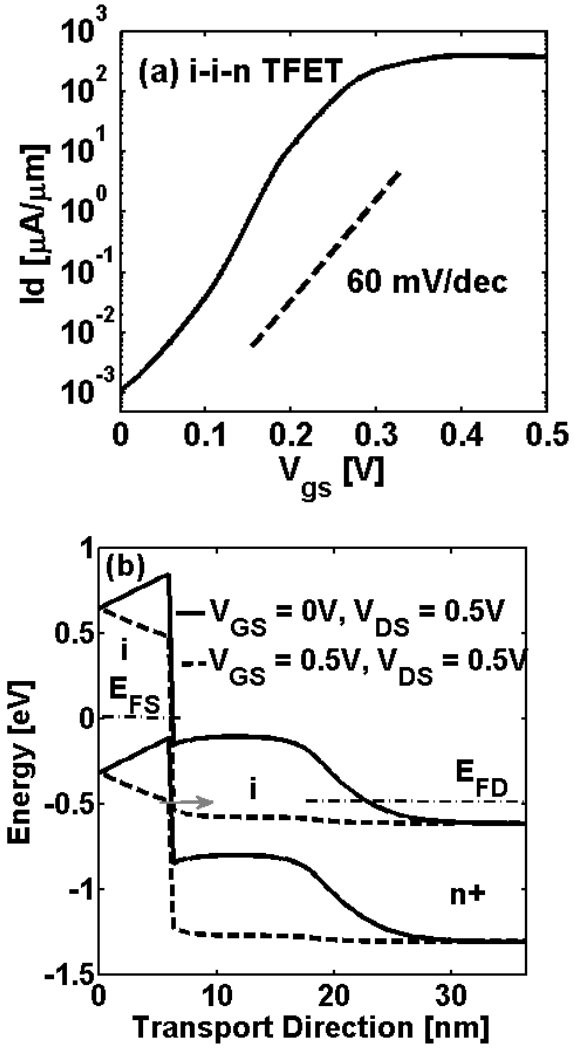

Fig. 4.6. Simulated (a) $I_D - V_{GS}$ curves (b) Band-diagrams in the OFF- and ON-state for intrinsic-source i-i-n TFET.

flowing through the device per μm. It is worthwhile mentioning that entire leakage current is due to direct source to drain tunneling. Other leakage-components like trap-assisted tunneling current and Shockley-Read-Hall recombination-generation current have been ignored in the simulations due to unavailability of suitable models. As the gate-voltage is increased, the channel bands move down, thereby exposing the broken-gap tunnel-junction leading to high on-current nearing 200μA/μm.

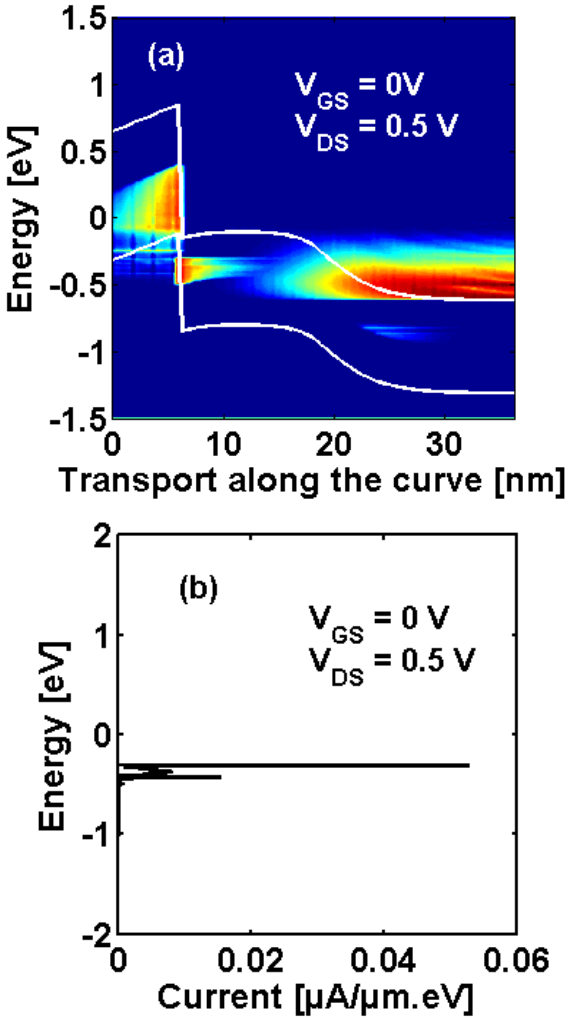

Fig. 4.7. Band diagram and energy resolved carrier density for i-i-n TFET; (b) Energy-resolved current density in the OFF state.

4.4 Variation Analysis

With the scaling of the devices in to nanometer dimensions, the effect of geometrical variations on the device characteristics becomes increasingly important. In this section, we assess the impact of gate-length, fin-thickness and oxide-thickness variations on the device behavior. Fig. 4.9(a) shows the transfer characteristics of the

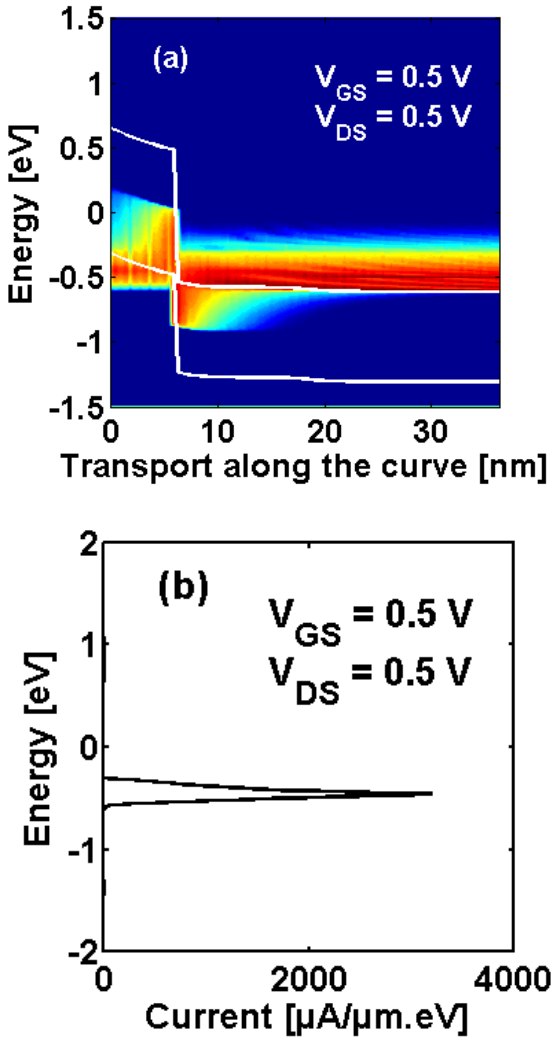

Fig. 4.8. Band diagram and energy resolved carrier density for i-i-n TFET; (b) Energy-resolved current density in the ON state.

proposed TFET for different gate-lengths.

The off-current rises sharply for scaled gate-lengths due to increase in direct inter-band source to drain tunneling. Large channel lengths reduce off-state current, however it should be noted that the transport would not remain ballistic anymore and scattering effects could not be ignored. Hence, we restrict our analysis to gate-lengths less than 15nm.

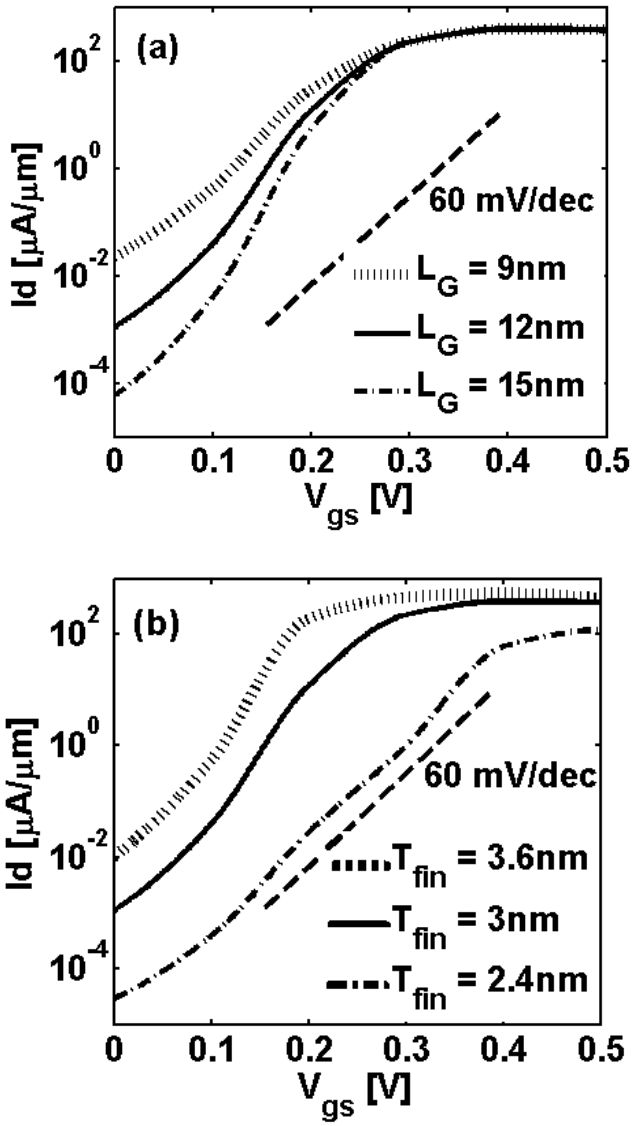

Fig. 4.9. Variation effect of (a) Gate-length, L_G (b) Fin-thickness, Tfin on i-i-n TFET $I_D - V_{GS}$ characteristics

The sensitivity of $I_D - V_{GS}$ characteristics to fin-thickness is shown in Fig. 4.9(b). Fin-thickness relaxation increases the OFF-current and reduces the average SS due to reduced gate-control. On the other hand, fin-thickness down-scaling is detrimental to ON-state performance in III-V transistors as clearly observed in Fig. 4.9(b). InAs has a very low density of states in the -valley [60], which tends to greatly reduce the

inversion charge for a fixed gate overdrive. At high gate field, due to quantization, the energy levels in -valley rise faster than the L and the X-valleys. Since the current is largely carried by these heavier mass L and X-valleys, the drive-current is reduced as observed in Fig 4.9(b). Another issue associated with fin-thickness scaling is the shortening of the broken-gap energy window. The tunnel-junction tends towards staggered-gap due to band-gap widening caused by quantum confinement as shown in Fig. 4.10.

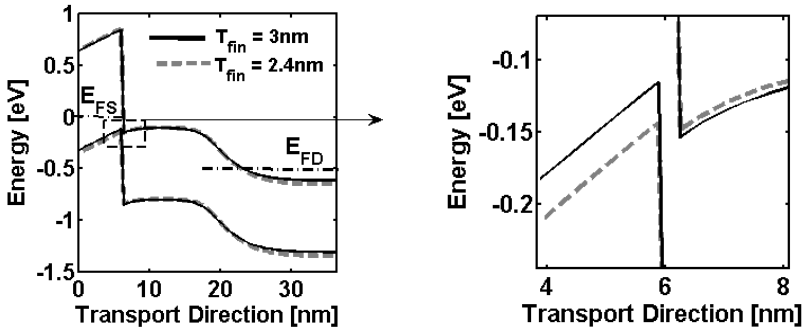

Fig. 4.10. Band-gap widening due to quantum confinement as a result of aggressive fin-thickness scaling can make the band-alignment staggered thereby making turn-on difficult.

This makes it difficult to turn-on the intrinsic-source TFET as explained below. For the normal operation of i-i-n TFET, it is required that the tunnel-junction presents a broken-gap band-alignment. If the TFET is a homo-junction or if the junction happens to be staggered-gap with an intrinsic source, it is almost impossible to enhance the electric-field across the tunnel-junction to achieve high drive current. A major portion of the drain-source potential gets dropped across the depletion region in the source, while the tunnel-junction width remains large across the entire gate-voltage sweep. Hence, it is difficult to turn-on the homo-junction or staggered-gap TFET if the source is left intrinsic. To elucidate this concept, we simulate a homojunction-InAs TFET having exact same geometry. Mid-gap Fermi-level pinning

has been assumed at source contact. Fig. 4.11(a) shows the band-diagram InAs TFET in the OFF (solid) and ON (dashed) state.

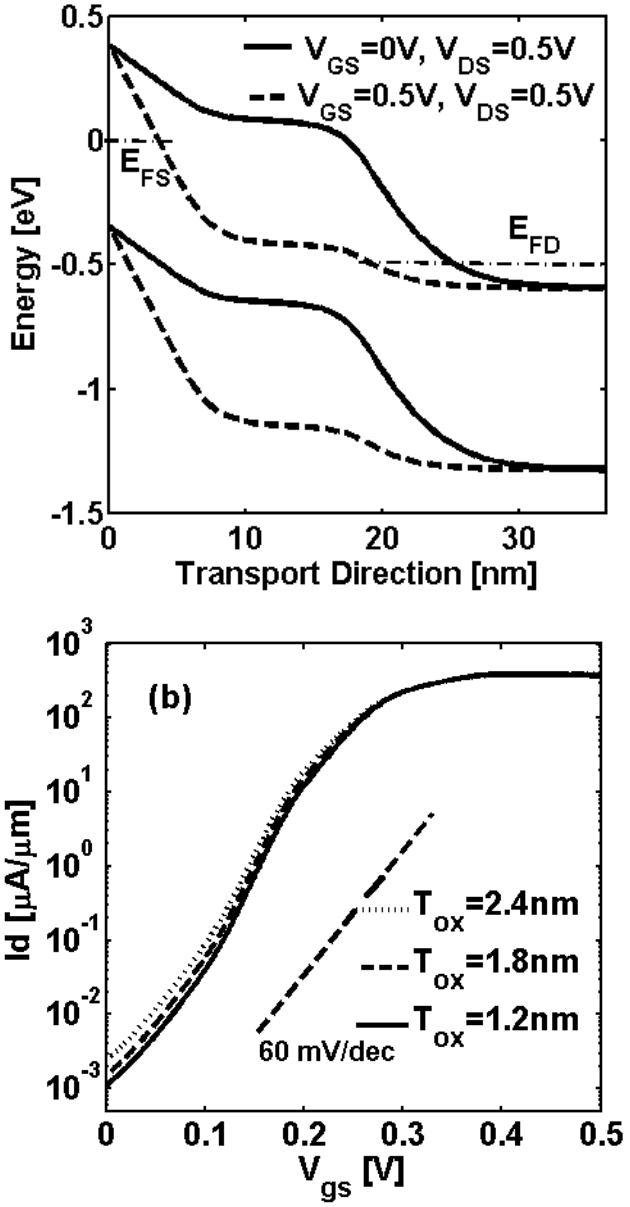

Fig. 4.11. (a) Simulated band-diagram of intrinsic-source InAs TFET. Even in the ON-state, the barrier remains large enough to prevent sufficient carriers required for high drive current. (b) Oxide-thickness variations

Even at high V_{GS}, the tunnel junction remains wide enough and prevents significant carrier tunneling. The impact of variations in oxide-thickness is shown in Fig. 4.11(b). The $I_D - V_{GS}$ characteristics are relatively insensitive to minor variations in the oxide thickness. This is a direct consequence of low-density of states of InAs, which results in low channel capacitance compared to oxide-capacitance. Hence, most of the applied gate-potential appears as channel surface potential with a little potential drop across the oxide.

4.5 Conclusion

This chapter examined the effects of band-tails associated with heavy source doping on subthreshold swing of III-V TFETs. Conventional p-i-n TFETs require high source doping to support high electric field in the source-to-channel region. High electric field in turn provides high interband tunnel drive current. Due to geometrical and substitutional disorders, the high source doping gives rise to band-tails that decay exponentially into the bandgap. These band-tails can behave like Fermi-tails and are shown to be detrimental to subthreshold characteristics of a TFET. To address this concern, we propose an intrinsic-source broken-gap TFET which achieves similar transfer characteristics as that of a p-i-n TFET, while simultaneously getting rid of any band-tail effects by having an undoped source. The high-drive current is supported by broken-gap tunnel junction while the Fermi-level pinning near the valence band of GaSb source helps in realizing near-ohmic source contact. Our detailed simulation analysis shows that intrinsic-source GaSb/InAs TFETs could be a stepping stone in the path to successful experimental realization of subthermal SS in III-V TFETs.

5. TFET APPLICATIONS - LOGIC AND MEMORIES

5.1 Inverter Chain Energy and Delay

To evaluate the circuit-level metrics of the heterojunction n- and p-type TFET devices discussed in *Chapter 3*, a loaded TFET based 6-stage inverter chain is implemented and compared with an inverter chain implemented entirely using FinFETs. The interconnection of n- and p-type TFETs in each constituent inverter is shown in Fig. 5.1. All the devices are minimum sized, i.e. the reference device structure described in *Chapter 3*. Corresponding layouts of inverters implemented using FinFETs and TFETs are shown in Fig. 5.2.

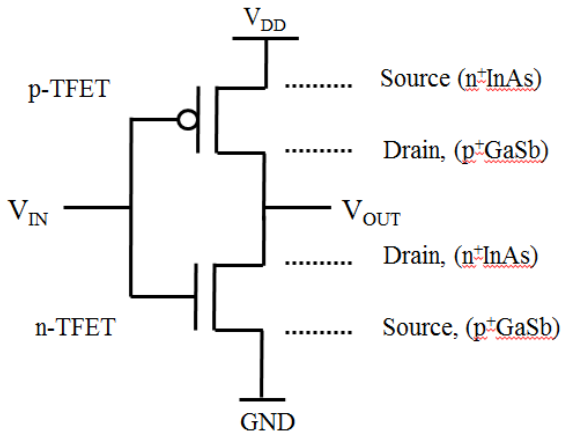

Fig. 5.1. Inverter schematic using TFETs. Tunneling occurs near the source region for both TFETs.

Here, F is the minimum feature size. The vertical TFETs use gates on the sides which can be contacted outside the active region. Hence, the contacted gate area can be reduced thereby resulting in 40% density gain over lateral devices [25].

To account for the gate parasitics, a fanout of 4 was considered at each stage. A logic activity factor of 10% is considered to represent switching activity realistically.

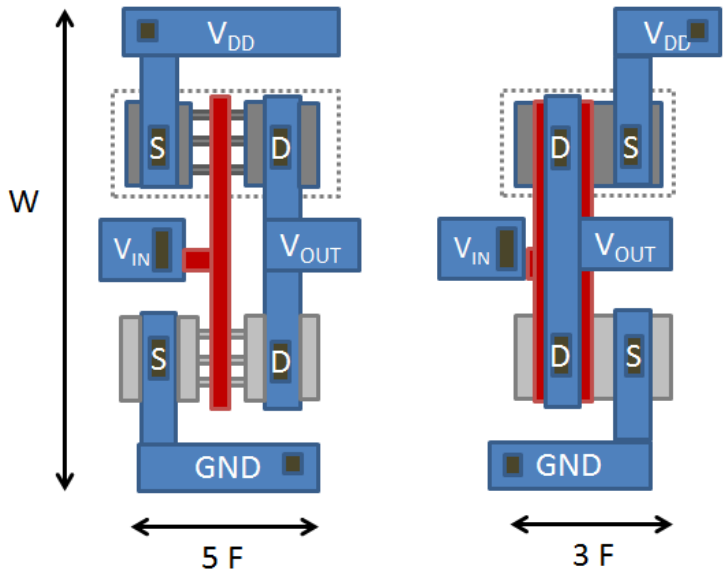

Fig. 5.2. (a) FinFET (b) Vertical TFET inverter layout. F is the minimum feature size.

The delay v/s supply voltage curve for these 6-stage inverter chains is shown in Fig. 5.3(a). At high V_{DD}, due to the low on-current of TFET, a TFET-based inverter chain cannot achieve as high performance as FinFET-based logic. However, for lower supply voltage targets, the TFET-based logic shows higher performance than FinFET-based logic due to its lower parasitic capacitance. In addition, the total energy consumption which includes the leakage energy and dynamic energy, shown in Fig. 5.3(b) is also low due to TFETs 100x lower standby leakage currents. While the reduction in supply voltage and capacitances causes the dynamic energy to improve in both FinFETs and TFETs, the leakage energy in TFET-based logic does not rise as severely as in FinFET-based logic (Fig. 5.4).

From the above analysis, it follows that TFETs would be good candidates for ultra-low voltage applications (or near-threshold voltage applications) which require medium-throughput but with ultra-low power consumption. To estimate the energy and performance metrics of systems built using TFETs and FinFETs in the presence of interconnect delay, we consider a LEON3 SPARC processor in the next section.

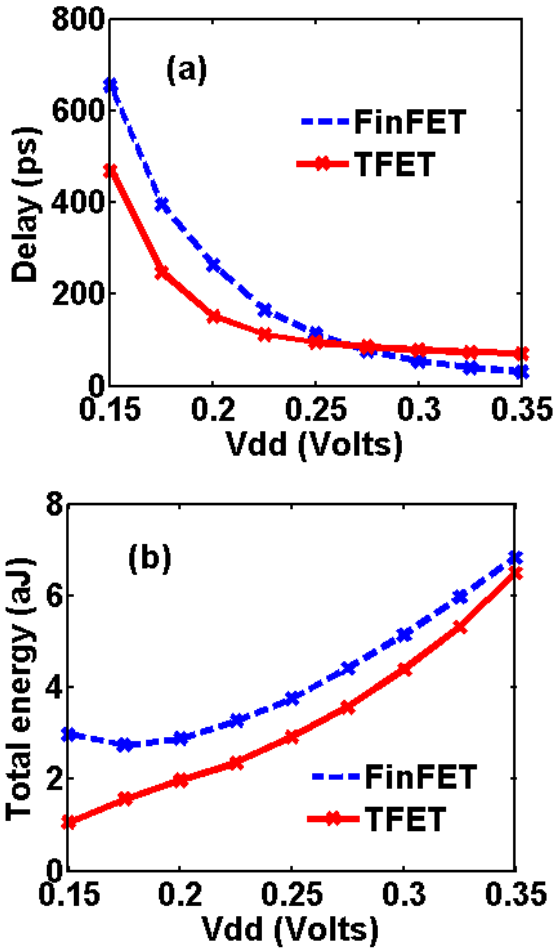

Fig. 5.3. (a) Delay v/s supply voltage (b) Total energy v/s supply voltage for 6-stage inverter chain implemented using FinFETs (dashed line) and TFETs (solid line).

5.2 System Level Evaluation of LEON3 Processor

Delay due to on-chip interconnections has become a critical factor for high performance designs in recent years. With devices scaling down into sub-20nm regime, wire resistance, R, and wire capacitance, C, have increased and hence, wire delays are significant. To assess the benefits of TFETs at scaled nodes in a realistic manner, in this section, we evaluate the performance of a TFET-based LEON3 processor and compare it with FinFET-based processor in the presence of interconnects modelled

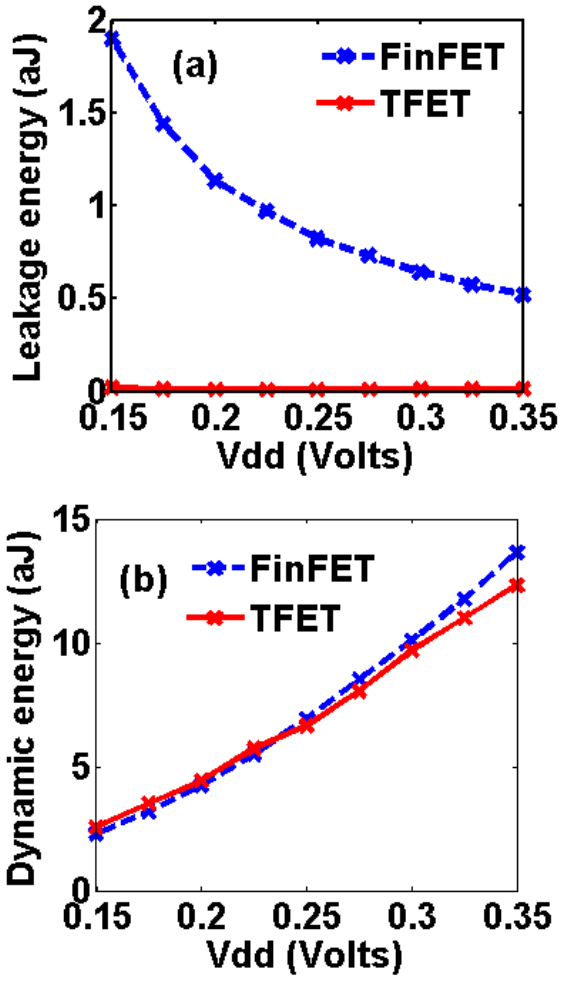

Fig. 5.4. (a) Leakage energy v/s supply voltage (b) Switching energy v/s supply voltage for 6-stage inverter chain implemented using FinFETs (dashed line) and TFETs (solid line).

as distributed RC wire-loads.

The values for wire R and C per unit length were extracted from the analytical interconnect model of CACTI cache simulator [19] which models RC based wires up 32nm technology node. Beginning with the projected R and C, multiple wire-load model sets were generated by scaling the R and C. The exact RC values, for varying wire-load conditions, used in this work are listed in Table 5.1. For example, for device structures described in Chapter 3, assuming Copper interconnect, the resistance for

FinFET is $R = 73\Omega/\mu m$, while for TFET, $R = 44\Omega/\mu m$. For a gate pitch of $\approx 40nm$ for vertical TFETs, the resistance per fanout would be 1.76Ω.

Table 5.1.
Wire Load Models

Device	**Resistance per fanout** (Ω)		**Capacitance per fanout** (fF)	
	FinFET	**TFET**	**FinFET**	**TFET**
WL1	2.92	1.76	0.011	0.011
WL2	5.84	3.52	0.022	0.022
WL3	11.68	7.04	0.044	0.044
WL4	23.36	14.08	0.088	0.088
WL5	46.72	28.16	0.176	0.176

The above wire-load models were used to synthesize LEON3 processor at a near-threshold $V_{DD} = 0.25V$ using Synopsys Design Compiler. The cell libraries needed for the synthesis included an inverter, 2 input NAND gate, 2 input NOR gate and a transmission gate based positive edge triggered D flip-flop. SPICE compatible compact lookup table models of TFETs and FinFETs were used to describe these gates and D flip-flop in the form of a SPICE netlist. Using Cadence Encounter Library Characterizer, these gates and the D flip-flop were characterized for power and timing characteristics by applying various input slew and load conditions. Due to non-availability of layouts for these cells, we do not consider the exact area information. Hence, the synthesis tool optimizes only for the delay and power while ignoring area constraints. The maximum attainable frequency of operation, as reported by the synthesis tool, for the LEON3 processor is shown in Fig. 5.5. The wire load was varied for each new synthesis. It is observed that with no wire load or at very small wire loads, when the gate parasitics entirely dominate the interconnect parasitics,

LEON3 realized using FinFETs can deliver higher performance than when realized using TFETs. When the gate parasitics become comparable to interconnect parasitics (WL1-WL4), TFETs turn out to be a better choice in terms of performance for realizing large circuits. Under heavy interconnect dominated situations (WL5), FinFETs are preferable for achieving high performance primarily because of their higher average drive currents.

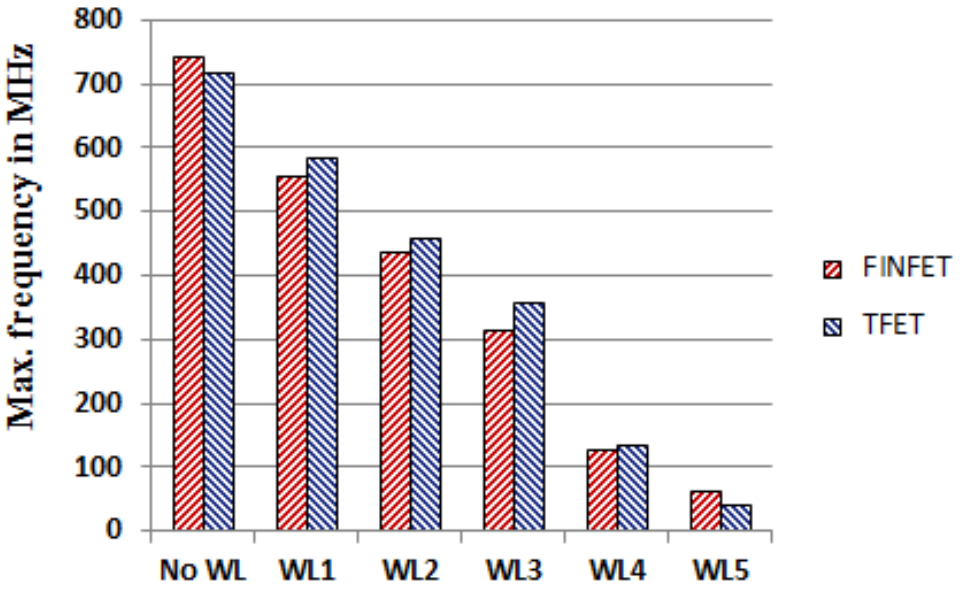

Fig. 5.5. Maximum operable frequency of LeonSPARC for varying interconnect RC values listed in Table II.

The total power consumption of the LEON3 processor, as reported by the synthesis tool, for the various TFET and FinFET realizations with varying interconnect parasitics is compared in Fig. 5.6.

The LEON3 processor realized using TFETs operates at much lower power (¿50%) than that realized using FinFETs for all load conditions. The leakage power accounts for almost 50% of the total power consumption in FinFET-based realization. In contrast, the LEON3 processor realized using TFETs shows nearly 50% total power reduction primarily because of negligible leakage current of TFETs. The switching power dissipation is given by $C_L V_{DD}^2.f$, where f is the frequency of operation. As

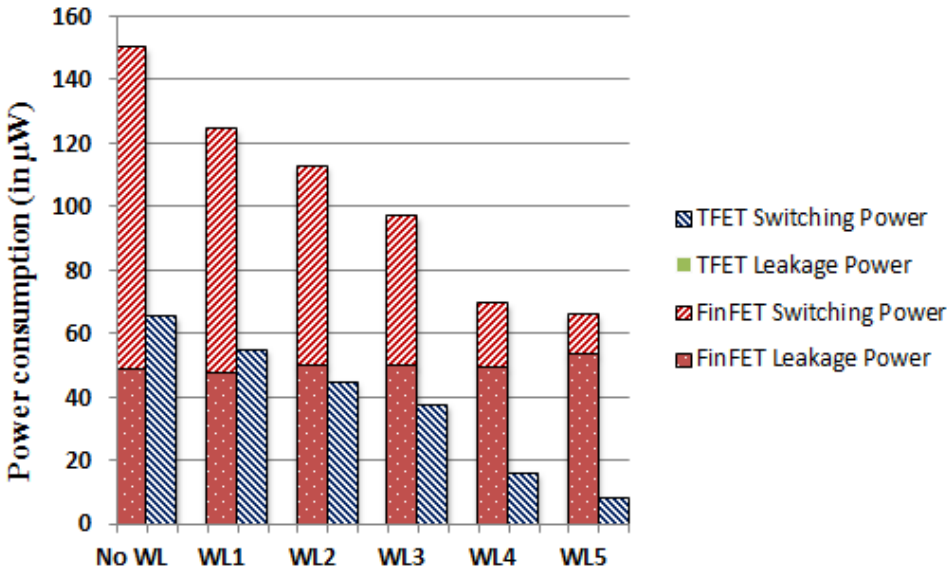

Fig. 5.6. Power consumption of LEON3 processor realized using TFETs and FinFETs under varying interconnect parasitics.

the interconnect parasitics increase, the maximum frequency at which the processor can operate reduces. Even though the wire load capacitance increases, this reduction in operating frequency causes the active power dissipation to fall drastically. On the other hand, leakage power being independent of the operating frequency remains nearly constant and starts to dominate the total power consumption in FinFETs with increasing interconnect parasitics.

5.3 8T TFET-based SRAM

The asymmetric current flow of TFET places restrictions on the use of the pass gate and the transmission gate [61]. This limitation is not severe for logic circuits since the CMOS logic, which is the most widely used logic, is not affected by this property because the current is expected to flow only in one direction in the channel of each transistors. Moreover, any pass-gate logic can be easily converted to CMOS logic to prevent malfunctions with TFET. However, the impact of TFET's asymmetric current flow on SRAM is significant since standard 6T SRAM uses pass gates for

access transistors, which is not trivial to replace. Hence, a 6T TFET-based cell with simultaneous read and write is unrealizable . In order to circumvent this limitation, we design an 8T cell, with both outward facing access transistors and compare them with 8T FinFET SRAM cells. Fig. 5.7. shows the write operation; whereby a 0 is written only from one access transistor while the other remains OFF. This results in slight WNM degradation as shown in Fig. 5.8(b). To assist a successful write, the access transistors are upsized to 3 fins. Fig. 5.9(a). shows that there is sufficient hold-SNM suggesting that hold state is not a serious hindrance for near-threshold (0.25V) operating voltages. The striking advantage of TFETs is seen from Fig. 5.8(a). and Fig. 5.9(b) where the SRAM can operate at similar frequency (with degraded WNM) as FinFET based SRAM but at 100x lower standby power.

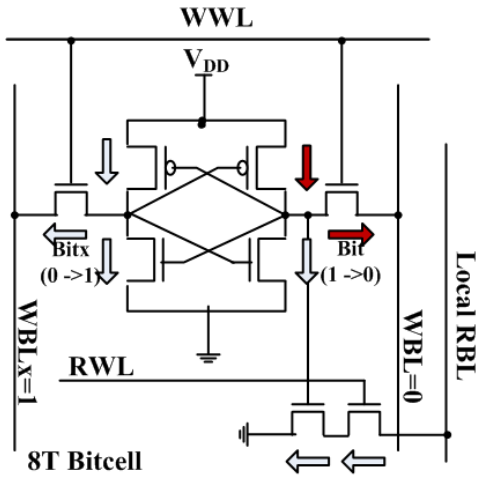

Fig. 5.7. 8T TFET-based SRAM cell configuration. During the 'write' operation, a '0' is written only from one access transistor while the other remains OFF

5.4 TFET-based Gain-Cell embedded-DRAM

Logic-compatible gain-cell (GC) embedded DRAM arrays are considered to be a competing alternative to SRAM due to their small transistor count, low static leakage and two-port functionality [62–66]. However, the exponentially increasing off-state

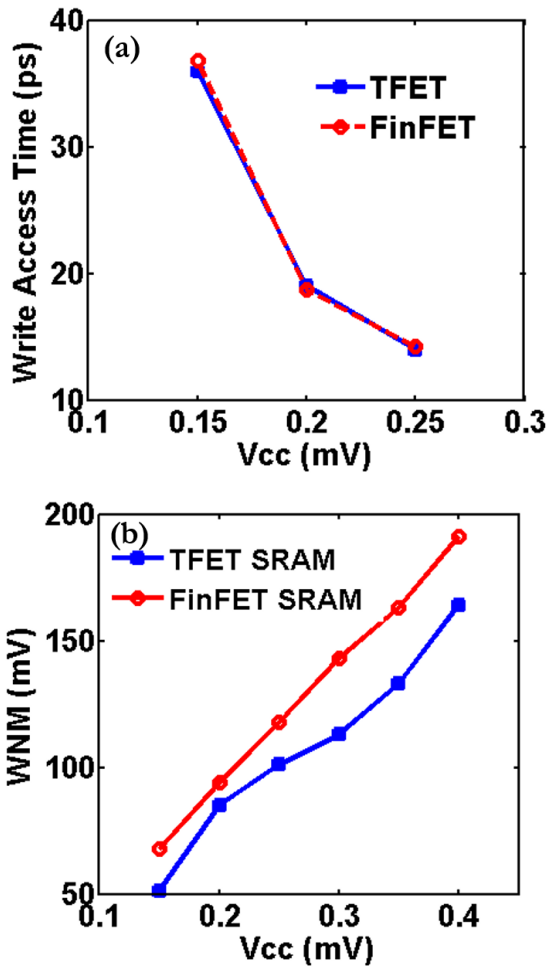

Fig. 5.8. (a) Write access time vs. supply voltage (b) Write Noise Margin vs. supply voltage

leakage of bulk MOSFETs due to continued scaling has led to extremely low data retention time (DRT) [67]. For energy-constrained biomedical systems, long retention times of 1-10ms are key design goal in order to achieve low retention power while for high-end processors, 10-100s retention time has previously been reported in mature CMOS technologies like 65nm [65]. Here we propose a novel single-supply 4T GC-eDRAM bitcell based on source-underlapped sub-10nm TFETs, operating at ultra-low voltage of 0.35V, and compare their performance against conventional TFET and Si-FinFETs based eDRAM. To further reduce the off-state leakage, the gate-metal

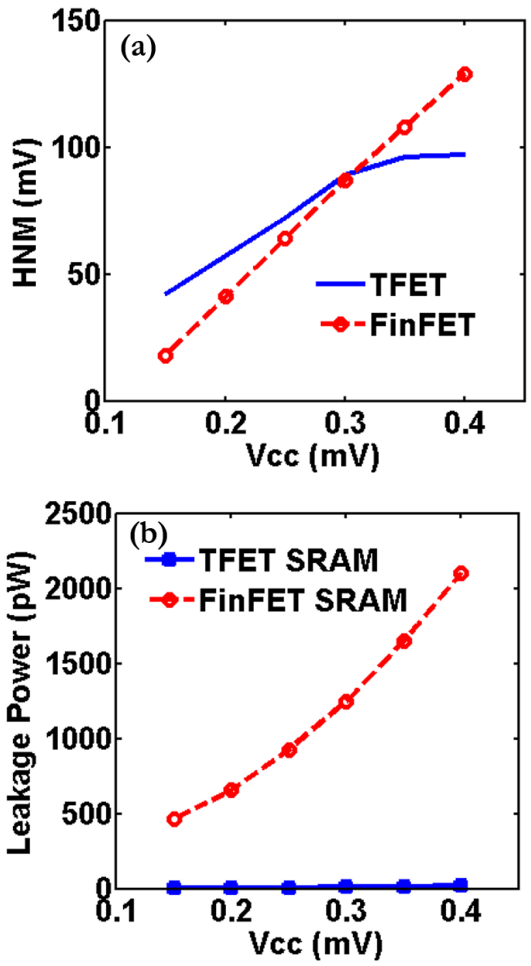

Fig. 5.9. (a) Hold Noise Margin v/s supply voltage (b) Leakage power v/s Supply voltage for single SRAM cell.

workfunction is increased by $0.1eV$ for n- and reduced by $0.1eV$ for p-type devices. Fig. 5.10(a) shows the resulting change in I-V characteristics of source-underlapped n-TFET. The schematic of proposed 4T-GC is shown in Fig. 5.10(b).

Since the TFETs are unidirectional, a transmission gate, with single-fin transistors, is required for bidirectional conduction with the current directionality as shown. To write a 1, WWL and WBL are pulled high. p-TFET charges the storage node (SN) to 1, while the n-TFET remains in non-conduction state because extremely low leakage due to negative V_{DS}, whereby the bandgap of InAs drain cuts-off the broken-

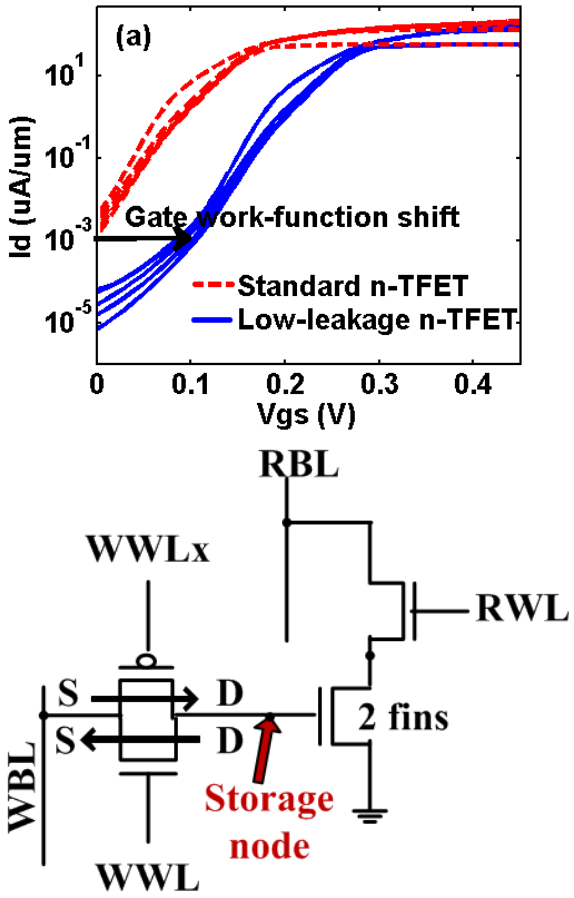

Fig. 5.10. (a) Gate work-function shift by $|0.1eV|$ to obtain ultra-low leakage access TFETs. (b) 4T TFET based eDRAM cell. The current conduction directions are shown by arrows.

gap tunneling window. To write a 0, WBL is pulled low. n-TFET discharges the storage node (SN) to 0, while the p-TFET remains in non-conduction state because of positive V_{DS}. Since the TFETs exhibit enhanced drain capacitance as discussed in Section VI, the proposed circuit also enhances the storage-node capacitance which is essential for high data-retention time. Fig. 5.11(a) demonstrates the circuit operation having subsequent read and write operations with standby states in between. The data retention time is defined as the maximum interval from writing a data level into the bitcell while still being able to correctly read out the written level. Assuming it to be 50% of V_{DD}, data retention time of proposed GC is $\approx 25\mu s$ as

observed from HSPICE plot of storage node voltage in Fig. 5.11(b). For these simulations, the fin-width was assumed to be four times the fin-thickness. Table. 5.2 presents the comparison of data retention time for different realizations usign three different devices under iso-cross-sectional area conditions. Extremely low DRT for 9nm Si FinFET, because of their large leakage, makes them unsuitable for practical implementation. TFETs show reasonable DRT ranging in few microseconds due their much lower leakage current. Source-underlapping the TFETs further helps in improving DRT to $25\mu s$.

Table 5.2.
Data Retention Time Comparison

Device	**Data Retention Time**
$Si - FinFET$	$5ns$
$GaSb - InAsTFET$	$10\mu s$
$6nmunderlappedGaSb - InAsTFET$	$25\mu s$

The proposed 4T gain cell can potentially be used for realizing long retention time GC DRAM at sub-10nm gate-lengths, thus addressing the scaling bottleneck associated with traditional MOSFET based eDRAMs. In addition, the suppressed temperature dependence of current in TFET, especially as compared to exponential dependence as in a subthreshold MOSFET, enhances robustness of scaled-TFET based eDRAMs.

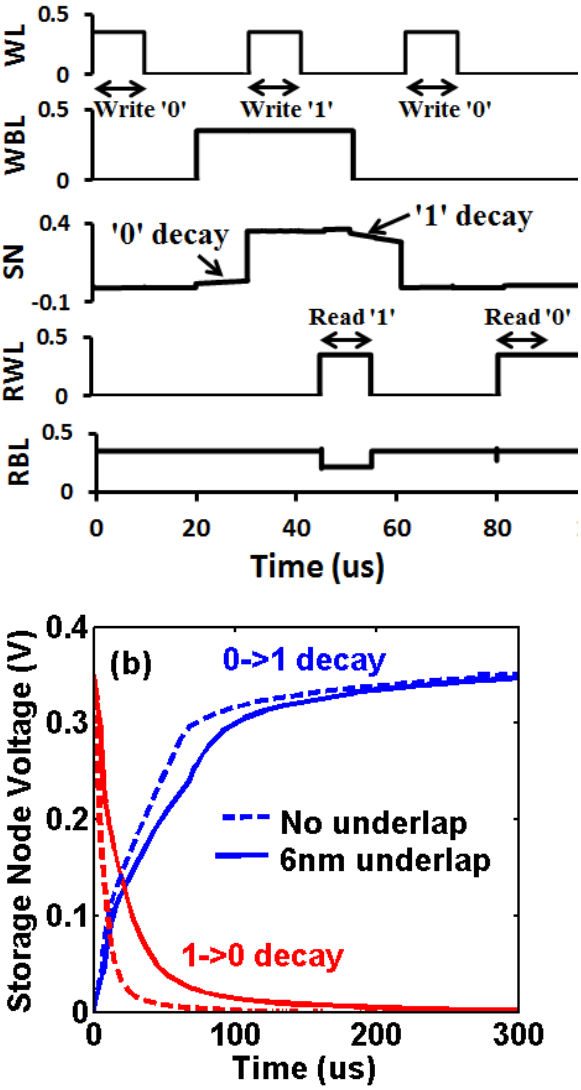

Fig. 5.11. (a) Timing diagram of subsequent writes and reads. Plots are extracted from HSPICE simulations. (b) Comparison of storage node voltage decay following a write operation under worst case WBL bias conditions. The underlapped TFETs show higher DRT because of their lower I_{OFF} compared to conventional non-underlapped TFETs.

5.5 Conclusion

A double-gate vertical n-type and p-type underlapped TFETs based on heterostructure GaSb-InAs, compatible with digital-circuit implementation, were com-

pared with symmetrically underlapped FinFETs, at sub-10 nm gate lengths for near-threshold logic operation. An investigation of TFET-based 6-stage inverter chain shows that TFETs can deliver a better performance at sub-threshold voltages (0.25 V) while operating at 100x lower standby power. A detailed circuit assessment of these devices was carried out at near-threshold voltages by synthesizing a LEON3 processor under varying interconnect scenarios. At near-threshold voltages and in the presence of moderate interconnect parasitics, TFET implementations were found to be preferable because of their ability to deliver similar performance as FinFETs while consuming nearly 50% lower power. As a result, GaSb-InAs TFETs appear to be a good choice for future ultra-low power applications since they enable a continuation of device scaling. At the same time, they provide additional benefits in power savings while delivering the same performance as Si FinFETs at near-threshold voltages.

To demonstrate their potential in a circuit application, a 4T gain cell is proposed, which utilizes the low-leakage and enhanced drain capacitance of TFETs to realize a robust and long retention time GC e-DRAMs at sub-10nm gate-lengths. Our device/circuit level evaluation of source-underlapped GaSb-InAs n and p-type TFETs demonstrates that they are promising candidates for future analog and ultra-low power digital applications.

6. NEGATIVE CAPACITANCE FETS

6.1 Introduction

The idea of utilizing negative capacitance of ferroelectrics to reduce the subthreshold swing of MOSFETs below 60mV/dec was proposed in 2008 by Salahuddin and Datta [68]. The proposal involves depositing the ferroelectric in the gate-stack of the MOSFET, the resultant device being called the Negative-Capacitance FET (NCFET). NCFET utilizes the negative capacitance of the ferroelectric in series with the underlying MOSFET, to cause an internal voltage amplification, thereby lowering the SS.

Recently, the validity of negative capacitance concept has been experimentally established and sub-60 mV/decade switching characteristics have been demonstrated in a hysteresis-free manner in long-channel MOSFETs [69–73]. However, the viability of negative-capacitance operation in sub-10nm technology nodes still needs to be explored and understood. Aggressive downscaling leads to quantum-mechanical effects which directly modify the charge distribution and potential profile within the channel. Since the capacitance matching depends on the MOS capacitance (which directly depends on the charge distribution), traditional approaches of NCFET modeling fail to accurately predict device behavior of nanoscale NCFETs.

In this chapter, we explore the design-space of NCFETs by performing a cross-device architecture analysis encompassing bulk-MOSFET, FDSOI (Fully Depleted Silicon on Insulator) MOSFET, and FinFET configurations in combination with the HfZrOx ferroelectric. Our results show that FDSOI and FinFET configurations can significantly improve the NCFET performance, thanks to their undoped body and improved gate-control which results in better capacitance matching. To start, we describe the origin of hysteresis in classical ferroelectric materials like Lead Zirconate

Titanate and Barium Titanate. However, these materials lack CMOS process compatibility. To counter this bottleneck, we utilize doped HfO_2, which has been shown to exhibit ferroelectricity, although it still remains an area of active research. We study the published HfZrOx ferroelectrics (FE-HZO) and choose a reference ferroelectric for NCFET simulations. Next, we perform a scalability analysis of NCFETs systematically. First we present the challenges associated with HfZrOx-based bulk-NCFETs, mainly arising from capacitance mismatch aggravated by substrate doping. The next subsection presents the design requirements of FE-HZO in FDSOI-NCFETs. Finally, we explore the potential for sub-10nm NC-FinFETs. A low-voltage NCFET operating down to 0.25V is predicted using ultrathin 3nm FE-HZO films. We summarize our findings in conclusion section of this chapter.

6.2 Background - Ferroelectrics

6.2.1 Introduction to Ferroelectrics

A ferroelectric is a non-conducting material characterized by the presence of two stable states with non-zero electric polarization, even in the absence of an applied external field. It was discovered in 1920 in Rochelle salt by Vasarek [74]. This was followed by demonstration of ferroelectricity in several inorganic perovskites, particularly Lead Zirconate Titanate($PbZr_xTi_{1-x}O_3$) and Barium Titanate ($BaTiO_3$). Since their discovery, they have been employed in numerous applications, covering all areas of our workplaces and homes. For example, the nonlinear nature of ferroelectric materials is utilized to make tunable capacitors. Furthermore, the development of non-volatile ferroelectric random access memories (FeRAM) based on perovskites has been actively progressed since 1980s and has been under volume production as a low-density embedded memory since 1995.

Ferroelectricity is a result of spontaneous electrical polarization in the unit cell as a result of non-centrosymmetric nature of the crystal structure. For instance, in

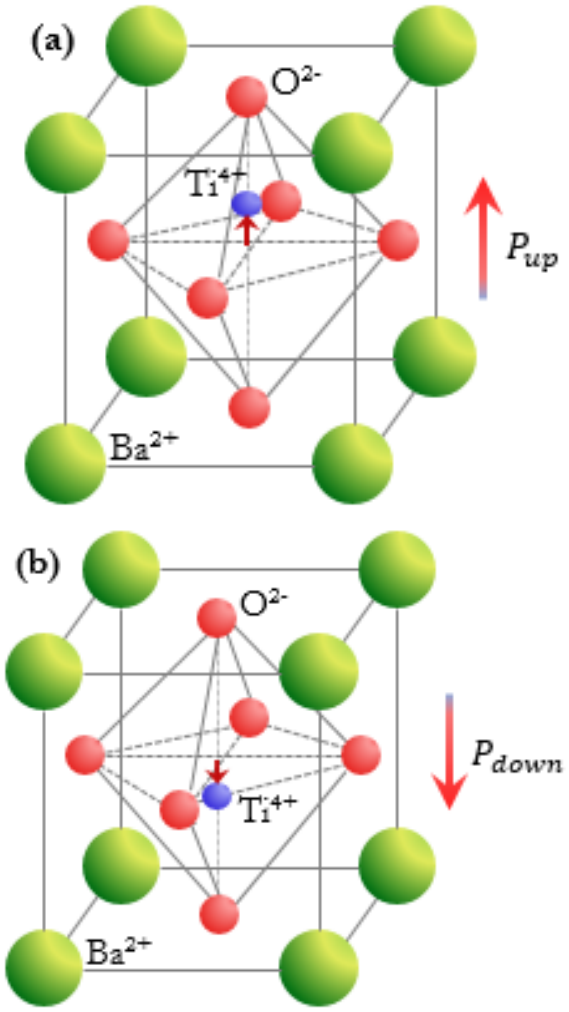

Fig. 6.1. Unit cell of classical ferroelectric $BaTiO_3$ showing (a) Upward polarization (b) Downward polarization

$BaTiO_3$, the dipole originates from the displacement of Ti^{4+} ion from the body center as shown in Fig. 6.1. The displacement, δ, of the central ion is of the order of picometres, which results in the net spontaneous polarization of $P = q.\delta/ca^2 \approx 50\mu C/cm^2$, where c and a are the sides of tetragonal unit cell of $BaTiO_3$. The displacement of central ion in two opposite directions corresponds to two stable states of the ferroelectric. This corresponds to two local minimas separated by an energy barrier in

the energy landscape of the ferroelectric as shown in Fig. 6.2. The central region is unstable and the ferroelectric spontaneously self-charges to one of the minimas.

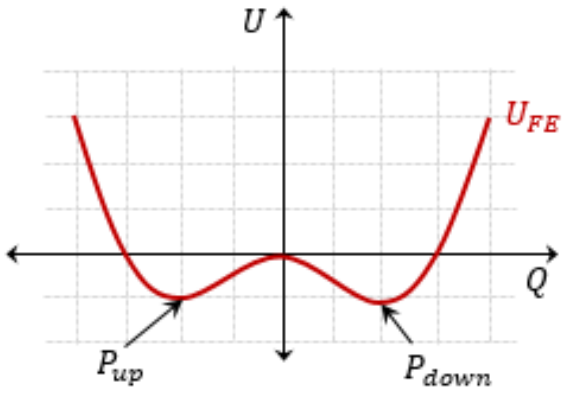

Fig. 6.2. Energy landscape of ferroelectric. The two stable states correspond to two minimas in the energy landscape separated by energy barrier

If the ferroelectric material is sandwiched between the metallic plates to form a ferroelectric capacitor, and no external field is applied, equal and opposite charges induce on the metallic plates thereby canceling any field within the ferroelectric. This ensures that the potential across the standalone ferroelectric capacitor is zero. This is depicted in Fig. 6.3. A ferroelectric is characterized two factors 1) the magnitude of spontaneous polarization, also called remnant polarization, $\pm P_R$ 2) the coercive field, $\pm E_C$, which is the minimum external electric-field required to switch the polarization. This is described in a hysteretic polarization-electric field $(P - E)$ plot of a sample material with $P_R = 3\mu C/cm^2$ and $E_C = 1.4MV/cm$ as shown in Fig. 6.4 below. In forthcoming chapters, we will use this ferroelectric material in a digital-logic and memory application.

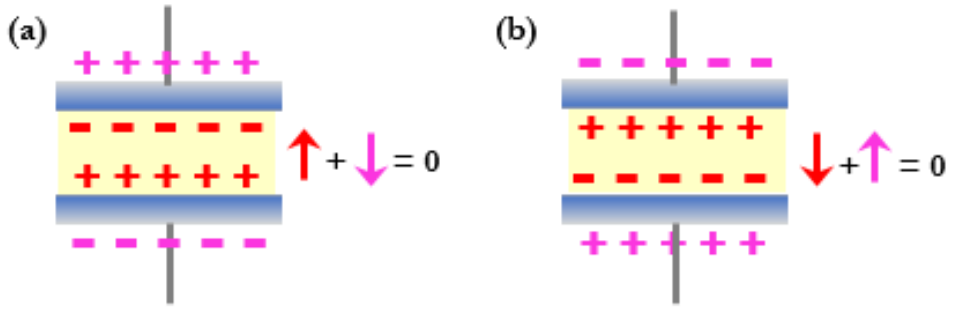

Fig. 6.3. Charge distribution in a standalone ferroelectric capacitor corresponding to (a) Upward polarization (b) Downward polarization, in the absence of applied electric field.

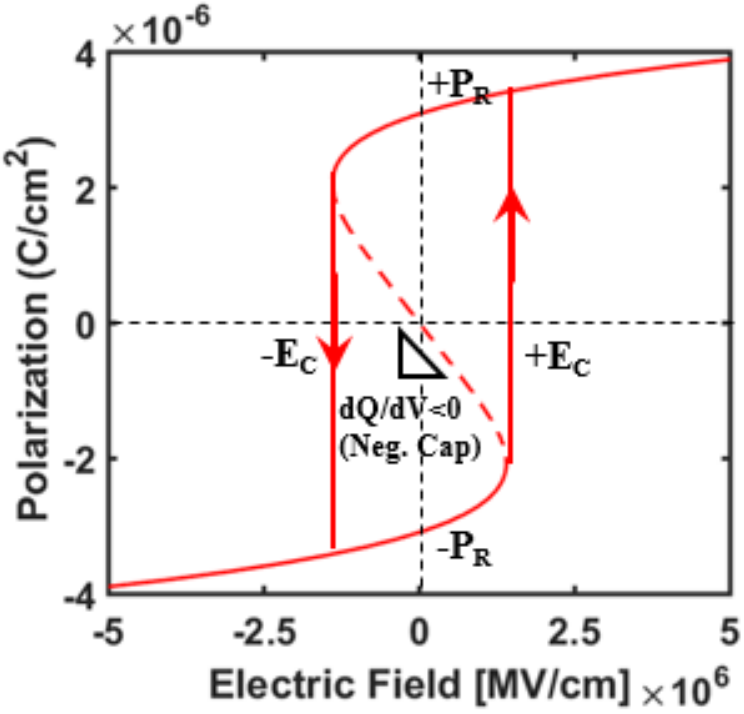

Fig. 6.4. Polarization-Electric field $(P - E)$ curve of a ferroelectric with $P_R = 3\mu C/cm^2$, and $E_C = 1.4MV/cm$

6.2.2 Landau Theory of Ferroelectrics

A thermodynamic free-energy perspective is usually employed to study the charge distribution when several capacitors like dielectric, ferroelectric and semiconductor

are connected in series [75]. Here, we describe two such combinations 1) Ferroelectric on top of a dielectric 2) Ferroelectric on top of a MOSCAP (i.e. ferroelectric+dielectric+semiconductor combination).

The overall free-energy of the system of ferroelectric-dielectric combination, under no external bias, can be written as

$$U_{Total} = U_{DE} + U_{FE} \tag{6.1}$$

where U_{DE} and U_{FE} is the free-energy of the dielectric and ferroelectric respectively. It is well known that, the energy stored in a dielectric capacitor is given by $U_{DE} = \frac{1}{2}CV^2 = \frac{Q^2}{2C}$, where Q is the charge across the dielectric capacitor and C is the capacitance. However, a ferroelectric is a non-linear capacitor and the free energy is described using Landau-Khalatnikov (L-K) theory of ferroelectrics [76]. Assuming the ferroelectric is single-domain, perfectly uniform and free of surface and domain boundary effects, the free-energy is dictated by L-K equation

$$U_{FE} = t_{FE}(\alpha Q^2 + \beta Q^4 + \gamma Q^6) \tag{6.2}$$

where Q is the charge across the ferroelectric capacitor and α, β and γ are the Landau parameters for the ferroelectric. Fig. 6.5 shows the free-energy profiles of an SiO_2 dielectric, $PbZr_xTi_{1-x}O_3$ (PZT) ferroelectric [77] and their combination. Two cases are considered. (a) 500nm PZT capacitor in series with 1nm SiO_2 (b) 2μm PZT capacitor in series with 10nm SiO_2. In the first case (Fig. 6.5(a)), the net energy-charge curve is dominated by dielectric, hence exhibits just one minima at Q=0. Therefore, even though a standalone ferroelectric is unstable at Q=0, the system of dielectric-ferroelectric combination can be stabilized at zero charge. Interestingly, the ferroelectric behaves as a negative capacitor ($dQ/dV_{FE} < 0$) in this region. The negative-capacitance of ferroelectric will later be utilized in a Negative-Capacitance FET (*Chapter 6*) to create internal voltage amplification and thereby lower the sub-threshold swing below Boltzmann limit of 60mV/dec.

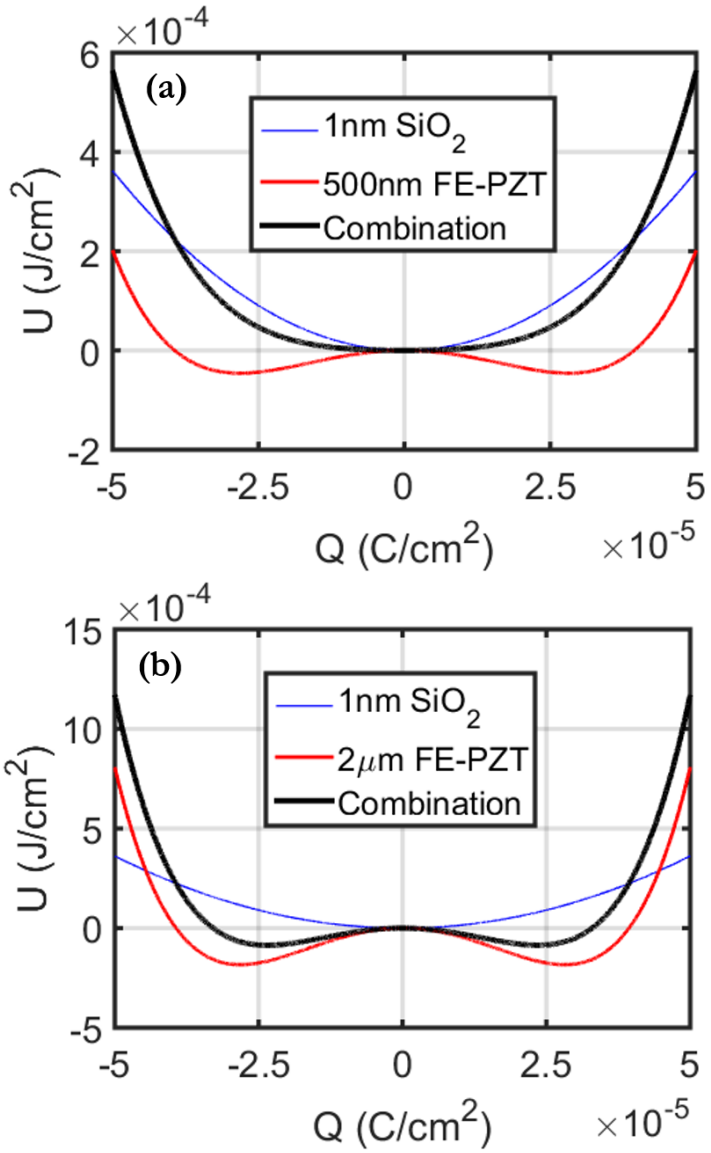

Fig. 6.5. Free-energy profiles of DE, FE and DE-FE combination (a) 500nm PZT capacitor in series with 1nm SiO_2. The system shows a single minima at zero charge. (b) 2μm PZT capacitor in series with 10nm SiO_2. In this case, the system exhibits two stable minimas at non-zero charge.

In the second case (Fig. 6.5(b)), when the ferroelectric thickness is increased, the system can stabilize in two stable polarizations. Also, noteworthy is the fact that the system may stabilize at a different polarization than the ferroelectric's remnant

polarization. The system can be switched from one-state to another via application of external bias. The net energy in Eqn. 6.2 can be expressed as:

$$U_{Total} = U_{DE} + U_{FE} + U_{SOURCE} \tag{6.3}$$

, where $U_{SOURCE} = -Q.V_G$ corresponds to the energy of the source with voltage V_G. Fig. 6.6 illustrates the switching of the system from negative to positive polarization under the effect of positive bias.

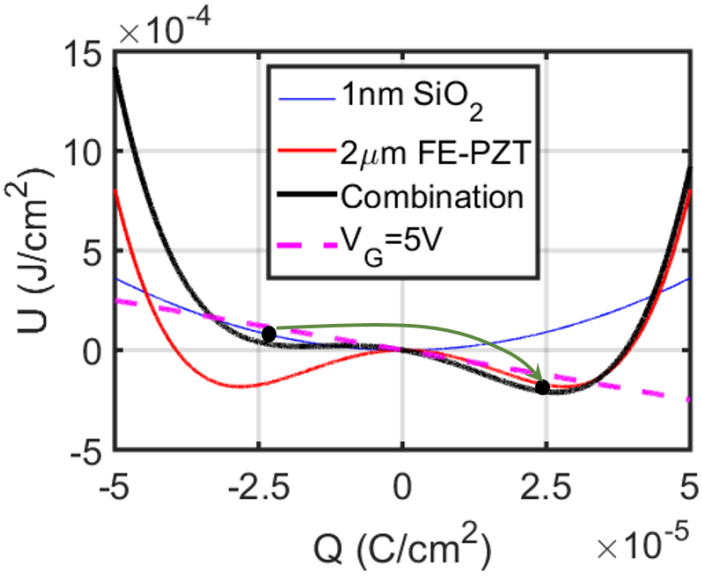

Fig. 6.6. Free-energy profiles of DE, FE and DE-FE combination under external bias. The system can be switched from one state to another by applying an external bias of appropriate magnitude and polarity.

In *Chapter 7*, we will exploit this behavior to design low-voltage 1T non-volatile memory based on Ferroelectric FETs.

6.2.3 Ferroelectricity in doped HfO_2

Classical ferroelectrics like Lead Zirconate Titanate ($PbZr_xTi_{1-x}O_3$) and Barium Titanate ($BaTiO_3$) exhibit large polarization and are incompatible with the CMOS

process. As such, they cannot be directly integrated into the gate-stack of a MOSFET. Recent discovery of ferroelectricity in thin films of doped HfO_2, where some Hf ions were replaced with other metals like silicon, yttrium or zirconium, have attracted particular interest because of their well-established compatibility with conventional silicon fabrication techniques [78–81]. Among them, Hafnium-Zirconium Oxide (HfZrOx) has been shown to retain ferroelectric properties down to physical thicknesses of 1.5nm [81]. Assuming, the ferroelectric is perfectly uniform and ignoring any surface and domain boundary effects, the Landau-Khalatnikov (L-K) theory dictates the voltage across the ferroelectric [76] given by

$$V_{FE} = \frac{dU_{FE}}{dQ} = T_{FE}(2\alpha Q + 4\beta Q^3 + 6\gamma Q^5) \tag{6.4}$$

where Q is the charge per unit area across the ferroelectric, and α, β and γ are Landau parameters for the ferroelectric. It was argued in [75] that Eqn. 6.5 holds only when ferroelectric is in series with a linear capacitor. However, recent investigation has established its validity even for non-linear semiconductor capacitances [82]. The capacitance of the ferroelectric can be calculated by taking inverse of the double derivative of Eqn.6.2:

$$C_{FE} = \left(\frac{d^2U_{FE}}{dQ^2}\right)^{-1} = \frac{1}{T_{FE}(2\alpha + 12\beta Q^2 + 30\gamma Q^4)} \tag{6.5}$$

Fig.6.7 qualitatively explains the relationship between free-energy, U, voltage, V and capacitance, C, both for dielectric and the ferroelectric.

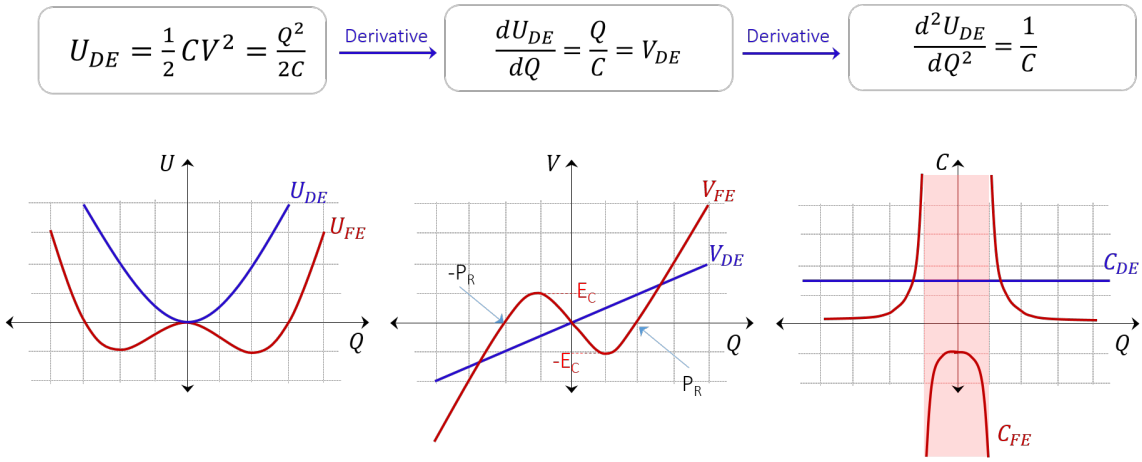

Fig. 6.7. Relationship between self-energy, voltage and capacitance for dielectric (blue) and ferroelectric (red).

6.3 Scalability Analysis of NCFETs

We conducted a survey of published data on FE-HZO which is summarized in Fig. 6.8(a). For effective match between FE-capacitance and the low channel capacitance, a low remnant polarization (P_R) and high coercive field (E_C) is desirable. Hence, the ferroelectric with $P_R = 3\mu C/cm^2$ and $E_C = 1.4MV/cm$, is chosen as reference (Fig. 6.8(a)). α, β and γ are calculated by fitting the ferroelectric $Q - V_{FE}$ characteristics to yield the $P - E$ curve in Fig.6.8(b) and are equal to $-4.2\text{x}10^{11} cmF^{-1}$, $1\text{x}10^{19} cm^5F^{-1}C^{-2}$ and $1.55\text{x}10^{33} cm^9F^{-1}C^{-4}$ respectively. In the following sections, we use this as a reference ferroelectric in the gate-stack of the NCFET.

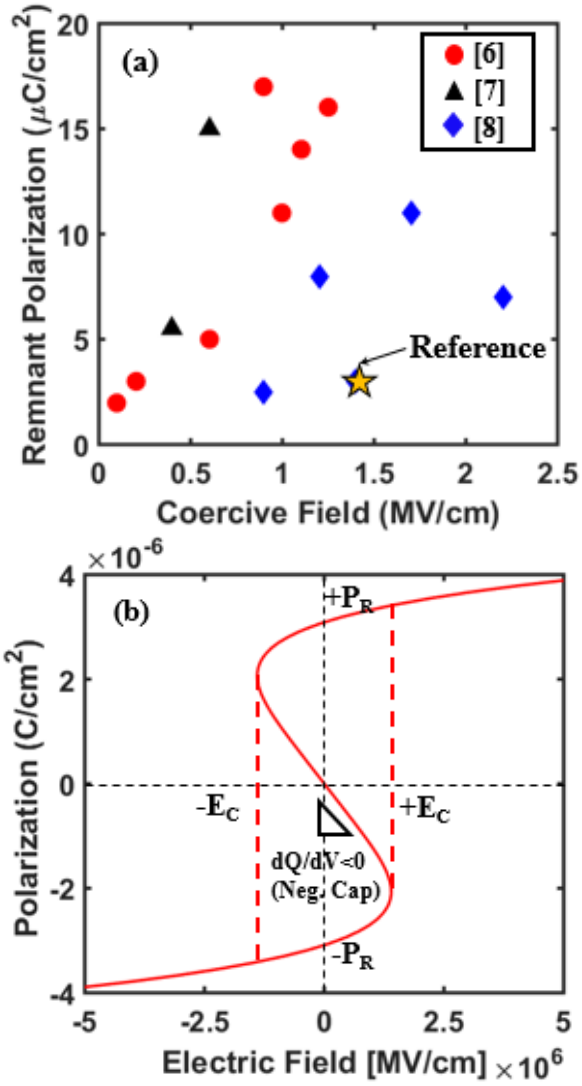

Fig. 6.8. (a) Plot of P_R and E_C of published HZO ferroelectrics. (b) $P-E$ curve of reference ferroelectric with $P_R = 3\mu C/cm^2$, $E_C = 1.4MV/cm$.

6.3.1 Bulk-NCFET

The cross-sectional schematic of bulk-NCFET is shown in Fig. 6.9(a). A bulk planar Si MOSFET with a gate length of 28nm and equivalent oxide thickness (EOT) of 0.7nm is used. Substrate doping is $N_A = 1\text{x}10^{18}cm^{-3}$ and source/drain doping is set to $N_D = 1\text{x}10^{20}cm^{-3}$. The referenced FE-HZO, with $P_R = 3\mu C/cm^{-2}$ and $E_C =$

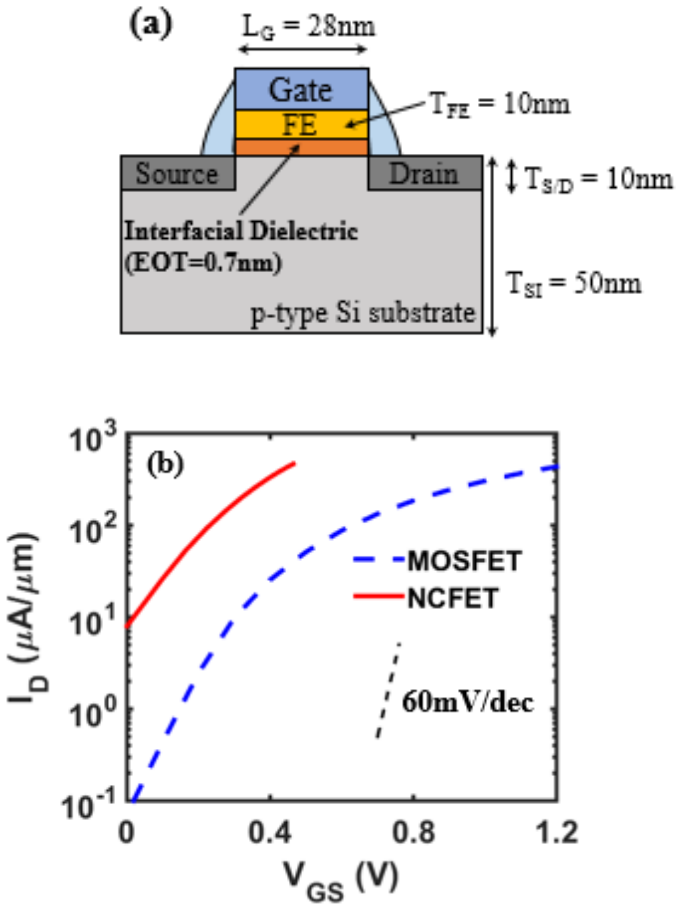

Fig. 6.9. (a) Schematic of bulk-NCFET. (b) $I_D - V_{GS}$ characteristics of underlying MOSFET (dashed) and NCFET (solid).

$1.4MV/cm$, and thickness of 10nm is used. Further, the metal gate-workfunction is adjusted to result in $I_{OFF} = 100nA/\mu m$. The 2-D electrostatics and transfer characteristics of the underlying MOSFET are simulated using TCAD Sentaurus. The NCFET is simulated by self-consistent solution of the charge-voltage characteristics of the ferroelectric obtained from Eqn. 6.5 and of the baseline MOSFET obtained from TCAD.

Fig. 6.9(b) compares $I_D - V_{GS}$ characteristics of bulk-MOSFET and bulk-NCFET. It is interesting to note that NCFET characteristic shows negligible improvement in SS despite the negative capacitance of the ferroelectric. Fig. 6.10(a) tries to justifies this observation. The major contribution to the net channel charge comes from ion-

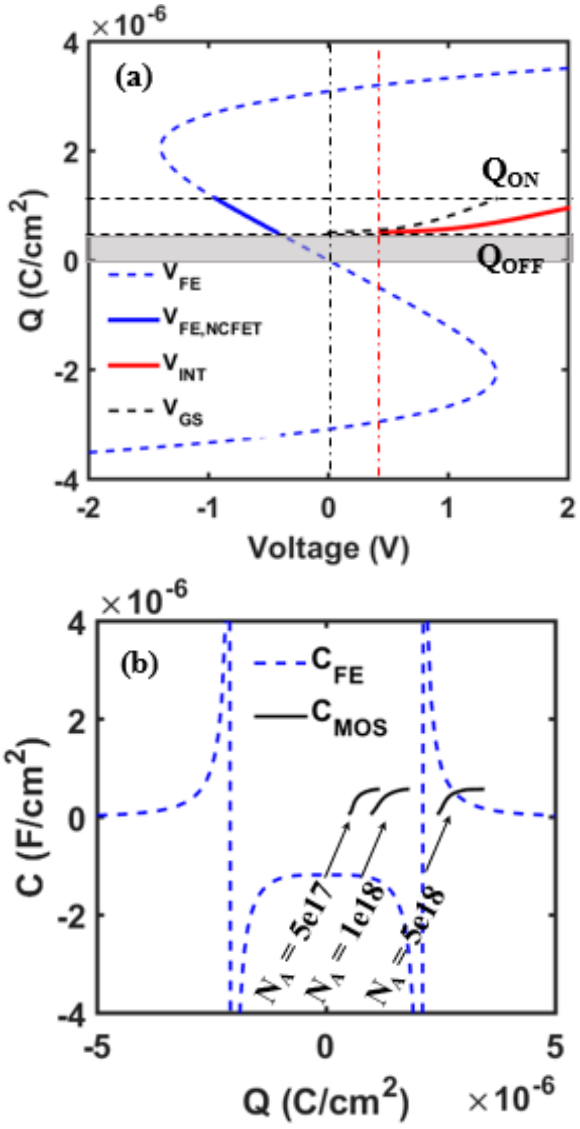

Fig. 6.10. (a) Charge-voltage characteristics of a Bulk-NCFET (b) Capacitance-Charge characteristics for various substrate dopings.

ized dopants in the OFF state. Hence, the shaded-charge region is never accessible. This leads to internal voltage, V_{INT}, being the shifted version of applied V_{GS} without significant amplification. Fig. 6.10(b) further shows that higher substrate doping aggravates the capacitance mis-match by translating the net channel charge modulation from OFF-to-ON state to higher charge values. To solve this problem, we investigate undoped channel FETs in the next sections.

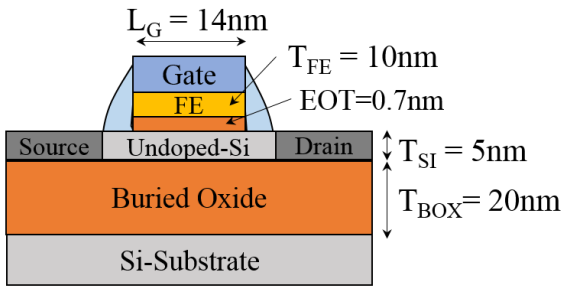

Fig. 6.11. Schematic of 14nm gate-length FDSOI-NCFET.

6.3.2 FDSOI-NCFET

Ultra-thin body fully-depleted silicon-on-insulator (UTB-FDSOI) MOSFETs have been successfully used in the high-performance world to drastically cut power consumption by minimizing short-channel effects, down to 20nm nodes and beyond [83]. Fig. 6.11 shows cross-sectional schematic of 14nm gate-length FDSOI FET with intrinsic channel having $T_{SI} = 5nm$. A S/D underlap of 2nm is utilized to minimize the fringe capacitance arising due to coupling between intermediate metallic film (at dielectric-ferroelectric interface) and S/D regions [84]. Simulation methodology is the same as described in previous section.

Fig. 6.12(a) compares the transfer characteristics of FDSOI-NCFET with an FDSOI MOSFET having the same geometry without FE-HZO. A significant improvement in SS is observed for $T_{FE} = 10nm$. Fig. 6.12(b) justifies this observation. Due to undoped body, the entire channel charge is contributed by inversion charge. The internal voltage, V_{INT}, is an amplified version of applied V_{GS}, which leads to improved SS. In the next section, we explore the viability of sub-10nm NC-FinFETs.

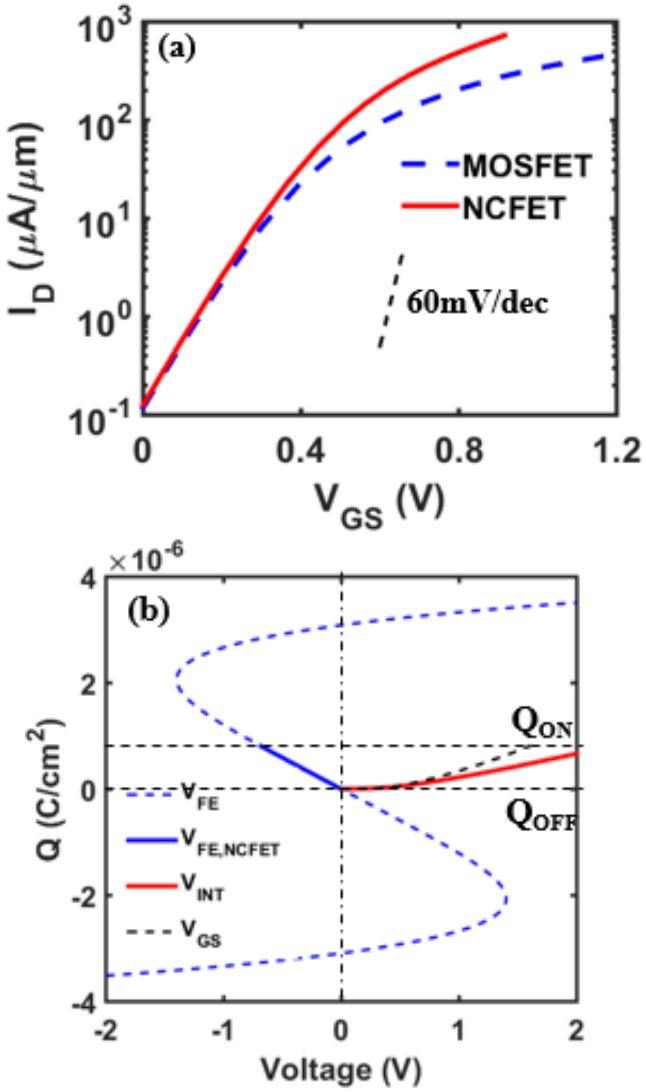

Fig. 6.12. (a) $I_D - V_{GS}$ characteristics of underlying FDSOI-FET (dashed) and FDSOI-NCFET (solid). (b) Charge-voltage characteristics of an FDSOI-NCFET.

6.3.3 Sub-10nm NC-FinFET

Excellent control over short-channel effects at sub-10nm nodes have made FinFETs a premier choice for area-constrained and low-power circuits [85]. Fig. 6.13(b) shows the schematic of intrinsic-channel silicon FinFET with drawn gate length of 9nm and S/D underlap of 1nm. The fin-thickness is 3nm and the EOT is equal to

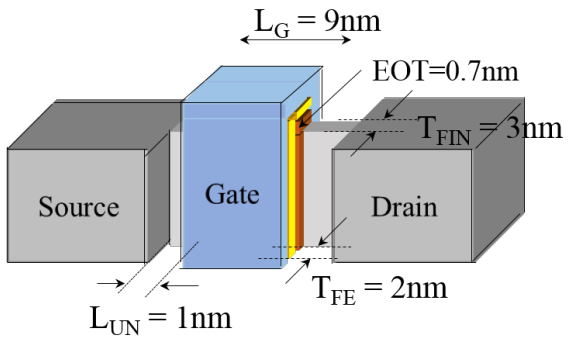

Fig. 6.13. Schematic of 9nm gate-length NC-FinFET

0.7nm. The scaled fin-pitch may not provide enough space to place thick ferroelectric, hence we restrict our analysis to $T_{FE} \leq 3nm$. Note that the absence of buried oxide capacitance in the FinFET structure, compared to FDSOI structure, increases the net gate-capacitance. This permits ferroelectric thickness downscaling, thereby increasing the magnitude of ferroelectric capacitance and further enabling easier matching with the underlying FinFET's capacitance. The source/drain doping is set to $1x10^{20} cm^{-3}$. A physics-based device simulation of double-gate FinFETs is necessary at sub-10-nm scale to capture quantum mechanical effects that manifest at such scales. To simulate FinFET, we use quantum physics-based NEMO5 simulator [9]. The device simulation involves self-consistently solving the ballistic 2-D nonequilibrium Greens function equations of transport in the Si fin by using an atomistic $sp^3d^5s^*$ tight-binding basis together with the 2-D Poisson equation for electrostatics in the fin cross-section. The NC-FinFET is then simulated by self-consistent solution of charge-voltage characteristics of ferroelectric (Eqn. 6.5) and that of FinFET.

Fig. 6.14(a) shows the transfer characteristics of the described baseline FinFET and NC-FinFET for T_{FE} of 2nm and 3nm. A low voltage NC-FinFET operating down to 0.25V is predicted using ultra-thin 3nm FE-HZO. Fig. 6.14 further shows the charge-voltage characteristics of NC-FinFET. Due to improved gate-control, a larger range of charge is swept from OFF-to-ON state over a lower gate-voltage swing. The resultant enhancement in channel capacitance of a FinFET thereby permits the down-

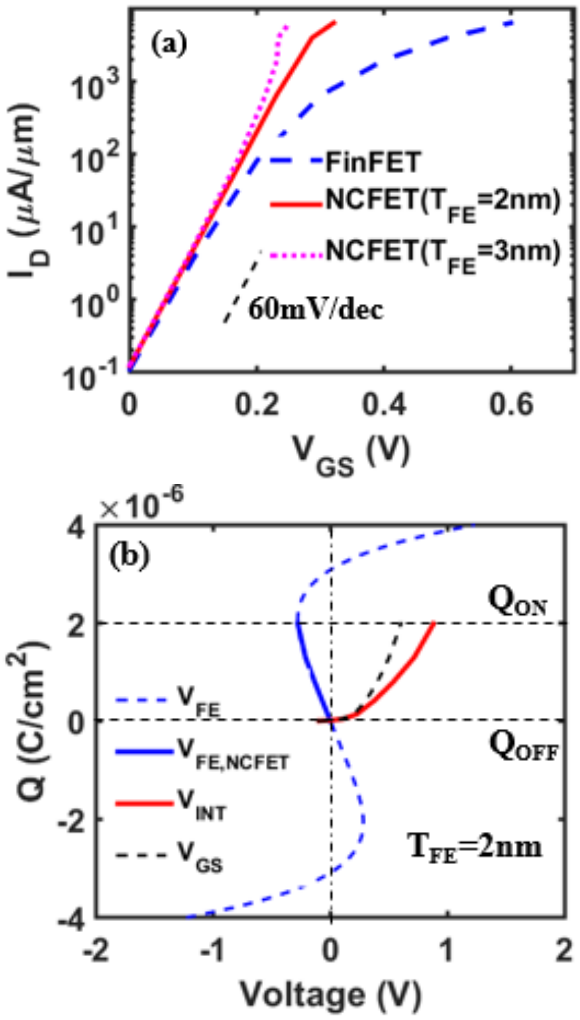

Fig. 6.14. (a) $I_D - V_{GS}$ characteristics of underlying FinFET (dashed) and FDSOI-NCFET for $T_{FE} = 2nm$ and $T_{FE} = 3nm$. (b) Charge-voltage characteristics of NC-FinFET for $T_{FE} = 2nm$.

scaling of ferroelectric thickness to below 3nm compared to 10nm in FDSOI-NCFETs discussed in previous section. To further explore scalability of NC-FinFETs, we consider ultra-scaled 5nm gate-length NC-FinFET with $T_{FE} = 1.5nm$ and compare it against a 5nm gate-length baseline FinFET. The transfer and output characteristics are shown in Fig. 6.15. The transfer characteristics of NC-FinFET follow nearly exponential trend entirely from off-to-on state which is in stark contrast to baseline FinFET, whereby current increases linearly w.r.t gate-voltage in super-threshold re-

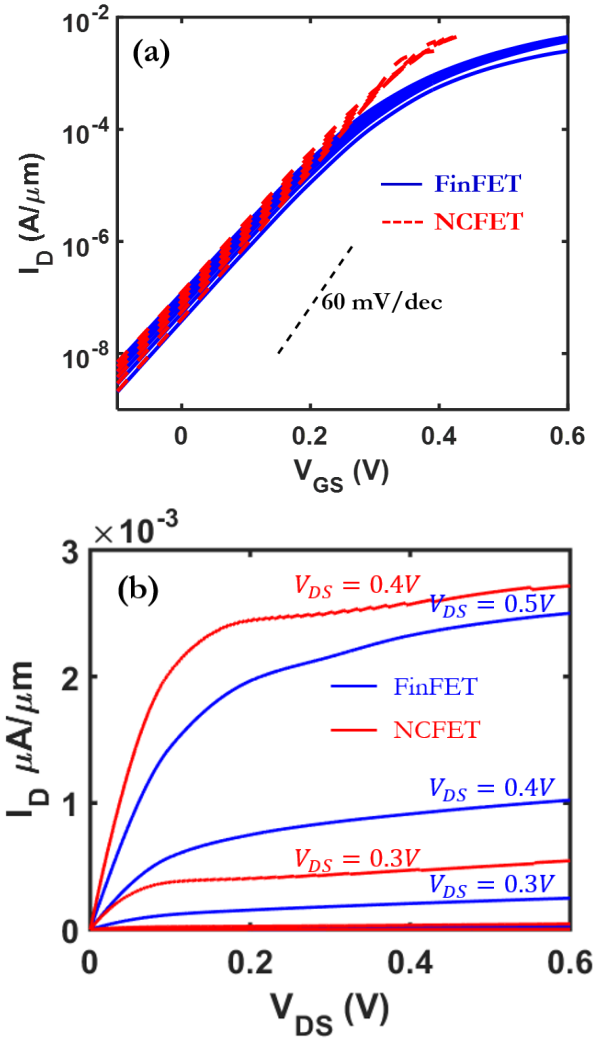

Fig. 6.15. Comparison of (a) $I_D - V_{GS}$ characteristics for various V_{DS} (b) $I_D - V_{DS}$ characteristics for various V_{GS}, of 5nm gate-length NC-FinFET and baseline FinFET.

gion. This exponential behavior manifests as enhanced drive current in NCFETs for the same gate-voltage. The output characteristics in Fig. 6.15(a) elucidates this proposition further. At low-gate bias, the $I_D - V_{DS}$ characteristics nearly overlap, however the separation between the curves for various V_{GS} increases dramatically for NC-FinFET, compared to near-linear dependence in baseline FinFET. In the following sections, we utilize this property of NCFETs and show how superior drive-current

can greatly minimize delay in circuits, specially at super-threshold supply voltages of operation.

Another important observation from Fig. 6.15 is the reduced Drain Induced Barrier Lowering (DIBL) in NCFETs. This is a result of an opposing effect known as Drain Induced Barrier Raising (DIBR). An increase in drain bias depletes the channel of carriers, which in turn reduces the charge across the ferroelectric. This leads to a lower negative voltage across the ferroelectric, thereby lowering the potential at the internal gate. This corresponds to a commensurate reduction in surface potential, effectively raising the barrier between the source to channel, thereby lowering the impact of DIBL. The analysis of DIBR in NCFETs has been pursued in detail by Seo. et. al [86].

6.4 Capacitance-Voltage Characteristics

Device capacitances play a critical role in determining circuit performance together with the drive current. The capacitance versus voltage characteristics of a 5nm FinFET and 5nm NC-FinFET with $T_{FE} = 1.5nm$, is shown in Fig. 6.16 for low and high drain bias. In the OFF state ($V_{GS} \approx 0V$), the gate-capacitance is low, due to negligible channel capacitance. However, the channel capacitance, hence the gate-capacitance, increases once the channel undergoes inversion. At low drain bias, the gate-capacitance is equally contributed by gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}), however, the contribution of the latter diminishes at high drain bias due to wider depletion at the source-drain junction. The gate-capacitance for NC-FinFET (red curves) is greater than that of baseline FinFET, across gate-voltage range where the ferroelectric capacitance is negative. This is more clearly shown in Fig. 6.17, whereby a cross-over in gate-capacitance and underlying MOSFETs capacitance is observed when the ferroelectric transitions from negative to positive capacitance regime. Also, noteworthy is the observation that en-

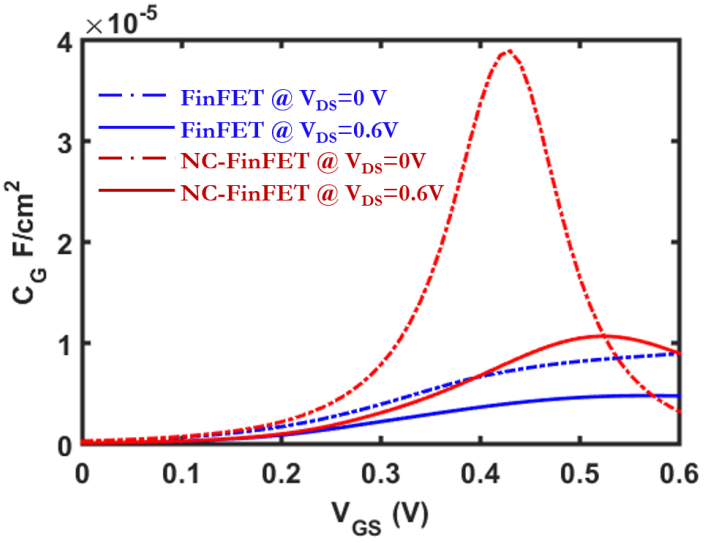

Fig. 6.16. Comparison of capacitance-voltage characteristics of FinFET and NCFET at low and high drain bias.

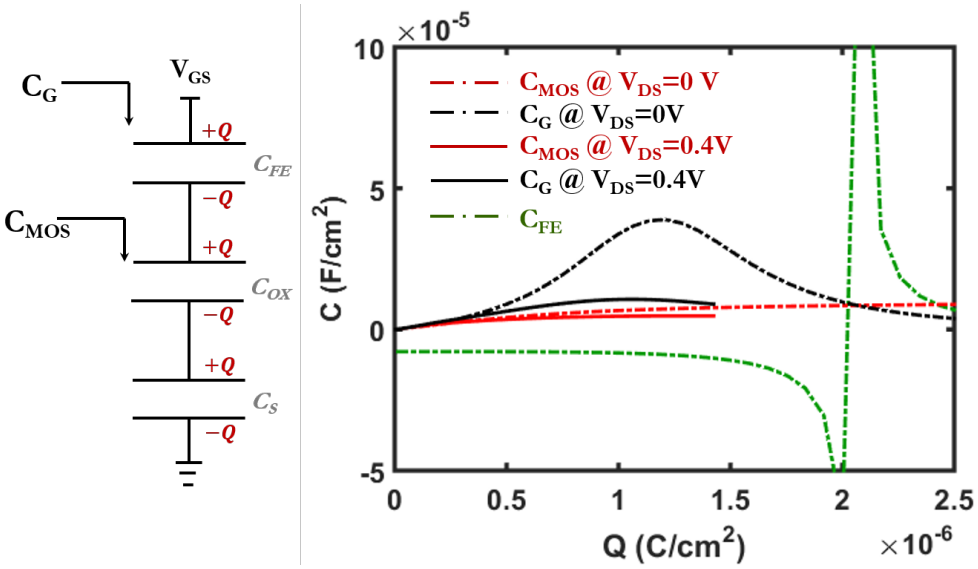

Fig. 6.17. Capacitance versus charge characteristics of NCFET at low and high drain bias.

hancement in gate-capacitance reduces at higher-drain bias due to poorer matching with the ferroelectric capacitance.

6.5 Circuit Evaluation - Inverter Chain

In this section, we evaluate circuit-level metrics of 5nm NC-FinFETs discussed in previous section. We develop look-up table based device models to perform SPICE-level simulations. For p-type NC-FinFET and baseline FinFETs, we assume $I_D - V_{GS}$ and $C - V$ characteristics symmetrical to n-type counterparts. A comparison of the simulated voltage-transfer characteristics of the inverter constituting n/p NC-FinFETs and n/p baseline FinFETs is shown in Fig. 6.18 for various supply voltages. The NC-FinFET based inverter shows increasingly steeper output transitions at higher supply voltages. This is a direct consequence of much higher drive currents in NCFETs compared to baseline MOSFETs, specially in superthreshold region. At subthreshold voltages, the improvement in SS is minuscule, which results in overlapping transfer characteristics.

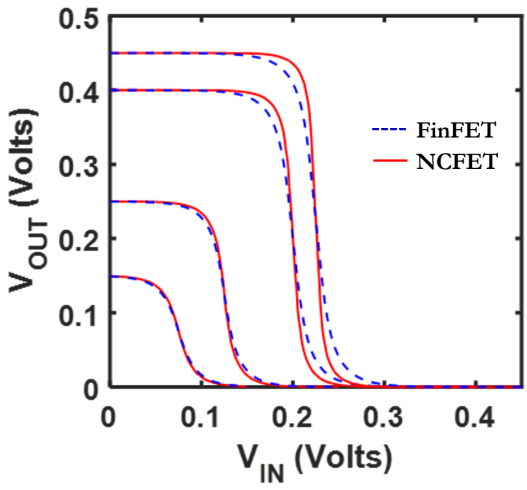

Fig. 6.18. (a) Comparison of voltage-transfer characteristics of NCFET based inverters and baseline MOSFET based inverters for various supply voltages.

To investigate performance and energy metrics, we implement a NC-FinFET (with $T_{FE} = 1.5nm$) based 6-stage inverter chain and compare with an inverter chain implemented entirely using similar sized FinFETs. As shown in Fig. 6.19(a), NC-FinFETs

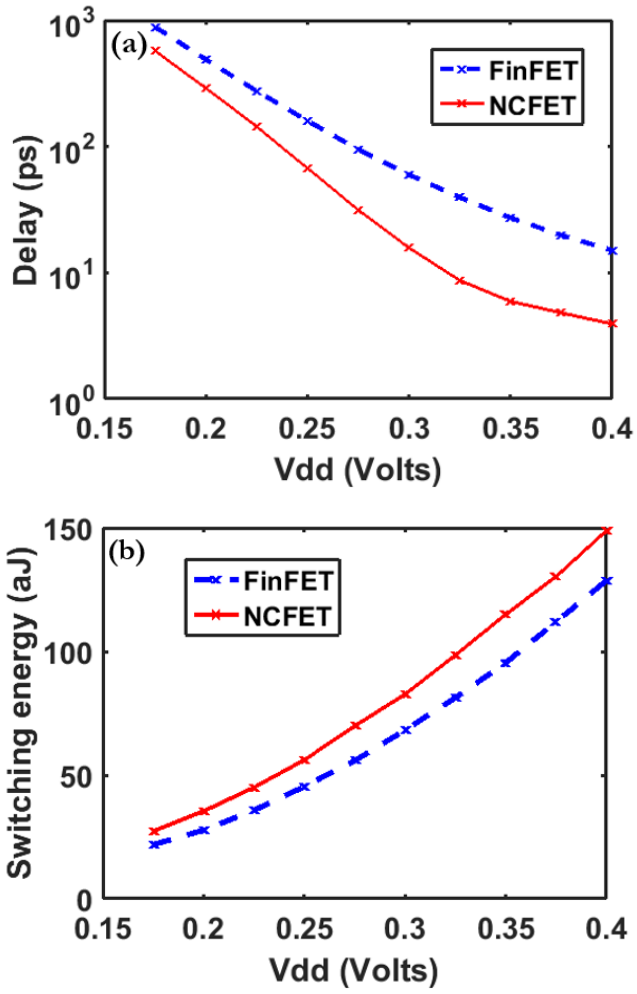

Fig. 6.19. (a) Delay v/s supply voltage (b) Switching energy v/s supply voltage for 6-stage inverter chain implemented using FinFETs (dashed line) and NCFETs (solid line).

based inverters exhibit superior performance compared to FinFET counterpart primarily because of much higher on-currents specially at super-threshold voltages. Even though NCFETs exhibit higher gate-capacitance than MOSFET counterparts, the exponential dependence of drain current in superthreshold region causes steeper transitions in intermediate nodes and manifests as much lower propagation delay. Interestingly, the switching energy consumption remains comparable across various supply voltages. This follows from the observation that NCFETs support faster transitions,

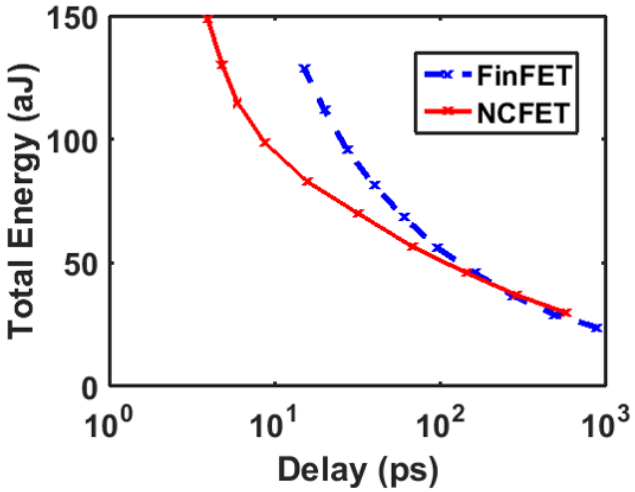

Fig. 6.20. Total energy v/s delay for 6-stage inverter chain implemented using FinFETs (dashed line) and NCFETs (solid line).

however sink a larger current during the transition, thereby consuming similar energy compared to FinFETs. Both the above inferences are more clearly exemplified in Fig. 6.20 where total energy is plotted vs. delay. At same energy, the NCFETs can potentially show much lower delays compared to MOSFETs, hence are more suitable for future high-performance applications.

6.6 Conclusion

To conclude, we have performed a detailed simulation analysis to investigate the design-space of HfZrOx-based NCFETs. Planar bulk-NCFETs are shown to complicate the capacitance matching with the FE-HZO due to channel charge contribution coming predominantly from ionized dopants. Sub-20nm FDSOI-NCFETs exhibit improved NCFET performance, with major benefits coming from its undoped body. Finally, a sub-10nm NC-FinFET analysis reveals that the improved gate-control permits downscaling of supply voltage to 0.25V while employing ultra-thin 3nm FE-HZO films. Furthermore, to examine their potential for logic applications, a VERILOG-A based look-up table model was developed for circuit evaluation. SPICE simulations

of 6-stage inverter chain suggest that NCFETs are particularly well suited for super-threshold high-performance applications due to their larger drive currents compared to MOSFETs.

7. FERROELECTRIC FET BASED 1T NON-VOLATILE MEMORY

7.1 Introduction to Ferroelectric FETs

Ferroelectric FETs (FeFETs), consisting of ferroelectric in the gate-stack of conventional MOSFET, have attracted considerable attention for future ultra low-power non-volatile memory applications [87–89]. They show excellent features such as non-volatility, better scalability and energy-efficient switching with non-destructive read-out. Furthermore, their high distinguishability between two states compared to spin-based memories [90], and high endurance compared to resistive RAMs [91], phase change memories [92] and flash memories make them outstanding candidates for future non-volatile memory applications.

Traditionally, ferroelectrics like PZT and BTO have been used in ferroelectric capacitor memories (FeRAMs) [93]. However, their incompatibility with semiconductor technology, poor scalability and destructive read operation has posed serious limitation compared to several competing memories [94]. Recent discovery of ferroelectricity in hafnium-oxide [78–81] has overcome shortcomings of FeRAMs and revived interest in scalable ferroelectric-gate type memories. Fast progress has been made in this segment whereby FeFETs with fast switching ($\sim 10ns$), retention of ~ 10 years [95] and endurance of $\sim 10^9$ [95] cycles have been demonstrated.

Previously, George et. al. [96] reported 2T FeFET memory with low read/write energy and superior characteristics compared to 1T FeRAMs, albeit a slight area penalty due to 2T design. The design, reproduced in Fig. 7.1(a), consists of a FeFET and a conventional MOSFET as an access transistor. In this letter, we propose 1T Fe-NOR memory by getting rid of the access transistor. This is made possible by dynamically modulating the memory window (MW) of FeFETs. We utilize ultra-

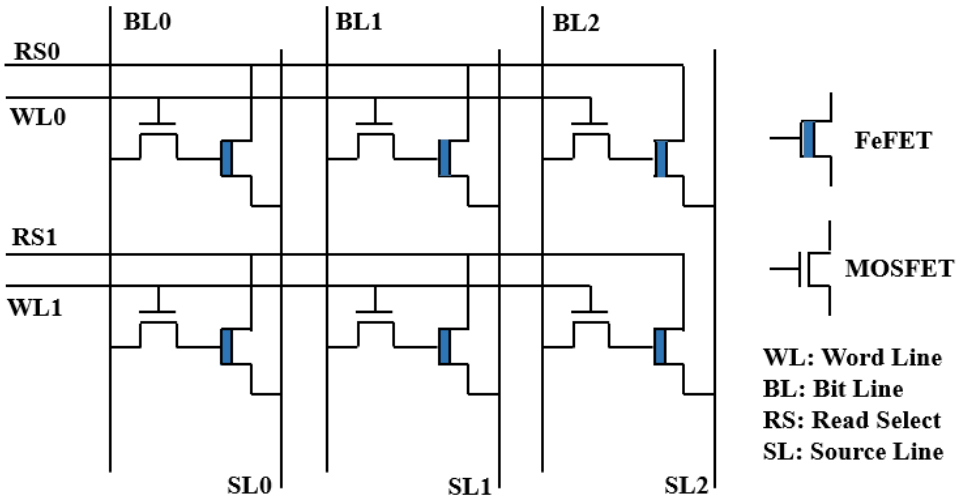

Fig. 7.1. A 2x3 FeFET memory array with 2T per cell [96].

scaled 5nm gate-length FinFET to design FeFET as a memory element which achieves sub-1V write/erase voltages whilst greatly simplifying the program/read operations compared to existing Fe-NAND realizations [97].

The rest of the paper is organized as follows. Section II lays the background about origin of hysteresis in FeFETs. In Section III, we propose 5nm gate-length FeFET as a 1T memory element, describe the device simulation methodology and explain the operating principle. In Section IV, we utilize the proposed FeFET in a prototype 3x3 FeFET array and describe the voltage conditions for program, erase and read operations. The impact of gate-length and ferroelectric material variations is discussed in Section V. Finally, we summarize our findings in Section VI.

7.2 Background - Hysteresis in FeFETs

In the past, several works have focused on the design of hysteresis-free negative capacitance FETs (NCFETs) for low-power logic applications. In the previous section, it was shown that the FinFET configuration greatly benefits the NCFET performance due to their undoped body and improved great control, which enables better capacitance matching with the ferroelectric [98]. A hysteresis-free NC-FinFET operating

down to 0.25V was predicted using 3nm FE-HZO. A higher ferroelectric thickness induces hysteresis in the transfer characteristics due to presence of two valleys in the net-free energy-charge curve of the system. This can be explained by writing the total free-energy of the system, U_{TOTAL} as:

$$U_{TOTAL} = U_{FE} + U_{MOS} + U_{SUPPLY} \tag{7.1}$$

where U_{FE}, U_{MOS} and U_{SUPPLY} are the free energies of the ferroelectric, the underlying MOSFET (dielectric and semiconductor channel) and the external supply, respectively. Fig. 7.2(a) plots these individual components w.r.t charge for an arbitrary ferroelectric-MOSFET combination designed in the hysteretic regime, assuming the supply is grounded (i.e. $U_{SUPPLY} = -Q.V_{DD} = 0$). The net free energy of the system exhibits two stable minimas, labeled as A and B, separated by an unstable negative capacitance region $\left(\frac{\partial^2 U_{TOTAL}}{\partial Q^2}\right)^{-1} < 0$. Fig. 2(b) shows the band-diagram from gate-to-substrate in both cases of stable polarization. A -ve ferroelectric polarization piles up holes in the channel leading to extremely low OFF-current through the transistor. On the other hand, a +ve polarization of the ferroelectric leads to strong inversion in the channel which represents the ON-state of the transistor. The polarization state can be switched from A to B and vice-versa via application of appropriate positive and negative gate-voltage respectively. The wide difference between the sense currents corresponding to the two polarization states greatly simplifies the read operation leading to simple sense and control circuitry. In the following sections, we introduce 5nm gate-length FeFETs and describe their operation in a 1T memory array.

7.3 FeFET Design And Simulation Methodology

Fig. 7.3(a) shows the schematic of intrinsic-channel silicon FeFET with drawn gate length of 5nm and fin-thickness of 3nm. An interfacial dielectric (SiO_x) thickness of 0.7nm is assumed while 9nm HfZrOx ferroelectric (FE-HZO), with $P_R = 3\mu C/cm^{-2}$ and $E_C = 1.4MV/cm$, is used [98]. The source/drain doping is set to $1x10^{20}cm^{-3}$.

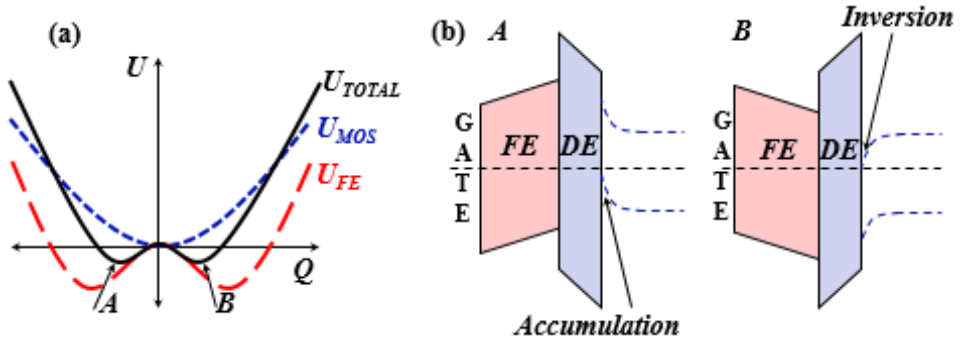

Fig. 7.2. (a) U_{FE}, U_{MOS} and U_{TOTAL} vs. charge relationship, when $U_{SUPPLY} = 0$. The total energy of the system shows two minima, i.e. two stable polarization states A and B (b) Band-diagram from gate to channel for polarization states A and B.

A physics-based device simulation is necessary at sub-10nm scale to capture quantum mechanical effects that manifest at such scales. To simulate the underlying FinFET in the FeFET structure, we use quantum physics-based NEMO5 simulator [9]. The device simulation involves self-consistently solving the ballistic 2-D nonequilibrium Greens function equations of transport in the Si fin by using an atomistic $sp^3d^5s^*$ tight-binding basis together with the 2-D Poisson equation for electrostatics in the fin cross-section. The energy stored in the FinFET, U_{MOS}, is obtained by $\int_0^Q V_{gs}dQ$, where V_{gs} is the internal voltage at ferroelectric-dielectric interface (see inset in Fig.7.3(b)). U_{FE} is dictated by L-K theory of ferroelectrics [76] and is given by, $U_{FE} = \alpha Q^2 + \beta Q^4 + \gamma Q^6$, where α, β, and γ are the Landau parameters for the ferroelectric [98]. Eqn.7.1 is then used to calculate net-free energy of the FeFET. The charge corresponding to the energy minimas gives the current through the FeFET at a given external gate-bias, V_{GS}.

Fig. 7.3(b) compares $Q - V_{gs}$ characteristics of the underlying FinFET structure for low and high drain-bias. A high drain-bias of 1V depletes the channel of free carriers, thereby significantly lowering the net charge available in the channel. Hence, for a given amount of channel charge, a higher gate bias needs to be applied when the drain bias is high. As a result, a higher energy is stored in the underlying FinFET

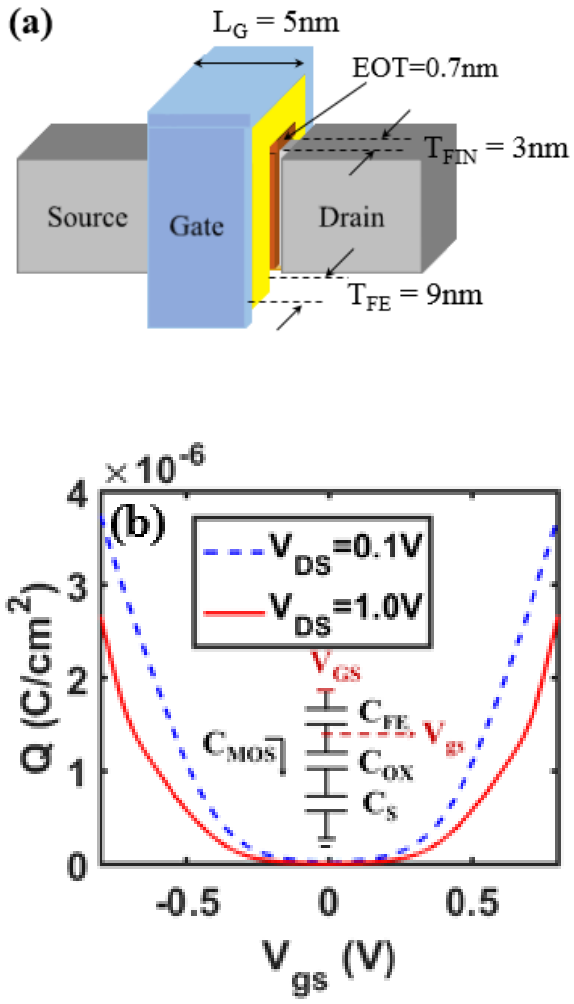

Fig. 7.3. (a) Schematic of 5nm FeFET (b) Charge-internal voltage (V_{gs}) characteristics of FinFET for low and high drain bias. An equivalent capacitance network of FeFET shown in the inset highlights the nomenclature of node voltages in the FeFET.

as shown in Fig.7.4(a). Fig.7.4(b) shows the net energy of the FeFET (U_{TOTAL}), at different bias conditions. At a lower drain bias, the net energy of the system is lower, hence a higher gate-voltage is needed to switch the polarization from A to B. In the structure described above, it is observed that $|V_{GS}|$ of 0.2V is needed to switch the polarization when $V_{DS} = 1.0V$, while a higher $|V_{GS}| = 0.3V$ is required to switch the polarization when $V_{DS} = 0.1V$. It is worthwhile noting that the dynamic control of the switching voltage, via drain bias, is facilitated by enhanced drain-channel coupling

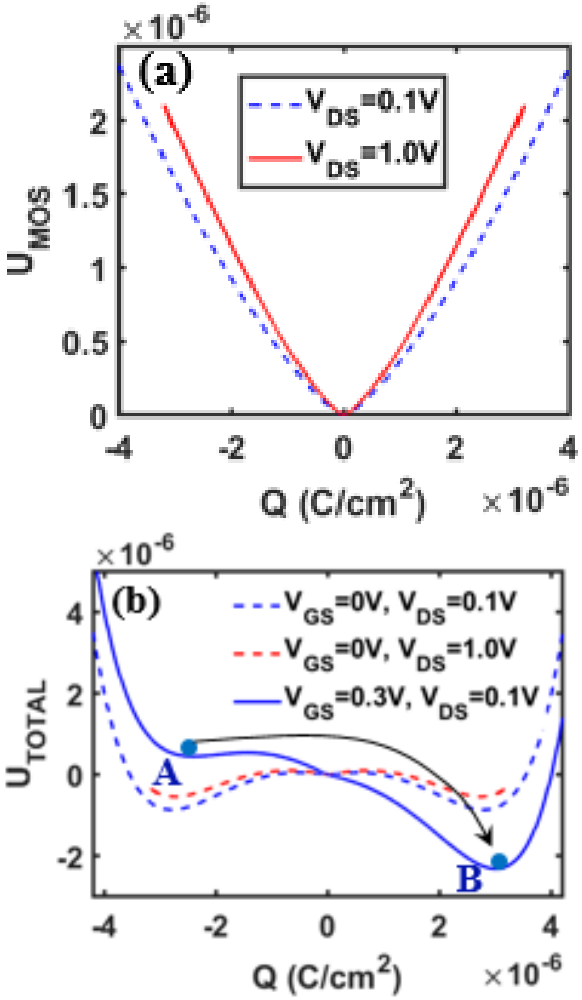

Fig. 7.4. (a) U_{MOS} vs charge for low and high drain bias (b) U_{TOTAL} vs charge for low and high drain bias at $V_{GS} = 0V$ (dashed curves). Also, shown is the curve for state transition from A to B (attained at $V_{GS} = 0.3V$), for low drain bias.

due to ultra-short gate-length. Higher gate-lengths would lead to convergence of the switching voltages w.r.t drain bias and render 1T memory design difficult, as described later in Section V.

Fig. 7.5 compares the transfer characteristics for the FeFET at two different drain bias. A higher drain bias results in a narrower memory window (MW), defined as the difference between the threshold voltages for the two different polarization values, thereby making switching feasible at a lower V_{GS}. We utilize this property to design

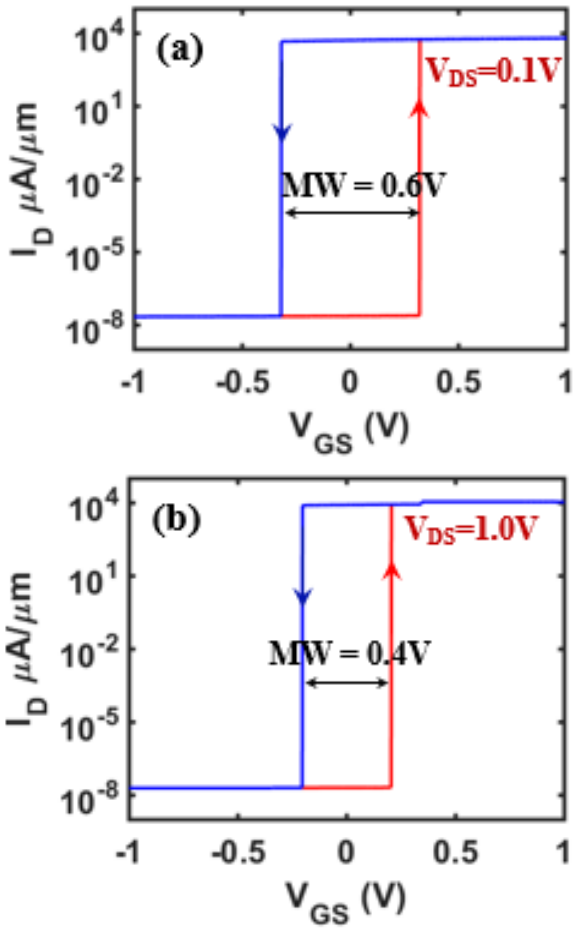

Fig. 7.5. (a) $I_D - V_{GS}$ characteristics of FeFET at $V_{DS} = 0.1V$ (b) $I_D - V_{GS}$ characteristics of FeFET at $V_{DS} = 1V$

a 1T FeFET based memory array in the NOR configuration, as described in the following section.

7.4 1T FeFET Memory

We consider a prototype 3x3 NOR-type array consisting of proposed FeFETs to illustrate Program, Erase and Read operations. Fig. 7.6(a) shows the voltage conditions for writing into the central column of the array. The bitline for the column to be programmed is set to high V_{DS}, which lowers the threshold voltage to write to

the FeFETs, as described in the previous section. The wordlines are subsequently set to +ve or -ve voltages satisfying $0.2V < |V_{GS}| < 0.3V$ to erase ($V_T < 0V$) or program ($V_T > 0V$) the cells respectively while the unselected columns are inhibited by setting their bitlines to ground. To estimate the write pulse-width requirements, a careful experimental measurement is necessary to account for capacitances and switching-time of the ferroelectric, which cannot be accurately deduced from the simulations due to abrupt switching behavior.

For reading the contents of the memory array, the bitlines are precharged to a voltage, $V_{READ} < 0.2V$, while the wordlines are set to 0V. The source line of the selected row is set to ground as shown in Fig. 7.6(b). This results in a $V_{GS} = 0V$ across the selected cells. The erased cells ($V_T < 0V$), with much higher drive current compared to programmed cells ($V_T > 0$), consequently discharge the bitlines which can be easily read through the sense amplifier. On the other hand, the unselected rows are inhibited by floating their source lines. If any of the cells in an unselected row is conductive (i.e. $V_T < 0$), it will charge the corresponding source line to V_{READ}. Any read-disturb on the unselected cells is averted by ensuring $V_{READ} < 0.2V$ (i.e. lower of the two threshold voltages, $V_{TH,MIN}$, of the FeFETs). This would keep $|V_{GS}| < 0.2V$ for the unselected cells and prevent their unwanted switching. Similarly, if all the unselected cells were non-conductive ($V_T > 0$), and if the floating source line rises beyond 0.2V, the bitline acts as a source, hence $|V_{GS}| < 0.2$ still holds true, which prevents accidental switching of the unselected FeFET cells.

7.5 Variation Analysis

In this section, we study the sensitivity of the switching characteristics of FeFETs to the variations in gate-length and ferroelectric material properties. Fig. 7.7(a) shows the variation of 0→1 switching threshold w.r.t gate-length at low and high drain bias. As expected, the drain control over the channel charge reduces at longer gate-lengths, thereby leaving a narrower margin to perform disturb-free write operation.

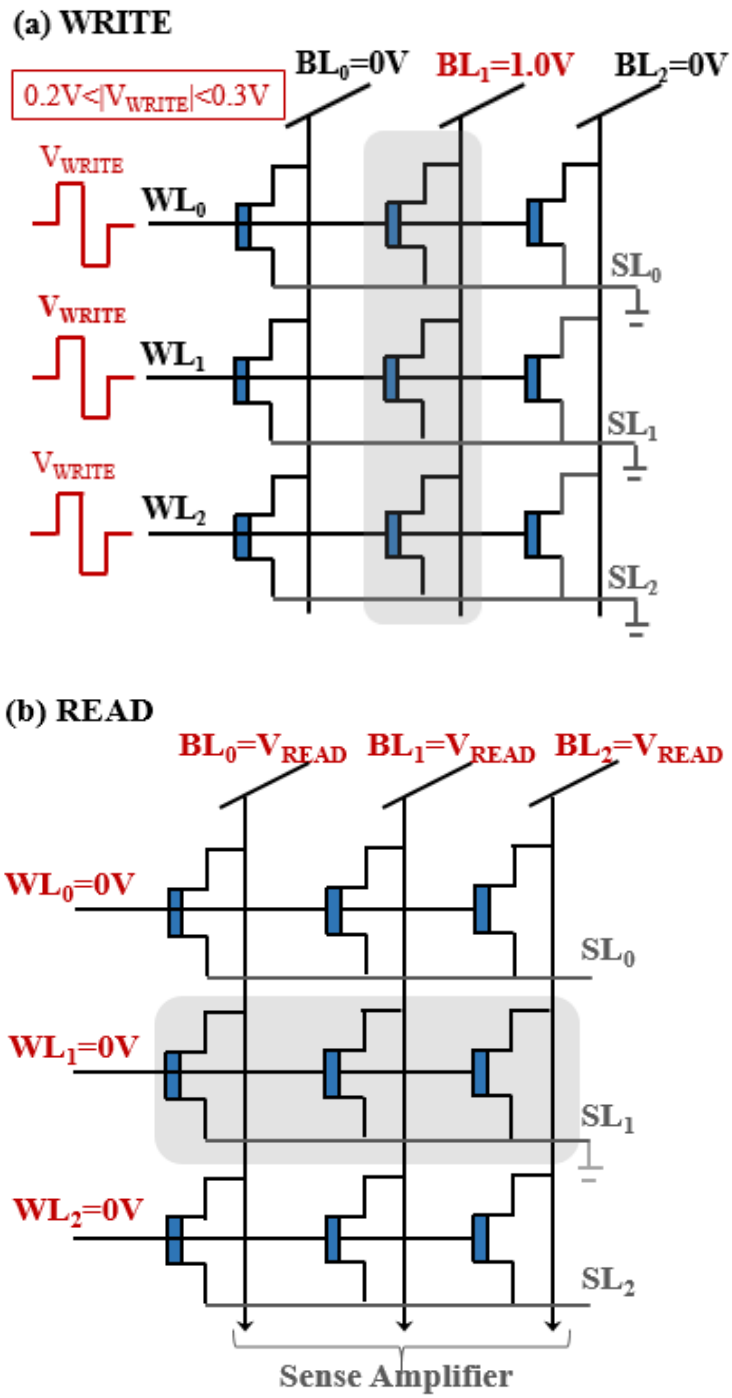

Fig. 7.6. (a) Voltage conditions for write operation on the central column (b) Voltage conditions for read operation on the central row.

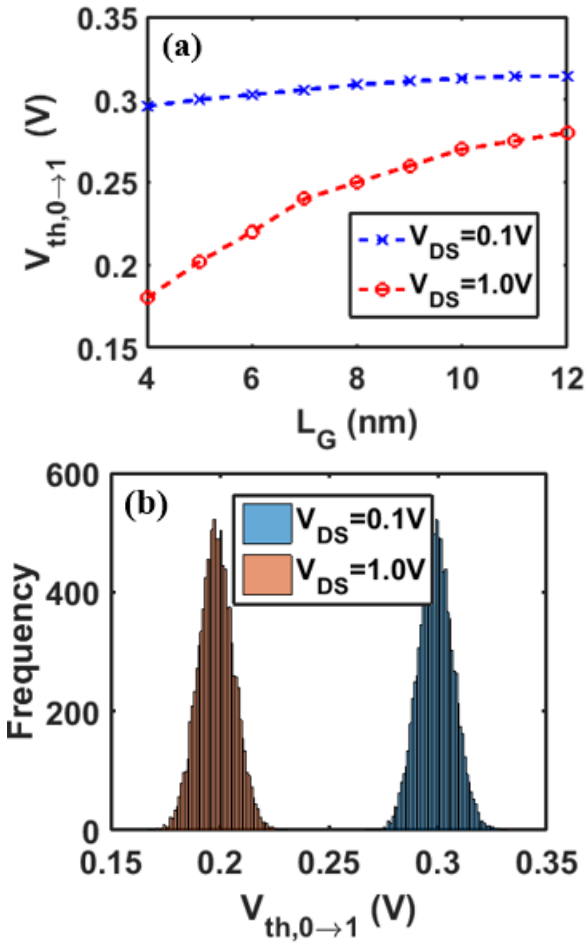

Fig. 7.7. (a) Variation of $0 \rightarrow 1$ switching threshold vs. gate-length for low and high-drain bias (b) V_T histogram for $0 \rightarrow 1$ switching threshold considering variations in P_R and E_C of HZO in a 5nm Fe-FET.

To evaluate the impact of variations in ferroelectric properties, namely P_R and E_C, on switching characteristics, we consider 10000 samples of normally distributed P_R and E_C values each having three-sigma (3-σ) variation of 3% [99].

Fig. 7.7(b) shows the resulting distribution of switching threshold, under combined variation in P_R and E_C, for $0 \rightarrow 1$ transition at low and high drain bias. A normal distribution with 3-σ variation of 8% in switching threshold is observed for both low and high drain bias. A clear separation between the two switching threshold levels is observed, which permits successful writing into the FeFET cell using the

methodology described in Section IV. However, it can be shown that this variation increases to 25%, if the variations in ferroelectric material properties is assumed to be 10%. This would necessitate the employment of appropriate error correction schemes to address write-errors arising from cells lying in the overlapping region of switching voltage distributions. Further, a relaxed placement of memory cells might be beneficial to minimize read-disturb arising due to capacitive coupling between neighboring cells.

7.6 Conclusion

To conclude, this work describes a realizable possibility of next generation 1T Ferroelectric-NOR type memory using 5nm FeFETs with HfZrOx ferroelectric. The dynamic modulation of memory window of FeFETs using drain bias facilitates 1T NOR configuration while also greatly simplifying the erase, program and read operations associated with Fe-NAND configuration [97]. Our simulation based analysis shows that memory array can operate with sub-1V program/erase voltages and is therefore a promising candidate for ultra-low power memory achieving ultra-high density while maintaining non-volatility. The proposed 1T ferroelectric memory is expected to expedite further research and technical developments in the memory business.

8. SUMMARY

A steep-slope transistor is inevitable to enable supply-voltage scaling which could reduce the overall power dissipation of future integrated circuits. In this thesis, two such transistor alternatives were discussed at sub-10nm gate-lengths: Tunnel-FETs (TFETs) and Negative-Capacitance FETs (NCFETs). It was shown that both the transistor alternatives can overcome the sub-60mV/dec subthreshold-swing (SS) limit of MOSFETs. TFETs typically improve SS in subthreshold region of operation, while the NCFETs offer more improvement in super-threshold region. The key contributions of this work are summarized below:

- *Doped-source underlapped TFETs:* Source underlapping is shown to achieve lower subthreshold swing in both n- and p- type sub-10nm GaSb-InAs TFETs and is verified with the analytical treatment. Impact of parameter variations on the performance of underlapped-TFETs is investigated through atomistic, 2D ballistic simulations using self-consistently, coupled Non-equilibrium Greens Function (NEGF)-Poisson approach. Variations in underlap length, underlap doping, fin-thickness and temperature are comprehensively studied.

- *Intrinsic-source TFET to reduce band-tail effects on subthreshold swing:* High doping is shown to be associated with band-tails in the density of states that decay exponentially into the bandgap, comparable to the decay of carrier density above the band-edge due to Fermi-tails. This severely limits the subthreshold swing and off-current in TFETs. As a solution, we propose an undoped-source GaSb/InAs broken-gap TFET in an i-i-n configuration which achieves similar performance to that of a corresponding p-i-n TFET while having exactly same geometry. In the proposed device, the high drive-current is supported by broken-gap tunnel junction, while the Fermi-level pinning near the valence band of GaSb

helps in realizing an ohmic source contact for carriers in the valence band which eventually participate in interband tunneling at broken-gap tunnel junction in the ON state.

- *Circuit evaluation of proposed TFETs and proposal of novel 4T Embedded DRAM:* Circuit simulations of a 6-stage inverter chain show that sub-10nm underlapped TFETs are especially suited for near-threshold computing because of their ability to achieve higher throughput while consuming $\approx$ 100x lower power compared to Si FinFETs. To analyze the suitability of sub-10 nm TFETs for medium-throughput and ultra-low power applications in future very large scale integrated designs, a LEON3 processor is synthesized at $V_{DD} = 0.25V$. The impact of interconnect parasitics on the performance of TFETs is considered by studying the power-performance of the LEON3 under varying wire-load conditions. Under moderate interconnect parasitics, TFETs-based processor is shown to exhibit more than 50% power reduction compared to FinFETs. We also study the potential of TFETs in ultra-low power and high density dynamic memories. A novel 4T gain cell embedded DRAM is proposed which utilizes the low leakage current of the source underlapped TFETs to improve the data retention time to $25\mu s$ at $V_{DD} = 0.35V$, thereby enabling prospects of embedded DRAM at nanoscale gate-lengths operating at ultra-low supply voltages.

- *Design-space exploration of hysteresis-free Sub-10nm NCFETs:* A detailed simulation analysis is performed to investigate the design-space of HfZrOx-based NCFETs. Planar bulk-NCFETs are shown to complicate the capacitance matching with the FE-HZO due to channel charge contribution coming predominantly from ionized dopants. Sub-20nm FDSOI-NCFETs exhibit improved NCFET performance, with major benefits coming from its undoped body. Finally, a sub-10nm NC-FinFET analysis reveals that the improved gate-control permits downscaling of supply voltage to 0.25V while employing ultra-thin 3nm FE-

HZO films. The results presented in this work can further be used to improve the NCFET performance in recent experimental works discussed in [72, 100].

- *Proposal of 1T non-volatile memory based on ferroelectric FETs:* A realizable possibility of next generation 1T Ferroelectric-NOR type memory was described using 5nm FeFETs with HfZrOx ferroelectric. The dynamic modulation of memory window of FeFETs using drain bias facilitates 1T NOR configuration while also greatly simplifying the erase, program and read operations associated with Fe-NAND configuration [97]. The simulation based analysis shows that memory array can operate with sub-1V program/erase voltages and is therefore a promising candidate for ultra-low power memory achieving ultra-high density while maintaining non-volatility. The proposed 1T ferroelectric memory is expected to expedite further research and technical developments in the memory business.

9. FUTURE WORK

9.0.1 TFETs based on TMDs

One of the major challenges of TFETs is their low ON-currents. 2D material based TFETs can have tight gate control and high electric fields at the tunnel junction, and can in principle generate high ON-currents along with a sub-threshold swing smaller than 60 mV/dec. TMDs form a general class of materials of the form MX2, where M is a transition metal (Mo, W, etc.) and X is a Chalcogenide (Te, Se, S), a variety of material parameters can be accessed by the correct choice of material. The field of 2D materials is still at its infancy as novel materials are being discovered, which opens up opportunities for TFET designs. Also, the band structure and electronic properties such as band gap, effective mass, and dielectric constant of TMD materials depend on the number of layers. Consequently, devices with different number of layers are expected to show different characteristics and are worth evaluation in a simulation/experimental environment.

9.0.2 Experimental Evaluation of i-i-n TFETs

Till date, there is no experimental evidence of band-tails via electronic transport measurements. We are in the process of exploring the possibility of experimental evaluation of i-i-n TFETs. Several material systems can be employed to explore the effects of band-tails on the subthreshold-swing of the TFET. Apart from the broken-gap GaSb/InAs material system discussed in chapters above, recent advances in phosphorene (black phosphorus) show that they can form similar broken-gap when deposited on a silicon substrate. Any advances in this direction is expected to uncover

the negative impacts of various non-ideal effects like trap-assisted tunneling, SRH leakage and band-tails on the subthreshold-swing of the TFET.

9.0.3 Modeling of Multi-domain Ferroelectrics

In *Chapters 6* and *7*, we used a simplistic single-domain model of ferroelectric, based on Landau-Khalatnikov theory, to analyze hysteresis-free Negative-Capacitance FETs and hysteretic Ferroelectric-FETs. This assumption works perfect for nano-scale devices, however breaks-down for larger devices due to the presence of multiple ferroelectric domains. Recent experimental investigations suggest that, in large devices, multiple pulses of varying amplitude and width need to be applied to switch them completely [101]. Also, the partial switching of large ferroelectric material can be utilized to design 1T multi-bit memories. Hence, a physics-based model which can accurately capture the switching mechanism in multi-domain ferroelectrics is of utmost importance to predict the behavior of large-sized fabricated devices.

9.0.4 Application of Ferroelectric FETs in Neuromorphic Computing

Artificial Neural Networks (ANN), capable of massive parallel information processing and adaptive learning, have attracted immense interest for future data-driven society. While taking inspiration from human brain, these networks can accomplish several complex tasks like image-recognition, learning, etc. with phenomenal accuracy, that too at much lower-power compared to traditional Von-Neumann CMOS-based computing. At the heart of this intelligence lie the artificial neurons which accept weighted input signals and generate output pulses if the total value of input exceeds a threshold value. The weighting operation is performed by synapses attached to neurons. Until now, the synapses and neurons have been predominantly implemented using CMOS neurons and SRAM-based synapse [102]. However, such implementation is rather difficult for a large-scale implementation, due to requirement of large number of synaptic connections. One feasible solution to this hardware prob-

lem is to use ultra-scale non-volatile memory devices. The 1T FeFET non-volatile memory array, discussed in *Chapter 7*, can be efficiently utilized as binary synapse in a crossbar-like implementation to perform binary operation (weighting by 1 or 0) on the inputs. They exhibit two specific features much superior to other information processing systems 1) Adaptive-learning capability which means that their electrical properties can be changed by applying signals of appropriate polarity 2) Low-power consumption to perform read/write operations.

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VITA

VITA

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