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Characterization of Manifold Microchannel Heat Sinks During Two-Phase Operation

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CHARACTERIZATION OF MANIFOLD MICROCHANNEL HEAT SINKS DURING TWO-PHASE OPERATION

by

Kevin P. Drummond

A Dissertation

Submitted to the Faculty of Purdue University

In Partial Fulfillment of the Requirements for the degree of

Doctor of Philosophy

School of Mechanical Engineering

West Lafayette, Indiana

May 2018

THE PURDUE UNIVERSITY GRADUATE SCHOOL
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ACKNOWLEDGMENTS

First and foremost, I would like to thank both of my advisors, Dr. Suresh V. Garimella and Dr. Justin Weibel, for their support and direction throughout my Ph.D. Their guidance has been invaluable to my personal and professional development and I am grateful for the opportunity that they have afforded me.

I would also like to thank the members of my advisory committee, Dr. Eckhard Groll and Dr. Dimitrios Peroulis, for the guidance that they have provided during my research. Their comments and suggestions have helped shape this work into what it is today.

Thank you to Dr. David Janes, Mr. Doosan Back, Mr. Michael D. Sinanis, and the rest of the DARPA MicroICE team, without which this research would not have been possible. Each team members' knowledge, expertise, and hard work were critical to the success of the project.

I am deeply indebted to many of my lab mates who helped me get acclimated at Purdue and in the lab and provided feedback on my research. Dr. Matt Rau, Dr. Ravi Patel, Dr. S. Niki Ritchey, and Mr. Todd Kingston deserve special recognition for the positive effect they have had on my work.

Finally, thank you to my family. Thank you for always encouraging me to pursue my dreams and providing me with the tools necessary to succeed from a young age. Thank you for guiding and supporting me throughout my life, which has helped shape me into the person I am today and for that I am truly grateful.

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NOMENCLATURE

A	area
AR	aspect ratio
d	depth
d_{wafer}	wafer thickness
c_p	specific heat
G	mass flux
h_{wall}	heat transfer coefficient
h_{LV}	latent heat of vaporization
I	electrical current
k	thermal conductivity
L	length
L_{nd}	nondimensional length
N_c	number of channels per heat sink
N_{sink}	number of heat sinks
P_{el}	electrical power
P_c	channel perimeter
Q	heat
$R_{HS,heater}$	hotspot heater electrical resistance
$R_{HS,tot}$	combined electrical resistance of hotspot heater and traces
R''_{th}	overall thermal resistance
R''_{cond}	conduction thermal resistance
R''_{fluid}	caloric thermal resistance
T	temperature
$T_{fl,ref}$	fluid reference temperature
V	voltage
w	width
x	thermodynamic quality
z	location along channel

GREEK SYMBOLS

ρ	mass density
η_f	fin efficiency
η_0	overall surface efficiency
φ	phase

SUBSCRIPTS

avg	average
b	base
base	base of channels
BG	background
c	channel
chip	chip surface
el	electrical
f	fin
fl	fluid
HS	hotspot
i	individual zone
in	inlet
loss	loss
out	outlet
sat	saturation
sens	sensible
Si	silicon
sink	heat sink
SiO_2	silicon dioxide
tot	total
wet	wetted area

ABSTRACT

Author: Drummond, Kevin P.. PhD
Institution: Purdue University
Degree Received: May 2018
Title: Characterization of Manifold Microchannel Heat Sinks During Two-Phase Operation
Major Professors: Suresh V. Garimella, Justin A. Weibel

High-heat-flux removal is necessary for next-generation microelectronic systems to operate more reliably and efficiently. The direct embedding of microchannel heat sinks into the heated substrate serves to reduce the parasitic thermal resistances due to contact and conduction resistances typically associated with the attachment of a separate heat sink. Manifold microchannel (MMC) heat sinks can dissipate high heat fluxes at moderate pressure drops, especially during two-phase operation. High-aspect-ratio microchannels allow for a large enhancement in heat transfer area. This work focuses on designing intrachip MMC heat sinks for high-heat-flux dissipation and to characterize the flow morphology present in the MMCs during two-phase operation.

A 3 × 3 array of heat sinks is fabricated into a heated silicon substrate for direct intrachip cooling. The heat sinks are fed in parallel using a hierarchical manifold distributor that is designed to deliver equal flow to each of the heat sinks. Each heat sink contains a bank of high-aspect-ratio microchannels; channels with nominal widths of 15 μm and 33 μm and nominal depths between 150 μm and 470 μm are tested. Discretizing the chip footprint area into multiple smaller heat sink elements with high-aspect-ratio microchannels ensures shortened effective fluid flow lengths. High two-phase fluid mass fluxes can thus be accommodated in micron-scale channels while keeping pressure drops low compared to traditional, microchannel heat sinks.

The thermal and hydraulic performance of each heat sink array geometry is evaluated using the engineered dielectric liquid HFE-7100 as the working fluid and for mass fluxes ranging from 600 kg/m²s to 2100 kg/m²s at a constant inlet temperature of 59 °C. To simulate heat generation from electronics devices, a uniform background heat flux is generated with thin-film serpentine heaters fabricated on the silicon substrate opposite the channels; temperature sensors placed across the substrate provide spatially resolved surface temperature measurements. Experiments are also

conducted with simultaneous background and hotspot heat generation; the hotspot heat flux is produced by an individual 200 μm × 200 μm hotspot heater.

During uniform heating conditions, heat fluxes up to 1020 W/cm² are dissipated at chip temperatures less than 69 °C above the fluid inlet and at pressure drops less than 120 kPa. Heat sinks with wider channels yield higher wetted-area heat transfer coefficients, but not necessarily the lowest thermal resistance; for a fixed channel depth, samples with thinner channels can have increased total wetted areas owing to the smaller fin pitches. During simultaneous background and hotspot heating conditions, background heat fluxes up to 900 W/cm² and hotspot fluxes up to 2,700 W/cm² are dissipated. The hotspot temperature increases linearly with hotspot heat flux and is independent of background heat flux and mass flux. At hotspot heat fluxes of 2,700 W/cm², the hotspot experiences a temperature rise of 16 °C above the average chip temperature.

The ability to fabricate and assemble a chip-integrated, compact hierarchical manifold used to deliver fluid to a 9 × 9 array of heat sinks has been demonstrated, with feature sizes significantly reduced compared to the 3 × 3 array of heat sinks. The integrated manifold provides ports to measure the pressure drop across the channel; combining these data with the overall pressure drop, the contributions of both components to the hydraulic performance is determined. The hierarchical manifold consists of eight feature layers that have a minimum feature size of 50 μm. The manifold is fabricated by etching one feature layer into each side of four silicon wafers and then thermocompression bonding the wafers together. The resulting manifold is a compact, leak-free device that is used to deliver fluid to the array of heat sinks and recollect the outlet flow from the heat sinks. A sample manifold was diced, revealing a manifold that was aligned with the channels within 5 μm. Heat fluxes up to 630 W/cm² are tested with temperatures and pressures reaching 110 °C and 135 kPa, respectively.

An experiment is designed to provide simultaneous high-speed flow visualization and spatially-resolved wall temperature measurements on a single manifold microchannel. Visualizing the flow morphology inside the channel during two-phase operation is critical to being able to understand the performance MMCs. This work provides an understanding of the two-phase flow structure and wall temperature profiles in high-aspect-ratio microchannels, which cannot be extracted from the area- and time-averaged data obtained using the heat sinks containing many parallel channels. In high-aspect-ratio channels, vapor blanketing at the bottom of the channel is observed, which leads to significantly diminished thermal performance. The vapor formation

characteristics in high-aspect-ratio microchannels also lead to time-periodic fluctuations that are not observed in low and intermediate aspect ratios. Opportunities for future experimental and model work to further understand flow boiling in MMCs are identified based on the work completed in this dissertation and the open literature.

1. INTRODUCTION

1.1 Background

The continuing miniaturization of electronics components of ever greater performance and functionality has led to severely increased thermal management challenges. For example, heat fluxes in excess of 1000 W/cm² must be dissipated in next-generation radar, power electronics, and high-performance computing systems [1,2]. Electronic devices have traditionally been cooled through the attachment of standalone heat sinks. In this 'remote cooling' architecture, the total temperature rise across the thermal management solution is governed by parasitic interfacial, conduction, and spreading resistances between the device and heat sink. The deterioration of electrical performance characteristics and thermomechanical reliability at high device temperatures calls for the development of transformative 'intrachip cooling' strategies, with coolant channels deployed directly in the electronic device, to enable improved functionality of electronic systems. While direct, intrachip cooling allows for reduced conduction resistances and altogether eliminates contact resistances, heat spreading is drastically reduced, necessitating high heat transfer coefficients in the heat sink. Local hotspots in the die also can lead to high local chip temperatures and large temperature gradients across the die. Dielectric working fluids are preferred for such systems because they minimize the threat for electrical shorting, do not interfere with RF signals, are non-corrosive, and are available at a variety of saturation temperatures.

High heat fluxes can be dissipated using heat sinks utilizing straight, parallel microchannels [3]. In general, increasing channel depth, decreasing channel width, and increasing fluid flow rate all allow for larger heat dissipation at a given chip temperature. However, there are practical limits to how deep and thin these channels can be made. Additionally, pressure drop along the length of the channels leads to intractably large pumping power requirements at the extremely small channel widths and high flow rates necessary to dissipate extreme heat fluxes on the order of 1000 W/cm^2. Transitioning to two-phase evaporative cooling in microchannel heat sinks can provide improved surface temperature uniformity and increased heat dissipation compared to single-phase heat sinks [4–6].

In addition to traditional microchannels, a variety of heat sink designs have been implemented to dissipate high heat fluxes at reduced pressure drop. One such design is manifold

microchannel (MMCs) heat sinks, which distribute the flow through the microchannel heat sink in multiple parallel flow paths of decreased effective flow length. Figure 1.1 shows the fluid flow paths in a manifold microchannel heat sink; fluid from the manifold (not shown) arrives normal to the microchannels through a plenum plate, which defines the inlets and outlets to the channels. The flow impinges on the channel base, splits and travels along the channel in both directions, and exits the channels through the plenum plate. The decreased flow length in MMC heat sinks can lead to significantly higher heat flux dissipation compared to conventional microchannel heat sinks at the same allowable pressure drop [7]. Significant effort has gone into predicting the optimal geometric and operational parameters for MMC heat sinks during single-phase operation; a range of experiments have also been conducted for single-phase flows in MMC heat sinks. The few studies that have focused on the two-phase operation of MMC heat sinks [8–10] have shown their viability as high-heat-flux removal devices.

1.2 Objectives and Major Contributions

The main goals of the present work are to: (1) design and fabricate hierarchical MMC heat sinks with thin, high-aspect-ratio microchannels in a monolithic substrate along with the simulated heat source, (2) experimentally characterize the thermal and hydraulic performance of the MMC heat sinks during two-phase operation using a dielectric working fluid, (3) design and characterize a compact, highly discretized MMC heat sink, and (4) to investigate the two-phase flow morphology and local wall temperature measurements for high-aspect-ratio microchannels.

A 3 × 3 array of heat sinks—each containing a bank of parallel, high-aspect-ratio (AR = 2.7 to 19.1), small hydraulic diameter (~20 to 60 μm) microchannels—are fabricated in a silicon chip over a 5 mm × 5 mm area. The intrachip microchannels are etched directly into the substrate of the heat source (also 5 mm × 5 mm) to limit conduction and contact resistances, allowing for higher heat flux removal. Fluid is delivered to the microchannels through a hierarchical manifold designed to provide uniform flow to each heat sink in the array throughout two-phase operation. Heat flux in excess of 1 kW/cm² are dissipated, demonstrating the ability of two-phase MMC heat sinks to dissipate high heat fluxes. The effects of fluid mass flux, channel depth, channel width, and aspect ratio are studied. Results are presented for the cooling of a uniform background heat flux and with simultaneous hotspot heating. A compact hierarchical manifold is designed and fabricated to deliver fluid to a 9 × 9 array of heat sinks over a 5 mm × 5 mm area. The overall size

of the test device, including the manifold, is 20 × 20 × 3 mm^3. The device shows reliable performance and was tested up to 660 W/cm^2. An experiment is designed to obtain simultaneous flow visualization and spatially resolved wall temperature measurements in a single manifold microchannel. These experiments provide valuable insights into the flow morphology in high-aspect-ratio MMCs during two-phase operation heat sinks and its effect on thermal performance.

1.3 Organization of the Document

Chapter 1 contained background information pertaining to MMC heat sinks and provided the objectives and major contributions of the present work. Chapter 2 provides a review of the literature containing heat sink designs focused on high heat flux removal with an emphasis on MMC heat sink design and optimization and evaporative cooling strategies. Chapter 3 presents the fabrication of a novel manifold microchannel heat sink design and experimental characterization of the thermal and hydraulic performance during two-phase operation. Chapter 4 describes the testing of manifold microchannel heat sinks with different channel geometries during simultaneous uniform and hotspot heat flux dissipation. Chapter 5 presents the design and testing of a compact, highly discretized manifold microchannel array and compares the results to select data from Chapter 3. Chapter 6 presents a novel single-channel test facility used to visualize the two-phase flow morphology in the manifold microchannel and simultaneously measure local fin temperatures. Chapter 7 provides a summary of the conclusions from this work and the suggestions for future research.

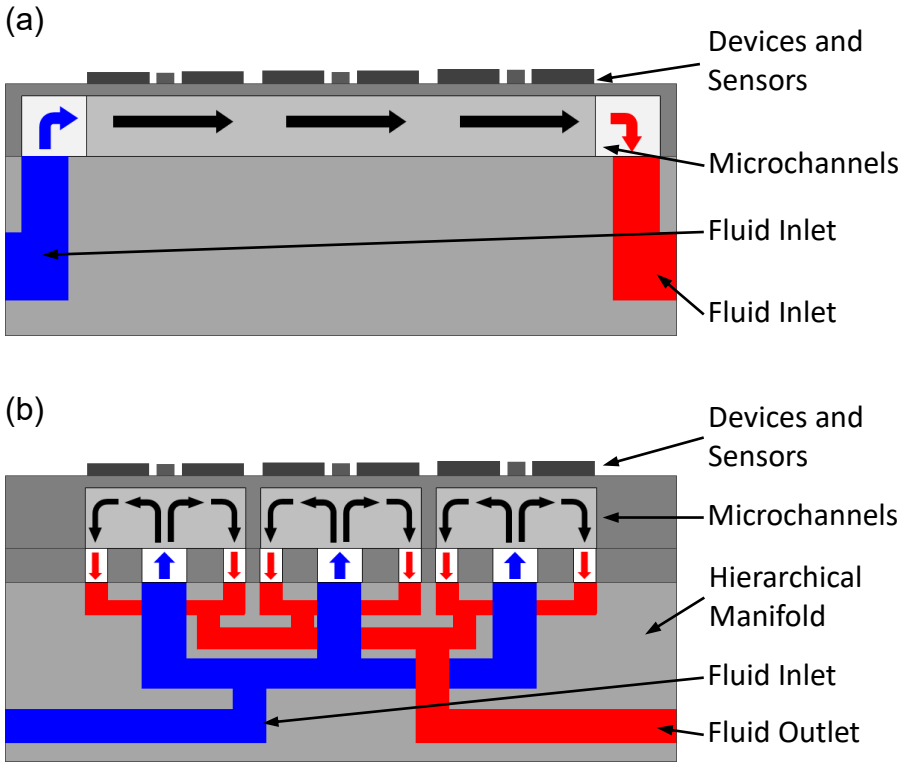

Figure 1.1. Cross-sectional schematic diagrams of direct cooling using (a) a traditional microchannel heat sink and (b) a intrachip hierarchical manifold microchannel heat sink design.

2. LITERATURE REVIEW

2.1 Single-Phase Microchannel Heat Sinks

Heat sinks containing deep, high-aspect-ratio microchannels provide high heat transfer coefficients and large area enhancement, which make them a candidate for high-heat-flux applications. In a pioneering study by Tuckerman and Pease [1], a 10 mm × 10 mm silicon microchannel heat sink with 50 μm wide and 300 μm deep channels was shown to dissipate 790 W/cm² at chip temperature rises of less than 71 °C above the fluid inlet temperature and pressure drops less than 186 kPa, using single-phase water as the working fluid. Single-phase microchannel heat sinks have been widely studied for electronics cooling applications [1], [2]. In general, increasing channel depth, decreasing channel width, and increasing fluid flow rate all allow for larger heat dissipation at a given chip temperature. However, there are practical limits to how deep and thin these channels can be made. Additionally, pressure drop along the length of the channels leads to intractably large pumping power requirements at the extremely small channel widths and high flow rates necessary to dissipate extreme heat fluxes on the order of 1000 W/cm^2.

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2.2 Two-Phase Microchannel Heat Sinks

Two-phase evaporative cooling occurs when the fluid flowing through a heated channel reaches a temperature that causes bubble incipience to occur at the heated surface. Figure 2.1 shows the progression of boiling regimes at a given location along a microchannel as heat flux is increased [3]. At low heat fluxes, small bubbles nucleate at the walls and detach as the fluid moves past the wall; the bubbles remain isolated and are smaller than the width of the channel. As heat flux is increased, the bubble nucleation rate increases and the bubbles grow, resulting in coalescence; in microchannels, where the flow is confined in the transverse direction, the bubble grows preferentially along the channel length, producing vapor slugs that occupy nearly the entire channel cross-section. With a further increase in heat flux, the vapor slugs merge, causing a continuous vapor core surrounded by a liquid annulus to form. At high heat fluxes, the liquid film becomes thinner and the vapor core velocity increases as more liquid evaporates. Eventually, there

is not enough fluid to keep the wall wetted, resulting in dryout. Sudden temperature rises usually accompany dryout due to the relatively ineffective heat transfer performance of the vapor at the wall compared to the thin, liquid film in the other flow regimes.

Two-phase evaporative cooling in traditional microchannel heat sinks has been widely explored to improve surface temperature uniformity and heat dissipation efficiency relative to single-phase cooling [4]–[7]. Two-phase operation can also enable reductions in size, weight, and overall power consumption when compared to single-phase systems, which can lead to lower overall system costs.

2.3 High-Heat Flux Cooling Technologies

For most working fluids, the latent heat of vaporization is orders of magnitude larger than the specific heat capacity; hence, evaporative cooling systems can operate at lower chip temperature rises and at reduced flow rates to dissipate the same amount of heat as single-phase systems. However, a significant fraction of the liquid must be evaporated before exiting the channel to realize the full potential of evaporative cooling. In most microchannel systems, intermittent dryout of the liquid film or flow instabilities causing premature critical heat flux (CHF) can lead to reduced performance well before a high exit quality can be reached. For flow boiling in microchannels, CHF has been found to increase with increasing channel wetted area, mass flux, and channel hydraulic diameter, as well as decreasing channel length [8]. Channel wetted area can be increased by decreasing channel pitch (*i.e.*, decreasing channel and fin widths to increase the number of channels) or increasing channel depth. Because pressure drop scales with L/d_H^2 [9], decreasing the channel width while holding flow length constant results in prohibitive increases in pressure drop.

A variety of heat sink designs have been employed to dissipate larger heat fluxes by delaying CHF or reducing the pressure drop in two-phase operation compared to a conventional design with straight, parallel channels fed by a single header. These designs have implemented one or more of features such as vapor venting [10], pin-fins and interrupted channels of various shapes and configurations [10]–[12], wick structures to aid in thin film evaporation [13]–[15], microchannels with reentrant cavities and/or inlet restrictors [16], microgaps [17], arrays of jets [18]–[21], diverging channels [22], [23], microchannels fed with tapered manifolds [24], and stacked heat sinks [25]. Heat fluxes as high as 1127 W/cm² have been dissipated with dielectric

fluids [26] using a 10 mm × 20 mm copper heat sink that incorporated both flow boiling in microchannels and jet impingement. In this demonstration, the surface temperature at the highest heat flux exceeded 200 °C for a refrigerated fluid inlet temperature of -20 °C, which would present significant implementation challenges in electronics cooling applications.

2.4 Single-Phase Manifold Microchannel Heat Sinks

Manifold microchannel heat sinks aim to increase maximum heat dissipation and decrease pressure drops at high flow rates and vapor fractions by distributing the flow through the microchannel heat sink in multiple parallel flow paths of decreased effective flow length. While channel length in traditional microchannel heat sinks is set by the length of the device being cooled, manifold microchannel heat sinks decouple flow length from the device size by delivering the fluid intermittently along the channel length, creating multiple parallel flow paths of decreased effective flow length. Figure 1.1(a) shows a traditional microchannel heat sink which contains a single inlet, a bank of microchannels spanning the entire device length, and a single outlet; Figure 1.1(b) shows a manifold microchannel heat sink design where the heated area is discretized into an array of multiple heat sinks, each with separate inlets and outlets that are fed in parallel.

Harpole and Eninger [27] developed a thermal model for single-phase flow in manifold microchannel heat sinks to optimize geometric parameters of a silicon heat exchanger using a water-methanol mixture as the working fluid. Their models predicted that steady-state heat fluxes greater than 1000 W/cm² were achievable with a fluid-to-chip temperature rise of less than 30 °C and a pressure drop of 101 kPa using high-aspect-ratio microchannels (channel widths from 7 μm to 14 μm and heights of 167 μm). Most research on manifold microchannel heat sinks for electronics cooling has continued to focus on single-phase operation. A variety of researchers have conducted numerical studies to identify optimized geometries and operating conditions for both the fluid distribution manifold and microchannel heat sink [28]–[36]. These studies concluded that (1) at a fixed pumping power, there is an optimal channel height, channel width, and flow length for which thermal resistance is minimized, (2) the flow length should be minimized to minimize pressure drop for a fixed heat flux until manifold pressure drop governs the overall pressure drop at extremely short flow lengths, and (3) decreasing the channel width and increasing the flow rate both increase the heat transfer rate at the cost of increased pressure drop. While the

optimal geometric and operational parameters depend on the working fluid, desired heat flux, and allowable pumping power, these studies have shown that manifold microchannel heat sinks can increase heat dissipation without significantly increasing pressure drop when compared to traditional microchannels. For example, Ryu *et al.* [28] found that single-phase manifold microchannel heat sinks can dissipate >50% higher heat fluxes than a conventional microchannel heat sink at the same allowable pressure drop. Several experimental studies have confirmed that, in single-phase operation, manifold microchannel heat sinks can dissipate high heat fluxes at moderate pressure drops [37]–[39].

Experimental studies have also shown that manifold microchannel heat sinks can dissipate high heat fluxes at moderate pressure drops [35], [40], [41]. The increased number of parallel flow paths in manifold microchannel heat sinks can lead to flow maldistribution between channels caused by uneven pressure drops in the manifold; this can cause significant performance reduction if not properly accounted for. Manifolds with constant cross-sectional area flow channels result in channels at the end of the manifold receiving a disproportionately large portion of the total flow [30], [42]. For the geometry and flow rates studied, Tang *et al.* [42] showed that the final four channels (out of 10 total) received 85 % of the total flow, with the final channel receiving over 35 %. Similarly, Escher *et al.* [30] showed that there is a 70 % difference in mass flow rate between the channel at the beginning of the manifold and the last channel. This amount of flow maldistribution can lead to significant chip temperature gradients and hotspots across the chip surface. Both studies found that flow maldistribution can be drastically reduced, but not eliminated, during single-phase operation by using tapered manifold flow channels.

2.5 Two-Phase Manifold Microchannel Heat Sinks

Few studies have considered two-phase operation of manifold microchannel heat sinks. In one study, Baummer *et al.* [40] demonstrated dissipation of a heat flux of 300 W/cm² over a 1 cm² area with a chip temperature rise less than 50 °C using a manifold microchannel heat sink having 42 μm wide and 483 μm deep channels using HFE-7100 as the working fluid.

Cetegen [43] characterized high-aspect-ratio manifold microchannel heat sinks during two-phase operation. Channel widths between 22 μm and 60 μm and heights between 406 μm and 483 μm (aspect ratios from 6.8 – 18.7) were fabricated in copper using Micro Deformation Technology. The heat sink covered a 1 cm² are and the manifold consisted of five rectangular fluid inlets; the

flow length (dictated by the wall thickness of the manifold walls, was 450 μm. Using R-245fa as the working fluid, heat fluxes up to 1.23 kW/cm² were dissipated over a 1 cm² area at a temperature rise of ~56 °C and pressure drop of 60 kPa.

2.6 Hotspot and Non-Uniform Heat Flux Dissipation

In many practical electronics cooling applications, non-uniform heat flux generation is common, and must be accommodated by the heat sink design to limit temperature gradients in the chip. For example, Sharma *et al.* [32], [44] tested a manifold microchannel heat sink designed to dissipate non-uniform heat fluxes more effectively by utilizing varying channel geometries depending on spatial location on the chip. Background heat fluxes of 20 W/cm² with periodic 300 W/cm² hotspots evenly distributed across the chip surface were tested; chip temperature uniformity was maintained within a 15 °C spread using single-phase water as the working fluid. Lorenzi *et al.* [45] modelled and experimentally-tested pin fin heat sinks with variable pin sizes and pitches to dissipate a hotspot heat flux superimposed on a background heat flux. Hotspot heat fluxes up to 750 W/cm² were dissipated with 250 W/cm² background heat fluxes, with the local substrate temperature at the hotspot remaining below the maximum substrate temperature, which occurred near the fluid outlet. Abdoli *et al.* [46] modelled a pin-fin heat sink with a hotspot heat flux of 2 kW/cm² superposed on a background heat flux of 1 kW/cm². Using single-phase water as the working fluid, they predicted that an array of pin fins would yield spatial temperature uniformity with a maximum variation of less than 10 °C.

Recent heat sink designs have targeted simultaneous dissipation of a high, uniform die-level heat flux (>1,000 W/cm²) with significantly higher heat flux hotspots, representative of RF electronic devices. Technologies that have been evaluated include a GaN-on-diamond manifold microchannel heat sink [47], an embedded pin-fin heat sink with a manifold fluid distributor [48], a manifold microchannel heat sink with non-uniform channel height and shape [49], and a heat sink employing fluid impingement onto diamond-lined, silicon-carbide microchannels [50] Additional complexities arise in evaporative heat sink systems during non-uniform heating. For example, Ritchey *et al.* [13-14] found that non-uniform heating can lead to flow instabilities and flow maldistribution that induce premature critical heat flux during two-phase operation of microchannel heat sinks.

2.7 Flow Visualization

Flow visualizations in traditional microchannels have provided key insights into the morphological changes that occur with different channel geometries, fluids and flow rates, and heat fluxes [53]. Due to drastic changes in the flow morphology with each of these variables, it is difficult to generally correlated performance in two-phase microchannel heat sinks with high accuracy. Rather, flow regime maps categorize discrete regions of similar flow morphology. For example, depending on the channel geometry and flow characteristics, flow regimes present in microchannel systems include bubbly, slug, and annular flows. Inside each regime, mechanistic models specific to the flow morphology yield improved predictive capabilities [54].

Flow visualizations of two-phase flows in manifold microchannels have not been widely reported. Cetegen [43] provided flow visualizations in a single manifold microchannel unit cell with a channel length of 3.875 mm and a channel height of 2.42 mm and channel widths of 70 μm and 225 μm using HFE-7100 as the working fluid. A heated copper block is used to provide a uniform wall heat flux boundary condition at the channel wall and a glass plate provides optical access from the other side. For the range of mass fluxes and heat fluxes tested, they observed flow regimes similar to traditional microchannels of the same dimensions; however, transitions between regimes occur radially from the inlet and vapor can be trapped in the stagnation regions for some operating conditions. Flow instabilities were also observed, which were attributed to nucleation suppression in the impingement region and vapor blockage at the outlet.

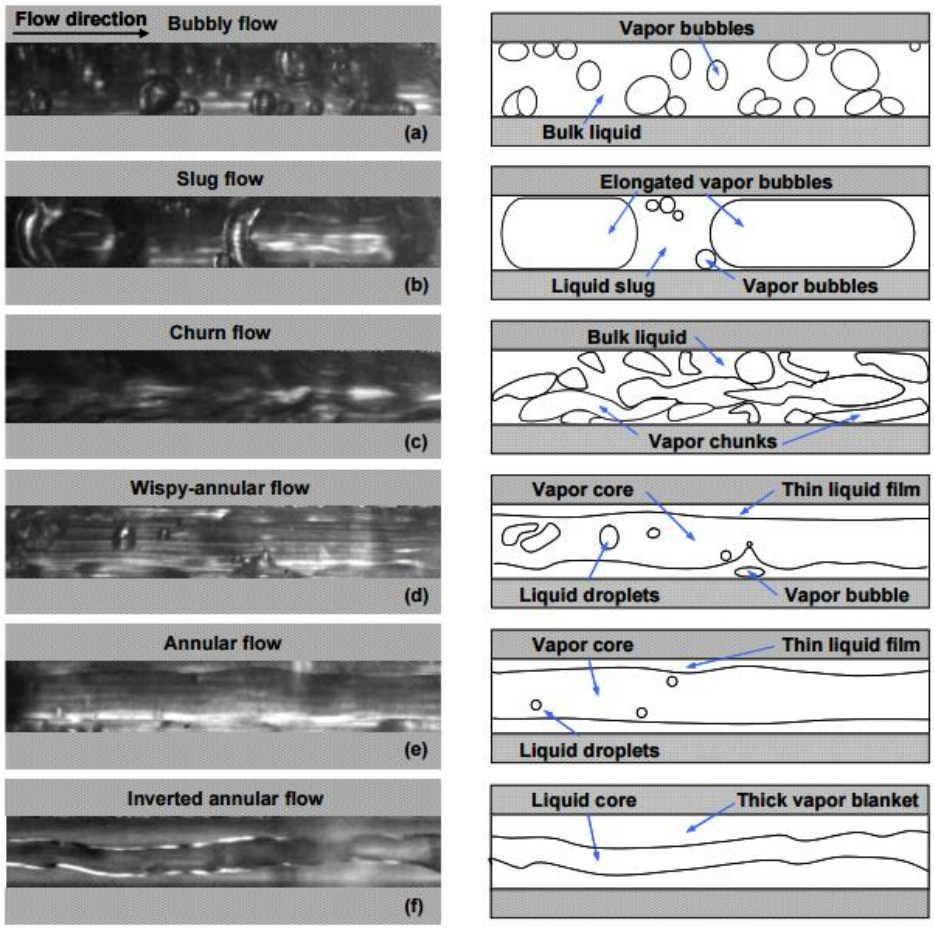


Figure 2.1. Description of boiling flow regimes [3].

3. A HIERARCHICAL MANIFOLD MICROCHANNEL HEAT SINK ARRAY FOR HIGH-HEAT-FLUX TWO-PHASE COOLING OF ELECTRONICS

This chapter focuses on designing, fabricating, and characterizing a hierarchical manifold microchannel array for intrachip evaporative cooling with a dielectric fluid. Extreme heat flux dissipation from electronic devices at low pressure drops and low chip temperatures has not been previously demonstrated using dielectric fluids. A 3 × 3 array of heat sinks—each containing 50 parallel, high-aspect-ratio (AR = 2.7 to 19.1), small hydraulic diameter (~20 to 30 μm) microchannels—are fabricated in a single silicon chip over a 5 mm × 5 mm area. The intrachip microchannels are etched directly into the substrate of the heat source (also 5 mm × 5 mm) to limit conduction and contact resistances, allowing for higher heat flux removal. Fluid is delivered to the microchannels through a hierarchical manifold designed to provide uniform flow to each heat sink in the array throughout two-phase operation. The material in this chapter was presented at the Government Microcircuit Applications and Critical Technology Conference in 2015 and published in the proceedings [57]. It was later refined and published in the International Journal of Heat and Mass Transfer [58].

The work in Chapters 3, 4, and 5 are the result of collaboration with Doosan Back and Michael D. Sinanis, Ph.D. students in the School of Electrical and Computer Engineering at Purdue University. Mr. Sinanis designed the etching recipes, etched two of the channel wafers and plenum wafers, and diced the wafers. Mr. Back designed the heater/sensor masks, performed all of the fabrication steps for the heater/sensors, and wire-bonded the samples. Mr. Drummond designed the channels and manifolds, fabricated the remaining channels and manifold layers (lithography and etching), calibrated the device heaters and sensors, fabricated and assembled all thermal/hydraulic characterization facilities, ran the thermal-hydraulic experiments, and processed the data. The text sections 5.1.2 and 5.3 were written Mr. Back but are included in this thesis for continuity.

3.1 Test Vehicle Design and Fabrication

3.1.1 Hierarchical Manifold Microchannel Concept

Manifold microchannel heat sinks are designed to distribute fluid through multiple inlets and outlets along the heat sink so that the flow length through any single set of microchannels is significantly reduced. This concept is extended to achieve greatly improved performance in the current work by using a hierarchical manifold to feed an array of intrachip microchannel heat sinks featuring high-aspect-ratio channels. Direct liquid cooling minimizes conduction resistances and eliminates contact resistances that result from approaches relying on separately attached heat sinks. Figure 3.1 shows a schematic diagram of the hierarchical manifold microchannel heat sink array concept used in the current work. The silicon microchannel plate contains a 2D array of microchannel heat sinks, with each heat sink containing 50 microchannels in parallel, as well as resistance heaters and thermometers, as discussed later. The manifold routes a single flow inlet into the individual inlets to the microchannel heat sinks (blue regions in Figure 3.1). Fluid from the manifold arrives normal to each heat sink through a rectangular inlet centered along the length of each microchannel. Within each microchannel, the flow impinges on the channel base, splits in two directions, travels along the remaining channel flow length and exits into the manifold. Within the manifold, the flow from the array of microchannel heatsinks is combined into a single outlet stream (red regions in Figure 3.1).

3.1.2 Test Vehicle Design

A thermal test vehicle, with all coolant distribution components heterogeneously integrated, is fabricated to demonstrate the thermal and hydraulic performance of the microchannel cooling approach (Figure 3.2(a)). The system consists of a manifold base, manifold distributor, plenum interface plate, microchannel plate, and printed circuit board (PCB). The base serves as an interface between the flow loop and the hierarchical manifold distributor and contains ports for inlet and outlet pressure and temperature measurements. The manifold distributor splits the single coolant inlet into 9 parallel flow streams that enter a 3 × 3 array of microchannel heat sinks covering a 5 mm × 5 mm chip area and also recombines the 18 flow streams exiting the heat sinks into a single coolant outlet (Figure 3.2(b)). Each heat sink cools a footprint area of 1667 μm × 1667 μm, with 50 parallel channels occupying a central area of 1500 μm × 1500 μm; the flow

enters at the center of the channel length resulting in an effective flow length of 750 μm. The purpose of the plenum plate is to provide an interface for sealing between the manifold distributor and the microchannels and to define the inlet and outlet regions to the microchannels; the plenum plate matches the manifold features, providing a smooth surface to seal against. The plenum interface plate is designed to have equal total inlet and outlet flow areas. Previous designs in the literature that were optimized for single-phase flows found the optimal inlet-to-outlet area ratio to be approximately 1.5:1 to 3.5:1 [28], [33]; an increased outlet plenum size was incorporated in the current design to limit contraction of the high-velocity two-phase mixture at the channel outlet. One side of the plenum plate is mated to a 10 μm-thick double-sided adhesive and brought into contact with the manifold; the opposite side of the plenum plate is bonded to the microchannel plate (Figure 3.2). The top side of the microchannel plate is instrumented with heaters and sensors to evaluate the thermal performance. The PCB provides a convenient electrical interface to the heaters and sensors.

The current design is based on self-similar hierarchical manifold features that distribute flow using multi-level bifurcation (Figure 3.1). The design and the fabrication methods employed can be easily scaled to shorter flow paths or to cover larger heated areas as desired.

3.1.3 Test Vehicle Fabrication

The fabrication and assembly of each test vehicle component is described in detail in this section. All fabrication steps were performed on 4-inch (100 mm), double-side polished silicon wafers in the Birck Nanotechnology Center at Purdue University.

3.1.3.1 Microchannel Plate Fabrication

To begin the fabrication process, a 350 nm-thick SiO_2 layer was thermally grown (wet oxide, 1000 °C) on both sides of a silicon wafer (Figure 3.3(a)); the wafer thicknesses for Samples A, B, and C were 220 μm, 300 μm, and 385 μm, respectively. This oxide layer functions as an insulation layer for the heaters and resistance temperature detectors (RTDs), and also as a sacrificial hard mask used during dry etching of the microchannels. Microchannel fabrication (Figure 3.3(a)-(c)) began by spinning and soft-baking a 7 μm-thick layer of AZ9260 (AZ Electronic Materials) positive photoresist (PR) on one side of the wafer. The PR layer was exposed using a mask containing patterns for the microchannel features (MA6, Karl Suss), and developed

in a 1:3 solution of AZ400K (AZ Electronic Materials) diluted in deionized (DI) water. The masked oxide layer was dry-etched (Advanced Oxide Etch System, Surface Technology Systems (STS)) and the channels were deep reactive ion etched (DRIE) into the silicon via the Bosch process (Advanced Silicon Etch System, STS). The PR layer was then stripped (PRS2000, Avantor Performance Materials) and the oxide was removed from the channel-side of the wafer using a buffered oxide etch (BOE).

Scanning electron microscopy (SEM) images (JEOL JCM-6000, NeoScope) of the three different fabricated channel geometries are shown in Figure 3.4. The critical channel dimensions measured from SEM images are summarized in Table 3.1. For simplicity, the test chips will be referred to by their nominal channel depths (i.e., A: 15 μm × 35 μm; B: 15 μm × 150 μm; and C: 15 μm × 300 μm) throughout the discussion. The measured channel cross-sectional area, Ac, and channel wetted area, Awet, are based on the actual perimeter along the channel boundary, which accounts for the taper in the channel sidewalls and curvature at the bottom of the channels. The fin pitch is constant at 30 μm for all channel depths.

Heater and sensor features were then fabricated on the side of the wafer surface opposite the microchannels (Figure 3.3(d)-(f)). Serpentine heaters were patterned on the chip, matching the footprint of the 3 × 3 grid of microchannel heat sinks, and the RTDs were positioned near the center of each heat sink. The same procedures as described in the previous paragraph were used to produce a patterned AZ9260 mask layer for the serpentine heaters and RTDs. A 5-nm-thick layer of Ti and a 20-nm layer of Pt were successively deposited using e-beam evaporation. The lift-off process was completed by stripping the PR using PRS2000. The same lift-off process was repeated to fabricate the heater and RTD lead-wire traces (5 nm Ti and 200 nm Au). The traces were used to wire the nine serpentine heaters in parallel and to route the signals to the wire-bond pads at the periphery of the chip.

3.1.3.2 Plenum Plate Fabrication

The plenum plate was fabricated from an oxidized silicon wafer using the processing steps shown in Figure 3.5. The same PR and oxide layer patterning and etching steps that were employed for the microchannel features were used to produce a masking layer for the plenum plate inlets and outlets (Figure 3.5(b)). The plenum features were etched completely through the wafer

using DRIE. The PR was then stripped off the wafer using PRS2000 and the oxide was removed from both sides of the wafer using BOE (Figure 3.5(c)).

3.1.3.3 Microchannel-Plenum Plates Bonding

The microchannel and plenum plates were thermo-compression bonded to each other for proper sealing at the interface. To create the interfacial bonding layer, a 400 nm-thick Au layer was sputtered on top of a 100 nm Ti layer (QPrep Series, Mantis Deposition Ltd.). The wafers were then aligned, pressed into contact, and clamped in place in the bonding equipment (SB6e, Karl Suss). The wafers were bonded at 450 °C and 5000 mbar for 60 min. Once bonded, the wafers were diced (DAD-2H/6, Disco) into 20 mm × 20 mm chips with the heaters and RTDs occupying a 5 mm × 5 mm area at the center. Figure 3.6(a) shows an SEM image of the isometric view of a plenum plate bonded to the microchannel plate; the image is taken from the channel side of the test chip such that the microchannels are visible through the plenum inlet and outlet flow ports.

3.1.3.4 Test Chip Assembly

A custom PCB was designed to allow connection of lead wires to the heaters and RTDs on the top side of the chip. The outer edge of the channel plate was fixed to the underside of the PCB using epoxy. Electrical traces terminating in contact pads on the chip were wire-bonded to Au contact pads on the PCB. The nine serpentine heaters were wired in parallel to provide uniform heating over the 5 mm × 5 mm area; the nine 4-wire RTDs were individually powered. Figure 3.6(b-d) show a microscope image of the heaters and RTDs and photographs of the assembled test chip mounted to a PCB and wire-bonded.

3.1.3.5 Manifold Fabrication

The manifold distributor contains the hierarchical network of channels that serve as the interface between the flow loop and the array of microchannel heat sinks, as shown in Figure 3.2(a). The manifold consists of four laser-cut (PLS65MW, Universal Laser Systems), 3 mm-thick, clear acrylic sheets. The manifold plate closest to the base contains one inlet feature and one outlet feature; this plate matches the base flow features and is used to seal the manifold to the base using a silicone gasket. The plate closest to the plenum plate contains individual inlet and outlet channels for each heat sink, with adjacent channel exits combined into a single exit, as shown in Figure

3.2(b); this is done to increase the bonding feature sizes at the interface between the manifold and plenum plate. The two interior plates discretize the flow from the single inlet and outlet into the 3 × 3 array. These sheets are joined using 10 μm-thick adhesive film preforms that are laser-cut to match the flow features. The acrylic base serves as an interface between the flow loop and the manifold and contains ports for thermocouples and pressure taps at the inlet and outlet streams. During testing, the onset of boiling is verified by observing for the presence of vapor at the outlet of the test section, which is easily visualized through the transparent acrylic plates. A silicone gasket seals the manifold to the base.

3.1.3.6 Test Vehicle Assembly

For final assembly of the test vehicle, stainless steel fittings are inserted into the manifold for fluid connections, as are fittings for thermocouples and pressure transducers. A 10 μm-thick double-sided adhesive (5601, Nitto Denko) is laser-cut to match the footprint features of the manifold distributor. The adhesive is aligned with the manifold using guide pins and attached. The test chip is then aligned to the manifold using the guide pins and bonded using the adhesive. Insulation blocks (PEEK) are placed on top of the PCB and below the manifold. The bottom insulation block is mounted on an optical table and a pneumatic cylinder presses down on the top insulation block to compress the test vehicle assembly with a constant pressure. The test chip heaters are wired to a programmable DC power supply (XG100-8.5, Sorensen) using 16-gauge wire with an inline shunt resistor (HA-5-100, Empro) to measure the electrical current. The RTDs are wired to a constant-current power supply using a ribbon cable.

3.2 Experimental Methods

3.2.1 Test Chip Calibration

The RTDs patterned directly on the microchannel plate were calibrated in a laboratory oven at temperatures spanning the operational range. A Pt100 RTD (PR-10-3-100, Omega) was placed in the oven with the test chip and was used as the reference temperature for the calibration. A linear regression was used to interpolate the temperature-dependence of electrical resistance and develop a unique calibration for each of the nine sensors. Heat flux uniformity across the chip was estimated by measuring the resistance of each of the nine individual heaters at ambient temperature prior to testing. The resistance variation across the chip surface was measured to be less than 1 %

for all samples, and hence, variations in heat flux would be negligible when fixing the voltage drop across the heaters during testing.

The heat lost by natural convection and radiation from the test vehicle assembly, Q_{loss}, was estimated by applying a heat input via the serpentine heaters on the chip without any fluid in the test section. Once the system reached a steady-state condition, the temperature of each RTD on the chip surface was recorded. The temperatures were then averaged spatially and temporally to determine the average chip temperature, $T_{chip,avg}$. This procedure was repeated for heat inputs that resulted in a range of chip temperatures experienced during the experiments. A best-fit line to the temperature-dependent heat loss in the test setup used in this work gave the equation: $Q_{loss} = 0.02576\ (T_{chip,avg} - 21.52)$.

3.2.2 Flow Loop

A flow loop (Figure 3.7) was constructed to facilitate evaluation of the chip temperature rise and pressure drop across the heat sink array for a specified channel mass flux and fluid temperature at the test section inlet. A reservoir with an adjustable volume contains excess fluid and sets the system pressure during testing; cartridge heaters installed in the reservoir are used to vigorously boil the working fluid prior to testing. A magnetically-coupled gear pump (GB-P23, Micropump) circulates fluid through the test section and the fluid mass flow rate is measured using a Coriolis mass flow meter (CMF010M, Micromotion). The test section inlet and outlet gage pressures are measured in the manifold base (Figure 3.2) with pressure transducers (S-10, WIKA) and the pressure drop across the test section is measured with a differential pressure transducer (PX2300, Omega). Inlet and outlet temperatures are measured using T-type thermocouples (Figure 3.2). The fluid temperature at the test section inlet is controlled using an inline heater. Fluid exiting the test section is cooled using a liquid–liquid heat exchanger and then returned to the reservoir.

3.2.3 Test Procedure

Performance of the test vehicle was evaluated at three channel mass fluxes: 1300 kg/m²s, 2100 kg/m²s, and 2900 kg/m²s for each of the three channel geometries. Table 3.2 shows the volumetric flow rates and Reynolds numbers ($Re = d_H G/\mu$) for each case. Fluid flow rates ranged

from 19 mL/min to 540 mL/min, with channel Reynolds numbers between 71 and 238; the low Reynolds numbers result from the extremely small hydraulic diameters of the channels tested.

Prior to testing, dissolved noncondensable gas (viz., air) was removed from the working fluid, HFE-7100, via vigorous boiling of fluid in the reservoir and subsequent recollection of condensate. Removing the dissolved gasses from dielectric fluids is critical to achieving repeatable and predictable results during two-phase testing [59]. Once degassed, fluid was circulated at the desired mass flux, and the volume of the reservoir was adjusted to maintain an outlet pressure of 123 kPa. The power to the preheater was adjusted to maintain an inlet temperature of 59 °C (7 °C below the saturation temperature at the test section outlet). Power to the test chip heater was incremented from zero until a maximum chip temperature of ~125 °C was reached. This temperature limit was chosen conservatively to guarantee that the heaters and wire bonds were not damaged during testing. For some of the experiments, the heater power was shut off due to critical heat flux being reached where a sudden temperature excursion was observed (*i.e.*, the chip temperature spiked suddenly, or slowly increased with time without reaching a steady-state value). Other experiments reached steady-state operating points at chip temperatures near 120 °C; heat fluxes that would lead to higher chip temperatures were not attempted to avoid the risk of damage to the test vehicle. Once steady-state conditions were reached for a fixed power level, the data were collected at a rate of 6000 Hz for 2 min. These data were time-averaged to yield a single steady-state data point corresponding to each power level. All data are collected using a National Instruments data acquisition (DAQ) system (cDAQ-9178, National Instruments) and are monitored and recorded through a LabVIEW interface.

3.2.4 Data Reduction

Electrical power supplied to the serpentine heaters, P_{el}, was calculated using the measured voltage and current. The net heat input was calculated by subtracting the heat loss, Q_{loss}, from the supplied electrical power as $Q_{net} = P_{el} - Q_{loss}$. The heat flux, q''_{base}, was calculated by dividing the total heat input by the base footprint area, A_b. The effective overall thermal resistance, R_{eff}, was calculated based on the average chip temperature rise above the fluid inlet temperature, $T_{fl,in}$

$$R_{eff} = \frac{A_b \left(T_{chip,avg} - T_{fl,in} \right)}{Q_{net}}. \tag{3.1}$$

This represents an effective resistance that includes the caloric resistance of the fluid and conduction resistance through the channel base.

The heat transfer coefficient was estimated using:

$$h_{wall} = \frac{Q_{net}}{\eta_o A_{wet}\left(T_{base,avg} - T_{fl,ref}\right)}. \tag{3.2}$$

To calculate the fluid reference temperature, the thermodynamic quality of the fluid at the channel exit was calculated using an energy balance:

$$x_{out} = \frac{Q_{in} - \dot{m} c_p \left(T_{fl,out} - T_{fl,in}\right)}{\dot{m} h_{fg}}. \tag{3.3}$$

For heat fluxes at which $x_{out} \leq 0$, T_{ref} is taken as the average of the fluid inlet and outlet temperatures. For $x_{out} > 0$, the location where the saturation temperature is reached, z_{sat}, is estimated using an energy balance; the fluid temperature is assumed to increase linearly up to the local saturation temperature at z_{sat} and decrease as the local pressure decreases along the remaining length of the channel. For this calculation, the pressure drop in the channel is assumed to be linear throughout and the heat flux is uniform along the length of the channel. The reference temperature is calculated by taking a length-weighted average of these temperatures:

$$T_{ref} = \begin{cases} \dfrac{T_{fl,in} + T_{fl,out}}{2} & ,if\ x_{exit} \leq 0 \\ \left(\dfrac{T_{fl,in} + T_{sat,x_{sat}}}{2}\right)\dfrac{z_{sat}}{L} + \left(\dfrac{T_{sat,x_{sat}} + T_{sat,out}}{2}\right)\dfrac{\left(L - z_{sat}\right)}{L} & ,if\ x_{exit} > 0 \end{cases} \tag{3.4}$$

The temperature at the base of the channels is calculated accounting for conduction resistances across the heat sink base layers as:

$$T_{base,avg} = T_{chip,avg} - \frac{Q_{net}}{A_b}\left(\frac{d_b}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}}\right) \tag{3.5}$$

Overall surface efficiency is defined as:

$$\eta_0 = 1 - \frac{NA_f}{A_{wet}}\left(1 - \eta_f\right), \tag{3.6}$$

where η_f is the fin efficiency and is defined as:

$$\eta_f = \frac{\tanh\left(md_c\right)}{md_c}, \quad \text{where} \quad m = \sqrt{\frac{2h_{wall}}{k_{Si} w_f}}. \tag{3.7}$$

The heat transfer coefficient is first solved assuming a fin efficiency of unity; fin efficiency is then iterated until the calculated heat transfer coefficient value converged.

3.2.5 Uncertainty

The measurement uncertainties of each instrument in the experimental test facility are listed in Table 3.3. The listed uncertainties were obtained from the manufacturers' specifications sheets except in the case of the custom RTDs; the uncertainties for the chip temperatures were conservatively estimated using the accuracy of the reference RTD used for the calibration, the linearity of the sensor calibration, and the repeatability of the sensors over time. The uncertainties of calculated values were determined using the method outlined in Ref. [60] and are also listed in Table 3.3. The maximum uncertainties in heat flux, effective thermal resistance, and heat transfer coefficient occur at low heat fluxes (and low chip temperatures) and generally decrease with increasing heat flux.

3.3 Results and Discussion

3.3.1 Temperature Distribution Across the Test Chip

Figure 3.8 shows the steady-state temperatures measured across the chip surface by the nine RTDs, each located near the center of the corresponding heat sink, and the average chip temperature, for the 15 μm × 150 μm channels (Sample B) at a mass flux of 1300 kg/m²s. At low heat fluxes (< 75 W/cm²), the heat input is less than the value required to reach the saturation temperature; the working fluid therefore remains in a liquid state at the outlet (*i.e.*, in the single-phase regime). The temperature variation remains below 3 °C in the single-phase regime, which can be attributed to uniform fluid delivery to each heat sink by the hierarchical manifold during single-phase operation. As heat flux is further increased, boiling is initiated in each zone (not necessarily simultaneously). Outlet flow in the manifold is monitored for vapor to visually confirm two-phase operation. While flow inside the channel cannot be monitored directly, the onset of boiling at different locations can be inferred from small (~1-2 °C), sudden drops in the local transient chip temperature data, due to the excess superheat required for vapor nucleation in highly wetting fluids. For the data shown in Figure 3.8, for example, vapor was first seen in the manifold at 100 W/cm², and the individual RTDs showed signatures of boiling onset for a range of heat fluxes between 100 W/cm² and 175 W/cm². Despite this spatially non-uniform onset of boiling,

the RTD temperatures remain relatively consistent across the chip surface (<5 °C variation) up to 220 W/cm². As the heat flux is further increased, the chip temperature variation increases. The spatial non-uniformity becomes severe at the highest heat fluxes; for example, at the maximum heat flux of 410 W/cm² in Figure 3.8, the temperatures on the chip ranged from 95 °C to 122 °C.

This experiment was discussed as a representative case and similar trends are observed for all test chips and flow rates. Chip temperatures are relatively uniform in single-phase operation and for a range of heat fluxes beyond incipience. The chip temperatures steadily diverge as heat flux is further increased, with the maximum temperature variation occurring at the highest heat flux tested. For a single test chip, the pattern of the temperature non-uniformity remains consistent (*e.g.*, the highest temperature location remains the same for all mass fluxes). However, the locations change for each different sample (*e.g.*, the highest temperature location is not the same for Sample A as it is for Sample B or Sample C). Therefore, the temperature divergence is attributed to manufacturing variations and assembly tolerances in the manifold, which are exacerbated in the two-phase regime, rather than to inherent flow maldistribution due to the manifold design.

3.3.2 Boiling Curves

The boiling curves for each different channel geometry at mass fluxes of 1300, 2100, and 2900 kg/m²s are shown in Figure 3.9. Single-phase fluid is delivered to the heat sink array at an inlet temperature 7 °C below the saturation temperature of the fluid based on the outlet pressure. For low heat fluxes, the fluid remains in a single-phase state through the channel length, resulting in a linear temperature rise with increasing heat flux. The slope of the boiling curve in the single-phase region increases with increasing mass flux and channel depth; increasing channel depth provides more surface area for heat transfer while increasing mass flux provides higher inlet velocities and longer developing flow length. The heat input required to reach the saturation temperature increases with increasing fluid flow rates, which results in the single-phase regime being extended to higher heat fluxes for deeper channels and larger mass fluxes. It has been observed in the literature that increasing mass flux leads to increased wall superheats at incipience in straight microchannels [55]. This trend is also observed in the current system, where all three samples begin boiling at chip superheats of 8 – 10 °C for a mass flux of 1300 kg/m²s and 14 – 22 °C for a mass flux of 2900 kg/m²s.

Boiling incipience in the channels results in an increase in slope of the boiling curve; this increase is most dramatic for low mass fluxes where the convective heat transfer is weakest. The boiling curves do not show a sharp transition at the onset of boiling due to the many parallel flow paths that each boil at slightly varying heat fluxes as described in Section 4.1. Sample A (15 μm × 35 μm), which has the shallowest channels and, therefore, the least wetted area, has significantly higher chip temperatures at any given base heat flux or mass flux, and reaches CHF at a much lower heat flux. For low heat fluxes, the temperature rise for Sample C (15 μm × 300 μm) is consistently lower than that for Sample B for a given mass flux and heat flux (except for one region where Sample B (15 μm × 150 μm) entered the two-phase region before Sample C), which can be attributed to the increased wetted area of Sample C. In absolute terms, the temperatures for Sample C and Sample B remain close at low heat fluxes. For example, at a mass flux of 1300 kg/m²s, Samples B and C yield chip temperatures within 5 °C of each other for heat fluxes up to 200 W/cm²; for mass fluxes of 2100 kg/m²s and 2900 kg/m²s, chip temperatures remained within 5 °C of each other up to 600 W/cm² and 500 W/cm², respectively.

The performance of Samples B and C begin to deviate from each other at higher heat fluxes, and this difference in performance is most pronounced where Sample B reaches its lower critical heat flux. For example, the highest heat flux dissipated by Sample B at a mass flux of 1300 kg/m²s is 410 W/cm² and results in a chip temperature rise of 34 °C; at this same heat flux, the chip temperature rise is only 21 °C at a mass flux of 2900 kg/m²s. The maximum heat flux dissipated increases significantly with increasing mass flux, especially for Samples A (15 μm × 34 μm) and B (15 μm × 150 μm) that were tested to CHF; this trend is not as apparent for Sample C (15 μm × 300 μm) because testing was stopped due to a temperature cut-off being reached before CHF. Maximum heat flux dissipation also increases significantly with channel depth, as shown in Table 3.4, which lists the maximum heat fluxes dissipated for each of the experiments. Critical heat flux has been shown to scale with mass flux and wetted area during flow boiling in straight microchannels [8]. Harirchian and Garimella [56] found that the suppression of nucleate boiling and partial wall dryout lead to decreased heat transfer at high heat fluxes in straight microchannels, which leads to increased wall temperatures; this mechanism has been found to occur at large wall heat fluxes ($q''_w = Q_{net}/(A_w*N)$) and large boiling numbers ($Bl = q''_w/(G*h_{fg})$). For a given base heat flux, the wall heat flux decreases with increasing channel depth, which in turn leads to a decrease in boiling number; boiling number also decreases with increasing mass flux, leading to a

higher CHF. These trends are both seen in Figure 3.9 where CHF increases for increasing channel depth (decreasing wall heat flux) and increasing mass flux (decreasing boiling number).

3.3.3 Heat Transfer Coefficient

Wall heat transfer coefficient, calculated using the procedure detailed in Section 3.4, as a function of outlet thermodynamic quality for mass fluxes of 1300, 2100, and 2900 kg/m²s is illustrated in Figure 3.10. In general, heat transfer coefficients remain relatively constant throughout the single-phase regime ($x_{out} < 0$) for a fixed channel geometry and mass flux. Single-phase heat transfer coefficient shows a strong dependence on mass flux, where increasing mass flux results in an increased single-phase heat transfer coefficient for all three channel geometries. Ryu *et al.* [28] found that the local heat transfer coefficient along the length of manifold microchannel heat sink channels is strongly dependent on the inlet jet region and the region immediately downstream of the inlet where the thermal boundary layer is smallest in thickness and developing. They also found that the boundary layer is developing for a significant portion of the total flow length for manifold microchannel heat sinks of similar dimensions as the current study. Therefore, it is expected that heat transfer coefficient would strongly depend on inlet velocities and channel mass fluxes. A clear correlation between the channel cross section and single-phase heat transfer coefficient is not seen here for the channel geometries tested.

Once boiling is initiated ($x_{out} \approx 0$), and heat is also removed by phase-change, the heat transfer coefficients increase. For a fixed mass flux, all three samples have similar heat transfer coefficients in the low-quality regime ($0 < x_{out} < 0.1$); for highly confined two-phase flows in small hydraulic diameter channels, such independence of the heat transfer coefficient on channel geometry has been shown in straight, parallel channels for low wall heat fluxes [56]. In this region, heat transfer coefficients steadily rise with increasing outlet quality as film thicknesses decrease and mean velocities increase due to increased vapor generation. Table 3.4 lists the maximum heat transfer coefficient calculated for each experiment. For Sample A (15 μm × 35 μm), the maximum two-phase heat transfer increases significantly with mass flux. For deeper channels (Samples B and C), this trend is not observed and maximum heat transfer coefficient remains nearly constant for all mass fluxes tested.

At higher outlet qualities ($x_{out} > 0.1$), the slope of the boiling curve begins to reduce, leading to a decrease in heat transfer coefficient. This degradation of performance is triggered by vapor

blanketing causing local and intermittent dryout at the wall, and has been previously observed in flow boiling experiments for microchannels [57], [58]. Because the hydraulic diameter of all three channel geometries is of the same order of magnitude as the bubble departure diameter, the flow is expected to be highly confined; boiling starts in the confined slug regime at the onset of boiling and transitions to annular flow at higher heat fluxes [59]; this can cause intermittent dryout at relatively low qualities after incipience. The heat transfer coefficient declines more gradually for lower mass fluxes, which is also consistent with behavior observed in straight, parallel microchannels [60]. Critical heat flux occurred between outlet qualities between 0.18 and 0.28 for Samples A and B; Sample C, which did not reach CHF, exhibited significantly lesser degradation in heat transfer coefficients, even at heat fluxes above 900 W/cm².

3.3.4 Effective Thermal Resistance

Figure 3.11 shows the calculated effective thermal resistance as a function of exit thermodynamic quality. For all mass fluxes tested, thermal resistance values for Sample A (15 μm × 35 μm) are significantly larger than those for Samples B and C and are therefore shown on a different scale in the top row of Figure 3.11. This difference can be attributed to the significantly reduced wetted area for Sample A. Note that the conduction thermal resistance through the silicon base is slightly different for each sample due to differences in base thicknesses; the resistances due to conduction for Samples A, B, and C are 1.5×10^{-6}, 1.2×10^{-6}, and 0.73×10^{-6} m²K/W, respectively. These values contribute 2 – 7 % of the total effective thermal resistance for Sample A, 9 – 16 % for Sample B, and 8 – 13 % for Sample C.

For a fixed channel geometry and mass flux, because the conduction resistance is constant and the heat transfer coefficient remains relatively constant in the single-phase regime, the effective thermal resistance is also relatively constant. Figure 3.11 shows that single-phase thermal resistance decreases with increasing mass flux and channel depth, which agrees with prior studies of manifold microchannel heat sinks [30], [32], [37]; in these studies, the largest contribution to the decrease was the reduced temperature rise of the fluid with increasing flow rates, especially at low flow rates. In the current study, it is difficult to separate the impingement and developing flow effects from the decrease in caloric resistance, which would all contribute to a lower thermal resistance with increasing flow rates. Similarly, the decrease in thermal resistance with channel depth can also be attributed to the increase in wetted area.

The increase in heat transfer coefficient in the low-quality regime ($0 < x_{out} < 0.1$) results in decreased thermal resistances for all channel geometries and mass fluxes. Thermal resistance is found to depend on both channel depth and mass flux, especially for shallow channels. Comparing Sample B (15 μm × 150 μm) to Sample A (15 μm × 35 μm), for a 77% decrease in wetted channel area, the minimum thermal resistance increases 160% from 7.66×10^{-6} m²K/W to 19.9×10^{-6} m²K/W. Sample C (15 μm × 300 μm) has a minimum thermal resistance of 5.60×10^{-6} m²K/W, a 27% decrease compared to Sample B for a 100% increase in surface area. Deeper channels provide diminishing return due to the decreased fin efficiency for deep channels (as low as 58 % for Sample C), making the added heat transfer area less effective.

The decreases in thermal resistance from single-phase to two-phase operation are more drastic at low fluid mass fluxes where the single-phase thermal resistance is greater. As mass flux is increased, single-phase convective thermal resistance decreases, but thermal resistances in the two-phase regime are largely unchanged. For higher exit qualities, the thermal resistance increases, mirroring the heat transfer coefficient trends at high exit qualities. The increase is not observed for Sample C because the experiments were terminated (due to the chip temperature limit) while the quality was relatively low.

3.3.5 Pressure Drop

The pressure drop as a function of heat flux is plotted in Figure 12. This differential pressure includes contraction into and expansion out of the channels as well as flow splitting and contraction/expansion resistances in the manifold.

For each experiment, pressure drop remains relatively constant in the single-phase region. In conventional microchannels, single-phase pressure drop scales with L/d_H^2, which would result in the shallowest channels having the highest pressure drop; however, it is observed that the pressure drops for the deeper channels (which also have larger hydraulic diameters) are larger for a given channel mass flux. While the channel velocities are equal for all channel geometries at a fixed mass flux, the velocities in the manifold are not constant because the manifold dimensions remain the same for all channel geometries. This results in the deeper channels (which have higher flow rates for a fixed mass flux) having higher pressure drops due to higher fluid velocities in the manifold. To approximate the contribution of the flow in the manifold to the overall pressure drop, a first-order estimate of the pressure drop in the channel was made assuming fully developed,

laminar flow in a pipe [61] with the length equal to the center-to-center distance of the manifold inlets and outlets (*i.e.*, 650 μm). These values were then subtracted from the measured total pressure drop for each experiment to estimate the manifold pressure drop. The estimated manifold pressure drops were then plotted as a function of flow rate and a quadratic polynomial was fit to the data with the intercept forced to zero; the resulting fit had an R^2 value of 0.97. For the flow rates delivered to Sample A (19 – 42 mL/min), the manifold pressure drop is only ~0.1 – 0.5 kPa; this increases to ~4 – 20 kPa for Sample B (115 – 245 mL/min) and ~20 – 100 kPa for Sample C (245 – 540 mL/min). These first-order estimates provide insight into the relative contribution of the manifold to the total pressure drop. For the highest flow rates tested, as much as 90% of the total single-phase pressure drop is estimated to come from losses due to sudden expansions, sudden contractions, and flow friction in the manifold; at the lowest flow rates tested, the relative contribution of the manifold to the total pressure drop is negligible (<2% for all flow rates for Sample A).

After entering the two-phase regime, the pressure drop monotonically increases; this is caused by the increase in velocity with increasing vapor quality and boiling occurring further upstream in the channel at higher heat fluxes. For a fixed mass flux, the slope of the pressure drop curve is steeper for the shallower channels. This occurs because pressure drop largely depends on flow quality, and shallower channels have a higher quality for a given base heat flux.

3.3.6 Conclusions

Two-phase, intrachip manifold microchannel heat sinks were successfully designed, fabricated and tested. Each test vehicle used a hierarchical manifold to feed an array of microchannel heat sinks with high-aspect-ratio channels. The nominal channel depth test vehicles A, B, and C were: 35 μm, 150 μm, 300 μm, respectively, while the nominal channel width was 15 μm for all three samples. A heated chip area of 5 mm × 5 mm was cooled by a discretized 3 × 3 grid of microchannel heat sinks. Each heat sink contained a bank of 50 microchannels; because the manifold directs flow into the center of the channels and out of both ends, the effective flow length in any flow passage is 750 μm.

The single-phase heat transfer coefficient was found to increase with increasing channel mass flux, which was attributed to impingement and developing flow effects. In the two-phase regime, heat transfer coefficient strongly depends on exit quality and weakly depends on channel

depth and mass flux. For all channel depths and mass fluxes, heat transfer coefficient increases with increasing exit quality until a maximum is reached; after this point, the heat transfer coefficient decreases with exit quality until critical heat flux is reached. These trends match the general trends experienced in traditional microchannel heat sinks. The heat sink with the smallest channel depth (Sample A, 15 μm × 35 μm) provided the highest heat transfer coefficient, 43,300 W/m²K, at a mass flux of 2900 kg/m²s and an exit quality of 0.16. The maximum heat transfer coefficients for Samples B (15 μm × 150 μm) and C (15 μm × 300 μm) were 31,000 W/m²K (G = 1300 kg/m²s, x_{out} = 0.22) and 29,000 W/m²K (G = 2200 kg/m²s, x_{out} = 0.14).

Effective thermal resistance was found to decrease with increasing channel depth and increasing mass flux. While the heat sink with the smallest channel depth provided the highest heat transfer coefficients, it also provided the highest thermal resistance due to the significantly reduced wetted area compared to the deeper channels. The decrease in thermal resistance provided by increasing the mass flux was minimal compared to the significant increase in pressure drop for deep channels. For a 150 μm channel depth, the minimum thermal resistance decreased from 9.2×10^{-6} m²K/W to 7.7×10^{-6} m²K/W while pressure drop increased from 41 kPa to 112 kPa when mass flux was increased from 1300 kg/m²s to 2900 kg/m²s. However, increasing the mass flux did increase the maximum heat flux dissipated from 411 W/cm² to 705 W/cm². The cooling approach provided a minimum effective heat sink thermal resistance of 5.6×10^{-6} m²K/W for the sample with channel depths of 300 μm at a mass flux of 2900 kg/m²s.

This work successfully demonstrated fabrication, heterogeneous integration, and characterization of hierarchical manifold microchannel heat sinks operating in the two-phase regime. Intrachip cooling using small hydraulic diameter, high-aspect-ratio microchannels is shown to dissipate extreme heat fluxes over a 5 × 5 mm heated area. Heat fluxes up to 910 W/cm² were dissipated at pressure drops less than 162 kPa and chip-to-fluid inlet temperature rises less than 47 °C using 15 μm × 300 μm channels. The maximum heat fluxes dissipated for heat sinks with 15 μm × 150 μm and 15 μm × 35 μm channels were 705 W/cm² and 142 W/cm², respectively.

Table 3.1. Summary of microchannel test sample dimensions.

Sample	w_c {μm)	d_c (μm)	d_H (μm)	AR (-)	A_c (μm^2)	A_{wet} (μm^2)
A	12.0	34	19.6	2.7	360	5.59×10^4
B	14.7	153	28.8	10.4	2275	2.41×10^5
C	16.2	310	31.7	19.1	5000	4.83×10^5

Table 3.2. Experimental operating conditions.

Sample	G (kg/m²s)	Flow Rate (mL/min)	Re (-)
A	1300	19	71
	2100	31	112
	2900	42	147
B	1300	115	97
	2100	178	156
	2900	245	216
C	1300	240	107
	2100	395	172
	2900	540	238

Table 3.3. Uncertainty in measured and calculated values.

Measured Value	Instrument	Uncertainty
Chip temperature	RTDs (calibrated)	± 1.0 °C
Heater voltage	Voltage divider circuit	± 1.0 %
Heater current	Shunt resistor	± 0.1 %
Fluid inlet temperature	T-type thermocouple (calibrated)	± 0.25 °C
Fluid outlet temperature	T-type thermocouple (calibrated)	± 0.25 °C
Outlet pressure	Gage pressure transducer	± 0.3 kPa
Pressure drop	Differential pressure transducer	± 0.17 kPa
Mass flow rate	Coriolis mass flow meter	± 0.1 %
Calculated Value		**Uncertainty**
Heater flux		± 0.6 – 2 %
Effective thermal resistance		± 5 – 10 %
Heat transfer coefficient		± 7 – 15 %

Table 3.4. Summary of thermal performance metrics for the three channel geometries at each mass flux tested (*experiment stopped due to high steady-state temperature rather than CHF).

Sample	**Mass flux, G (kg/m²s)**	**Maximum heat flux dissipation, q''_{base} (W/cm²)**	**Maximum heat transfer coefficient, h_{wall} (W/m²K)**	**Minimum thermal resistance, R_{eff} (m²K/W)**
A	1300	68.5	33.7×10^3	27.4×10^{-6}
(15 μm × 35 μm)	2100	104	35.9×10^3	24.2×10^{-6}
	2900	142	43.3×10^3	19.9×10^{-6}
B	1300	411	26.9×10^3	9.22×10^{-6}
(15 μm × 150 μm)	2100	641	31.0×10^3	7.73×10^{-6}
	2900	705	30.7×10^3	7.66×10^{-6}
C	1300	761*	28.7×10^3	5.90×10^{-6}
(15 μm × 300 μm)	2100	873*	27.0×10^3	5.83×10^{-6}
	2900	910*	28.2×10^3	5.60×10^{-6}

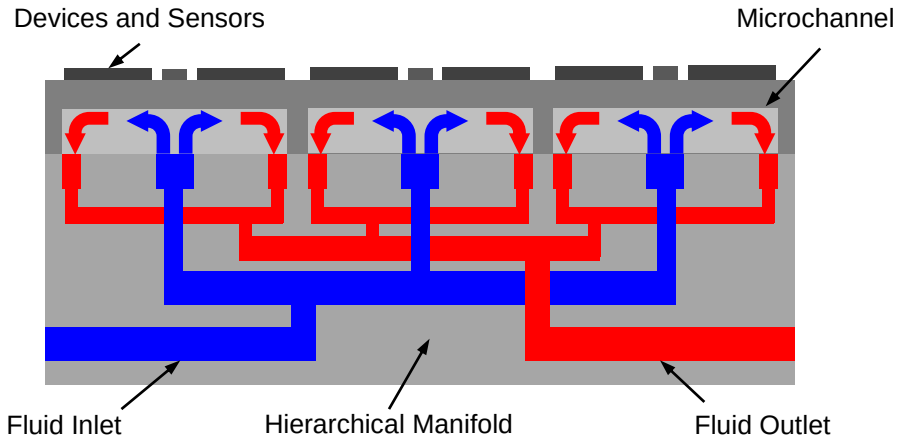


Figure 3.1. Cross-sectional schematic diagram of the hierarchical manifold microchannel heat sink array design concept.

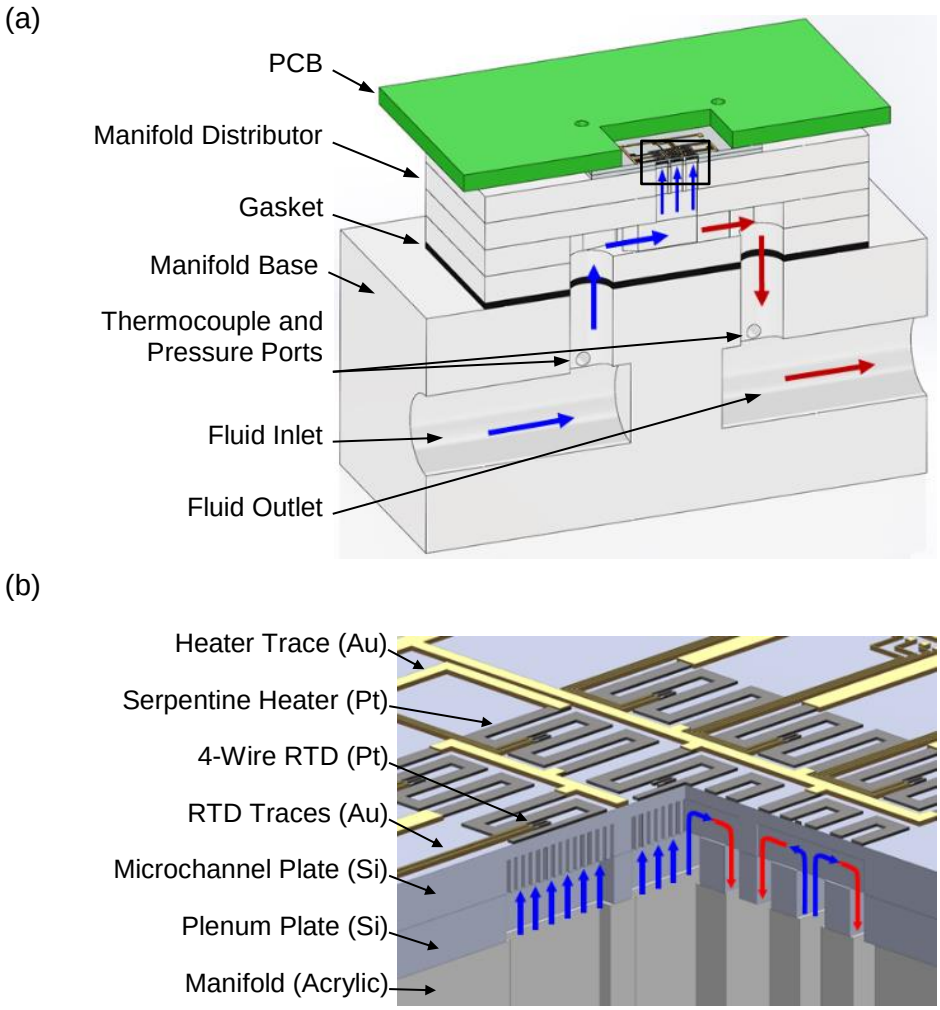


Figure 3.2. (a) Drawing of the thermal test vehicle with half-symmetry section removed to show the fluid flow paths; (b) the inset shows a zoomed in view of the test chip and the fluid flow paths through the microchannels (quarter-symmetry section removed; channels and heater/sensor thicknesses are not to scale).

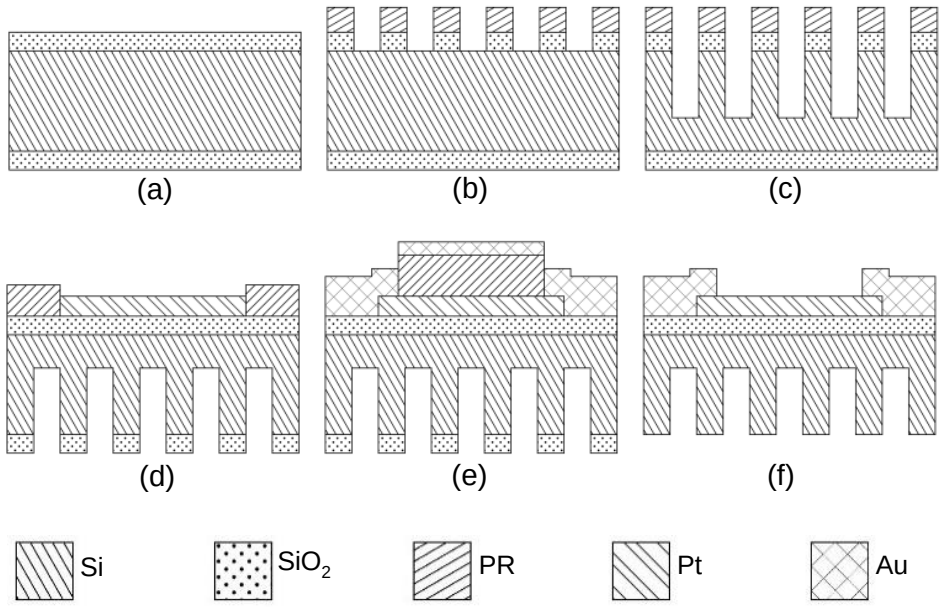


Figure 3.3. Schematic diagram of microchannel plate fabrication: (a) silicon wafer with oxide; (b) exposed and developed PR (Mask #1, channels) and oxide dry-etched; (c) silicon dry-etched; (d) PR stripped from channel side, PR spun, exposed, and developed on heater-side (Mask #2, heaters/sensors) and sputtered Ti-Pt; (e) exposed and developed PR (Mask #3, lead wire traces) and deposited Ti-Au; and (f) final microchannel plate after lift-off, PR stripped, and channel-side oxide layer removed. (Drawings are not to scale.)

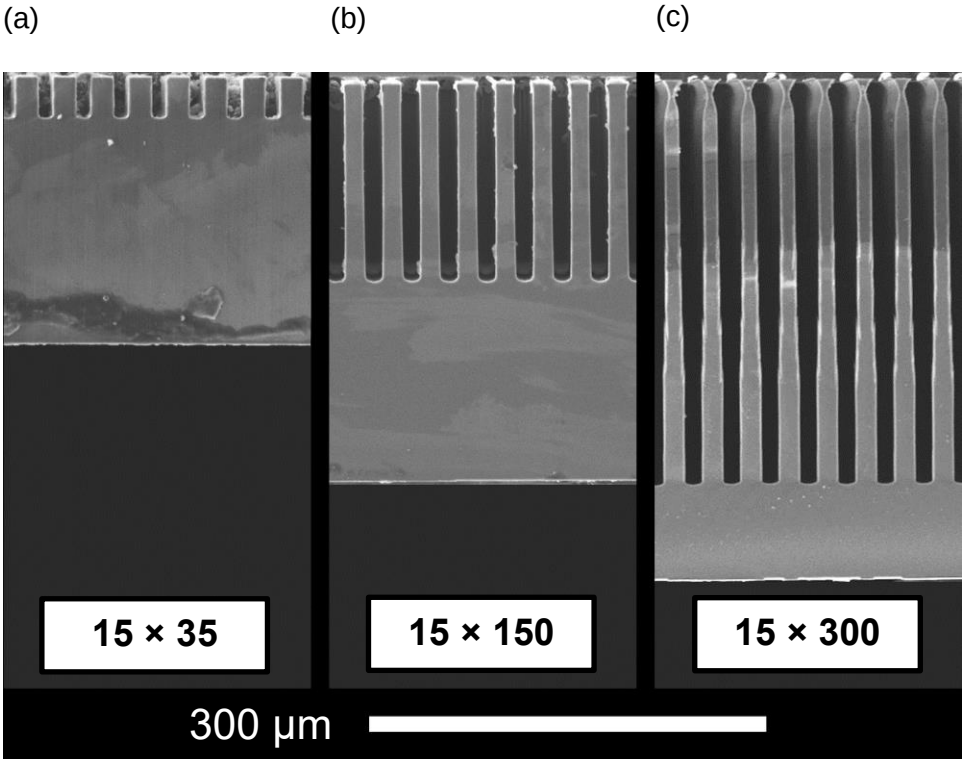


Figure 3.4. SEM images of channel cross-sections for (a) Sample A (15 µm × 35 µm), (b) Sample B (15 µm × 150 µm), and (c) Sample C (15 µm × 300 µm).

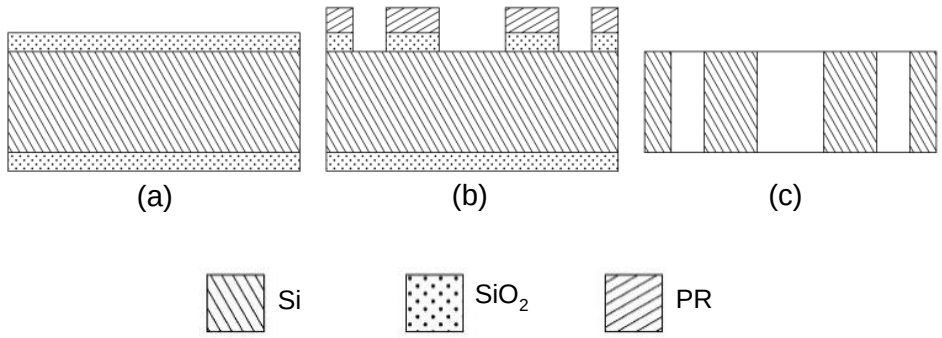


Figure 3.5. Schematic diagram of plenum plate fabrication process: (a) silicon wafer with oxide; (b) exposed, developed PR (Mask #4, plenum), and oxide dry-etch; and (c) final plenum plate after silicon dry-etched through wafer, PR stripped, and oxide removed. (Drawings are not to scale.)

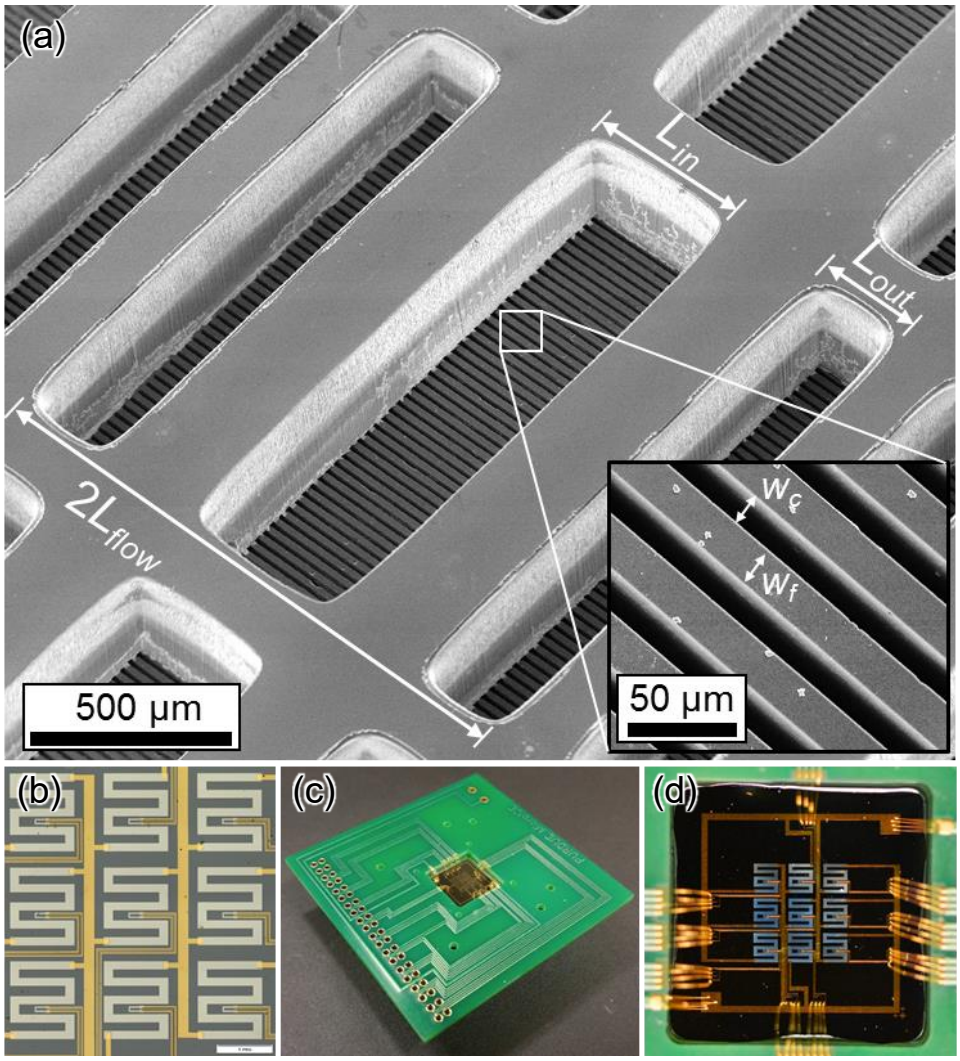


Figure 3.6. (a) SEM image of plenum plate (with bonded microchannel plate underneath) and inset showing zoomed-in view of the exposed top surface of the microchannel plate; (b) microscope image of the serpentine heaters, RTDs, and lead-wire traces on the test chip; (c) photograph of the test chip mounted to the PCB with the heater-side surface face up; and (d) zoomed-in view of the heaters and sensors wire-bonded to the PCB contact pads.

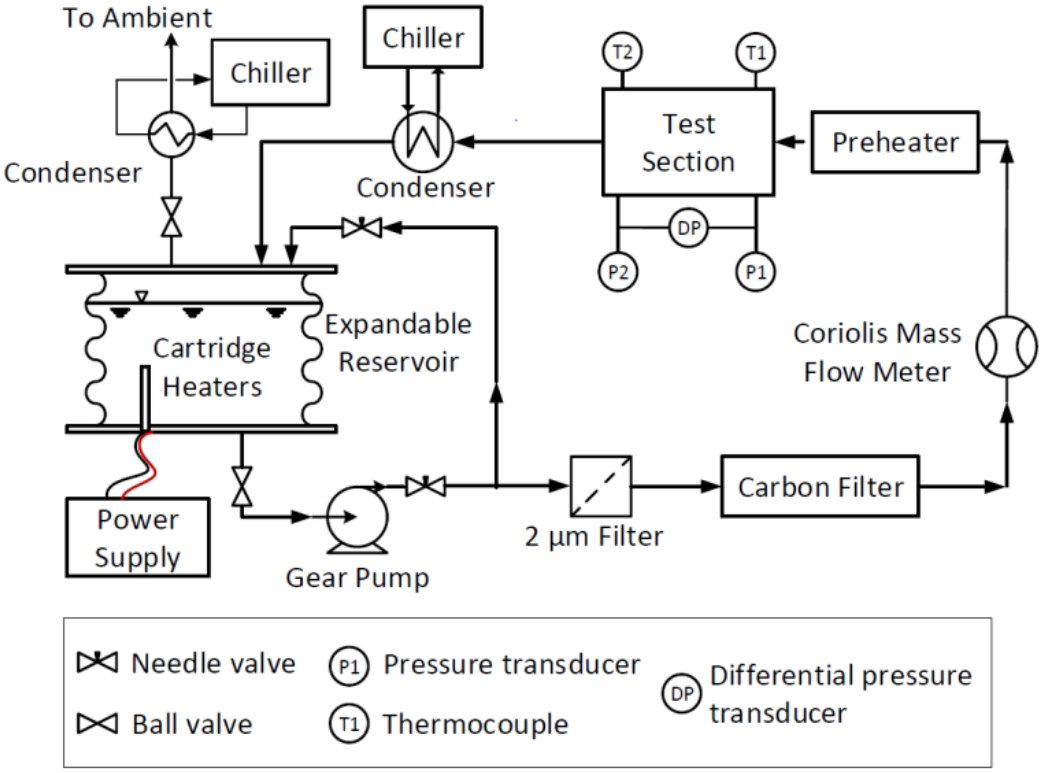


Figure 3.7. Schematic diagram of the flow loop.

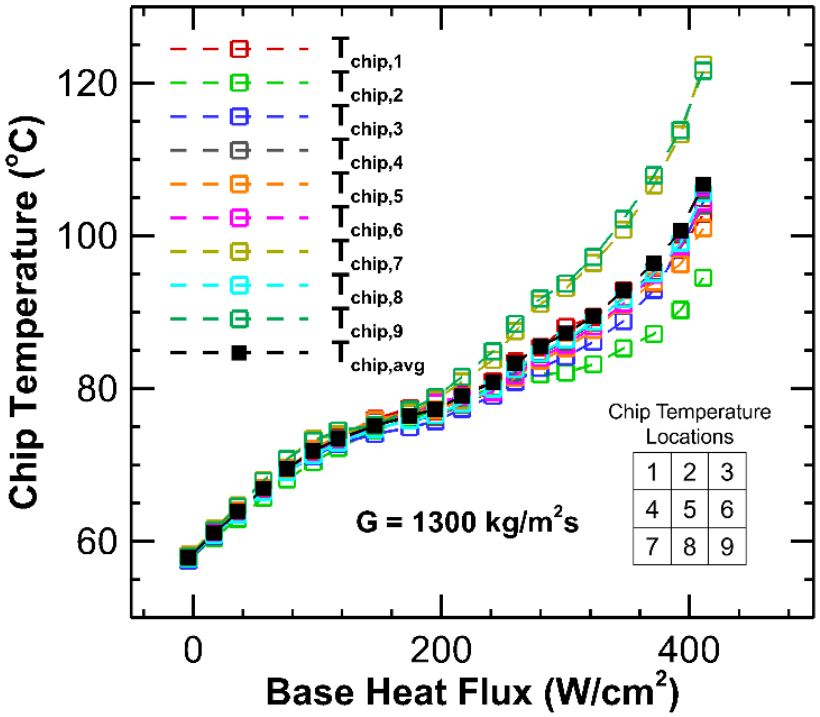


Figure 3.8. Individual temperatures across chip surface as a function of base heat flux for Sample B (15 μm × 150 μm) at G = 1300 kg/m²s.

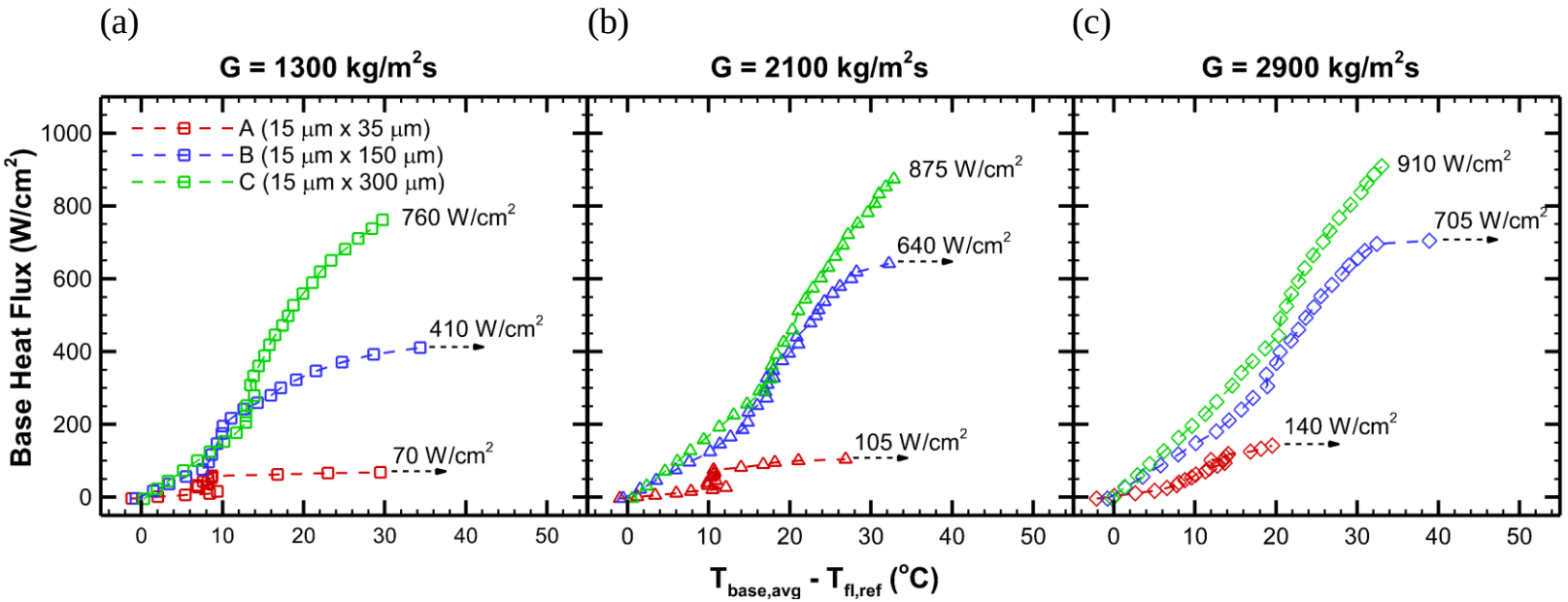


Figure 3.9. Base heat flux as a function of chip temperature rise for all three heat sink arrays at mass fluxes, G, of (a) 1300 kg/m²s, (b) 2100 kg/m²s, and (c) 2900 kg/m²s.

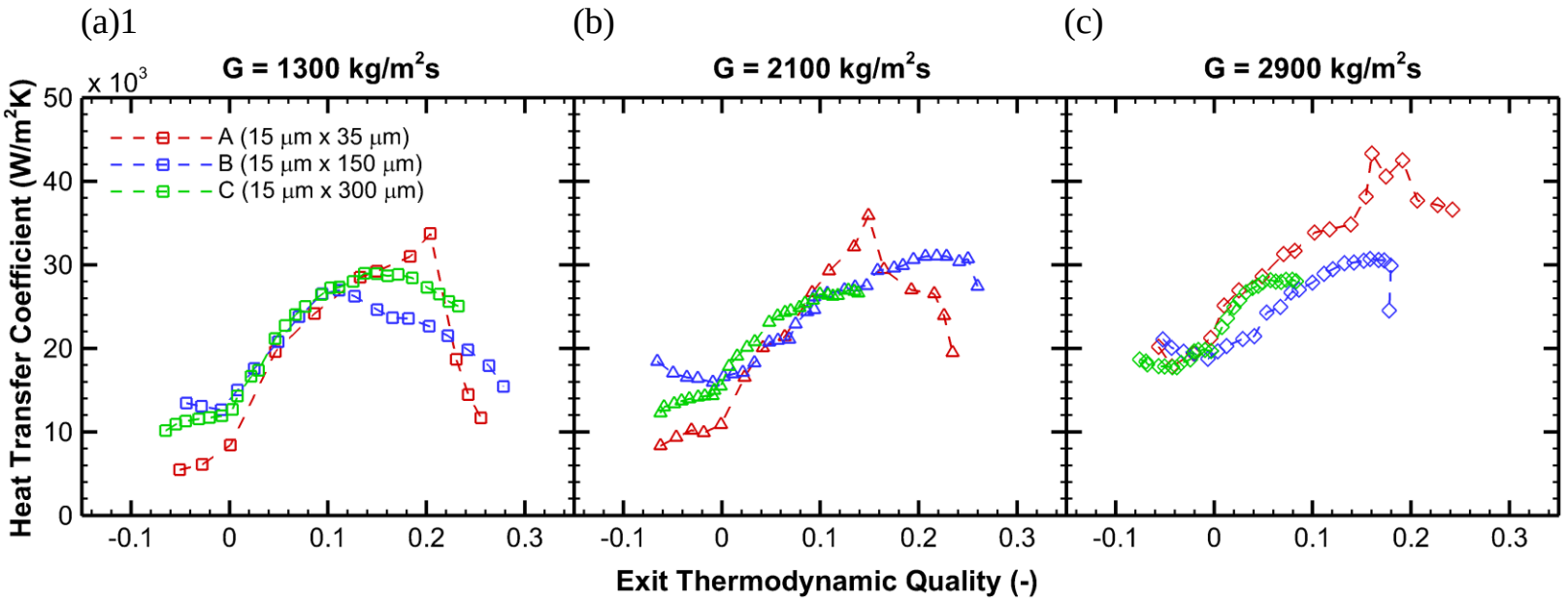


Figure 3.10. Heat transfer coefficient as a function of exit thermodynamic quality at mass fluxes, *G*, of (a) 1300 kg/m²s, (b) 2100 kg/m²s, and (c) 2900 kg/m²s.

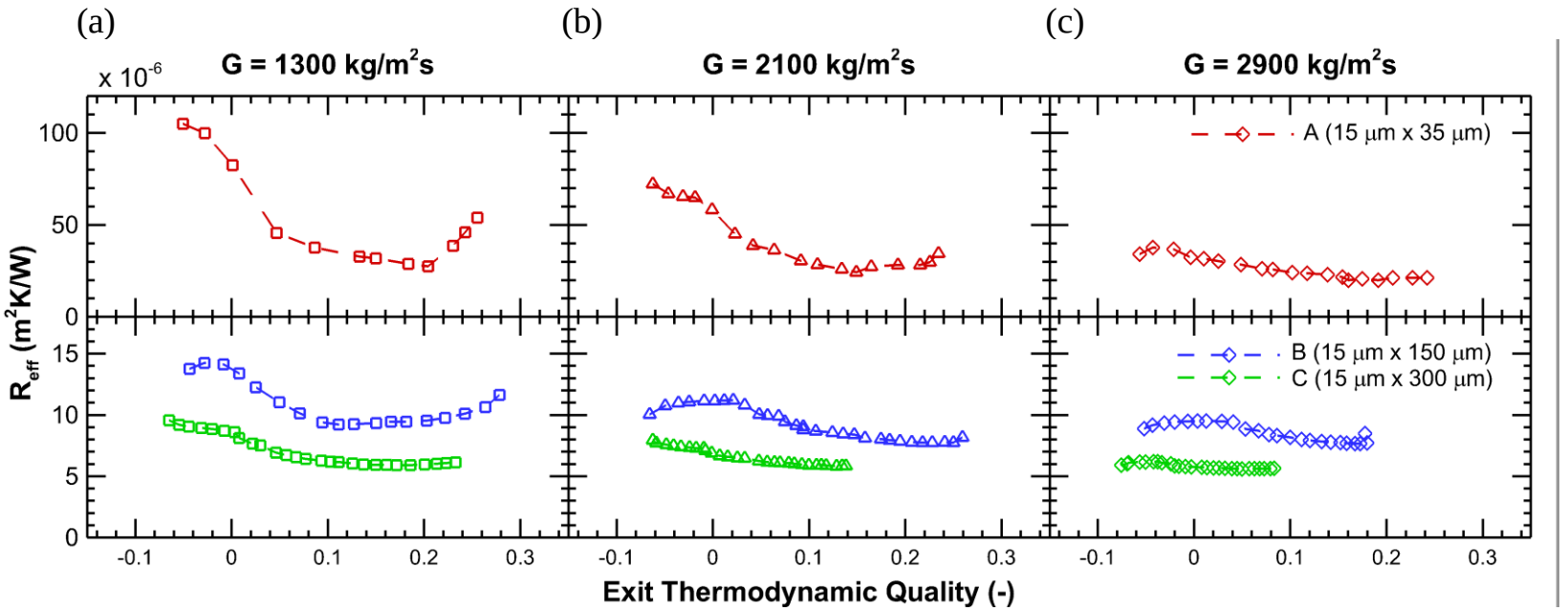


Figure 3.11. Effective thermal resistance as a function of exit thermodynamic quality for mass fluxes, *G*, of (a) 1300 kg/m²s, (b) 2100 kg/m²s, and (c) 2900 kg/m²s; note that the ordinate scale is different for the top and bottom rows of plots.

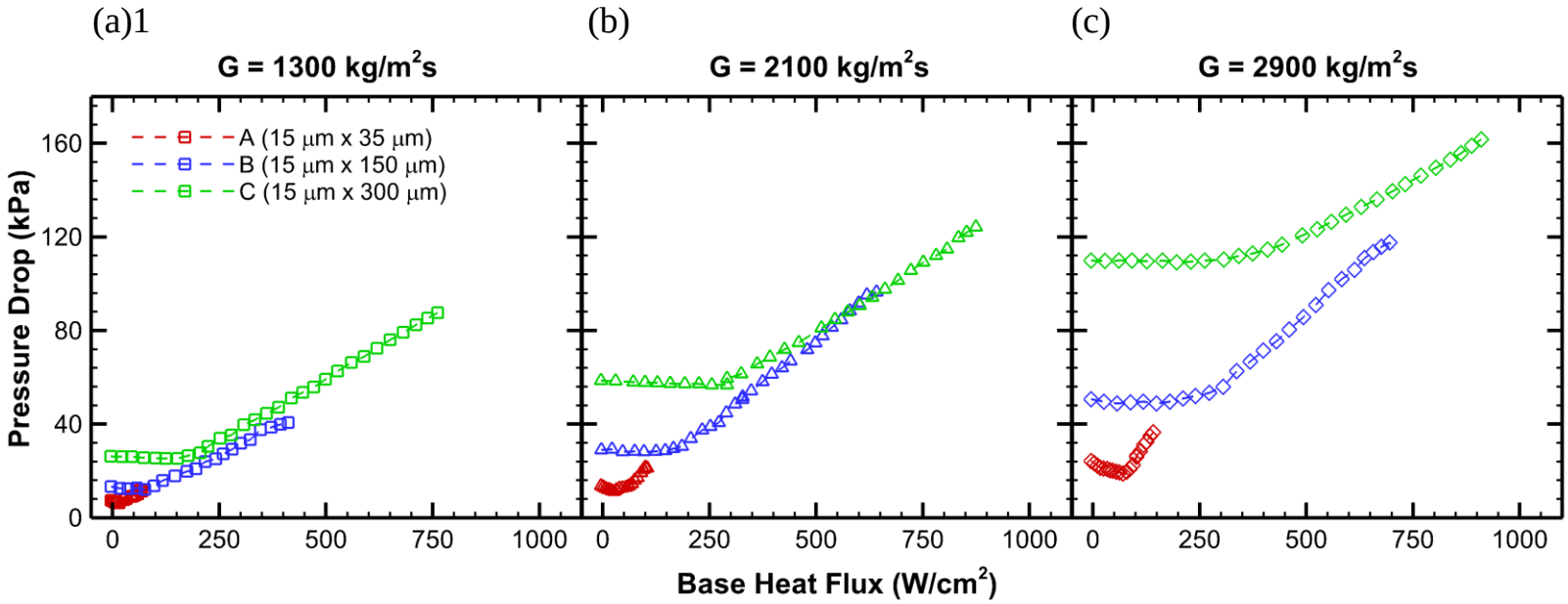


Figure 3.12. Pressure drop as a function of base heat flux for mass fluxes, *G*, of (a) 1300 kg/m²s, (b) 2100 kg/m²s, and (c) 2900 kg/m²s.

4. CHARACTERIZATION OF HIERARCHICAL MANIFOLD MICROCHANNEL HEAT SINK ARRAYS UNDER SIMULTANEOUS BACKGROUND AND HOTSPOT HEATING CONDITIONS

The work in this chapter focuses on further characterizing intrachip heat sink systems that utilize hierarchical manifolds to distribute flow to microchannel arrays during two-phase operation. This work aims to build upon the results presented in Chapter 3 by investigating a broader set of channel geometries that includes channel width variations, as well as subjecting the heat sink to hotspot heat fluxes. The effect of channel dimensions and mass flux are studied for heat sinks with banks of small-diameter, high-aspect-ratio microchannels. Results are presented for the cooling of a uniform background heat flux and with simultaneous background and hotspot heating. The material in this chapter was presented at the *IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)* in 2016 and published in the proceedings [62]. It was later refined and is under review in the International Journal of Heat and Mass Transfer [63].

4.1 Experimental Setup

A thermal test vehicle is fabricated to demonstrate the thermal and hydraulic performance of the hierarchical manifold microchannel heat sink array; Figure 4.2(a) shows the thermal test vehicle with a half-symmetry section removed and Figure 4.2(b) shows a zoomed-in view of the test chip with a quarter-symmetry removed to show the channel features and internal fluid flow paths. The system consists of a manifold base, manifold distributor, plenum interface plate, microchannel plate, and printed circuit board (PCB). The manifold base is used to interface with the flow loop and contains ports for inlet and outlet temperature and pressure measurements. The manifold distributor (Figure 4.2(c-f)) splits the single fluid inlet into nine parallel flow streams that enter the 3 × 3 array of microchannel heat sinks covering the 5 mm × 5 mm chip area; each heat sink covers a footprint area of 1667 μm × 1667 μm with channels covering 1500 μm × 1500 μm; after traveling through the channels, the manifold combines the 18 flow streams into a single fluid outlet. The plenum plate matches the finest-level manifold features and provides smooth

surfaces for sealing between the manifold distributor and the microchannels. The microchannel plate contains the 3 × 3 array of heat sinks, each with a bank of parallel, high-aspect-ratio microchannels; the opposite side of the microchannel plate is instrumented with heaters and sensors to evaluate the thermal performance. The PCB provides a convenient electrical interface to the heaters and sensors (Figure 4.2).

4.1.1 Test Chip Fabrication and Assembly

All fabrication steps were performed in the Birck Nanotechnology Center at Purdue University. This section provides an abbreviated overview of the fabrication steps detailed in Section 3.1.3. While the heater layout and channel dimensions are different in the current work, all fabrication steps are the same.

Starting with a thermally oxidized 4-inch silicon wafer, high-aspect-ratio microchannels were deep reactive-ion etched on one side of a silicon wafer using the Bosch process. On the opposite side of the wafer, heater and sensor features were patterned using a lift-off process. The heaters and resistance temperature sensors (RTDs) consist of a 20-nm layer of Pt deposited on top of a 5-nm seed layer of Ti. The heater and RTD lead-wire traces are a 300-nm thick layer of Au on top of a 5-nm layer of Ti. The silicon dioxide layer was then removed from the channel side of the wafer using a buffered oxide etch. Figure 4.3(a) shows a schematic diagram of the microchannel plate cross-section (features are not to scale). This fabrication process was repeated (while adjusting the channel pattern and etching parameters) to achieve multiple channel geometries; the critical channel dimensions, measured from scanning electron microscopy (SEM) images (Figure 4.4), are summarized in Table 4.1. The listed number of channels, N_c, is for a single heat sink; the total number of channels is calculated by multiplying the number of channels per heat sink by the number of heat sinks, N_{sink}, which is held constant at nine for the current work. The channel cross-sectional area is measured by tracking points on the channel walls and interpolating between the points. Channel wetted area includes the sidewall surfaces, base surface, and surfaces at the ends of the channels ($A_{wall} = P_c L_c + 2w_c h_c$); the wetted area of the manifold is not included because the manifold temperature is expected to be significantly lower than the channels due to contact resistance at the interface. It is worth noting that samples 15×150 and 15×300 were previously characterized in Chapter 3.

Plenum plates were fabricated from separate 4-inch silicon wafers. Features were patterned and deep reactive ion etched with through features; the silicon dioxide layer was then removed using a buffered oxide etch and the wafer was cleaned. A schematic diagram of the final cross-section is shown in Figure 4.3(b).

The 4-inch microchannel wafers were diced into 20 mm × 20 mm dies with the heaters, RTDs, and microchannels occupying the center 5 mm × 5 mm area of the channel wafer. Similarly, the plenum wafers were diced into 20 mm × 20 mm dies with the fluid routing features covering the center 5 mm × 5 mm area.

Figure 4.5(a) shows the layout of the heaters and temperature sensors on the thermal test chip. The background heaters are patterned over nine zones that match the locations of the 3 × 3 grid of microchannel heat sinks on the opposite side. Figure 4.5(b,d) show an example trace layout for a single zone that does not contain the hotspot heater. In each such zone, the heater is composed of nine linear resistors powered in parallel. Lead wires deliver power to each end of the resistors and terminate at two pads located along the periphery of the test chip; these pads are wire-bonded to a printed circuit board (PCB) in the subsequent assembly steps. Two RTDs are patterned in each zone, providing 18 total temperature measurements over the 5 mm × 5 mm chip area. Each four-wire RTD contains two lead wires to supply electrical current and two wires to measure voltage. Figure 4.5(c,e) show the heater layout for the central zone that contains the hotspot. In this zone, the background heater is divided into two parallel arrays of four resistors each, with the hotspot heater positioned tightly in between the background heaters.

A custom printed circuit board (PCB) was designed for connection of the wire-bonded pads to the data acquisition system and to the heater power supplies. The outer edge of the channel plate was fixed to the underside of the PCB using epoxy. All the electrical traces for each of the background heaters, hotspot heater, and 18 four-wire RTDs are wire-bonded to corresponding gold contact pads on the PCB. Figure 4.6 shows photographs of the assembled test chip.

4.1.2 Manifold Fabrication

A multi-layer, hierarchical manifold distributor is used to deliver fluid to the array of microchannel heat sinks. The hierarchical manifold architecture allows for scaling to larger footprint dimensions and smaller inlet and outlet features [18]. The manifold consists of four layers of laser-cut (PLS65MW, Universal Laser Systems) acrylic sheets and an acrylic base, as

shown in Figure 4.2(c-f). The laser-cut layers contain the hierarchical network of channels that distribute flow from a single inlet to the array of heat sinks; these layers are assembled with 100 μm-thick double-sided adhesive sheets (9150, Nitto Denko) that are laser-cut to match the fluid routing features. The acrylic base routes fluid from the flow loop to the bonded sheets and contains ports for inlet and outlet pressure and temperature measurements. A silicone gasket is laser-cut and is used to seal between the acrylic base and manifold layers. One side of the plenum plate is bonded to the manifold using a 10 μm-thick double-sided adhesive (9105, Nitto Denko) that is laser-cut to match the dimensions of the plenum plate; the opposite side of the plenum plate is bonded to the microchannel plate using the same adhesive. The adhesive is aligned on the manifold using guide pins before attaching the test chip.

4.1.3 Test Vehicle Assembly

Stainless steel fittings are inserted into the manifold base for fluid connections to the flow loop and placement of thermocouples and pressure transducers. A PEEK insulation block is used to limit heat lost from the chip to the environment. The heaters that are used to provide the background heat flux are all wired in parallel to a programmable DC power supply (XG100-8.5, Sorensen). A variable resistor is added in series with each heater; during testing, this variable resistor can be adjusted to ensure a uniform background heat flux is generated. The voltage drop across each background heater is measured using a divider circuit to step down the voltage and the corresponding electrical current is measured using a shunt resistor (Y14880R10000B9R, Vishay). The overall electrical current supplied to the background heaters is measured using a shunt resistor (HA-5-100, Empro). The hotspot heater is wired to a separate power supply (1550, B&K Precision); hotspot voltage drop and current were measured in the same manner as the background heater zones. The RTDs were wired to a constant-current power supply and the data acquisition system using a ribbon cable.

4.2 Experimental Methods

The RTDs on the chip surface are calibrated using the same procedure outlined in Section 3.2.1. Heat losses to the environment are also found in Section 3.2.1; the temperature-dependent heat loss for this test chip is: $Q_{loss} = 0.02768 * (T_{chip,avg} - 22.52)$. The two-phase test loop that is detailed in Section 3.2.2 is used to evaluate the chip temperature rise and pressure drop across the heat sink

for a specified fluid mass flux, fluid temperature at the test section inlet, and pressure at the test section outlet.

4.2.1 Test Procedure

Dissolved air is removed from the working fluid, HFE-7100, via vigorous boiling of fluid in the reservoir and subsequent recollection of condensate. The flow loop is then sealed from the environment and degassed fluid is circulated at the desired flow rate; the mass fluxes, flow rates and Reynolds numbers for each sample are shown in Table 4.2. The fluid inlet temperature is maintained at 59 °C and the outlet pressure is maintained at 121 kPa (corresponding to a saturation temperature of 65 °C). Power to the background heaters is increased in small increments from zero to a power at which a maximum RTD temperature reading of 130 °C is reached; testing is ceased at this point to prevent damage to the heaters and wire bonds. Once steady-state conditions are reached for a fixed power level, data are collected at a rate of 6,000 Hz for 2 min. These data are time-averaged to yield a single steady-state data point.

To investigate the effect of a hotspot heat flux on chip temperatures, a fixed uniform background heat flux is applied to the entire 5 mm × 5 mm chip area while the power to the 200 μm × 200 μm hotspot heater is increased in ~550 W/cm² increments up to a heat flux of ~2,700 W/cm². The process is repeated at multiple background heat fluxes. The hotspot heat flux is limited below 3,000 W/cm² to avoid potential electromigration at high current densities.

4.2.2 Data Reduction

The fluid mass flux through each channel is calculated using $G = \dot{m}/(2N_{sink}N_cA_c)$. Electrical power supplied to each of the heaters is calculated using $P_{el,i} = V_i I_i$. The total power supplied to the background heaters, $P_{el,BG}$, is then calculated by summing the power to each of the zones. The net heat input is calculated by subtracting the heat loss from the supplied electrical power as $Q_{net} = P_{el,BG} - Q_{loss}$. The base heat flux, q''_{base}, is calculated by dividing the net heat input by the base footprint area, A_b; similarly, the wall heat flux, q''_{wall}, is calculated by dividing the net heat input by the total channel area $(A_{wall,tot} = N_c N_{sink} A_{wall})$.

The fluid thermodynamic quality at the channel outlet is calculated by:

$$x_{out} = \frac{Q_{in} - \dot{m}c_p\left(T_{sat,out} - T_{fl,in}\right)}{\dot{m}h_{LV}} \tag{4.1}$$

where the latent heat of vaporization is evaluated at the saturation temperature based on the outlet pressure. The effective overall thermal resistance, which represents an effective resistance that includes the caloric resistance of the fluid, conduction resistance through the microchannel base, and resistance due to convection at the channel walls, is calculated based on the base area and the average chip temperature rise above the fluid inlet temperature:

$$R''_{th} = \frac{\left(T_{chip,avg} - T_{fl,in}\right)}{q''_{base}}. \tag{4.2}$$

The contribution of conduction and caloric resistances to the total resistance is calculated using:

$$R''_{cond} + R''_{fluid} = \left(\frac{d_{wafer} - d_c}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}}\right) + \frac{A_b}{2\dot{m}c_p} \tag{4.3}$$

The heat transfer coefficient, which is a measure of the convective heat transfer at the channel walls, is estimated using the channel wetted area and the difference between the average channel base temperature and average fluid temperature:

$$h_{wall} = \frac{q''_{wall}}{\eta_o\left(T_{base,avg} - T_{fl,ref}\right)}, \tag{4.4}$$

For heat fluxes at which $x_{out} \leq 0$, T_{ref} is the average fluid temperature in the heat sink. For $x_{out} > 0$, the location where the saturation temperature is reached, z_{sat}, is estimated using an energy balance; the fluid temperature is assumed to increase linearly up to the local saturation temperature at z_{sat} and decrease as the local pressure decreases along the remaining length of the channel. For this calculation, the pressure drop in the channel is assumed to be linear throughout and the heat flux is uniform along the length of the channel. The reference temperature is calculated by taking a length-weighted average of these temperatures:

$$T_{ref} = \begin{cases} \dfrac{T_{fl,in} + T_{fl,out}}{2} & ,if\ x_{exit} \leq 0 \\ \left(\dfrac{T_{fl,in} + T_{sat,x_{sat}}}{2}\right)\dfrac{z_{sat}}{L} + \left(\dfrac{T_{sat,x_{sat}} + T_{sat,out}}{2}\right)\dfrac{\left(L - z_{sat}\right)}{L} & ,if\ x_{exit} > 0 \end{cases} \tag{4.5}$$

The temperature at the base of the channels is calculated assuming 1D conduction across the silicon base and silicon dioxide insulation layer:

$$T_{base,avg} = T_{chip,avg} - q''_{base}\left(\frac{\left(d_{wafer} - d_c\right)}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}}\right) \tag{4.6}$$

The overall surface efficiency is defined as:

$$\eta_0 = 1 - \frac{NA_f}{A_{wet}}\left(1-\eta_f\right), \tag{4.7}$$

where the fin efficiency is defined as:

$$\eta_f = \frac{\tanh\left(md_c\right)}{md_c}, \text{ where } m = \sqrt{\frac{2h_{wall}}{k_{Si}w_f}}. \tag{4.8}$$

The heat transfer coefficient is first solved assuming a fin efficiency of unity; fin efficiency is then iterated until the calculated heat transfer coefficient value converged.

The total power supplied to the hotspot is calculated using $P_{el,HS} = V_{HS}I_{HS}$. Due to the relatively long lead wires and the low resistance of the hotspot heater, a significant portion of the supplied power is dissipated in the lead wires. Prior to testing, the electrical resistance of the hotspot heater, excluding the lead wires, is measured using a probe station (H-150, Signatone); the combined resistance of the hotspot heater, lead wires, wire bonds, and PCB traces is then measured using the same method. The net heat input into the hotspot heater is calculated using $Q_{HS} = \left(R_{HS,heater}/R_{HS,tot}\right)P_{el,HS}$.

The temperature of the hotspot heater is determined *a posteriori* by calibrating the hotspot heater resistance as a function of temperature using the RTDs adjacent to the heater as a reference under uniform heating conditions for which it can be assumes that all of these resistors are at the same temperature. The hotspot heater resistance is estimated at each background heating level for which hotspot heating tests are performed (because resistance the hotspot heater is not powered, the resistance is estimated by extrapolating the measured resistances to a hotspot heat flux of zero). A linear regression is fitted to these resistances as a function of chip temperature and is used to determine the hotspot temperature.

4.2.3 Uncertainty

The measurement uncertainties of each instrument in the experimental test facility are obtained from the manufacturers' specifications sheets and are listed in Chapter 3. In the case of the custom RTDs, the uncertainty for the chip temperatures (±1 °C) are conservatively estimated using the accuracy of the reference RTD used for the calibration, the linearity of the sensor calibration, and the repeatability of the sensors over time. The uncertainties of calculated values

are determined using the method outlined in Ref. [64]. The uncertainty in the stated heat flux is calculated to be ±2%, while uncertainty in effective thermal resistance and heat transfer coefficient are ±4-12% and ±8-17%, respectively.

4.3 Results and Discussion

4.3.1 Uniform Background Heat Flux

4.3.1.1 Effect of Channel Mass Flux

Figure 4.7 shows the steady-state base heat flux as a function of average chip temperature for Sample 33×370 (channel width × channel height: 33 μm × 370 μm) at three mass fluxes. Single-phase fluid is delivered to the channels at 59 °C (~6 °C subcooling based on the outlet pressure). At low heat fluxes, the heat input is insufficient for the fluid to reach the saturation temperature, so the fluid remains as single-phase liquid throughout the channels. In this low-heat-flux region (shown with open symbols in Figure 4.7), chip temperatures increase linearly with heat flux for all mass fluxes, which is characteristic of single-phase flow. For a fixed heat flux in the single-phase region, the chip temperature decreases with increasing mass flux. The heat input required to transition from single-phase to two-phase operation increases with mass flux due to the increase in sensible heat necessary to reach the saturation temperature, which is characteristic of two-phase systems [65]. At sufficiently large heat inputs, boiling is initiated, which results in a slight increase in the slope of the curve. While flow visualization in the channels is not possible, the outlet fluid in the manifold is monitored for the presence of vapor. The onset of boiling is often accompanied by a sharp drop in the wall temperature in systems containing straight, parallel microchannels [55]; this behavior is not seen in Figure 4.7 due to the large number of parallel channels, which each boil at slightly varying heat fluxes. This trend is described in Chapter 3 where the spatial temperature distribution is discussed in detail for the same heat sink system. As heat fluxes are increased further within the two-phase regime, the chip temperature rises are relatively linear, with higher mass fluxes resulting in higher slopes. The chip temperatures for each mass flux remain relatively similar to each other up to ~500 W/cm^2; at this point, the chip temperature for the lowest mass flux (600 kg/m^{2}s) begins to increase significantly for small increases in heat flux. The maximum heat flux dissipated increases with mass flux, with a maximum of 1020 W/cm^2 dissipated at a mass flux of 2100 kg/m^{2}s and an average chip temperature

of 127 °C. It is worth noting that this particular experiment was allowed to operate at a higher chip temperature than the cutoff to demonstrate the ability to dissipate high heat fluxes.

Figure 4.8(a) shows heat transfer coefficient as a function of exit thermodynamic quality for Sample 33×470. In the single-phase region, the heat transfer coefficient is relatively constant for a given mass flux and increases with increasing mass flux. This increase indicates the importance of developing flow and impingement effects in manifold microchannels; these effects have been shown in numerical models [28] and in experimental testing of manifold microchannels with smaller channel widths [66]. For all three mass fluxes, boiling is initiated at heat fluxes where the exit thermodynamic quality is less than zero, signifying subcooled boiling; while the bulk mean fluid temperature at the channel outlet is lower than the saturation temperature, local fluid temperatures near the wall can reach a superheat that causes bubble nucleation. As with the heat transfer coefficients in the single-phase region, the two-phase heat transfer coefficients also increase with mass flux for a given exit quality. For flow boiling in traditional microchannels, the nucleate boiling contribution to heat transfer has been shown to be largely unaffected by mass flux, but the convective transport is strongly affected by mass flux [55]; because the heat transfer coefficient is not constant for a given exit quality in the current work, this indicates that both nucleate boiling and convection transport mechanisms are significant [60]. Figure 4.8(a) shows that heat transfer coefficients begin to decrease at lower exit qualities for higher mass fluxes. Critical heat flux correlations that were developed for flow boiling in straight, parallel microchannels predict that the thermodynamic quality at critical heat flux decreases with increasing mass flux [67]. The decrease in heat transfer coefficient at high heat fluxes occurs due to intermittent dryout at the channel walls and has been shown to correspond to the suppression of bubble nucleation at channel wall in microchannel systems [6], [55], [68].

The effective thermal resistance as a function of base heat flux is shown in Figure 4.8(b) for Sample 35×470; the plotted points show the total thermal resistance (Equation (4.2)), while the horizontal, dashed lines represent the sum of conduction and caloric thermal resistances (Equation(4.3)). The horizontal lines define the minimum possible thermal resistance, in the absence of any convective thermal resistance, given the base thickness, base material, fluid, and mass flux. The single-phase thermal resistance (open data points) decreases with increasing mass flux, which correlates to the increase in heat transfer coefficient with increasing mass flux in Figure 4.8(b). For a fixed mass flux, thermal resistance decreases significantly from single-phase to two-

phase operation (closed data points), especially at low mass fluxes for which the single-phase thermal resistance is relatively large. At these low thermal resistances in the two-phase regime, the conduction and caloric resistances contribute significantly to the overall thermal resistance; for example, at a mass flux of 2100 kg/m²s, the conduction and caloric resistances together contribute 34% of the total thermal resistance at the minimum thermal resistance (2.20×10^{-6} m²K/W of 6.46×10^{-6} m²K/W). The contribution of the resistances other than convection, result in moderate decreases in thermal resistance for relatively large increases in heat transfer coefficient. For example, increasing the mass flux from 600 kg/m²s to 2100 kg/m²s increases the maximum heat transfer coefficient by 32% (32.4×10^{6} m²K/W to 42.8×10^{6} m²K/W), while the minimum thermal resistance only decreases by 15% (7.62×10^{-3} m²K/W to 6.46×10^{-3} m²K/W).

4.3.1.2 Effect of Channel Geometry

Figure 4.9(a) shows the base heat flux dissipated as a function of the average chip base temperature increase above the fluid inlet temperature for a mass flux of 2100 kg/m²s, for all of the channel geometries listed in Table 4.1. For a fixed channel width, the maximum base heat flux dissipated increases with channel depth; both heat transfer area and fluid flow rate increase with increasing channel depth, which allow for the dissipation of higher base heat fluxes. For a fixed aspect ratio (*viz*, Samples 15×150 and 33×300, $AR \approx 10$), the sample with the smaller hydraulic diameter (Sample 15×150) is able to dissipate a higher maximum heat flux (618 W/cm² compared to 494 W/cm²). Both samples have similar wetted areas, but Sample 33×300 has over twice the flow rate as Samples 15×150 for a given mass flux, which would in contrast result in a higher base heat flux in traditional microchannel systems where critical heat flux is largely dependent on fluid quality [67]. For a fixed channel depth (Samples 15×300 and 33×300, $d_c \approx 300$), the sample with thinner channels dissipates a 77% higher maximum heat flux (874 W/cm² compared to 494 W/cm²) than the sample with wider channels. This can largely be attributed to the 86% increase in wetted area due to the decrease in fin pitch for the thinner channels.

Figure 4.9(b) shows the wall heat flux, which calculated based on the measured wetted area, dissipated as a function of the average chip temperature increase above the fluid reference temperature. For a fixed wall heat flux and channel width, chip temperature rise increases with increasing channel depth; the samples with the highest aspect-ratio at each channel width exhibit significantly higher temperature rises for a given wall heat flux. For a fixed channel depth,

Samples 15×300 and 33×300 ($d_c \approx 300$) achieve similar maximum wall heat fluxes, with Sample 15×300 having a higher temperature rise at any given wall heat flux. In contrast, decreasing channel width has been shown to decrease chip temperature rise for a fixed channel depth [56] for larger channel widths (100-1000 μm) in traditional microchannels. Experimental data are not available for small-diameter, high-aspect-ratio channels similar to those used in this work; however, all available trends in the literature indicate lower temperature rises for thinner channels, which is not seen in the current work. The increase in temperature rise with decreasing width can be attributed to the decrease in impingement effects and decrease in flow rate at the base of the channels, which are caused by the increase in flow resistance in the direction normal to the flow [66]. In traditional, low-aspect-ratio microchannels with larger hydraulic diameters (400-1000 μm), wall superheat has been shown to be largely independent of hydraulic diameter [56]; smaller hydraulic diameter channels (<400 μm) were shown to have lower wall superheats at low wall fluxes, but reached critical heat flux at lower wall heat fluxes. These trends are not seen in the high-aspect-ratio, manifold microchannels tested in this work. For a fixed aspect ratio, Samples 15×150 and 33×300 (AR ≈ 10) show similar temperature rises to each other until wall heat fluxes of ~50 W/cm², above which Sample 33×300 experiences large temperature rises.

Heat transfer coefficient as a function of wall heat flux is plotted in Figure 4.10(a). Single-phase heat transfer coefficient is relatively constant for each channel geometry. Upon incipience, the heat transfer coefficient increases significantly and continues to rise as boiling is initiated in more of the channels. While the boiling curves (Figure 4.9(b)) were similar for Samples 33×150 and 33×300 (AR ≈10) up to wall fluxes of 50 W/cm², the heat transfer coefficients are much larger for Sample 33×300; this occurs due to the relatively low fin efficiency in the wide, deep channels (49-63% compared to 86-92% for Sample 33×150). In traditional microchannel systems, two-phase heat transfer coefficient is slightly dependent on channel dimensions and strongly dependent on fluid quality; namely, the heat transfer coefficient increases with increasing quality and decreasing channel hydraulic diameter (at low qualities) [56]. This trend is not seen in the current data where heat transfer coefficient is significantly larger for wider channels; this could be caused by the reduced flow resistance in wider channels allowing for better fluid replenishment at the channel base. For each sample, the heat transfer coefficient reduces sharply with heat flux after the maximum is reached, which may be caused by local/intermittent dryout at the wall [57] or flow instabilities that decrease flow to individual channels [58].

Thermal resistance as a function of base heat flux is shown in Figure 4.10(b). Single-phase thermal resistance is constant for a given channel geometry, which is a result of the constant single-phase heat transfer coefficient. Thermal resistance decreases as the flow enter two-phase operation, matching the trend in heat transfer coefficient. For a given base heat flux, Sample 15×150 has the highest thermal resistance due to its relatively small wetted area and low fluid flow rate. For all base heat fluxes, the thermal resistance of Sample 33×300 is significantly less than that of Sample 15×150, which has the same nominal wetted area and aspect ratio; this could be due to the increase in fluid flow rate for the deeper channels. For a fixed channel depth of ~300 μm (Samples 15×300 and 33×300), the sample with thinner channels has a minimum thermal resistance 15% lower than the sample with wider channels despite having a significantly lower heat transfer coefficient; in this situation, the increase in wetted area (Sample 15×300 has ~86% more wetted area than Sample 33×300) outweighs the decrease in the heat transfer coefficient.

4.3.1.3 Pressure Drop

Figure 4.11(a) shows the pressure drop as a function of base heat flux for Samples 33×470 for three mass fluxes. This differential pressure includes contraction into and expansion out of the microchannels as well as flow splitting and contraction/expansion resistances in the manifold. During single-phase operation, the pressure drop decreases slightly with increasing heat flux due to the decrease in viscosity at elevated temperatures. In the two-phase region, pressure drop increases with heat flux since the length of two-phase flow increases and the mixture velocity increases from the increase in vapor void fraction. Pressure drop during single-phase and two-phase operation increases with increasing mass flux for all base heat fluxes.

Pressure drop as a function of base heat flux for each of the samples is shown in Figure 4.11(b) at a mass flux of 2100 kg/m²s. Generally, single-phase pressure drop increases with increasing channel depth due to increased velocities in the manifold. For example, Sample 33×300 has a larger hydraulic diameter than Sample 15×150, which would lead to a lower pressure drop in straight, parallel channels because pressure drop is inversely proportional to hydraulic diameter for a fixed flow length [61]; however, Sample 33×300 has a single-phase pressure drop ~66% larger than Sample 15×150 (49 kPa compared to 30 kPa). This different behavior for the manifold microchannel heat sink is attributed to the increased fluid flow rate for a given mass flux for deeper channels leading to increased manifold pressure drops. Because the manifold dimensions remain

fixed for all channel geometries, the manifold velocities increase with increasing channel depth for a given mass flux. For a fixed channel depth of ~300 μm, where both samples are expected to have similar manifold pressure drops, the sample with wider channels has slightly lower single-phase pressure drop due to the increase in hydraulic diameter. The slope of the pressure drop curve is slightly steeper for samples with thinner channels because the two-phase pressure gradient depends on the inverse of hydraulic diameter, which is smaller for the thinner channels. Pressure drops below 120 kPa are maintained for all experiments.

4.3.2 Simultaneous Background and Hotspot Heat Flux Dissipation

Experiments were conducted with a hotspot heat flux applied over the central 200 μm × 200 μm area while simultaneously applying a uniform background heat flux over the entire 5 mm × 5 mm chip area. As mentioned in Section 4.3, the supplied power to the hotspot heater was scaled to account for electrical resistances external to the 200 μm × 200 μm heater. For the sample tested in this work, the hotspot heater resistance was measured to be ~48 % of the combined resistance of the hotspot heater, lead wires, wire bonds, and PCB traces; therefore, ~48% of the power supplied to the hotspot was dissipated external to the hotspot. Hotspot heat fluxes were increased from 0 to ~2,700 W/cm² at background heat fluxes of 100, 300, 500, 700, and 900 W/cm² for mass fluxes of 600, 1300, and 2100 kg/m²s using Sample 33×470. Note that all background heat fluxes are not possible for each mass flux due to chip temperature limits. Also note that for all combinations of background and hotspot heat fluxes, the total power supplied to the hotpot heater is negligible compared to the total power of the background heating. The minimum power to the background heaters is ~25 W (for a heat flux of 100 W/cm² over a 5 mm × 5 mm area) and the maximum power for the hotspot heater is ~1.1 W (2,700 W/cm² over a 200 μm × 200 μm area).

Figure 4.12(a) shows the steady-state hotspot temperature as a function of hotspot heat flux for a fluid mass flux of 2100 kg/m²s and various background heat fluxes. The temperatures at q''_{HS} = 0 W/cm² correspond to the hotspot temperature under background heating conditions and the subsequent points show the hotspot temperature as hotspot heat flux is increased. The hotspot temperature increases linearly with background heat flux. . For all background heat fluxes the hotspot temperature rise is constant at 16±1 °C at the maximum hotspot heat flux (q''_{HS}= 2,700 W/cm²). The hotspot temperature rise for the other two mass fluxes (not shown) exhibit the same trends, with a linear temperature rise and a slope that is unaffected by background heat flux. For

the background heat fluxes tested, the heat transfer coefficients are between 17×10^3 W/m²K and 43×10^3 W/m²K, a 150% difference; this large difference in heat removal rate at the backside has little effect on the measured hotspot temperature. The temperature rise due to the hotpot heat flux is dictated by the heat spreading and conduction resistances in the base.

Figure 4.12(b) shows the background heat flux as a function of the hotspot temperature rise above the fluid reference temperature with the hotspot heating cases overlaid on the boiling curves. Black data points represent the measured hotspot temperatures with only the background heat flux applied; blue data points represent hotspot temperatures during simultaneous hotspot and background heating conditions. The blue data points in Figure 4.12(b) are the same data as Figure 4.12(a), but plotted against background heat flux rather than hotspot heat flux; since the background heat flux does not change for each case, the hotspot temperatures show up as a horizontal line on the plot. The hotspot temperature rise resulting from the high local heat flux is significant compared to the temperature rise from uniform, background heating. The RTDs adjacent to the hotspot heater (~200 μm from the edge of the hotspot) measure temperature rises of only 3±1 °C above the background temperature at the maximum hotspot heat flux; the RTDs across the chip surface do not increase by more than 1 °C during hotspot testing for any background heat flux and mass flux. This indicates that the temperature rise at the hotspot is extremely localized and the rest of the chip surface is largely unaffected by the high hotspot heat flux. Also, given the relatively thick base substrate (185 μm), the temperature at the channel base is expected to be relatively uniform. This allows the heat sink to operate without any significant flow maldistribution (indicated by the chip temperatures remaining relatively constant throughout hotspot testing) despite the highly localized heating of the channels directly under the hotspot.

4.4 Conclusions

Single-phase and two-phase thermal and hydraulic performance characteristics for a variety of hierarchical manifold microchannel heat sink arrays, each with a unique channel geometry, are presented. The test vehicle uses a hierarchical manifold to feed an array of intrachip microchannel heat sinks with high-aspect-ratio channels. A heated chip area of 5 mm × 5 mm is cooled by a 3 × 3 array of microchannel heat sinks fabricated directly into the heated die, which also covers 5 mm × 5 mm. The test vehicles have channel widths of 15 μm and 33 μm and depths between 150 μm and 470 μm; the effective flow length in any flow passage is 750 μm.

It was shown in our previous study [66] that the maximum heat flux dissipation increases with increasing channel depth and mass flux; heat transfer coefficient is largely independent of channel depth, but strongly depends on exit thermodynamic quality. In this study, the effect of channel width and aspect ratio are also studied. Heat sinks with wider channels yield higher heat transfer coefficients, but not necessarily the lowest thermal resistance. For a fixed channel depth of ~300 μm, the sample with 15-μm wide channels has a wetted area ~86% larger than the sample with 33-μm wide channels; while the heat transfer coefficient is lower for the sample with thinner channels, the increased wetted area outweighs the decrease in heat transfer rate. To investigate the effect of hydraulic diameter on thermal performance, samples with a fixed aspect ratio of ~10 and equal wetted areas were tested; the sample with a larger hydraulic diameter (Sample 33×300) provided a higher heat transfer coefficient and lower thermal resistance compared to the sample with a smaller hydraulic diameter (Sample 15×150), which is attributed to the increase in fluid flow rate. In traditional two-phase microchannel heat sinks, heat transfer coefficient has been shown to be largely unaffected by channel dimensions for a given mass flux; maximum heat flux dissipation, therefore, increases with increasing wetted area (decreased fin pitch and deeper channels). This work shows that, unlike traditional heat sinks, maximum heat flux dissipation does not necessarily increase with increasing wetted area for two-phase manifold microchannel heat sinks.

Heat fluxes up to 1020 W/cm² are dissipated at pressure drops of less than 120 kPa and measured chip-to-fluid inlet temperature rises less than 58 °C using HFE-7100 as the working fluid and a heat sink with 33 μm × 470 μm channels. The cooling approach provides a minimum thermal resistance of 5.5×10^{-6} m²K/W at a mass flux of 2100 kg/m²s.

Hotspot heat fluxes of ~2,700 W/cm² (200 μm × 200 μm) were dissipated simultaneous with background heat fluxes up to 900 W/cm² (5 mm × 5 mm). The hotspot temperature rise was linear with hotspot heat flux for all mass fluxes and background heat fluxes; at ~2,700 W/cm², the temperature rise was 16±1 °C above the chip surface temperature.

Table 4.1. Summary of microchannel dimensions.

Sample	N_c	w_c (μm) (actual value)	d_c (μm) (actual value)	AR (-)	d_H (μm)	$A_{wet,tot}$ (mm²)	$A_{cross,tot}$ (mm²)	d_{wafer} (μm)
15×150	50	15 (14.7)	150 (153)	10.4	28.8	217	2.05	300
15×300	50	15 (16.2)	300 (310)	19.1	31.7	434	4.50	385
33×300	25	33 (33.7)	300 (317)	9.4	64.6	233	4.82	390
33×400	25	33 (33.5)	400 (397)	11.9	65.5	290	6.08	500
33×470	25	33 (33.0)	470 (465)	14.0	63.0	331	6.66	650

Table 4.2. Summary of experimental operating conditions

Sample	G (kg/m²s)	$\dot{V}$ (mL/min)	Re (-)
15×150	1300, 2100, 2800	160, 255, 340	96, 155, 207
15×300	1300, 2100, 2800	350, 565, 750	105, 171, 229
33×300	600, 1300, 2100	170, 375, 435	99, 216, 349
33×400	600, 1300, 2100	215, 470, 550	100, 219, 354
33×470	600, 1300, 2100	240, 515, 605	97, 211, 341

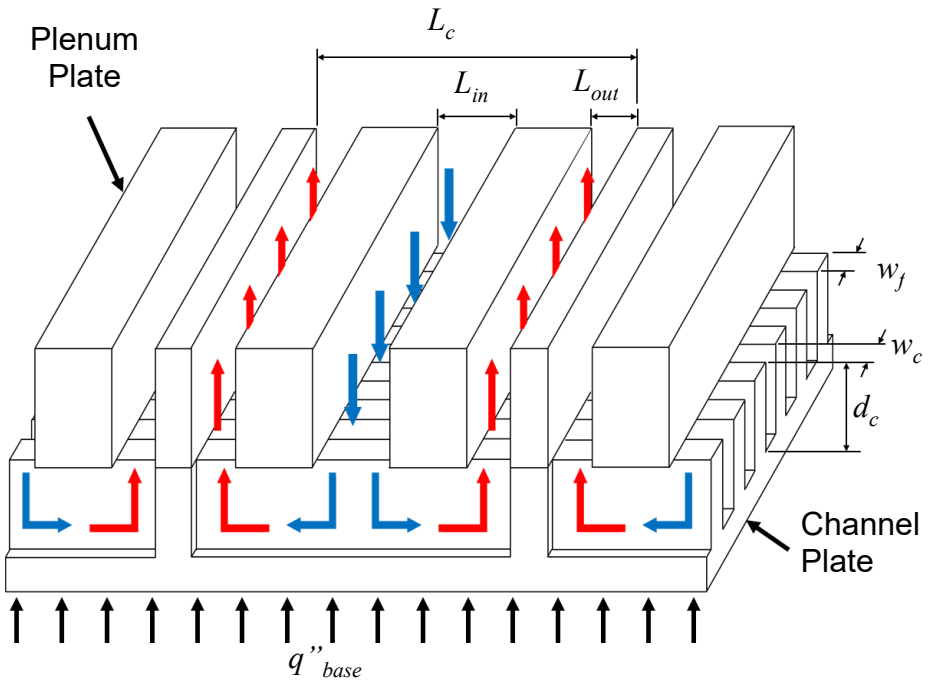


Figure 4.1. Schematic diagram of the heat sink unit cell showing the fluid flow paths and relevant dimensions.

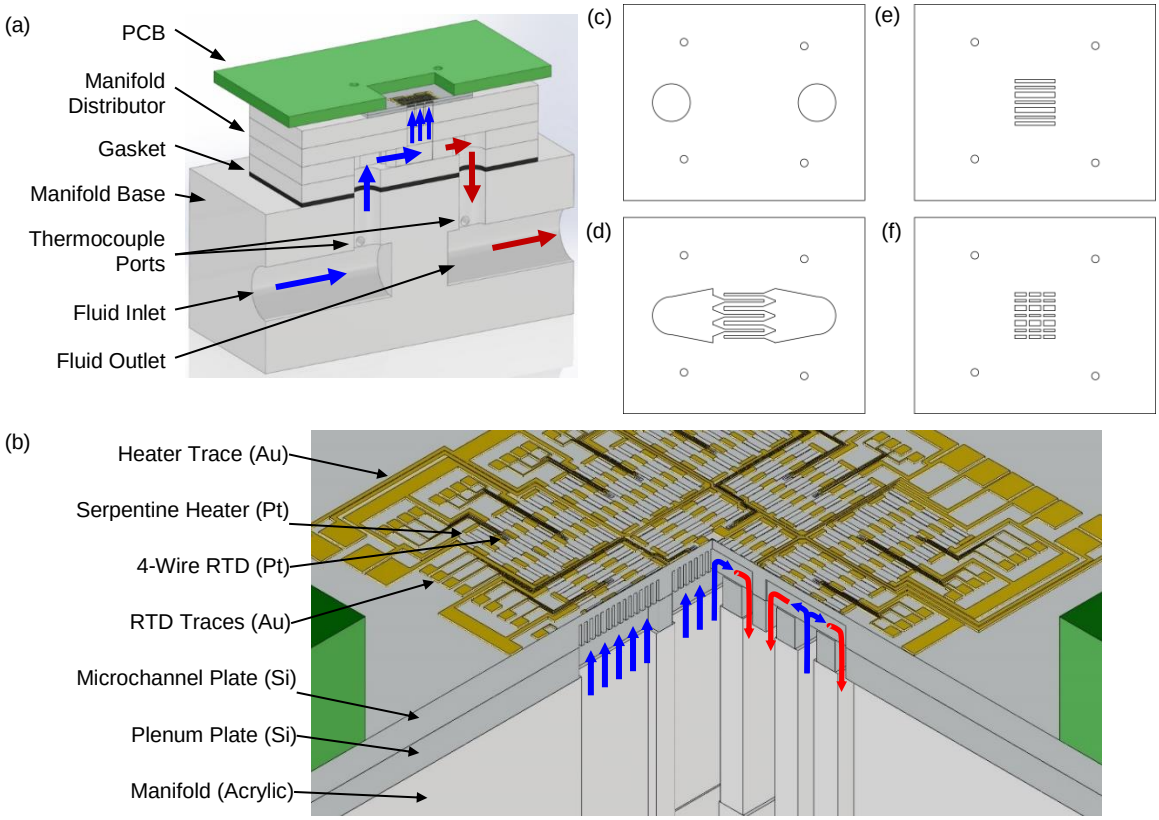


Figure 4.2. (a) CAD image of the test vehicle with a half-symmetry section removed and fluid inlets (blue) and outlets (red) shown; (b) zoomed-in view of the test vehicle with a quarter-symmetry section removed showing the fluid flow paths in the test chip; and (c-f) each plate level of the manifold distributor used to deliver fluid to individual heat sinks.

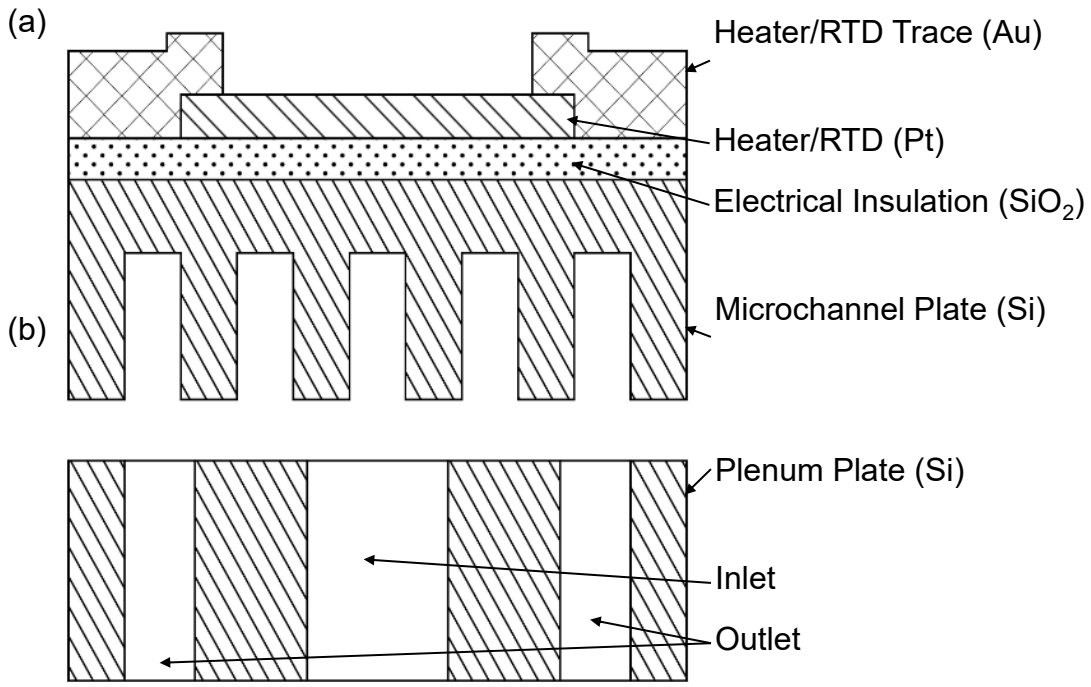


Figure 4.3. Schematic diagram of (a) the microchannel plate and (b) the plenum plate.

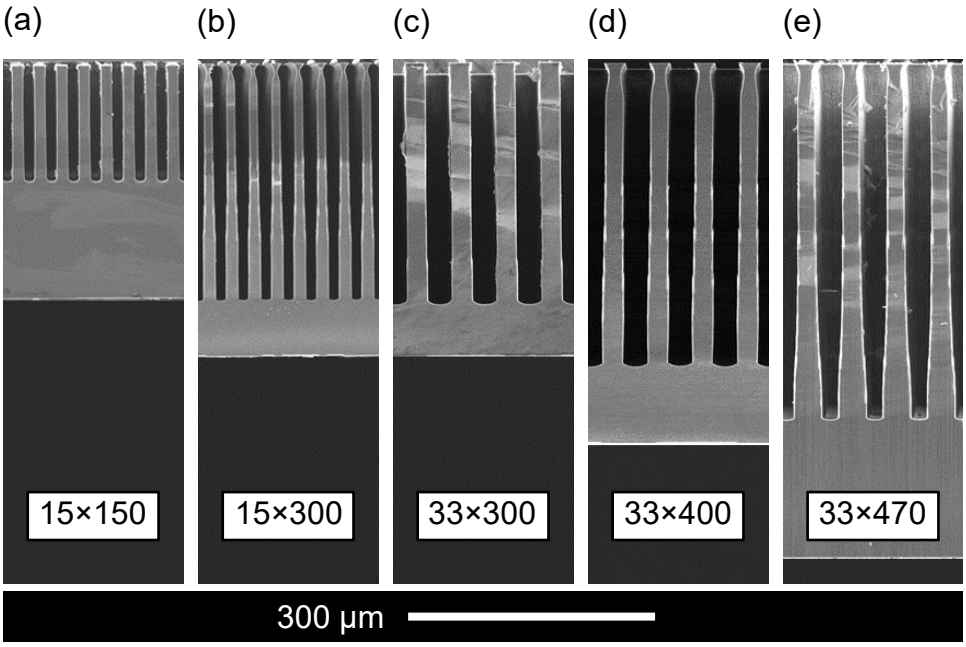


Figure 4.4. SEM images of the five microchannel cross-sections tested: (a) 15×150, (b) 15×300, (c) 33×300, (d) 33×400, (e) 33×470.

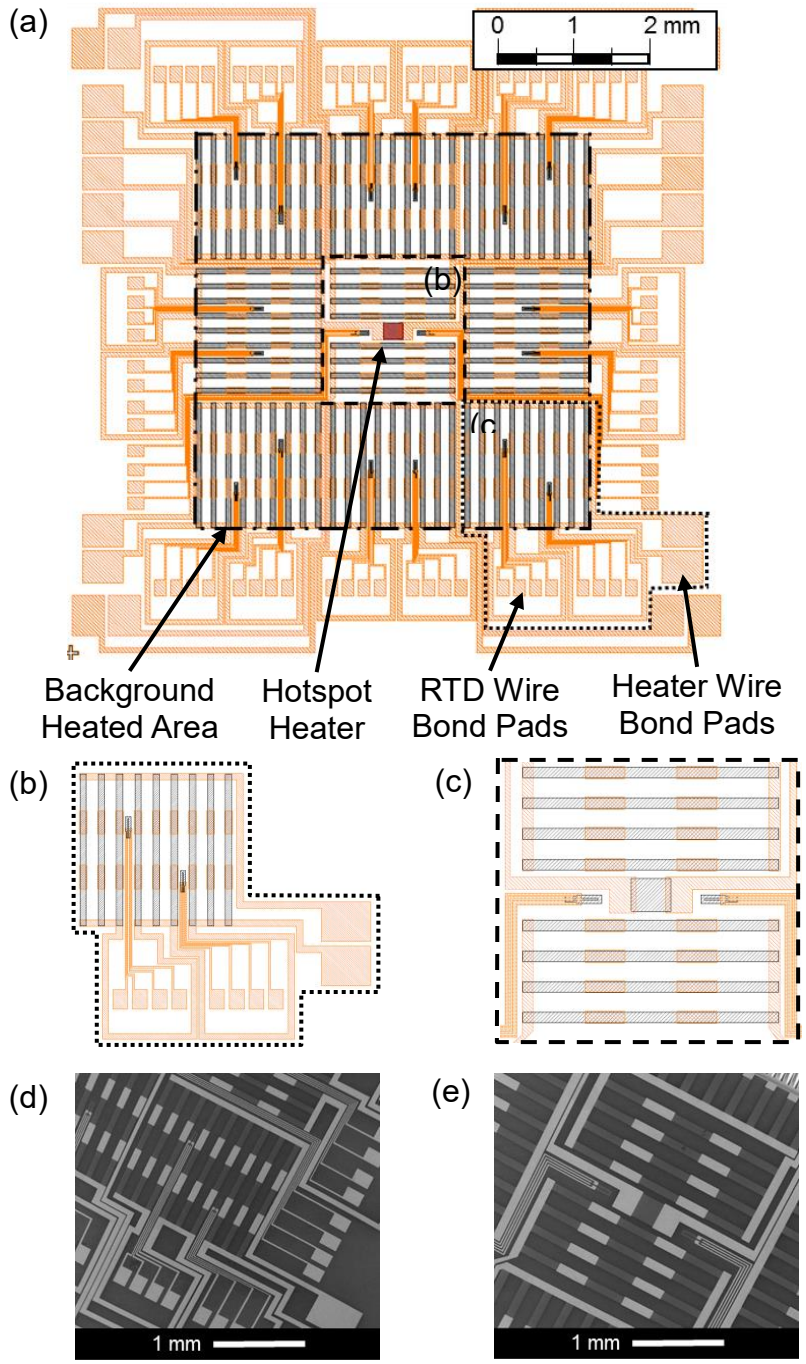


Figure 4.5. CAD drawing of (a) entire heater and RTD layout, (b) a background-only heater zone, and (c) the center zone with background and hotspot heaters. SEM images are shown for these same two heater zones consisting of (d) only background heaters and (e) background and hotspot heaters.

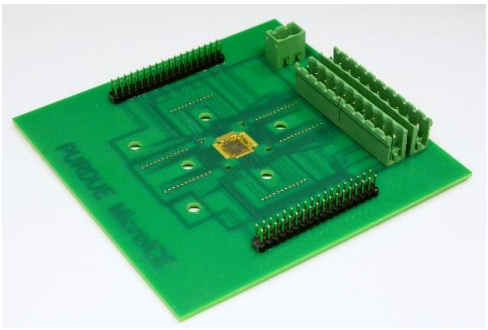
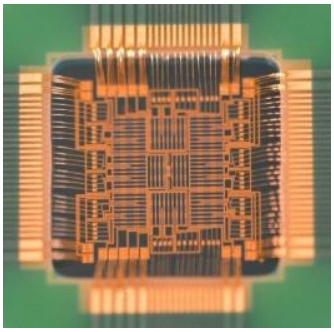
(a)  (b) 

Figure 4.6. (a) Photograph of the test chip mounted to the PCB with heaters and sensors face up and (b) zoomed-in view of the heaters and sensors wire-bonded to PCB contact pads.

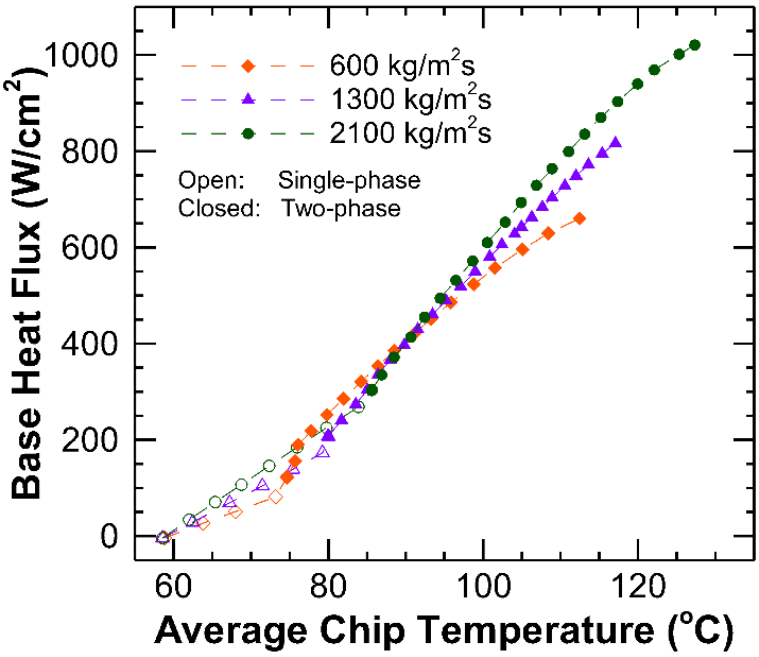


Figure 4.7. Base heat flux as a function of average chip temperature for Sample 33×470.

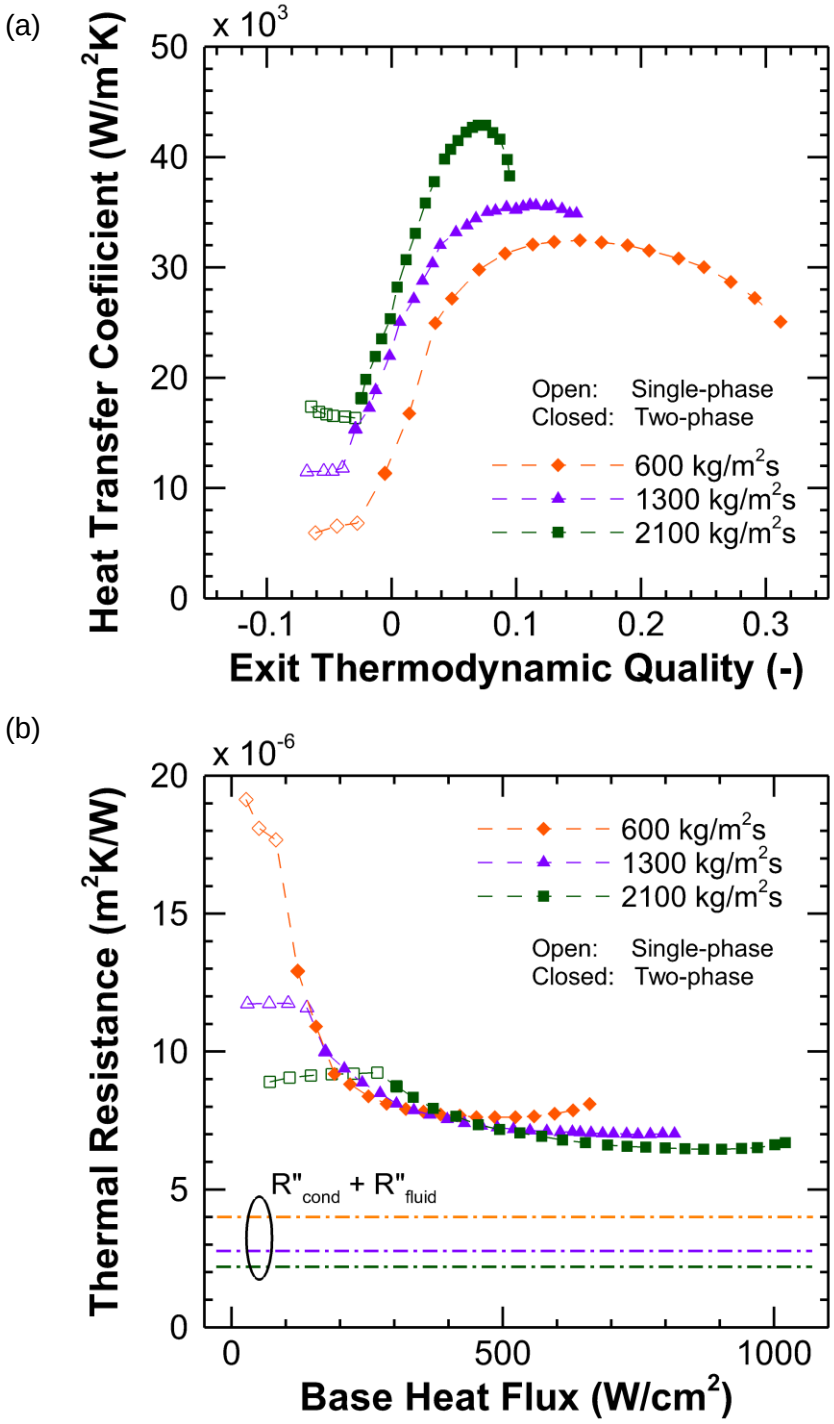


Figure 4.8. (a) Heat transfer coefficient as a function of exit thermodynamic quality and (b) effective thermal resistance as a function of base heat flux for Sample 33×470 with data points showing total resistance and dashed lines showing sum of conduction and caloric resistances.

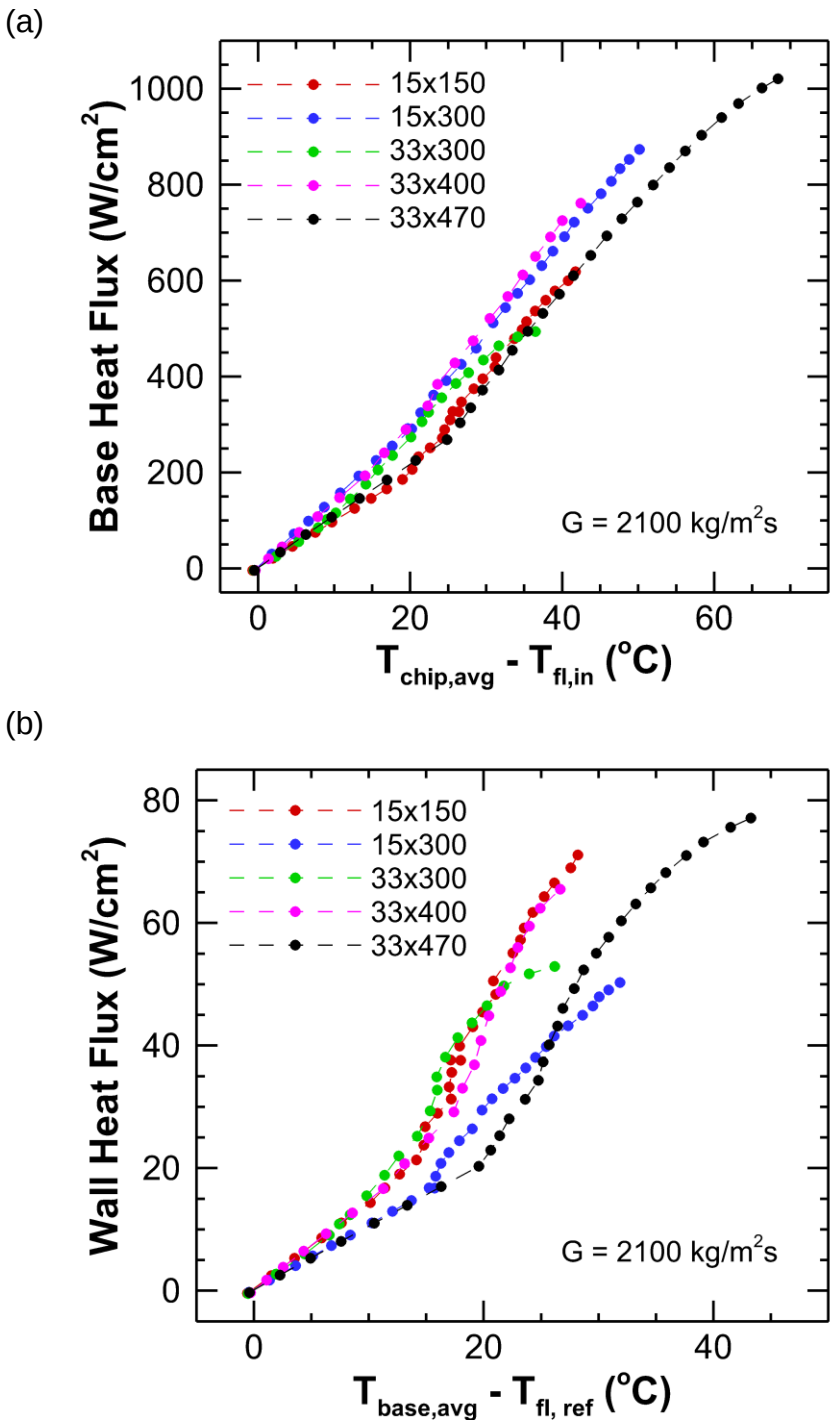


Figure 4.9. (a) Base heat flux as a function of chip temperature rise above the fluid inlet temperature and (b) wall heat flux as a function of chip temperature rise above the fluid reference temperature, at a mass flux of 2100 kg/m²s.

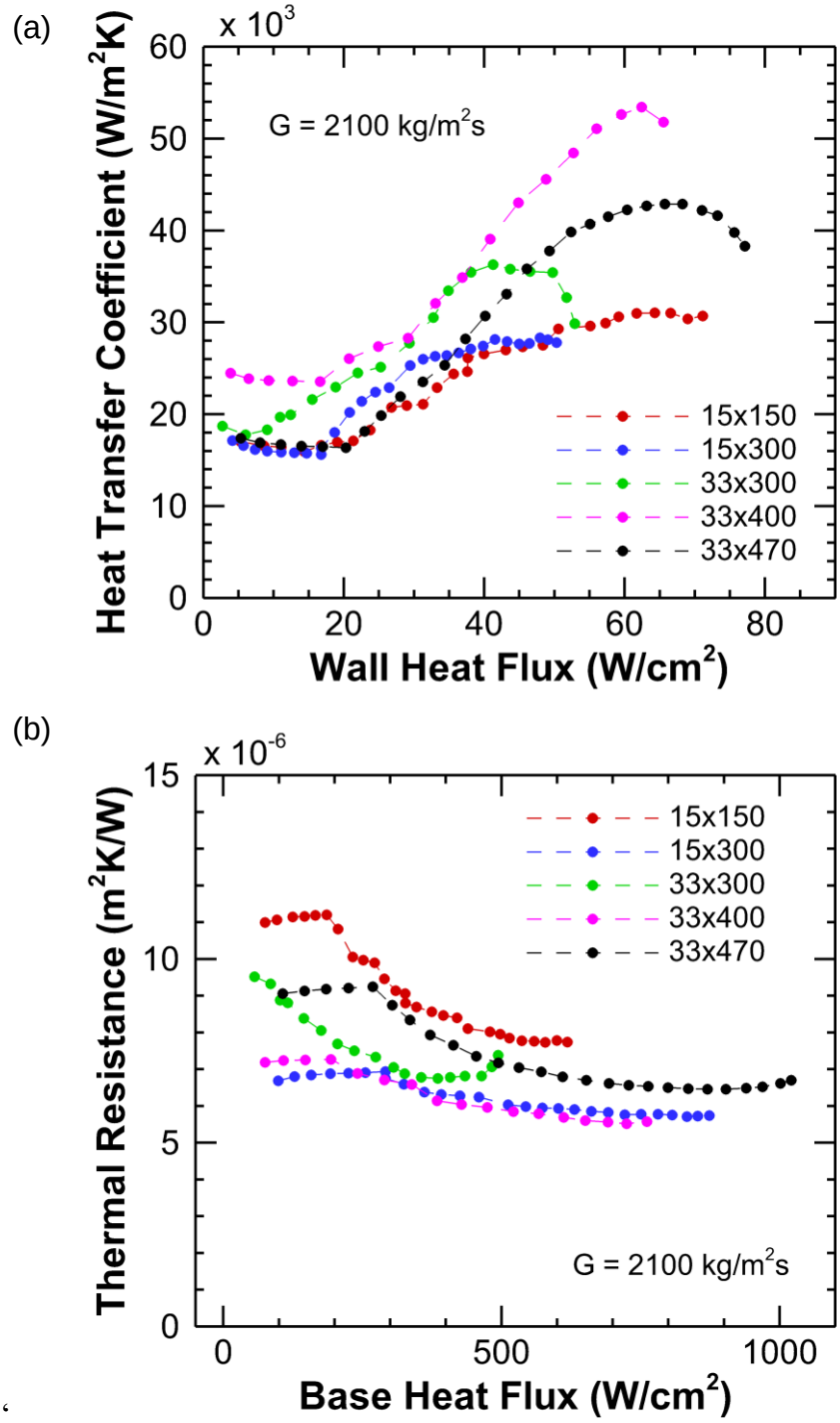


Figure 4.10. (a) Thermal resistance as a function of base heat flux and (b) heat transfer coefficient as a function of fluid exit thermodynamic quality at a mass flux of 2100 kg/m²s.

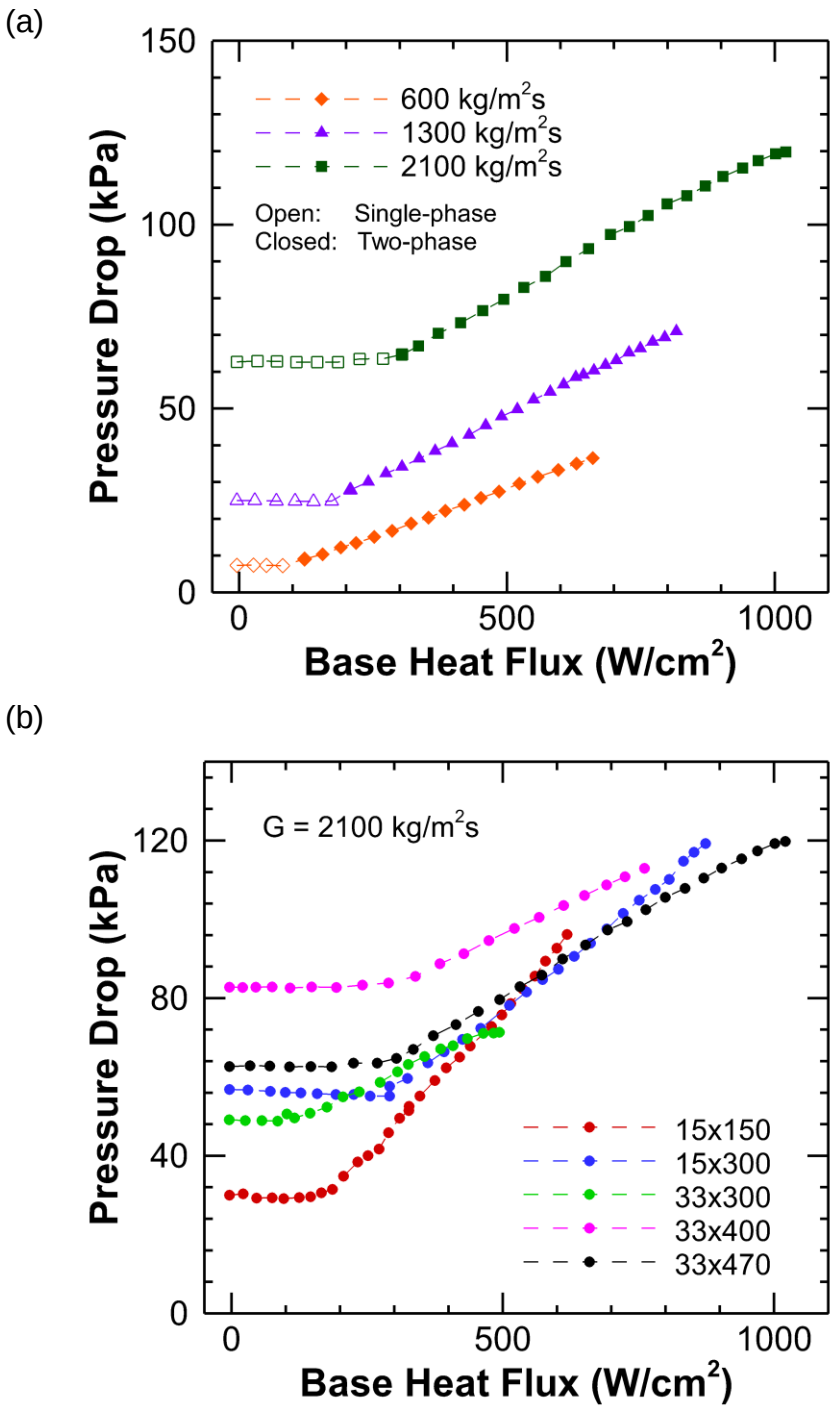


Figure 4.11. (a) Pressure drop as a function of base heat flux and mass flux for Sample 33×470 and (b) pressure drop as a function of base heat flux and channel geometry at a mass flux of 2100 kg/m²s.

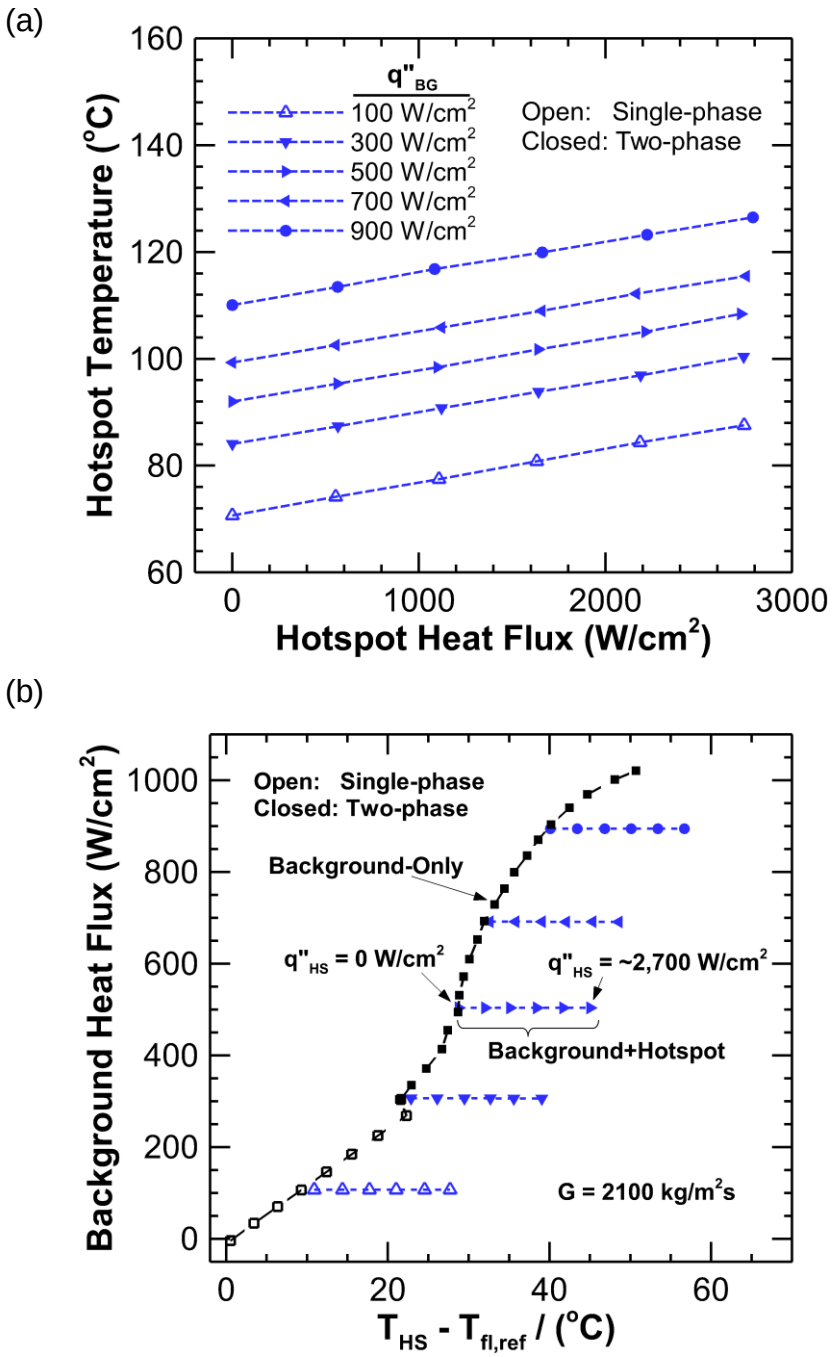


Figure 4.12. (a) Hotspot temperatures as a function of hotspot heat flux for a variety of fluid mass fluxes and background heat fluxes. (b) Hotspot temperature rise above fluid reference temperature; boiling curves with black data points show hotspot temperature at zero hotspot heat flux and colored data points show hotspot temperature during hotspot testing (arrow pointing to hotspot temperature at the maximum hotspot heat flux of ~2,700 W/cm²).

5. DESIGN, FABRICATION, AND CHARACTERIZATION OF A COMPACT, MULTI-LEVEL HIERARCHICAL MANIFOLD MICROCHANNEL HEAT SINK

In this chapter, a novel hierarchical manifold microchannel design utilizing a multi-level manifold distributor that feeds an array of microchannel heat sinks is presented. The test vehicle allows the characterization of the key figures of merit such as heat flux, heat transfer coefficient, and pressure drop in hierarchical manifold and microchannel heat sink. The manifold layers and microchannels are fabricated in silicon using deep reactive ion etching. The overall dimensions of the manifold are 6 mm × 15 mm × 2 mm for an overall volume of 180 mm². The simulated heat source is provided via Joule heating using thin-film platinum heaters and spatial temperature measurements are made using 4-wire resistance temperature detectors. Individual manifold layers and the microchannels are bonded to each other using thermocompression bonding with interstitial gold layers on the mating surfaces. Thermal and hydraulic testing is performed by pumping the dielectric fluid HFE-7100 into the device at a known flow rate, temperature, and pressure while heat flux is incrementally increased until the test is concluded. Heat fluxes up to 630 W/cm² are dissipated over a 5 mm × 5 mm heated area at chip temperatures less than 110 °C and channel pressure drops less than 24 kPa. Pressure drops due to contractions and expansions and flow in the manifold result in a large portion of the overall pressure drop in the system.

5.1 Experimental Setup

5.1.1 Hierarchical Manifold and Microchannels

In a hierarchical manifold microchannel heat sink, fluid is delivered to an array of microchannels using a multi-level manifold, as shown schematically in Figure 5.1. The manifold consists of multiple layers that bifurcate the flow into gradually finer features. Maximum granularity occurs at the channel inlets where flow is delivered intermittently along the flow length of the channels thereby reducing the flow length. In previous work [69], a two-phase hierarchical manifold microchannel heat sink was introduced with a 3 × 3 array of microchannel heat sinks etched into a single silicon die with a total heated area of 5 mm × 5 mm. Each of the nine heat sinks consisted of 50 high aspect ratio microchannels that were nominally 15 μm wide and ranged

in depth from 35 μm to 310 μm. In this work, the same 5 mm × 5 mm die area was discretized into a 9 × 9 array of heat sinks, resulting in shorter fluid flow lengths compared to the previous design. The detailed dimensions of the manifold and microchannels are shown in Table 1.

A CAD model of the hierarchical manifold microchannel heat sink used in this work is shown in Figure 5.2. The manifold has features etched into both sides of four silicon wafers for a total of eight levels. Fluid enters the manifold at Level 1 where there is a single flow path; as the fluid travels from Levels 2 through 8, it is gradually split into finer features. After reaching the 8th level where there is a distinct flow feature for each of the 81 zones, the fluid enters the microchannels, bends 90 degrees, and travels along the length of the channels. During testing, the fluid is heated by the simulated heat source on the back side of the wafer while flowing through the microchannels. After traveling along the length of the channels, the fluid bends 90 degrees and travels back through the manifold where the fluid is recollected from the 182 channel outlets (Level 8) into a single fluid exit (Level 1). The fluid pressure drop is measured between the inlet and outlet streams at Level 0 and Level 8; the measurement at Level 0 provides the total system pressure drop while the measurement at Level 8 provides the channel pressure drop.

5.1.2 Heater/Sensor Layout

The heater and sensor layout are designed to provide a uniform background heat flux over the 5 mm × 5 mm die area, and to measure local temperatures across the die area. For ease of fabrication, the RTDs and heaters are deposited and patterned at the same time. Since all the features are in the same plane, the heaters and RTDs—and their traces—cannot overlap. Test heaters consist of a 3 × 3 array of individually addressable background heaters and a 200 μm × 200 μm area hotspot heater in the center of the heated area. The background and hotspot heat generation were achieved using serpentine heaters and a square heater, respectively, as shown in Figure 5.3. Two important features of the heater design are that (i) all of the background heaters have same width and are equally spaced across the entire heated area and (ii) relatively thick gold pads are periodically patterned on top of the serpentine heaters to reduce local heat generation. While the heat flux is produced locally at the heater locations, thermal simulations show that heat diffusion in the base of the microchannel results in a uniform heat flux at the base of the channels. RTDs are placed between the lines of the heaters, each zone contains two RTDs for a total of 18

temperature measurements across the die surface. All RTDs are connected using the four-wire technique to eliminate the lead wire resistance from the measured resistance.

Electromigration has been shown to create voids and hillocks on metals due to the movement of ions under bias and is likely to happen at large when the current densities and high temperatures [70]. Electromigration can be avoided by increasing heater resistance, which results in lower current densities for a given power. However, higher resistance will require a higher voltage and this may cause dielectric breakdown. Therefore, the resistance of heater is determined based on both electromigration limit (10^7 A/cm^2) and breakdown voltage limit of dielectric layer (~10 MV/cm for SiO_2). As shown in Table 5.2, analytical solution showed that 333 Ω of background heater and 18 Ω of hotspot heater satisfy these requirements when the heaters reached at 1 kW/ cm^2 and 2.5 kW/cm^2, respectively. It should be noted that the heat generation in the lead wires is not negligible for hotspot heater due to the low resistance of the hotspot heater and long lead wire length. Thus, it is necessary to account for the heat dissipation in the wires during heat flux calculations. Platinum is used as heating element as it has strong resistance to oxidation and chemical reactions. In addition, the electrical resistance of Pt is linear with respect to temperature over the normal operating temperature of electronics making it a good candidate for RTDs [71]. Gold is chosen as the lead wire material not only to minimize heat generation in the leads, but also for robust connections to PCB using gold wires during wire-bonding. Titanium is deposited as an adhesion layer for both platinum and gold.

5.2 Fabrication of Microchannel Plate and Manifolds Plate

The overall fabrication can be divided into three parts: i) Manifold (top and bottom) & microchannel etch, ii) Heater & RTD patterning, and iii) integration, as shown in Figure 5.4. The mirochannel wafer fabrication process, which is outlined in Figure 5.5, begins by etching the microchannel features in a 300 μm-thick, 4-inch silicon wafer. A single wafer yields 12 dies, each 20 mm × 20 mm. The channels occupy the center 5 mm × 5 mm area of the die with the remaining area available for traces and wire-bond pads and mounting the wafer to the PCB. The wafer is cleaned using Piranha solution and a 2-μm thick silicon dioxide (SiO_2) hard mask layer is thermally grown on the wafer. A Hexamethyldisilazane (HMDS) adhesion promotor is then applied to one side of the wafer followed by a 7-um AZ9260 positive photoresist layer, both using a using a SCS G3 Spin Coater Series spinner. The photoresist layer is exposed using a mask aligner (MA6, Karl

Suss) and developed in a diluted AZ400K solution (DI water:AZ400K = 3:1). The SiO_2 layer is removed from the open areas using a plasma dry etch (STS-AOE). The channels are then etched to the desired depth in the silicon using the BOSCH process (STS-ASE). For the etching of high aspect ratio microchannels, photoresist and SiO_2 are both used as a mask; the photoresist provides the mask for most of the area while the SiO_2 provides sharper edges and more vertical sidewalls. The key etch parameters are listed in Table 5.3.

Once the channels are etched, the photoresist and SiO_2 layers are removed using PRS2000 and BOE respectively. Figure 5.6 shows the SEM images of etched microchannel. Unlike wet etch process, where etch direction depends on wafer orientation, a straight wall is made as a result of the BOSCH process. All channels have consistent width and the wall and bottom surface are smoothly finished.

Heater and RTD patterns are fabricated directly on the microchannel wafer. After the microchannel etch process is done, a 200-nm thick layer of SiO_2 is thermally grown on the wafer as a dielectric layer. The same lithography procedure as the microchannel patterning—HMDS and a 7-μm thick AZ9260 resist layer—is applied to the wafer on the side opposite to the microchannels. Backside lithography was used to align the heater and RTD patterns with respect to the microchannels. Once patterns are defined, 5 nm of Ti and 20 nm of Pt are deposited via electron beam evaporation (CHA Industries, Inc.). This was done at the pressure level of 2.0×10^{-6} torr and the deposition rate was 1.0 Å/s. Lift-off process is done by stripping of photoresist using PRS2000. To fabricate the heater and RTD lead wires, this lithography procedure is repeated with two differences: the trace locations are defined using a new mask and the depositions are 10 nm of Ti and 400 nm of Au. Figure 5.5 shows heaters and RTDs deposited on the opposite side of microchannel wafer.

Since the hierarchical manifold requires multiple layers for flow distribution, etching features into both sides of the wafers reduce the required number of wafers while also increasing the alignment between layers. Features are etched from one side and then from the other side, with the features meeting near the middle of the wafer. Representative cross-sections at various steps in the manifold fabrication are shown in Figure 5.8. The same fabrciation procedure that was used for microchannel etch is used on each side of the wafer: a 2 μm-thick SiO_2 layer is thermally grown on 500 μm-thick wafers, HMDS and AZ9260 are spun on one side of the wafer, the photoresist is exposed and developed, the SiO_2 layer is dry-etched, and the silicon is etched using BOSCH

process. Etching parameters are the same as microchannel etch parameters and are shown in Table 5.3. Photoresist and SiO_2 are removed by PRS2000 and BOE. The same procedure is then repeated on the opposite side of the wafer. Backside lithography is used to align the features with the features already etched in the wafer.

5.3 Integration

All the layers of the manifold and microchannels are mechanically joined to seal between the manifold's fluid routing features and to prevent fluid from bypassing the microchannels. The hermiticity of thermocompression bonded samples for this application began by fabricating two silicon wafers, each with fluid routing features, depositing 500 nm of gold on the mating surfaces, and then thermocompression bonding the wafers. Other bonding methods such as anodic bonding and silicon fusion bonding were not able to bond Si (manifold plate) and SiO_2 (microchannel plate). This may be due to the absence of intermediate layer [72] or insufficient temperature or voltage, which was limited by equipment [73]. Thermocompression bonding successfully bonded the wafers and the bonded wafers survived after the dicing process showing monolithic sealing between plates. The hermiticity of the test vehicle was estimated by testing a sample with similar feature sizes

Prior to bonding, the microchannel and manifold wafers are cleaned using Piranha solution. 50 nm of Ti and 500 nm of Au are deposited on both sides of manifold interface using a magnetron sputtering system (CUSP-Series, MANTIS Deposition). The system pressure during deposition is held at 7.3×10^{-3} Torr and the DC deposition current is 0.1 A. The Ti layer is used to increase adhesion of the subsequent Au layer and the sample is rotated during deposition for uniformity across the wafer. The wafers are then diced into the 20 mm × 20 mm dies for bonding (Disco DAD-2H/6 Dicing Saw). Figure 5.9 shows the metallized and diced manifold dies.

A custom-made, ceramic assembly fixture is used to align microchannel die and manifold dies during thermocompression bonding. The assembly is completed in cleanroom to prevent possible contamination. Once the manifold and microchannel dies are stacked in order, the fixture is installed in the bonding facility, as shown in Figure 5.10. Thermocompression bonding is conducted at 350 °C and a pressure of 500 kPa for 1 hour. To characterize the manifold feature alignment and dimensions, one sample was diced normal to the channel flow direction, as shown in Figure 5.11. The arrows indicate fluid path through the manifolds. The results show no cracks

or gaps between the plates and the flow features are aligned within a few microns of tolerance. Prior to dicing, the system was leak-tested up to 100 kPa using the working fluid, HFE-7100, without any leaks.

After thermocompression bonding is completed, the wafer assembly is bonded to the underside of a custom-designed printed circuit board (PCB) using high temperature epoxy (Duralco 4700 Ultra Temp Adhesive) and annealed at 120 ℃ for two hours. The heaters and RTDs are then electrically connected to the PCB bond pads using gold wire bonds as shown in Figure 5.12. Each of the background heaters, the hotspot heater, and each of the RTDs are wirebonded separately such that they are addressed and monitored individually. (Ultrasonic wedge wire bonder, West·bond, Inc.).

5.4 Experimental Methods

5.4.1 Measurement Details

A schematic diagram of the electrical components used to measure the voltage and current to each of the heaters, and to adjust the power to each of the heaters, is shown in Figure 5.13. A single programmable DC power supply (Sorrensen XG100-8.5) is used to power all of the heaters. While the design of each test chip heater is identical, slight differences in metal deposition thicknesses, trace lengths, wire bond resistances, lead wire lengths, and operational temperatures can lead to slight differences in resistance between heaters. To ensure uniform heat flux across the chip surface throughout testing, a potentiometer (Ohmite RES25RE) is added in series with each of the heaters; this provides a variable resistance that is used to adjust the relative resistances of each parallel branch and thus equalize the power applied by each heater. A voltage divider circuit (TE Connectivity 1622796-6, 10 kΩ ± 0.1%; TE Connectivity 8-1879026-9, 499 kΩ ± 0.1%) is wired in parallel to each heater of the test chip, which is used to step down below the 10 V limit for the data acquisition hardware (National Instruments cDAQ-9178). By measuring the voltage drop across R_{div2}, the overall voltage is calculated using $V_i = V_{meas,i} * ((R_{div1} + R_{div2})/R_{div2})$. The voltage drop across a shunt resistor (Vishay Y14880R10000B9R, 0.1 Ω ± 0.1%) wired in series to each heater is used to calculate the current through each heater: $I_i = \left(V_{shunt,i}/R_{shunt}\right)$. The total voltage drop and current are measured using the same techniques and are used to verify the individual measurements.

5.4.2 Testing Procedure

During testing, most of the applied heat is absorbed into the fluid via convective and boiling heat transfer; however, some of the heat is conducted into the test fixture and lost via natural convection and radiation. This heat loss was estimated prior to testing using the method outlined in Section 4.2.2and was found to be $Q_{loss} = 0.02768 * (T_{chip,avg} - T_{amb})$.

To calibrate the on-chip RTDs, the test chip is placed in a laboratory oven along with a Pt100 RTD (PR-10-3-100, Omega), which is used as the reference temperature. The oven temperature is adjusted to multiple points spanning the entire operational range. A first-order linear regression is used to determine the relationship between electrical resistance and temperature for each of the 18 RTDs across the chip surface.

Prior to testing, the working fluid—HFE-7100—is degassed via vigorous boiling and subsequent recollection of the vapor; noncondensable gases escape during this process, leaving pure HFE to be used for testing. HFE-7100 was chosen because of its high dielectric strength and its low attenuation of RF signals as well as its boiling point (61 °C at 1 bar) and high wettability. A flow loop is designed to deliver fluid to the test section at a constant and known flow rate, inlet temperature, and outlet pressure. Experimental testing was performed with an inlet temperature of 59 °C (~6 °C below the saturation temperature at the outlet pressure), outlet pressure of 121 kPa (3 psig), and fluid flow rates ranging from 150 to 350 g/min. During testing, the heat input to the test chip heaters begins at 0 W and is incrementally increased until a maximum chip temperature of 120 °C is reached, recording the steady-state data (temperatures, pressures, voltages, currents, and flow rate) for each heat input.

5.4.3 Data Reduction

The data reduction procedure for these experiments is the same the procedure outlined in Section 4.2.2.

5.5 Results

This section provides a description of the thermal-hydraulic performance of the test chip described above; for a more thorough, in-depth analysis of performance trends in manifold microchannel heat sinks during two-phase operation, please refer to [23,24].

5.5.1 Boiling Curves

Figure 5.14 shows the chip temperature as a function of base heat flux for four fluid flow rates. The fluid enters the test chip at 59 °C and is heated as it flows along the length of the channels. At low heat fluxes, the energy absorbed by the fluid is not sufficient to initiate boiling. This single-phase region provides a linear chip temperature increase with heat flux, visible at low heat fluxes for each flow rate. As more heat is delivered to the fluid, the fluid begins to boil, resulting in a lower temperature rise for a given increase in heat flux compared to the single-phase region. At higher heat fluxes, the fluid begins to boil further upstream in the channel and a larger portion of the channel is in the two-phase regime, resulting in even lower temperature rises. Once a large enough heat flux is applied, the fluid begins to boil enough that it cannot be properly replenished at the nucleation site, which causes local regions with extremely low heat transfer performance. The degradation in performance is shown in Figure 5.14 where the temperature rise increases for a given heat flux increase. The heat fluxes required for incipience and dryout are extremely dependent on the fluid flow rates, as shown in Figure 5.14. As flow rate is increase, the heat necessary for the fluid to reach the saturation temperature increases, delaying incipience (~100 W/cm² for 150 g/min, ~210 W/cm² for 350 g/min). Similarly, dryout is delayed as flow rate increases, allowing for higher heat flux dissipation for higher flow rates. The highest heat flux dissipated at a flow rate of 150 g/min was 305 W/cm² and increased to 660 W/cm² for a flow rate of 350 g/min, an increase of 116%.

5.5.2 Pressure Drop

Figure 5.15(a) shows the measured pressure drop across the entire test chip, including pressure drops due to flow in the inlet and outlet manifolds as well as the channels. For each flow rate, the pressure drop is relatively constant in the single-phase region. Upon incipience, the bulk fluid density decreases causing an increase in fluid velocity and pressure drop. The two-phase pressure drop increases linearly with heat flux due to the increase in vapor generation with increasing heat flux for a given flow rate. Pressure drop increases with increasing flow rate once again due to the increase in fluid velocity. Figure 5.15(b) shows the pressure drop across the test chip along with the measured pressure drop across the channels for flow rates of 290 and 350 g/min. In single-phase operation, the increase in flow rate from 290 to 350 g/min results in an increase in total pressure drop from 54 kPa to 82 kPa, a 52% increase; the corresponding channel

pressure drop increases from 15 kPa to 16.5 kPa, a 10% increase. For both flow rates, a majority of the total pressure drop occurs in the inlet and outlet manifold flow features; the channel pressure drop accounts for a between 20% and 27% of the total pressure drop, depending on the heat flux. This is important because channel pressure drop tied to thermal performance, while manifold pressure drop can be minimized without affecting thermal performance. It is worth noting that a portion of the manifold pressure drop is inevitable due to the contracting flow present.

5.5.3 Comparison to 3 × 3 Array

Figure 5.16(a) shows the high-flow-rate data from Figure 5.15(a), now compared to a sample with a 3×3 array of heat sinks at similar mass flow rates. The samples have close to the same channel geometries (the sample with a 3 × 3 array of heat sinks contains 15 μm × 150 μm channels). Overall, the thermal performance is extremely similar for the 9 × 9 and 3 × 3 arrays of heat sinks at both flow rates. While the flow length and number of parallel flow paths are significantly different for the two samples, the hydraulic diameters are nearly identical; therefore, the fluid quality should be similar for a given flow rate and heat flux. For traditional microchannels, thermal performance is closely tied to fluid quality during two-phase operation, which is also seen in the current data. Figure 5.16(b) shows the total systems pressure drop for the 3×3 array compared to that the 9×9 array; the channel pressure drop for the 9×9 array is also show (channel pressure drop was not measured for the sample containing the 3×3 array. The 3 × 3 array, which has a flow length approximately twice that of the 9×9 array, has a lower pressure drop for a given flow rate and heat flux. This shows the relative importance of the manifold pressure drop in the overall pressure drop. The 9×9 array requires much smaller manifold features, which results in much larger manifold pressure drops compared to the 3×3 array. Additionally, the total size of this manifold is significantly reduced compared to the 3 × 3 array; all flow features could be confined into a 6 × 5 × 2.3 mm^3 (L × W × H) for the 9 × 9 manifold compared to an envelope of 25 × 8 x 10 mm^3 for the 3 × 3 manifold. This results in a maximum heat density of 2000 W/cm^3 for the 9 × 9 array compared to a maximum of 285 W/cm^3 for the 3 × 3 array.

5.6 Conclusions

A hierarchical manifold microchannel heat sink was fabricated and tested with integrated microheaters and RTDs. Top layer has a 9 × 9 array of high aspect ratio microchannels which

covers the 5 mm × 5 mm heated area. In order to improve thermal and hydraulic performance, the microchannel heat sinks have short flow paths and deep channels. The hierarchical manifold consists of 8 fluid routing levels which distribute fluid uniformly to the microchannels. Both microchannels and manifolds are fabricated using photolithography and DRIE process. The fabricated channels are aligned using a custom-designed assembly fixture and bonded using thermocompression bonding. Cross section images proved no cracks as well as successful alignment. Heaters and RTDs are patterned directly on top of the microchannel plate and background heaters and hotspot heaters are separately addressable. 4-wire RTDs locally measure the temperature of plate including hotspot temperature. The assembled test device, including the hierarchical manifold, is confined to a 20 × 20 × 3 mm^3 working envelope. With stringent size constraints on most heat sinks, this compact, robust manifold design provides a functional manifold in a small form factor.

The test chip functionality was demonstrated using HFE-7100 as the working fluid. Heat fluxes up to 660 W/cm^2 are dissipated at chip temperatures less than 155 °C and total pressure drops less than 138 kPa during two-phase operation; the corresponding channel pressure drops remained less than 27 kPa (20% of the total pressure drop), which demonstrates the importance of proper manifold design to the overall performance of manifold microchannel heat sinks. These temperatures and pressures are compared to the data from a 3×3 array of heat sinks with a similar channel geometry. For a given flow rate, the 9×9 and 3×3 arrays have similar base temperatures for a given heat flux; however, the pressure drop is lower for the 3×3 array, which has a longer channel length. This increase in pressure drop with decreasing flow length can be attributed to the increase in manifold pressure drop for these extremely small flow lengths.

Table 5.1. Summary of manifold and microchannel dimensions.

Parameter	Value	Units
Channel width	19	μm
Channel height	150	μm
Aspect ratio	7.9	
Fin width	11	μm
Base thickness	50	μm
Plenum inlet length	100	μm
Plenum outlet length	50	μm
Manifold length	175	μm

Table 5.2. Electrical parameters of platinum heaters.

Parameters	Heater	
Type	Background	Hotspot
Resistance (Ω)	333 (each zone)	18
Voltage (V)	96	3.8
Power (W)	27.8 (each zone)	0.8
Current Density (A/cm^2)	7.6×10^6	8.2×10^6

Table 5.3. Key parameters for deep reactive ion etching (DRIE) of high aspect ratio microchannels.

Parameter	Value	Units
Etch rate (approx.)	3	μm/minute
Etch step time	10	seconds
Passivation step time	10	seconds
RF power	1000	Watt
Platen power	10	Watt
C_4F_8 flow rate	100	SCCM
SF_6 flow rate	250	SCCM
O_2 flow rate	30	SCCM

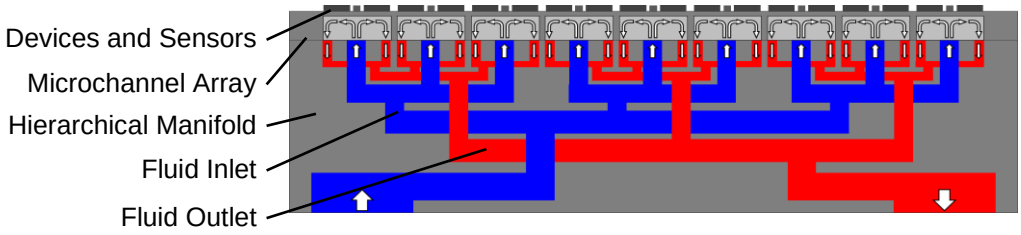


Figure 5.1. Schematic diagram showing a hierarchical manifold microchannel heat sink array.

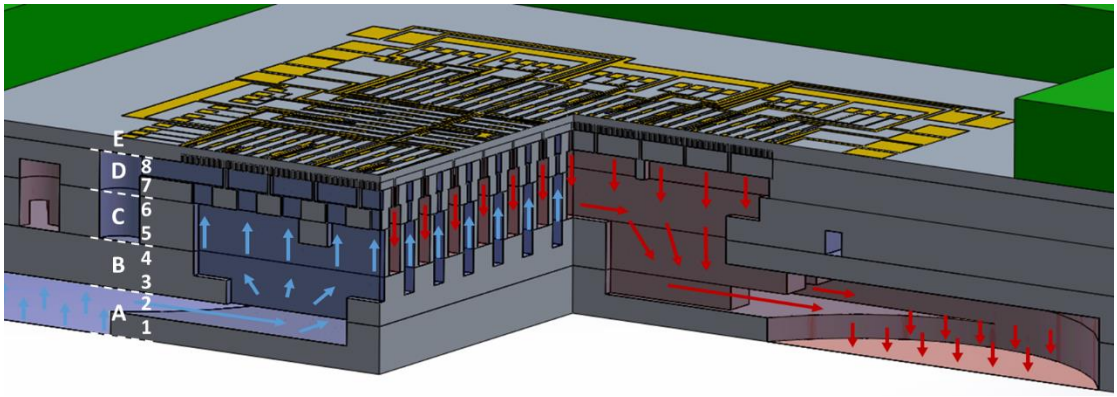


Figure 5.2. CAD model of the hierarchical manifold microchannel heat sink used in this work with sections removed to show internal flow features.

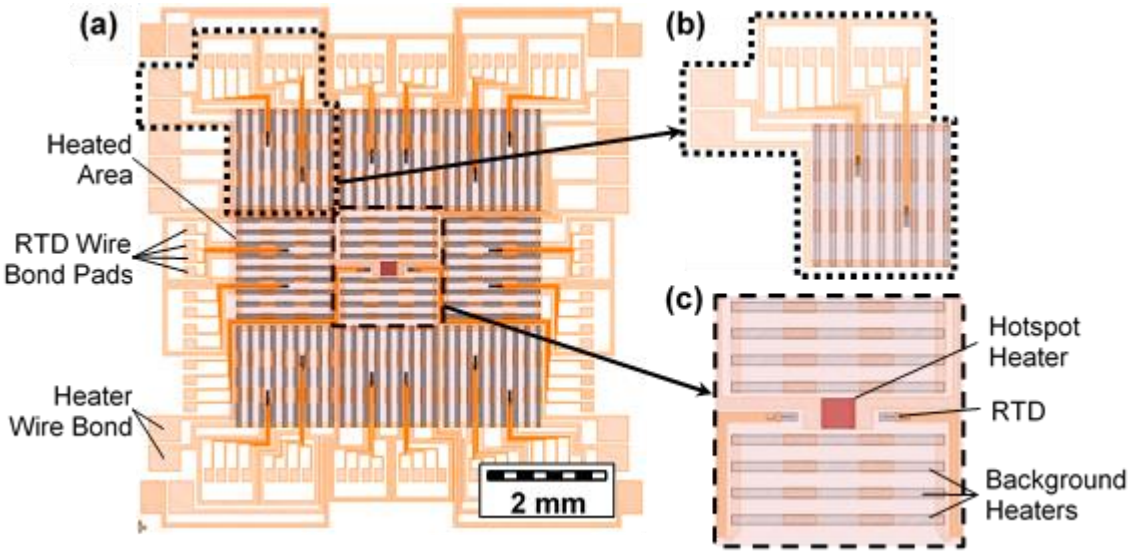


Figure 5.3. Heater/RTD layout.

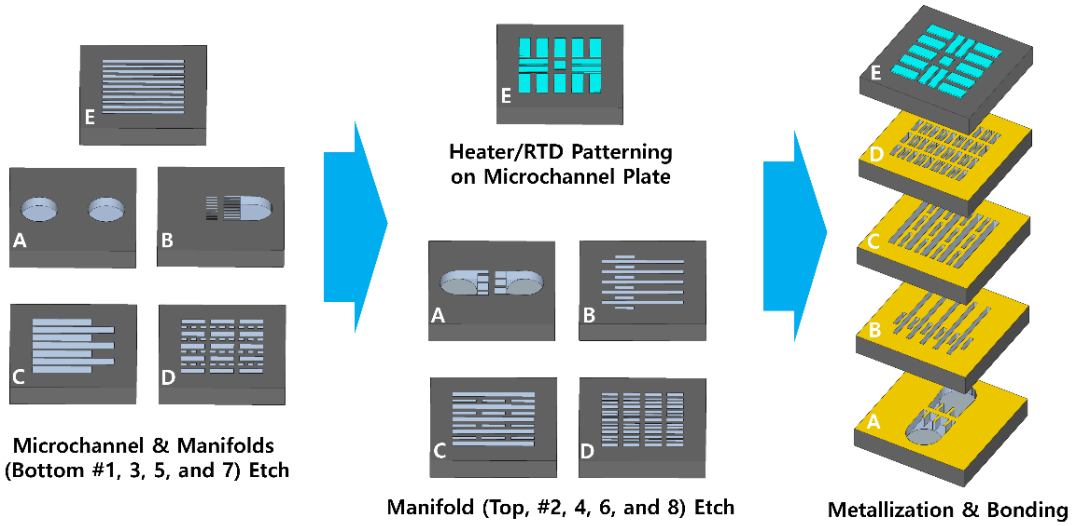


Figure 5.4. Overall fabrication flow (Refer to Figure 5.1 for wafer letters and level numbers).

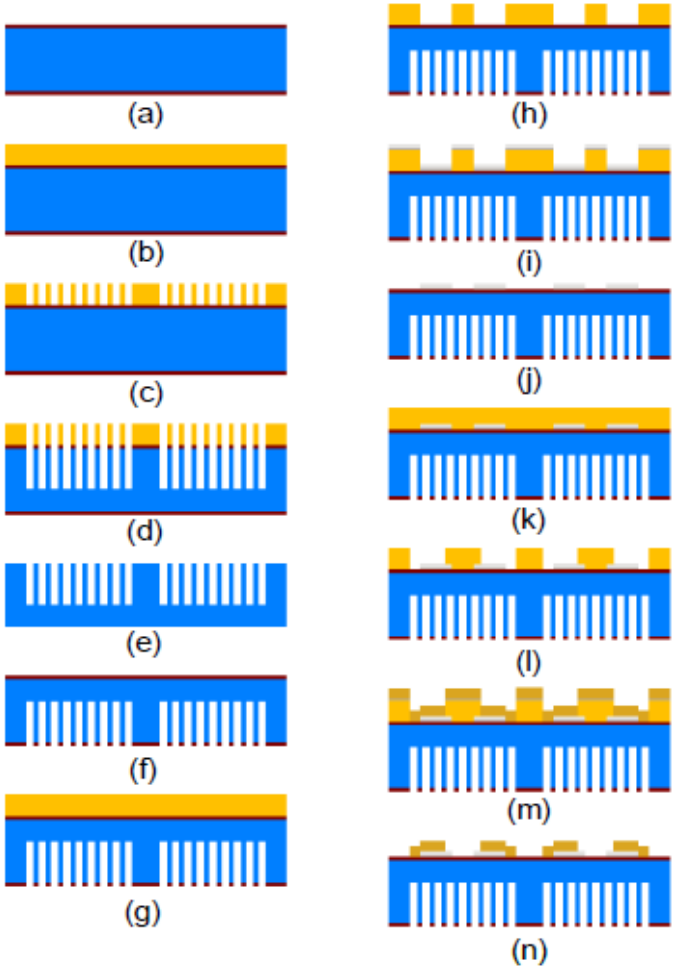


Figure 5.5. Cross-section of microchannel and heater/RTD fabrication process. (a) Piranha clean & oxidation (b) HMDS & PR coating (c) microchannel lithography (d) SiO_2 & Si etch (e) PR removal and BOE (f) piranha clean & oxidation (g) HMDS & PR coating (h) heater/RTD backside lithography (i) Ti and Pt deposition (j) lift-off (k) HMDS & PR coating (l) lead wire lithography (m) Ti and Au deposition and (n) lift-off.

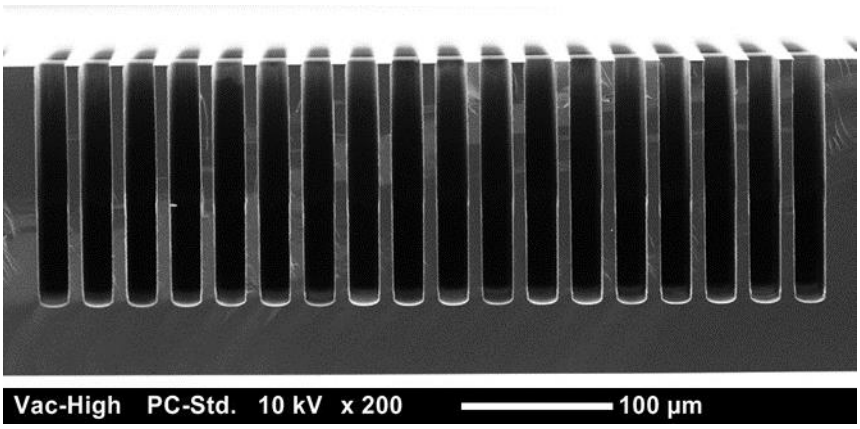


Figure 5.6. SEM image of microchannel cross-section.

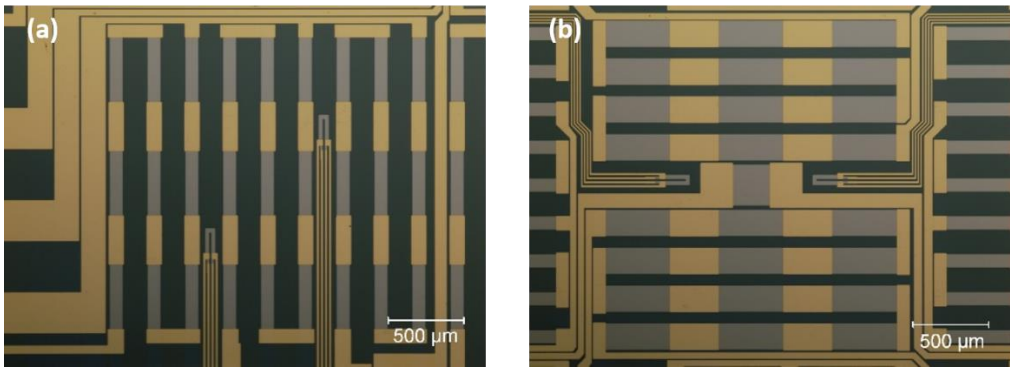


Figure 5.7. Optical images of fabricated heater/RTD. (a) background heater array and (b) center hotspot heater with background heaters.

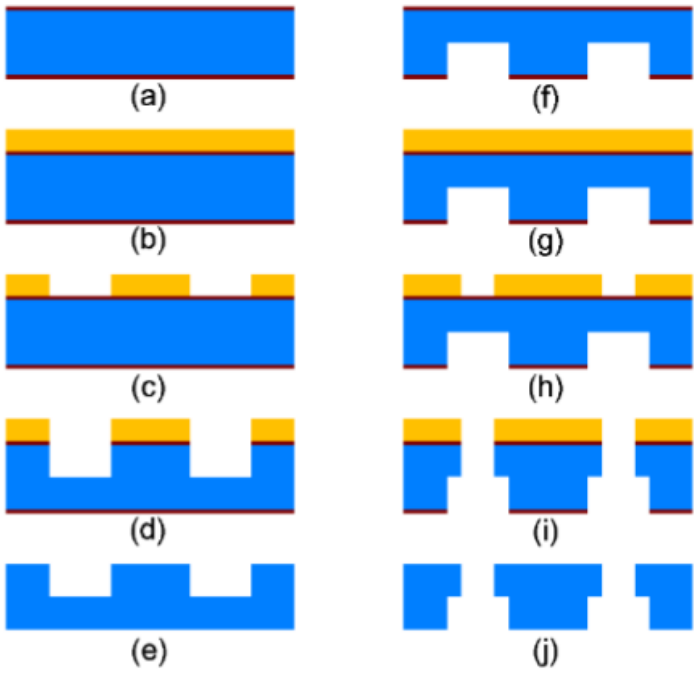


Figure 5.8. Cross-section of manifold fabrication process (a) piranha clean & oxidation (b) HMDS & PR coating (c) bottom-side lithography (d) SiO_2 & Si etch (e) PR removal and BOE (f) piranha clean & oxidation (g) PR coating (h) top-side lithography (i) SiO_2 & Si etch (j) PR removal and BOE.

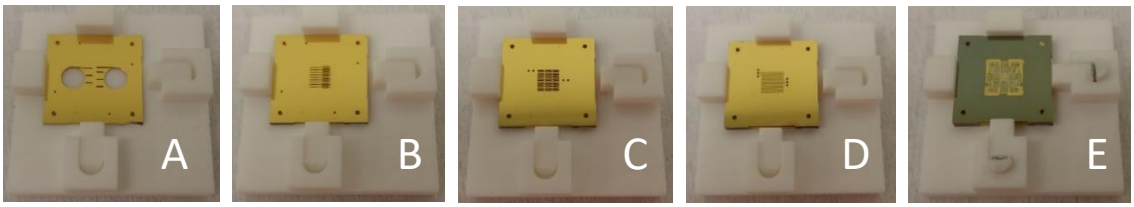


Figure 5.9. Top view of fabricated manifolds (metallized with Ti/Au). Plate labels correspond the labels in Figure 2 and plates are stacked in alphabetical order.

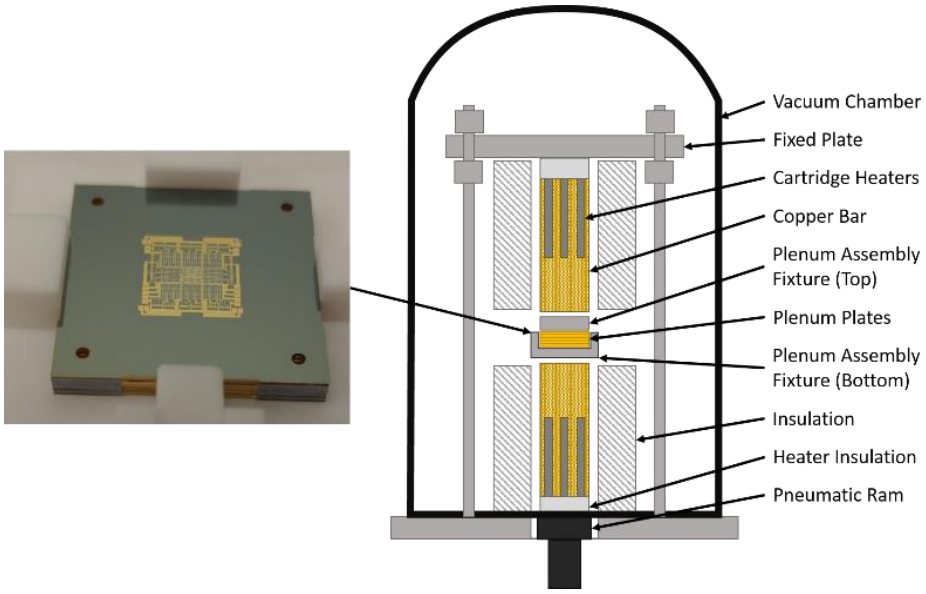


Figure 5.10. Schematic of bonding facility and a bonded chip after thermocompression bonding.

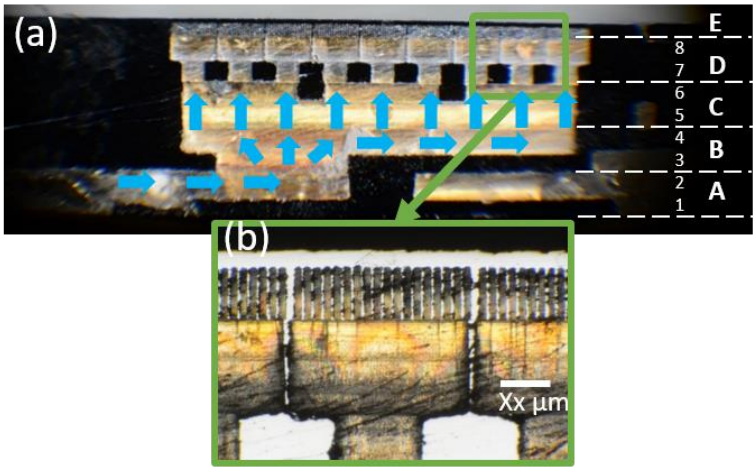


Figure 5.11. (a) Cross-section images of bonded microchannel array test vehicle. Arrows indicate inlet flow direction. (b) Magnified image of top microchannel plate.

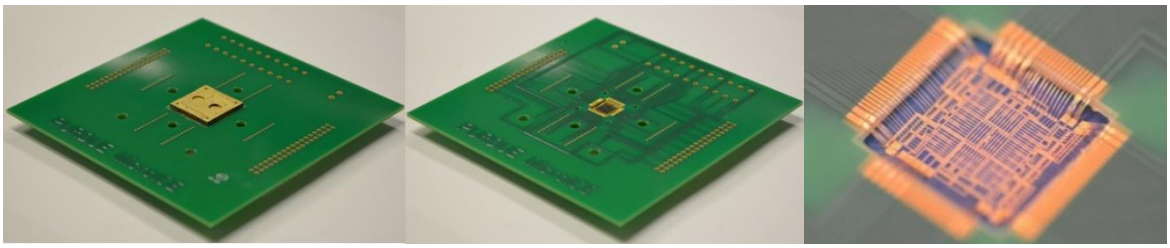


Figure 5.12. Fully assembled microchannel array test vehicle.

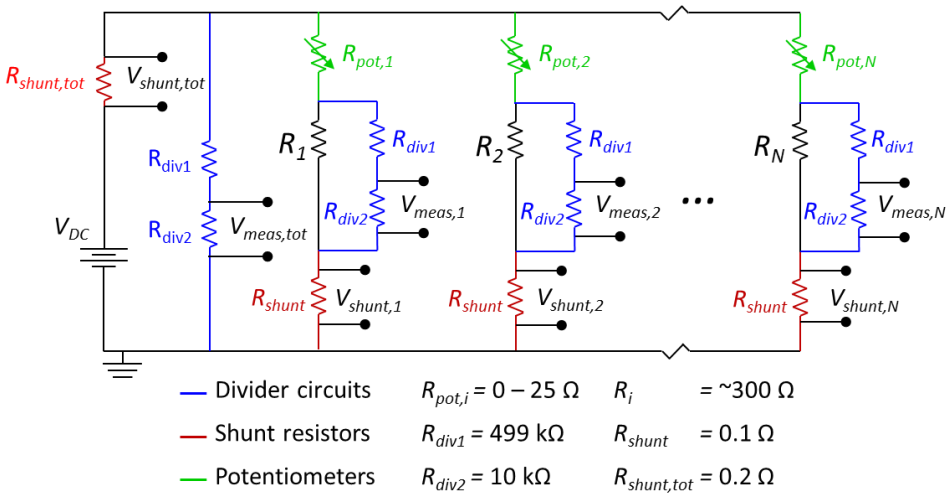


Figure 5.13. Electrical circuit showing the components used to measure heater power to the test vehicle.

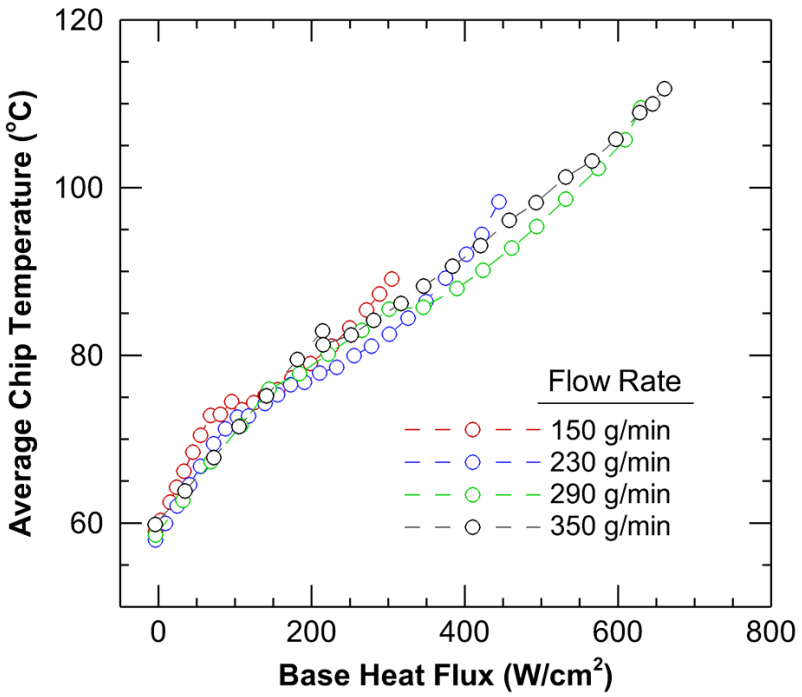


Figure 5.14. Average chip temperature as a function of base heat flux at flow rates of 150, 230, 290, and 350 g/min.

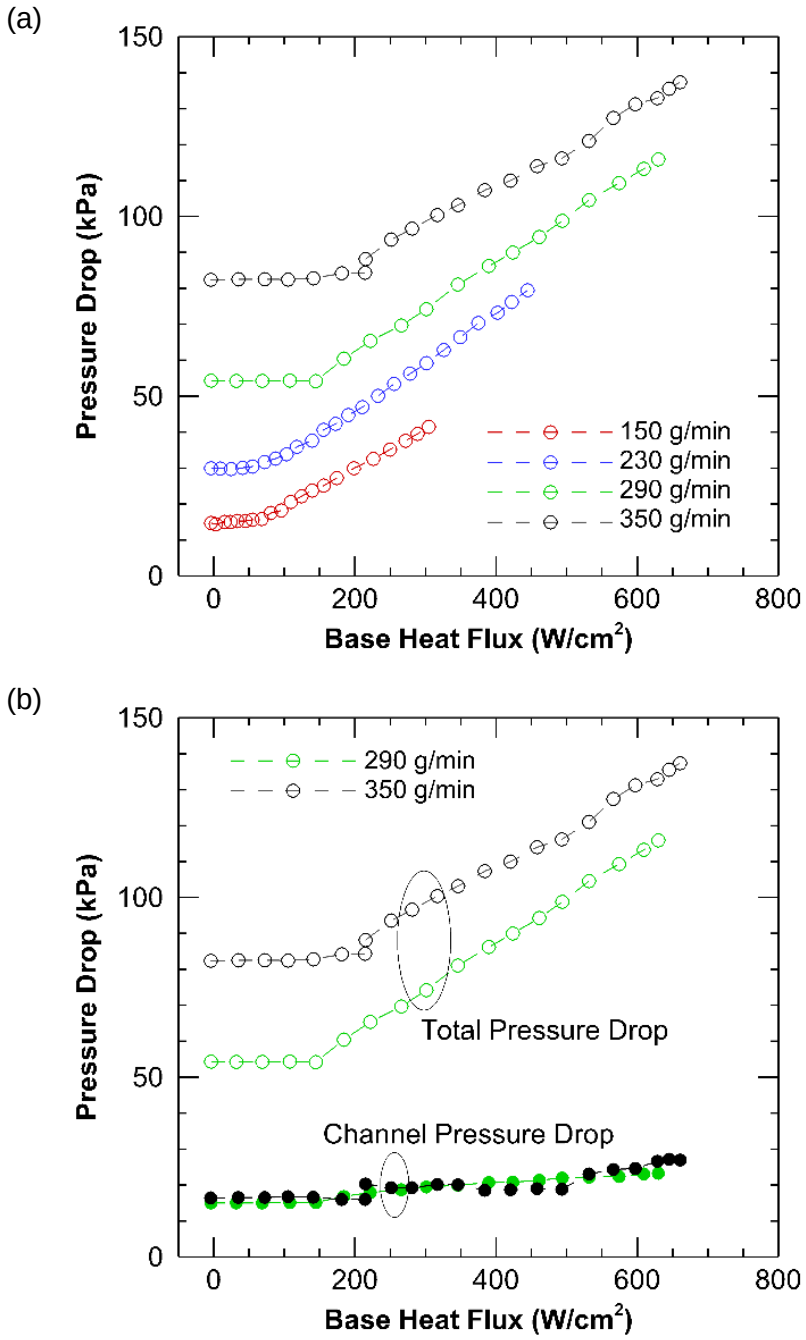


Figure 5.15. (a) Total overall pressure drop as a function of base heat flux at flow rates of 150, 230, 290, and 350 g/min and (b) and the total pressure drop across the test section compared to the channel pressure drops at flow rates of 290 and 350 g/min.

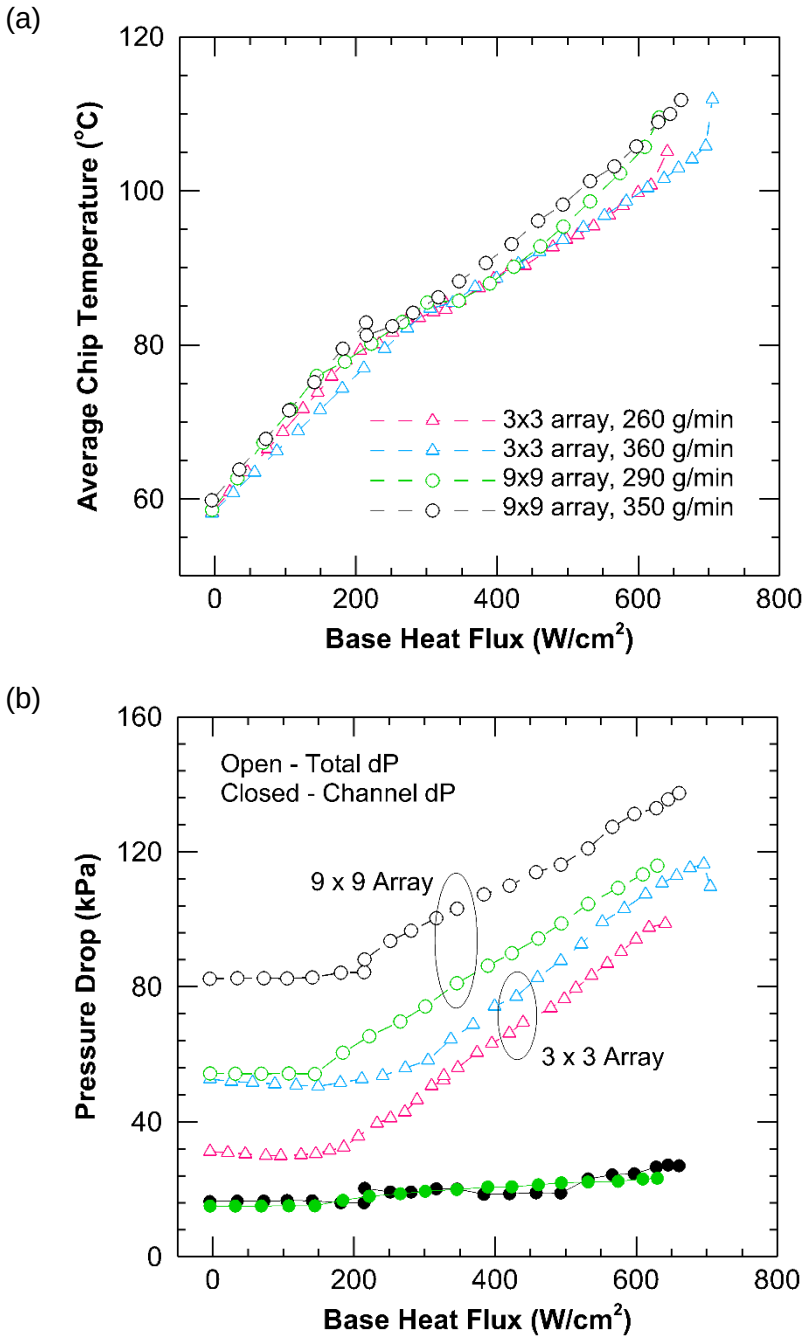


Figure 5.16. (a) Average chip temperature as a function of base heat flux at flow rates of 150, 230, 290, and 350 g/min.

6. THE EFFECTS OF TWO-PHASE FLOW MORPHOLOGY ON LOCAL WALL TEMPERATURES IN HIGH-ASPECT-RATIO MANIFOLD MICROCHANNELS

In this chapter, a single manifold microchannel, representative of a repeating unit in a heat sink, is fabricated in silicon with a bonded glass viewing window. Samples with different channel lengths (750 μm and 1500 μm) and depths (125 μm and 1000 μm) are evaluated; channel and fin widths are both maintained at 60 μm. A high-speed camera is used to visualize the two-phase flow in the channel through the glass sidewall; an infrared camera measures the temperature distribution on the opposite silicon channel sidewall. The flow visualizations provide insight into the flow patterns that emerge in manifold microchannels during two-phase operation; the spatially resolved infrared (IR) temperature measurements allow the effects of flow morphologies to be linked to thermal performance.

6.1 Experimental Test Apparatus

6.1.1 Test device Design

Manifold microchannel heat sinks differ from traditional microchannel heat sinks in their method of fluid delivery to the channels. Manifold microchannel heat sinks distribute fluid along the length of a bank of microchannels such that the effective flow length, and thereby pressure drop, is reduced. In these heat sinks, the fluid enters the channels normal to the heated surface through an inlet manifold, impinges on the channel base, travels along the length of the channel, and exits into an outlet manifold (Figure 6.1). Ideally, the manifold would provide the same amount of fluid to each channel while adding no flow resistance to the system; in practice, the manifold is designed to reduce the manifold pressure drop as much as possible while keeping the flow distribution uniform. Various manifold designs have been proposed with the most common (and simple) being alternating inlet and outlet ducts running perpendicular to the heat sink channels that are connected to a single inlet header and outlet header, respectively [41]. In an effort to reduce flow maldistribution, modified versions of this design have included tapered manifold ducts [42] and hierarchical manifolds with multiple layers [18], [66]. Figure 6.2(a) shows an exploded view of a representative manifold microchannel heat sink and Figure 6.2 (b) shows the assembled

manifold microchannel heat sink with a quarter-symmetry removed for clarity. The manifold microchannel heat sink unit cell, which is the repeating unit of the manifold microchannel heat sink, is shown Figure 6.2(c).

In this work, a single manifold microchannel, representative of a repeating unit in a heat sink, is fabricated in silicon with a bonded glass viewing window. Samples with different channel lengths (750 μm and 1500 μm) and depths (125 μm, 250 μm, and 1000 μm) are fabricated; channel and fin widths are both maintained at 60 μm. Subcooled fluid (HFE-7100) is delivered to the channel at a constant flow rate and a uniform heat flux is applied to the base of the channel. The test device is designed to allow for simultaneous flow visualization and measurement of spatially-resolved temperatures on the backside of the channel.

Figure 6.3 shows a CAD drawing of the test device as viewed from the front side. The channel is positioned such that the channel depth is in the plane of the silicon wafer and the channel width is determined by the etch depth into the wafer; this orientation allows for optical access along the entire channel depth, which is valuable for high-aspect-ratio microchannels where large variations in wall temperature and fluid flow patterns along the channel depth may occur. Fluid enters and exits the microchannel via etched manifold features. Figure 6.3(a) shows the manifold and channel features and Figure 6.3(c) shows the same region with a cut-plane through the inlet manifold to display the base and fin thicknesses. Pressure taps are etched to the same depth as the manifold flow features and are used to measure the fluid pressure immediately before and after the channel. Holes for the inlet and outlet fluid flow paths, inlet and outlet pressure taps, and guide pins are etched through the silicon. The channel is heated from the bottom using an attached ceramic heater and fluid is delivered from the top using manifolds etched into the silicon. Insulation air gaps are etched through the silicon around the heater to direct the heat into the channel.

6.1.2 Test Device Fabrication

All fabrication steps were performed in the Birck Nanotechnology Center at Purdue University.

To begin the test device fabrication, a 4-inch, double-side polished silicon wafer is cleaned using a Piranha solution (3:1 H_2SO_4:H_2O_2). Photoresist (AZ 9260, 7 μm) is spun on one side of the wafer and soft baked (100 °C, 10 min). The photoresist is then exposed to the photomask

containing the channel features (Suss MA6, 72 s) and developed (3:1 AZ400K:H_2O). The 4-inch wafer is then mounted to a 6-inch carrier wafer (Crystalbond 555) and the channel features are etched (STS Advanced Silicon Etch System) to the desired channel width (Figure 6.4(a)). The photoresist is then cleaned (PRS-2000, 100 °C, 8 hr). This process is then repeated for the plenum features (Figure 6.4(b)). The wafer is then flipped over and the process is repeated, this time to remove material from the area of the wafer behind the channel to achieve the proper fin thickness of the unit cell (Figure 6.4(c)). The through-features are etched using the same process (Figure 6.4(d)); this mask includes fluid inlet and outlet holes, pressure taps, holes for alignment pins, and insulation gaps which confine the heat to the channel region. The silicon wafer and a borosilicate glass wafer are then cleaned using a Piranha solution and anodically bonded (Suss SB6e, 350 °C, 1000 V) as shown in Figure 6.4(e). Figure 6.4(f-g) show the etched features as seen from the top and bottom of the wafer. After bonding, the silicon side of the bonded wafer is metalized via electron-beam evaporation (PVD E-beam evaporator); a 10-nm Ti seed layer is coated by a 100-nm copper layer. The 4-inch wafer is then diced into individual test devices. A thin layer of carbon is then deposited on the copper surface, resulting in an IR-opaque, high-emissivity coating. Photographs of the completed test apparatus as viewed from the channel side and fin side are shown in Figure 6.5(a) and (b), respectively.

6.1.3 Assembly of the Test Apparatus

The test apparatus consists of the test apparatus mounted on a PEEK test fixture, a ceramic heater (CER-1-01-00335, Watlow), a PEEK insulation block, as well as gaskets and auxiliary fittings and hardware, as shown in Figure 6.6(a). The test fixture contains fluid ports, thermocouple ports, pressure taps, a cutout for the IR camera to view the sample through, and a cutout for the ceramic heater set. A ceramic insert surrounds the heater to limit the exposure of the PEEK test fixture to high temperatures during testing; a small spring located under the heater provides compression force to maintain contact with the test device throughout testing. A small amount of thermal grease (AS5, Arctic Silver) is applied to the top surface of the heater during assembly to limit the thermal contact resistance between the heater and the test apparatus. A silicone gasket (thickness: 0.38 mm, hardness: 35A) is used to seal the fluid features at the surface between the test fixture and the apparatus; the same gasket material is also placed under the ceramic insert to provide uniform deflection under the apparatus as it is compressed. A PEEK block insulates the

test vehicle from the top and provides a method to mechanically compress and seal the test apparatus to the fixture; the insulation block contains a viewing window to provide optical access for high-speed visualizations in the channel. Stainless steel bolts are paired with springs, washers, and bolts to compress the test apparatus between the PEEK plates. Figure 6.6(b) and (c) show photographs of the assembled test vehicle from the top and bottom sides, respectively.

6.2 Experimental Testing Procedure

6.2.1 Experimental Test Facility

Once assembled, the test vehicle is mounted to an optical rail and all the fittings are attached (Figure 6.6(d)). The fluid inlet and outlet ports are connected to the flow loop, the pressure taps are connected to the pressure transducers, and the thermocouples are placed in the inlet and outlet flow paths. A high-speed camera (Phantom v1212, Vision Research) along with a high-magnification lens (VH-Z100R, Keyence) is mounted to the optical rail facing the top side of the test apparatus. An IR camera (SC7650, FLIR) with a magnifying lens (Asio 4×, Janos) is mounted to the same optical rail facing the test vehicle from the opposite side. The IR camera is positioned such that the channel is located near the top of the window, as shown in Figure 6.7. The alignment of the IR camera is determined using the scale bars that were etched into the test apparatus during fabrication; these scale bars are also used to calculate the precise pixel size of this sensor/lens system, which was measured to be 6.41 μm/pixel. The IR camera has a resolution of 320 × 256, resulting in a viewing window that is 2.05 mm × 1.64 mm.

The flow loop is designed to deliver single-phase HFE-7100 to the test apparatus at a controllable and measurable temperature, flow rate, and pressure. An adjustable-volume reservoir stores the fluid and also contains immersion heaters that are used to degas the fluid prior to testing. A gear pump (GB-P23, Micropump) delivers fluid at a constant flow rate to the test section and the flow rate is measured using a Coriolis mass flow meter (CMF010M, Micromotion). Outlet pressure is measured using a gage pressure transducer (PX302-015G, Omega) and the pressure drop across the test apparatus is measured using a differential pressure transducer (PX409-050DWU5V-EH, Omega). Inlet and outlet temperatures are measured using ungrounded 500 μm-diameter thermocouples with stainless steel sheaths (TJC36-CPSS-020U-6, Omega). The data are recorded using a National Instruments cDAQ-9178 chassis with the appropriate modules and are

monitored using a custom LabVIEW interface. Steady-state temperature, pressure, and flow rate data are collected at 3,000 Hz and averaged over a 20 s period. Flow visualizations are recorded at 70,000 – 115,000 frames per second, depending on the resolution of the images being captured; the IR images are recorded at 10 Hz and are averaged over 20 s to provide a single time-averaged, spatially-resolved temperature map for each test condition.

6.2.2 Infrared Camera Calibration

To calibrate the IR camera, a sample from the same wafer as the test device is mounted to a copper sheet using thermal grease; this sample went through the same fabrication processes and consists of the same materials and surface treatments as the test device. A thermocouple (TJC36-CPSS-020U-6, Omega) is placed on the sample surface with a small bead of thermal paste on the tip. A resistive heater is attached to the opposite side of the copper sheet. This fixture is then placed on the optical rail above the infrared camera and brought into focus. The integration time, measurement frequency, and measurement time for the camera are set (175 μs, 10 Hz, 20 s). The power to the heater is increased in increments that resulted in 10 temperatures spanning the range of temperatures experienced during testing (35 °C – 120 °C). The intensity is measured for each pixel for each steady-state point. The thermocouple temperature measures the sample surface temperature, which is assumed to uniform across the IR viewing window. A calibration algorithm determines the nonuniformity across the infrared image and fits a fourth-order polynomial for each pixel. Because the calibration surface and the test apparatus surface have the same properties, the emissivity is accounted for directly.

6.2.3 Data Reduction

The heat flux is calculated based on the temperatures over spanning from 100 μm below the channel bottom to the edge of the IR viewing region (Figure 6.7(b)); the region nearest the channel is excluded due nonuniformity caused by three-dimensional conduction effects due to the channel geometry and nonuniform heat transfer coefficients in the channel. To limit the contribution of edge effects, only the central region is used in the heat flux calculation. The temperatures in the area of interest are averaged across the *z*-direction, resulting in an array of z-averaged temperatures along the *y*-direction. Figure 6.8 shows representative z-averaged temperatures as a function of *y* position in the heat flux region for a heat flux of 148 W/cm^2; the

dashed line shows the first-order linear regression that is fit to these data with the slope being the temperature gradient. Once the temperature gradient is calculated, base heat flux can be calculated assuming one-dimensional heat conduction: $q''_{base} = -k_{Si} \frac{dT(y)}{dy}$. The channel base temperature is calculated by averaging the temperatures at the bottom of the channel region in the *z*-direction.

6.2.4 Uncertainty

The measurement uncertainties of each instrument in the experimental test facility are obtained from the manufacturers' specifications and are listed in

Table 6.1. The uncertainty in the wall temperature is estimated based on the uncertainty in the calibration procedure as well as the uncertainty in the reference thermocouple. The uncertainty in the heat flux calculation is based on the uncertainties in the wall temperature measurements, the position, and the goodness of the linear fit and the uncertainty in the pixel size.

6.2.5 Testing Conditions

The critical parameters for the three test devices are shown in Table 6.2. These channel geometries were chosen to provide a range of aspect ratios ($AR = d_c / w_c$) and nondimensional lengths ($L_{nd} = L_c / h_c$). At low aspect ratios, the wall temperature is relatively constant along the channel height; as aspect ratio increases, the temperature drop along the channel height increases. Small nondimensional lengths lead to nonuniform flow along the channel height where the velocity at the top of the channels is significantly larger than at the channel base. Sample 1 consists of a low-aspect-ratio microchannel that closely resembles a traditional microchannel, with a large nondimensional length and relatively low aspect ratio. Sample 3, on the other hand, is a high-aspect-ratio microchannel (AR = 16.7) with a nondimensional length less than unity. Sample 2 provides an intermediate aspect ratio and nondimensional length to help understand the trends with these two variables. The samples are tested at flow rates that provide a fluid velocity of 1.05 - 1.1 m/s at the inlet to the channel.

6.3 Results and Discussion

This section describes the steady-state data that are spatially and temporally averaged; trends in base temperature and pressure drop as a function of heat flux and channel geometry are presented. To help understand the thermal-hydraulic trends, flow visualization images are then presented for select two-phase operating points.

6.3.1 Steady-State, Time-Averaged Experimental Results

Figure 6.9(a) shows channel base temperatures for the range of heat fluxes tested for each sample. The open symbols signify single-phase operation and the closed symbols represent two-phase operation. For all samples, testing was terminated due to heater temperature limits rather than reaching critical heat flux in the channel. Sample 1 remains in single-phase operation up to 100 W/cm^2; in this single-phase region, the temperature rise with increasing heat flux is linear, which is characteristic of single-phase flow. Upon boiling insipience at 100 W/cm^2, the base temperature decreases. During two-phase operation, the slope of the boiling curve increases compared to single-phase operation because of the increased heat transfer coefficient during flow boiling. For Sample 1, the temperature rise with heat flux remains constant throughout two-phase operation. Boiling is initiated in Samples 2 and 3 at approximately 40 W/cm^2, upon which both samples show a slight increase in slope. During two-phase operation, Sample 3 shows a much more irregular temperature response to applied heat flux, which is not seen in most traditional microchannel systems; between 75 and 116 W/cm^2, the temperature rises linearly at which point the temperature rises 3 °C with a slight increase in heat flux and above 116 W/cm^2 the temperature rise is again linear.

Figure 6.9(b) shows the pressure drop as a function of heat flux for the three samples. During single-phase operation, pressure drop remains relatively constant with heat flux for each sample. Upon incipience, pressure drop increases sharply due to the increase in bulk fluid velocity in the channel. The pressure drop increases linearly with increasing heat flux in the two-phase regime due to the increase in vapor quality leading to larger velocities.

6.3.2 Flow Morphology and Spatially Resolved Wall Temperatures

High-speed flow visualization provides useful information pertaining to the two-phase flow structure, which affords unique insights into the mechanisms that cause the steady-state, spatially-averaged data shown in Section 6.3.1.

6.3.2.1 Low-Aspect-Ratio Microchannel (Sample 1)

Figure 6.10(a) shows the measured wall temperature distributions normalized against the maximum wall temperature measured at that operating point for all steady-state operating points shown in Figure 6.9 for Sample 1; flow visualizations are shown for all operating points where boiling occurs (Figure 6.10(b)). During single-phase operation, subcooled fluid enters the channel and is heated along its length, as shown in the temperature maps in Figure 6.10(a) for heat fluxes from 6 – 98 W/cm². At the lowest heat flux after incipience (116 W/cm²), vapor nucleates at the top surface of the channel, the bottom corner near the exit plenum, and at the top of the fin at the exit. Vapor bubbles nucleate at these sites, grow, depart, and become entrained in the bulk flow. At the outlet plenum, the flow becomes well-mixed due to the bend in the flow path. As heat flux is increased (116 – 202 W/cm²), the number of nucleation sites increases and the sites move toward the inlet plenum. For all heat fluxes, the flow is extremely stable and temporally consistent (see Supplemental Materials).

While the wall temperature profiles for each heat flux during single-phase operation are similar to each other as are the profiles during two-phase operation, the transition from single-phase to two-phase operation brings with it a drastic change in the wall temperature profile. During single-phase operation (<98 W/cm²), the region immediately under the fluid inlet is consistently the coolest region due to the fluid arriving subcooled as well as impingement and developing flow effects; this same region becomes the hottest during two-phase operation. At heat fluxes of 116 and 133 W/cm², boiling is suppressed in the region below the fluid inlet, which could cause the relatively higher temperature compared to the downstream regions with boiling; at heat fluxes133 W/cm², a relatively stable vapor bubble embryo forms in this region, which could also lead to the local relative increase in temperature. During saturated flow boiling, the fluid will cool down along the length of a channel due to the decrease in saturation temperature with decreasing pressure; each two-phase temperature profile shows a decrease in temperature along the length of the channel and also a sharp drop near the expansion to the outlet plenum. Also, the fluid is delivered

to the test device at a constant temperature, but the fluid is being preheated in the plenum region for higher heat fluxes; this results in a higher fluid inlet temperature, which eliminates the relatively cool region near the inlet plenum present in the low-heat-flux operating points. The temperature drop along the height of the channel is less than 2 °C for all heat fluxes, which can be attributed to the shallow channel depth.

6.3.2.2 Medium-Aspect-Ratio Microchannel (Sample 2)

Figure 6.11 shows the time-averaged wall temperature maps (Figure 6.11(a)) and images of the two-phase flow in Sample 2 (Figure 6.11(b)). The wall temperatures are plotted with respect to the maximum temperature measured at each heat flux. The wall temperatures are very uniform during single-phase operation (12, 35 W/cm²), with all local wall temperatures within 2 °C of each other at each heat flux. Like Sample 1, the wall temperature profile changes significantly upon incipience, where the regions near the inlet and outlet plenums have the lowest and highest relative wall temperatures, respectively; this trend of decreasing wall temperature along the flow length remains throughout two-phase operation (85 – 137 W/cm²). At the highest heat fluxes tested (137 W/cm²), the wall temperature profile becomes more symmetric about the channel midplane. The maximum temperature difference is approximately 6 °C, which occurs at 137 W/cm².

At the first steady-state heat flux after incipience (85 W/cm²), vapor nucleates at the sidewall beneath the inlet plenum and is dragged into the bulk flow. A stagnant vapor bubble is confined to the region under the channel top wall; vapor is pinched off from this vapor plume where the top wall and outlet plenum meet. As heat flux is increased (106, 127 W/cm²), discreet bubble are still visible throughout most of the flow length, with mixing occurring near the end of the channel under the outlet plenum. At heat fluxes between 85 and 143 W/cm² , the stagnant vapor bubble remains pinned to the channel top wall. This vapor structure is disrupted by the large amounts of vapor generated at higher heat fluxes (136 – 138 W/cm² observed anywhere in the channel other than the small region under the channel top wall where the stagnant bubble occupies

6.3.2.3 High-Aspect-Ratio Microchannel (Sample 3)

While the two-phase flow morphologies for Samples 1 and 2 were largely temporally invariable, the flow morphology for Sample 3 exhibits extreme, time-periodic variations. Figure 6.12 shows a sequence of images for three selected heat fluxes along with the time-averaged wall

temperatures at these heat fluxes. In Figure 6.12(a), at 89 W/cm², the channel starts (0.00 ms) with the bottom portion largely covered in vapor with most of the fluid bypassing the bottom half of the channel; nucleation is largely occurring at the sidewall near the outlet and below the manifold near the inlet. The amount of vapor being generated bridges the entire channel height, temporarily restricting the flow (0.27 ms). This restriction causes the liquid arriving from the inlet to move toward the channel bottom, impinge on the bottom of the channel (0.54 ms), and spread along the channel bottom (1.07 ms). The vapor blanket is then reformed (2.75 ms) and the cycle repeats. The resulting temperature map (Figure 6.12(b)) shows a large temperature gradient along the channel height from the base to the fin tips; for a given height on the fin, the temperature is largely unchanged along the flow length direction. The trends for the higher heat flux of 115 W/cm² are largely the same, with a vapor blanket present along the bottom of the channel and a periodic rewetting of the entire channel base (Figure 6.12(c)). At the highest heat flux tested for this channel geometry (148 W/cm²), the liquid is not able to re-wet the entire channel base, as shown in Figure 6.12(e). Unlike at the lower heat fluxes, the region near the bottom corner under the inlet is continuously coated in vapor and the channel base is only rewetted near the corner under the outlet. This leads to a temperature gradient along the channel length, with the hottest region near the channel base close to the inlet (in addition to the temperature gradient along the channel height, which persists).

6.3.3 Discussion

In traditional heat sinks, increasing channel depth provides a straightforward method to increase surface area for heat transfer necessary to dissipate high heat fluxes. For manifold microchannel heat sinks, where the fluid arrives at the top of the channel, the two-phase flow morphology plays a large role in determining an optimal channel depth. As shown for Sample 3, the fluid inlet velocity is insufficient to disrupt the vapor blanket that forms on the bottom of the channel at high heat fluxes; this causes large regions of the channel to largely remain dried out and not contribute to the heat removal. Sample 2, which has a 4× reduction in wetted area compared to Sample 3, consistently provides lower wall temperatures for the same flow rate and similar pressure drops, which is not seen in traditional microchannels. Sample 2 did not show any local dryout near the channel base for any base flux tested. Sample 3, on the other hand, showed a large vapor blanket that is present throughout two-phase operation and only re-wets intermittently.

Because the heat transfer coefficient in this vapor-filled region will be extremely poor, this wall area does not contribute significantly to the overall heat removal. Additionally, Sample 3 has a temperature drop of approximately 12 °C from the bottom of the channel to the top. Because the vapor blanket is located at the bottom of the channel where the wall temperature is highest, this has the added consequence of having high heat transfer coefficients in areas with relatively small wall temperature superheats.

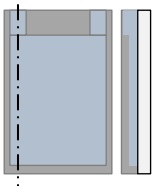
6.4 Conclusions

Simultaneous high-speed visualizations of the flow morphology and infrared channel wall temperature maps are presented for two-phase flow in a manifold microchannel. Test devices with different flow lengths and channel depths are experimentally evaluated using HFE-7100 as the working fluid. During single-phase operation, the wall region near the inlet manifold has the coldest temperatures and the wall becomes hotter along the fluid flow length. For the deepest channels, stagnant vapor becomes intermittently trapped at the bottom portion of the channel, thereby limiting the amount of local heat transfer and increasing the wall temperature near the channel base. At high heat fluxes, the vapor blanket in some regions is not able to be temporarily disrupted by liquid that impinges on the channel base, leading to a high local wall temperature in these regions. The temperature difference between the bottom and top of the deepest channel becomes larger than 12 °C at a heat flux of 148 W/cm², demonstrating the importance of fin effects in high-aspect-ration microchannels. The consequence for having extremely deep channels with short flow lengths is demonstrated when comparing the two samples with equal flow lengths (750 μm) and channel depths of 250 μm and 1000 μm. While the deeper channel has ~4 times the surface area of the shallower channel, the base temperatures are lower for the shallower channel for a given base heat flux. The vapor blanketing the bottom of the channel insulates this region; while the upper region of the channel still has the high heat transfer coefficients, the temperature drop along the fin height leads to relatively high base temperatures to maintain the necessary wall superheat in the upper region.

Table 6.1. Uncertainty in measured and calculated data

Measurement	Instrument	Manufacturer	Uncertainty
Wall temperature	IR camera	FLIR	± 1.5 °C
Location	IR camera	FLIR	10 μm
Heat flux	IR camera	FLIR	± 5 W/cm²
Fluid inlet temperature	T-type thermocouple	Omega	± 0.5 °C
Fluid outlet temperature	T-type thermocouple	Omega	± 0.5 °C
Pressure drop	Differential pressure transducer	Omega	± 0.17 kPa
Mass flow rate	Coriolis mass flow meter	Micromotion	± 5.0 %

Table 6.2. Summary of microchannel dimensions and operating conditions. The embedded figures show a view of the channel from the front and a cross sectional view when cut through the inlet plenum.

Sample	*Channel Length* L_c (μm)	*Inlet Plenum Length* L_{in} (μm)	*Outlet Plenum Length* L_{out} (μm)	*Channel Depth* d_c (μm)	*Aspect Ratio* AR (-)	*Normalized Length* L_{nd} (-)
1 	1500	400	400	125	2.1	12
2 	750	200	200	250	4.2	3
3 	750	200	200	1000	16.7	0.75

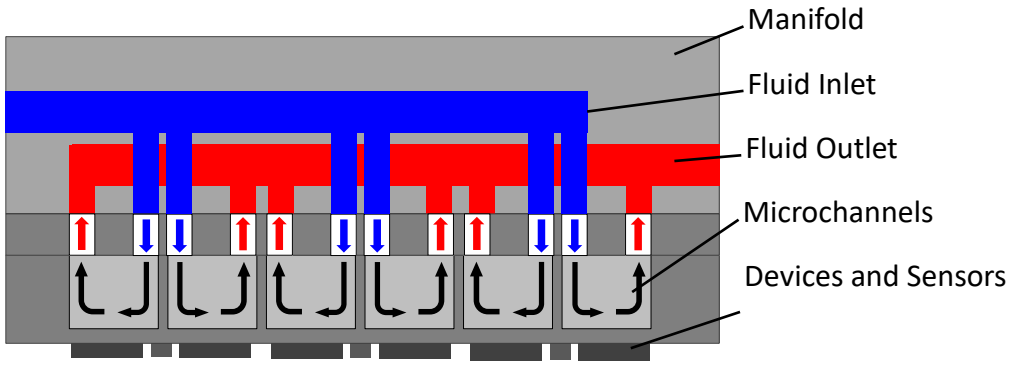


Figure 6.1. Schematic diagram of a manifold microchannel heat sink.

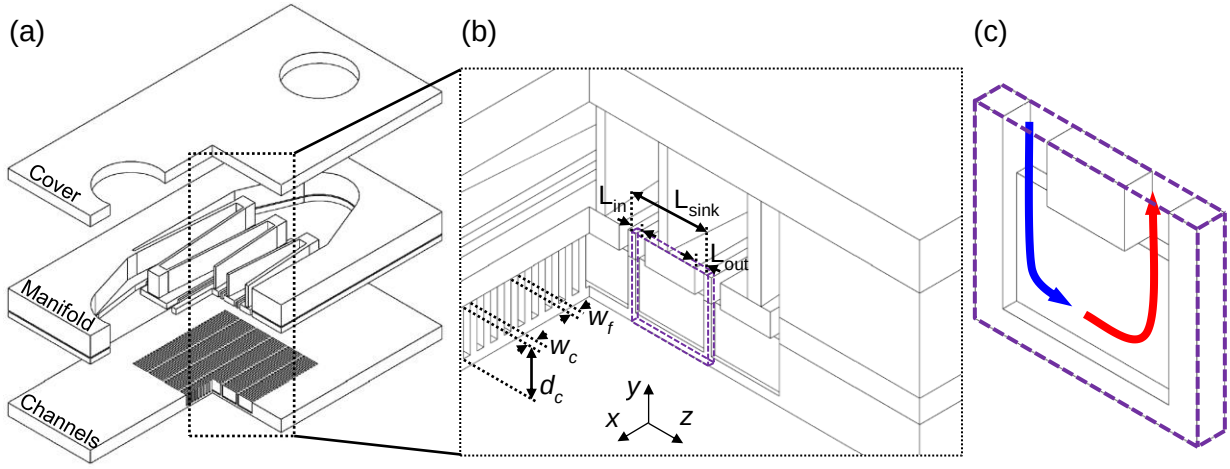


Figure 6.2. (a) Exploded view of a manifold microchannel (MMC) heat sink with a quarter-section removed, (b) the same MMC heat sink with the critical channel dimensions labeled, and (c) the MMC unit cell with the flow inlet and outlet paths shown.

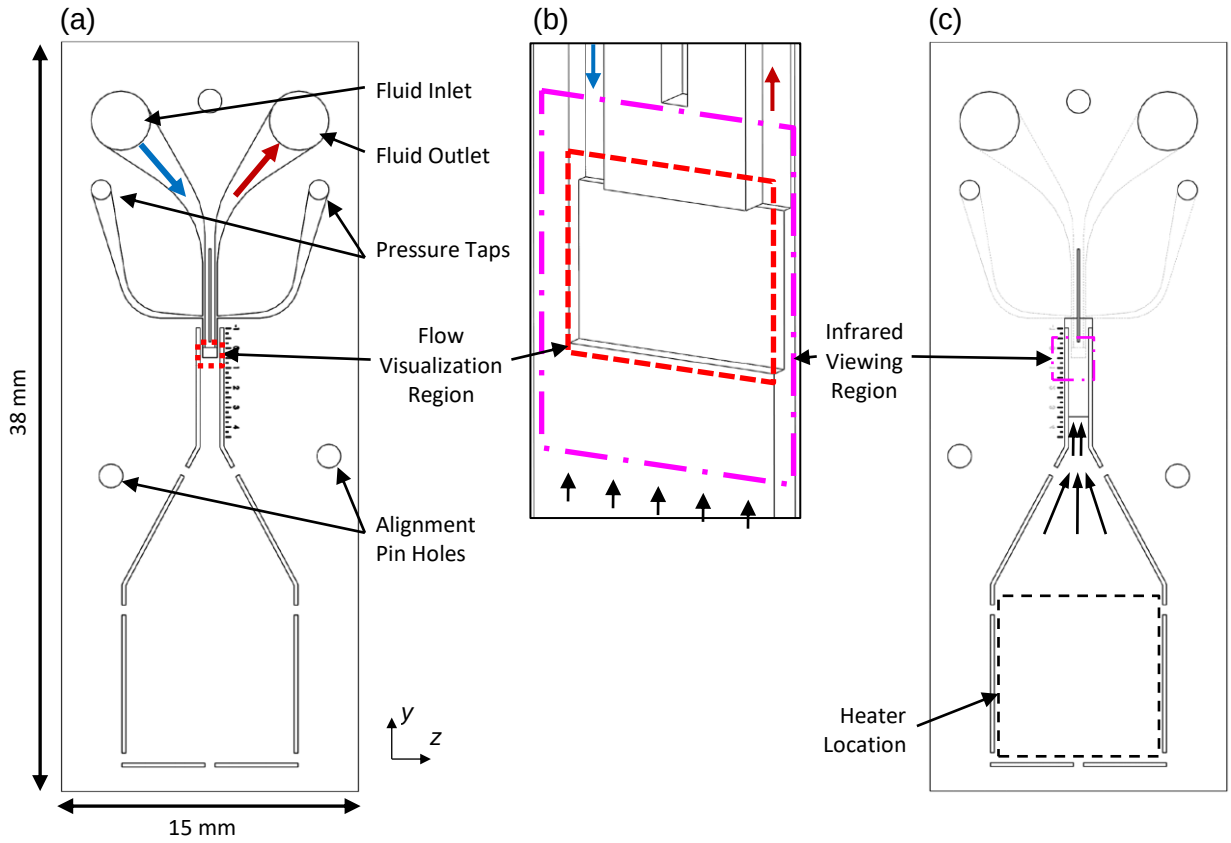


Figure 6.3. CAD drawings of the test device: (a) front side with arrows showing the heat flow path to the channel (black) and the fluid inlet (blue) and outlet (red), (b) inset of the channel region viewed at an angle with a section removed to view the channel cross-section, and (c) back side of the test device.

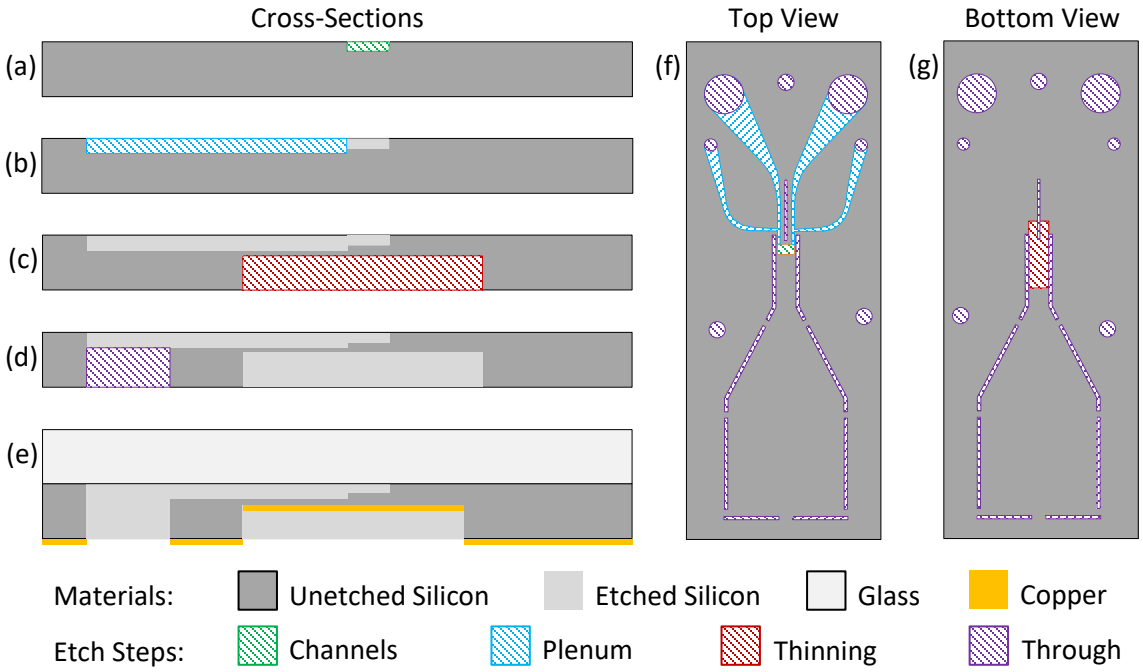


Figure 6.4. (a-e) Schematic diagrams showing the test device cross-sections throughout the fabrication procedure and (f) top and (g) bottom schematic diagrams after fabrication. Dimensions are not to scale.

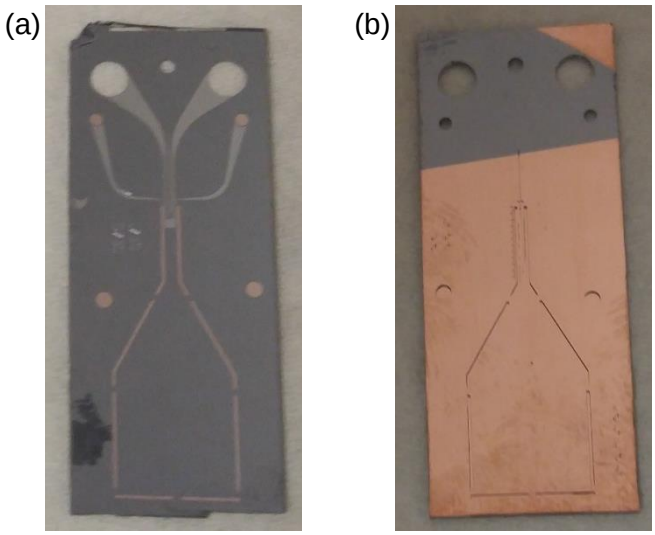


Figure 6.5. Photographs of a test apparatus from the (a) front side and (b) back side.

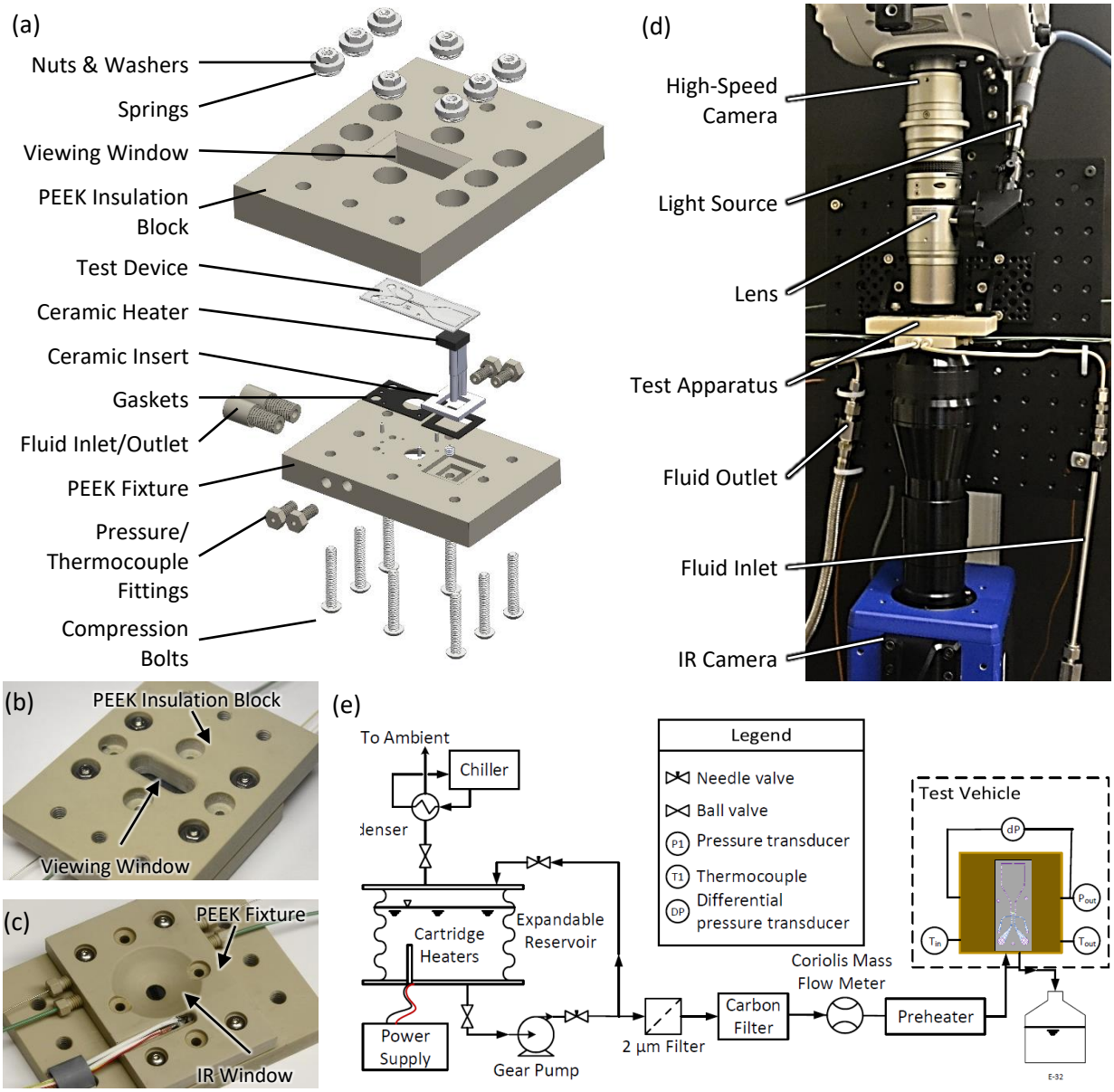


Figure 6.6. (a) Exploded view of the test section assembly, and photographs of the test vehicle from the (b) top side, which contains a viewing window for high-speed visualizations and (c) bottom side, showing the pressure taps, thermocouples, heater leads, and IR viewing window, (d) photograph of the test vehicle assembled in the flow loop with the IR camera and high-speed camera mounted, and (e) a schematic diagram of the experimental flow loop.

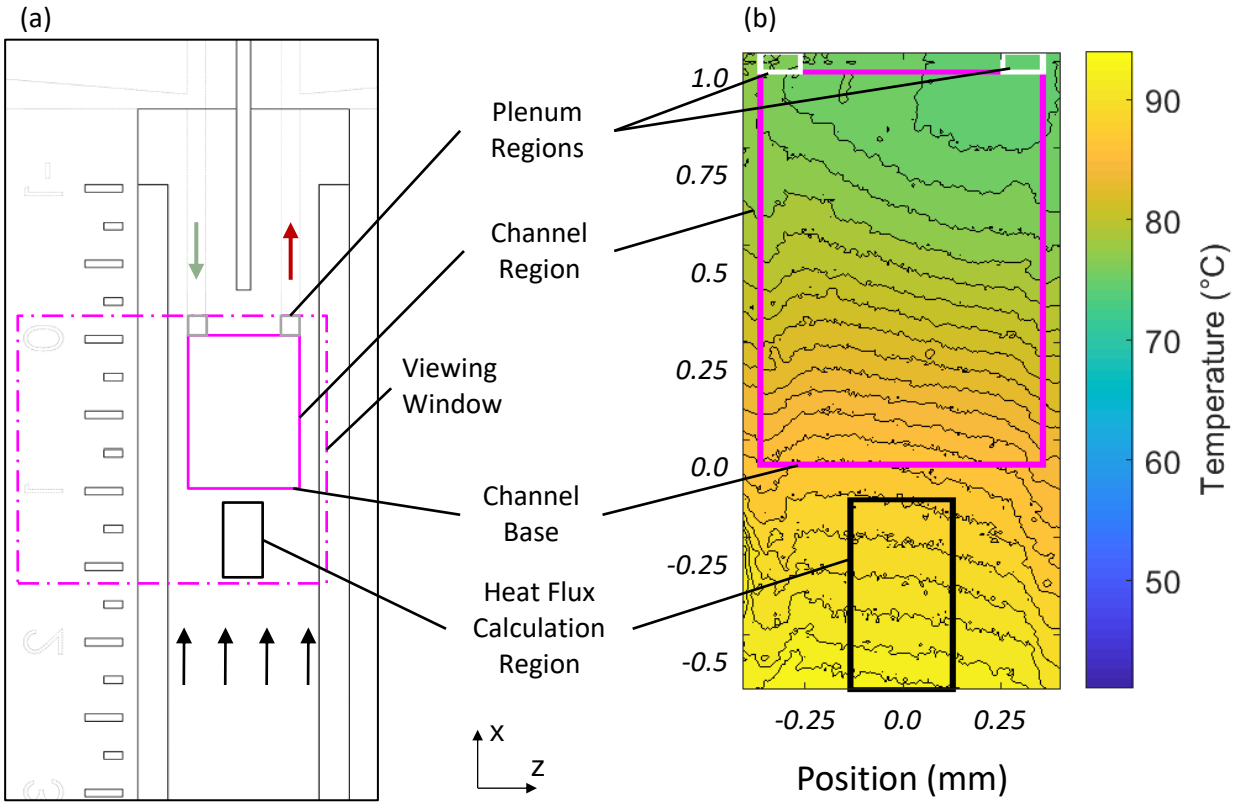


Figure 6.7. (a) CAD model of the test device (Sample 3, 750 × 1000 μm) viewed from the back side showing the position of the uncropped IR viewing region and (b) a sample temperature map showing the region used to calculate heat flux into the channel and the channel region.

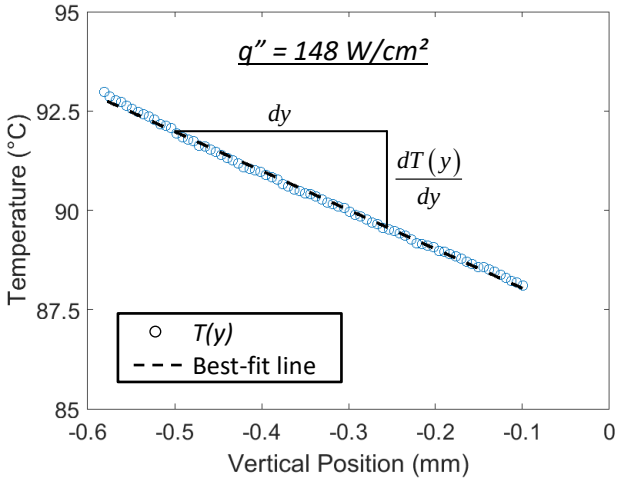


Figure 6.8. A representative set of *z*-averaged temperature measurements as a function of vertical position for Sample 3 at a heat flux of 148 W/cm² along with the best-fit line for these data.

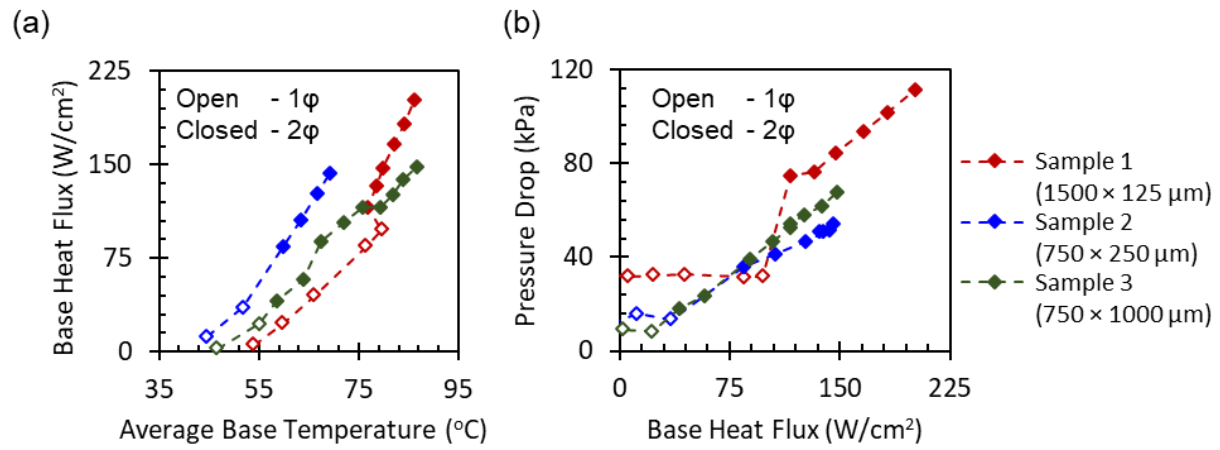


Figure 6.9. (a) Base heat flux as a function of base temperature and (b) pressure drop as a function of base heat flux for each channel geometry.

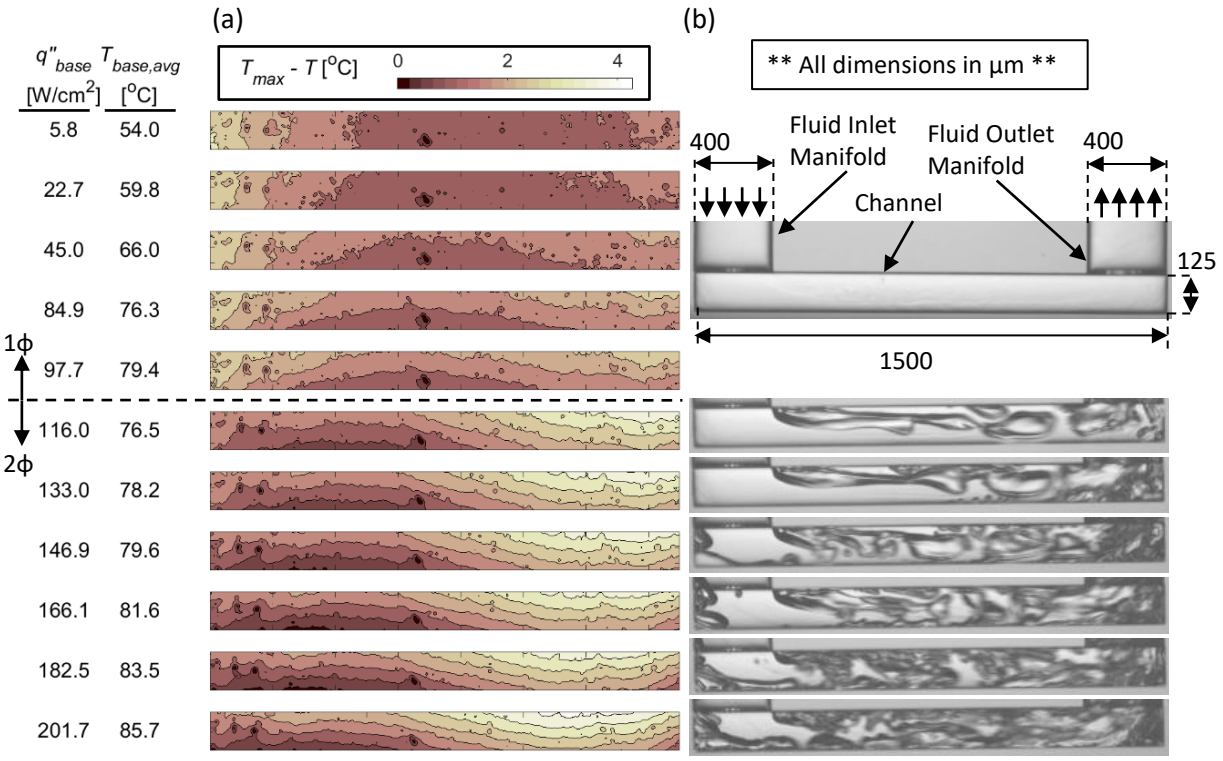


Figure 6.10. (a) Wall temperature maps for Sample 1 (1500 × 125 µm) over the range of heat flux inputs shown in Figure 6.9. The relative temperature range remains constant while the absolute temperature scales change for each plot. (b) Flow visualization images are shown during two-phase operation.

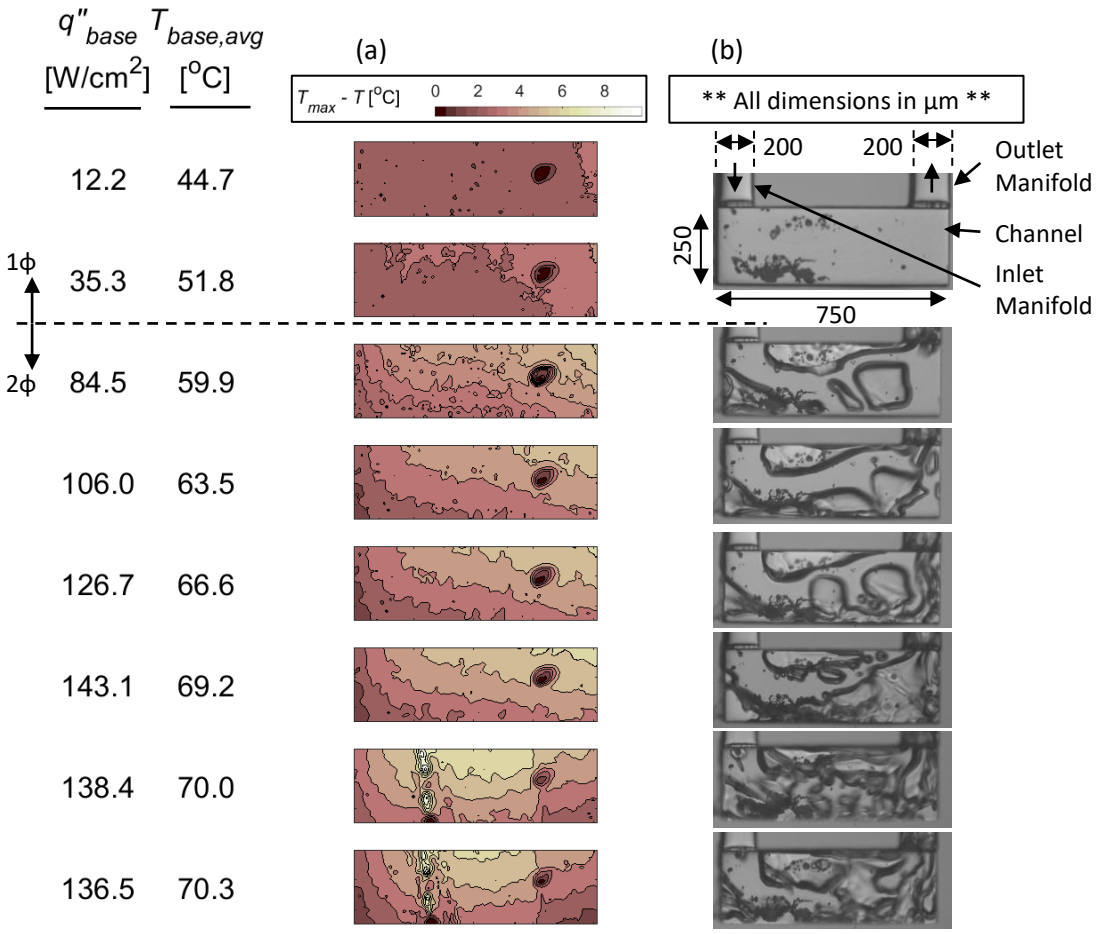


Figure 6.11. (a) Wall temperature maps for Sample 2 (750 × 250 µm) over the range of heat flux inputs shown in Figure 6.9. The relative temperature range remains constant while the absolute temperature scales change for each plot. (b) Flow visualization images are shown during two-phase operation.

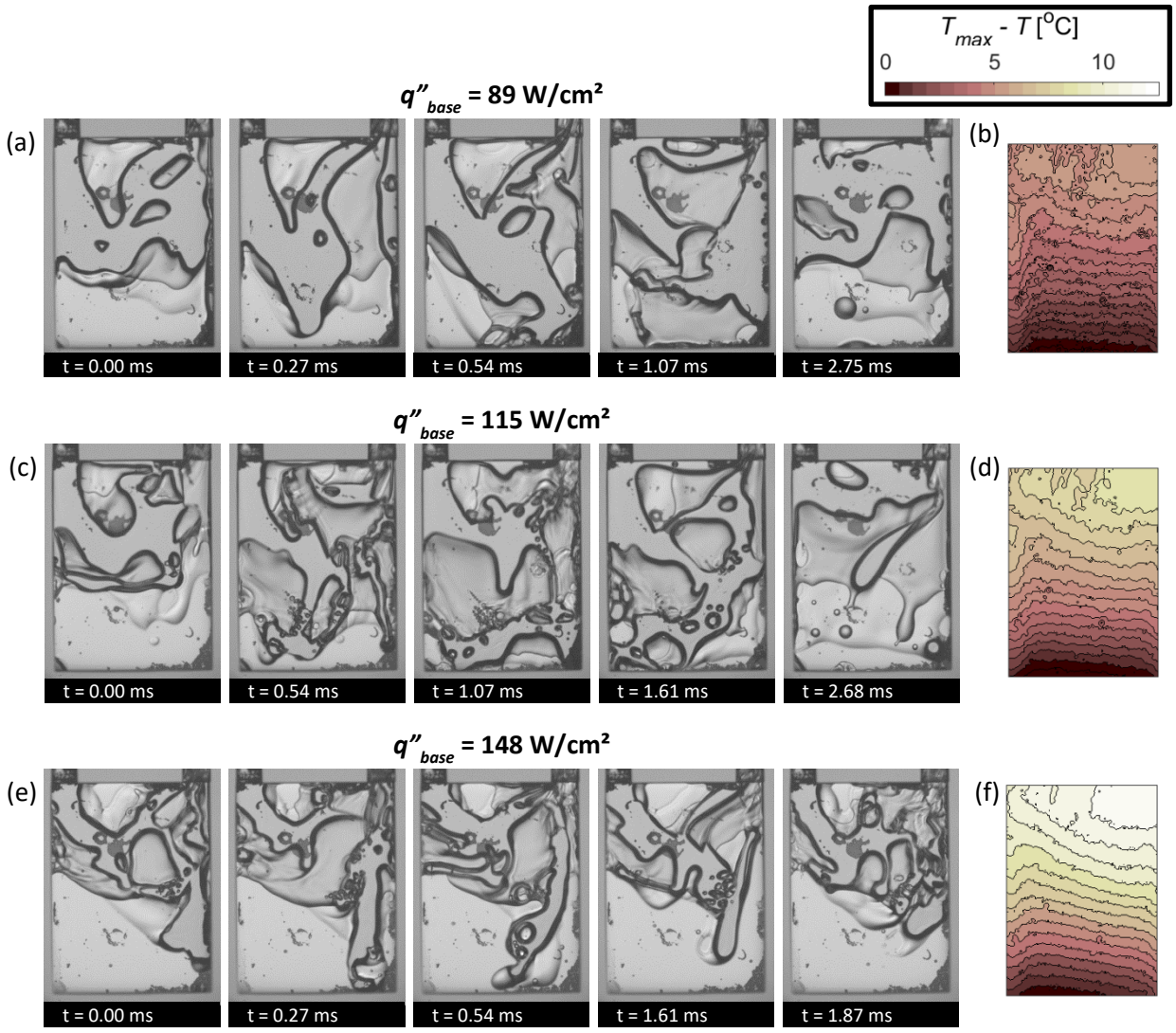


Figure 6.12. High-speed images showing the two-phase flow inside the channel of Sample 3 along with the corresponding time-averaged wall temperature map for each heat flux. Data for base heat fluxes of (a,b) 89 W/cm², (c,d) 115 W/cm², (e,f) 148 W/cm² are shown.

7. CONCLUSIONS AND FUTURE WORK

The overarching goal of this dissertation was to investigate the performance of manifold microchannel (MMC) heat sinks during two-phase operation. This work includes a wide range of experiments that were conducted to characterize the thermal and hydraulic performance of MMCs which had not been reported in the literature. This section provides a summary of the conclusions from each of the studies and suggested future work pertaining to MMC heat sinks.

7.1 Conclusions

In Chapter 3, a novel hierarchical manifold microchannel heat sink array was designed and fabricated to dissipate heat over a 5 mm × 5 mm heated area. The heated area was cooled by a 3 × 3 array of heat sinks, which were fabricated directly in the heat-generating substrate and HFE-7100 is used as the working fluid. Steady-state, temporally-averaged data are presented for three channels with nominal widths of 15 μm and depths of 35, 150 and 300 μm.

- The channel with the shallowest channels provided the highest heat transfer coefficient, but the reduced heat transfer area leads to dryout at lower base heat fluxes compared to the deeper channels. Heat fluxes up to 142, 705, and 910 W/cm² were dissipated using 15 × 35 μm, 15 × 150 μm, and 15 × 300 μm channels, respectively.
- The single-phase heat transfer coefficient was found to increase with increasing channel mass flux, which was attributed to impingement and developing flow effects. In the two-phase regime, heat transfer coefficient strongly depends on exit quality and weakly depends on channel depth and mass flux. For all channel depths and mass fluxes, heat transfer coefficient increases with increasing exit quality until a maximum is reached; after this point, the heat transfer coefficient decreases with exit quality until critical heat flux is reached. These trends match the general trends experienced in traditional microchannel heat sinks.
- Effective thermal resistance was found to decrease with increasing channel depth and increasing mass flux. While the heat sink with the smallest channel depth provided the highest heat transfer coefficients, it also provided the highest thermal resistance due to the significantly reduced wetted area compared to the deeper channels. The decrease in

thermal resistance provided by increasing the mass flux was minimal compared to the significant increase in pressure drop for deep channels. The cooling approach provided a minimum effective heat sink thermal resistance of 5.6×10^{-6} m²K/W for the sample with channel depths of 300 μm at a mass flux of 2900 kg/m²s.

The work in Chapter 4 aims to build upon the results presented in Chapter 3 by investigating a broader set of channel geometries that includes channel width variations, as well as subjecting the heat sink to hotspot heat fluxes. The effect of channel dimensions and mass flux are studied for heat sinks with banks of small-diameter, high-aspect-ratio microchannels.

- Heat sinks with wider channels yield higher heat transfer coefficients, but not necessarily the lowest thermal resistance. For a fixed channel depth of ~300 μm, the sample with 15-μm wide channels has a wetted area ~86% larger than the sample with 33-μm wide channels; while the heat transfer coefficient is lower for the sample with thinner channels, the increased wetted area outweighs the decrease in heat transfer rate.
- For a fixed aspect ratio of ~10 and equal wetted area, the sample with a larger hydraulic diameter (33×300 μm channels) provided a higher heat transfer coefficient and lower thermal resistance compared to the sample with a smaller hydraulic diameter (Sample 15×150 μm channels), which is attributed to the increase in fluid flow rate. This work shows that, unlike traditional heat sinks, maximum heat flux dissipation does not necessarily increase with increasing wetted area for two-phase manifold microchannel heat sinks.
- Hotspot heat fluxes up to 2,700 W/cm² are superimposed over background heat fluxes up to 900 W/cm² result in local temperature rises of ~16 °C near the hotspot. The heat sink heat transfer coefficient does not change significantly during hotspot heating, resulting in a linear local surface temperature rise with increasing hotspot heat flux.

In Chapter 5, a compact, monolithic hierarchical manifold was designed and used to feed a highly discretized heat sink array for intrachip cooling. The same 5 mm × 5 mm heated area was discretized into a 9×9 array of heat sinks, compared to the heat sinks with a 3×3 array of heat sinks presented in Chapters 3 and 4.

- A multi-layer hierarchical manifold is fabricated in silicon and thermocompression bonded together to create a compact manifold, which distributes the single fluid inlet into 82 inlets to the 9 × 9 array of heat sinks and also recollects the 164 outlets and merges them into a single fluid outlet. Due to its small overall size (~20 × 20 × 3 mm^3) and small feature sizes necessary to achieve the necessary discretization,
- The thermal performance of the 3 × 3 array and 9 × 9 array are extremely similar for a given mass flow rate. The decrease in flow length does not result in a decrease in overall system pressure drop due to the increased manifold pressure drop. The pressure drop in the manifold for the 9×9 array is relatively large due to the small feature sizes necessary to achieve the necessary discretization and the compact design of the manifold. With additional manifold design modifications in the manifold for the 9×9 array could lead to pressure drops lower than that for the 3×3 array due to the decreased channel flow length.
- The temperatures across the chip surface remain relatively constant over the range of heat fluxes tested, signifying even flow distribution to each of the heat sinks.

In Chapter 6, a single manifold microchannel, representative of a repeating unit in a heat sink, is fabricated in silicon with a bonded glass viewing window. A high-speed camera is used to visualize the two-phase flow in the channel through the glass sidewall; an infrared camera measures the temperature distribution on the opposite silicon channel sidewall.

- For the deepest channels, stagnant vapor becomes intermittently trapped at the bottom portion of the channel, thereby limiting the amount of local heat transfer and increasing the wall temperature near the channel base. At high heat fluxes, the vapor blanket in some regions is not able to be temporarily disrupted by liquid that impinges on the channel base, leading to a high local wall temperature in these regions.
- The consequence for having extremely deep channels with short flow lengths is demonstrated when comparing the two samples with equal flow lengths (750 μm) and channel depths of 250 μm and 1000 μm. While the deeper channel has ~4 times the surface area of the shallower channel, the base temperatures are lower for the shallower channel for a given base heat flux. The vapor blanketing the bottom of the channel insulates this region; while the upper region of the channel still has the high heat

transfer coefficients, the temperature drop along the fin height leads to relatively high base temperatures to maintain the necessary wall superheat in the upper region.

7.2 Suggested Future Work

Plans for future studies are proposed in this section. These studies are designed to provide a more thorough understanding of the fundamental heat transfer mechanisms in manifold microchannels during two-phase operation. All of the proposed studies focus on fundamental, single-channel experiments rather than system-level heat sinks.

1. The mechanisms leading to critical heat flux in manifold microchannels have not been studied. The current single-channel experimental facility (Chapter 6) was limited by the maximum temperature at the ceramic heater and surrounding materials. Due to this restriction, the maximum heat flux input was approximately 200 W/cm², which is much lower than the critical heat flux for the small-diameter channels of interest (Chapter 3, 4, 5). By redesigning the experiment for high-heat-flux operation, the flow morphology could be studied at high heat fluxes and high vapor qualities.

2. The results from Chapters 3, 4, and 5 show that thermal performance of MMC heat sinks is closely tied to the channel width, depth, and length during two-phase operation. The work presented in Chapter 6 provided the design for a novel single-channel experimental test device and demonstrated its function for a small range of operating parameters and channel geometries. A more complete test matrix that isolates the effects of channel width, aspect ratio, and nondimensional channel length would provide valuable insights into the operation of manifold microchannels. The output of this study should not only be qualitative trends, but also predictive models, which are not currently available for two-phase manifold microchannels.

3. While flow visualization provided valuable information concerning the flow morphology in manifold microchannels, there is still critical information that has not been gathered. The film thickness and fluid velocities, which are both critical to the heat transfer performance, were not able to be measured in the present study. Measurement techniques such as particle

image velocimetry can be used to determine the liquid velocity in bubbly two-phase flows. Local film thickness can be measured using a laser focus displacement meter or an interferometer.

4. The flow morphology for high-aspect-ratio manifold microchannels was shown to be time periodic in Chapter 6. Vapor blankets the bottom of the channel and is intermittently broken by impinging fluid. Temporally resolved spatial temperature maps synced to the high-speed videos would provide critical information about the local heat transfer coefficients at the channel wall. In Section 6.3.2, the relevant time scale for changes in flow morphology was shown to be approximately 0.5 ms; the current state-of-the-art in IR imaging allows for measurement at frequencies as high as 4 kHz ($1/f$ = 0.25 ms) at a resolution of 54 × 43. The experiment presented in Chapter 6 measured the temperature at the fin wall. To limit spreading and signal delay, the temperature should be measured at the channel wall surface. Undoped silicon has a high transmissivity in the IR wavelengths so an IR-opaque surface should be deposited on the channel wall to measure the local temperature directly at the fluid interface. These wall temperatures can be used to directly calculate the local heat transfer coefficients.

5. One of the major barriers to implementation of manifold microchannel heat sinks is flow maldistribution across the chip area. Problems with flow maldistribution can become exacerbated with two-phase flow instabilities, which can lead to extreme flow rate and temperature fluctuations. Due to the numerous parallel flow paths in MMCs, flow instabilities are a major concern. Flow instabilities can be suppressed, for the most part, by adding an artificial upstream pressure drop, which changes the overall channel load curve. However, this added pressure drop increases the pumping power for a given heat flux and temperature. An investigation into methods of suppressing flow instabilities in manifold microchannel heat sinks is needed prior to implementation.

6. Compared to experiments, computational fluid dynamics can provide a more cost-effective method to predict the performance of numerous channel geometries. Accurate modeling of the two-phase flows having simple flow structures in straight channels, using level-set and

volume of fluid methods, have been presented in the literature and verified against experiments. These methods can be extended to manifold microchannels and verified against the experiments already conducted. Once verified, the methods can be used to determine optimal channel and flow parameters in MMCs.

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APPENDIX A. LIST OF EXPERIMENTAL EQUIPMENT

This section contains a list of equipment used in the experimental facilities constructed to conduct the work outlined in this document.

Table A.1. Equipment used in the two-phase manifold microchannel heat sink facility.

Part Name	Vendor/ Manufacturer	Part Number	Description
12V power supply	TDK-Lambda Americas, Inc.	LS50-12	Modular 12V power supply for sensors
Data acquisition	National Instruments	cDAQ-9178	Data acquisition chassis (accepts DAQ cards)
DAQ electrical voltage card	National Instruments	NI 9205	DAQ card used to acquire voltage signals
DAQ electrical current card	National Instruments	NI 9208	DAQ card used to acquire current signals
DAQ thermocouple card	National Instruments	NI 9213	DAQ card used to acquire thermocouple signals
DAQ RTD card	National Instruments	NI 9217	DAQ card used to power and measure RTDs

Table A.1. Continued.

Part Name	Vendor/ Manufacturer	Part Number	Description
Mass flow meter	Micromotion	CMF010M	Coriolis mass flow meter
Thermocouples	Omega	TMTSS-062U-6	T-Type thermocouples for fluid inlet and outlet pressures
RTD	Omega	P-M-1/10-1/4-6-0-P-3	Reference temperature sensor for chip temperature sensors
Gage pressure transducer	WIKA	S-10	Sensor used to measure pressure at test section outlet
Differential pressure transducer	Omega	PX2300-10BDI	Sensor used to measure pressure drop across test section
Particulate filter (2 μm)	Swagelok	SS-4TF-2	In-line filter used to remove fine particles from fluid stream
Carbon filter	Pall	12011	Activated charcoal filter for removing organic materials from working fluid

Table A.1. Continued.

Part Name	Vendor/ Manufacturer	Part Number	Description
Condensers	Ace Glass	5977-14	Graham condensers used to condense vapor during degassing
Liquid-liquid heat exchanger	Lytron	LL520G12	Heat exchanger located at the outlet of the test section for condensing and cooling working fluid
Chiller	Coherent	T255P	Chiller for liquid-liquid heat exchanger and reflux condensers
150V Programmable Power Supply	Sorensen	XG 150-5.6	Power supply for test chip heaters
100V Programmable Power Supply	Sorensen	XG 100-8.5	Power supply for immersion heaters used for degassing
Infrared camera	FLIR	SC7500	IR camera used for wall temperature measurement in single-channel experiment

Table A.1. Continued.

Part Name	Vendor/ Manufacturer	Part Number	Description
Infrared lens	Janos	Asio 4×	Magnifying lens for IR camera
High-speed camera	Phantom	v1212	High-speed camera for flow visualization in single-channel experiment
Optical lens	Keyence	VH-Z100R	100-1000× magnification lens for flow visualization

APPENDIX B. TECHNICAL DRAWINGS OF FABRICATED COMPONENTS

This section details the fabrication of the hierarchical MMC heat sink test vehicles used in Chapter 3 and Chapter 4 of the present work, which is shown in Figure B.1, and the test chips that contain the 9 × 9 array of heat sinks. The test vehicles consist of: (1) a manifold base, (2) hierarchical manifold, (3) test chip, (4) printed circuit board, and (5) insulation block. Table B.1 lists and describes the individual components. The technical drawings of the components are also provided in this section.

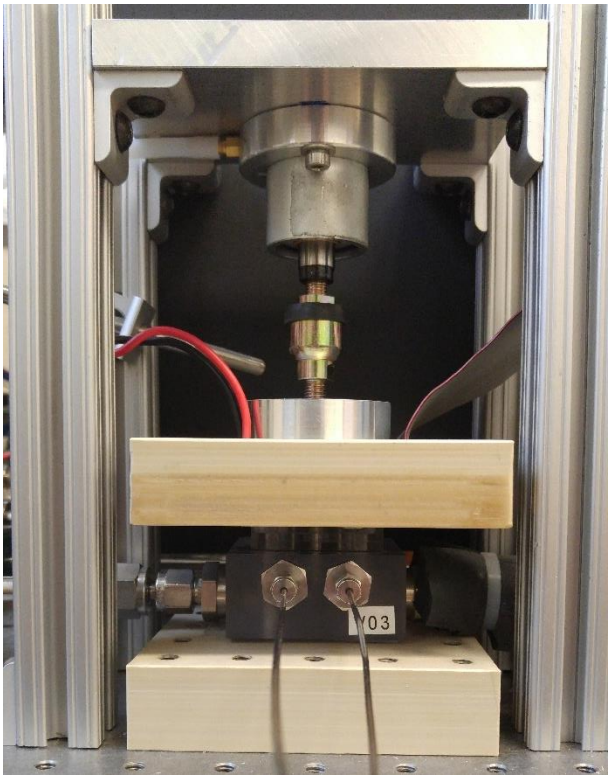

Figure B.1. Photograph of the test vehicle installed in the flow loop.

Table B.1. Custom-fabricated equipment used in the 3 × 3 two-phase manifold microchannel heat sink test vehicle.

Component	Drawing	Description
Manifold base (3 × 3)	Figure B.2 Figure B.3	Machined acrylic base for routing fluid from flow loop to 3 × 3 manifold microchannel heat sink
Manifold base (9 × 9)	Figure B.19 Figure B.20 Figure B.21 Figure B.22	Machined acrylic base for routing fluid from flow loop to 9 × 9 manifold microchannel heat sink
Hierarchical manifold plates (3 × 3)	Figure B.6	Four layers of laser-cut, 3-mm acrylic sheets for fluid routing
Manifold plates (9 × 9)	Figure B.11 Figure B.12 Figure B.13 Figure B.14 Figure B.15 Figure B.16	CAD drawings of the photomasks used to pattern the eight levels of the hierarchical manifold to feed the heat sink with a 9 × 9 array of heat sinks.
Microchannels (3 × 3)	Figure B.4	Mask design for the microchannel patterning and etching (3 × 3)
Microchannels (9 × 9)	Figure B.10	Mask design for the microchannel patterning and etching (9 × 9)
Heaters and temperature sensors (background-only)	Figure B.5	Mask design for the heater and temperature sensor patterning
Heaters and temperature sensors (background + hotspot)	Figure B.8	Mask design for the heater and temperature sensor patterning

Table B.1. Continued.

Component	Drawing	Description
Printed circuit board (background-only)	Figure B.9	Printed circuit board for convenient electrical interface between test chip and data acquisition (for use with background-only heater design)
Plenum plate	Figure B.7	Plenum interface plate for the 3 × 3 array of heat sinks
Assembly fixture for 9 × 9 manifold	Figure B.17 Figure B.18	Machined Macor assembly fixture used for die-level bonding of the multi-level manifold
Insulation block (9 × 9)	Figure B.23	Machined PEEK insulation block to limit heat losses to the environment during experimental testing

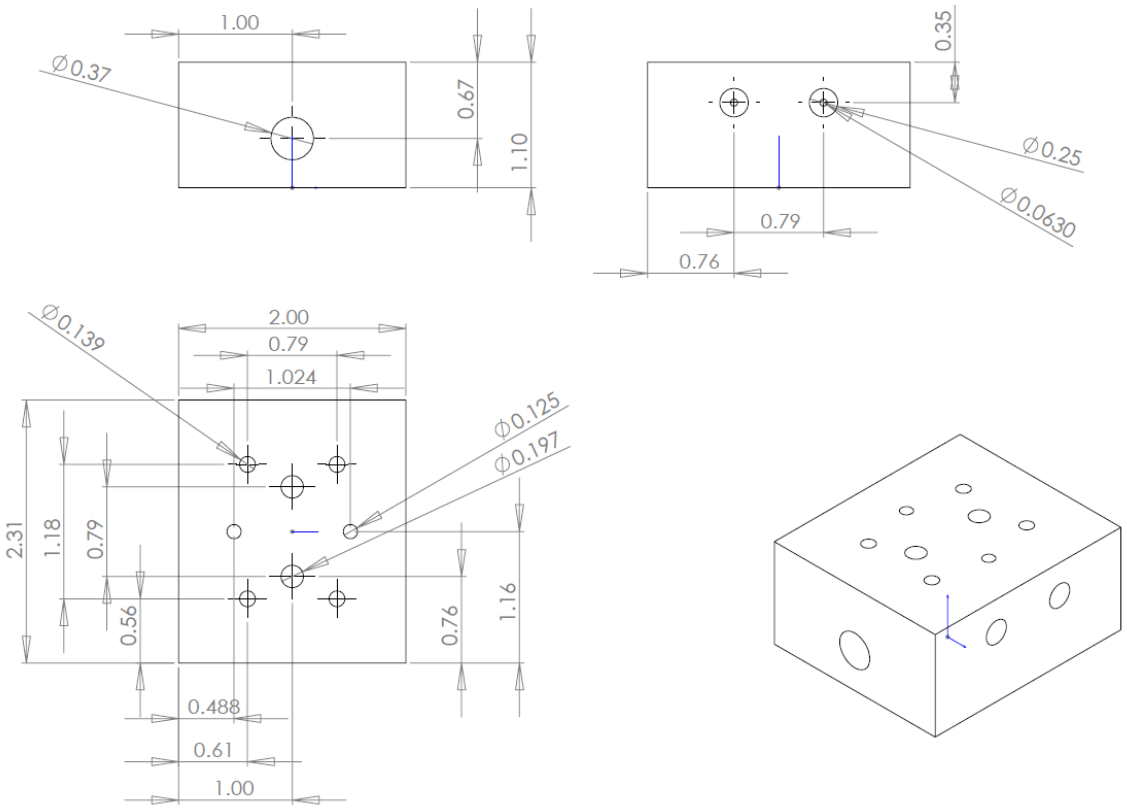

Figure B.2. Technical drawings of the manifold base; all dimensions in inches unless otherwise specified.

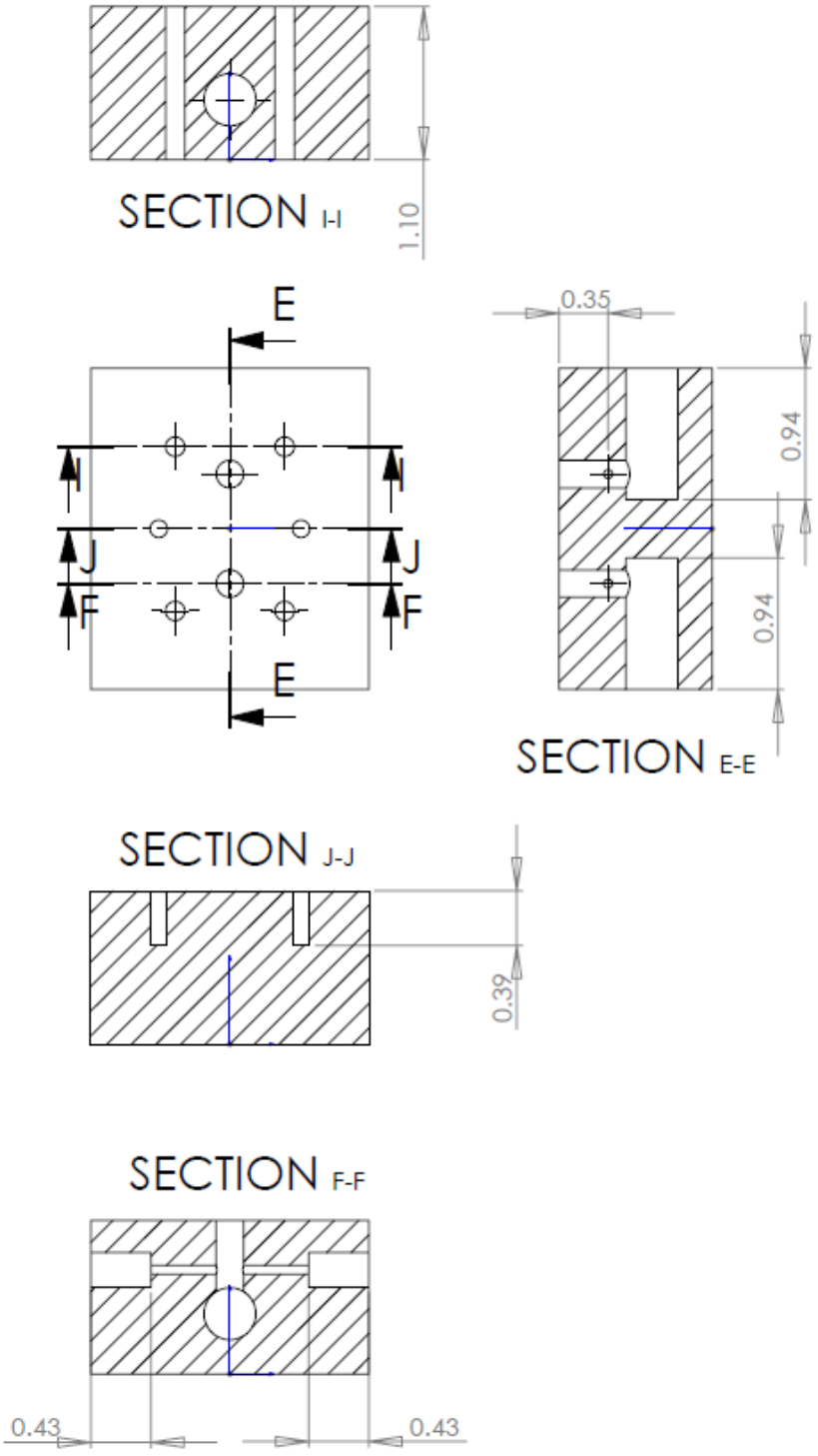

Figure B.3. Technical drawings of the manifold base; all dimensions in inches unless otherwise specified.

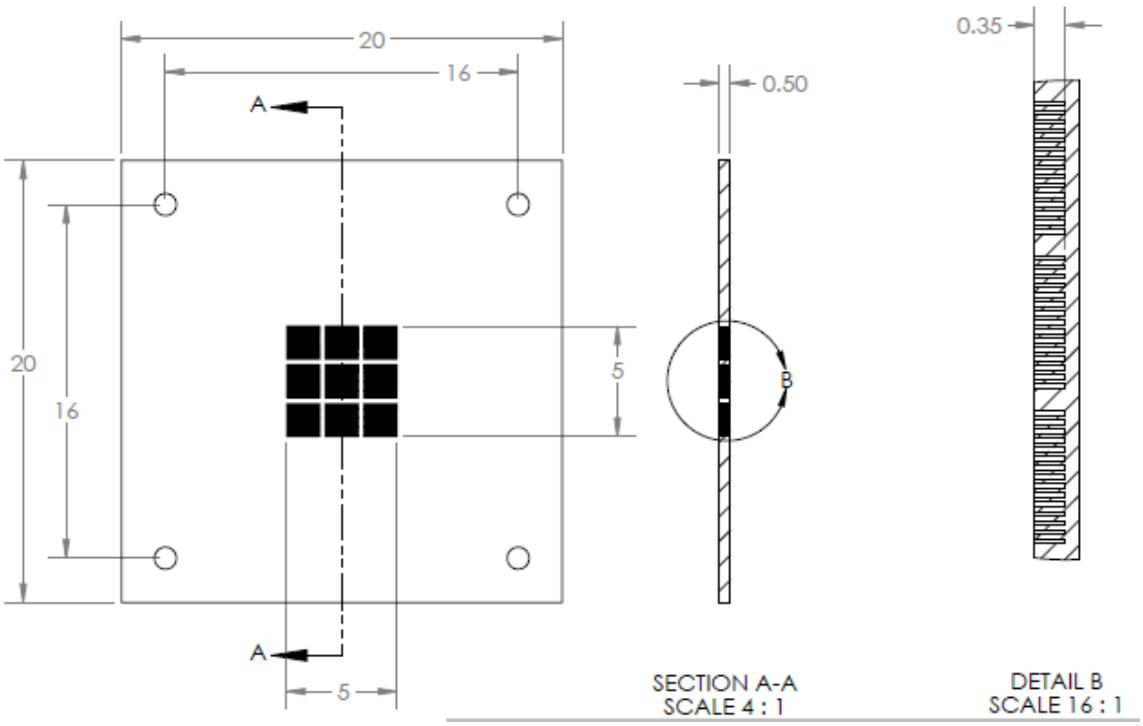

Figure B.4. Technical drawing for a 3 × 3 microchannel plate. Note that the channel dimensions change depending on the sample.

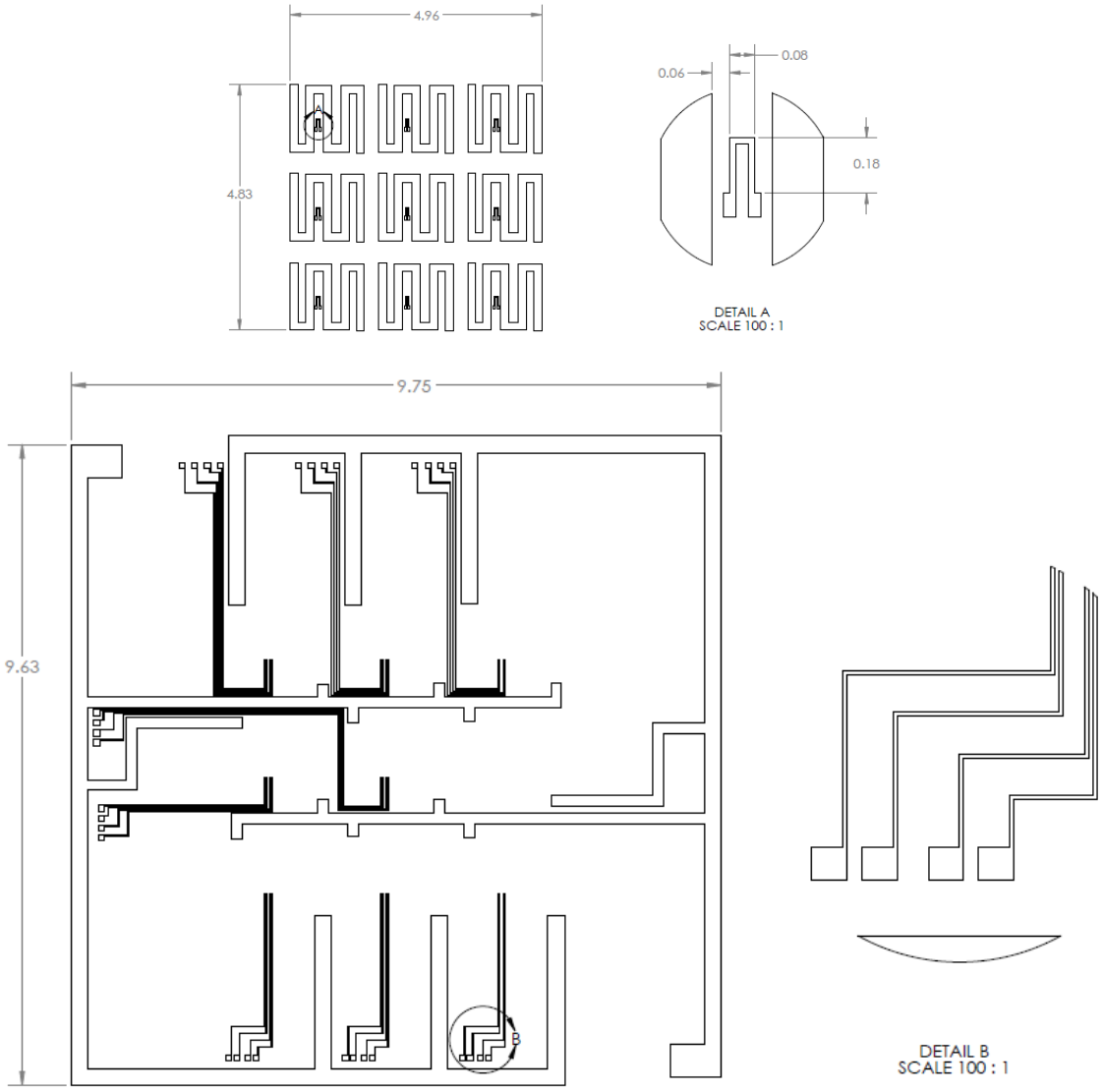

Figure B.5. Mask design for the Pt heaters and temperature sensors and Au traces.

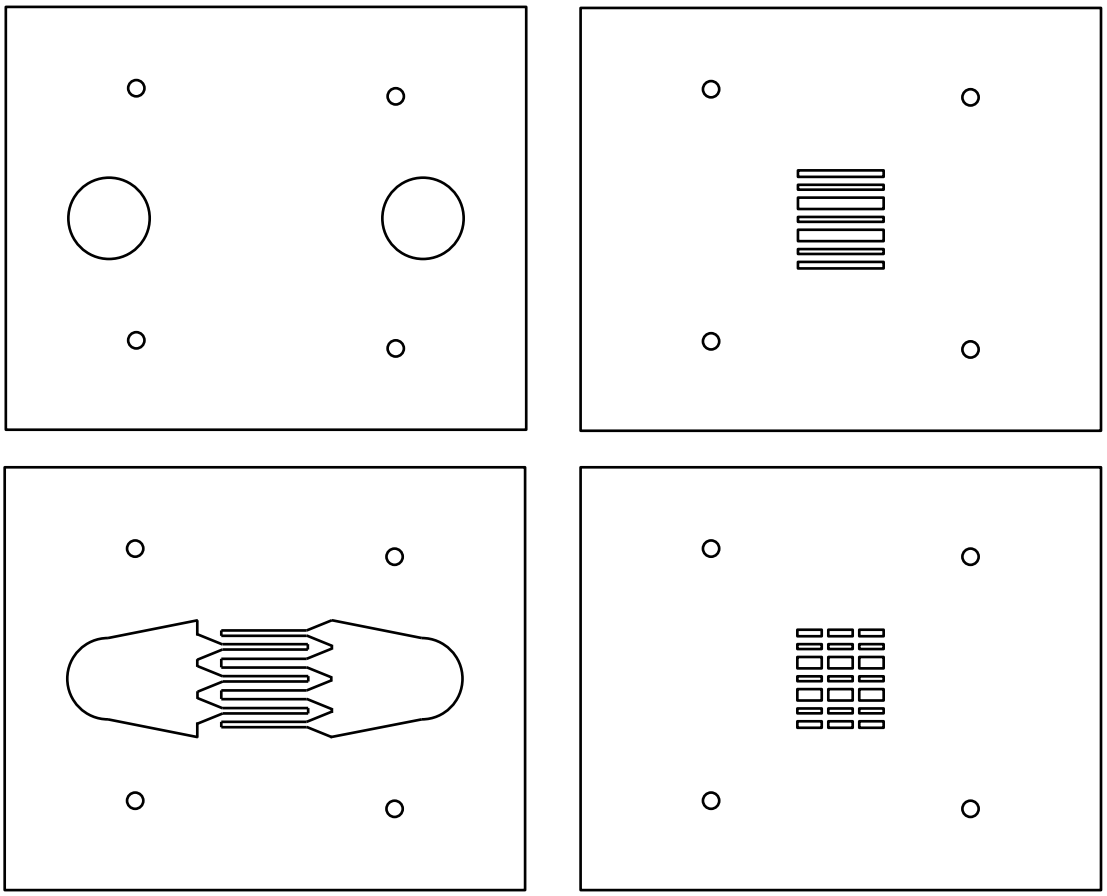

Figure B.6. Technical drawings of the manifold; all dimensions in inches unless otherwise specified.

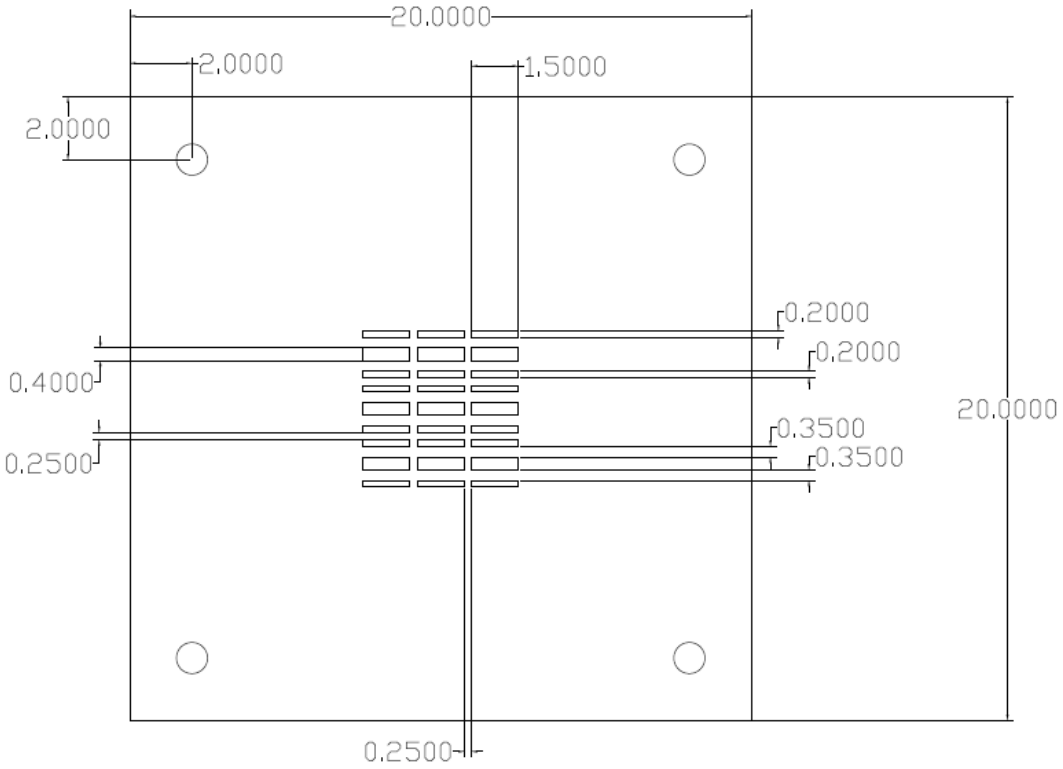

Figure B.7. Technical drawing of the plenum plate mask for a single die. All dimensions in millimeters.

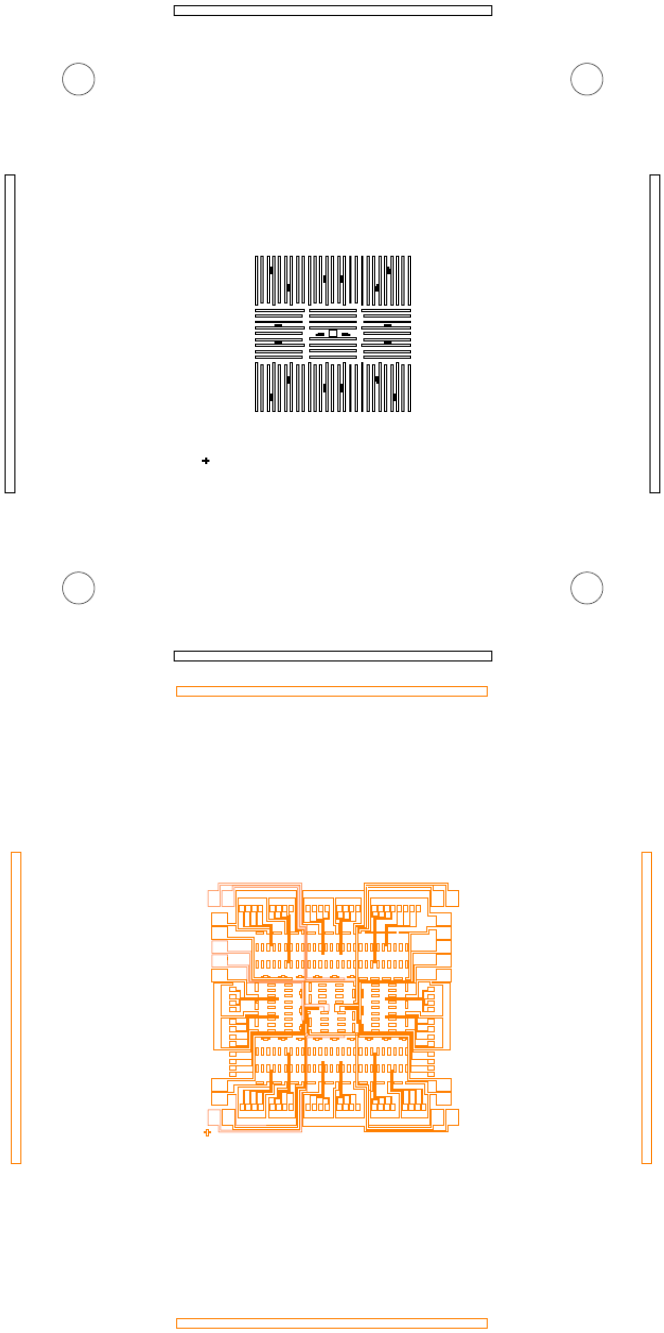

Figure B.8. Mask design for the heater deign containing the hotspot heater. (a) Pt heaters and RTDs and (b) Au traces.

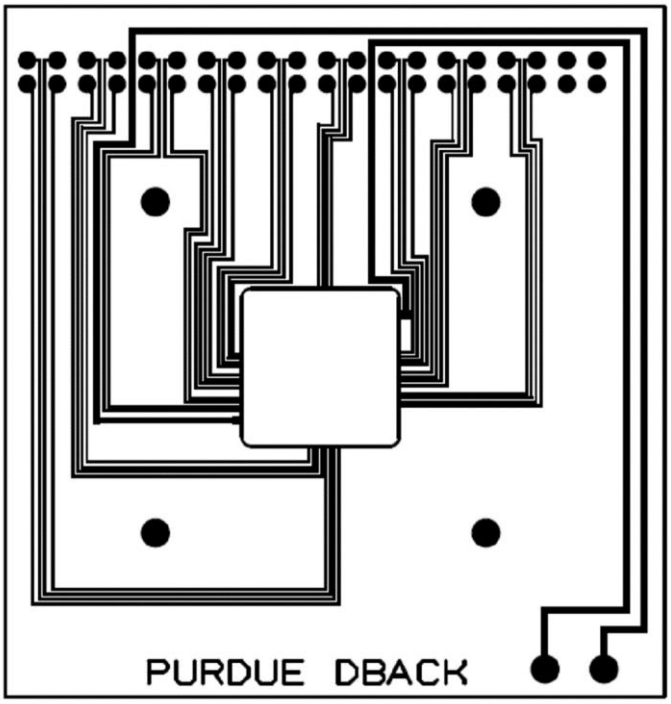

Figure B.9. Mask design of the printed circuit board used for the background-only heater design.

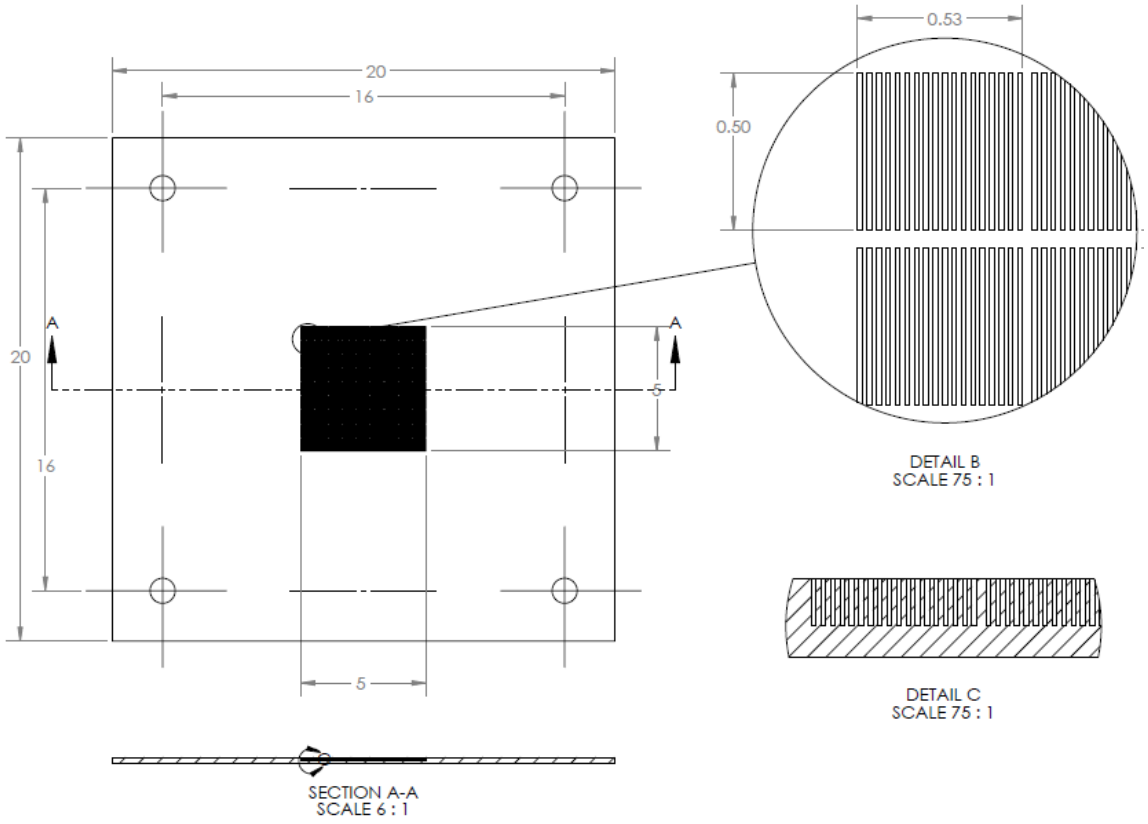

Figure B.10. Technical drawing for the 9 × 9 array of microchannel heat sinks. All dimensions in millimeters.

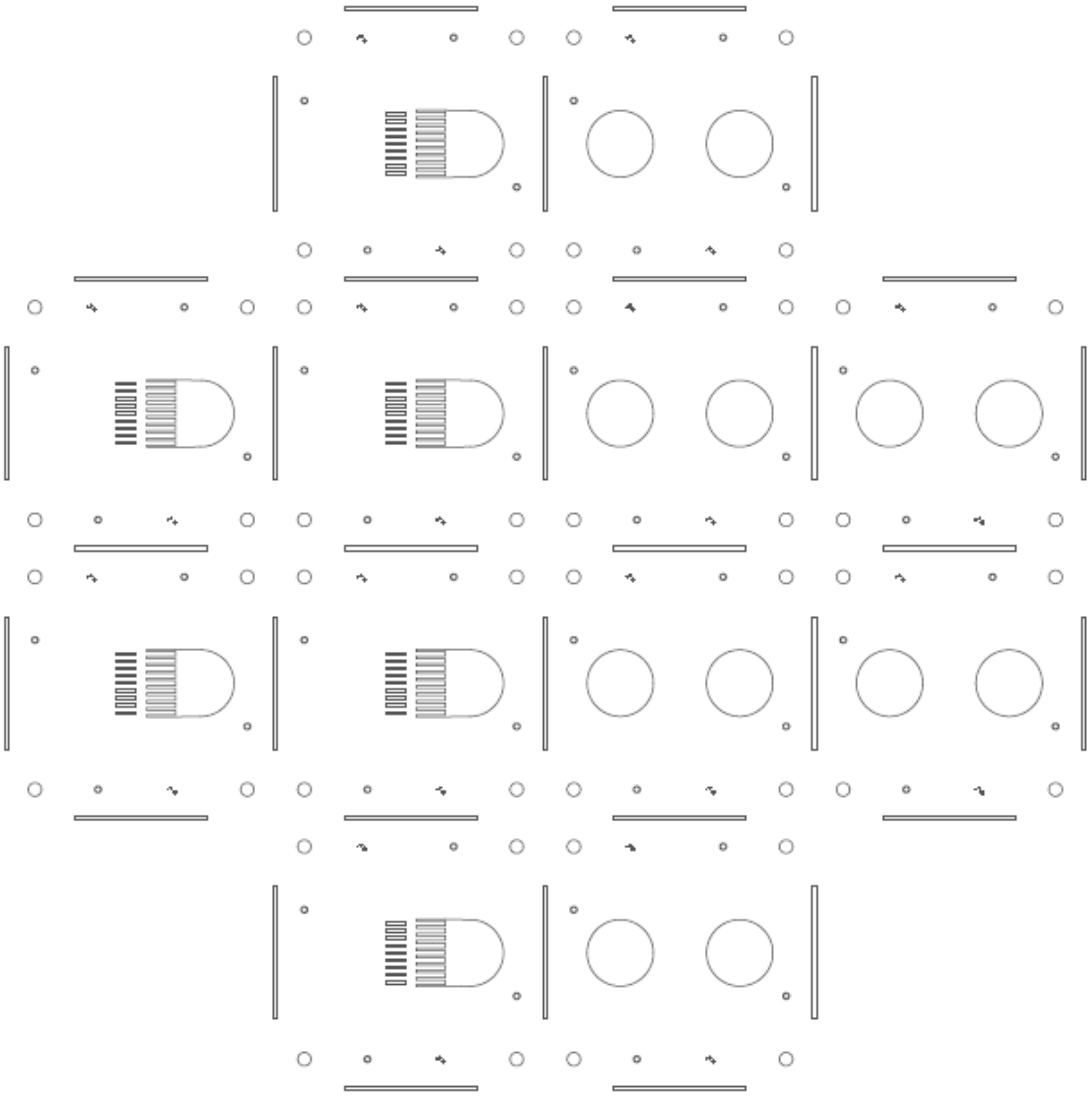

Figure B.11. Mask layout for 4-inch wafer for compact manifold used to feed 9 × 9 array of heat sinks.

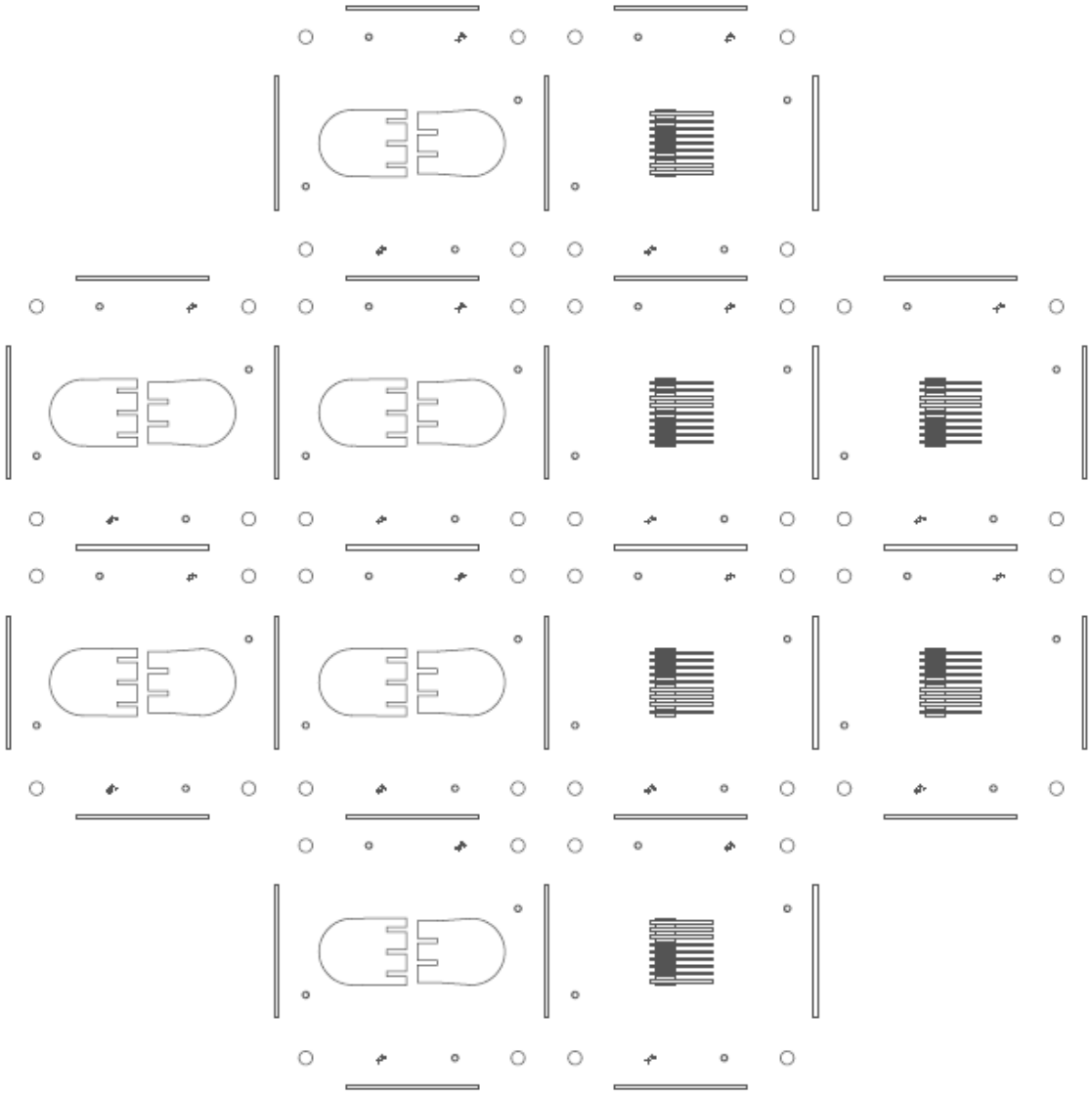

Figure B.12. Mask layout for 4-inch wafer for compact manifold used to feed 9 × 9 array of heat sinks.

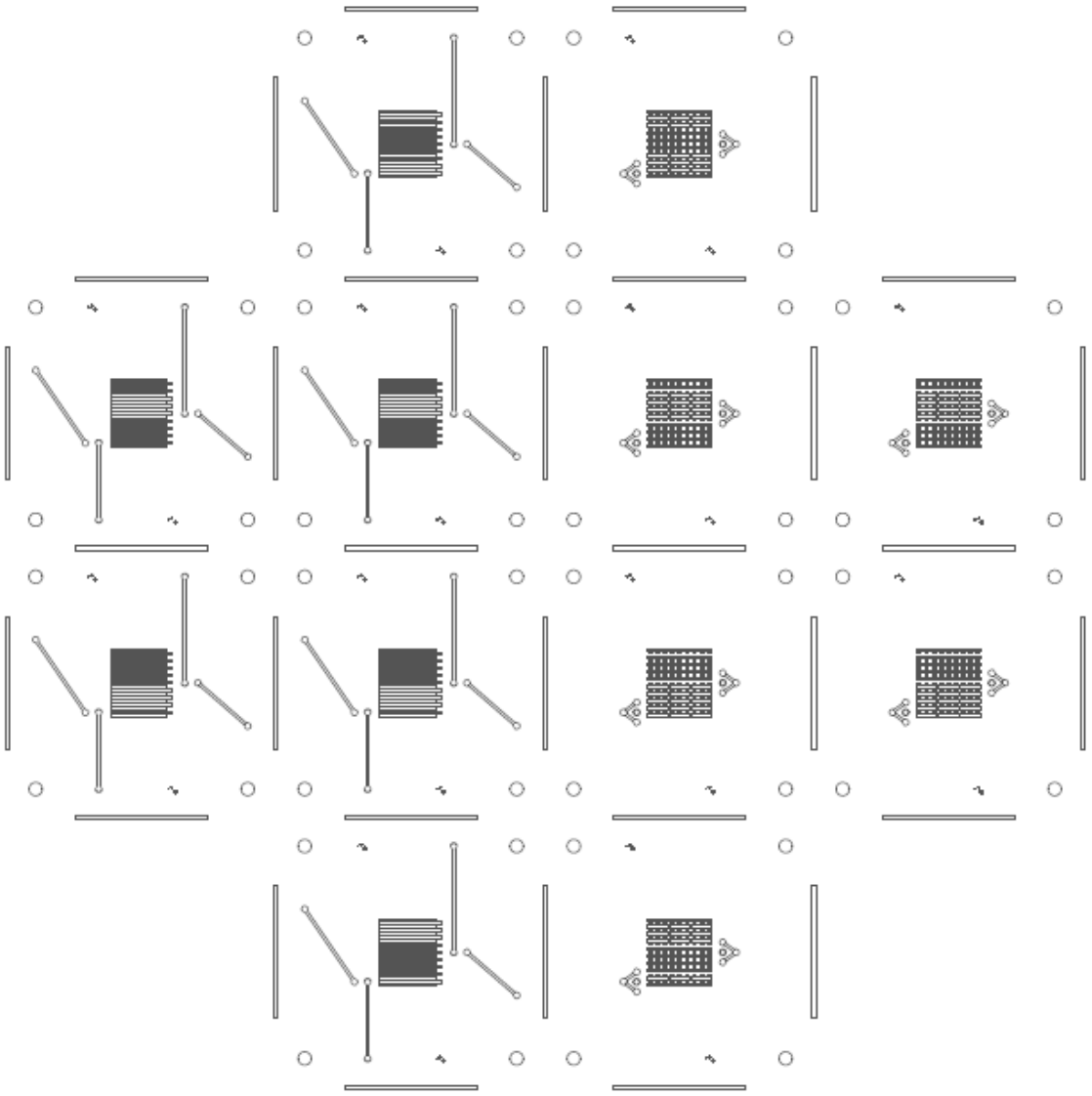

Figure B.13. Mask layout for 4-inch wafer for compact manifold used to feed 9 × 9 array of heat sinks.

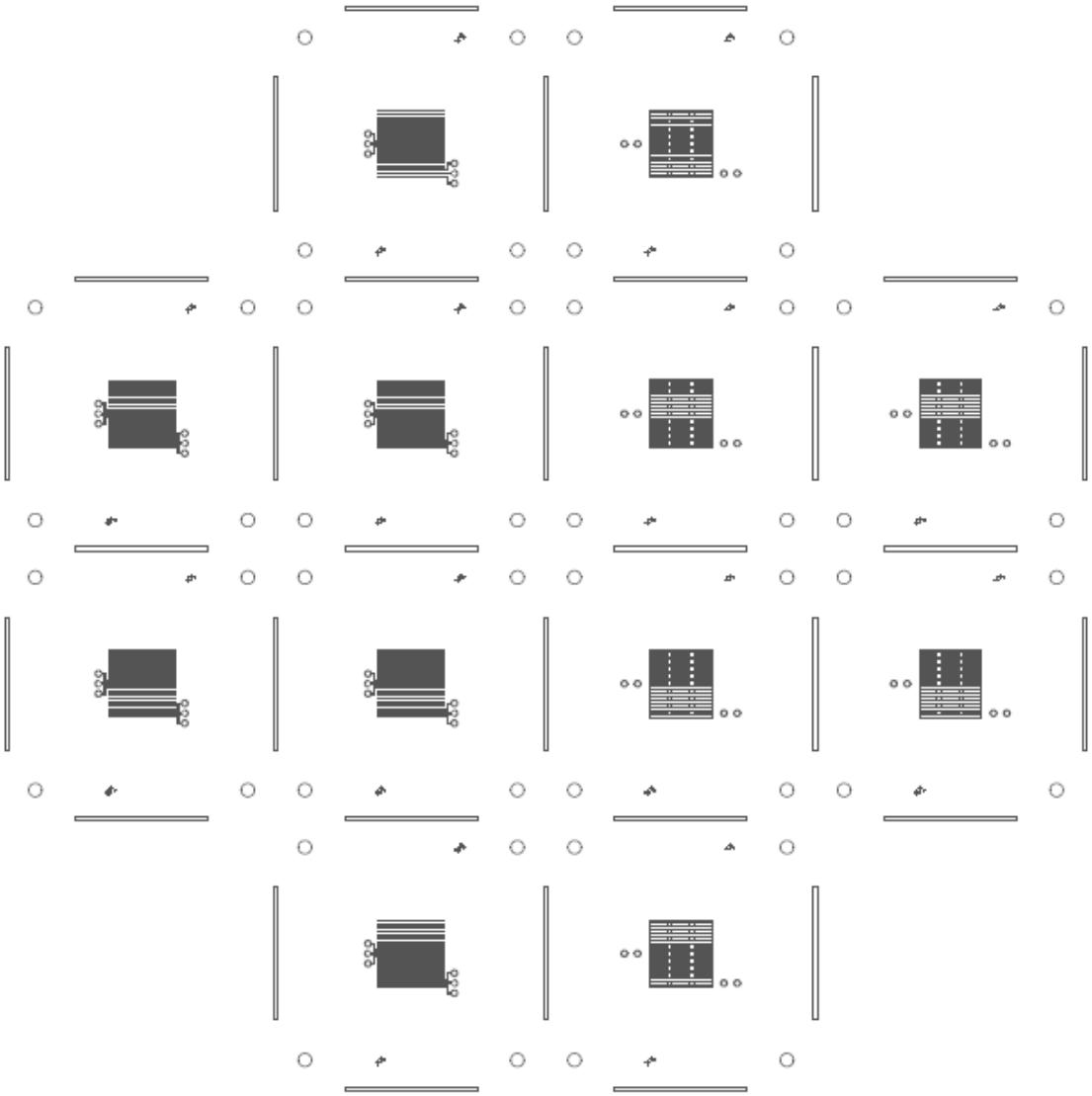

Figure B.14. Mask layout for 4-inch wafer for compact manifold used to feed 9 × 9 array of heat sinks.

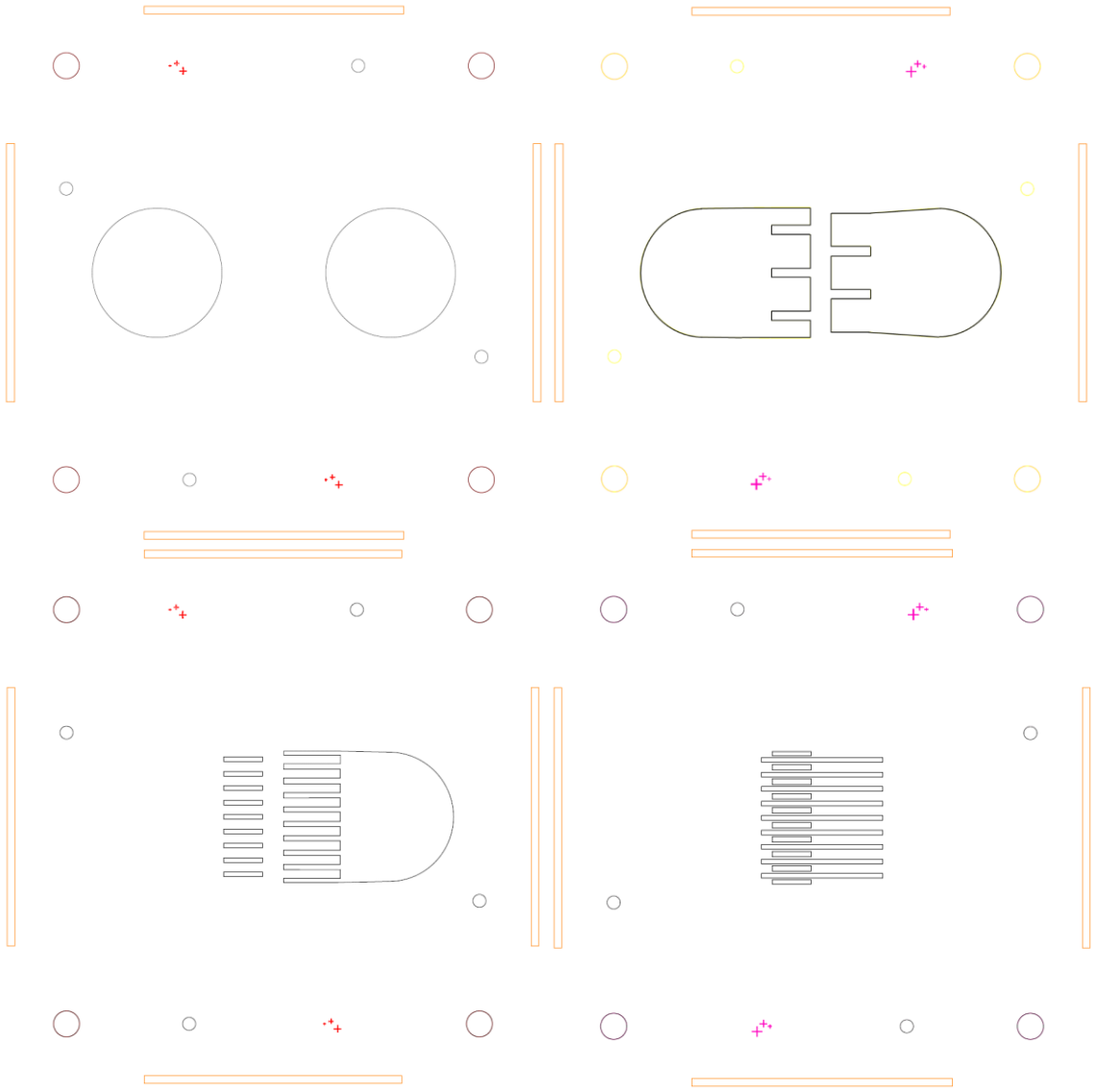

Figure B.15. CAD drawings of the photomasks for levels 1-4 of the hierarchical manifold.

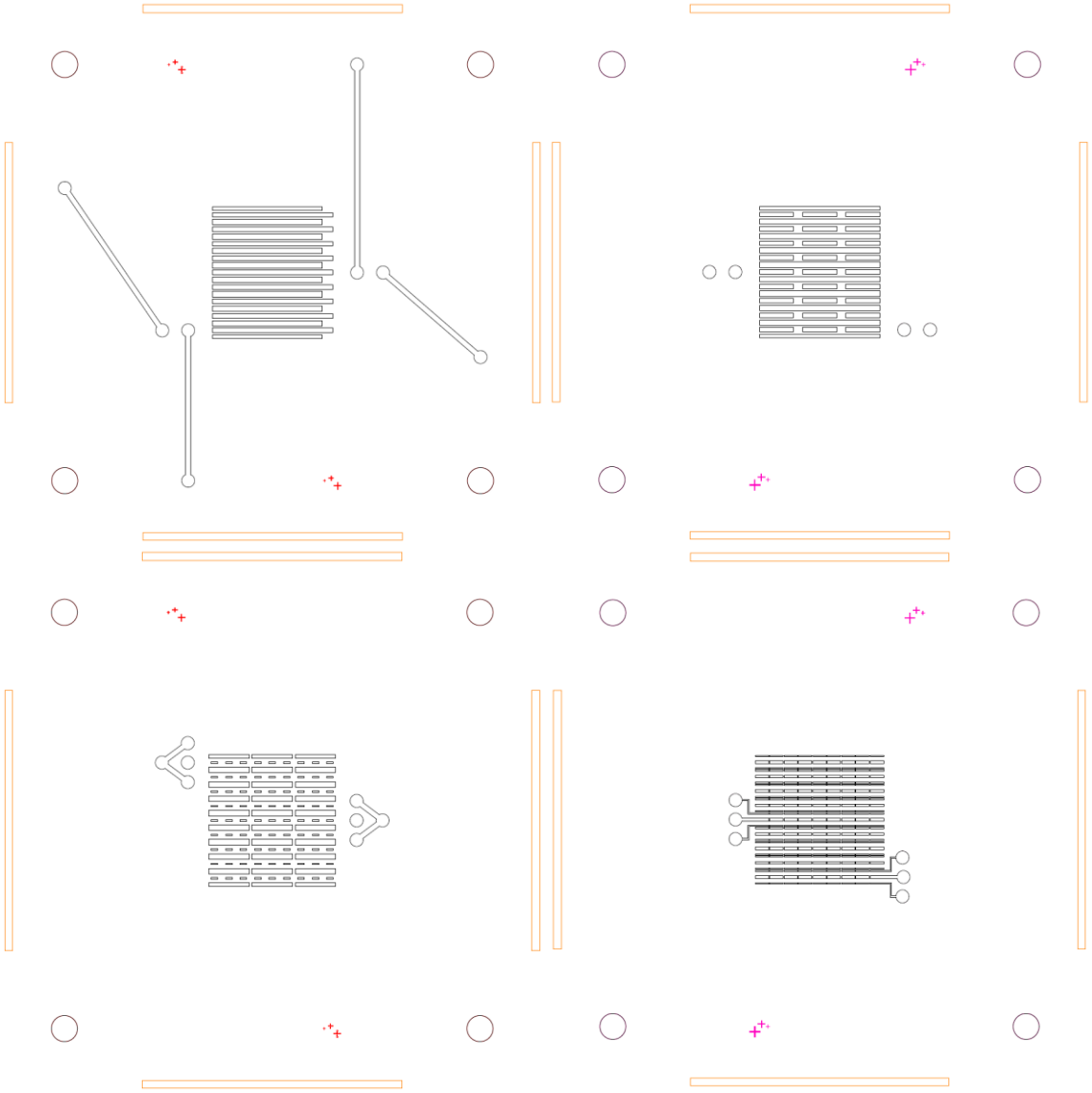

Figure B.16. CAD drawings of the photomasks for levels 5-8 of the hierarchical manifold.

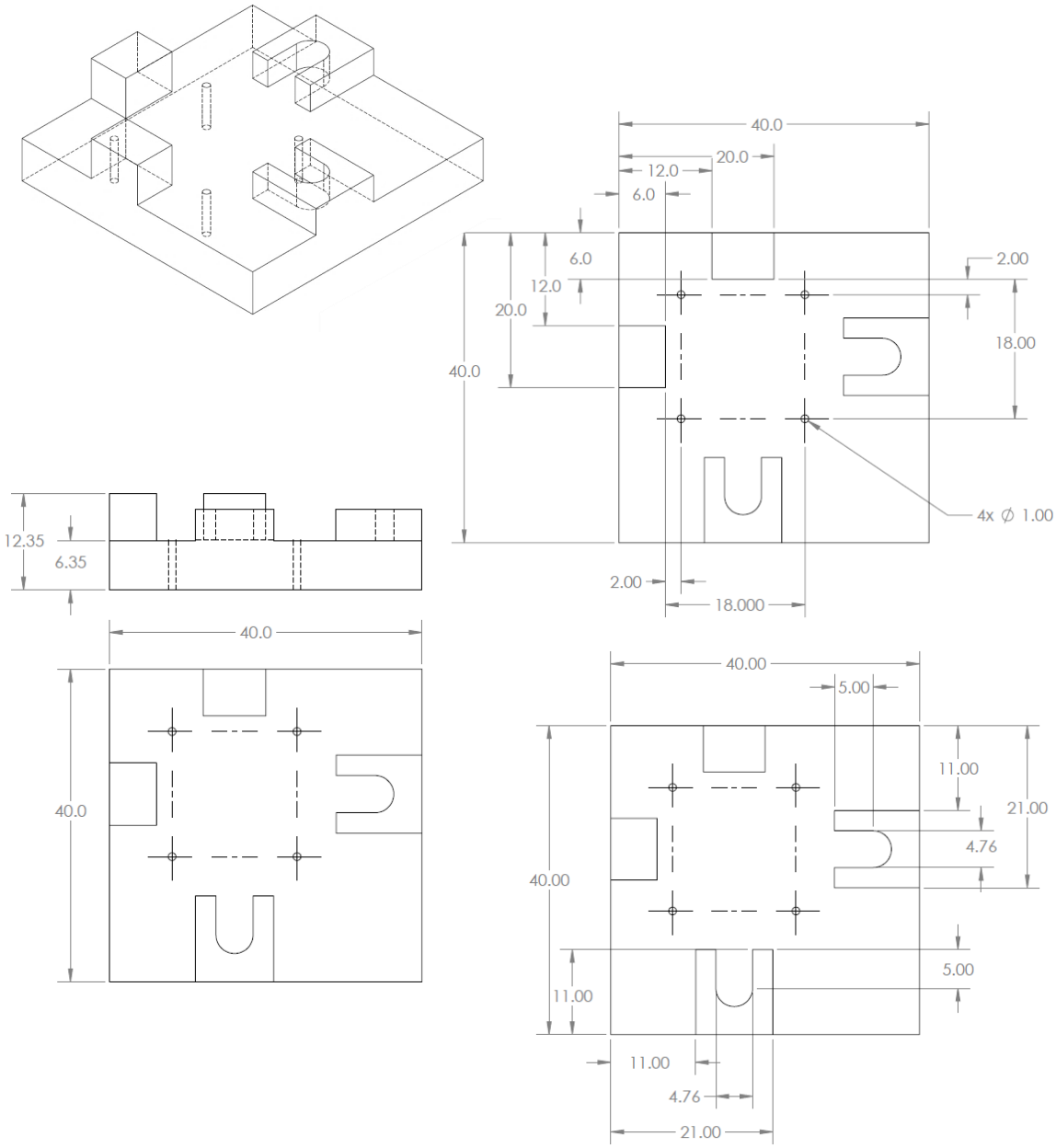

Figure B.17. Technical drawings of the manifold assembly fixture; all dimensions in millimeters unless otherwise specified.

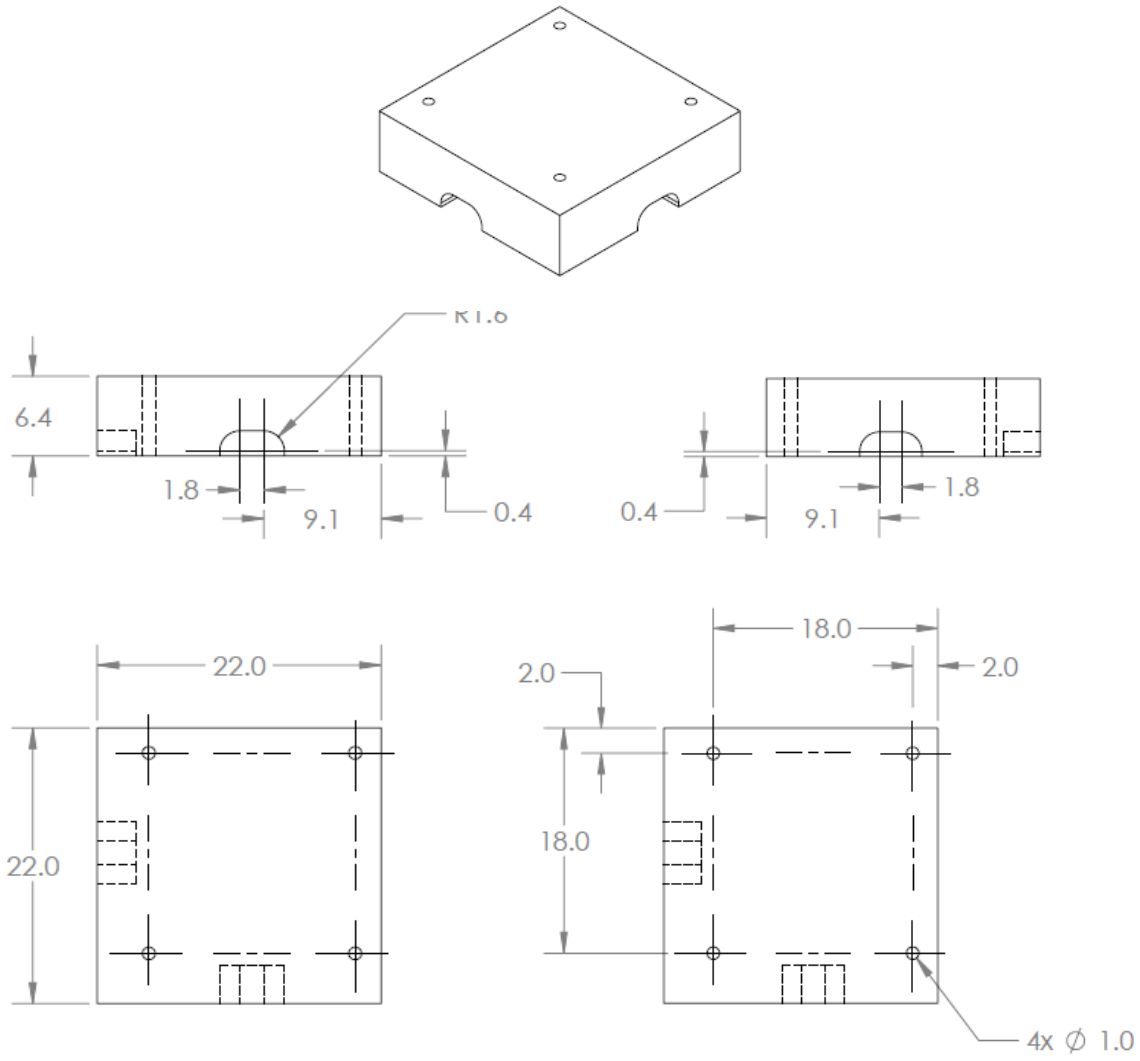

Figure B.18. Technical drawings of the manifold assembly fixture (bottom); all dimensions in millimeters unless otherwise specified.

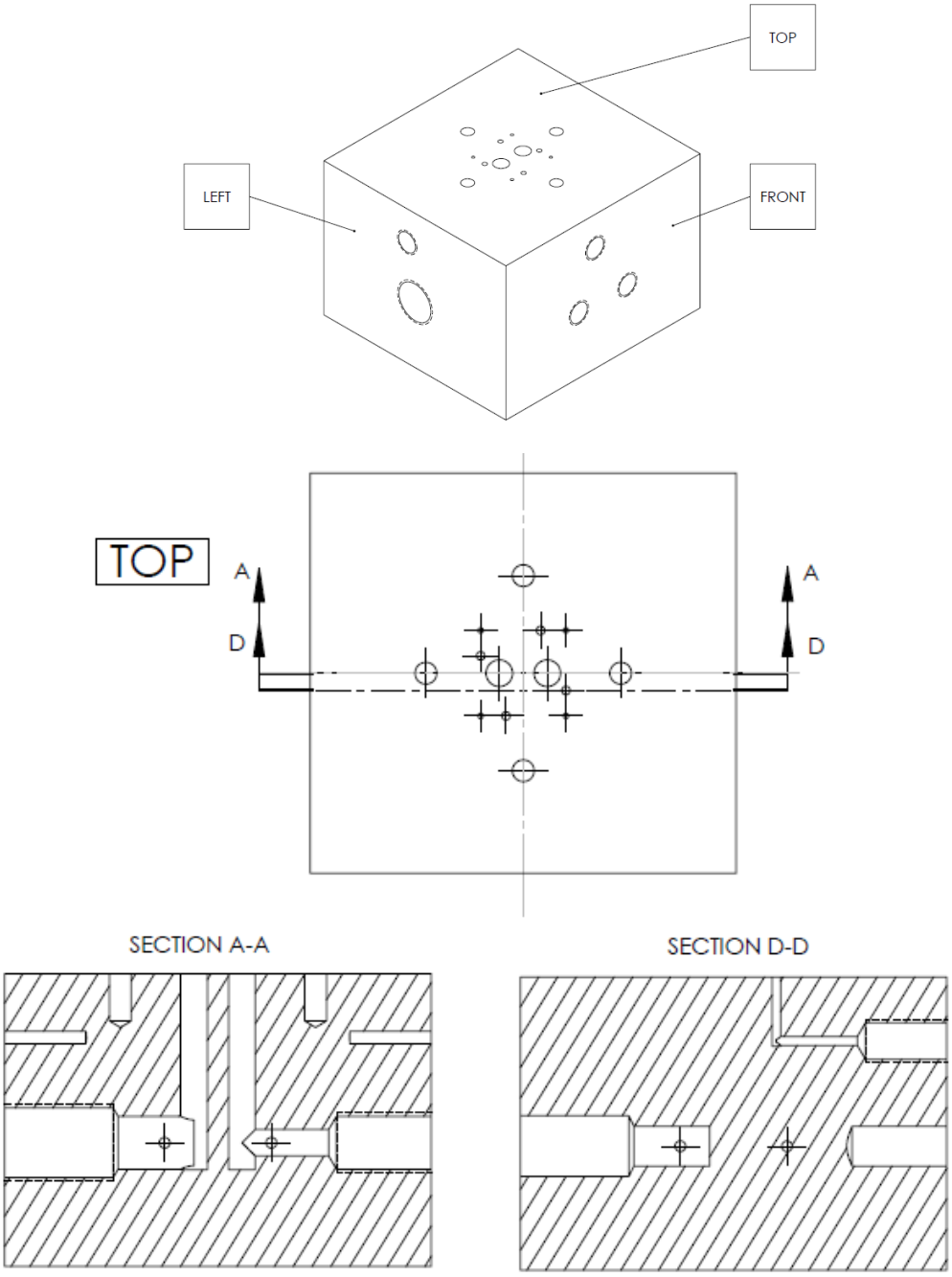

Figure B.19. Technical drawings of the manifold base for the test vehicle with a 9 × 9 array of heat sinks; all dimensions in inches unless otherwise specified.

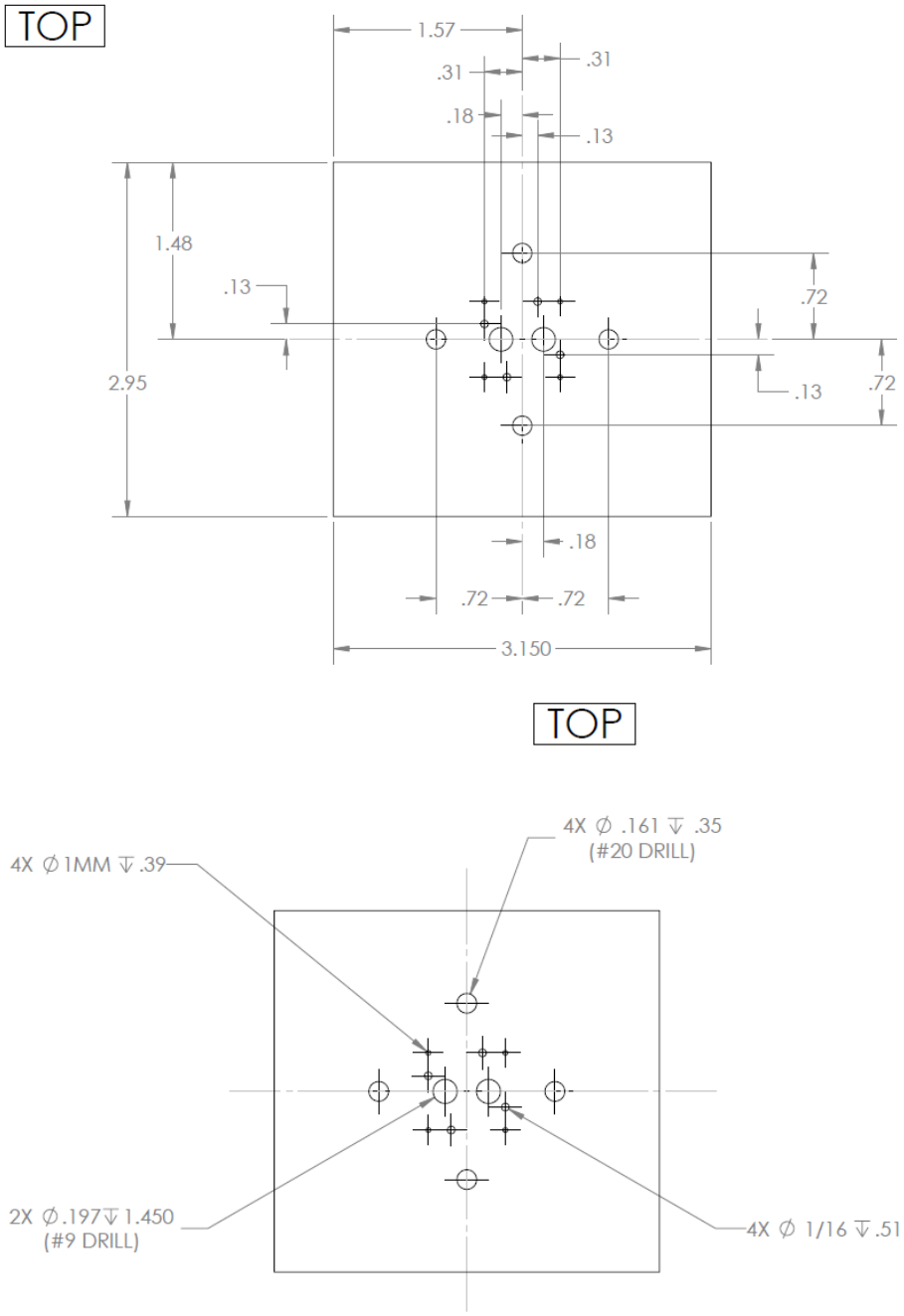

Figure B.20. Technical drawings of the manifold base for the 9 × 9 test vehicle; all dimensions in inches unless otherwise specified.

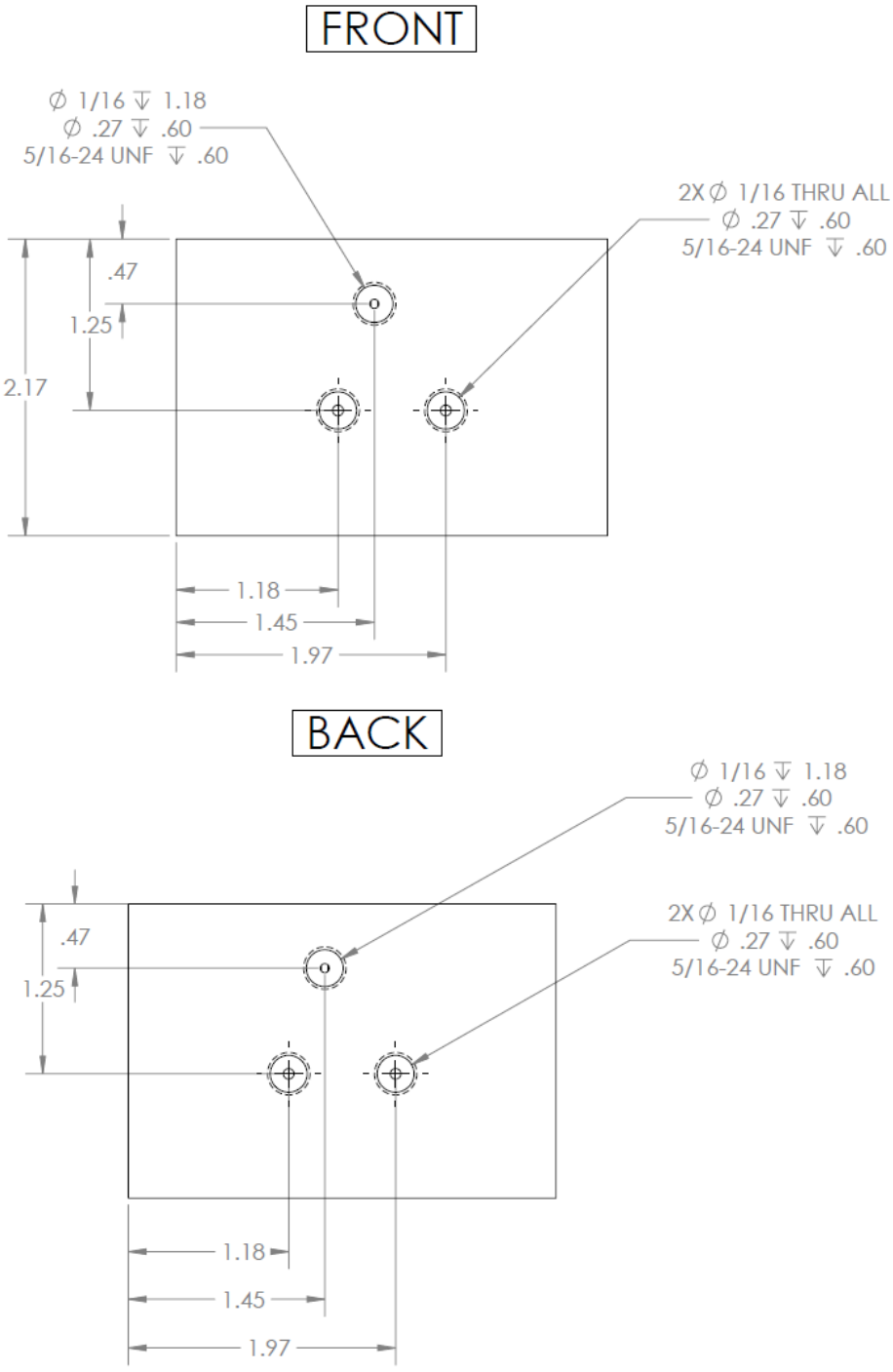

Figure B.21. Technical drawings of the manifold base for the 9 × 9 test vehicle; all dimensions in inches unless otherwise specified.

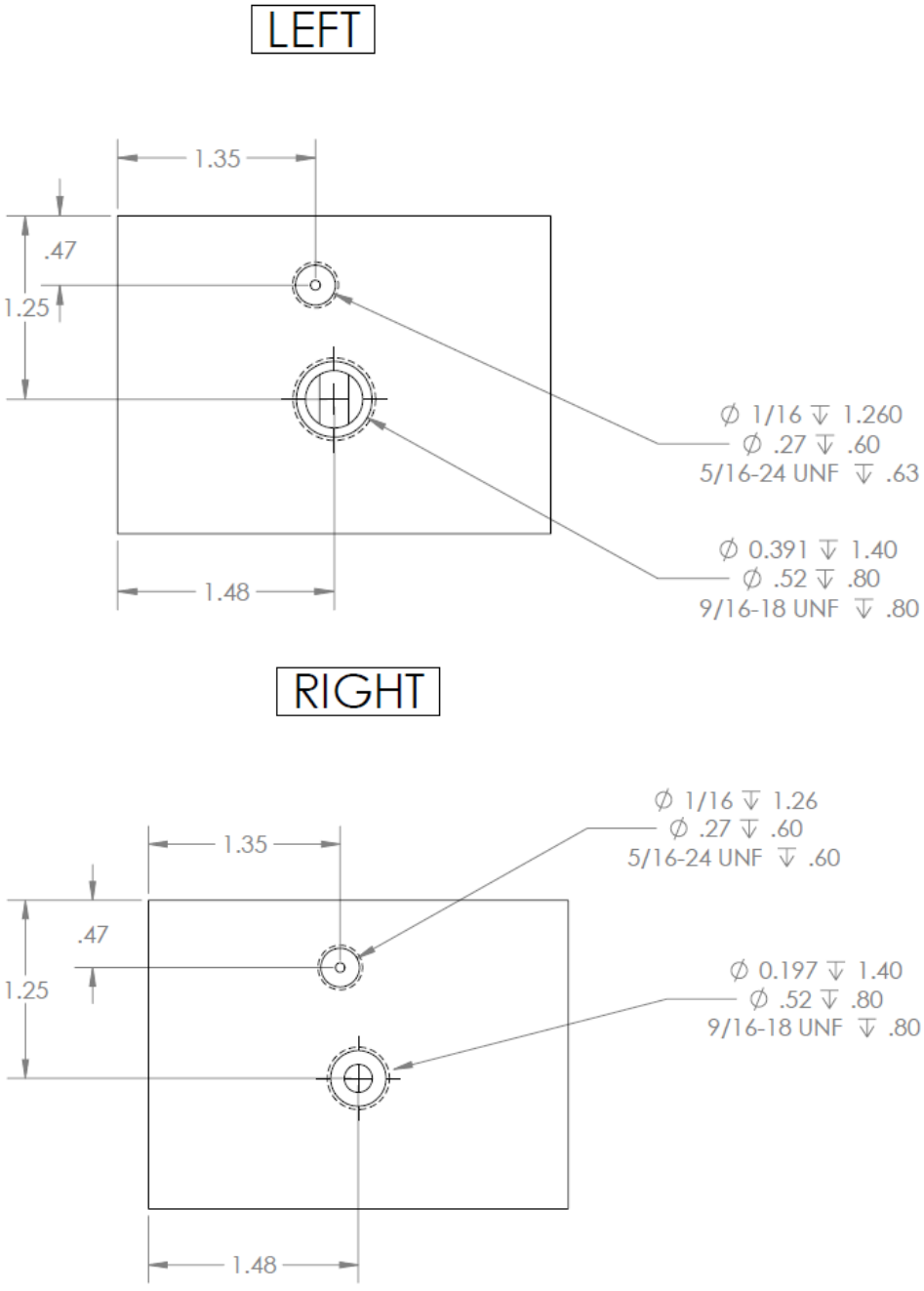

Figure B.22. Technical drawings of the manifold base for the 9 × 9 test vehicle; all dimensions in inches unless otherwise specified.

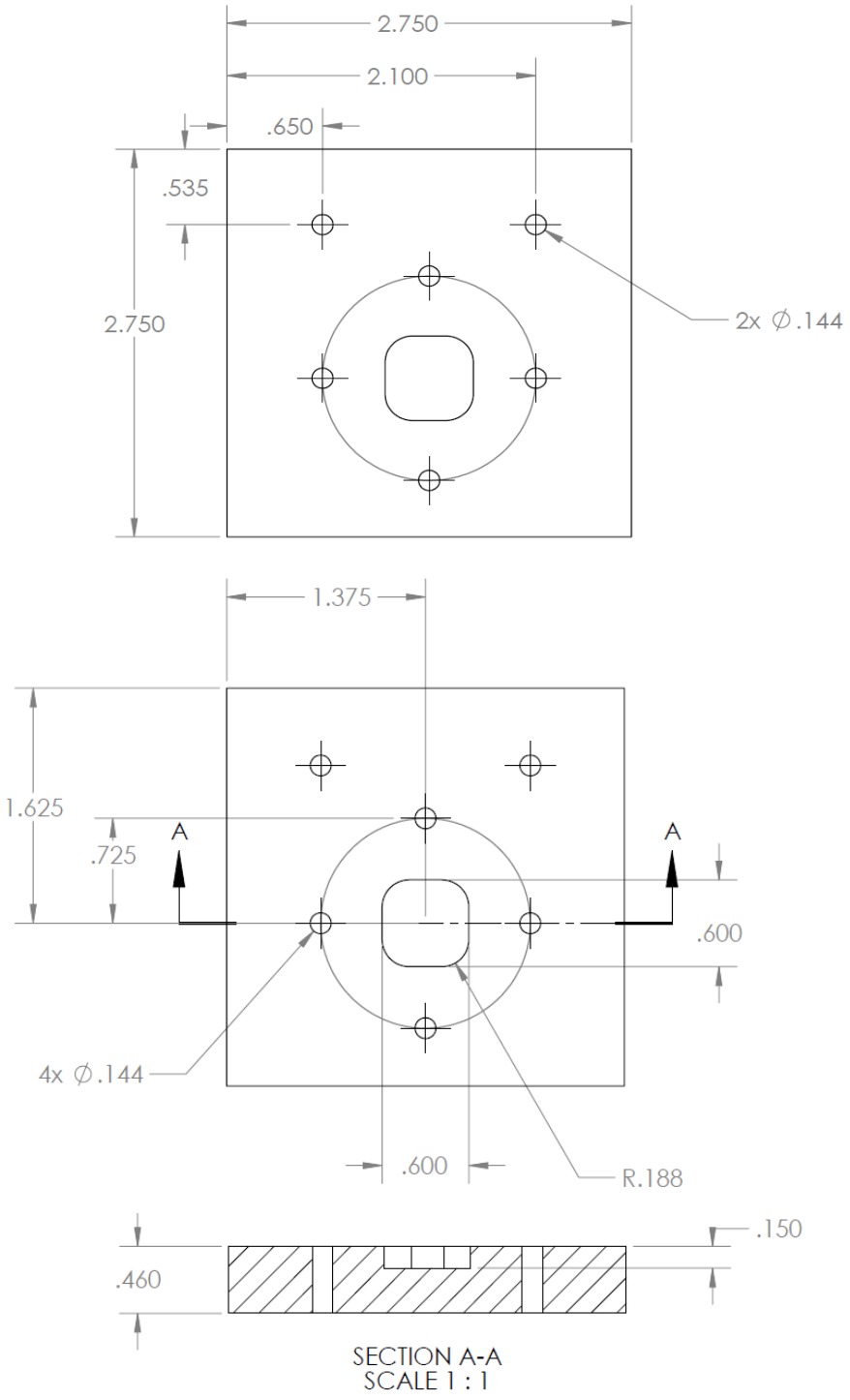

Figure B.23. Technical drawings of the insulation block for the 9 × 9 test vehicle; all dimensions in inches unless otherwise specified.

APPENDIX C. MATLAB SCRIPTS FOR DATA REDUCTION

This section contains MATLAB codes used in the post-processing of the experimentally measured data. The data reduction script reads the raw data from a .CSV file and calls functions that compute steady-state averages of the measured values as well as derived values (*e.g.*, reference temperature, heat transfer coefficient, thermal resistance) and the uncertainties in each of the measured and calculated values.

Note that the MATLAB codes for the post-processing of the data that is obtained using the heater layout that contains the hotspot heater are not listed because they are nominally the same as those provided; the procedure for calculating background heat flux is slightly altered due to the power to each zone being recorded separately. There are also additional lines of code to calculate the hotspot heat flux.

Table C.1. A list of codes for post-processing data.

Script Number	Function Name	Description	Page Number
C.1	Script_Reduction_H1.m	Script to input location of raw data, steady-state times, and channel geometry	155
C.2	Function_Reduction_H1.m	Function to reduce the raw data into steady-state averages and to compute derived values	156
C.3	Function_Error_H1.m	Function to calculate the uncertainty of the calculated variables	161

C.1. Script_Reduction_H1.m

```
Clc; clear all; close all;

% file name containing raw data
meas.file_name = 'YYYYMMDD_SAMPLE##_WWxHHH_XXXgmin.xls';
meas.write_file = strcat(meas.file_name(1:end-4),'_reduced.xls');
meas.write_loc  = 'C:\Data\ReducedData\';

% times for steady-state data points
date = 'MM/DD/YYYY';
SS_times = ['HH:MM'; 'HH:MM'; 'HH:MM'];
SS_times = strcat(date1,{' '},SS_times1,':00 PM');

% number of raw data points
meas.raw_points = 120;

% array of RTD numbers for any broken/incorrect RTDs
%(enter 'RTD_off =[0]' if all RTDs are working properly)
meas.RTD_off = [0];

% Geometry Constants
geom.w_c         = 13.7;          % Channel width [um]
geom.w_f         = 16.3;          % Fin width [um]
geom.d_c         = 105;           % Channel depth [um]
geom.d_b_Si      = 100;           % Silicon base thickness [um]
geom.d_b_SiO2    = 0.35;          % Oxide base thickness [um]
geom.P_w_meas    = 225;           % Wetted perimeter (3 sides) [um]
geom.A_c_meas    = 1420;          % Channel cross-sectional area [um^2]
geom.L           = 1500;          % Total flow length [um]
geom.A_base      = 2.5e7;         % Base area [um^2]
geom.N           = 50;            % Number of parallel channels [-]
geom.N_RTD       = 9;             % Number of RTDs
geom.heaterzones= 9;              % Number of heater zones
geom.sinkzones   = 9;             % Number of heat sink zones

% Calculated geometry values
geom.A_w_meas= geom.P_w_meas*geom.L;    % Wetted channel area [um^2]
geom.P_w_calc= 2*geom.d_c + geom.w_c; % Wetted perimeter (3 sides) [um]
geom.A_w_fin= 2*geom.d_c*geom.L;        % Wetted area (3 sides) [um]
geom.d_H= 4*geom.A_c_meas/geom.P_w_calc; % Hydraulic Diameter [um]

% location of the data reduction function
addpath C:\Data\MATLAB\
meas.write_name = strcat(meas.write_loc,meas.write_file);
meas.chip_num = meas.file_name(10:17);

% call to the data reduction function
[prop, geom, meas, avg, calc] = function_datareduction_heater1(geom, meas);
[error] = function_error_heater1(prop, geom, meas, avg, calc);
[write] = function_write_heater1(prop, geom, meas, avg, calc, error);
```

C.2. Function_Reduction_H1.m

```
function [prop, geom, meas, avg, calc] = Reduction_H1(geom, meas)

% number of heat fluxes tested
meas.SS_points = length(meas.SS_times);
% total number of steady-state data points
meas.total_points = meas.raw_points*meas.SS_points;

N_RTD = 9;
% Chip RTDs to use (0 = don't use, 1 = use)
meas.RTD_use = ones(N_RTD,1);
% array that will set all of the broken RTDs' temperatures to zero
for i = 1:N_RTD
    if any(abs(i-meas.RTD_off)<0.0001)
        meas.RTD_use(i,1) = 0;
    end
end
% scale RTD_use so as not to skew averages
meas.RTD_use = meas.RTD_use*N_RTD/sum(meas.RTD_use);

%% Material Constants
% All fluid values are taken at the saturation temperature at 1 bar
prop.k_Si       = 149;          % Silicon therm.  cond.  [W/mK]
prop.k_SiO2     = 1.5;          % Oxide therm.  cond.  [W/mK]
prop.k_HFE      = 0.062;        % HFE-7100 therm.  cond.  {W/mK]
prop.rho_HFE    = 1429;         % HFE-7100 density [kg/m^3]
prop.cp_HFE     = 1253;         % HFE-7100 specific heat [J/kgK]
prop.LV_HFE     = 1.1e5;        % HFE-7100 latent heat of vap.  [J/kg]

%% Raw Data
meas.SS_times = cellstr(meas.SS_times);
range_times = sprintf('A3:A%d',22000);
[blank, alltimes] = xlsread(meas.file_name,'Sheet1',range_times);
SS_row = zeros(size(meas.SS_times,1),1);
for i=1:size(meas.SS_times,1)
    SS_row(i)= strmatch(meas.SS_times(i),alltimes)+2;
    range = sprintf('B%d:DE%d',SS_row(i),SS_row(i)+meas.raw_points-1);
    raw.all_rs(:,i,:) = xlsread(meas.file_name,'Sheet1',range);
end

% Final column containing chip temperatures
col_f = 9*2;
% Starting column containing chip temperatures used
col_i = 1;

% Temperatures
for i = 1:N_RTD
    raw.T.chip_V(:,:,i)=raw.all_rs(:,:,col_i+i);      % Raw RTD voltages (V)
    raw.T.chip_T(:,:,i)=raw.all_rs(:,:,col_i+i+N_RTD-1);    % RTD temps.  (C)
end
raw.T.pump      = raw.all_rs(:,:,col_f+2);
raw.T.flow      = raw.all_rs(:,:,col_f+3);
raw.T.pre_in    = raw.all_rs(:,:,col_f+4);
raw.T.pre_out   = raw.all_rs(:,:,col_f+6);
```

```
raw.T.cond_in   = raw.all_rs(:,:,col_f+8);
raw.T.cond_out  = raw.all_rs(:,:,col_f+9);
raw.T.reservoir = raw.all_rs(:,:,col_f+12);
raw.T.in        = raw.all_rs(:,:,col_f+13);
raw.T.out       = raw.all_rs(:,:,col_f+14);
raw.T.icept     = raw.all_rs(:,:,col_f+23);
raw.T.ambient   = raw.all_rs(:,:,col_f+24);

% Pressures
raw.P.in_I = raw.all_rs(:,:,col_f+15);            % Raw inlet pressure signal
(A)
raw.P.in_P = raw.all_rs(:,:,col_f+16);            % Calibrated inlet pressure
(kPa)
raw.P.out_I = raw.all_rs(:,:,col_f+17);           % Raw outlet pressure signal
(A)
raw.P.out_P = raw.all_rs(:,:,col_f+18);           % Calibrated outlet pressure
(kPa)
raw.P.dP_I = raw.all_rs(:,:,col_f+19);            % Raw outlet pressure signal
(A)
raw.P.dP_P = raw.all_rs(:,:,col_f+20);            % Calibrated outlet pressure
(kPa)

% Flow Rate
raw.flow.flow_I = raw.all_rs(:,:,col_f+21);            % Raw flow rate signal
(A)
raw.flow.flow_m  = raw.all_rs(:,:,col_f+22);           % Calibrated flow rate
(g/min)

% Electrical Power
raw.power.shunt_dV = raw.all_rs(:,:,col_f+25);
raw.power.divider_dV = raw.all_rs(:,:,col_f+26);
meas.shunt_R = 0.05;                              % Shunt resistance (ohms)
meas.divider_R1 = 100;
meas.divider_R2 = 200000;

% Measured Divider and Shunt Voltages to voltage and current
raw.power.I_meas = raw.power.shunt_dV./meas.shunt_R;
raw.power.V_meas                                                          =
(meas.divider_R1+meas.divider_R2)./meas.divider_R1.*raw.power.divider_dV;


%% Averages over single heat flux

for i = 1:meas.SS_points
    for j = 1:N_RTD
        % Steady-state temp for each chip RTD (meas.SS_points x # of RTDs)
        avg.T.chip_temps(i,j) = mean(raw.T.chip_T(:,i,j));
    end
    % Average chip temp.  at each SS point (only using
    avg.T.chip_avetemp(i)                                                 =
mean(avg.T.chip_temps(i,:).*transpose(meas.RTD_use));
    avg.T.chip_avetemp(i) = avg.T.chip_avetemp(i);
    avg.T.in(i)         = mean(raw.T.in(:,i));
    avg.T.out(i)        = mean(raw.T.out(:,i));
    avg.flow_m(i)       = mean(raw.flow.flow_m(:,i));
```

```
    avg.P_in(i)          = mean(raw.P.in_P(:,i));
    avg.P_out(i)         = mean(raw.P.out_P(:,i));
    avg.dP(i)            = mean(raw.P.dP_P(:,i));
    avg.V_divider(i)     = mean(raw.power.shunt_dV(:,i));
    avg.V_shunt(i)       = mean(raw.power.divider_dV(:,i));      % [mV]
    avg.I(i)             = mean(raw.power.I_meas(:,i));
    avg.V(i)             = mean(raw.power.V_meas(:,i));
end

%% Data Reduction
calc.R = avg.V ./ avg.I;
%Pressure drop
calc.dP = avg.P_in - avg.P_out;
% Electrical power
% power (W) calculated from the recorded values from the power supply (W)
calc.power_rec = avg.V.*avg.I;
% power (W) calculated using divider (V) and shunt (I)
calc.power_meas = avg.V.*avg.I;
% heat loss (W)
calc.power_loss = heatloss(avg.T.chip_avetemp);
% heat into test section (W)
calc.power_in = calc.power_meas-calc.power_loss;
% base heat flux (W/m2)
calc.flux_base = calc.power_in/geom.A_base*1e12;
% wall heat flux (W/m2)
calc.flux_wall = calc.power_in/(geom.A_w_meas*9*geom.N)*1e12;

% Flow rate
avg.flow_m  = avg.flow_m/1000/60;            % convert (g/min) to (kg/s)
calc.flow_v = avg.flow_m/prop.rho_HFE;       % vol.  flow rate (m3/s)
calc.flow_G = avg.flow_m/(geom.A_c_meas*1e-12*geom.N*geom.cells*2);
avg.flow_G  = mean(calc.flow_G);

% Pumping power
calc.pumppower = calc.dP*1000.*calc.flow_v;

% base temperature
avg.T.base = avg.T.chip_avetemp - calc.flux_base*(geom.d_b_Si/prop.k_Si ...
                                          + geom.d_b_SiO2/prop.k_Si)/1e6;

% Saturation temperature at outlet pressure
prop.T_sat = HFE7100_P_to_Tsat(avg.P_out);

% sensible heat (W) to get fluid to saturation temperature
calc.power_sens = avg.flow_m.*prop.cp_HFE.*(prop.T_sat-avg.T.in);

% exit quality
calc.x_ex = (calc.power_in-calc.power_sens)./(avg.flow_m.*prop.LV_HFE);

% determine reference temperature for heat transfer coefficient and boiling
% curve
for i = 1:meas.SS_points
if calc.power_sens(i) >= calc.power_in(i)
    % reference temperature if boiling does not occur (C)
    calc.T_ref(i) = 0.5*(avg.T.in(i)+avg.T.out(i));
```

```
    calc.z_sat(i) = geom.L/2;
else
    % approximate location of saturation in streamwise direction (micron)
    calc.z_sat(i) = calc.power_sens(i)/calc.power_in(i)*geom.L/2;
    % pressure at z_sat (kPa)
    calc.P_z_sat(i)                =                avg.P_in(i)-(avg.P_in(i)-
avg.P_out(i))/(geom.L/2)*calc.z_sat(i);
    % temperature at z_sat (C)
    calc.T_z_sat(i) = HFE7100_P_to_Tsat(calc.P_z_sat(i));
    % temperature at outlet (C)
    calc.T_sat_out(i) = HFE7100_P_to_Tsat(avg.P_out(i));
    % reference temperature if boiling occurs (C)
    calc.T_ref(i) = 0.5*((avg.T.in(i)+calc.T_z_sat(i))*calc.z_sat(i) + ...
        (calc.T_z_sat(i)+avg.T.out(i))*(geom.L/2 - calc.z_sat(i)))/(geom.L/2);
end
end

thresh = 0.01;
eff_o_old = ones(1,meas.SS_points);                % start with guess of nu=1

% temperature difference between chip and reference (C)
calc.dT_chip_ref = avg.T.base - calc.T_ref;

% temperature difference between chip and fluid inlet (C)
calc.dT_chip_in = avg.T.base - avg.T.in;

% Wall heat transfer coefficient calculation
for i = 1:meas.SS_points
    dh = 100;
    while abs(dh) > thresh
        calc.h_old(i) = calc.flux_wall(i)/(eff_o_old(i)*calc.dT_chip_ref(i));
        % skip data points where the fluid temperature is greater than the
        % chip temperature or the flux is negative
        if calc.dT_chip_ref(i) <= 0
            break
        elseif calc.flux_base(i) <= 0
            break
        end
        calc.m(i) = sqrt(2*calc.h_old(i)/(prop.k_Si*geom.w_f*1e-6));
        calc.eff_f(i)  =  tanh(calc.m(i)*geom.d_c*1e-6)/(calc.m(i)*geom.d_c*1e-
6);
        calc.eff_o_new(i) = 1-(geom.A_w_fin/geom.A_w_meas)*(1-calc.eff_f(i));
        calc.h_new(i)                                                          =
calc.flux_wall(i)/(calc.eff_o_new(i)*calc.dT_chip_ref(i));
        dh = calc.h_new(i) - calc.h_old(i);
        calc.eff_o_new(i) = calc.eff_o_new(i) - dh/abs(calc.h_new(i))/10;
        eff_o_old(i) = calc.eff_o_new(i);
    end
    % effective thermal resistance calculation
    calc.R_eff(i)    =    (avg.T.chip_avetemp(i)-avg.T.in(i))*geom.A_base*1e-
12/calc.power_in(i);
    % base heat transfer coefficient
    calc.h_base(i) = calc.flux_base(i)/calc.dT_chip_ref(i);
end

% Nusselt Number
```

```
calc.Nu = calc.h_new.*(geom.d_H.*1e-6)./prop.k_HFE;

end
```

C.3. Function_Error_H1.m

```
function [error] = function_error_heater1(prop, geom, meas, avg, calc)

A_c_meas    = geom.A_c_meas*1e-12*geom.N*geom.cells;
A_w_meas    = geom.A_w_meas*1e-12*geom.N*geom.cells;
A_w_fin     = geom.A_w_fin*1e-12*geom.N*geom.cells;
A_base      = geom.A_base*1e-12;
d_b_Si      = geom.d_b_Si*1e-6;
d_b_SiO2    = geom.d_b_SiO2*1e-6;
z_x0        = calc.z_sat.*1e-6;
w_f         = geom.w_f*1e-6;
d_c         = geom.d_c*1e-6;

% Stated errors
error.T_chip    = 1.0;
error.T_in      = 0.5;
error.T_out     = 0.5;
error.T_sat_x0  = 1.0;
error.T_sat_out = 0.25;
error.V_divider = 0.01*avg.V_divider;
error.V_shunt   = 0.001*avg.V_shunt;
error.P_out     = 0.3;
error.P_diff    = 0.17;
error.flow_m    = 0.001*avg.flow_m;
error.A_wet     = 0.05*A_w_meas;
error.A_fin     = 0.05*A_w_fin;
error.A_c       = 0.05*A_c_meas;
error.d_base    = 5e-6;
error.d_c       = 5e-6;
error.w_c       = 2e-6;
error.d_SiO2    = 1e-8;
error.h_LV      = 400;
error.cp        = 20;
error.k_Si      = 1;
error.L         = 25e-6;
error.h_guess   = 0.06*calc.h_new;

Q_loss_C1 = 0.02768;
Q_loss_C2 = 22.5;
error.Q_loss_C1 = 0.1*Q_loss_C1;
error.Q_loss_C2 = 0.1*Q_loss_C2;

R1 = meas.divider_R1;
R2 = meas.divider_R2;
R_shunt = meas.shunt_R;
N_tot = geom.N*geom.cells*2;

error.R1 = 0.05*R1;
error.R2 = 0.05*R2;
error.R_shunt = 0.001*R_shunt;

error.V                                                                    =
sqrt((((R1+R2)./R1).*error.V_divider).^2+(avg.V_divider./R2.*error.R1).^2+(av
g.V_divider.*R1./(R2.^2).*error.R2).^2);
```

```
error.I                                                                    =
sqrt((error.V_shunt./R_shunt).^2+(avg.V_shunt./R_shunt.^2.*error.R_shunt).^2);
error.P_el = sqrt((avg.I.*error.V).^2+(avg.V.*error.I).^2);

error.T_chip_avg = error.T_chip./sqrt(geom.N_RTD);

error.G = sqrt((error.flow_m./(A_c_meas.*N_tot)).^2+...
    (avg.flow_m./(A_c_meas.^2.*N_tot).*error.A_c).^2);

error.Q_loss = sqrt(((avg.T.chip_avetemp-Q_loss_C2)*error.Q_loss_C1).^2+...
    (Q_loss_C1*error.T_chip_avg).^2+(Q_loss_C1*error.Q_loss_C2).^2);

error.Q_in = sqrt((error.P_el).^2+(error.Q_loss).^2);       %[W]
error.flux_base = error.Q_in/0.25;                          %[W/cm2]

error.T_base = sqrt(error.T_chip_avg.^2+...
    (1./A_base.*(d_b_Si./prop.k_Si+d_b_SiO2./prop.k_SiO2).*error.Q_in).^2+...
    (calc.power_in./(A_base.*prop.k_Si).*error.d_base).^2+...
    (calc.power_in./(A_base.*prop.k_SiO2).*error.d_SiO2).^2);

error.x_exit = sqrt((error.Q_in./(avg.flow_m.*prop.LV_HFE)).^2+...
    (calc.power_in.*error.flow_m./(avg.flow_m.^2.*prop.LV_HFE)).^2+...
    ((avg.T.out-avg.T.in).*error.cp./prop.cp_HFE.^2).^2+...
    (prop.cp_HFE.*error.T_out./prop.LV_HFE.^2).^2+...
    (prop.cp_HFE.*error.T_in./prop.LV_HFE.^2).^2);


for i = 1:size(meas.SS_times,1)
    if calc.power_in(i) < 0
        error.T_ref(i) = 0;
        error.z_x0(i) = 0;
        error.m(i) = 0;
        error.eta_f(i) = 0;
        error.eta_o(i) = 0;
        error.h(i) = 0;
        error.R_eff(i) = 0;
    else

        error.R_eff(i) = sqrt((A_base/calc.power_in(i)*error.T_chip_avg)^2+...
            (A_base/calc.power_in(i)*error.T_in)^2+...
            (A_base*(avg.T.chip_avetemp(i)-
avg.T.in(i))/(calc.power_in(i)^2)*error.Q_in(i))^2);

        if calc.x_ex(i) < 0
            error.T_ref(i) = 0.5*sqrt(error.T_in^2+error.T_out^2);
            error.z_x0(i) = 0;
        else
            error.z_x0(i)                                                  =
sqrt((avg.flow_m(i)*prop.cp_HFE*(calc.T_sat_out(i)-
avg.T.in(i))*geom.L/calc.power_in(i)^2*error.Q_in(i))^2+...
                (prop.cp_HFE*(calc.T_sat_out(i)-
avg.T.in(i))*geom.L/calc.power_in(i)*error.flow_m(i))^2+...
                (avg.flow_m(i)*(calc.T_sat_out(i)-
avg.T.in(i))*geom.L/calc.power_in(i)*error.cp)^2+...
```

```
(avg.flow_m(i)*prop.cp_HFE*geom.L/calc.power_in(i)*error.T_sat_out)^2+...

(avg.flow_m(i)*prop.cp_HFE*geom.L/calc.power_in(i)*error.T_in)^2+...
                (avg.flow_m(i)*prop.cp_HFE*(calc.T_sat_out(i)-
avg.T.in(i))/calc.power_in(i)*error.L)^2);

            error.T_ref(i) = 0.5*sqrt((error.T_sat_x0)^2+...
                (z_x0(i)/geom.L*error.T_in)^2+...
                ((1-z_x0(i)/geom.L)*error.T_sat_out)^2+...
                ((avg.T.in(i)-calc.T_sat_out(i))/geom.L*error.z_x0(i))^2);
        end

        error.m(i)                                                              =
sqrt((1/(2*calc.h_new(i)*prop.k_Si*w_f))*error.h_guess(i)^2+...
            (calc.h_new(i)/(2*prop.k_Si^3*w_f))*error.k_Si^2+...
            (calc.h_new(i)/(2*prop.k_Si*w_f^3))*error.d_c^2);

        error.eta_f(i)          =          sqrt((((sech(calc.m(i)*d_c))^2/d_c-
tanh(calc.m(i)*d_c)/(calc.m(i)*d_c^2))*error.d_c)^2+...
            (((sech(calc.m(i)*d_c))^2/calc.m(i)-
tanh(calc.m(i)*d_c)/(calc.m(i)^2*d_c))*error.m(i))^2);

        error.eta_o(i) = 1/A_w_meas*sqrt(((1-calc.eff_f(i))*error.A_fin)^2+...
            (A_w_fin/A_w_meas*(1-calc.eff_f(i))*error.A_wet)^2+...
            (A_w_fin*error.eta_f(i))^2);

        error.h(i)                                                              =
calc.power_in(i)/(calc.eff_o_new(i)*A_w_meas*calc.dT_chip_ref(i))*...
            sqrt((error.Q_in(i)/calc.power_in(i))^2+...
                 (error.eta_o(i)/calc.eff_o_new(i))^2+...
                 (error.A_wet/A_w_meas)^2+...
                 (error.T_base(i)/calc.dT_chip_ref(i))^2+...
                 (error.T_ref(i)/calc.dT_chip_ref(i))^2);
    end
end

%Relative Errors (percentages)
error.rel.P_el      = abs(error.P_el./calc.power_meas)*100;
error.rel.T_chip    = abs(error.T_chip_avg./avg.T.chip_avetemp)*100;
error.rel.G         = abs(error.G./calc.flow_G)*100;
error.rel.Q_loss    = abs(error.Q_loss./calc.power_loss)*100;
error.rel.Q_in      = abs(error.Q_in./calc.power_in)*100;
error.rel.R_eff     = abs(error.R_eff./calc.R_eff)*100;
error.rel.T_base    = abs(error.T_base./avg.T.base)*100;
error.rel.x_exit    = abs(error.x_exit./calc.x_ex)*100;
error.rel.h         = abs(error.h./calc.h_new)*100;
```

APPENDIX D. SIMULTANEOUS HOTSPOT AND BACKGROUND HEAT FLUX DISSIPATION RESULTS

This section shows the additional data that was obtained for multiple mass fluxes and background heat fluxes. All data were obtained using Sample 33 × 470 and the inlet temperature was maintained at 59 °C and the outlet pressure remained at 121 kPa.

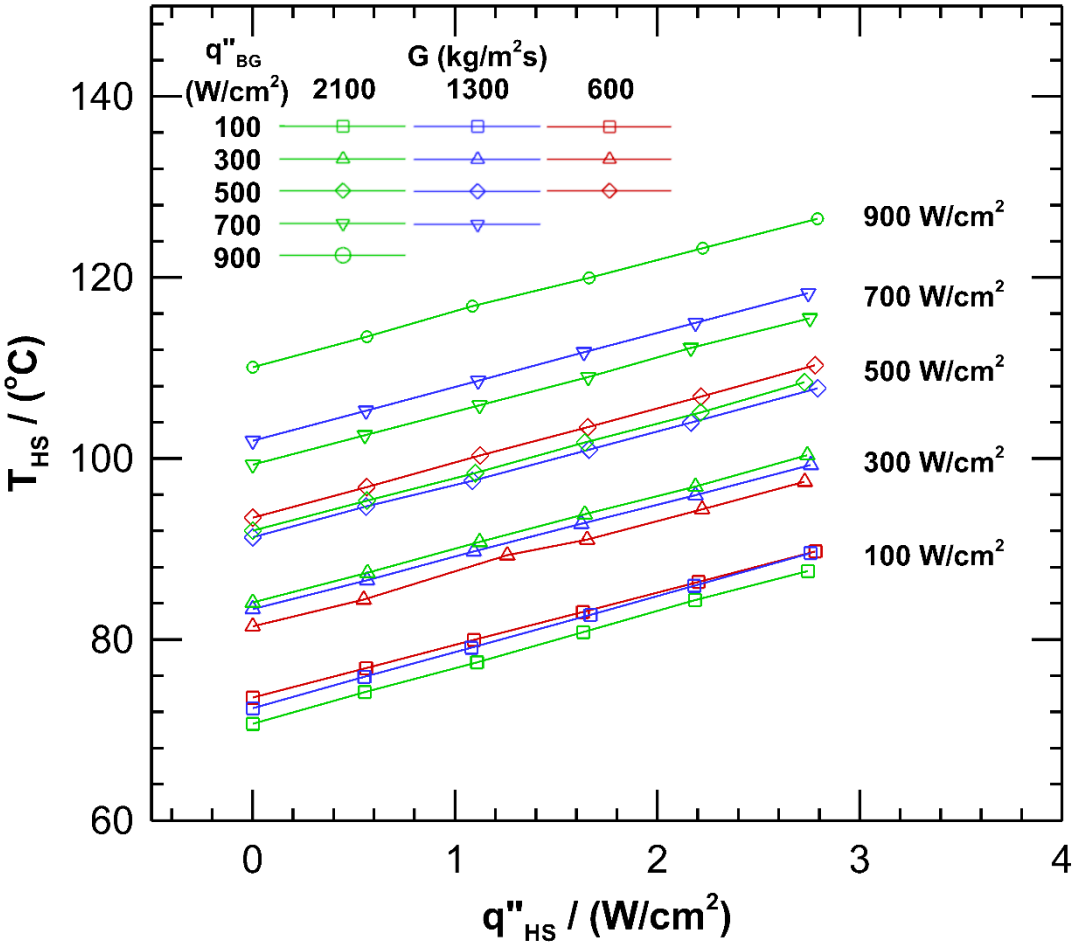

Figure D.1. Hotspot temperatures as a function of hotspot heat flux for a variety of fluid mass fluxes and background heat fluxes.

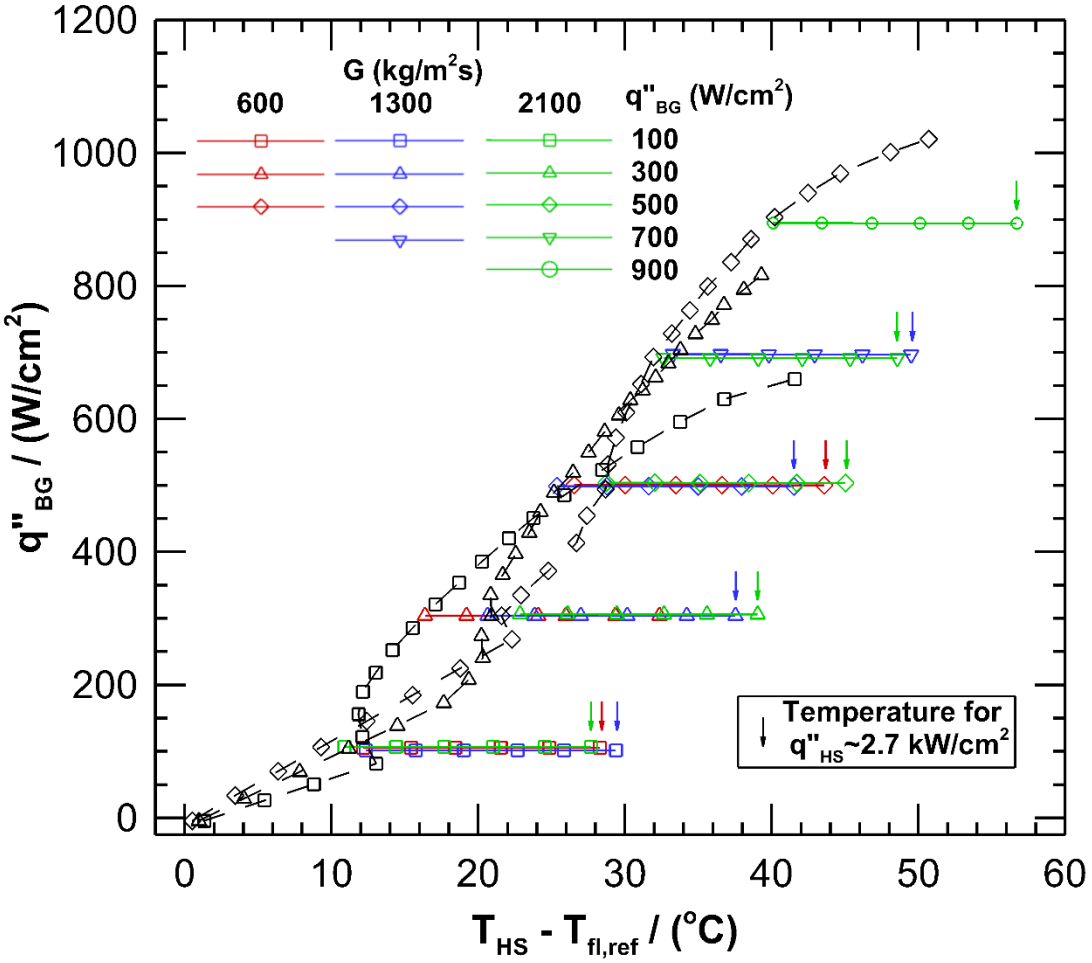

Figure D.2. Hotspot temperature rise above fluid reference temperature; boiling curves with black data points show hotspot temperature at zero hotspot heat flux and colored data points show hotspot temperature during hotspot testing (arrow pointing to hotspot temperature at the maximum hotspot heat flux of ~2,700 W/cm²).

APPENDIX E. EXPERIMENTAL UNCERTAINTY ANALYSIS

This section provides an overview of the procedure for determining the uncertainty of the reported experimental values. The uncertainties are calculated for both versions of the heater/sensor layout (labeled ‘Single Heater’ and ‘3x3 Heater’).

Table E.1. Stated uncertainties from the manufacturers.

Measurement	Instrument	Manufacturer	Uncertainty
Chip temperature	RTDs (calibrated)	Custom	± 1.0 °C
Heater voltage	Voltage divider	Custom	± 1.0 %
Heater current	Shunt resistor	Empro	± 0.1 %
Fluid inlet temperature	T-type thermocouple (calibrated)	Omega	± 0.5 °C
Fluid outlet temperature	T-type thermocouple (calibrated)	Omega	± 0.5 °C
Outlet pressure	Gage pressure transducer	Wika	± 0.3 kPa
Pressure drop	Differential pressure transducer	Omega PX-2300	± 0.17 kPa
Mass flow rate	Coriolis mass flow meter	Micromotion	± 0.1 %
Wetted area			± 5 %
Channel cross-sectional area			± 5 %
Base silicon thickness			± 5 μm
Base oxide thickness			± 0.01 μm

Mass Flux

$$G = \frac{\dot{m}}{A_c N} \tag{E.1}$$

$$\begin{aligned}
\Delta G &= \sqrt{\left(\frac{1}{A_c N}\left(\Delta\dot{m}\right)\right)^2 + \left(\frac{-\dot{m}}{A_c^2 N}\left(\Delta A_c\right)\right)^2} \\
&= \sqrt{\left(\frac{1}{900A_c}\left(.001\dot{m}\right)\right)^2 + \left(\frac{\dot{m}}{900A_c^2}\left(.05A_c\right)\right)^2} \\
&= \sqrt{\left(\frac{\dot{m}}{A_c}\left(1.11\times10^{-5}\right)\right)^2 + \left(\frac{\dot{m}}{A_c}\left(5.56\times10^{-5}\right)\right)^2} \\
\Delta G &= \left(5.67\times10^{-5}\right)\frac{\dot{m}}{A_c}
\end{aligned}$$

Heater Voltage

Single Heater

$$V = V_{divider}\left(\frac{R_1 + R_2}{R_2}\right) \tag{E.2}$$

$$\begin{aligned}
\Delta V &= \sqrt{\left(\left(\frac{R_1 + R_2}{R_2}\right)\Delta V_{divider}\right)^2 + \left(\left(\frac{V_{divider}}{R_2}\right)\Delta R_1\right)^2 + \left(\left(\frac{V_{divider}\left(R_1\right)}{\left(R_2\right)^2}\right)\Delta R_2\right)^2} \\
&= \sqrt{\left(\left(\frac{5000+100}{100}\right)0.001V_{divider}\right)^2 + \left(\left(\frac{V_{divider}}{100}\right)0.01\right)^2 + \left(\left(\frac{V_{divider}\left(5000\right)}{\left(100\right)^2}\right)0.01\right)^2} \\
&= \left(\sqrt{.0026 + 1\times10^{-8} + 2.5\times10^{-5}}\right)V_{divider} \\
\Delta V &= 0.051V_{divider}
\end{aligned}$$

3 × 3 Heater

$$V = \left(\frac{R_1 + R_2}{R_2}\right)\sum_{i=1}^{10} V_{divider,i} \tag{E.3}$$

$$\begin{aligned}\Delta V &= 10\sqrt{\left(\left(\frac{R_1+R_2}{R_2}\right)\Delta V_{divider}\right)^2+\left(\left(\frac{V_{divider,avg}}{R_2}\right)\Delta R_1\right)^2+\left(\left(\frac{V_{divider,avg}\left(R_1\right)}{\left(R_2\right)^2}\right)\Delta R_2\right)^2}\\ &= \sqrt{\left(\left(\frac{5000+100}{100}\right)0.001V_{divider}\right)^2+\left(\left(\frac{V_{divider,avg}}{100}\right)0.01\right)^2+\left(\left(\frac{V_{divider,avg}\left(5000\right)}{\left(100\right)^2}\right)0.01\right)^2}\\ &= \left(\sqrt{.0026+1\times10^{-8}+2.5\times10^{-5}}\right)V_{divider,avg}\\ \Delta V &= 0.051V_{divider,avg}\end{aligned}$$

Heater Current

$$I = \frac{V_{shunt}}{R_{shunt}} \tag{E.4}$$

$$\begin{aligned}\Delta I &= \sqrt{\left(\left(\frac{1}{R_{shunt}}\right)\Delta V_{shunt}\right)^2+\left(\left(\frac{-V_{shunt}}{R_{shunt}^2}\right)\Delta R_{shunt}\right)^2}\\ &= \sqrt{\left(\left(\frac{1}{0.05}\right)0.001V_{shunt}\right)^2+\left(\left(\frac{V_{shunt}}{\left(.05\right)^2}\right)0.001\left(.05\right)\right)^2}\\ &= \left(\sqrt{.0004V_{shunt}^2+.0004V_{shunt}^2}\right)\\ \Delta I &= 0.028V_{shunt}\end{aligned}$$

Heater Power

Single Heater

$$P_{el} = VI \tag{E.5}$$

$$\begin{aligned}\Delta P_{el} &= \sqrt{\left(\frac{V_{shunt}}{R_{shunt}}\left(\Delta V\right)\right)^2+\left(V_{divider}\left(\frac{R_1+R_2}{R_2}\right)\left(\Delta I\right)\right)^2}\\ &= \sqrt{\left(\frac{V_{shunt}}{.05}\left(0.051V_{divider}\right)\right)^2+\left(V_{divider}\left(\frac{5000+100}{100}\right)\left(0.028V_{shunt}\right)\right)^2}\\ \Delta P_{el} &= 1.56V_{divider}V_{shunt}\end{aligned}$$

3 × 3 Heater

$$P_{el} = \sum_{i=1}^{9} V_i I_i \tag{E.6}$$

$$\begin{aligned}
\Delta P_{el} &= \sqrt{\left(\frac{V_{shunt}}{R_{shunt}}(\Delta V)\right)^2 + \left(V_{divider}\left(\frac{R_1+R_2}{R_2}\right)(\Delta I)\right)^2} \\
&= \sqrt{\left(\frac{V_{shunt}}{.05}(0.051V_{divider})\right)^2 + \left(V_{divider}\left(\frac{5000+100}{100}\right)(0.028V_{shunt})\right)^2} \\
\Delta P_{el} &= 1.56V_{divider}V_{shunt}
\end{aligned}$$

Chip Temperature

$$T_{chip,avg} = \sum_{1}^{N_{RTD}} \frac{T_{chip,i}}{N_{RTD}} \tag{E.7}$$

$$\begin{aligned}
\Delta T_{chip,avg} &= \sqrt{\left(\frac{\Delta T_{chip,1}}{N_{RTD}}\right)^2 + \left(\frac{\Delta T_{chip,2}}{N_{RTD}}\right)^2 + \ldots + \left(\frac{\Delta T_{chip,N_{RTD}}}{N_{RTD}}\right)^2} \\
&= \sqrt{N_{RTD}\left(\frac{\Delta T_{chip}}{N_{RTD}}\right)^2} = \frac{\Delta T_{chip}}{\sqrt{N_{RTD}}} \\
\Delta T_{chip,avg} &= \frac{1.0}{\sqrt{9.0}}°C = \pm 0.33°C
\end{aligned}$$

Heat Loss

$$Q_{loss} = C_1\left(T_{chip,avg} - C_2\right) \tag{E.8}$$

$$\begin{aligned}
\Delta Q_{loss} &= \sqrt{\left(\left(T_{chip,avg} - C_2\right)\left(\Delta C_1\right)\right)^2 + \left(\left(C_1\right)\left(\Delta T_{chip,avg}\right)\right)^2 + \left(\left(-C_1\right)\left(\Delta C_2\right)\right)^2} \\
&= \sqrt{\left(\left(T_{chip,avg} - 21.52\right)(.00129)\right)^2 + \left((0.02576)(0.33)\right)^2 + \left((0.02576)(1)\right)^2} \\
&= \sqrt{1.66\times10^{-6}\left(T_{chip,avg} - 21.52\right)^2 + 0.0007358}
\end{aligned}$$

Heat Input

$$Q_{in} = P_{el} - Q_{loss} \tag{E.9}$$

$$\begin{aligned}
\Delta Q_{in} &= \sqrt{\left(\Delta P_{el}\right)^2 + \left(\Delta Q_{loss}\right)^2} \\
&= \sqrt{\left(1.56 V_{divider} V_{shunt}\right)^2 + \left(\sqrt{1.66\times10^{-6}\left(T_{chip,avg} - 21.52\right)^2 + 0.0007358}\right)^2} \\
&= \sqrt{\left(1.56 V_{divider} V_{shunt}\right)^2 + 1.66\times10^{-6}\left(T_{chip,avg} - 21.52\right)^2 + 0.0007358}
\end{aligned}$$

Thermal Resistance

$$R_{eff} = \frac{A_b\left(T_{chip,avg} - T_{fl,in}\right)}{Q_{in}} \tag{E.10}$$

$$\begin{aligned}
\Delta R_{eff} &= \sqrt{\left(\frac{A_b}{Q_{in}}\left(\Delta T_{chip,avg}\right)\right)^2 + \left(\frac{-A_b}{Q_{in}}\left(\Delta T_{fl,in}\right)\right)^2 + \left(\frac{-A_b\left(T_{chip,avg} - T_{fl,in}\right)}{{Q_{in}}^2}\left(\Delta Q_{in}\right)\right)^2} \\
&= \frac{A_b}{Q_{in}}\sqrt{{\Delta T_{chip,avg}}^2 + \left(\Delta T_{fl,in}\right)^2 + \left(\frac{\left(T_{chip,avg} - T_{fl,in}\right)}{Q_{in}}\left(\Delta Q_{in}\right)\right)^2} \\
&= \frac{2.5\times10^{-5}}{Q_{in}}\sqrt{\left(0.33\right)^2 + \left(0.5\right)^2 + \left(\frac{\left(T_{chip,avg} - 59\right)}{Q_{in}}\left(\Delta Q_{in}\right)\right)^2}
\end{aligned}$$

Chip Base Temperature

$$T_{base,avg} = T_{chip,avg} - \frac{Q_{in}}{A_b}\left(\frac{d_b}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}}\right) \tag{E.11}$$

$$\begin{aligned}
\Delta T_{base,avg} &= \sqrt{\left(1\left(\Delta T_{chip,avg}\right)\right)^2 + \left(\frac{1}{A_b}\left(\frac{d_b}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}}\right)\left(\Delta Q_{in}\right)\right)^2 + \left(\frac{Q_{in}}{A_b k_{Si}}\left(\Delta d_b\right)\right)^2 + \left(\frac{Q_{in}}{A_b k_{SiO_2}}\left(\Delta d_{SiO_2}\right)\right)^2} \\
&= \sqrt{\left(1.0\right)^2 + \left(\frac{1}{2.5\times10^{-5}}\left(\frac{d_b}{149} + \frac{d_{SiO_2}}{1.3}\right)\left(\Delta Q_{in}\right)\right)^2 + \left(\frac{Q_{in}\left(5\times10^{-6}\right)}{\left(2.5\times10^{-5}\right)\left(149\right)}\right)^2 + \left(\frac{Q_{in}\left(1\times10^{-8}\right)}{\left(2.5\times10^{-5}\right)\left(149\right)}\right)^2} \\
&= \sqrt{1.0 + \left(\left(268.5 d_b + 3.08\times10^{4} d_{SiO_2}\right)\Delta Q_{in}\right)^2 + 1.8\times10^{-6} Q_{in}^2}
\end{aligned}$$

Location of x=0 along channel

$$z_{x=0} = \frac{\dot{m} c_p \left(T_{sat,p_{out}} - T_{fl,in}\right) L}{Q_{in}} \tag{E.12}$$

$$\Delta z_{x=0} = \sqrt{\begin{array}{l} \left(\frac{\dot{m} c_p \left(T_{sat,p_{out}} - T_{fl,in}\right) L}{{Q_{in}}^2}\left(\Delta Q_{in}\right)\right)^2 + \left(\frac{c_p \left(T_{sat,p_{out}} - T_{fl,in}\right) L}{Q_{in}}\left(\Delta \dot{m}\right)\right)^2 + \ldots \\ \left(\frac{\dot{m}\left(T_{sat,p_{out}} - T_{fl,in}\right) L}{Q_{in}}\left(\Delta c_p\right)\right)^2 + \left(\frac{\dot{m} c_p L}{Q_{in}}\left(\Delta T_{sat,p_{out}}\right)\right)^2 + \ldots \\ \left(\frac{\dot{m} c_p L}{Q_{in}}\left(\Delta T_{fl,in}\right)\right)^2 + \left(\frac{\dot{m} c_p \left(T_{sat,p_{out}} - T_{fl,in}\right)}{Q_{in}}\left(\Delta L\right)\right)^2 \end{array}}$$

Exit Quality

$$x_{exit} = \frac{Q_{in} - \dot{m} c_p \left(T_{out} - T_{in}\right)}{\dot{m} h_{fg}} \tag{E.13}$$

$$\Delta x_{exit} = \sqrt{\begin{array}{l} \left(\frac{1}{\dot{m} h_{fg}}\left(\Delta Q_{in}\right)\right)^2 + \left(\frac{Q_{in}}{h_{fg}{\dot{m}}^2}\left(\Delta \dot{m}\right)\right)^2 + \left(\frac{c_p \left(T_{out} - T_{in}\right) - Q_{in}}{\dot{m} {h_{fg}}^2}\left(\Delta h_{fg}\right)\right)^2 + \\ \left(\frac{\left(T_{out} - T_{in}\right)}{h_{fg}}\left(\Delta c_p\right)\right)^2 + \left(\frac{c_p}{h_{fg}}\left(\Delta T_{out}\right)\right)^2 + \left(\frac{c_p}{h_{fg}}\left(\Delta T_{in}\right)\right)^2 \end{array}}$$

$$= \sqrt{\begin{array}{l} \left(\frac{1}{1.1\times10^5 \dot{m}}\left(\Delta Q_{in}\right)\right)^2 + \left(\frac{Q_{in}}{1.1\times10^5 {\dot{m}}^2}\left(0.001\dot{m}\right)\right)^2 + \left(\frac{1253\left(T_{out} - 59\right) - Q_{in}}{\dot{m}\left(1.1\times10^5\right)^2}\left(400\right)\right)^2 + \\ \left(\frac{\left(T_{out} - 59\right)}{1.1\times10^5}\left(20\right)\right)^2 + 2\left(\frac{1253}{1.1\times10^5}\left(0.5\right)\right)^2 \end{array}}$$

$$= \sqrt{\begin{array}{l} 8.26\times10^{-11}\left(\frac{\Delta Q_{in}}{\dot{m}}\right)^2 + 1.18\times10^{-15}\left(\frac{Q_{in}}{\dot{m}}\right)^2 + 1.37\times10^{-12}\left(\frac{\left(T_{out} - 59\right)}{\dot{m}}\right)^2 + \\ 3.31\times10^{-8}\left(T_{out} - 59\right)^2 + 6.5\times10^{-5} \end{array}}$$

Reference Temperature

$$T_{ref} = \begin{cases} = \dfrac{T_{in} + T_{out}}{2} & ,if\ x_{exit} \le 0 \\ = \left(\dfrac{T_{sat,x_{sat}} + T_{fl,in}}{2} \right) \dfrac{z_{sat}}{L} + \left(\dfrac{T_{sat,x_{sat}} + T_{sat,L}}{2} \right) \dfrac{(L - z_{sat})}{L} & ,if\ x_{exit} > 0 \end{cases} \tag{E.14}$$

$$\begin{aligned} \Delta T_{ref} &= \sqrt{\left(\frac{1}{2}(\Delta T_{in}) \right)^2 + \left(\frac{1}{2}(\Delta T_{out}) \right)^2} \\ &= \frac{1}{2}\sqrt{(\Delta T_{in})^2 + (\Delta T_{out})^2} \\ &= \frac{1}{2}\sqrt{(0.5)^2 + (0.5)^2} \\ &= 0.354°C \end{aligned}$$

$$\begin{aligned} \Delta T_{ref} &= \frac{1}{2}\sqrt{\left((\Delta T_{sat,z_{sat}}) \right)^2 + \left(\left(\frac{z_{sat}}{L} \right)(\Delta T_{fl,in}) \right)^2 + \left(\left(1 - \frac{z_{sat}}{L} \right)(\Delta T_{sat,L}) \right)^2 + \left(\left(\frac{T_{fl,in} - T_{sat,L}}{L} \right)(\Delta z_{sat}) \right)^2} \\ &= \frac{1}{2}\sqrt{\left((1.0) \right)^2 + \left(\left(\frac{z_{sat}}{7.5\times10^{-4}} \right)(0.5) \right)^2 + \left(\left(1 - \frac{z_{sat}}{7.5\times10^{-4}} \right)(0.25) \right)^2 + \left(\left(\frac{59 - 65.7}{7.5\times10^{-4}} \right)(5\times10^{-5}) \right)^2} \\ &= \frac{1}{2}\sqrt{5.55\times10^5 z_{sat}{}^2 - 666 z_{sat} + 2.2} \end{aligned}$$

$$0.71°C \le \Delta T_{ref} \le 0.74°C$$

Fin Efficiency

$$\eta_0 = 1 - \frac{NA_f}{A_{wet}}(1 - \eta_f), \tag{E.15}$$

$$\eta_f = \frac{\tanh(md_c)}{md_c}, \quad \text{where} \quad m = \sqrt{\frac{2h_{wall}}{k_{Si} w_f}}. \tag{E.16}$$

$$\Delta m = \sqrt{\left(\frac{1}{\sqrt{2h_{wall}k_{Si}w_f}}\left(\Delta h_{wall}\right)\right)^2 + \left(\sqrt{\frac{h_{wall}}{2k_{Si}{}^3 w_f}}\left(\Delta k_{Si}\right)\right)^2 + \left(\sqrt{\frac{h_{wall}}{2k_{Si}w_f{}^3}}\left(\Delta w_f\right)\right)^2}$$

$$= \sqrt{\frac{1}{2h_{wall}k_{Si}w_f}\left(\Delta h_{wall}\right)^2 + \frac{h_{wall}}{2k_{Si}{}^3 w_f}\left(\Delta k_{Si}\right)^2 + \frac{h_{wall}}{2k_{Si}w_f{}^3}\left(\Delta w_f\right)^2}$$

$$\Delta\eta_f = \sqrt{\left(\left(\frac{\operatorname{sech}^2\left(md_c\right)}{d_c} - \frac{\tanh\left(md_c\right)}{md_c{}^2}\right)\left(\Delta d_c\right)\right)^2 + \left(\left(\frac{\operatorname{sech}^2\left(md_c\right)}{m} - \frac{\tanh\left(md_c\right)}{m^2 d_c}\right)\left(\Delta m\right)\right)^2}$$

$$\Delta\eta_0 = \frac{N}{A_{wet}}\sqrt{\left(\left(1-\eta_f\right)\left(\Delta A_f\right)\right)^2 + \left(\frac{A_f}{A_{wet}}\left(1-\eta_f\right)\left(\Delta A_{wet}\right)\right)^2 + \left(A_f\left(\Delta\eta_f\right)\right)^2}$$

Wall Heat Transfer Coefficient

$$h_{wall} = \frac{Q_{in}}{\eta_o A_{wet}\left(T_{base,avg} - T_{ref}\right)} \tag{E.17}$$

$$\Delta h_{wall} = \sqrt{\begin{array}{l}\left(\left(\frac{1}{\eta_o A_{wet}\left(T_{base,avg}-T_{ref}\right)}\right)\left(\Delta Q_{in}\right)\right)^2 + \left(\left(\frac{-Q_{in}}{\eta_o{}^2 A_{wet}\left(T_{base,avg}-T_{ref}\right)}\right)\left(\Delta\eta_o\right)\right)^2 + \ldots \\ \left(\left(\frac{-Q_{in}}{\eta_o A_{wet}{}^2\left(T_{base,avg}-T_{ref}\right)}\right)\left(\Delta A_{wet}\right)\right)^2 + \left(\left(\frac{-Q_{in}}{\eta_o A_{wet}\left(T_{base,avg}-T_{ref}\right)^2}\right)\left(\Delta T_{base,avg}\right)\right)^2 + \ldots \\ \left(\left(\frac{Q_{in}}{\eta_o A_{wet}\left(T_{base,avg}-T_{ref}\right)^2}\right)\left(\Delta T_{ref}\right)\right)^2\end{array}}$$

$$= \frac{Q_{in}}{\eta_o A_{wet}\left(T_{base,avg}-T_{ref}\right)}\sqrt{\left(\frac{\Delta Q_{in}}{Q_{in}}\right)^2 + \left(\frac{\Delta\eta_o}{\eta_o}\right)^2 + \left(\frac{\Delta A_{wet}}{A_{wet}}\right)^2 + \left(\frac{\Delta T_{base,avg}}{T_{base,avg}-T_{ref}}\right)^2 + \left(\frac{\Delta T_{ref}}{T_{base,avg}-T_{ref}}\right)^2}$$

APPENDIX F. SINGLE-PHASE MODELING

This section presents work that was completed to predict the performance of manifold microchannels during single-phase operation. Figure F.1 shows the model mesh for a given channel geometry; both the fluid and the solid walls were meshed using a square mesh. A single fluid inlet and a single outlet are modeled. All of the outside walls have a symmetry boundary condition, which is used to simulate the repeating nature of this 'unit cell'. The CFD simulation software ANSYS Fluent was used to solve the energy equation in the solid and fluid phases and the mass and momentum conservation equations in the fluid phase. Conjugate heat transfer occurs at the fluid-solid interface. Figure F.2 shows the temperature, pressure, and fluid velocities for Samples A, B, and C (Chapter 3) at a heat flux of 75 W/cm² and a mass flux of 2900 kg/m²s. The pressure drop and maximum fluid velocity increase with increasing channel depth because the inlet fluid velocity increases with increasing depth for a given channel mass flux. The wall temperature for Sample A is much higher than Samples B and C due to the reduced wetted area.

Figure F.3 shows the average base temperature above the fluid inlet as a function of pressure drop. The 15 μm-wide channels show a much larger difference in performance compared to the 10 μm-wide channels; The shallowest 15 μm-wide channel has ~8.5× less wetted area compared to the deepest channel whereas the difference is <0.5× for the 30 μm-wide channels. For all pressure drops, the 15 μm-wide, 300 μm-deep channel has the lowest temperature rise out of these channel geometries. Figure F.4 and Figure F.5 show the effect of channel depth on base temperature for 15 μm-wide and 30 μm-wide channels, respectively. For the thinner channels, there is a large temperature drop at a given pressure drop when the depth is increased from 100 μm to 200 μm after which the performance is largely unchanged. For the wider channels, increasing the depth up to 300 μm results in a small decrease in temperature at a given pressure drop. Increasing the depth past ~400 μm can result in higher chip temperatures at some pressure drops.

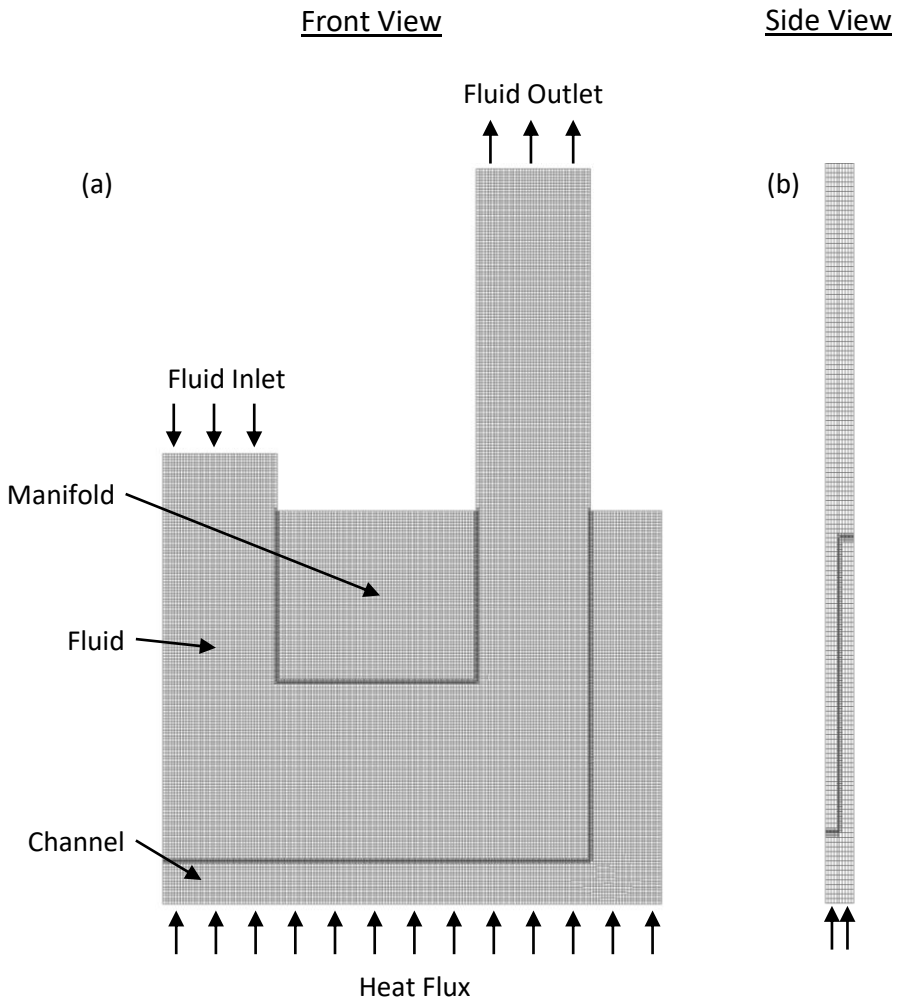

Figure F.1. Images of the meshed model domain for the CFD simulations from the (a) front and (b) side.

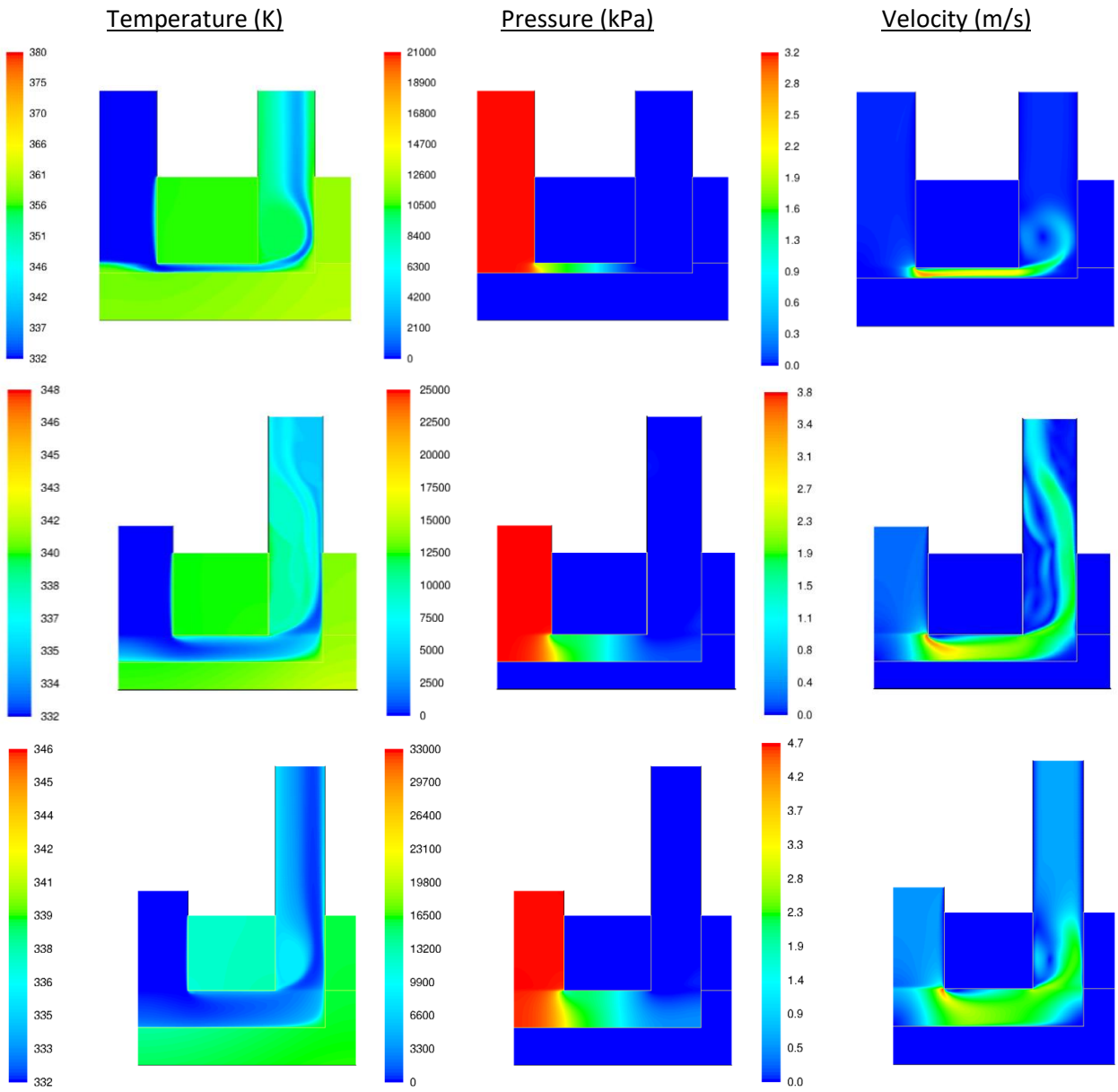

Figure F.2. Temperature, pressure and velocity profiles in MMCs of (a) Sample A, (b) Sample B, and (c) Sample C (from Section 3.3) for a channel mass flux of 2900 kg/m²s and a heat flux of 75 W/cm² during single-phase operation.

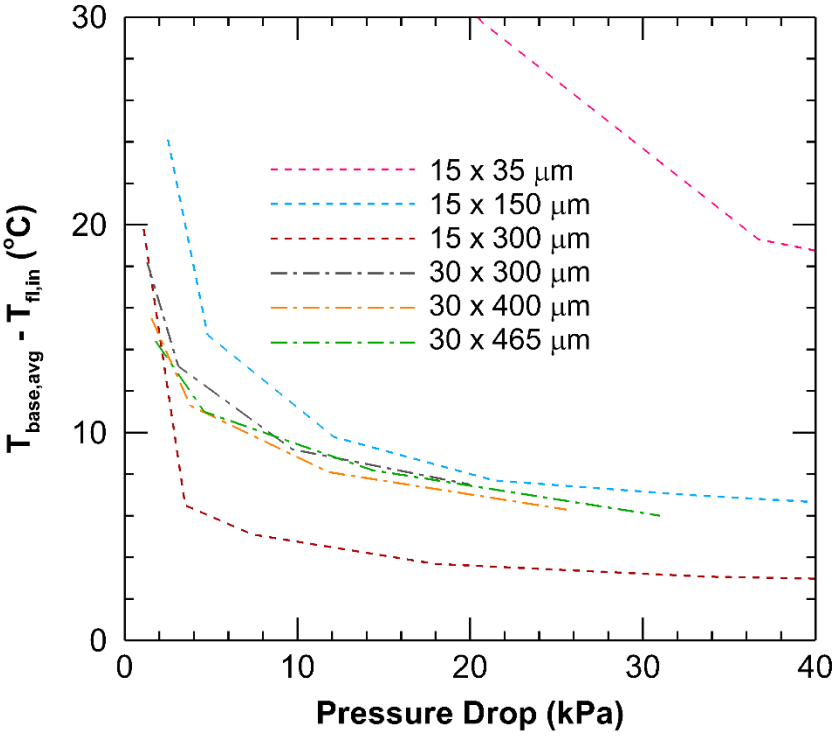

Figure F.3. Average base temperature above the fluid inlet temperature as a function of pressure drop for the channel geometries tested in Chapters 3 and 4.

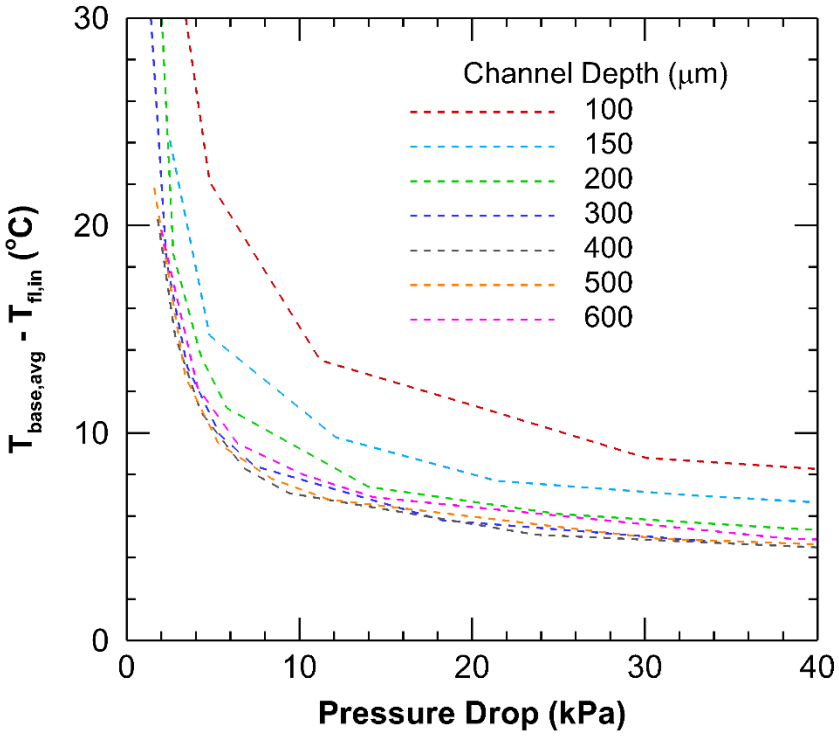

Figure F.4. Average base temperature above the fluid inlet temperature as a function of pressure drop for a fixed channel width of 15 μm and various channel depths.

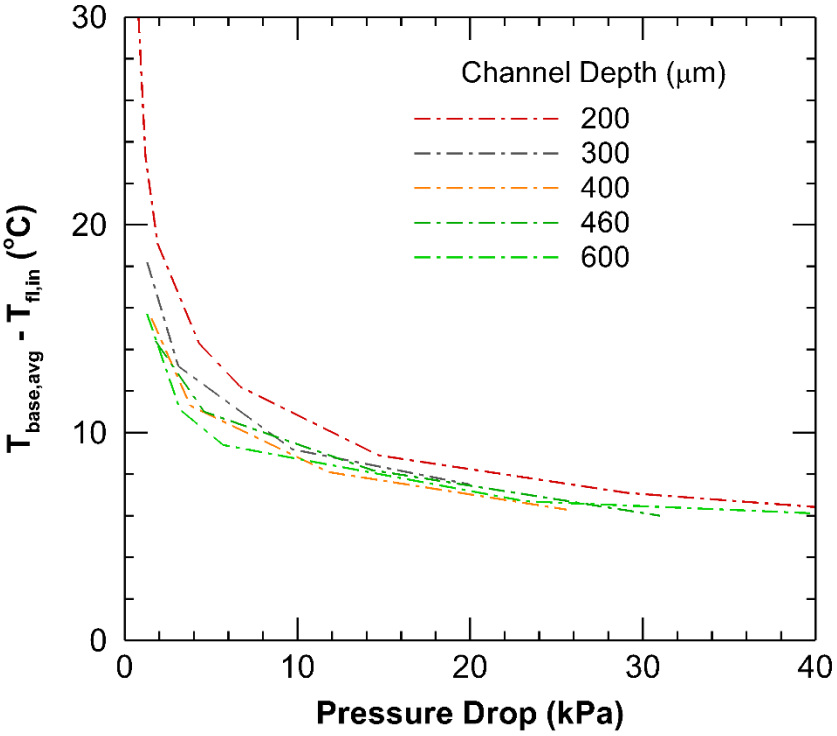

Figure F.5. Average base temperature above the fluid inlet temperature as a function of pressure drop for a fixed channel width of 30 μm and various channel depths.

VITA

Kevin Patrick Drummond was born in Youngstown, OH in 1987. He received his Bachelor of Science in Mechanical Engineering and Master of Science in Mechanical Engineering from Ohio University in 2010 and 2012, respectively. He joined the School of Mechanical Engineering at Purdue University in 2012 to pursue his PhD. He studied under the advisement of Prof. Suresh V. Garimella and Dr. Justin A. Weibel. His research interests include the design, fabrication, experimental testing, and characterization of multiphase microchannel heat sink performance with a focus on manifold microchannel heat sinks. He was the recipient of the Cordier Fellowship for study in Mechanical Engineering.

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