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Analysis and Mitigation of Common-mode Behavior in Hybrid Vehicle Applications

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ANALYSIS AND MITIGATION OF COMMON-MODE BEHAVIOR IN HYBRID VEHICLE APPLICATIONS

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To my parents, Bruce and Lorena, whose encouragement gave rise to this thesis

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SYMBOLS

m	mass
P	geometric point
K	number of lines
r	radius
S	switch state
p	Heaviside operator
v	voltage
i	current
λ	flux linkage
q	charge
E	back electromotive force
k	coupling coefficient
Z	impedance
r	resistance
L	inductance
X	reactance
Y	admittance
g	conductance
C	capacitance
B	susceptance
T	period or temporal duration
d	duty cycle
m	modulation index
f	ordinary frequency

ω angular frequency or angular speed

T_e electromagnetic torque

ABBREVIATIONS

1SVPWM	first space vector modulation
3AVM	three active vector modulation
3DSVPWM	three-dimensional space vector modulation
AC	alternating current
ASMG	Automated State Model Generator
AZVC	active zero vector control
CM	common mode
CMEC	common-mode equivalent circuit
DC	direct current
DM	differential mode
DM/CM	mixed mode
EMF	electromotive force
EMTP	electromagnetic transients program
ESR	equivalent series resistance
ESL	equivalent series inductance
FB10	Full-bridge converter with ten switches
H6	H-bridge converter with six switches
HERIC	Highly Efficient and Reliable Inverter Concept
IST3PWM	interleaved sine-triangle modulation with third-harmonic injection
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MATLAB	Matrix laboratory
PCKA	PC Krause & Associates

PWM	pulse width modulation
RMS	root-mean-square
ST3PWM	sine-triangle modulation with third harmonic injection
STPWM	sine-triangle modulation
SVPWM	space vector modulation
WBG	wide bandgap

GLOSSARY

Admittance	reciprocal of impedance with real part conductance and imaginary part susceptance, SI unit of siemans (S)
Alternating Current	periodically varying circuit quantities associated with symmetric flow in both directions; in regards to a system, one intended to carry power through AC quantities in the differential mode
Antiprism	a polyhedron composed of two parallel, identical polygons rotated with respect with one another such that the vertices of each polygon are connected by triangular faces
Bipyramid	a polyhedron formed by joining two, identical pyramids at their bases
Common Mode	circuit mode associated with effort across and flow between a set of conductors and an arbitrary return path usually including some part of the system identified as ground
Current	flow of electric charge past a cross-sectional area, SI unit of amperes (A)
Differential Mode	circuit mode associated with effort across and flow between each conductor in a pair usually comprising the typical operation of the system
Direct Current	constant circuit quantities associated with flow in one direction; in regards to a system or bus, one intended to carry DC power in the differential mode
Gyroelongated	describing a polyhedron that has added axial height by the insertion of an antiprism into the middle

H-bridge	a common type of full-wave, single-phase active rectifier and topology typically drawn such that there are four electronic switches, one on each of the vertical segments of a capital letter "H", with the AC source or load drawn on the horizontal segment
Impedance	complex ratio of AC voltage to AC current $\left(Z = \frac{\widetilde{V}}{\widetilde{I}}\right)$ that includes amplitude and phase information; the real part is resistance, and the imaginary part is reactance, SI unit of ohms (Ω)
Mixed Mode	also called fully detailed in regards to models or phase quantity in regards to circuit quantities, a combination of the differential mode and common mode
Root-mean-square	an operation associated with the effective value of a sinusoidal quantity that squares all values over a period, averages them together, and takes the square root of the result
Voltage	electrical potential difference between two points that gives electric potential energy per unit charge, SI unit of volts (V)

ABSTRACT

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Modeling techniques to predict common-mode (CM) current in an electric drive intended for a hybrid vehicle are examined. A particular focus is on the derivation of a common-mode equivalent circuit (CMEC) in which machines, cables, and passives are represented by their passive coupling paths to ground and power electronic devices are replaced by equivalent voltage sources. The interconnection of components is accomplished using a judicious selection of a reference point used to define CM voltage.

Circuit-based simulation results are presented for a system consisting of a permanent magnet generator coupled to an active rectifier that is providing power to an inverter/permanent magnet motor. The simulation results are compared to those obtained from a detailed system model in which the switching behavior of all semiconductor devices is represented. It is shown that the CM current predicted using the CM equivalent circuit closely matches that obtained using the detailed system model.

Finally, several switching strategies are presented for three-phase, three-leg converters with the intent of reducing the CM voltage at a single or multitude of frequencies. The CM equivalent circuit is used to explore the impact that these strategies have on CM current in modern power electronics systems as well as future systems that will be dominated by wide-bandgap semiconductor devices.

1. INTRODUCTION

The advent of fast-switching power electronic devices has led to unintended voltages and currents that are often referred to as common-mode (CM) issues. Large common-mode voltages can lead to insulation breakdown and drive large common-mode currents. Common-mode currents flow through parasitic paths in the electrical system and often negatively affect electromagnetic compatibility, i.e., false triggering of fault detection systems, and motor bearing wear-out. [1] [2] With these considerations in mind, more powerful modeling approaches are sought to predict and eventually mitigate common-mode behavior.

The modeling of common-mode systems to date has mostly been confined to two approaches. The first involves adding parasitic elements to the differential-mode (DM) circuit used for intended operation. [3] [4] By simulating the circuit with parasitics included, mixed-mode (DM/CM) behavior may be predicted, including inter-mode coupling effects. This approach has the disadvantage of needing significant computing power in order to simulate the stiff system dynamics. The second is the establishment of common-mode equivalent circuits by characterizing paths through which common-mode current flows and establishing sources that represent power electronics or imbalance. [5] [6] [7] While the computing power required to model this smaller linear circuit is reduced, there had been few attempts to create a process to form, connect, and apply these CM equivalent circuits until recently. In the writings of Brovont and Pekarek [8] [9], an approach was derived to transform the mixed-mode circuits into common-mode circuits. In this thesis, this approach is applied to a drive system that includes two machines and their drive circuits.

1.1 Literature Review

Currents flowing through the shafts of machines were first identified in the 1920's, and the modern rise of power electronics in inverters has led to heightened scrutiny of their effects on bearings. [10] Methods to predict and measure shaft currents have been presented by several researchers. [11] [3] [4] In general, the modeling approach used to study shaft currents in this thesis is based on the work of Chen, Lipo, and Fitzgerald. [11]

The CM equivalent circuit approach presented follows the work of Brovont and Pekarek. [8] [9] Previous attempts to create common-mode equivalent circuits involved fitting empirical impedance data to equivalent resistances, inductances, and capacitances as presented by Naik, Nondahl, Melfi, Schiferl, and Wang. [3] While such efforts may produce accurate models, they are not readily adaptable as modifications are made to the system nor do they give intuition based on machine physics. In order to construct common-mode equivalent circuits for the variety of circuit blocks that might be encountered in a hybrid vehicle drive system, the Brovont and Pekarek modeling method is detailed after this literature review.

Hardware solutions to common-mode effects include filters such as the one designed by Rendusara and Enjeti made to handle the effects of long motor cables. [12] More comprehensive solutions include modifying the inverter topology and accepting additional computational complexity and switching losses. One example uses a four-leg inverter for active CM voltage control and incorporating a second-order filter as presented by Julian, Oriti, and Lipo [13]. Another uses an active common-noise canceler (ACC) in which a fourth phase leg responds to noise on three-phase cables by injecting a signal into a four-winding transformer as Ogasawara, Ayano, and Akagi detailed. [6] By combining multi-level converters with many filtering stages, Parreiras, Prado, and Filho produced a mining pump drive that severely curtails common-mode effects at the cost of many added components. [7] One of the most drastic solutions proposed involved constructing open-end machines, connecting a second three-leg

drive, and using clamp-on ferrites as Narasimhan, Tewari, Severson, Baranwal, and Mohan suggested. [14]

As might be anticipated, common-mode behavior can also affect DC systems that are supplied by power electronics converters attached to the DC bus. Common-mode chokes and multi-stage filters remain an option for handling common-mode behavior. Buck converters can introduce a complimentary switch and balance inductance to make the circuit block symmetric and reduce the transmission of common-mode current. [15] Virtually every other form of switched mode power supply admits a balanced counterpart that prevents the generation of large common-mode voltages. [16] Numerous other DC-DC converter topologies such as H6 (H-bridge with six switches) and the Highly Efficient and Reliable Inverter Concept (HERIC) are used to construct single-phase inverters and active rectifiers that minimize common-mode behavior compared to the conventional H-bridge with four switches. [17] While the space of single-phase power electronic converters may seem distinct from three-phase converters, novel ideas such as the Full-bridge with ten switches (FB10) topology can result from the hybridization of single-phase and three-phase topologies meant to reduce common-mode behavior. [18] Despite the advantages of modified power converter topologies, they tend to be rather scarce outside of academic settings due to their novelty and small selection of commercial options available. For these reasons, no further attention is paid to this area of research.

When addressing common-mode behavior in existing products, modifications to software are generally preferred to hardware changes due to the relative simplicity of implementation without affecting the supply chain or manufacturing processes. To that end, alterations are made to simple switching strategies such as sine-triangle modulation (STPWM) or space vector modulation (SVPWM) to minimize the common-mode voltage generated. A survey of published techniques is included in the final chapter of this thesis.

1.2 Basis of Modeling Approach

The common-mode equivalent circuit derivations utilized in this research will take a mixed-mode circuit and algorithmically produce a common-mode equivalent circuit. The judicious use of definitions of CM voltage and CM current will enable this process. One may predict common-mode behavior and evaluate the type and placement of mitigation measures to use using standard elementary circuit theory. [8]

Recall that the differential mode represents the desired operation of a circuit. DM voltages are conceptualized as existing between pairs of terminals, and DM currents are assumed to travel down one conductor and back through the second. In contrast, the common mode represents the unintended operation of a circuit due to parasitic couplings, asymmetric design, or the environmental influence of a power system. CM voltages are conceptualized as existing between all terminals in a set and an arbitrary point, and CM currents are thought to travel down the set of all conductors simultaneously and back through a ground path.

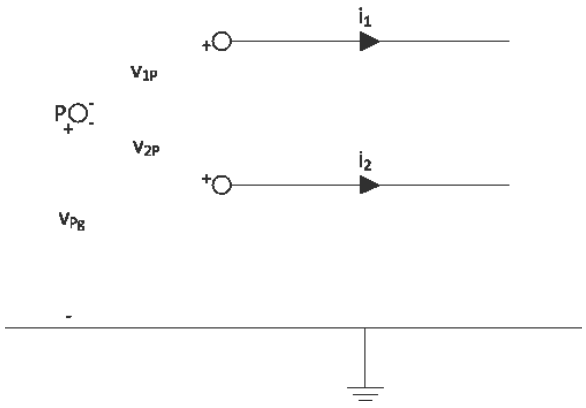


Fig. 1.1. Diagram for Common-mode and Differential-Mode Definitions

For the pair of wires in Figure 1.1, the convention is that current is considered positive going into the system. DM voltage, DM current, CM voltage, and CM current may be defined for use in this thesis using Figure 1.1 as a basis [8]:

$$v_{DM} \triangleq v_{1P} - v_{2P} \tag{1.1}$$

$$i_{DM} \triangleq \frac{1}{2}(i_1 - i_2) \tag{1.2}$$

$$v_{CM} \triangleq \frac{1}{2}(v_{1P} + v_{2P}) \tag{1.3}$$

$$i_{CM} \triangleq i_1 + i_2 \tag{1.4}$$

While the form of the DM voltage in (1.1) may be familiar, DM current (1.2) might seem a little strange. Suppose that current I flows down from terminal 1 and returns through terminal 2 ($i_2 = -i_1$). In this situation, $i_{DM} = \frac{1}{2}[(I) - (-I)] = \frac{1}{2}[2I] = I$ with zero CM current. Similarly, the CM voltage in (1.3) may be verified by supposing that the voltages are balanced with respect to arbitrary reference point P $\left(v_{1P} = +\frac{V}{2},\, v_{2P} = -\frac{V}{2}\right)$. In this situation where P is the differential voltage midpoint, $v_{CM} = \frac{1}{2}(\frac{+V}{2} + \frac{-V}{2}) = 0$ and $v_{DM} = V$.

Care must be taken when generalizing these definitions to $K \geq 2$ lines.

$$v_{CM} \triangleq \frac{1}{K}\sum_{k=1}^{K} v_{kP}, \text{ (single voltage of this form)} \tag{1.5}$$

$$i_{CM} \triangleq \sum_{k=1}^{K} i_k, \text{ (single current of this form)} \tag{1.6}$$

The equation (1.6) reveals that the CM current is defined as the sum of currents. The CM voltage equation (1.5), the arithmetic mean of voltages, retains the arbitrary point P as a reference.

2. SYSTEM OF INTEREST

2.1 Hybrid Vehicle Drive Architecture

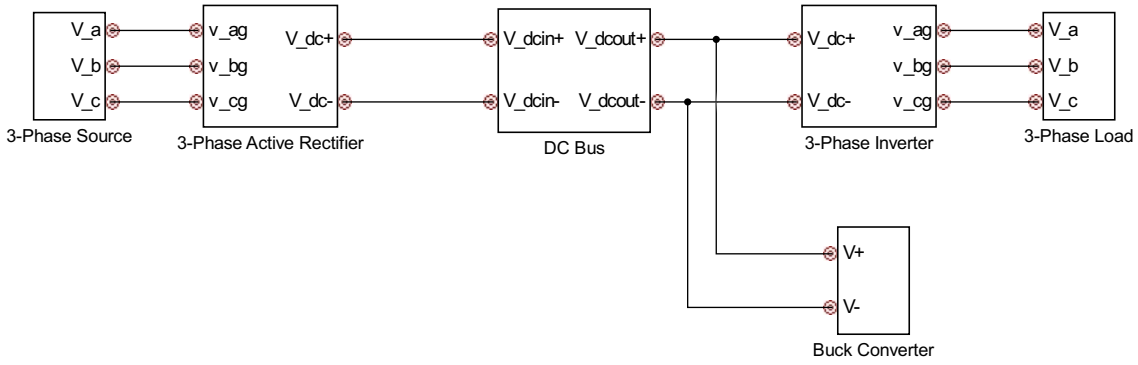


Fig. 2.1. Block Diagram of Prototypical Hybrid Vehicle Drive Architecture

The system under consideration in this research is a hybrid vehicle drive architecture intended for a heavy-duty, off-road vehicle. The primary components in the architecture are a source machine acting as a generator, a load machine acting as a motor, and a DC bus between them. There may be DC-DC converters attached to the DC bus to perform voltage conversion or provide electronic braking. Cables attach the major system components to the DC bus, and common-mode suppression devices may be introduced at various locations in the architecture. The block diagram of a prototypical system is shown in Figure 2.1.

2.2 System Components

The process of taking an existing electrical system and finding the common-mode equivalent system can be divided into four steps.

1. Add parasitic elements to each DM circuit block, including coupling paths to ground
2. Use Kirchhoff's Laws and the CM definitions to derive CM equivalent circuit blocks
3. Combine CM equivalent circuit blocks to achieve a system-level CM equivalent circuit
4. Characterize CM sources (typically voltage sources)

The dominant parasitic pathways that are added to form a DM/CM (mixed-mode or fully detailed) circuit vary from situation to situation. The recommended number varies depending on the CM problems encountered, the desired fidelity of the model, or the available bandwidth of impedance analyzers and other measurement equipment. Complicated models exist in the literature, but it may be difficult to capture their effects with an impedance analyzer or network analyzer and more difficult still to represent the results with lumped circuit elements. In this chapter, the components of the system in Figure 2.1 are analyzed and a common-mode equivalent circuit is formed.

There are two possible tripping points with the arbitrary reference point CM equivalent circuit formation. The first is that it presupposes that there is no DM-CM coupling in the circuit. Both circuit designs and circuit models should intentionally be made as symmetrically as possible. A symmetrical system will lack a DM-CM coupling that allows DM voltage to drive CM current. The second is that the circuit remains in the mode of operation used to derive the circuits. This usually means that the electronic switches in the circuit must remain in continuous mode (current greater than zero) and not go discontinuous at any point in time, which may be difficult to predict and subsequently enforce because of mixed-mode effects. While the CM equivalent circuit may be modified to support continuous and discontinuous modes, it may be difficult to identify the timing when the zero-current threshold is reached due to the superposition of DM current and CM current. When these two

conditions are met, the information in the CM equivalent circuit will be absolutely identical to the CM information in the mixed-mode model.

2.2.1 Three-phase Machine Model

Akagi Machine Model

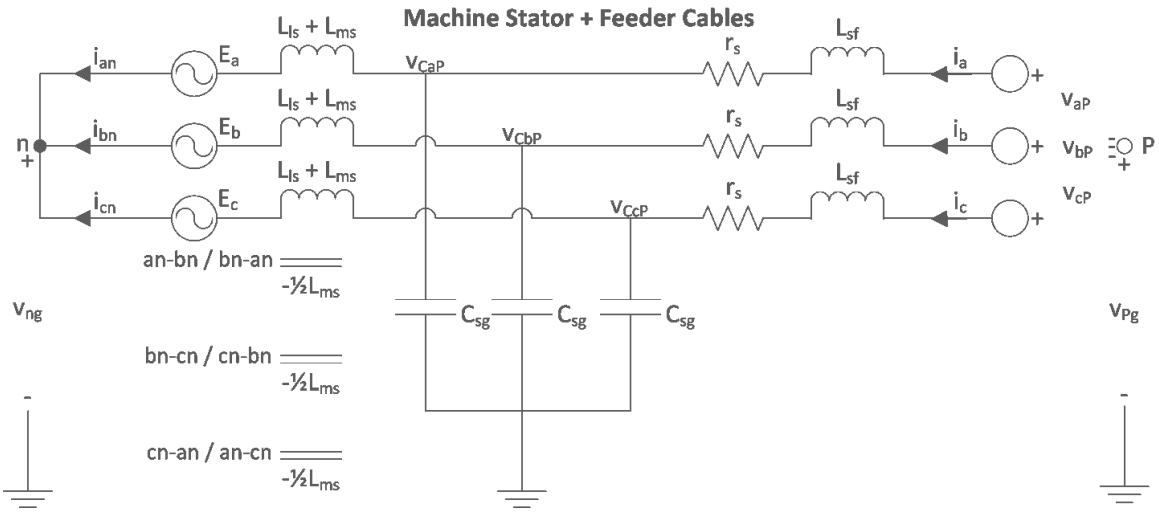


Fig. 2.2. Akagi Model of Three-phase Machine Stator and Attached Feeder Cables

Figure 2.2 shows a simple model of a three-phase machine and feeder cables developed by Hirofumi Akagi. [5] L_{sf} represents the inductance of the feeder cables. r_s is the sum of the feeder cable resistance and the machine stator resistance. $L_{ls} + L_{ms}$ represents the stator winding self-inductance, and the mutual inductance between any two phases is $-\frac{L_{ms}}{2}$. E_x, $x \in \{a, b, c\}$ represents the back-emf of the machine. This machine is assumed to be wye-connected to the neutral, denoted n with a voltage with respect to ground of V_{ng}. Three parasitic capacitances C_{sg} join the nodes between r_s and L_s in each phase to ground. These represent winding-to-stator parasitic coupling paths.

The feeder cables have terminals that are at potentials v_{aP}, v_{bP}, and v_{cP} with respect to arbitrary point P. The arbitrary point is at a potential v_{Pg} above ground. Currents i_a, i_b, and i_c are defined as positive into the cable terminals. The currents flowing through the machine phases towards the neutral are i_{an}, i_{bn}, and i_{cn}. With all of these circuit elements and quantities defined, one can start using circuit laws to start the derivation of the CM equivalent circuit.

The first set of loops are through the cable terminals through the parasitic capacitances to ground using KVL. One can express this set of loops using p as the Heaviside operator ($p = \frac{d}{dt}$):

$$\begin{aligned}
0 &= v_{Pg} + v_{aP} - L_{sf}p(i_a) - r_s(i_a) - \tfrac{1}{C_{sgp}}(i_a - i_{an}) \\
0 &= v_{Pg} + v_{bP} - L_{sf}p(i_b) - r_s(i_b) - \tfrac{1}{C_{sgp}}(i_b - i_{bn}) \\
+\,0 &= v_{Pg} + v_{cP} - L_{sf}p(i_c) - r_s(i_c) - \tfrac{1}{C_{sgp}}(i_c - i_{cn}) \\
\hline
0 &= 3v_{Pg} + v_{aP} + v_{bP} + v_{cP} - L_{sf}p(i_a + i_b + i_c) - r_s(i_a + i_b + i_c) - \tfrac{1}{C_{sgp}}(i_a + i_b + i_c - i_{an} - i_{bn} - i_{cn}) \\
0 &= 3v_{Pg} + 3v_{CM,P} - L_{sf}p(i_{CM}) - r_s(i_{CM}) - \tfrac{1}{C_{sgp}}(i_{CM} - i_{CM,n}) \\
0 &= v_{Pg} + v_{CM,P} - \tfrac{L_{sf}}{3}p(i_{CM}) - \tfrac{r_s}{3}(i_{CM}) - \tfrac{1}{3C_{sgp}}(i_{CM} - i_{CM,n})
\end{aligned} \tag{2.1}$$

The loops for each phase are added to produce the fourth line in (2.1). Using the definitions of common-mode current (1.6) and $K = 3$ lines times common-mode voltage (1.5), the simplification in the fifth line follows from the fourth. The sixth line divides the fifth line through by 3 in order to aid in the reconstruction of a circuit from this equation.

The second set of loops are through the machine neutral point through the parasitic capacitances to ground using KVL:

$$\begin{aligned}
0 &= v_{ng} + E_a + (L_{ls} + L_{ms})p(i_{an}) - \tfrac{L_{ms}}{2}p(i_{bn}) - \tfrac{L_{ms}}{2}p(i_{cn}) - \tfrac{1}{C_{sgp}}(i_a - i_{an}) \\
0 &= v_{ng} + E_b + (L_{ls} + L_{ms})p(i_{bn}) - \tfrac{L_{ms}}{2}p(i_{cn}) - \tfrac{L_{ms}}{2}p(i_{an}) - \tfrac{1}{C_{sgp}}(i_b - i_{bn}) \\
0 &= v_{ng} + E_c + (L_{ls} + L_{ms})p(i_{cn}) - \tfrac{L_{ms}}{2}p(i_{an}) - \tfrac{L_{ms}}{2}p(i_{bn}) - \tfrac{1}{C_{sgp}}(i_c - i_{cn})
\end{aligned} \tag{2.2}$$

The loops for each phase in (2.2) are summed before applying common-mode definitions and dividing by 3. $E_{CM,n} = \frac{1}{3}(E_a + E_b + E_c)$ is treated as a CM voltage source

that represents the imbalance in the machine back-emf. $L_{ms}p$ components cancel, which yields:

$$0 = v_{ng} + E_{CM,n} + \frac{L_{ls}}{3}p(i_{CM,n}) - \frac{1}{3C_{sg}p}(i_{CM} - i_{CM,n}) \tag{2.3}$$

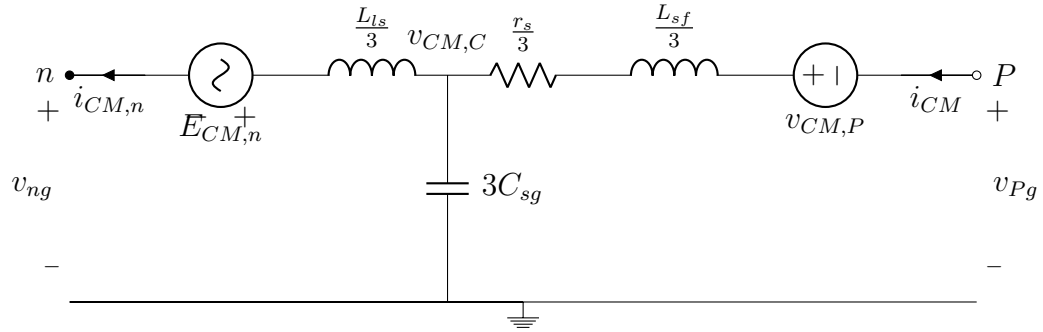


Fig. 2.3. CM Equivalent Circuit of Akagi's 3-phase Machine Stator and Feeder Cables

Taking (2.1) and (2.3), a circuit shown in Figure 2.3. $v_{CM,P}$ will be represented as an independent voltage source. Note that there is no path in the model for CM current to flow through the wye connection: [5]

$$i_{CM,n} = i_{an} + i_{bn} + i_{cn} = 0 \tag{2.4}$$

When a common-mode current is equal to zero, then that means there is an open-circuit in the CM equivalent circuit. In this case, v_{ng} represents an open-circuit voltage. The elements $E_{CM,n}$ and $\frac{L_{ls}}{3}$ have no effect in this circuit. The caution is that experimental results are needed to validate whether further parasitic elements in the stator can be neglected. If not, a more complicated model is needed.

Chen and Lipo Machine Model

Shaotang Chen and Thomas A. Lipo developed a more complicated model of a three-phase machine based on Π-models from transmission line theory. [11] Standard

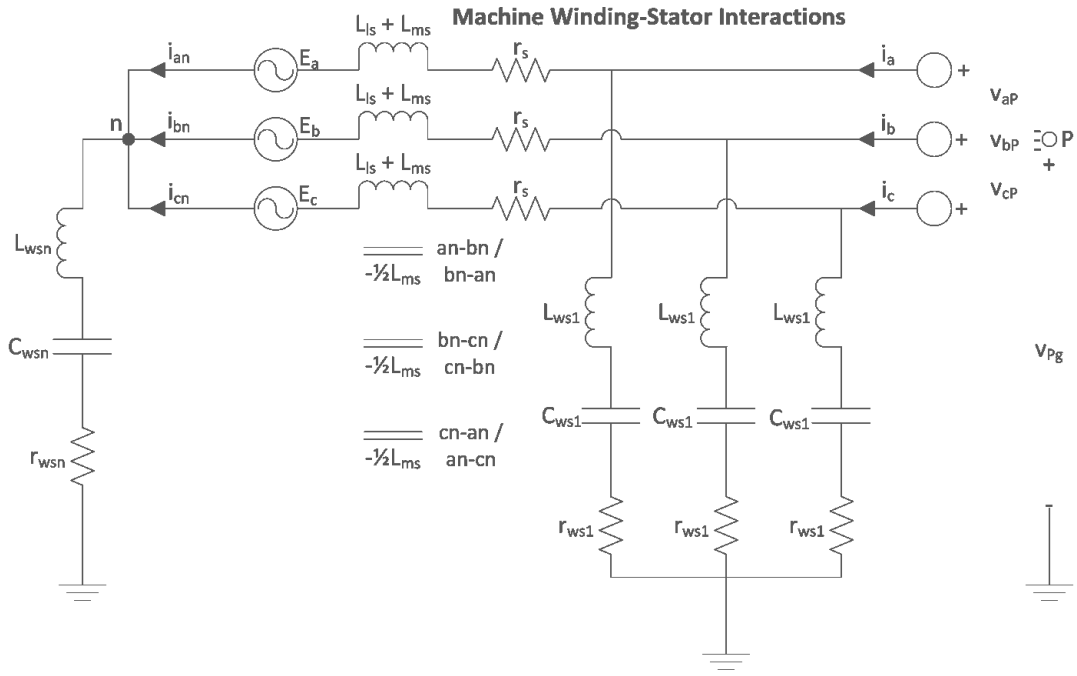


Fig. 2.4. Chen and Lipo Model of Three-phase Machine Winding-Stator Interactions

machine parameters such as winding resistance r_s, stator self-inductance $L_{ls} + L_{ms}$, stator mutual inductance $-\frac{1}{2}L_{ms}$, and back-emf E_x, $x \in \{a, b, c\}$ appear. This model is able to approximate several distributed parasitic paths rather than just a single path of the common-mode cable and terminal effects shown in the Akagi model. The feeder cables are modeled separately. One half of the circuit model represents winding-stator interactions, shown in Figure 2.4. The "ws1" subscript refers to a lumped element path to ground at the terminals of the machine. The "wsn" subscript refers to a lumped element path to ground at the neutral point of the windings. If the stator core is separated from the grounded chassis, then the capacitances to ground C_{ws1} and C_{wsn} are the effective capacitances from the windings to the stator core and from the stator core to the chassis at the machine terminals and neutral point, respectively.

The machine terminals are at potentials v_{aP}, v_{bP}, and v_{cP} from an arbitrary point P. The arbitrary point is at a potential v_{Pg} above ground. Currents i_a, i_b, and i_c are

defined positive into the cable terminals. The currents flowing through the machine phases towards the parasitically-grounded neutral are i_{an}, i_{bn}, and i_{cn}. With all of these circuit elements and quantities defined, one can start using circuit laws to start the derivation of the CM equivalent circuit.

The first set of loops are through the machine terminals through the parasitic impedances "ws1" to ground using KVL:

$$\begin{aligned}
0 &= v_{Pg} + v_{aP} - \left(L_{ws1}p + \tfrac{1}{C_{ws1}p} + r_{ws1}\right)(i_a - i_{an}) \\
0 &= v_{Pg} + v_{bP} - \left(L_{ws1}p + \tfrac{1}{C_{ws1}p} + r_{ws1}\right)(i_b - i_{bn}) \\
+\,0 &= v_{Pg} + v_{cP} - \left(L_{ws1}p + \tfrac{1}{C_{ws1}p} + r_{ws1}\right)(i_c - i_{cn}) \\
\hline
0 &= 3v_{Pg} + (v_{aP} + v_{bP} + v_{cP}) - \left(L_{ws1}p + \tfrac{1}{C_{ws1}p} + r_{ws1}\right)(i_a + i_b + i_c - i_{an} - i_{bn} - i_{cn}) \\
0 &= 3v_{Pg} + 3v_{CM,P} - \left(L_{ws1}p + \tfrac{1}{C_{ws1}p} + r_{ws1}\right)(i_{CM} - i_{CM,n}) \\
0 &= v_{Pg} + v_{CM,P} - \left(\tfrac{L_{ws1}}{3}p + \tfrac{1}{3C_{ws1}p} + \tfrac{r_{ws1}}{3}\right)(i_{CM} - i_{CM,n})
\end{aligned} \tag{2.5}$$

The loops for each phase are added together to produce the fourth line in (2.5). Using the definitions of common-mode current (1.6) and $K = 3$ lines times common-mode voltage (1.5), the simplification in the fifth line follows from the fourth. The sixth line divides the fifth line through by 3 in order to aid in the reconstruction of a circuit from this equation.

The second set of loops are through the machine terminals, through the neutral point, and through the parasitic impedances "wsn" to ground using KVL:

$$\begin{aligned}
0 &= v_{Pg} + v_{aP} - (r_s + L_{ls}p + L_{ms}p)(i_{an}) + \tfrac{L_{ms}}{2}p(i_{bn}) + \tfrac{L_{ms}}{2}p(i_{cn}) - E_a - \left(L_{wsn}p + \tfrac{1}{C_{wsn}p} + r_{wsn}\right)(i_{an} + i_{bn} + i_{cn}) \\
0 &= v_{Pg} + v_{bP} - (r_s + L_{ls}p + L_{ms}p)(i_{bn}) + \tfrac{L_{ms}}{2}p(i_{cn}) + \tfrac{L_{ms}}{2}p(i_{an}) - E_b - \left(L_{wsn}p + \tfrac{1}{C_{wsn}p} + r_{wsn}\right)(i_{an} + i_{bn} + i_{cn}) \\
0 &= v_{Pg} + v_{cP} - (r_s + L_{ls}p + L_{ms}p)(i_{cn}) + \tfrac{L_{ms}}{2}p(i_{an}) + \tfrac{L_{ms}}{2}p(i_{bn}) - E_c - \left(L_{wsn}p + \tfrac{1}{C_{wsn}p} + r_{wsn}\right)(i_{an} + i_{bn} + i_{cn})
\end{aligned} \tag{2.6}$$

The loops for each phase are added together before applying common-mode definitions and dividing by 3. $E_{CM,n} = \frac{1}{3}(E_a + E_b + E_c)$ is treated as a CM voltage source that

represents the imbalance in the machine back-emf. It is noted that the $L_{ms}p$ terms cancel, yielding:

$$0 = v_{Pg} + v_{CM,P} - \left(\frac{r_s}{3} + \frac{L_{ls}}{3}p\right)(i_{CM,n}) - E_{CM,n} - \left(L_{wsn}p + \frac{1}{C_{wsn}p} + r_{wsn}\right)(i_{CM,n}) \tag{2.7}$$

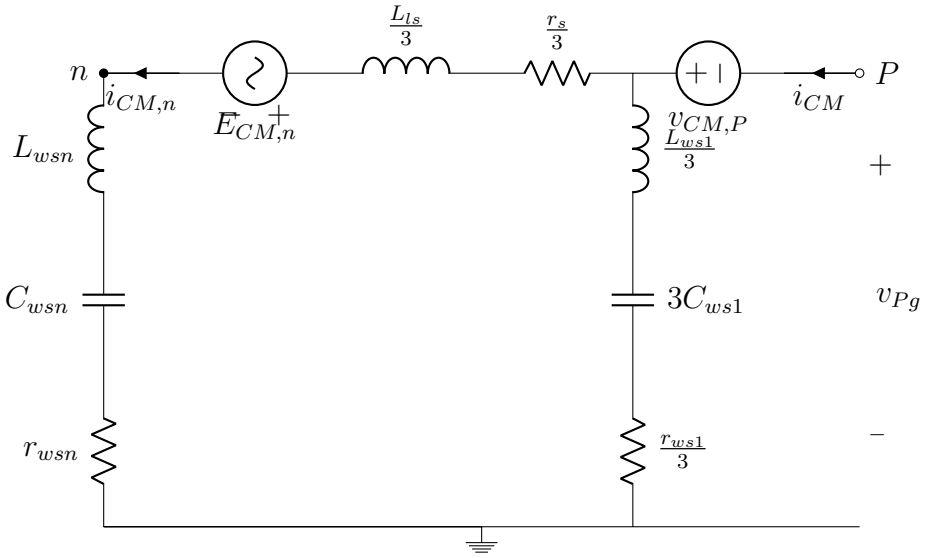


Fig. 2.5. CM Equivalent Circuit of Chen and Lipo's 3-phase Machine Winding-Stator Interactions

Taking (2.5) and (2.7), a circuit can be constructed as shown in Figure 2.5. Note that this model has a path for CM current to flow through the neutral point of the wye connection.

$$i_{CM,n} = i_{an} + i_{bn} + i_{cn} \neq 0 \tag{2.8}$$

The CM voltage source $E_{CM,n}$ (if the back-emf is unbalanced or has harmonics of the electrical rotor frequency f_r present) and stator resistance and leakage inductance have an effect on the common-mode behavior of the system.

The Shaotang Chen and Thomas A. Lipo model of a three-phase machine is only halfway complete. A winding-rotor-bearing interactions model also based on Π-models from transmission line theory needs to be added. [11] This model shares

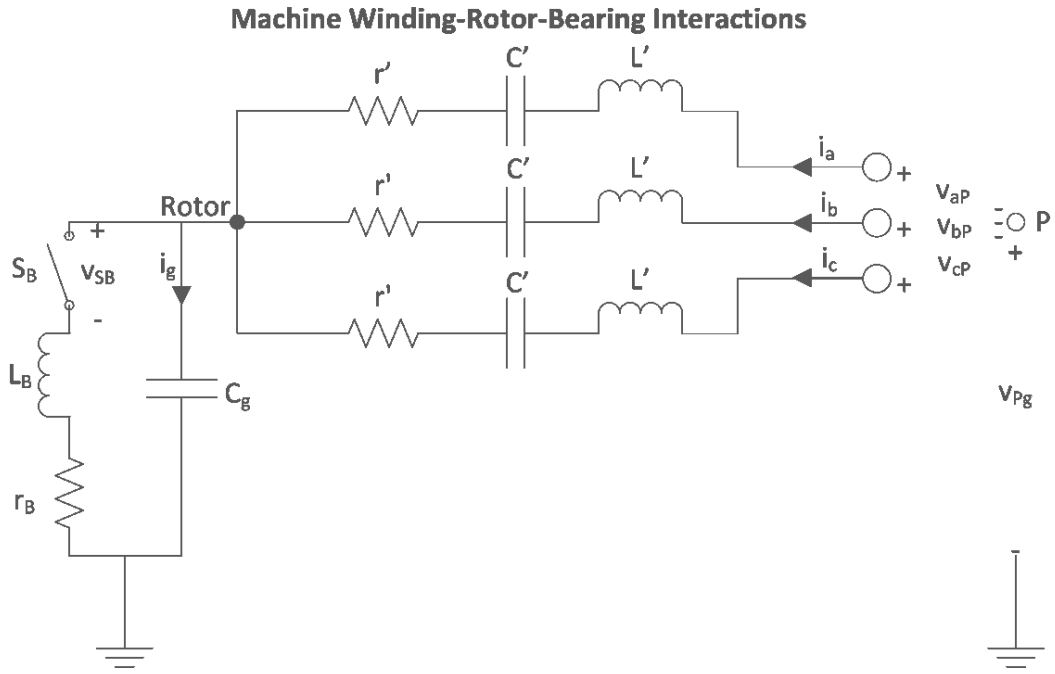


Fig. 2.6. Chen and Lipo Model of Three-phase Machine Winding-Rotor-Bearing Interactions

the same arbitrary point P and the terminal voltages v_{aP}, v_{bP}, and v_{cP} with the winding-stator model. The lumped circuit approximation may be seen in Figure 2.6. The primed impedances r', C', and L' are the result of a circuit reduction when the transmission line modeling the distributed impedance of the winding with respect to the rotor steel can be reduced to a single RLC circuit. The capacitance C_g models both the airgap capacitance between the rotor to ground (the dominant component) and the capacitance across the bearing itself (a smaller component). This capacitance has a current i_g flowing through it. The resistance r_B and inductance L_B comes from the path that current would take when the steel bearings conduct from the rotor through the inner raceway and to the grounded chassis. The switch S_B represents the stochastic behavior of the bearing which will randomly conduct based on lubrication chemistry, age, and electric potential difference. Normally, scheduled switching events are coalesced into CM voltage sources as described at the start of

Section 2.2, but the random switching behavior representing the bearing will prompt the inclusion of a discrete switch in the common-mode equivalent circuit. The net effect of this switch in the model is to discharge the airgap capacitance through the bearing resistance and inductance, corresponding to a life-draining electric discharge machining event.

The first set of loops are through the machine terminals through the primed coupling impedances to ground through the airgap capacitance using KVL:

$$\begin{aligned}
0 &= v_{Pg} + v_{aP} - \left(L'p + \tfrac{1}{C'p} + r'\right)(i_a) - \tfrac{1}{C_g p}(i_g) \\
0 &= v_{Pg} + v_{bP} - \left(L'p + \tfrac{1}{C'p} + r'\right)(i_b) - \tfrac{1}{C_g p}(i_g) \\
+\,0 &= v_{Pg} + v_{cP} - \left(L'p + \tfrac{1}{C'p} + r'\right)(i_c) - \tfrac{1}{C_g p}(i_g) \\
\hline
0 &= 3v_{Pg} + (v_{aP} + v_{bP} + v_{cP}) - \left(L'p + \tfrac{1}{C'p} + r'\right)(i_a + i_b + i_c) - \tfrac{1}{C_g p}(3i_g) \\
0 &= 3v_{Pg} + 3v_{CM,P} - \left(L'p + \tfrac{1}{C'p} + r'\right)(i_{CM}) - \tfrac{1}{C_g p}(3i_g) \\
0 &= v_{Pg} + v_{CM,P} - \left(\tfrac{L'}{3}p + \tfrac{1}{3C'p} + \tfrac{r'}{3}\right)(i_{CM}) - \tfrac{1}{C_g p}(i_g)
\end{aligned} \tag{2.9}$$

The loops for each phase are added together to produce the fourth line in (2.9). Using the definitions of common-mode current (1.6) and $K = 3$ lines times common-mode voltage (1.5), the simplification in the fifth line follows from the fourth. The sixth line divides the fifth line through by 3 in order to aid in the reconstruction of a circuit from this equation.

This set of loops is sufficient to describe operation when the bearing is not conducting. However, a single loop will concisely show how the randomly conducting bearing fits into the common-mode equivalent circuit. Let $v_{S_B} = 0$ be the voltage across the ideal switch S_B when the bearing is conducting.

$$\textit{Rotor and Bearing: } 0 = \frac{1}{C_g p}(i_g) - v_{S_B} - (L_B p + r_B)(i_{CM} - i_g) \tag{2.10}$$

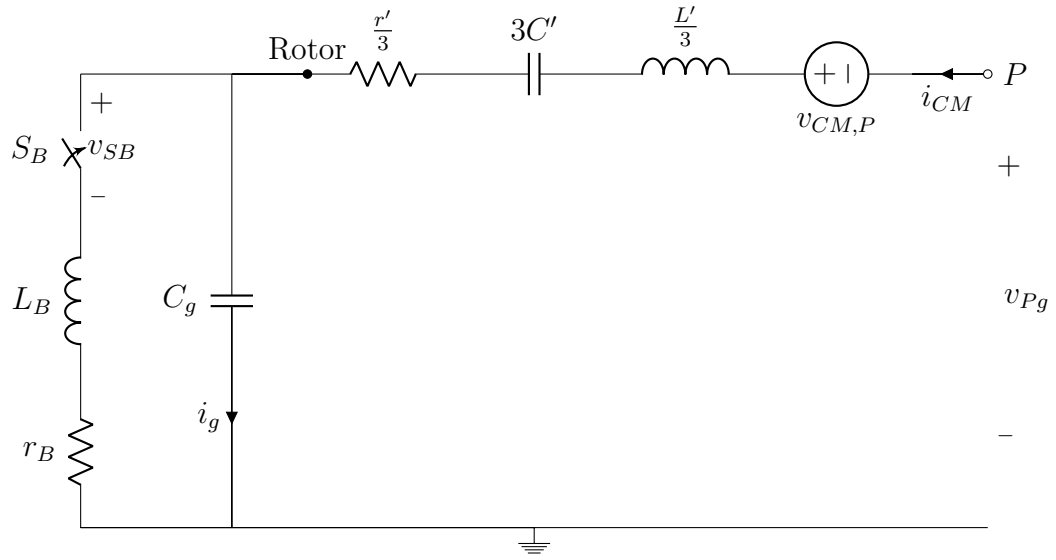


Fig. 2.7. CM Equivalent Circuit of Chen and Lipo's 3-phase Machine Winding-Rotor-Bearing Interactions

Taking (2.9) and (2.10), a circuit is constructed from those equations and is shown in Figure 2.7. Depending on how the engineer chooses to model the random conduction of the bearing, the CM equivalent circuit has one of two possible topologies.

$$\begin{cases} i_{CM} - i_g = 0, \ S_B = 0 \\ i_{CM} - i_g \neq 0, \ S_B = 1 \end{cases} \tag{2.11}$$

The motor model gains a fourth parasitic connection to ground when the bearing conducts in addition to the permanent "ws1" branch of the stator, the permanent "wsn" branch of the stator, and the permanent C_g path of the rotor.

2.2.2 Three-phase Cable Model

Short Transmission Line

The Chen and Lipo model requires an external model of the phase cables. When dealing with electrically short cables, a simple model of a three-phase transmission

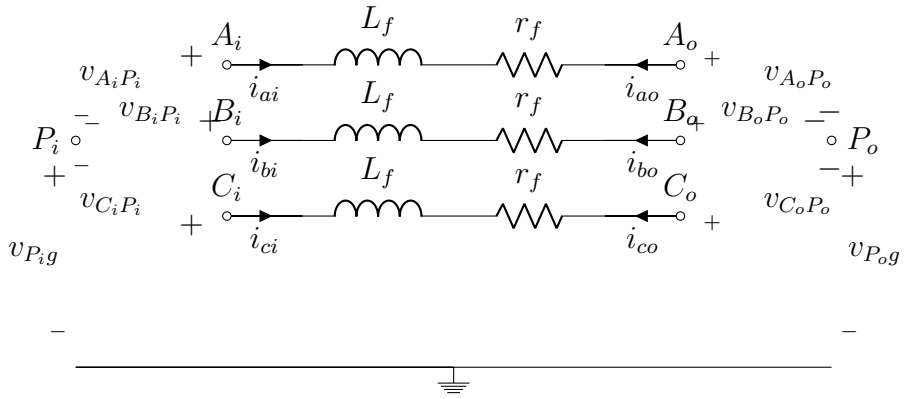


Fig. 2.8. Series Impedance Model of Three-phase Cables

line as uncoupled series impedances may be used. The circuit model is seen in Figure 2.8. Each phase cable has a resistance r_f and a self-inductance L_f. The input side refers the three terminals A_i, B_i, and C_i to the arbitrary point on the input side P_i. Currents i_{ai}, i_{bi}, and i_{ci} flow into the input terminals. The output side refers the three terminals A_o, B_o, and C_o to a different arbitrary point on the output side, P_o. Currents i_{ao}, i_{bo}, and i_{co} are defined positive into the terminals on the output side. Note that for this simple model, $i_{xi} = -i_{xo}$, $x \in \{a, b, c\}$.

A single set of loops describes this circuit block:

$$
\begin{aligned}
0 &= v_{P_ig} + v_{A_iP_i} - (L_f p + r_f)(i_{ai}) - v_{A_oP_o} - v_{P_og} \\
0 &= v_{P_ig} + v_{B_iP_i} - (L_f p + r_f)(i_{bi}) - v_{B_oP_o} - v_{P_og} \\
+\,0 &= v_{P_ig} + v_{C_iP_i} - (L_f p + r_f)(i_{ci}) - v_{C_oP_o} - v_{P_og} \\
\hline
0 &= 3v_{P_ig} + (v_{A_iP_i} + v_{B_iP_i} + v_{C_iP_i}) - (L_f p + r_f)(i_{ai} + i_{bi} + i_{ci}) - (v_{A_oP_o} + v_{B_oP_o} + v_{C_oP_o}) - 3v_{P_og} \\
0 &= 3v_{P_ig} + 3v_{CM,P_i} - (L_f p + r_f)(i_{CM,i}) - 3v_{CM,P_o} - 3v_{P_og} \\
0 &= v_{P_ig} + v_{CM,P_i} - \left(\tfrac{L_f}{3} p + \tfrac{r_f}{3}\right)(i_{CM,i}) - v_{CM,P_o} - v_{P_og}
\end{aligned}
\tag{2.12}
$$

The sum of the loops in (2.12) produces the fourth line. Simplification results by using CM voltage definitions $3v_{CM,P_i} = v_{A_iP_i} + v_{B_iP_i} + v_{C_iP_i}$ and $3v_{CM,P_o} = v_{A_oP_o} + v_{B_oP_o} + v_{C_oP_o}$ and the CM current definition $i_{CM,i} = i_{ai} + i_{bi} + i_{ci}$. Dividing the resulting

equation by 3 produces the equation of a loop that gives rise to the CM equivalent circuit.

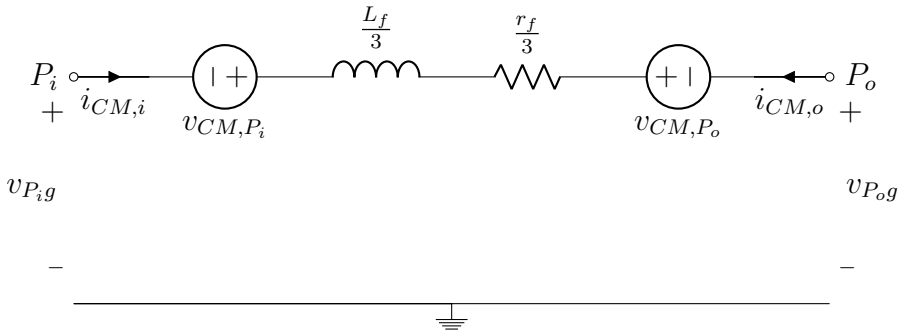


Fig. 2.9. CM Equivalent Circuit for Series Impedance Model of Three-phase Cables

The CM equivalent circuit of the cables is shown in Figure 2.9. The input reference point P_i and the output reference point P_o appear with independent voltage sources v_{CM,P_i} and v_{CM,P_o} next to them. The impedances have been cut by three, the number of wires. If shunt admittances are significant, then a medium-length cable model should be used.

Medium Transmission Line

Cables that are of a medium length electrically require a shunt admittance to be included in addition to the uncoupled series impedances. This model is seen in Figure 2.10. Each phase cable has a resistance r_f and a self-inductance L_f. There are a capacitance C_f and a conductance g_f that appear in a line-to-line (DM) fashion. Additionally, a capacitance C_g and a conductance g_g placed in a phase-to-ground fashion grow with length and must be addressed. The input side refers the three terminals A_i, B_i, and C_i to the arbitrary point on the input side P_i. Currents i_{xi} are defined positive into the input terminals. The output side refers the three terminals A_o, B_o, and C_o to a different arbitrary point on the output side, P_o. Currents i_{xo}

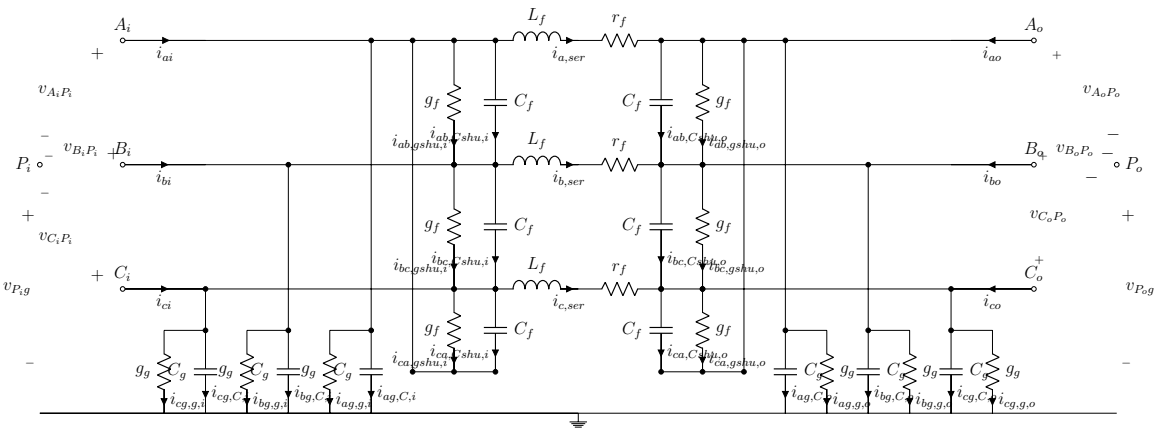


Fig. 2.10. Series Impedance and Shunt Admittance Model of Three-phase Cables

are defined positive into the terminals on the output side and are generally distinct from the current on the input side. A current $i_{x,ser}$ is defined through the lumped series elements. Let $i_{x_1x_2,yshu,z}$ represent the current in the phase-to-phase lumped elements. Let $i_{xg,y,z}$ represent the current in the phase-to-ground lumped elements. The sets are as follows: $x, x_1, x_2 \in \{a, b, c\}$, $x_1 \neq x_2$ for the phases, $y \in \{C, g\}$ for the type of admittance, and $z \in \{i, o\}$ for the side.

The first set of loops constructed is through P_i, both shunt elements to the phase behind and back, both shunt elements to the phase ahead and back, the series elements, and the output capacitances to ground:

$$\begin{aligned}
0 &= v_{P_ig} + v_{A_iP_i} - \tfrac{1}{g_f}(i_{ab,gshu,i}) + \tfrac{1}{C_fp} i_{ab,Cshu,i} + \tfrac{1}{g_f}(i_{ca,gshu,i}) - \tfrac{1}{C_fp} i_{ca,Cshu,i} - (r_f + L_fp)(i_{a,ser}) - \tfrac{1}{C_gp}(i_{ag,C,o}) \\
0 &= v_{P_ig} + v_{B_iP_i} - \tfrac{1}{g_f}(i_{bc,gshu,i}) + \tfrac{1}{C_fp} i_{bc,Cshu,i} + \tfrac{1}{g_f}(i_{ab,gshu,i}) - \tfrac{1}{C_fp} i_{ab,Cshu,i} - (r_f + L_fp)(i_{b,ser}) - \tfrac{1}{C_gp}(i_{bg,C,o}) \\
0 &= v_{P_ig} + v_{C_iP_i} - \tfrac{1}{g_f}(i_{ca,gshu,i}) + \tfrac{1}{C_fp} i_{ca,Cshu,i} + \tfrac{1}{g_f}(i_{bc,gshu,i}) - \tfrac{1}{C_fp} i_{bc,Cshu,i} - (r_f + L_fp)(i_{c,ser}) - \tfrac{1}{C_gp}(i_{cg,C,o})
\end{aligned} \tag{2.13}$$

The sum of the three loops in (2.13) begins the process of forming the loop equation for the CM equivalent circuit. Simplification results by using CM voltage definition $3v_{CM,P_i} = v_{A_iP_i} + v_{B_iP_i} + v_{C_iP_i}$ and the CM current definitions $i_{CM,ser} = i_{a,ser} + i_{b,ser} + i_{c,ser}$ and $i_{CMg,C,o} = i_{ag,C,o} + i_{bg,C,o} + i_{cg,C,o}$. Noticing the cancellation of g_f and C_f

terms and dividing the resulting equation by 3 produces the equation of a loop that helps give rise to the CM equivalent circuit:

$$0 = v_{P_ig} + v_{CM,P_i} - \left(\frac{r_f}{3} + \frac{L_f}{3}p\right)(i_{CM,ser}) - \frac{1}{3C_gp}(i_{CMg,C,o}) \tag{2.14}$$

The second set of loops constructed is through P_o, both shunt elements to the phase behind and back, both shunt elements to the phase ahead and back, the series elements, and the input capacitances to ground:

$$\begin{aligned}
0 &= v_{P_og} + v_{A_oP_o} - \tfrac{1}{g_f}(i_{ab,gshu,o}) + \tfrac{1}{C_fp}i_{ab,Cshu,o} + \tfrac{1}{g_f}(i_{ca,gshu,o}) - \tfrac{1}{C_fp}i_{ca,Cshu,o} + (r_f + L_fp)(i_{a,ser}) - \tfrac{1}{C_gp}(i_{ag,C,i}) \\
0 &= v_{P_og} + v_{B_oP_o} - \tfrac{1}{g_f}(i_{bc,gshu,o}) + \tfrac{1}{C_fp}i_{bc,Cshu,o} + \tfrac{1}{g_f}(i_{ab,gshu,o}) - \tfrac{1}{C_fp}i_{ab,Cshu,o} + (r_f + L_fp)(i_{b,ser}) - \tfrac{1}{C_gp}(i_{bg,C,i}) \\
0 &= v_{P_og} + v_{C_oP_o} - \tfrac{1}{g_f}(i_{ca,gshu,o}) + \tfrac{1}{C_fp}i_{ca,Cshu,o} + \tfrac{1}{g_f}(i_{bc,gshu,o}) - \tfrac{1}{C_fp}i_{bc,Cshu,o} + (r_f + L_fp)(i_{c,ser}) - \tfrac{1}{C_gp}(i_{cg,C,i})
\end{aligned} \tag{2.15}$$

The sum of the three loops in (2.15) is simplified by using the CM voltage definition $3v_{CM,P_o} = v_{A_oP_o} + v_{B_oP_o} + v_{C_oP_o}$ and the CM current definitions $i_{CM,ser} = i_{a,ser} + i_{b,ser} + i_{c,ser}$ and $i_{CMg,C,i} = i_{ag,C,i} + i_{bg,C,i} + i_{cg,C,i}$. Noticing the cancellation of g_f and C_f terms and dividing the resulting equation by 3 produces the equation of a loop that helps give rise to the CM equivalent circuit:

$$0 = v_{P_og} + v_{CM,P_o} + \left(\frac{r_f}{3} + \frac{L_f}{3}p\right)(i_{CM,ser}) - \frac{1}{3C_gp}(i_{CMg,C,i}) \tag{2.16}$$

A third set of loops is through the shunt conductances to ground. The loops are through g_g on the input side, the series elements, and g_g on the output side:

$$\begin{aligned}
0 = &\quad \tfrac{1}{g_g}(i_{ag,g,i}) &- &\quad (r_f + L_fp)(i_{a,ser}) &- &\quad \tfrac{1}{g_g}(i_{ag,g,o}) \\
0 = &\quad \tfrac{1}{g_g}(i_{bg,g,i}) &- &\quad (r_f + L_fp)(i_{b,ser}) &- &\quad \tfrac{1}{g_g}(i_{bg,g,o}) \\
+\,0 = &\quad \tfrac{1}{g_g}(i_{cg,g,i}) &- &\quad (r_f + L_fp)(i_{c,ser}) &- &\quad \tfrac{1}{g_g}(i_{cg,g,o}) \\
\hline
0 = &\ \tfrac{1}{g_g}(i_{ag,g,i} + i_{bg,g,i} + i_{cg,g,i}) - (r_f + L_fp)(i_{a,ser} + i_{b,ser} + i_{c,ser}) - \tfrac{1}{g_g}(i_{ag,g,o} + i_{bg,g,o} + i_{cg,g,o}) \\
0 = &\quad \tfrac{1}{g_g}(i_{CMg,g,i}) &- &\quad (r_f + L_fp)(i_{CM,ser}) &- &\quad \tfrac{1}{g_g}(i_{CMg,g,o}) \\
0 = &\quad \tfrac{1}{3g_g}(i_{CMg,g,i}) &- &\quad \left(\tfrac{r_f}{3} + \tfrac{L_f}{3}p\right)(i_{CM,ser}) &- &\quad \tfrac{1}{3g_g}(i_{CMg,g,o})
\end{aligned} \tag{2.17}$$

The general procedure in (2.17) is well established, but the simplification in the sixth line may seem unprompted. The equation in the fifth line is divided by three because (2.14) and (2.16) both use $\left(\frac{r_f}{3} + \frac{L_f}{3}p\right)$ as their impedances. For that reason, this set

of loops is used to produce an equation with the same form in order to construct the equivalent circuit from the equations.

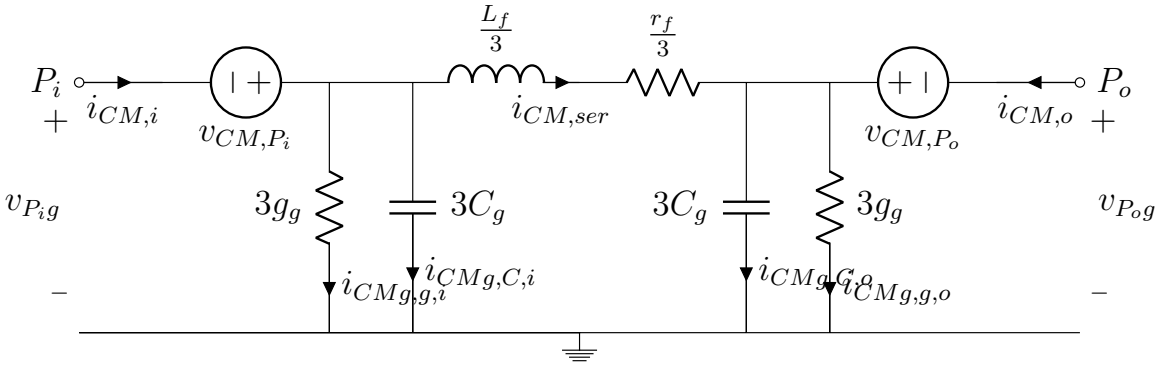


Fig. 2.11. CM Equivalent Circuit for Z_{ser} and Y_{shu} Model of Three-phase Cables

The CM equivalent circuit of the cables built from equations (2.14), (2.16), and (2.17) is shown in Figure 2.11. The input reference point P_i and the output reference point P_o appear with independent voltage sources v_{CM,P_i} and v_{CM,P_o} next to them. This three-phase transmission line model should be more accurate than the electrically short one because shunt capacitances and conductances are included in a Π configuration to ground.

For shielded cables, the capacitance and conductance will be larger than they would be for unshielded cables because ground and the conductors are physically close, thus providing a lower impedance path for CM currents to ground. The capacitance $3C_g$ represents the flow of charge between the conductors and the sheath through the cable insulation. The conductance $3g_g$ represents small losses from dielectric leakage.

2.2.3 DC Bus Model

The DC bus has a model that shares many similarities to a medium-length, single-phase transmission line as shown in Figure 2.12. The positive rail and the negative rail each have a series resistance of r_b and a series inductance of L_b that come from the

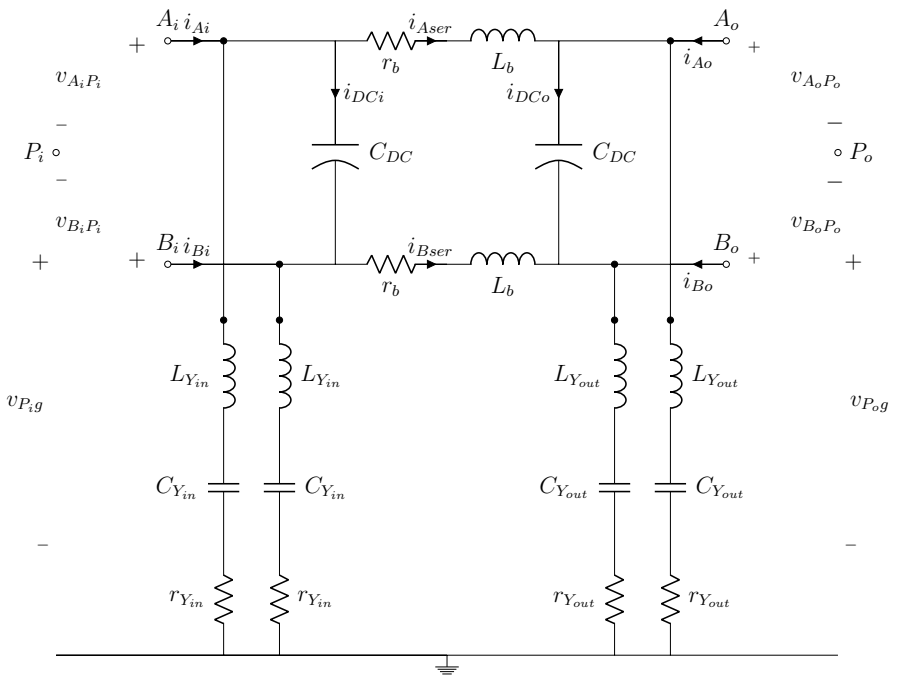


Fig. 2.12. Mixed-mode Model of DC Bus

bus bars on the supply rail and return rail. Large DC bus capacitors with capacitance C_{DC} are placed between the rails. There are Y capacitors placed on the input side (referred to arbitrary point P_i) and output side (referred to arbitrary point P_o) of the DC bus. The Y capacitors on the input side have a capacitance of $C_{Y_{in}}$, an equivalent series resistance (ESR) of $r_{Y_{in}}$, and an equivalent series inductance (ESL) of $L_{Y_{in}}$. The Y capacitors on the output side have a capacitance of $C_{Y_{out}}$, an ESR of $r_{Y_{out}}$, and an ESL of $L_{Y_{out}}$. Should Y capacitors only exist on one side of the DC bus, then set the values of the capacitance, ESR, and ESL on the other side to zero. The naming of terminal voltages and currents follows the example set forth in Subsection 2.2.2.

The first set of loops constructed are through P_i, the series elements, the output-side DC link capacitor, and the output Y capacitors, yielding:

$$\begin{aligned}
0 &= v_{P_ig} + v_{A_iP_i} - (r_b + L_b p)\,(i_{Aser}) - \tfrac{1}{C_{DC}p}(+i_{DCo}) - \left(L_{Y_{out}}p + \tfrac{1}{C_{Y_{out}}p} + r_{Y_{out}}\right)(i_{Bo} + i_{Bser} + i_{DCo}) \\
0 &= v_{P_ig} + v_{B_iP_i} - (r_b + L_b p)\,(i_{Bser}) - \tfrac{1}{C_{DC}p}(-i_{DCo}) - \left(L_{Y_{out}}p + \tfrac{1}{C_{Y_{out}}p} + r_{Y_{out}}\right)(i_{Ao} + i_{Aser} - i_{DCo})
\end{aligned} \tag{2.18}$$

For these two-wire systems, the common-mode impedances will have a divisor of 2 in (2.19)instead of 3 as they are for three-phase systems. Notice that the DC link capacitance C_{DC} between the positive rail A and the negative rail B does not appear in the common-mode equivalent circuit despite its large size and many design considerations for intended circuit operation.

$$0 = v_{P_i g} + v_{CM,P_i} - \left(\frac{r_b}{2} + \frac{L_b}{2}p\right)(i_{CM,ser}) - \left(\frac{L_{Y_{out}}}{2}p + \frac{1}{2C_{Y_{out}}p} + \frac{r_{Y_{out}}}{2}\right)(i_{CM,o} + i_{CM,ser}) \tag{2.19}$$

In order to determine the placement of the remaining DC bus model elements into the CM equivalent circuit, a second set of loops is through P_o, the series elements, the input-side DC link capacitor, and the input Y capacitors, yielding:

$$\begin{aligned} 0 &= v_{P_o g} + v_{A_o P_o} + (r_b + L_b p)(i_{Aser}) - \tfrac{1}{C_{DC}p}(+i_{DCi}) - \left(L_{Y_{in}}p + \tfrac{1}{C_{Y_{in}}p} + r_{Y_{in}}\right)(i_{Bi} - i_{Bser} + i_{DCi}) \\ 0 &= v_{P_o g} + v_{B_o P_o} + (r_b + L_b p)(i_{Bser}) - \tfrac{1}{C_{DC}p}(-i_{DCi}) - \left(L_{Y_{in}}p + \tfrac{1}{C_{Y_{in}}p} + r_{Y_{in}}\right)(i_{Ai} - i_{Aser} - i_{DCi}) \end{aligned} \tag{2.20}$$

After summing the two loops, the resulting loop equation for the CM equivalent circuit is:

$$0 = v_{P_o g} + v_{CM,P_o} + \left(\frac{r_b}{2} + \frac{L_b}{2}p\right)(i_{CM,ser}) - \left(\frac{L_{Y_{in}}}{2}p + \frac{1}{2C_{Y_{in}}p} + \frac{r_{Y_{in}}}{2}\right)(i_{CM,i} - i_{CM,ser}) \tag{2.21}$$

Taking (2.19) and (2.21), a circuit is constructed and is shown in Figure 2.13.

This example allows a set of general observations of the output of the common-mode equivalent circuit transformation.

1. Elements that appear in series from one set of terminals to another (such as bus bars or conductor quantities) affect both DM behavior ($Z_{ser} \rightarrow Z_{DM} = 2Z_{ser}$) and CM behavior ($Z_{ser} \rightarrow Z_{CM} = \frac{Z_{ser}}{K}$, where $K = 2$ lines in the example of the DC bus).

2. Elements that appear in a line-to-line configuration (X capacitors or inter-line admittances) only affect DM behavior ($Z_{DM} = Z_{\ell\ell}$) and disappear in the common mode. Even if there were ESR and ESL modeled in the DC link capacitors in Figure 2.12, the traversal of the branch in both directions when forming loops

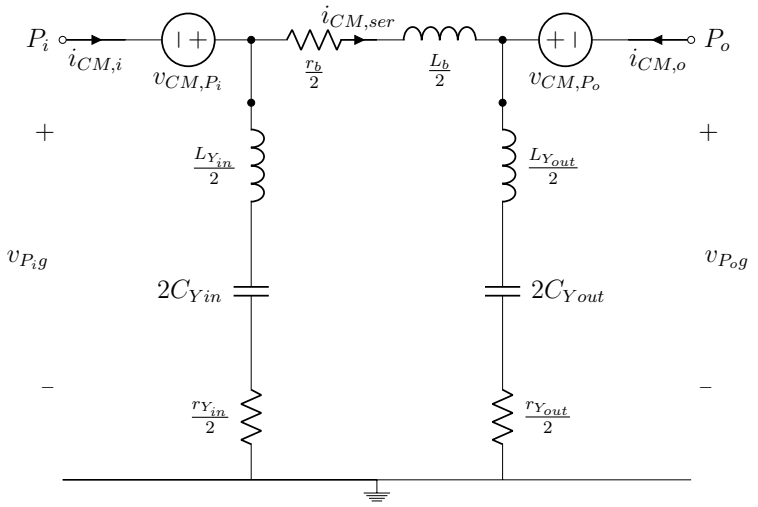


Fig. 2.13. Common-mode Equivalent Circuit of DC Bus

means that those elements disappear alongside C_{DC} for the CM equivalent circuit.

3. Elements that appear in a line-to-ground fashion (Y capacitors or parasitic impedances) affect both CM behavior ($Z_{\ell g} \rightarrow Z_{CM} = \frac{Z_{\ell g}}{K}$, where $K = 2$ lines in the example of the DC bus) and DM behavior ($Z_{\ell g} \rightarrow Z_{DM} = 2Z_{\ell g}$) despite being left out of the design for intended operation in the differential mode.

4. Elements that appear in series in the grounding path only affect CM behavior ($Z_{CM} = Z_g$) and disappear in the differential mode.

As a final observation, consider the case of a mixed-mode (DM/CM) DC bus where $L_{Y_{in}} = L_{Y_{out}} = 0$ and $r_{Y_{in}} = r_{Y_{out}} = 0$. The DM impedances of the two rails form a balanced box-topology (related to the unbalanced Π-topology) of a lumped transmission line. The CM impedances after finding the CM equivalent circuit of the mixed-mode circuit block look like a Π-topology between the arbitrary points and ground. In general, balanced circuits resembling transmission lines (e.g. DC bus bars, three-phase cables, etc.) may often be represented as transmission lines with ground using different component values when constructing their CM equivalent

circuit. Any analysis tools that work for transmission lines such as EMTP for grid electromagnetics can be adapted for analysis of these circuit blocks.

2.2.4 Active Rectifier and Inverter Model

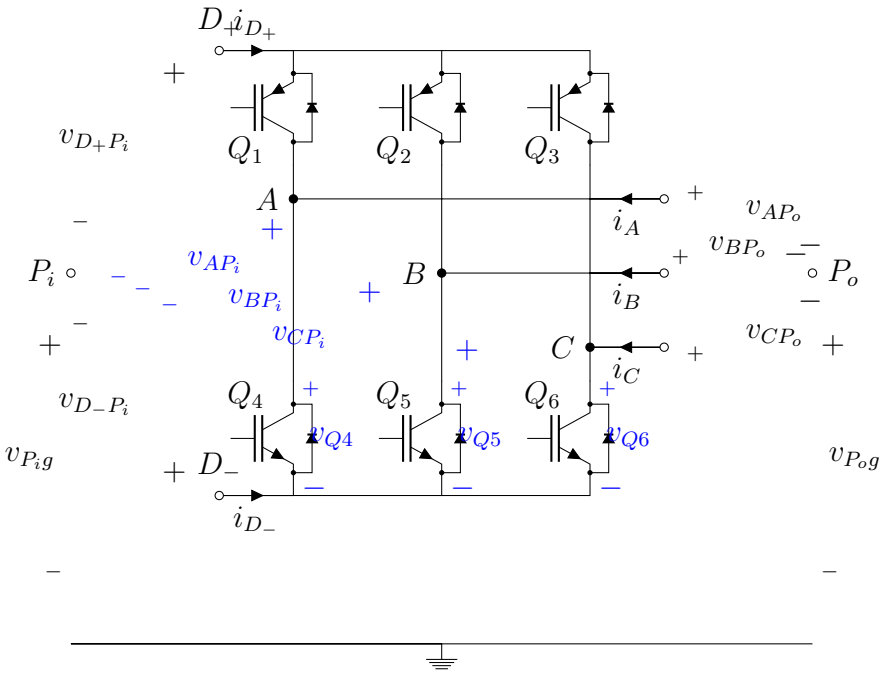


Fig. 2.14. Determining Common-mode Voltage Sources from Power Electronics

All of the attention thus far has been on circuit blocks with just linear components, but power electronics are a vital part of drive systems that need to be incorporated into the CM equivalent circuit of a drive system using the process outlined in Section 2.2. To illustrate the way that equations are made that represent the common-mode voltage sources, consider the three-phase active rectifier or three-phase inverter shown in Figure 2.14. These considerations depend on the interconnection of circuit blocks, so it is instructive to view the circuit as implemented in simulation software.

The terminals V_{d+} and V_{d-} will connect directly to the positive and negative rails, respectively, of the DC bus. The terminals connected to each of the three-phase legs will go to three-phase cables. Since the semiconductor devices will disappear from the CM equivalent circuit, there must be some way of connecting the DC bus model directly to the three-phase cable model. An unusual set of loops is used:

$$\begin{aligned}
0 &= v_{P_ig} + v_{AP_i} - v_{AP_o} - v_{P_og} \\
0 &= v_{P_ig} + v_{BP_i} - v_{BP_o} - v_{P_og} \\
+\ 0 &= v_{P_ig} + v_{CP_i} - v_{CP_o} - v_{P_og} \\
\hline
0 &= 3v_{P_ig} + (v_{AP_i} + v_{BP_i} + v_{CP_i}) - (v_{AP_o} + v_{BP_o} + v_{CP_o}) - 3v_{P_og} \\
0 &= 3v_{P_ig} + 3v_{CM,trans} - 3v_{CM,P_o} - 3v_{P_og} \\
0 &= v_{P_ig} + v_{CM,trans} - v_{CM,P_o} - v_{P_og}
\end{aligned} \tag{2.22}$$

When the direct connection is made, the arbitrary point P_i of the active rectifier must be assigned an electric potential for (2.22) to have any practical use. In this case, P_i is the same as that in the CM equivalent circuit block for the DC bus in Figure 2.13. It was chosen to be the lower rail of the DC bus to which the inverter connects ($P_i = D_-$). Thus, it follows that $v_{CM,P_i} = \frac{v_{D_+P_i} + v_{D_-P_i}}{2} = \frac{v_{D_+D_-} + v_{D_-D_-}}{2} = \frac{V_{dc}+0}{2} = \frac{V_{dc}}{2}$ (as labeled in Figure 2.14 and Figure 2.13) and $v_{CM,trans} = \frac{v_{AP_i} + v_{BP_i} + v_{CP_i}}{3} = \frac{v_{Q4} + v_{Q5} + v_{Q6}}{3}$, the common-mode voltage due to the transistor configuration, obtained using the common-mode voltage definition in (1.5). As will be explored later in Section 2.3, there is a net common-mode voltage source placed at v_{P_ig} between the blocks of value $v_{ext,rect} = v_{CM,trans} - v_{CM,P_i}$.

2.2.5 Buck Converter Model

A mixed-mode model of a buck converter is seen in Figure 2.15. There are equal inductors L_{buck} on the supply and return lines of the buck converter with magnetic axes pointing in opposite directions. A discrete capacitor with capacitance C_{out} helps

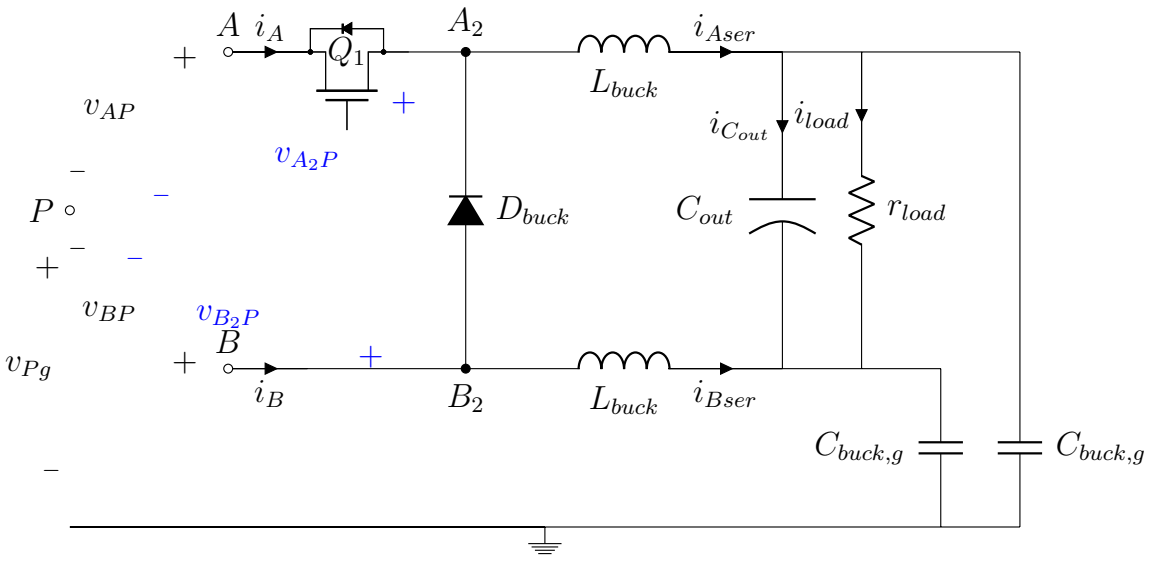


Fig. 2.15. Mixed-mode Model of Balanced Buck Converter

maintain a DC bus voltage that is less than the DC bus voltage. The buck converter services a load that is modeled as a resistance r_{load}. There are parasitic capacitances $C_{buck,g}$ that connect both the supply and return lines to ground. There is a diode D_{buck} between the lines, and a transistor Q_1 that will allow current to flow in the direction of i_A when closed. Notice that an antiparallel diode (body diode of Q_1) is needed in this model so that CM current may flow leftwards through the source line. i_A is positive for intended steady-state operation, and i_B is negative compared to the defined direction. However, current flow through both of these terminals may be in either direction when considering CM current in isolation.

Complicating issues further is how intertwined the semiconductor components are to the linear, passive components. The tricky aspect is that the arbitrary point P is going to be the reference for points A_2 and B_2 that lie further in than Q_1, the body diode, and D_{buck}. Furthermore, continuous operation of the buck converter for a transistor switching at a constant frequency f_{buck} with duty cycle d will be assumed. This assumption implies that $i_{Aser} > 0$ (strict inequality) and $i_{Bser} < 0$ in steady state operation. Should the continuous mode assumption be violated (typically

avoided in practice), then the following CM equivalent circuit derivation no longer ensures complete congruence of common-mode behavior with the mixed-mode model.

A single loop set determines the placement of all linear components:

$$\begin{aligned} 0 &= v_{Pg} + v_{A_2P} - L_{buck}p(i_{Aser}) - \tfrac{1}{C_{outp}}(+i_{C_{out}}) - r_{load}(-i_{load}) - \tfrac{1}{C_{buck,gp}}(i_{Aser} - i_{C_{out}} - i_{load}) \\ 0 &= v_{Pg} + v_{B_2P} - L_{buck}p(i_{Bser}) - \tfrac{1}{C_{outp}}(-i_{C_{out}}) - r_{load}(+i_{load}) - \tfrac{1}{C_{buck,gp}}(i_{Bser} + i_{C_{out}} + i_{load}) \end{aligned} \tag{2.23}$$

L_{buck} is a discrete component that affects the both DM behavior and CM behavior; therefore, there should be additional design considerations when choosing that inductor. Neither the output capacitor nor the amount of load affects the CM behavior:

$$0 = v_{Pg} + v_{CM,P} - \frac{L_{buck}}{2}p(i_{CM,ser}) - \frac{1}{2C_{buck,g}p}(i_{CM,ser}) \tag{2.24}$$

An additional step is needed to characterize the common-mode voltage source $v_{CM,P}$ given the power electronics contained within the circuit block. Terminals A and B connect directly to the positive and negative rails of the DC bus, respectively, with a voltage of V_{dc} between them. Note that points B and B_2 always have the same potential because there is no semiconductor device in between them. Let S_1 denote the status of the transistor as though it were an ideal switch, with $S_1 = 0$ corresponding to switch being off and $S_1 = 1$ corresponding to the switch being on. When the switch is on, then the current i_A forces points A and A_2 to the same potential. When the switch is off, then it is assumed that the inductors force the current to recirculate through the load, causing D_{buck} to conduct and force points B_2 and A_2 to the same potential. The following equation describes the common-mode voltage source with frequency f_{buck} and duty cycle d and arbitrary point P chosen to be the negative rail of the DC bus:

$$v_{CM,P} = \frac{v_{A_2P} + v_{B_2P}}{2} = \frac{v_{A_2B} + v_{B_2B}}{2} \text{ (choice) } = \begin{cases} \frac{V_{dc}+0}{2},\ S_1 = 1 \\ \frac{0+0}{2},\ S_1 = 0 \end{cases} = \begin{cases} \frac{V_{dc}}{2},\ S_1 = 1 \\ 0,\ S_1 = 0 \end{cases} \tag{2.25}$$

Taking (2.23) and (2.25), a CM equivalent circuit is constructed from those equations and takes the form in Figure 2.16. Because common-mode current can flow

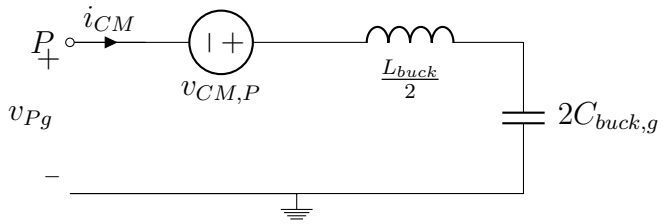


Fig. 2.16. Common-mode Equivalent Circuit of Balanced Buck Converter

rightwards (through Q_1) or leftwards (through D_1), i_{CM} is the same as $i_{CM,ser}$. Note that the CM equivalent circuit is just a driven LC resonator. Unless the ESR of the inductors is a significant consideration to merit inclusion, there is no resistance in this branch to ground to damp out CM currents with time. Furthermore, the relatively large value of L_{buck} compared to the parasitic inductances of an electric drive system will mean that the common-mode resonance associated with the buck converter branch will occur at a lower frequency than most other paths.

2.2.6 Electronic Brake Model

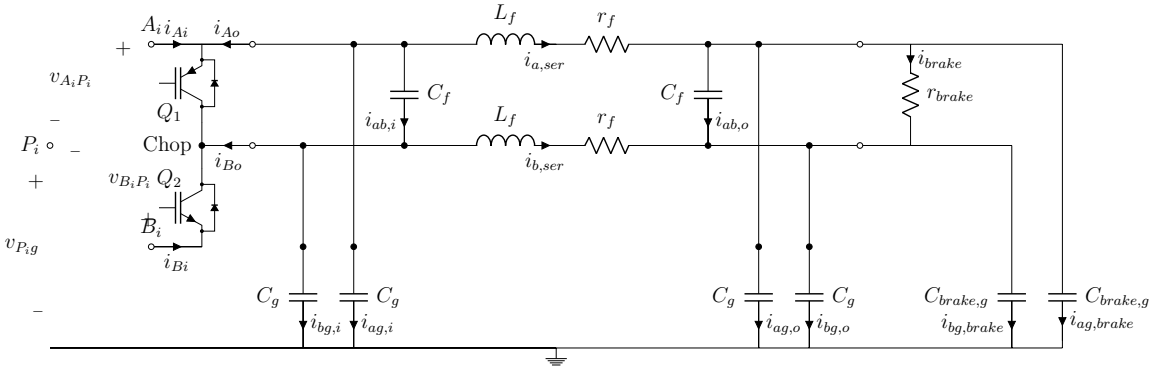


Fig. 2.17. Electronic Brake Model Consisting of Brake Chopper, Single-phase Cable, and Brake Resistor

Brake Chopper

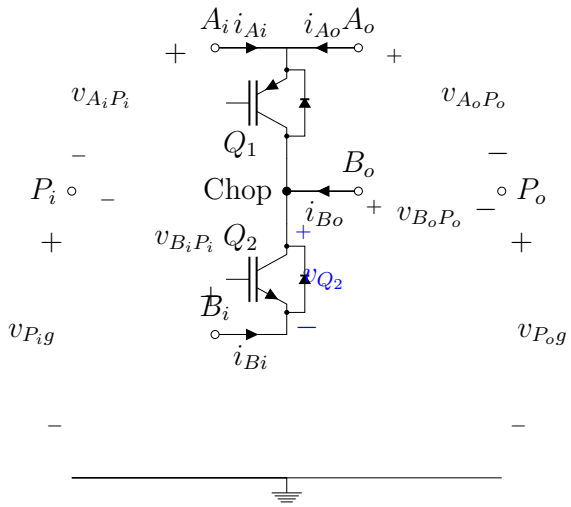


Fig. 2.18. Voltage Determination from Mixed-mode Model of a Brake Chopper

The power electronics of the electronic brake as shown in Figure 2.17 are simply a two-quadrant chopper attached to the DC bus. The mixed-mode model seen in Figure 2.18 will lead to common-mode voltage sources. The terminals A_i and B_i will be connected to the positive and negative rails, respectively, of a DC bus. The chopped DC output terminals A_o and B_o will connect to a brake resistor. The handling of the power electronics uses a similar loop set as the inverter or active rectifier module of Subsection 2.2.4:

$$\begin{aligned}
0 &= v_{P_ig} + v_{A_oP_i} - v_{A_oP_o} - v_{P_og} \\
+\ 0 &= v_{P_ig} + v_{B_oP_i} - v_{B_oP_o} - v_{P_og} \\
\hline
0 &= 2v_{P_ig} + (v_{A_oP_i} + v_{B_oP_i}) - (v_{A_oP_o} + v_{B_oP_o}) - 2v_{P_og} \\
0 &= 2v_{P_ig} + 2v_{CM,trans} - 2v_{CM,P_o} - 2v_{P_og} \\
0 &= v_{P_ig} + v_{CM,trans} - v_{CM,P_o} - v_{P_og}
\end{aligned} \tag{2.26}$$

The arbitrary point P_i of the brake chopper must be fixed in order to determine $v_{CM,trans}$, the common-mode voltage due to the pair of transistors, in (2.26).

It was chosen that P_i should be the lower rail of the DC bus to which B_i also connects. Thus, it follows that $v_{CM,P_i} = \frac{v_{A_iP_i}+v_{B_iP_i}}{2} = \frac{v_{A_iB_i}+v_{B_iB_i}}{2} = \frac{V_{dc}+0}{2} = \frac{V_{dc}}{2}$ and $v_{CM,trans} = \frac{v_{A_oP_i}+v_{B_oP_i}}{2} = \frac{v_{A_oB_i}+v_{B_oB_i}}{2} = \frac{V_{dc}+v_{Q_2}}{2}$, obtained using the common-mode voltage definition in (1.5). In the upcoming Section 2.3, the net common-mode voltage placed at v_{P_ig} between the DC bus block and brake chopper blocks will be $v_{ext,brake} = v_{CM,trans} - v_{CM,P_i} = \frac{v_{Q_2}}{2}$.

Single-phase Cables

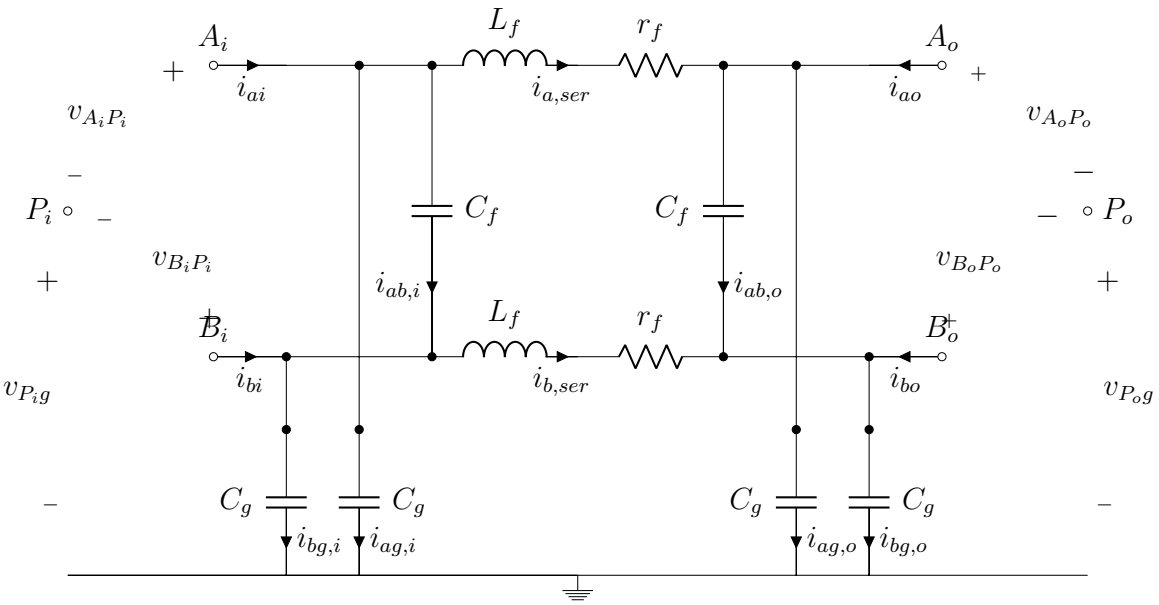


Fig. 2.19. Series Impedance and Shunt Capacitance Model of Single-phase Cables

The electronic brake model includes a medium-length pair of cables. The model of a single-phase transmission line contains uncoupled series impedances and shunt capacitances (shunt conductances are neglected) as seen in Figure 2.19. Each phase cable has a resistance r_f and a self-inductance L_f. A capacitance C_f appears in a line-to-line (DM) fashion, and a capacitance C_g appears in a phase-to-ground fashion. The DC chopper input side refers the two terminals A_i and B_i to the arbitrary point on

the input side P_i. Currents i_{ai} and i_{bi} are defined positive into the input terminals. The output side refers the two terminals A_o and B_o to a different arbitrary point on the output side, P_o. Currents i_{ao} and i_{bo} are defined positive into the terminals on the output side. Currents $i_{a,ser}$ and $i_{b,ser}$ are defined through the lumped series elements. $i_{ab,i}$ and $i_{ab,o}$ represent the currents in the phase-to-phase capacitors. Let $i_{xg,z}$ represent the current in the phase-to-ground lumped elements with $x \in \{a, b, c\}$ for the phases and $z \in \{i, o\}$ for the side.

The first set of loops constructed is through P_i, the input shunt capacitor, the series elements, and the output capacitances to ground:

$$\begin{aligned} 0 &= v_{P_ig} + v_{A_iP_i} - \tfrac{1}{C_fp}(+i_{ab,i}) - (r_f + L_fp)(i_{b,ser}) - \tfrac{1}{C_gp}(i_{bg,o}) \\ 0 &= v_{P_ig} + v_{B_iP_i} - \tfrac{1}{C_fp}(-i_{ab,i}) - (r_f + L_fp)(i_{a,ser}) - \tfrac{1}{C_gp}(i_{ag,o}) \end{aligned} \tag{2.27}$$

The sum of the two loops in (2.27) begins the process of forming the loop equation for the CM equivalent circuit. Simplification results by using CM voltage definition $2v_{CM,P_i} = v_{A_iP_i} + v_{B_iP_i}$ and the CM current definitions $i_{CM,ser} = i_{a,ser} + i_{b,ser}$ and $i_{CMg,o} = i_{ag,o} + i_{bg,o}$. Noticing the cancellation of C_f terms and dividing the resulting equation by 2 produces the equation of a loop that helps give rise to the CM equivalent circuit:

$$0 = v_{P_ig} + v_{CM,P_i} - \left(\frac{r_f}{2} + \frac{L_f}{2}p\right)(i_{CM,ser}) - \frac{1}{2C_gp}(i_{CMg,C,o}) \tag{2.28}$$

The second set of loops constructed is through P_o, the output shunt capacitor, the series elements, and the input capacitances to ground:

$$\begin{aligned} 0 &= v_{P_og} + v_{A_oP_o} - \tfrac{1}{C_fp}(+i_{ab,o}) + (r_f + L_fp)(i_{b,ser}) - \tfrac{1}{C_gp}(i_{bg,i}) \\ 0 &= v_{P_og} + v_{B_oP_o} - \tfrac{1}{C_fp}(-i_{ab,o}) + (r_f + L_fp)(i_{a,ser}) - \tfrac{1}{C_gp}(i_{ag,i}) \end{aligned} \tag{2.29}$$

The sum of the two loops in (2.29) is simplified by using the CM voltage definition $2v_{CM,P_o} = v_{A_oP_o} + v_{B_oP_o}$ and the CM current definitions $i_{CM,ser} = i_{a,ser} + i_{b,ser}$ and $i_{CMg,i} = i_{ag,i} + i_{bg,i}$. Noticing the cancellation of C_f terms and dividing the resulting

equation by 2 produces the equation of a loop that helps give rise to the CM equivalent circuit:

$$0 = v_{P_o g} + v_{CM,P_o} + \left(\frac{r_f}{2} + \frac{L_f}{2}p\right)(i_{CM,ser}) - \frac{1}{2C_g p}(i_{CMg,C,i}) \tag{2.30}$$

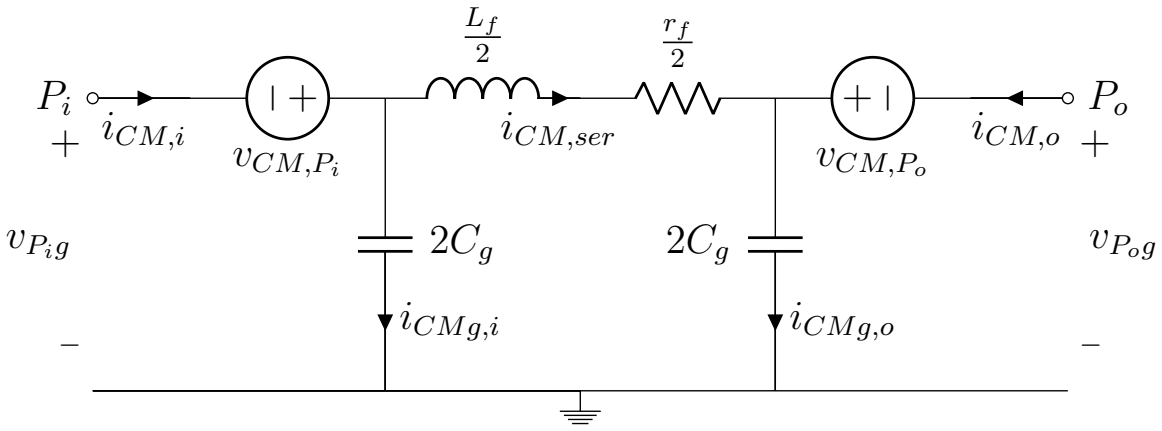


Fig. 2.20. CM Equivalent Circuit for Z_{ser} and C_g Model of Single-phase Cables

The CM equivalent circuit of the single-phase cables shown in Figure 2.20 is built from (2.28) and (2.30). The input reference point P_i and the output reference point P_o appear with independent voltage sources v_{CM,P_i} and v_{CM,P_o} next to them. The impedances have been divided by two, the number of wires.

Brake Resistor

The electronic brake model is shown in Figure 2.21. It simply consists of a large resistor of resistance r_{brake} connected line-to-line with parasitic capacitances $C_{brake,g}$

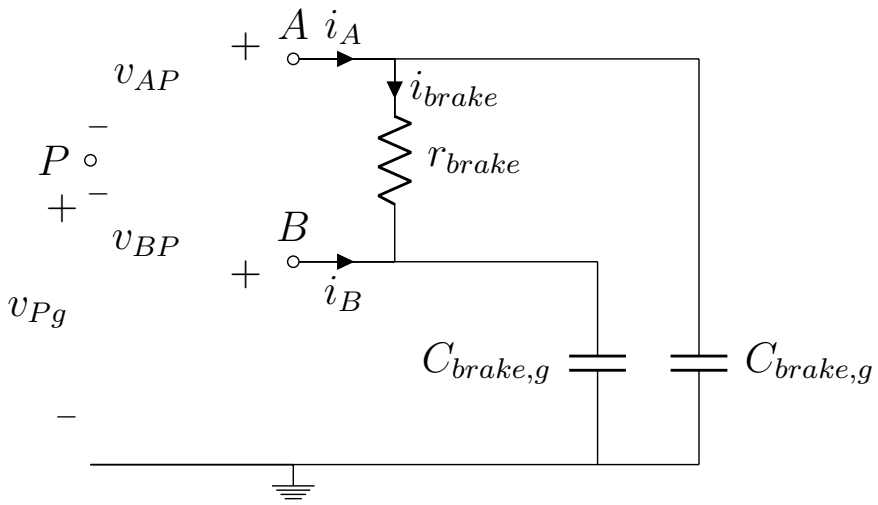


Fig. 2.21. Mixed-mode Model of a Brake Resistor

associated with each line. A pair of loops determines the CM equivalent circuit, yielding:

$$\begin{aligned}
0 &= v_{Pg} + v_{AP} - r_{brake}(+i_{brake}) - \tfrac{1}{C_{brake,g}p}(i_B + i_{brake}) \\
+\,0 &= v_{Pg} + v_{BP} - r_{brake}(-i_{brake}) - \tfrac{1}{C_{brake,g}p}(i_A - i_{brake}) \\
\hline
0 &= 2v_{Pg} + (v_{AP} + v_{BP}) - 0 - \tfrac{1}{C_{brake,g}p}(i_A + i_B) \\
0 &= 2v_{Pg} + 2v_{CM,P} - 0 - \tfrac{1}{C_{brake,g}p}(i_{CM}) \\
0 &= v_{Pg} + v_{CM,P} - 0 - \tfrac{1}{2C_{brake,g}p}(i_{CM})
\end{aligned} \tag{2.31}$$

A simple circuit can be readily constructed from (2.31) as depicted in Figure 2.22 with the arbitrary point P as a terminal. $v_{CM,P}$ is an independent voltage source that connects the brake resistor block to the rest of the system.

2.3 Circuit Block Interconnection

With so many circuit blocks available for interconnection, the engineer may be eager to connect them together in a system. Care must be taken when following this third step outlined in Section 2.2. To that end, a very simple DC source model will

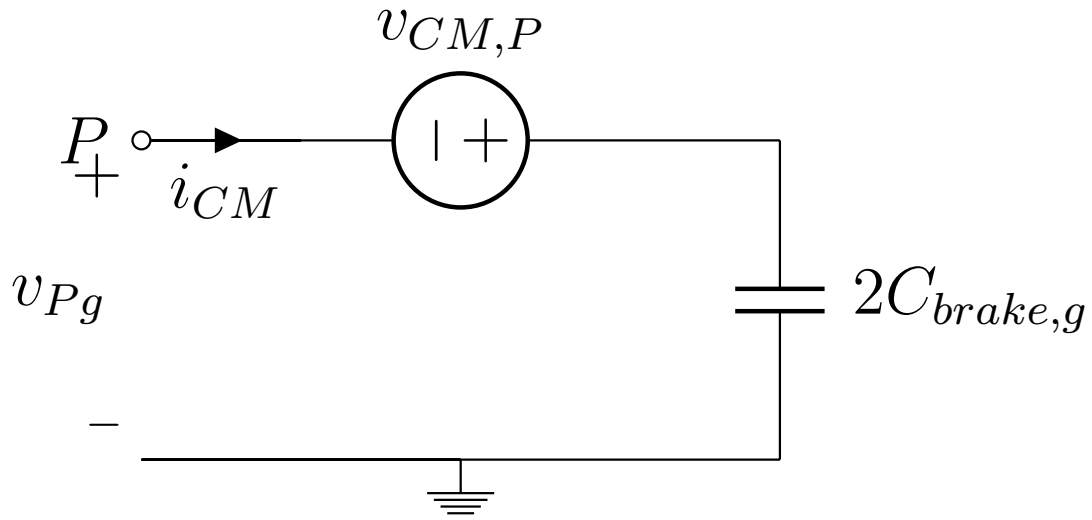
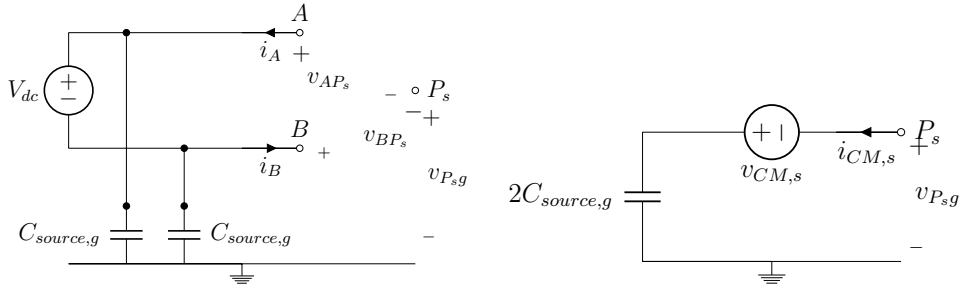


Fig. 2.22. Common-mode Equivalent Circuit of a Brake Resistor

be introduced to illustrate a common-mode equivalent circuit of a DC-DC conversion system.



(a) Mixed-mode Model of Simple DC Source

(b) CM Equivalent Model of Simple DC Source

Fig. 2.23. Common-mode Equivalent Circuit Transformation for Simple DC Source

The DC source model shown in Figure 2.23 would basically be a stripped-down, single-port version of the DC bus shown in Figures 2.12 and 2.13 with most components set to zero. There is an ideal differential-mode voltage source of V_{dc} with

current i_{dc} flowing from the positive terminal down to the negative terminal of the voltage source. There is some parasitic connection that this DC power supply has with ground, shown here as capacitors of capacitance $C_{source,g}$ between the positive rail and ground as well as the negative rail and ground.

The CM equivalent circuit should be able to be formed by inspection; however, the set of loop equations supporting the transformation are shown below. Note the polarity of the CM voltage source arises by convention.

$$\begin{aligned}
0 &= v_{P_sg} + v_{AP_s} + -V_{dc} - \tfrac{1}{C_{source,g}p}(i_B + i_{dc}) \\
+\,0 &= v_{P_sg} + v_{BP_s} + +V_{dc} - \tfrac{1}{C_{source,g}p}(i_A - i_{dc}) \\
\hline
0 &= 2v_{P_sg} + (v_{AP_s} + v_{BP_s}) + 0 - \tfrac{1}{C_{source,g}p}(i_A + i_B) \\
0 &= 2v_{P_sg} + 2v_{CM,s} + 0 - \tfrac{1}{C_{source,g}p}(i_{CM}) \\
0 &= v_{P_sg} + v_{CM,s} + 0 - \tfrac{1}{2C_{source,g}p}(i_{CM})
\end{aligned} \tag{2.32}$$

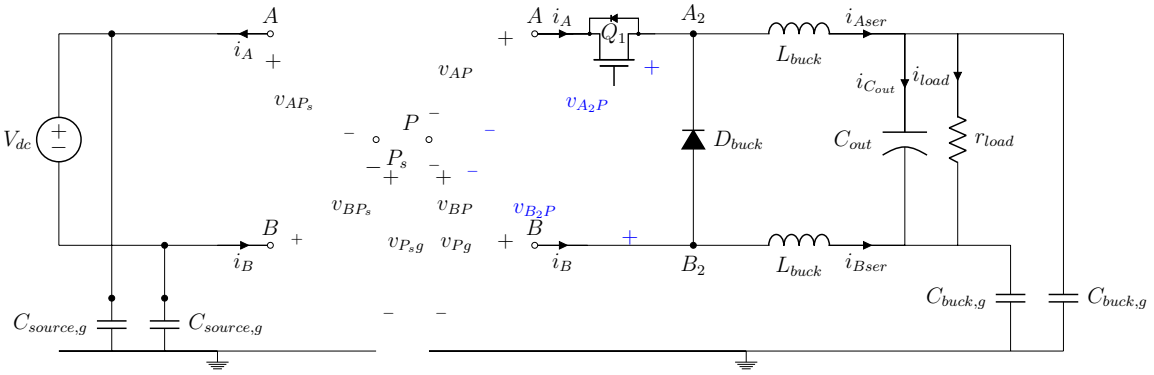


Fig. 2.24. Mixed-mode Model of DC Source Feeding a Balanced Buck Converter

Figure 2.24 shows a mixed-mode model of a DC power supply connected to a buck converter with a resistive load r_{load}. The interconnection of the blocks should be straightforward since there are only two terminals. The ground plane is assumed to be an equipotential surface regardless of the physical distance between the two circuit blocks.

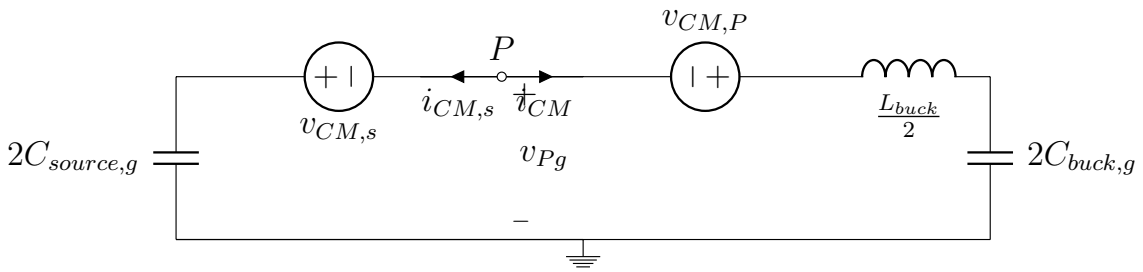


Fig. 2.25. CM Equivalent Circuit of DC Source Block and Buck Converter Block

The common-mode equivalent circuits of the two blocks may be connected together as shown in Figure 2.25. The only question would concern what to do with the arbitrary points P and P_s. They need to be assigned to a fixed potential within the system. A sensible choice is lower rail of the DC bus, just like was done for (2.25). Once this choice is made, an equation may be written to give a known potential difference for $V_{CM,s}$.

$$v_{CM,s} = \frac{v_{AP_s} + v_{BP_s}}{2} = \frac{v_{AB} + v_{BB}}{2} \text{ (choice) } = \frac{V_{dc} + 0}{2} = \frac{V_{dc}}{2} \tag{2.33}$$

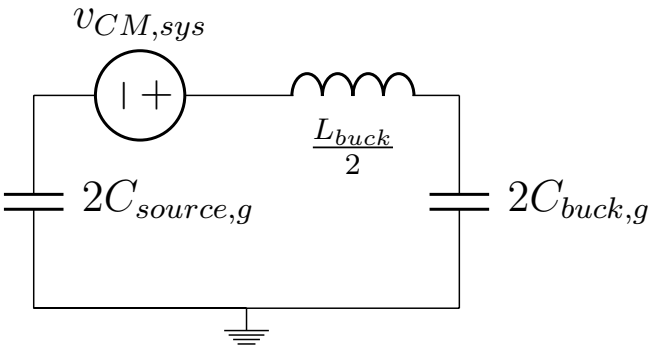


Fig. 2.26. CM Equivalent Circuit of DC-DC Converter System

While the simple CM equivalent circuit of the system could be solved as is, there are some improvements that could be made for better simulation performance. Such improvements will become more important as the number of branches in the circuit

increases and the states representing reactive elements become more numerous. The first change would be to replace the two CM voltage sources in series with a single voltage source. The resulting voltage source must face one direction or another, so it was decided to pick a right-facing source arbitrarily by subtracting (2.33) from (2.25).

$$v_{CM,sys} = v_{CM,P} - v_{CM,s} = \begin{cases} \frac{V_{dc}}{2}, & S_1 = 1 \\ 0, & S_1 = 0 \end{cases} \quad - \frac{V_{dc}}{2} = \begin{cases} 0, & S_1 = 1 \\ -\frac{V_{dc}}{2}, & S_1 = 0 \end{cases} \tag{2.34}$$

The result will be the CM equivalent circuit of the system shown in Figure 2.26. The second change that could be considered would be to combine the capacitors in series. It may be instructive to see and probe components in different connected subsystem blocks separately, but an unnecessary state can be removed by making the circuit simplification. The common-mode current will not die down when the CM voltage source is in the $1 - d$ duration because no damping has been introduced in the form of a common-mode resistance. The circuit will resonate with a frequency of $\omega = \frac{1}{\sqrt{L_{equiv}C_{equiv}}} = \left[\frac{1}{2}L_{buck} \times \left(\frac{1}{2C_{buck,g}} + \frac{1}{2C_{source,g}}\right)^{-1}\right]^{-\frac{1}{2}} = \left[L_{buck} \times \left(\frac{1}{C_{buck,g}} + \frac{1}{C_{source,g}}\right)^{-1}\right]^{-\frac{1}{2}}$.

After the system has been formed, linear circuit analysis techniques can be used to predict the common-mode response for simple excitations as shown for the buck converter and DC source system. The connection of circuit blocks of linear components will cancel out the CM voltage sources between them, drastically reducing the number of excitations to manage. However, many times the switching patterns may be complicated due to dead time and the DC bus voltage used for making the CM voltage sources may have oscillations on it. In that case, the characterization of common-mode voltage sources in a mixed-mode (DM/CM) environment will have to take place first. This can be obtained with laboratory measurements or by simulation of the DM/CM system. This usually means that characterization of CM voltage sources is the last step in the process in Section 2.2.

Analytic voltage sources can be placed in the simulation, or data import can be used to make arbitrary CM voltage sources to drive the common-mode impedances in

the circuit. Time-domain simulation software may be used to obtain CM current in various loops in response to those simulated or measured CM voltages. From there, potential electromagnetic compatibility issues may be identified and potential electric machine damage may be predicted. Potential CM current mitigation steps include changing grounding schemes to alter parasitic values and branches to ground, inserting components like Y capacitors and common-mode chokes in problematic areas, and altering the switching so as to modify the voltage waveforms.

3. COMPARISON OF MODELS

3.1 Source-fed Inverter and Brake Chopper

3.1.1 Mixed-mode Model

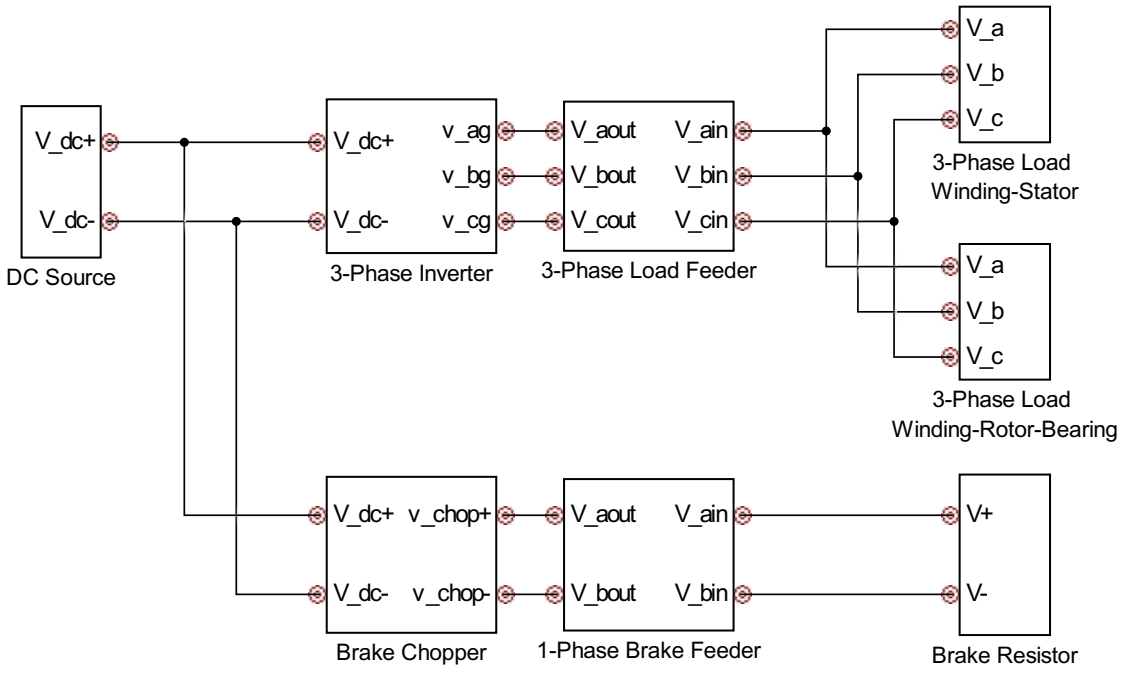


Fig. 3.1. Top-level Mixed-mode Model in ASMG

A mixed-mode model of a simplified DC source-fed inverter and brake chopper system was built using MATLAB and the ASMG for Simulink® Toolbox from PCKA. The top-level blocks may be seen in Figure 3.1. The "3-Phase Load" blocks correspond to the three-phase Chen and Lipo machine model in Subsection 2.2.1. The "3-Phase Load Feeder" block corresponds to the short transmission line model in Subsection 2.2.2. The "DC Source" block corresponds to the model explored in Section 2.3. The

"3-Phase Inverter" block corresponds to the model in Subsection 2.2.4. The "Brake Chopper", "1-Phase Brake Feeder", and "Brake Resistor" blocks correspond to the model presented in Subsection 2.2.6.

3.1.2 Common-mode Equivalent Circuit Model

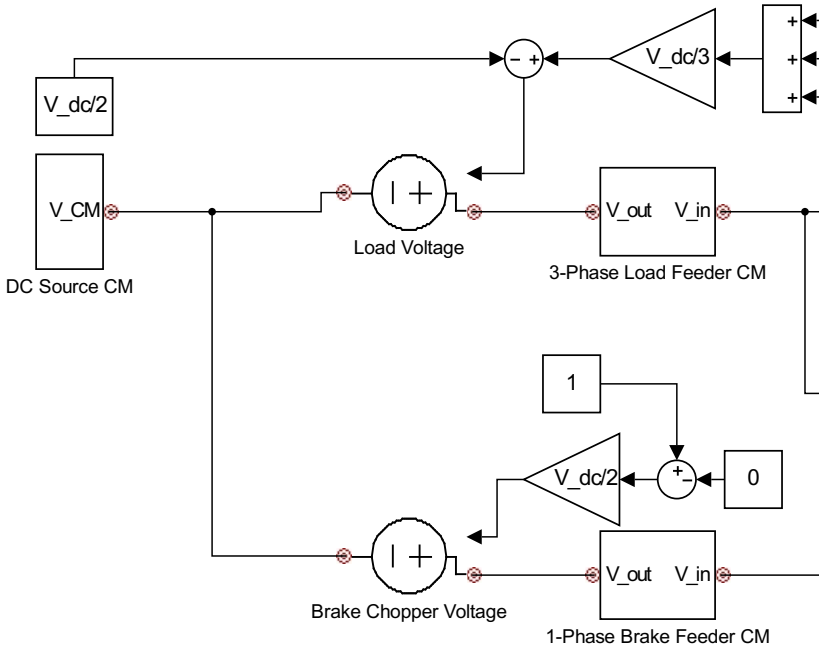
A common-mode equivalent model of the simplified DC source-fed inverter and brake chopper system was built using MATLAB and the ASMG for Simulink® Toolbox from PCKA. The correspondence of blocks seen in Figure 3.2 to component models matches that of the mixed-mode model presented before. Following the example of Section 2.3, only the nontrivial CM voltage sources are left in the model. Namely, the voltage sources left are "Load Voltage" and "Brake Chopper Voltage" after combination of circuit blocks. These voltage sources are characterized assuming a fixed DC bus voltage of V_{dc} and the commanded switching signals.

3.1.3 Findings from Simulation

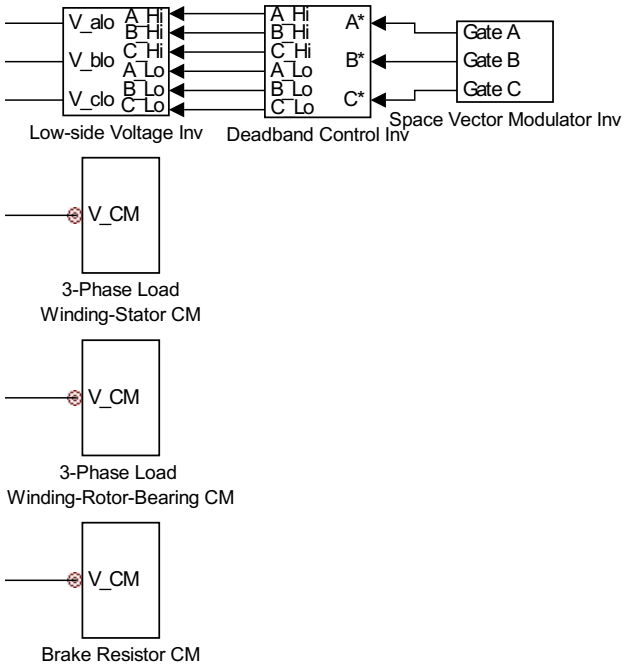
The mixed-mode and common-mode equivalent simulations used the variable-step solver *ode23t (moderately stiff – trapezoidal rule)*. The simulation time started at 0 and ran until $t_{stop} = 0.02\,\text{s}$. The load machine has an electrical frequency of $f_{e\ell} = 400\,\text{Hz}$ and commanded torque of $T^*_{e\ell} = 300\,\text{Nm}$. The DC source voltage is $V_{dc} = 1050\,\text{V}$. The inverter has a switching frequency of $f_{inv} = 4000\,\text{Hz}$. The brake chopper is not switching at all.

Run-time Performance

The simulations were executed on a Windows 7 workstation with an Intel® Core™i7 3.60 GHz processor, 16 GB of RAM, and integrated graphics. The DM/CM simulation completed in 1h, 40 min, 50 s. The CM simulation completed in 31 min, 56 s.



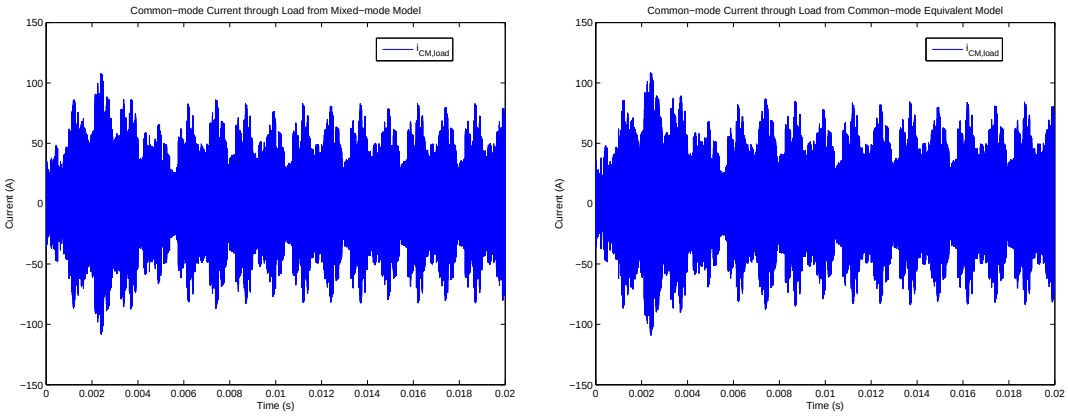
(a) Left Side



(b) Right Side

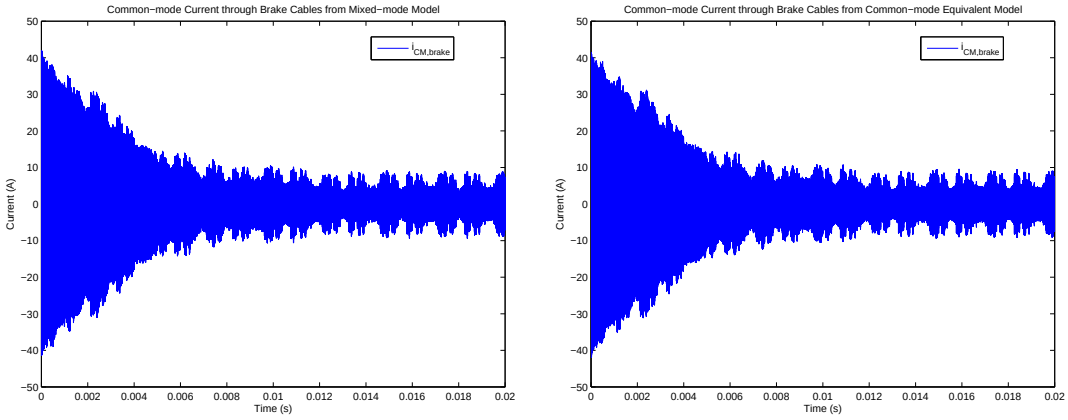
Fig. 3.2. Top-level Common-mode Equivalent Model in ASMG

Predicted Common-mode Current Magnitude



(a) Mixed-mode Model Results (b) Common-mode Equivalent Results

Fig. 3.3. Load Machine CM Current of System without Rectifier



(a) Mixed-mode Model Results (b) Common-mode Equivalent Results

Fig. 3.4. Brake Cables CM Current of System without Rectifier

Both the DM/CM and CM models are able to produce waveforms for the CM current as shown in Figure 3.3 for the load machine and Figure 3.4 for the brake cables. Though the waveforms should be identical from the mathematical definitions written

in Section 1.2, differences between the two simulations are attributed to numerical effects. Indeed, the RMS CM current through the load machine was 26.157 A_{rms} according to the DM/CM simulation and 26.703 A_{rms} according to the CM simulation. This corresponds to a 2.09% error. The RMS CM current through the brake cables was 3.080 A_{rms} according to the DM/CM simulation and 3.167 A_{rms} according to the CM simulation, a 2.82% error.

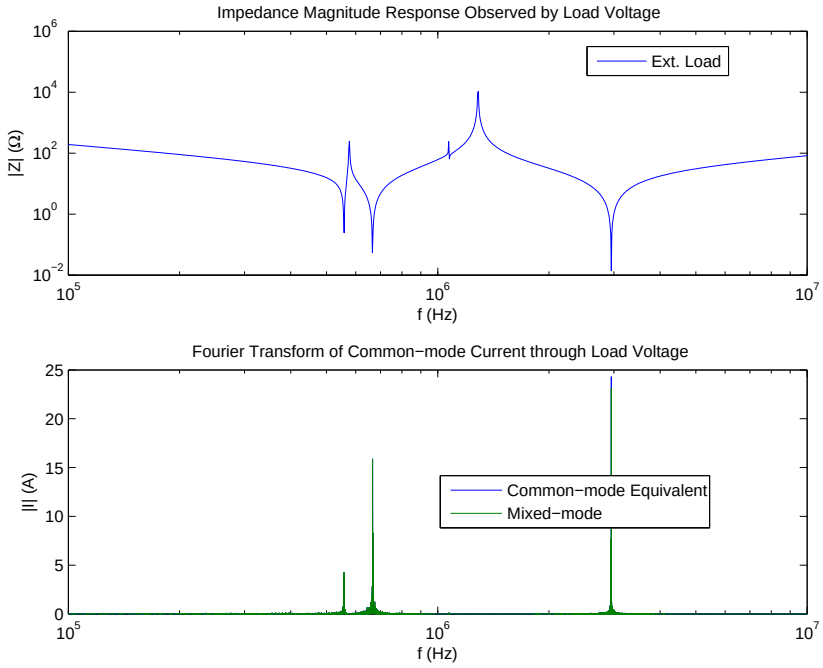


Fig. 3.5. CM Load Current in Frequency Domain for System without Rectifier

The data from the CM equivalent circuit can be brought into the frequency domain for the load machine in Figure 3.5 and for the brake cables in Figure 3.5. By comparing the impedance magnitude response to the Fourier transform of the currents, it is readily apparent that CM current appears strongly at the locations of the resonances seen by the CM source.

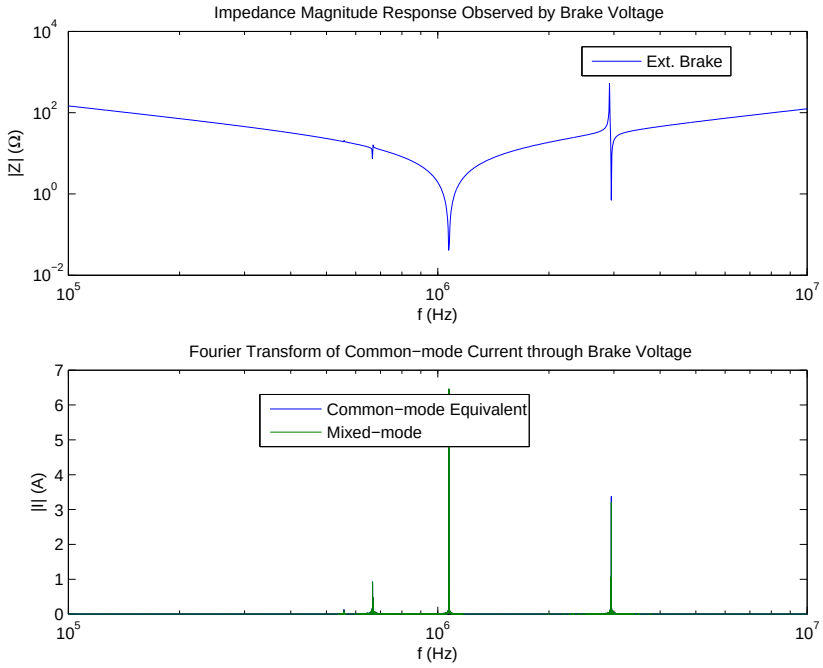
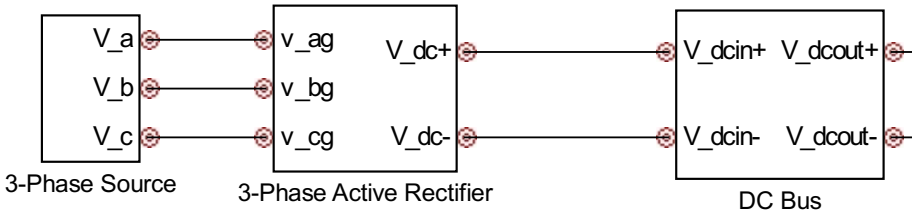


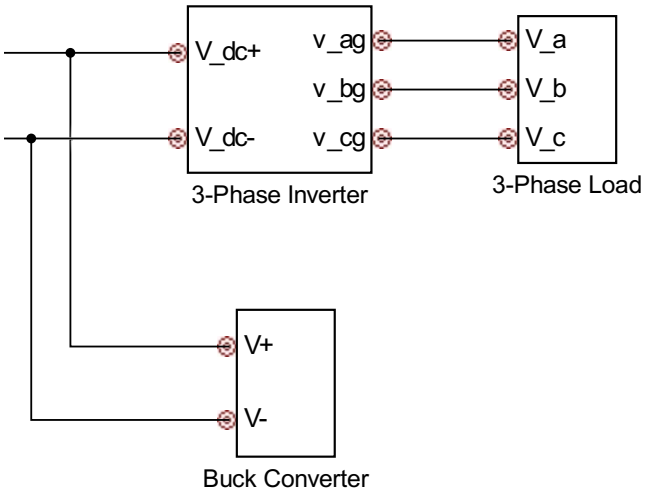
Fig. 3.6. CM Brake Current in Frequency Domain for System without Rectifier

3.2 Hybrid Drive Architecture

3.2.1 Mixed-mode Model



(a) Left Side



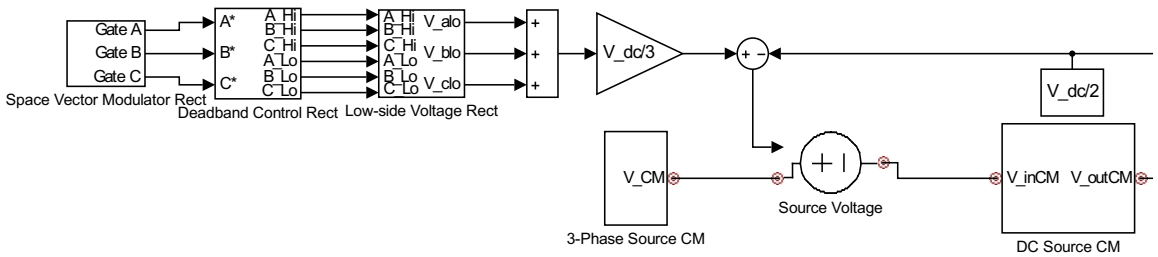
(b) Right Side

Fig. 3.7. Top-level Mixed-mode Model in ASMG

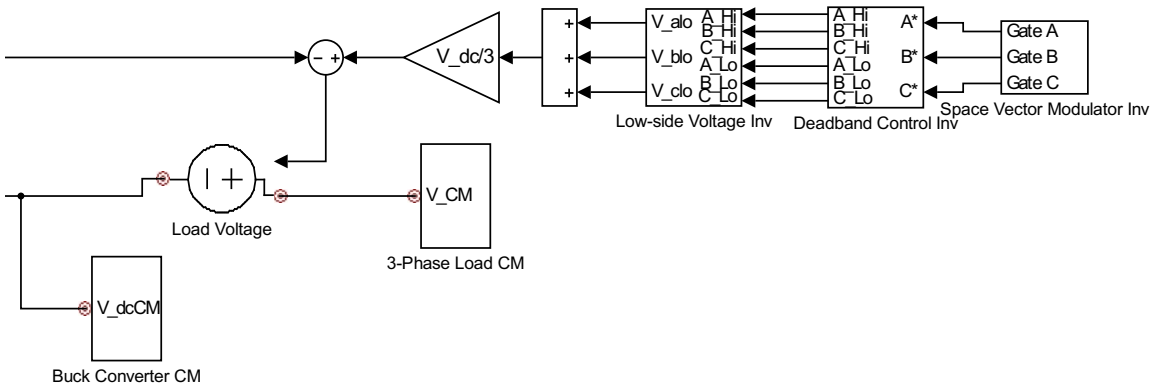
A mixed-mode model of the hybrid vehicle drive was built using MATLAB and the ASMG for Simulink® Toolbox from PCKA. The top-level blocks may be seen in

Figure 3.7. The "3-Phase Source" and "3-Phase Load" blocks correspond to the three-phase Akagi machine model in Subsection 2.2.1. The "DC Bus" block corresponds to the model in Subsection 2.2.3 with Y capacitors used on both the input side and the output side. The "3-Phase Active Rectifier" and "3-Phase Inverter" blocks correspond to the models in Subsection 2.2.4. The "Buck Converter" block corresponds to the model presented in Subsection 2.2.5.

3.2.2 Common-mode Equivalent Circuit Model



(a) Left Side



(b) Right Side

Fig. 3.8. Top-level Common-mode Equivalent Model in ASMG

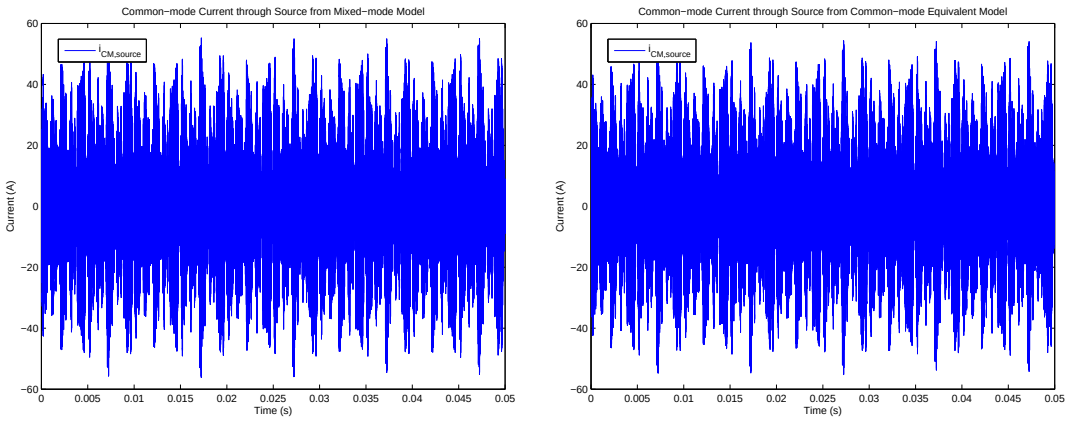
A common-mode equivalent model of the hybrid vehicle drive was built using MATLAB and the ASMG for Simulink® Toolbox from PCKA. The correspondence of blocks seen in Figure 3.8 to component models matches that of the mixed-mode model presented before. Following the example of Section 2.3, only the nontrivial CM voltage sources are left in the model. Namely, the voltage sources left are "Source Voltage", "Load Voltage", and "Buck Converter Voltage" as the voltage source depicted in Figure 2.16 after combination of circuit blocks. These voltage sources are characterized assuming a fixed DC bus voltage of V_{dc}, ignoring any effects of control or voltage drop from one side to another, and the commanded switching signals.

3.2.3 Findings from Simulation

The mixed-mode and common-mode equivalent simulations used the variable-step solver *ode113 (Adams)*. The simulation time started at 0 and ran until $t_{stop} = 0.05\,\text{s}$. The source machine has an electrical frequency of $f_{es} = 500\,\text{Hz}$ and commanded torque of $T^*_{es} = -318\,\text{Nm}$. The load machine has an electrical frequency of $f_{e\ell} = 400\,\text{Hz}$ and commanded torque of $T^*_{e\ell} = 300\,\text{Nm}$. The DC bus voltage is $V_{dc} = 1050\,\text{V}$. The active rectifier has a switching frequency of $f_{rect} = 5000\,\text{Hz}$, and the inverter has a switching frequency of $f_{inv} = 4000\,\text{Hz}$. The buck converter has a frequency of $f_{buck} = 1000\,\text{Hz}$, commanded output voltage of $V^*_{out} = 750\,\text{V}$, and commanded output voltage ripple of $\Delta V^*_{out} = 7.5\,\text{V}$.

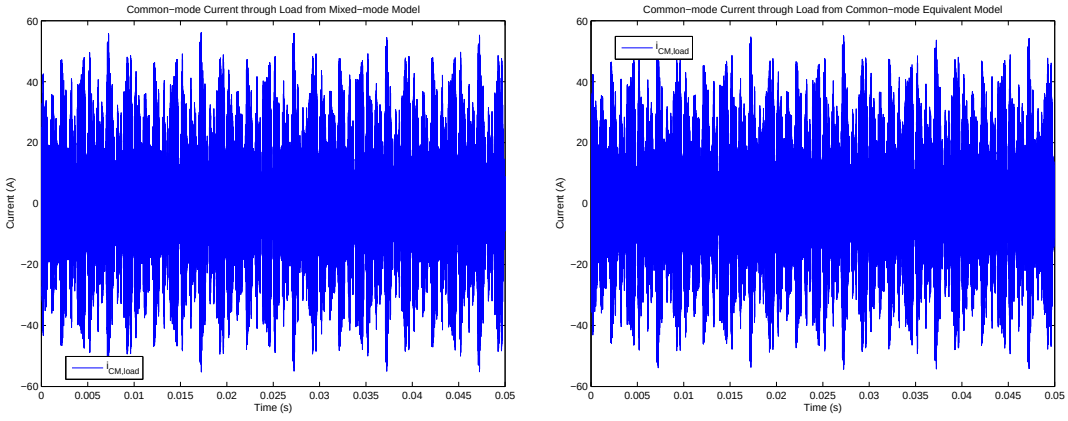
Run-time Performance

The simulations were executed on a Windows 7 workstation with an Intel® Core™i7 3.60 GHz processor, 16 GB of RAM, and integrated graphics. The DM/CM simulation completed in 10 min, 16 s. The CM simulation completed in 4 min, 30 s.



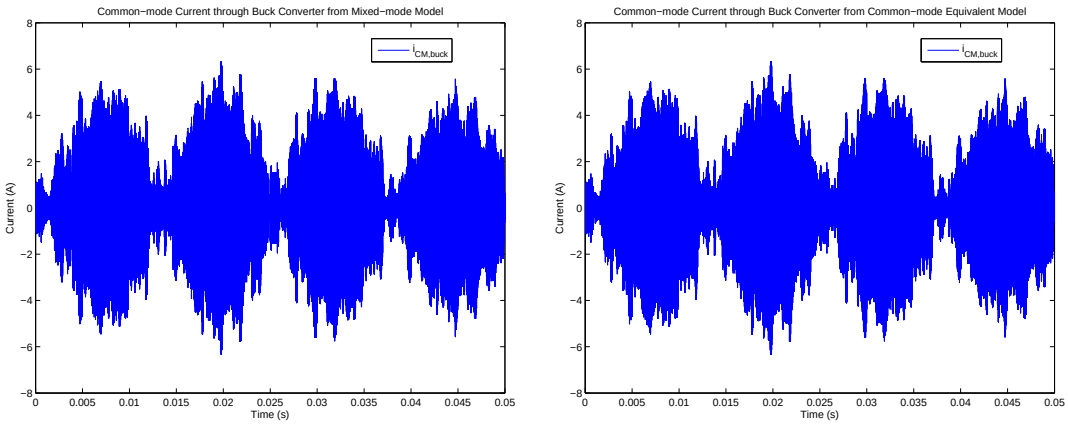
(a) Mixed-mode Model Results (b) Common-mode Equivalent Results

Fig. 3.9. Source Machine Common-mode Current of Drive System



(a) Mixed-mode Model Results (b) Common-mode Equivalent Results

Fig. 3.10. Load Machine Common-mode Current of Drive System



(a) Mixed-mode Model Results (b) Common-mode Equivalent Results

Fig. 3.11. Buck Converter Common-mode Current of Drive System

Predicted Common-mode Current Magnitude

Both the DM/CM and CM models are able to produce waveforms for the CM current as shown in Figure 3.9 for the source machine, Figure 3.10 for the load machine, and Figure 3.11 for the buck converter. Though the waveforms should be identical from the mathematical definitions written in Section 1.2, differences between the two simulations are attributed to numerical effects. Indeed, the RMS CM current through the source machine was $17.2\,\mathrm{A_{rms}}$ according to the FD simulation and $16.9\,\mathrm{A_{rms}}$ according to the CM simulation. This corresponds to a 2% error. Both simulations agree on the RMS CM current through the buck converter as being $2.3\,\mathrm{A_{rms}}$.

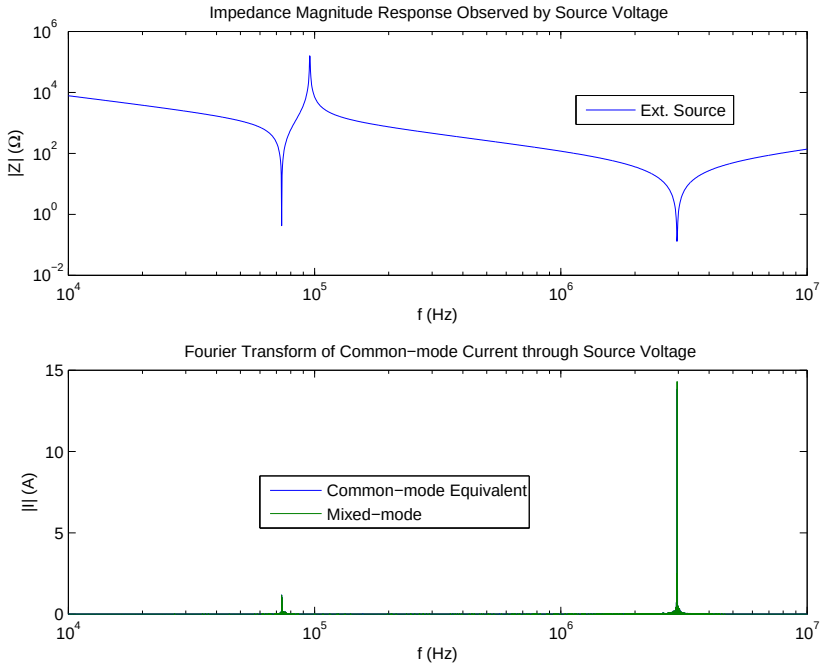


Fig. 3.12. CM Source Current in Frequency Domain for Drive System

The data from the CM equivalent circuit can be brought into the frequency domain for the source machine in Figure 3.12, for the load machine in Figure 3.13, and for the brake cables in Figure 3.13. By comparing the impedance magnitude response to

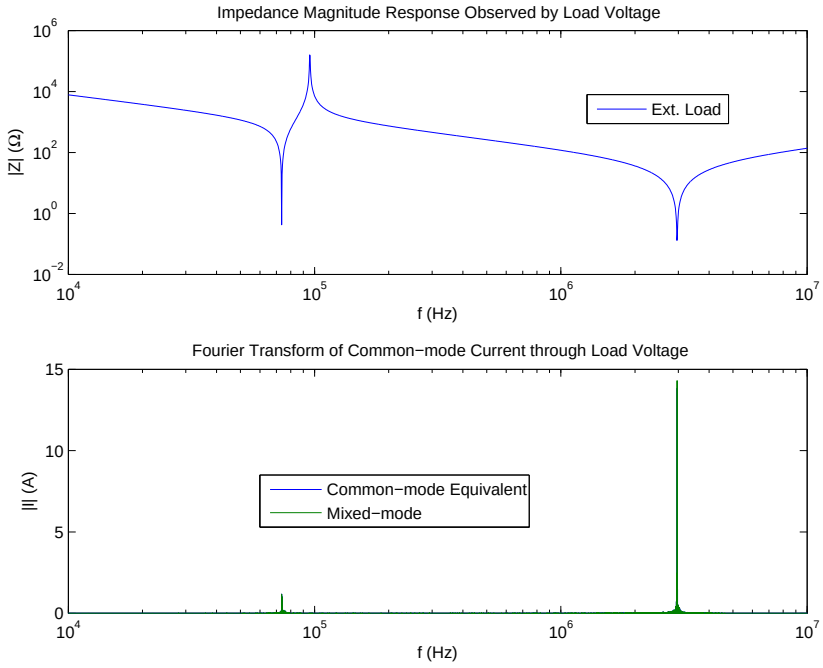


Fig. 3.13. CM Load Current in Frequency Domain for Drive System

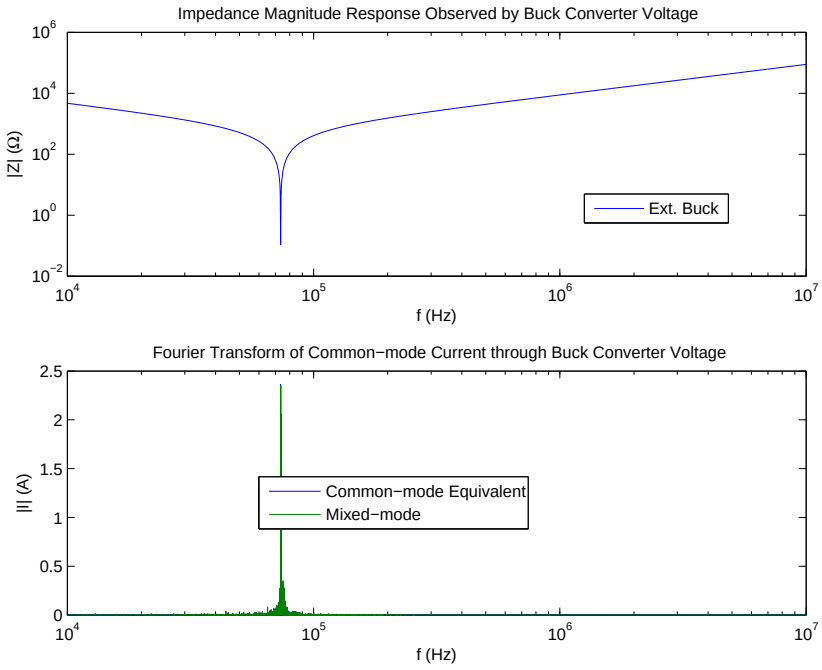


Fig. 3.14. CM Buck Converter Current in Frequency Domain for Drive System

the Fourier transform of the currents, it is readily apparent that CM current appears strongly at the locations of the resonances seen by the CM source.

Importance of Ensuring Correct Operating Mode

As mentioned back in Subsection 2.2.5, the linear components of the buck converter are intertwined with the operation of the semiconductor components. A designer may find the critical inductance that keeps the current through the load positive at all times during normal operation, halve that value, and place inductors with that inductance on the supply and return lines to minimize the physical volume of the buck converter. However, a DM/CM simulation will reveal that the supply-line inductor current will reach negative values. The superposition of the relatively low-frequency DM waveform and the relatively high-frequency CM waveform will cause periodic excursions to negative current values. This effect will cause the results of a CM simulation not to match those of a DM/CM simulation.

It would appear that the simple solution is just to increase the inductance of the pair of inductors. As the inductance increases, the DM current will reach a minimum value farther above zero. However, a designer must remember that the line inductance has mixed-mode effects. The increased inductance will cause the CM resonant points of nearby CM voltage sources to shift downwards in frequency, potentially causing CM current to increase because of the frequencies excited as compared to the critical inductance design. Since parasitic impedances are seldom known in advance, the designer should be cautious in selecting the inductance by employing preliminary FD simulations and choosing a substantial margin above the critical inductance. Furthermore, the selected inductance must also avoid contributing to a CM current resonance that aligns with the frequency spectrum of the excitation.

4. MITIGATION OF COMMON-MODE VOLTAGES

4.1 Alternative Switching Strategies

The previous chapters detailed the modeling of the common-mode impedances in an electronic system, in other words, the establishment of a transfer function. This chapter concentrates on the forcing function applied to the system that arises from common-mode voltage sources with behaviors given by switching strategies. The principal goal is to minimize the amplitude of the CM voltage that is generated by semiconductor devices. By careful selection of the switching frequency, it is possible to calculate the CM voltage spectrum and avoid the resonances established by the CM impedances so as to minimize CM currents.

In the context of three-phase motor drivers, many switching strategies exist to produce a balanced three-phase set of voltages. The goal for inverter operation is to produce pulse width modulation waveforms containing the desired sinusoidal magnitude and fundamental frequency within minimal harmonic content from a DC bus. Of these strategies, space vector modulation (abbreviated SVPWM) has emerged as a common choice. The number of SVPWM variants are numerous and designed to meet different design criteria. The impact on common-mode voltage is often relegated to secondary importance when evaluating switching strategy options. Common-mode voltage induces common-mode currents that lead to electromagnetic compatibility issues, triggering of fault detections systems, and motor bearing wear-out. [1] [2] Part of this chapter will focus on space vector modulation strategies designed to reduce the common-mode voltage generated.

Space vector modulation arose from the work of Murai and Tsunehiro in 1983. [19] The approach in SVPWM is to map the switch states onto a finite space such that a desired voltage vector in the stationary reference frame under certain constraints may

be synthesized. The reference vector is formed based on its projections onto a few switching vectors. For over two decades, alternative switching strategies have arisen in the technical literature in association with efforts to reduce motor bearing damage. These alternative strategies are numerous and remain mostly confined to academic literature rather than in collegiate curricula or industrial practice likely due to their complexity or computational demands. They present extensions to SVPWM with the additional consideration of the spectrum of common-mode voltage generated. [20]

4.1.1 First Space Vector Modulation (1SVPWM) and Other Switching Strategies using Active Switching Vectors

In traditional SVPWM, a commanded stationary reference frame voltage vector must lie in the circle inscribed in the hexagon defined by the vertices of the switching vectors. Synthesis of such a voltage vector is possible using the two switching vectors adjacent to the sector the commanded voltage vector lies in (for direction) along with the zero vectors (for magnitude). For a three-phase machine connected to a DC bus by an inverter, the common-mode voltage that exists between the DC bus and three-phase machine using the lower rail of the DC bus as a voltage reference is $v_{CM,ext}$.

$$v_{CM,ext} = \frac{v_{a-} + v_{b-} + v_{c-}}{3} - \frac{V_{dc}}{2} = \left(\frac{S_a + S_b + S_c}{3} - \frac{1}{2} \right) V_{dc} \tag{4.1}$$

v_{a-}, v_{b-}, and v_{c-} represent the phase voltages applied to the machine relative to the lower rail of the DC bus, V_{dc} is the DC bus voltage, and S_a, S_b, and S_c represent the state of the upper switch for each phase leg (1 for on, 0 for off). Using (4.1), one may conclude that the largest absolute value of $v_{CM,ext}$ results when $S_a = S_b = S_c = 0$ or $S_a = S_b = S_c = 1$. These switch states are the zero vectors $\vec{V}_0$ and $\vec{V}_7$, respectively, in space vector modulation. Thus, the magnitude of the common-mode voltage may be reduced by avoiding the zero vectors and using some other means to establish the magnitude of the synthesized voltage vector.

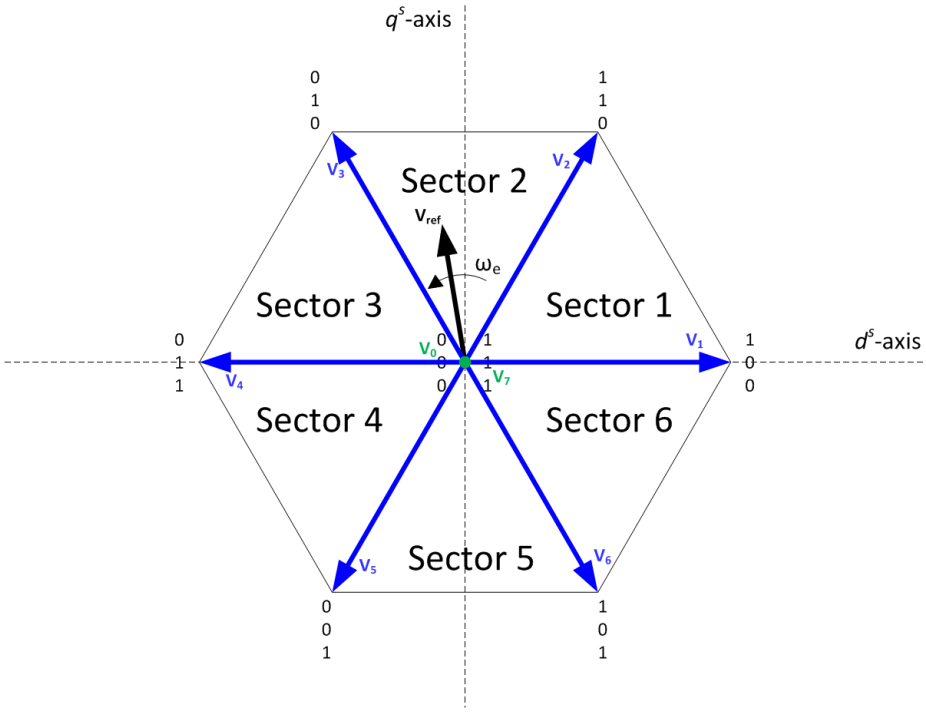


Fig. 4.1. Switching Vector and Hexagonal Sector Definitions in Traditional SVPWM

Say for example that the commanded voltage vector lay in Sector 2 following the definitions in Figure 4.1. The needed switching vectors to synthesize the proper direction of the commanded voltage vector are $\vec{V}_3$ ($S_b = 1$) and $\vec{V}_2$ ($S_a = S_b = 1$). If the zero vectors are to be avoided, then there are three options to consider using a linear combination of the six active switching vectors to synthesize the reference voltage vector with the appropriate magnitude.

1. Three active vector modulation (3AVM): Define a single-switch vector as a member of the set of switching vectors where only one of the three upper switches in the phase legs is on. Namely, either $\vec{V}_1$, $\vec{V}_3$, or $\vec{V}_5$. Similarly, define a double-switch vector as a member of the set of switching vectors where two of the three upper switches in the phase legs are on. Namely, either $\vec{V}_2$, $\vec{V}_4$, or $\vec{V}_6$. If the reference vector is closest to the double-switch vector $\vec{V}_2$ in the sector, in this

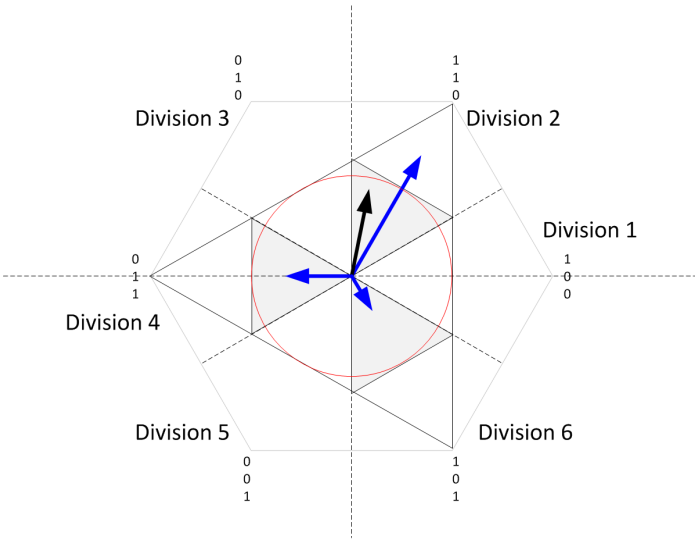


Fig. 4.2. Synthesizing a Voltage Vector in Division 2 with 3AVM

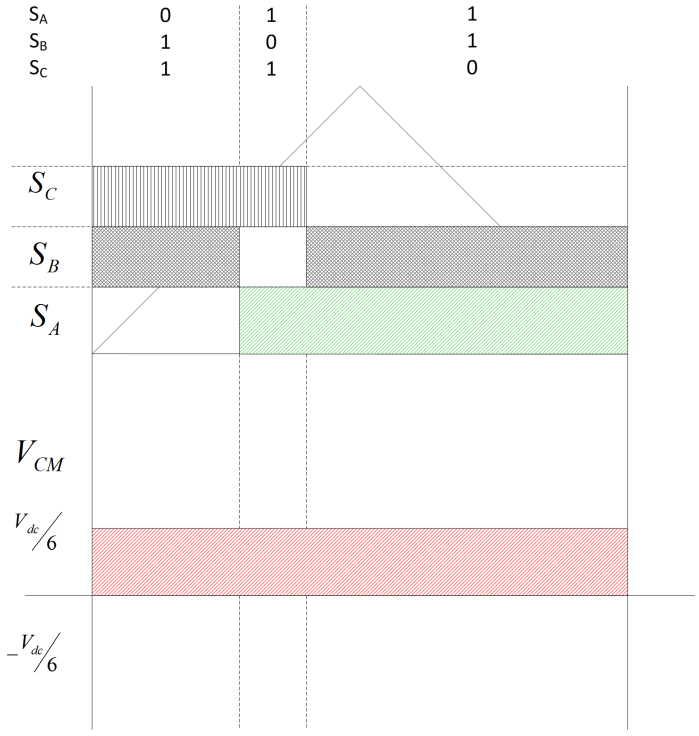


Fig. 4.3. Switch Timing in Division 2 with 3AVM

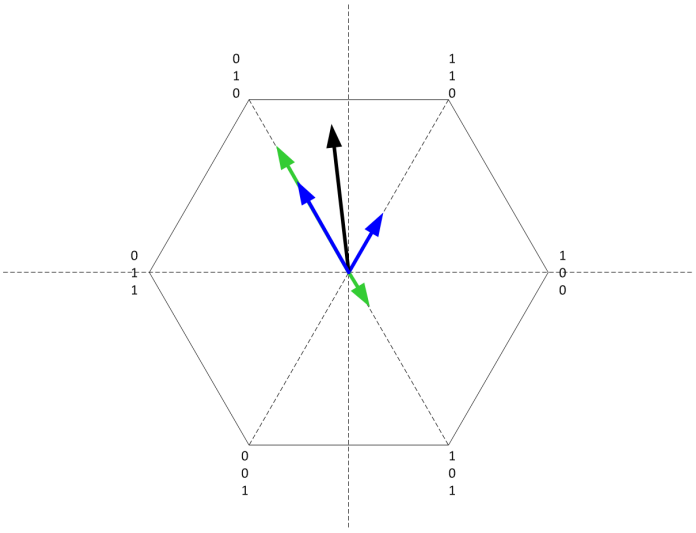


Fig. 4.4. Synthesizing a Voltage Vector in Sector 2 with AZVC-1

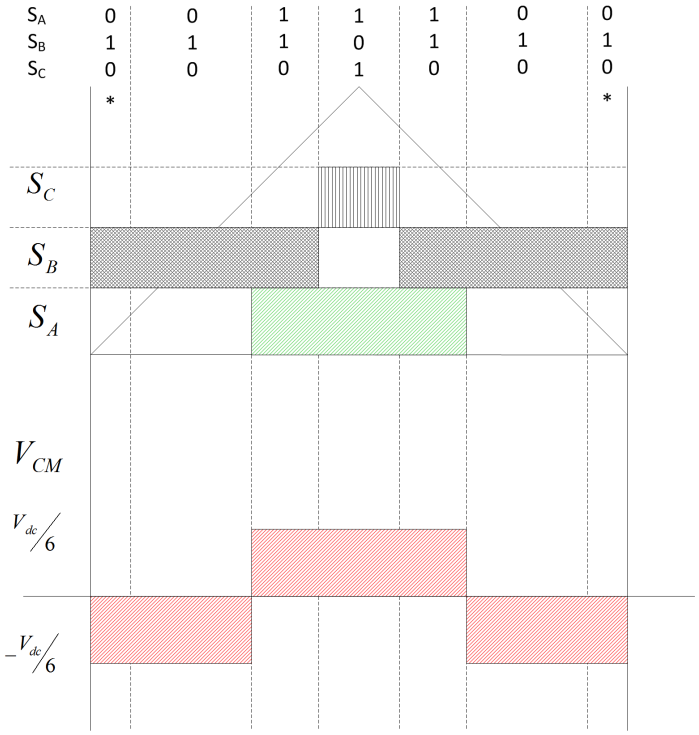


Fig. 4.5. Switch Timing in Sector 2 with AZVC-1

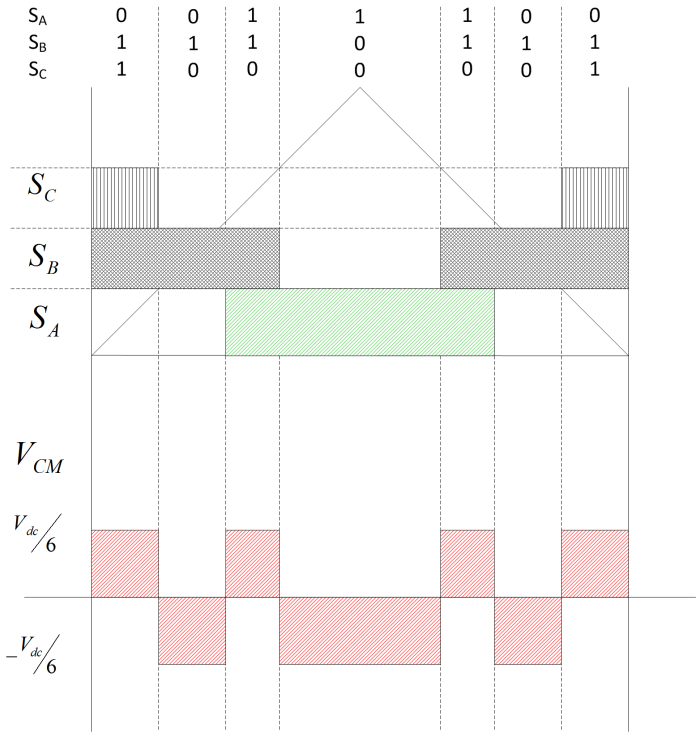


Fig. 4.6. Switch Timing in Sector 2 with 1SVPWM (AZVC-2)

example, replace the projection of the single-switch vector $\vec{V}_3$ with the other two double-switch vectors $\vec{V}_4$ & $\vec{V}_6$ and vice-versa. In other words, when $\vec{V}_{ref}$ is located in the clockwise half of Sector 2 (gray region labeled as Division 2), only $\vec{V}_2$, $\vec{V}_4$, and $\vec{V}_6$ are used to synthesize it as shown in Figure 4.2. Similarly, when $\vec{V}_{ref}$ is located in the counterclockwise half of Sector 2 (white region labeled as Division 3), only $\vec{V}_1$, $\vec{V}_3$, and $\vec{V}_5$ are used to synthesize it. While the decreased number of switching events leads to reduced switching losses, the rich spectrum of common-mode voltage produced and the reduction of the maximum modulation index from the traditional $m = \frac{|\vec{V}_{ref}|}{V_{dc}} = \frac{1}{\sqrt{3}} \approx 0.577$ to $m = \frac{1}{2} \times \frac{2}{3} = \frac{1}{3} \approx 0.333$ is not worth the smaller common-mode voltage magnitude. [20] When moving from one switching vector to another, two switches must change state simultaneously as depicted in Figure 4.3. When dead time is introduced, there is no way to avoid the zero vectors, $\vec{V}_0$ and $\vec{V}_7$. [2] This is a robustness issue that interferes with the original objective of lowering the common-mode voltage magnitude.

2. Active zero vector control with one inverse voltage vector (AZVC-1): An active zero vector is made by adding $\vec{V}_6$ to an additional $\vec{V}_3$ component of the same magnitude as shown in Figure 4.4 or by adding $\vec{V}_5$ to an additional $\vec{V}_2$ component of the same magnitude. This way, the need of having $\vec{V}_0$ or $\vec{V}_7$ as a zero state is eliminated. While this control has the smallest magnitude common-mode voltage spectrum spread over a larger frequency range and an unchanged maximum modulation index of $m = \frac{1}{\sqrt{3}} \approx 0.577$ [20], dead time considerations (using the NSVM1 or NSVM2 pattern introduced by Lai and Shyu [2]) and sector transitions will cause no improvement over traditional space vector modulation. Since robustness cannot be improved because multiple switches must change state at once (evident in Figure 4.5 and explained in the next section), then AZVC-1 will not be considered any further. [2]

3. Active zero vector control with two additional space vectors (AZVC-2 or 1SVPWM): The remaining active vector options to produce a zero vector are $\vec{V}_1$ and $\vec{V}_4$ in equal proportion, the antiparallel pair adjacent to each of the active vectors defining the sector. This method has the same maximum modulation index of $m = \frac{1}{\sqrt{3}}$, similar spectral characteristics of common-mode voltage as conventional SVPWM though with less overall energy [20], and the potential for robust maintenance of the reduced common-mode voltage range with dead time and sector transitions [2] as discussed in the section to follow.

Three equations are used to establish the time spent on each vector in 1SVPWM for a given switching period T_s [1]:

$$T_s = T_1 + T_2 + T_0 \tag{4.2}$$

$$V^s_{q,ref} T_s = V^s_{single,q} T_1 + V^s_{double,q} T_2 \tag{4.3}$$

$$V^s_{d,ref} T_s = V^s_{single,d} T_1 + V^s_{double,d} T_2 \tag{4.4}$$

Times T_1 and T_2 are the durations the single-switch and double-switch active vectors are applied in the switching period, respectively. T_0 is the off duration to be split equally between the switching vectors adjacent to $\vec{V}_{single}$ and $\vec{V}_{double}$. Continuing the example in which $\vec{V}_{ref}$ is in Sector 2, the adjacent switching vectors are $\vec{V}_4$ and $\vec{V}_1$ following the definitions in Figure 4.1. $V^s_{single,q}$ and $V^s_{single,d}$ are the projections of the single-switch active vector onto the stationary reference frame quadrature-axis and direct-axis, respectively, and similarly for $V^s_{double,q}$ and $V^s_{double,d}$ for the double-switch active vector. $V^s_{q,ref}$ and $V^s_{d,ref}$ are q-axis and d-axis components of the commanded voltage vector such that the average value of the switching vectors over T_s yields $\vec{V}_{ref}$.

The primary advantage of 1SVPWM is that the range of modulation indices that can be reached (up to $m = \frac{1}{\sqrt{3}} \approx 0.577$) is just as wide as that for traditional space vector modulation without a large change in the common-mode voltage spectrum. If performed with a standard three-leg inverter, then the reduction in common-mode voltage approaches one-half. The trade-off is that the line-to-line voltage develops a

distortion at the switching frequency and a smaller distortion at the third harmonic of the switching frequency. [1]

4.1.2 Three-dimensional Space Vector Modulation (3DSVPWM)

Three-dimensional space vector modulation is a further extension of first space vector modulation. The antiparallel vectors adjacent to the vector defining the sector in which $\vec{V}_{ref}$ is located are now allowed to have unequal durations ($T_0 = T_{0AD} + T_{0AS}$, $T_{0AS} \neq T_{0AD}$). The time T_{0AD} is defined as the duration of the switching vector adjacent to $\vec{V}_{double}$, called $\vec{V}_{adj,doub}$. The time T_{0AS} is introduced as the duration of the switching vector adjacent to $\vec{V}_{single}$, called $\vec{V}_{adj,sing}$. Because of the fourth unknown time that divides the switching period, an additional equation is needed to solve the system of equations governing the switching strategy. That equation will be the remaining component of the stationary reference frame transformation, the zero-sequence component of each vector. Traditional space vector modulation along the quadrature and direct-axes is being extended into the third dimension using the zero-axis.

All of the switching vectors retain their quadrature-axis and direct-axis components. The zero-axis component is computed by using (4.1). In doing so, the length of the active vectors increases from their two-dimensional value of $\frac{2}{3}$. The switching vector modulation index components may be found in Table 4.1. It might be misleading to continue calling $\vec{V}_0$ and $\vec{V}_7$ "zero vectors" in three dimensions. Both have relatively strong yet opposite effects on zero-sequence voltages.

Table 4.1.
Modulation Index Components of Three-dimensional Switching Vectors

Vector	m_d^s	m_q^s	m_0	$\|m\|$
$\vec{V}_0$	0	0	$-\frac{1}{2}$	$\frac{1}{2}$
$\vec{V}_1$	$+\frac{2}{3}$	0	$-\frac{1}{6}$	$\frac{\sqrt{17}}{6}$
$\vec{V}_2$	$+\frac{1}{3}$	$+\frac{1}{\sqrt{3}}$	$+\frac{1}{6}$	$\frac{\sqrt{17}}{6}$
$\vec{V}_3$	$-\frac{1}{3}$	$+\frac{1}{\sqrt{3}}$	$-\frac{1}{6}$	$\frac{\sqrt{17}}{6}$
$\vec{V}_4$	$-\frac{2}{3}$	0	$+\frac{1}{6}$	$\frac{\sqrt{17}}{6}$
$\vec{V}_5$	$-\frac{1}{3}$	$-\frac{1}{\sqrt{3}}$	$-\frac{1}{6}$	$\frac{\sqrt{17}}{6}$
$\vec{V}_6$	$+\frac{1}{3}$	$-\frac{1}{\sqrt{3}}$	$+\frac{1}{6}$	$\frac{\sqrt{17}}{6}$
$\vec{V}_7$	0	0	$+\frac{1}{2}$	$\frac{1}{2}$

The four equations establishing 3DSVPWM vector durations for a given switching period T_s are [1]:

$$T_s = T_{0AS} + T_1 + T_2 + T_{0AD} \tag{4.5}$$

$$V^s_{q,ref}T_s = V^s_{adj,sing,q}T_{0AS} + V^s_{single,q}T_1 + V^s_{double,q}T_2 + V^s_{adj,doub,q}T_{0AD} \tag{4.6}$$

$$V^s_{d,ref}T_s = V^s_{adj,sing,d}T_{0AS} + V^s_{single,d}T_1 + V^s_{double,d}T_2 + V^s_{adj,doub,d}T_{0AD} \tag{4.7}$$

$$V_{0,ref}T_s = V_{adj,sing,0}T_{0AS} + V_{single,0}T_1 + V_{double,0}T_2 + V_{adj,doub,0}T_{0AD} \tag{4.8}$$

The subscript "0" in Equation 4.8 refers to projections of a vector along the zero-axis. Since it has been established that common-mode voltage leads to many undesirable occurrences, it is desired to set $V_{0,ref} = 0$ so that the synthesized voltage vector will lack a contribution to the common-mode voltage over a switching period on average. While 1SVPWM also limits the instantaneous magnitude of common-mode voltage to $\frac{V_{dc}}{6}$, only 3DSVPWM has the stronger benefit of $\bar{v}_{CM,ext} = 0$ as summarized in Table 4.2.

Table 4.2.
Summary of Alternative Space Vector Modulation Performance

Metric	**Traditional SVPWM**	**1SVPWM**	**3DSVPWM**
$\lvert v_{CM,ext}(t)\rvert$	$\leq \frac{V_{dc}}{2}$	$\leq \frac{V_{dc}}{6}$	$\leq \frac{V_{dc}}{6}$
$\bar{v}_{CM,ext}$	$\neq 0$	$\neq 0$	$= 0$
$v_{CM,ext}$ spectrum	rich and strong	rich and reduced	rich and reduced
v_{ll} spectrum	baseline	noticeable distortions at f_{sw} and $3f_{sw}$	small distortions at f_{sw} and $3f_{sw}$
m_{max}	$\frac{1}{\sqrt{3}}$	$\frac{1}{\sqrt{3}}$	$\frac{1}{2}$

The hexagon in the q^sd^s-plane commonly used to visualize space vector modulation is a projection of the vertices of a gyroelongated triangular bipyramid formed from the eight switching vectors in q^sd^s0-space as seen in Figure 4.7. This solid geometry is only valid for the standard three-leg inverter. Viewing this region from above produces the traditional hexagon in Figure 4.8 used to visualize space vector modulation with

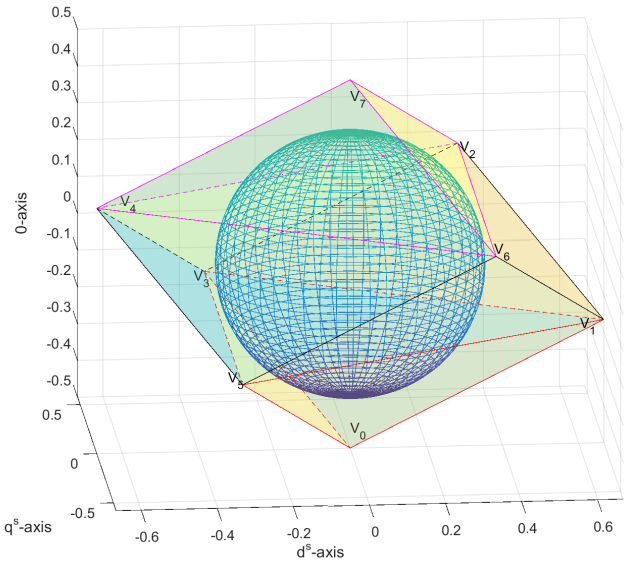


Fig. 4.7. Gyroelongated Triangular Bipyramid Region of Space Vector Modulation in QD0-Space

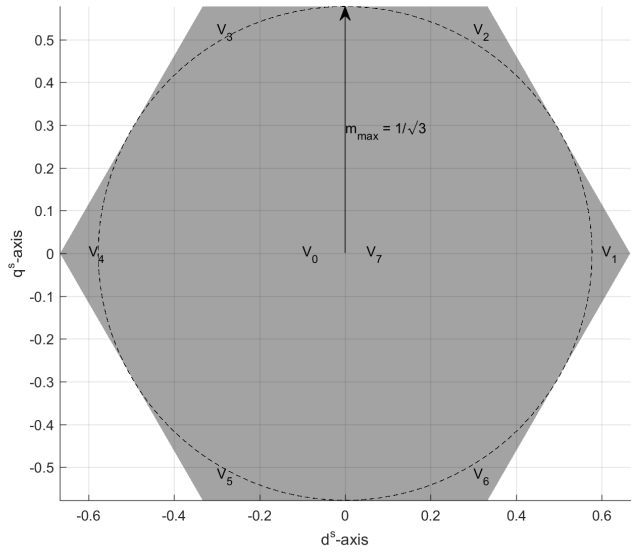


Fig. 4.8. Projection of Three-dimensional Space Vector Modulation onto QD-plane

an inscribed circle of radius $\frac{1}{\sqrt{3}}$ giving the overmodulation boundary. The direction of the *0*-axis using unit vectors is

$$\hat{v}_0 = \hat{v}_d \times \hat{v}_q. \tag{4.9}$$

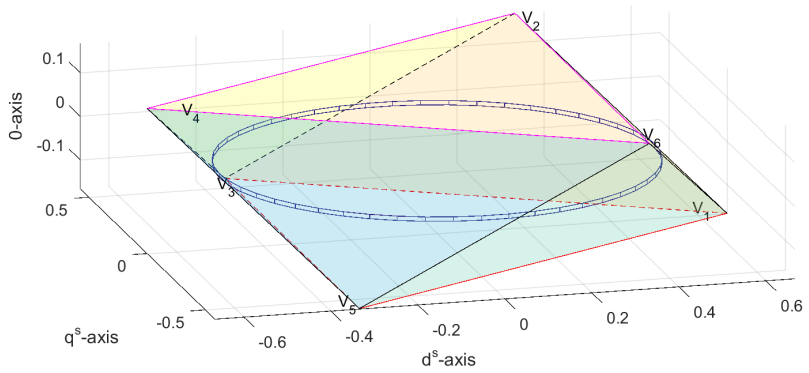


Fig. 4.9. Active Vectors in Three-dimensional Space Vector Modulation

Viewed in three dimensions, the single-switch vectors $\vec{V}_1$, $\vec{V}_3$, and $\vec{V}_5$ extend towards an equilateral triangle in a plane below the $q^s d^s$-plane. Similarly, the double-switch vectors $\vec{V}_2$, $\vec{V}_4$, and $\vec{V}_6$ extend towards an equilateral triangle rotated 30° relative to the first in a plane above the $q^s d^s$-plane. By themselves, the active switching vectors define a triangular antiprism as shown in Figure 4.9. The zero vector with all switches off, $\vec{V}_0$, points opposite the positive *0*-axis and forms the triangular pyramid outlined in red with the single-switch triangle. The zero vector with all switches on, $\vec{V}_7$, points along the positive *0*-axis and forms the triangular pyramid outlined in magenta with the double-switch triangle. Because of their greater zero-axis components that give rise to increased instantaneous common-mode voltages compared to

the active vectors (evidenced by their formation of the apices of the gyroelongated triangular bipyramid in Figure 4.7), these two zero vectors are avoided.

Analyzing the geometry to find the overmodulation boundary is much more complicated in three dimensions. The goal is to find the largest sphere of radius r $\left(r = \sqrt{(m_q^s)^2 + (m_d^s)^2 + (m_0)^2}\right)$ that lies entirely within the gyroelongated triangular bipyramid. The antiprismatic faces are closer to the origin than the pyramidal faces; therefore, they provide the limit on the volume of the sphere. By finding the plane normal of a face, the distance from the face to the origin sets the radius of the sphere and thus the maximum modulation index (reference vector amplitude divided by DC bus voltage) to $m = \frac{|\vec{V}_{ref}|}{V_{dc}} = \frac{1}{2\sqrt{2}} \approx 0.354$. Recall that the reference vector will be stationary along the *0*-axis (typically with no component in that direction for balanced loads), and its q^s-axis and d^s-axis components travel in a circle over a fundamental period.

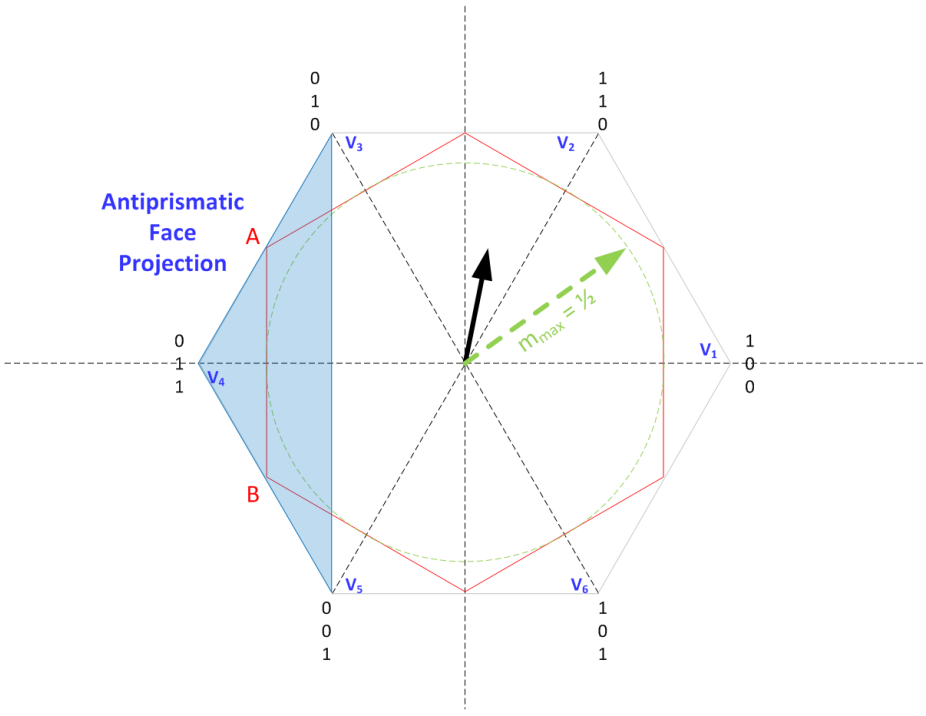


Fig. 4.10. QD-plane Slice of Three-dimensional Space Vector Modulation

While this spherical radius would appear to be a significant reduction in performance, the value of $V_{0,ref}$ is almost always chosen to be zero. The intersection of the antiprismatic faces of the region (see Figure 4.9) with the $q^s d^s$-plane defines the red hexagon seen in Figure 4.10. The radius of the inscribed circle of this hexagon will be the maximum modulation index without a *0*-axis component for the linear range. It is known that the triangular bases are equidistant from the $q^s d^s$-plane. Therefore, the circle will have a radius that is the mean of the d^s-axis components of $\vec{V}_4$ and $\vec{V}_3/\vec{V}_5$ (alternatively, the d^s-axis mean of $\vec{V}_1$ and $\vec{V}_2/\vec{V}_6$). This mean line $\overline{AB}$ may be seen connecting the midpoints of the legs of the *0*-axis projection of the antiprismatic face $V_4V_3V_5$ also in Figure 4.10. A similar argument may be applied to the other five edges of the hexagon. Thus, the maximum modulation index with 3DSVPWM and $V_{0,ref} = 0$ is $m = \frac{1}{2} \ -\frac{2}{3} - \frac{1}{3} \ = \frac{1}{2} = 0.500$.

The primary advantage of 3DSVPWM is the ability to command zero common-mode voltage on average in addition to the reduced instantaneous value of $|v_{CM,ext}(t)|$. It produces less line-to-line voltage distortion than 1SVPWM but more than traditional SVPWM. [1] The disadvantage is that the maximum modulation index is limited to $0.500 < 0.577$, a reduction of 13.4%.

4.1.3 Interleaved Sine-Triangle Modulation with Third Harmonic Injection (IST3PWM)

It has been shown with substantial calculation [21] that a switching strategy called interleaved sine-triangle modulation with third harmonic injection (IST3PWM) is equivalent to 3DSVPWM. This fact is in analogy to the equivalence of sine-triangle modulation with third harmonic injection (ST3PWM) to conventional SVPWM. Implementing IST3PWM from ST3PWM is rather straightforward. Rather than compare the desired phase waveform to a single carrier waveform for all three phases, the desired phase waveform is compared to a carrier waveform specific to that phase. The three carrier waveforms of IST3PWM are identical to each other except each is

shifted by $\frac{2\pi}{3}$ rad in the switching period. IST3PWM is significantly less calculation intensive in exchange for requiring additional timers and comparators.

4.2 Switching Patterns to Address Non-ideal Behavior

The attention thus far has been on switching strategies, the selection of switching vectors to use and their respective durations to best synthesize the stationary reference frame vector under given criteria. There is a separate idea of switching patterns that must be considered independently afterwards in order to implement the switching patterns on hardware. Switching patterns include practical considerations of dead time and finite rise and fall times as well as sector transitions to achieve switching strategy objectives. The outcome of the switching pattern is the best sequence to visit the switching vectors for the switching strategy and how to handle successive switching periods.

4.2.1 Dead Time Considerations

Dead time is the duration given to electronic switches in a phase leg to avoid the shoot-through condition when the switches change state. This creates instances in which neither switch is commanded to be on. While dead time has been mentioned in the above descriptions of alternative switching strategies, it is helpful to understand the effect that it has on common-mode voltage.

Consider the situation in Figure 4.11 where a phase leg is commutating with the current heading out of the phase. A dead time t_{dead} is split, $\frac{t_{dead}}{2}$ to the rising edges and $\frac{t_{dead}}{2}$ to the falling edges, and applied to the top and bottom switches. Whenever the bottom switch is on, the voltage at the terminal is pulled to the lower rail of the DC bus. If the bottom switch is closed, then the current flowing out of the phase terminal causes the top antiparallel diode to conduct and pull the phase terminal to the upper rail of the DC bus. There is an indeterminate rise or fall period within

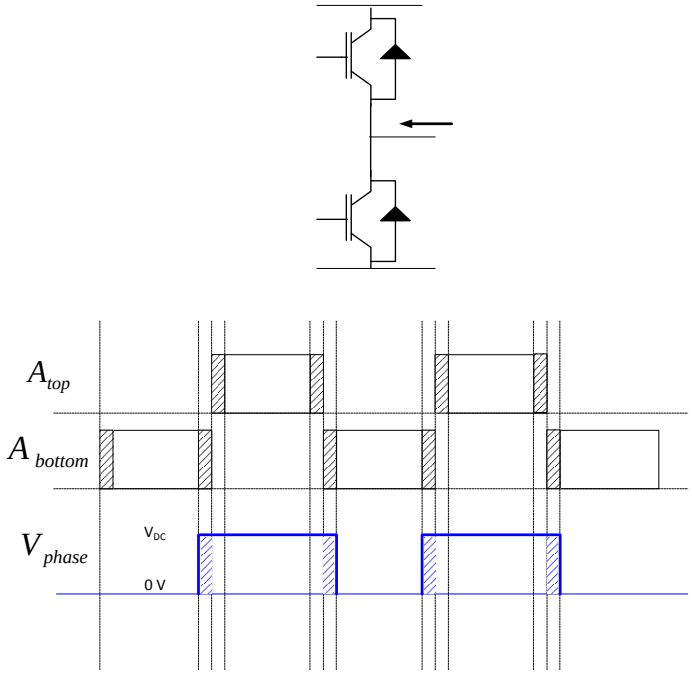


Fig. 4.11. Switching Waveforms with Current Out of the Phase Terminal

t_{dead} immediately after the bottom switch is in the process of closing or opening. The overall effect is to increase the duration in which the phase is active.

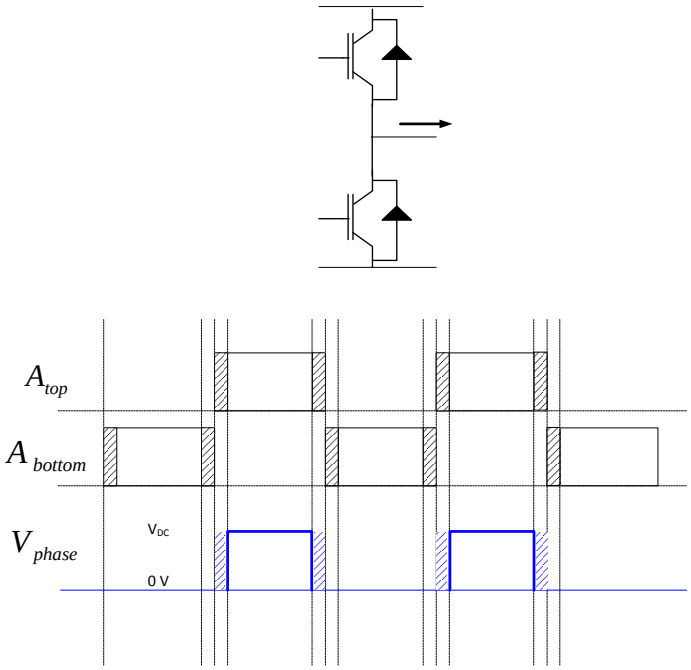


Fig. 4.12. Switching Waveforms with Current Into the Phase Terminal

The opposite situation in which the phase leg is commutating with the current heading into the phase is depicted in Figure 4.12. A dead time t_{dead} is likewise split, $\frac{t_{dead}}{2}$ to the rising edges and $\frac{t_{dead}}{2}$ to the falling edges, and applied to the top and bottom switches. Whenever the top switch is on, the voltage at the terminal is pulled to the upper rail of the DC bus. If the top switch is closed, then the current flowing into the phase terminal causes the bottom antiparallel diode to conduct and pull the phase terminal to the lower rail of the DC bus. There is an indeterminate rise or fall period within t_{dead} while the top switch is in the process of opening or closing. The overall effect is to decrease the duration in which the phase is active.

From this knowledge of how dead time affects single phases, an understanding of three-phase switching patterns with dead time may be developed. AZVC-1 was mentioned earlier to have an unresolvable problem with dead time, and so it will

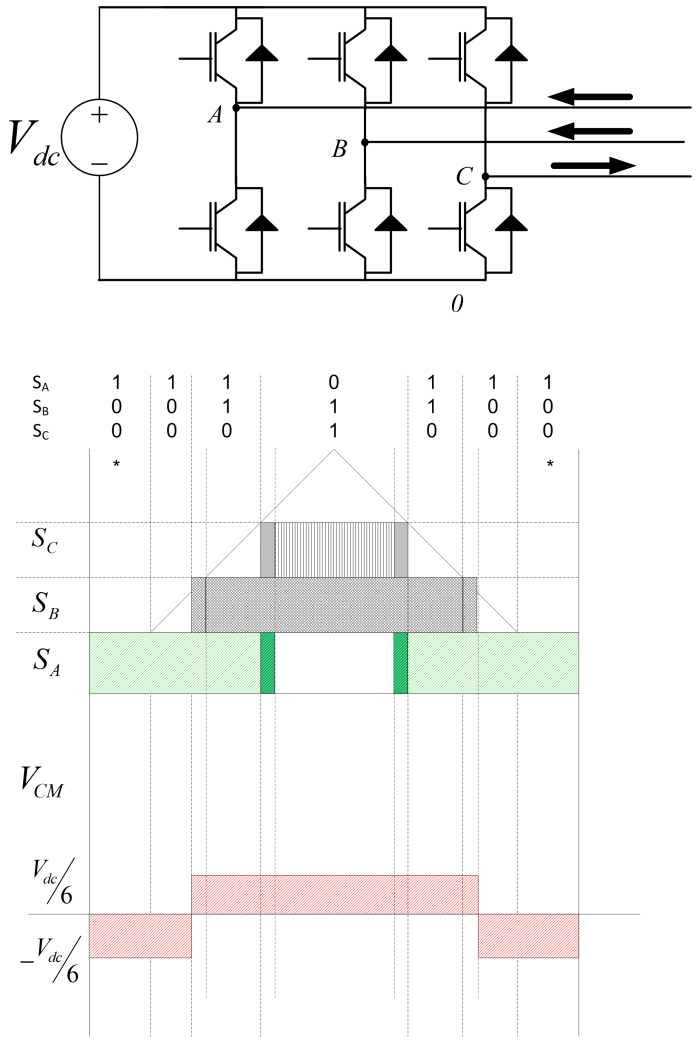


Fig. 4.13. Dead Time Problem Avoided for AZVC-1 Sector 2 Case

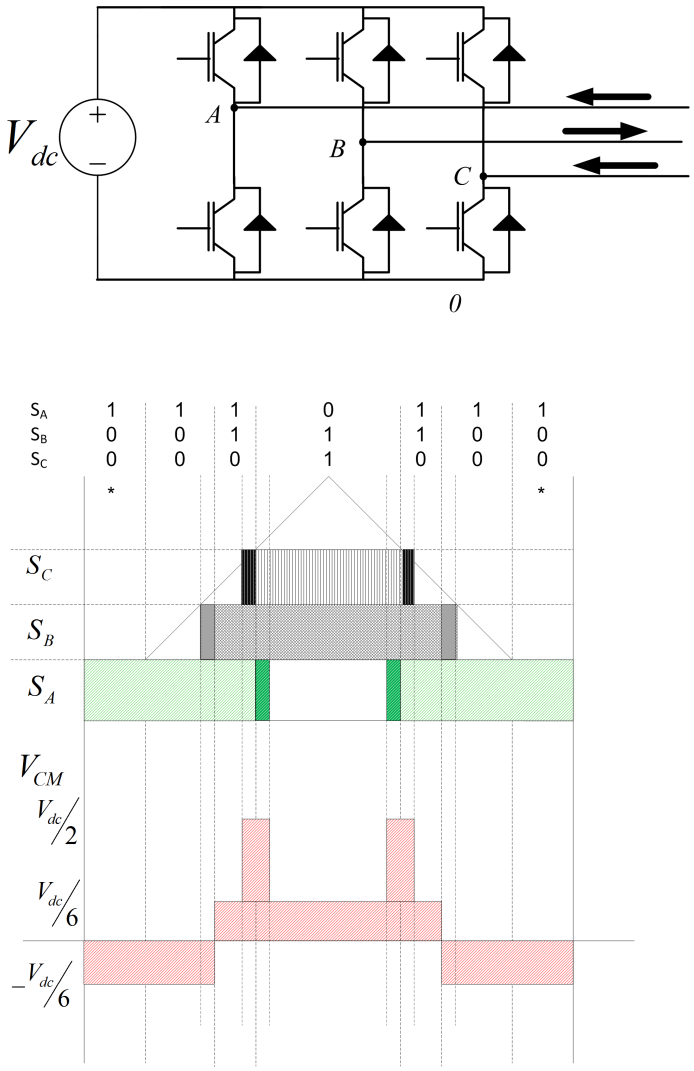


Fig. 4.14. Dead Time Problem Encountered for AZVC-1 Sector 2 Case

be used here with the NSVM 1 switching pattern to illustrate dead time effects. [2] Figure 4.13 depicts a situation in which the reference vector is in sector 2, the a- and b-phase currents are heading out of the phases, and the c-phase current heads into the phase. Notice that the increased duration of the b phase is not an issue for realistic values of t_{dead}. The transition from $\vec{V}_2$ to $\vec{V}_4$ is suspect because the a phase and c phase commute simultaneously. The "swelling" of the a phase (phase now active when darker green) due to the current out that phase is offset by the "contraction" of the c phase (phase now inactive when lighter gray) due the current into the phase. There are only two phases active over the course of the transition, so $v_{CM,ext} = \frac{V_{dc}}{6}$ during this time. The currents of the simultaneously commutating phases being in opposite directions is not a hazard for violating the $|v_{CM,ext}| \leq \frac{V_{dc}}{6}$ condition that AZVC-1 tried to achieve.

Figure 4.14 depicts the AZVC-1 switching strategy in sector 2 with the a- and c-phase current heading out of the phases and the b-phase current now into the phase. The NSVM 1 switching pattern is still being used. [2] The decreased duration of the b phase is not of concern here. The $\vec{V}_2$ to $\vec{V}_4$ is now problematic because both phases "swell" due to the current into the phase while both phases commutate (phases active when darker green and darker black). The transition leads to a time of duration t_{dead} in which $\vec{V}_7$ is reached, so $v_{CM,ext} = \frac{V_{dc}}{2}$ is achieved in this instant. The currents of the simultaneously commutating phases being in the same direction caused a violation of the desired limitation of the instantaneous common-mode voltage. The simultaneous "swell" of two phases over t_{dead} when the remaining phase is active or the simultaneous "contraction" of two phases over t_{dead} when the remaining phase is inactive are both problematic.

Both 1SVPWM and 3DSVPWM manage to reduce the range of the common-mode voltage to span just one-third of the DC bus voltage instead of the full DC bus voltage just like 3AVM and AZVC-1. However, the former two are more advanced switching strategies that only use adjacent vectors to synthesize $\vec{V}_{ref}$. Without simultaneous commutation that comes from jumping over adjacent, active switching vectors, there

is no risk of accidentally applying the zero vectors, $\vec{V}_0$ and $\vec{V}_7$. The switching pattern developed must visit the switching vectors successively; otherwise, the common-mode voltage will display unexpected peaks during the dead time t_{dead} that counteract what had been accomplished with the switching strategy changes. [2] The danger potentially lies with the sequence within a switching period T_s and the transition between switching periods. These ideas will be explored now.

4.2.2 Proper Switching Period Sequence

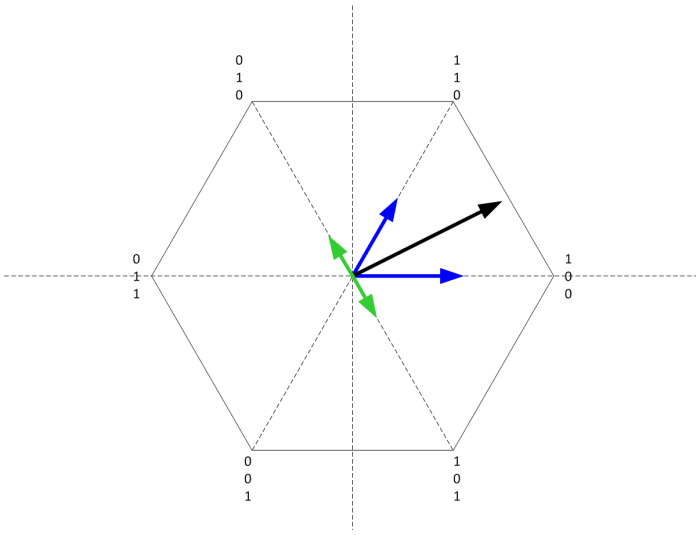


Fig. 4.15. Synthesizing a Voltage Vector in Sector 1 with 1SVPWM

Lai and Shyu devote much scrutiny and hardware evaluation towards determining the optimum switching sequence for reducing common-mode voltage. They determine that the NSVM3 pattern presented is robust for all possible sector transitions and dead time lengths. The pattern within a switching period goes $\overline{S_{single} \oplus S_{double}} \rightarrow S_{single} \rightarrow S_{double} \rightarrow S_{single}S_{double}$ for the leading edge and $S_{single} \oplus S_{double} \rightarrow S_{single} \rightarrow S_{double} \rightarrow \overline{S_{single} \oplus S_{double}}$ for the trailing edge of each switching period. [2] S_{single} is the set of switch states for the single-switch active vector that borders the sector in which $\vec{V}_{ref}$ lies, and S_{double} is the set of switch states for the double-switch active

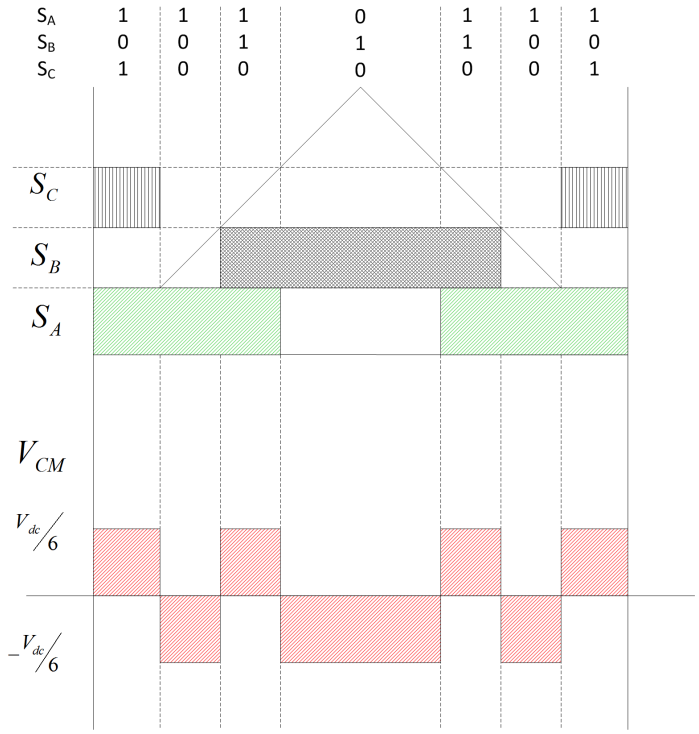


Fig. 4.16. Switch Timing in Sector 1 with 1SVPWM

vector that borders the sector on the other side. The NSVM3 pattern has the voltage projections in Figure 4.15 and the timing in Figure 4.16. By visually inserting a brief "swell" or "contraction" of t_{dead} when switches commutate, it can be seen that zero vectors are never reached because 1SVPWM and 3DSVPWM only uses adjacent switching vectors. Note that the optimal sequence of 3DSVPWM is the same as for 1SVPWM except that the constraint that $\frac{T_0}{2} = T_{0AS} = T_{0AD}$ no longer applies in the three-dimensional case.

By careful examination of the NSVM3 switching pattern, it can be noted that it is equivalent to $S_{adj,sing} \rightarrow S_{single} \rightarrow S_{double} \rightarrow S_{adj,doub}$ for the leading edge and $S_{adj,doub} \rightarrow S_{double} \rightarrow S_{single} \rightarrow S_{adj,sing}$ for the trailing edge. Because $S_{adj,sing}$ is the set of switch states for the active vector adjacent to the single-switch vector outside of the sector and similarly for $S_{adj,doub}$, it can be found that the switching pattern is just a careful generalization of the 3DSVPWM that Oriti, Julian, and Lipo developed to the other sectors. [1] A given switching period will have vector durations follow in the leading-edge, trailing-edge sequence for odd-numbered sectors:

$$\frac{T_{0AS}}{2} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_2}{2} \rightarrow T_{0AD} \rightarrow \frac{T_2}{2} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_{0AS}}{2}.$$

It is important to note which vectors are single-switch active vectors and which are double-switch active vectors. To make this clear, a commanded voltage reference vector in the second sector is synthesized as seen in Figure 4.17. Note that the pattern of the vectors in Figure 4.18 in 1SVPWM starts with the leading edge (first is the active zero vector component adjacent to the single-switch vector). Now in this sector, that implies that the switch states travel clockwise in the $q^s d^s$-plane on the leading edge of each switching period rather than counterclockwise as they did for the odd-numbered sectors. For this reason, a lookup table is needed to determine whether the switching period should progress leading edge to trailing edge (for reference vectors sampled in odd-numbered sectors) or trailing edge to leading edge (for even-numbered

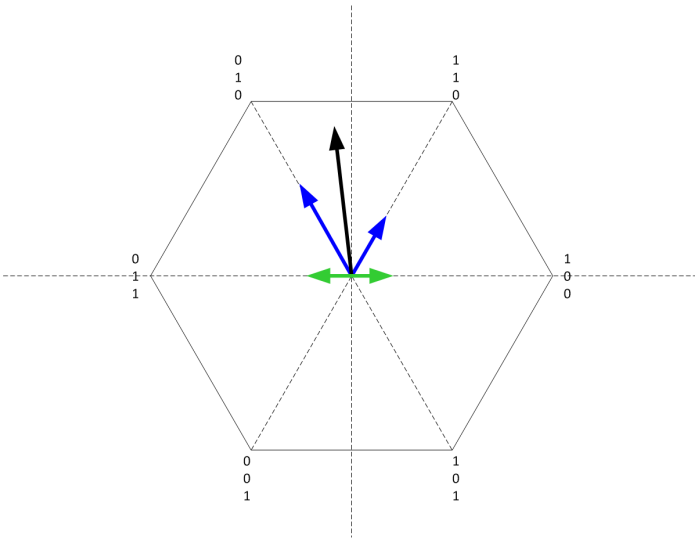


Fig. 4.17. Synthesizing a Voltage Vector in Sector 2 with 1SVPWM

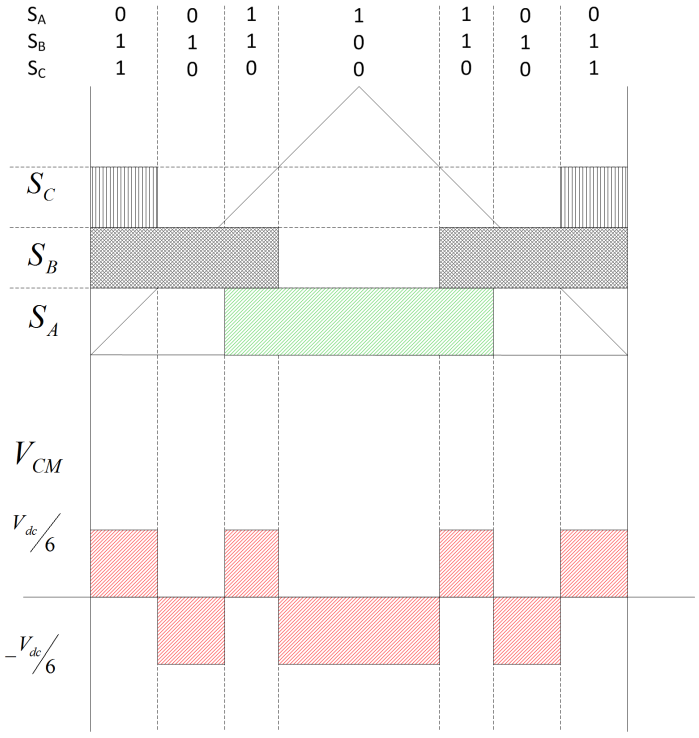


Fig. 4.18. Switch Timing in Sector 2 with 1SVPWM

sectors) and simplify this matter. The switching period should use the following trailing-edge, leading-edge sequence for even-numbered sectors:

$$\frac{T_{0AD}}{2} \rightarrow \frac{T_2}{2} \rightarrow \frac{T_1}{2} \rightarrow T_{0AS} \rightarrow \frac{T_1}{2} \rightarrow \frac{T_2}{2} \rightarrow \frac{T_{0AD}}{2}.$$

4.2.3 Sector Transitions

As mentioned earlier, caution must be taken when $\vec{V}_{ref}$ passes over a sector boundary between successive samplings. The trouble arises because the leading edge of the switching sequence travels counterclockwise around the switching vectors for odd-numbered sectors and clockwise for even-numbered sectors. In order to avoid the zero vectors, only a single switch can change state at a time (jump to an adjacent switching vector) due to dead time. Lai and Shyu propose a way to do this at sector transitions by introducing a switching period immediately after the transition with the leading edge of the sector the voltage reference vector left followed by another leading edge, this time of the sector being entered. The sequence continues alternating trailing edges and leading edges after that. [2] While introducing some complexity, this ensures that the switching vector at the end of one switching period is the same as the one at the start of the next and puts pattern changes in the middle of the switching period. To see the robust sequence, let the superscript denote the sector number for a switching period in sector 1 followed by a transition to sector 2 followed by another switching period in sector 2. Note that the values of T_{0AS}, T_1, T_2, and T_{0AD} will differ for the three different switching periods T_s depicted below.

$$\cdots \rightarrow \frac{T^1_{0AS}}{2} \rightarrow \frac{T^1_1}{2} \rightarrow \frac{T^1_2}{2} \rightarrow T^1_{0AD} \rightarrow \frac{T^1_2}{2} \rightarrow \frac{T^1_1}{2} \rightarrow \frac{T^1_{0AS}}{2} \text{ (Sector 1)} \rightarrow$$
$$\frac{T^1_{0AS}}{2} \rightarrow \frac{T^1_1}{2} \rightarrow \frac{T^1_2}{2} \rightarrow \frac{T^1_{0AD}}{2} \rightarrow \frac{T^2_{0AS}}{2} \rightarrow \frac{T^2_1}{2} \rightarrow \frac{T^2_2}{2} \rightarrow \frac{T^2_{0AD}}{2} \text{ (Post-transition Step)} \rightarrow$$
$$\frac{T^2_{0AD}}{2} \rightarrow \frac{T^2_2}{2} \rightarrow \frac{T^2_1}{2} \rightarrow T^2_{0AS} \rightarrow \frac{T^2_1}{2} \rightarrow \frac{T^2_2}{2} \rightarrow \frac{T^2_{0AD}}{2} \text{ (Sector 2)} \rightarrow \cdots$$

Here is the same sequence with the commanded switch states instead of the durations:

$$\cdots \rightarrow \begin{pmatrix}1\\0\\1\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\1\end{pmatrix} \text{ (Sector 1)} \rightarrow$$
$$\begin{pmatrix}1\\0\\1\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\1\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \text{ (Post-transition Step)} \rightarrow$$
$$\begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\1\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \text{ (Sector 2)} \rightarrow \cdots$$

With fast hardware to do space vector modulation calculations for a standard three-leg inverter, the benefits of having the switching vector at the end of one switching period match that at the start of the next can be minimal. The post-transition step can be removed altogether since the vector corresponding to $\frac{T^1_{0AS}}{2}$ (end of trailing edge at end of switching period for odd-numbered sectors) is adjacent to the one corresponding to $\frac{T^2_{0AD}}{2}$ (start of trailing edge at start of switching period for even-numbered sectors). Therefore, dead time will not present any issues at the sector transition. The potential for voltage error is reduced this way, and some of the complexity of sector transitions is made smaller. The robust sequence for the reference vector being sampled in sector 1 followed by sector 2 would then be as follows.

$$\cdots \rightarrow \frac{T^1_{0AS}}{2} \rightarrow \frac{T^1_1}{2} \rightarrow \frac{T^1_2}{2} \rightarrow T^1_{0AD} \rightarrow \frac{T^1_2}{2} \rightarrow \frac{T^1_1}{2} \rightarrow \frac{T^1_{0AS}}{2} \text{ (Sector 1)} \rightarrow$$
$$\frac{T^2_{0AD}}{2} \rightarrow \frac{T^2_2}{2} \rightarrow \frac{T^2_1}{2} \rightarrow T^2_{0AS} \rightarrow \frac{T^2_1}{2} \rightarrow \frac{T^2_2}{2} \rightarrow \frac{T^2_{0AD}}{2} \text{ (Sector 2)} \rightarrow \cdots$$

The same sequence showing the commanded switch states would be:

$$\cdots \rightarrow \begin{pmatrix}1\\0\\1\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\1\end{pmatrix} \text{ (Sector 1)} \rightarrow$$
$$\begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\1\end{pmatrix} \rightarrow \begin{pmatrix}0\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\1\\0\end{pmatrix} \rightarrow \begin{pmatrix}1\\0\\0\end{pmatrix} \text{ (Sector 2)} \rightarrow \cdots$$

4.3 Implementing Switching Changes

The performance requirements of modern power electronic systems require switching strategies capable of larger modulation indices without causing large common-mode voltages. Oriti, Julian, and Lipo presented two different extensions of space vector modulation to generate less common-mode voltage. Lai and Shyu carefully examined the effects of dead time and sector transitions on common-mode voltage and developed the appropriate switching pattern through the active vectors that will forbid instances where $v_{CM,ext} = \pm\frac{V_{dc}}{2}$. Hofmann and Zitzelsberger developed quantitative metrics for many active vector formulations of space vector modulation, including the impact on the voltage spectrum.

Evaluating the objectives given for selecting a modified space vector modulation strategy for implementation, 1SVPWM should be the first investigated because it offers the same performance capabilities as before. However, 3DSVPWM should be left as an option since it can achieve the maximum benefits of common-mode voltage reduction unlike 1SVPWM with dead time and because it will distort the differential-mode voltages to a lesser extent. The NSVM 3 switching pattern should be used for both. The effectiveness of switching-strategy-based common-mode current mitigation will lie in experimental results that might hybridize ideas based on the modulation index and switching frequency being used at a particular time.

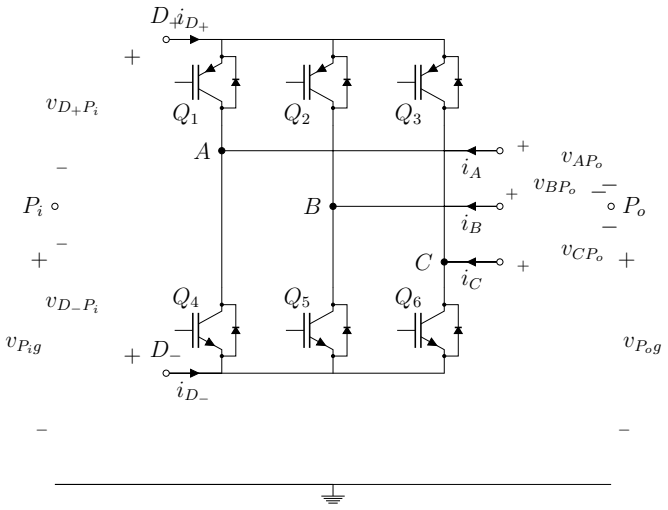


Fig. 4.19. Standard Three-leg Inverter

It should be noted that these switching algorithms were meant to operate on a four-leg inverter instead of the standard three-leg inverter shown in Figure 4.19 as they have been presented in this chapter. These inverters contain a fourth pair of electronic switches that moves in tandem with one of the other phase-leg switch pairs to cancel out common-mode voltage actively rather than on average over a switching period. The region formed by the sixteen switching vectors in this alternate configuration fits inside a hexagonal prism. The calculation of adjacent vectors to one of twenty-four tetrahedral sectors becomes much more involved. [22] It has also been proven that a carrier-based alternative using an offset voltage is equivalent to the 3DSVPWM strategy while being less computationally involved. [21] While these four-leg inverters would incur increased product costs, volumes, and masses, the reduction in common-mode current with these modified switching strategies goes from being a factor of one-half to two orders of magnitude less. [1]

4.4 Hardware Changes

The mitigation effects that come from modifying power electronics switching may not be sufficient to avoid the unwanted common-mode issues that an engineer may wish to avoid. After all, no amount of modifying the switching can shift the location in frequency of a troublesome CM resonant point. For a given impedance response, only the switching frequency may be adjusted to avoid the resonances present. Changes to the electrical system will change the CM impedance, shifting resonances, redirecting CM current, and adjusting the magnitude of various CM current components.

5. CONCLUSION

In this research, the common-mode equivalent circuit modeling approach taken by Brovont and Pekarek [9] was applied to an electric drive system. The system was divided into several circuit blocks, and the common-mode equivalent circuit of each was derived, sometimes finding results for models of different complexity for the same circuit block. References were chosen for the arbitrary points in the circuit blocks so that they may be interconnected and so that the common-mode voltages may be characterized.

Simulations of the mixed-mode circuit and common-mode equivalent circuit were run for two different systems: a source-fed inverter and brake chopper using the Chen and Lipo machine model and a hybrid drive architecture using the Akagi machine model for both machines within. It was shown that the common-mode equivalent circuit takes less time to solve and produces common-mode voltage and common-mode current waveforms that are nearly identical to those produced by the mixed-mode circuit to within an acceptable margin of error.

Switching effects on the common-mode voltage waveforms were also analyzed. First space vector modulation (1SVPWM) and three-dimension space vector modulation (3DSVPWM) are presented as methods of reducing the magnitude of the common-mode voltage waveform. To address non-ideal behavior that arises from dead time, a switching pattern is developed that avoids violating commanded common-mode voltage magnitude in 1SVPWM and 3DSVPWM during switch state transitions. Future work is needed to address alternative switching strategies for common-mode voltage reduction, negative impacts of alternative switching strategies on line-to-line voltages, different semiconductor device topologies in inverters, and simulation of many complicated models in the hybrid drive architecture.

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