Load Slammer Design for DC-DC Converter Testing

A Senior Project

presented to

the Faculty of the Electrical Engineering Department

California Polytechnic State University, San Luis Obispo

In Partial Fulfillment

of the Requirements for the Degree

Bachelor of Science

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March, 2022

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Abstract

In this work, we dive into the detailed design of a test load or load slammer circuit for DC/DC converters to ensure their correct functioning. This is accomplished through quick variations in frequency, amplitude, and duty cycle of the current being drawn by the converter into the load. Computer simulations of the design were performed using LTSpice and the results show that the load current could be varied per design objectives. Hardware implementation of the design was also conducted and then tested. Results were then compared with the design requirements at lower currents to evaluate the validity of the design. Although good results were obtained from the current design, further improvements would still be needed to improve the overall performance and design of the load slammer circuit.

Chapter 1 – Introduction

Since the establishing of Moore's famous law in the 1960s that the number of components per integrated circuit would double every year, the rule has remained steadfastly correct until now and will seemingly keep its course for the near future as technology is developed further [1]. However, the greater computing and processing capabilities due to the more densely packed transistors comes with many drawbacks, one of which being an increasingly high-power consumption. For example, modern Intel Core processors of the 8th and 9th generations can consume current on the scale of nearly up to 200 amps [2].

Luckily, the field of power electronics has been steadily improving as well, leading to vastly improved converters, inverters, and other such architectures. Of particular note are DC/DC converters due to their high efficiency in changing an input voltage to a specific output voltage [12]. A decrease from the input to output voltage with relatively unchanging power would necessitate an increase in the input to output current. Following this logic, a DC/DC converter would be able to source a significant amount of current with a high enough voltage differential between the input and output. The ability to do this makes DC/DC converters prime candidates for sourcing the current and voltage necessary for many modern devices to function. For high output current applications, a technique called multiphase is most commonly used [13]-[15].

However, circuitry that will be offered on a commercial level needs to be tested for many reasons, particularly regarding functionality, reliability, and safety. As such, circuitry for testing DC/DC converters has been developed to ensure their proper working order, of which there are many different methods and architectures.

Chapter 2 – Background

As DC/DC converters are crucial to many applications, they need to be extremely accurate and reliable to ensure that whatever utilizes them can function as expected. In order to verify their working order, there needs to exist certain methods to test them so that they can be used without fear of failure and, in the case of high-power circuitry, dangerous faults that can lead to injury. Many methods have been explored throughout the lifetime of DC/DC converters, many of which are still prominent today.

One such example is highly advanced software, which is becoming more and more accessible as the simulation of circuitry becomes more advanced and therefore more accurate in predicting the outcomes when tested with hardware. However, one of the main benefits of software is that it can test for edge cases that could potentially damage real circuits without having to run the risk. This can be accomplished using many advanced programs such as MATLAB, Simulink, LabVIEW, and other coding languages, most of which are often used in conjunction with each other to further elevate the level of simulation accuracy [3]. The downside of such methods, however, is that higher order simulations can often take a very long time to run, and may miss certain environmental constraints, such as temperature, if forgotten by the programmer.

Another method is HALT, wherein the converter is put through a series of high-stress tests involving things such as mechanical vibrations, temperature transitions, and electrical stress [4]. This method can provide various statistics and test the hardware to a very high degree. However, HALT testing necessitates a very specific test chamber and software. This makes it a

viable option for products that need to be extensively tested but can prove to be a hindrance for equipment that needs to be tested, but not quite to such a high degree.

For hardware that doesn't need such extensive tests, a more simplistic approach can be followed by simply using an electronic load. Such loads are capable of drawing different current values from the circuit that they're attached to and commercially available in high supplies. Alternatively, they can be built with relative ease, as explored in certain papers on the theory behind and construction of modular electronic loads [5, 6]. Although such loads don't necessarily test as extensively as methods such as HALT, they are much cheaper and are sufficient for many circuits that won't be used in high-stress environments.

There exists a certain offshoot of electronic loads similar to those described above. These loads, colloquially called "load slammers," test the converter by very quickly changing the drawn current [7]. This allows the converter to undergo a series of current tests in a very short period of time, therein allowing the user to quickly ascertain whether the converter that they're testing is faulty to begin with or whether it can go on to more rigorous tests, if necessary. The goal of such a design is to provide a quick and cheap test to the user so that more time- or resource-intensive tests can be bypassed.

For this project, a similar design philosophy to that of the aforementioned "load slammer" is implemented. The end goals are to provide a test circuit for DC/DC converters that can quickly and accurately pull varying currents at steps provided by the user. This allows for an experience where the user can easily test a converter under customizable restraints at low cost and with very little time delay.

Chapter 3: Design Requirements

Before diving into the design of the load slammer, design requirements need to be defined. Because this is a sponsored project by Monolithic Power Systems, many constraints and requirements were given. The load slammer must be able to support 0.5-3.3V and sink 0-100A peak from the DC/DC converter. The current must be translated to a sense voltage range of 0-1V and must be a pulse with adjustable slew rates of 1-100A/us and an adjustable frequency of 0.1-1kHz. The load on pulse duration should be adjustable from 10us-1ms, though there is some leeway in this spec. The load on pulse duration will be limited by the thermals primarily on the power MOSFET, fortunately there is no limit on the size of the load slammer, so we are free to increase the size of the load slammer to improve thermals. The given specifications are best summarized by Figure 3-1.

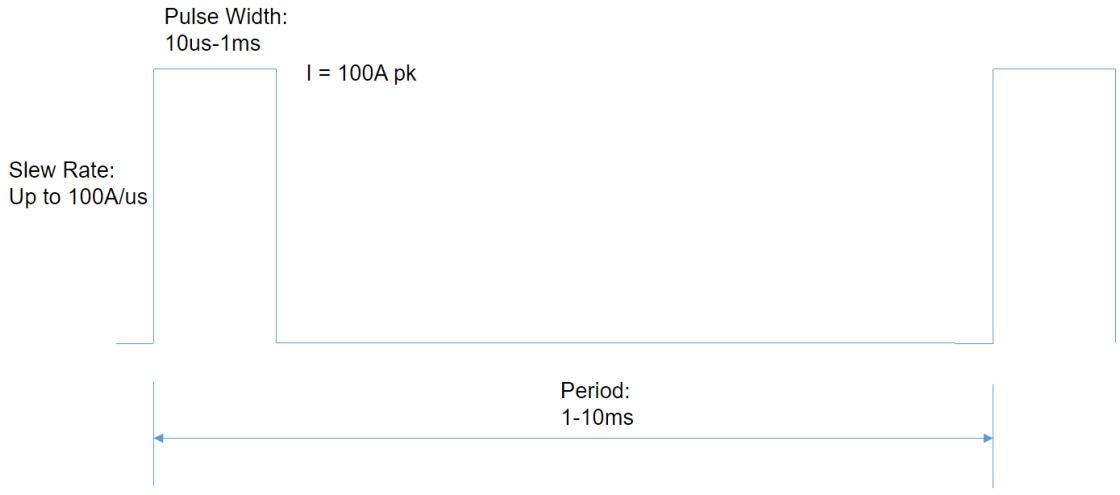

Figure 3- 1: Current Design Requirements

To begin the design process of the load slammer, a functional block diagram is preferred over a system block diagram. It is important to note a system block diagram details specific

implementations, while the functional block diagrams shown in this chapter will feature black boxes detailing required inputs and outputs.

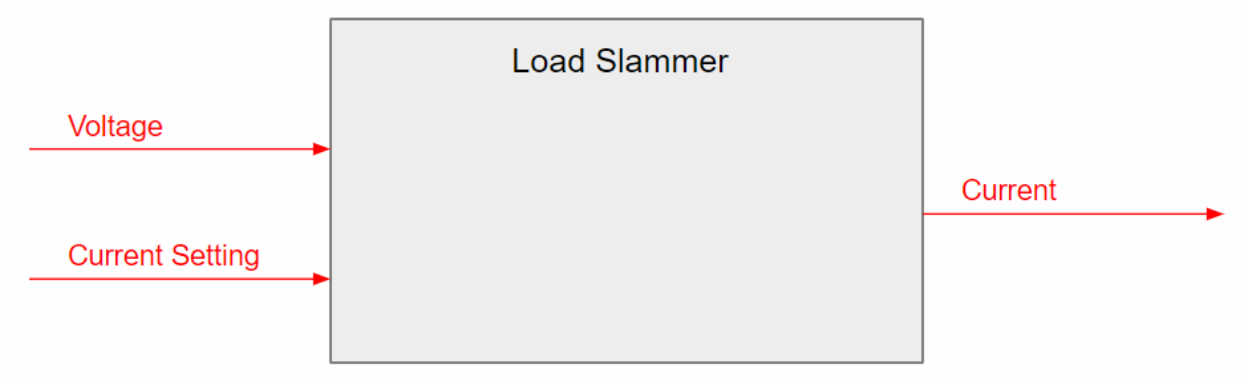

Figure 3- 2: Level 0 Block Diagram for Load Slammer

Figure 3-2 shows how the load slammer will work from a very high-level point of view. At its core, all one has to do is select a current setting within the specs shown in figure 3-1 and then observe the current that is actually drawn from the attached DUT. The voltage shown in figure 3-2 is the external voltage needed to power the system on.

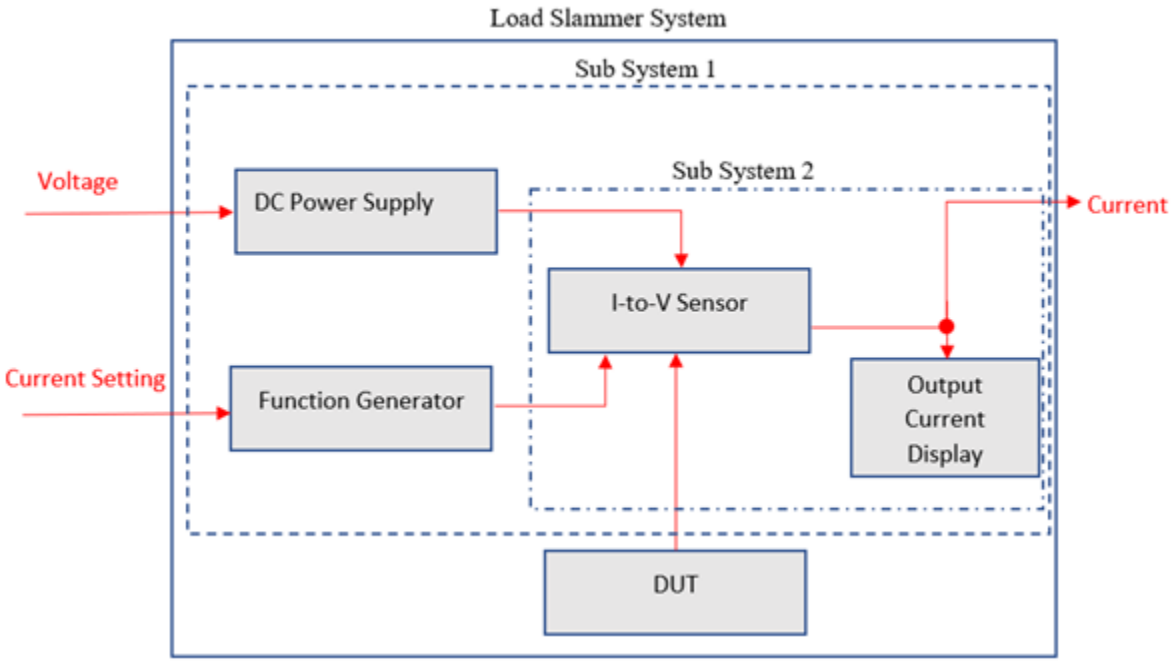

Figure 3- 3: Level 1 Block Diagram for Load Slammer

Figure 3-3 starts to break down the load slammer into different subsystems. The blocks in subsystem 1 are blocks that are required for the project, but we will not be designing. The design detailed in this paper corresponds to what will go in subsystem 2.

As seen in figure 3-3, the current setting is determined by a function generator. This will allow us to vary the input waveform such that it matches the desired waveform seen on figure 3-1. The current setting will then go to a current to voltage sensor, which is powered by a DC power supply. The actual current drawn will be the output of the load slammer, and there is a black box that is needed to display the output current so it can be measured and compared to the desired input.

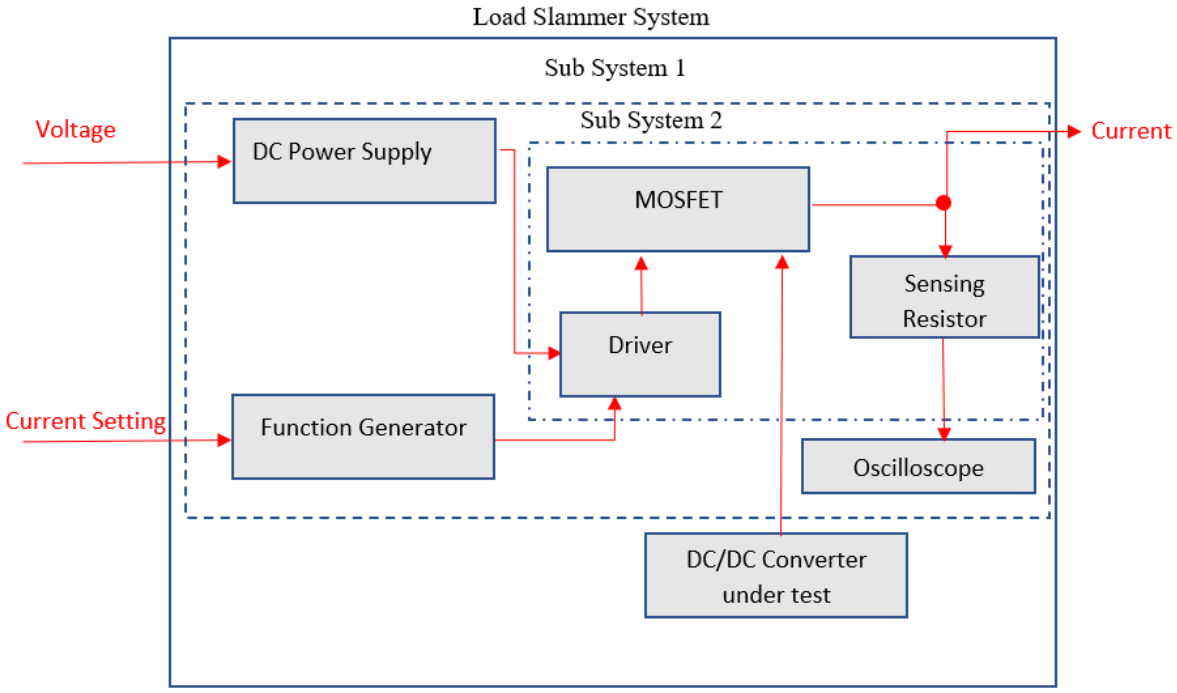

Figure 3- 4: Level 2 Block Diagram for Load Slammer

In the most detailed functional block diagram, it is noted that the DUT that will be used for this project is a DC/DC Converter. The current to voltage sensor black box got expanded to a

MOSFET and driver, which will be in charge of precisely controlling how much current is drawn from the DC/DC converter. The current drawn is then passed through a precise, sensing resistor to create a voltage that can be measured. This voltage will be displayed in an oscilloscope and will be how we measure the accuracy of our load slammer. The measured voltage should look similar to figure 3-5.

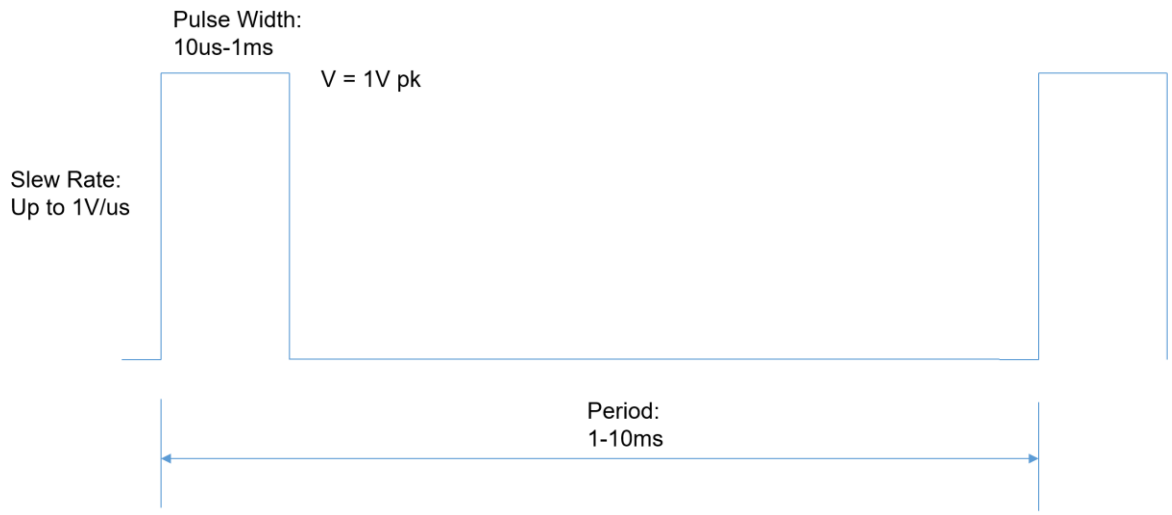

Figure 3- 5: Measurable Project Specs

Chapter 4: Design and Simulation Results

Subsystem 2 of the Load Slammer, as seen on figure 3-3, is the part that will be designed. In the simplest words, subsystem 2 must be a controllable current sink. According to both TI and Maxim, the easiest way to make a precise current sink is by using a transistor, OpAmp, and resistor [8] [9]. This basic topology is shown in figure 4-1.

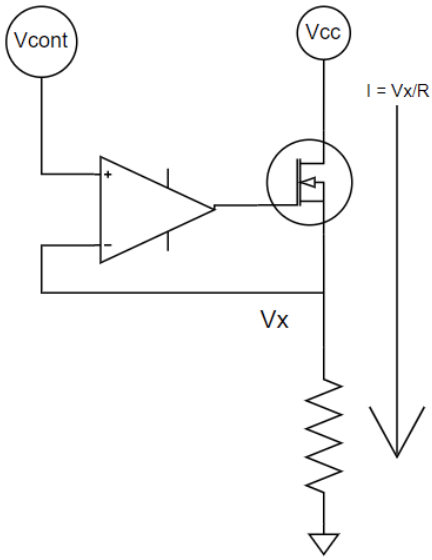

Figure 4- 1: Precise Voltage Controlled Current Sink

By using an OpAmp in an error amplifier configuration, we can control how much voltage shows up across the resistor, this voltage being Vx. When a control voltage signal gets sent to the noninverting input of an OpAmp, the OpAmp will output a signal to the gate of the MOSFET that will drive it to saturation. When the MOSFTET is on, current will rise until Vx matches the input signal, Vcont. Current will sink from Vcc down to ground because the non-

inverting input of the OpAmp has a high input impedance, so current will not want to flow into that node. In summary, this ideal case gives us:

$$I = \frac{V_x}{R} \qquad (4-1)$$

$$V_x = V_{cont} \qquad (4-2)$$

To tie this back to Subsystem 2, Figure 4-2 was created. The control signal will be generated from a Function Generator and the supply voltage from which we will be sinking current is a DC/DC Converter DUT. To measure how much current is being drawn from the DUT, we can measure voltage across the resistor, which should show a waveform similar to figure 3-5.

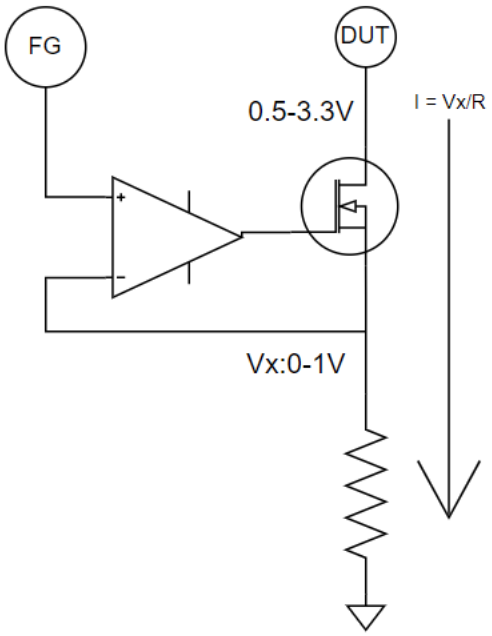

Figure 4- 2: Precise Voltage to Current Sink Version 2

There are two problems with the design in Figure 4-2. The first problem is caused by the required sink current range given. The Load Slammer must be able to pull 100A in pulses, with a worst case scenario of 100A DC, as seen on figure 3-1. Figure 3-5 shows that the output voltage sense current range must be 0-1V, so the value of the resistor should be:

$$R = \frac{V_x}{I} \tag{4-3}$$

$$R = \frac{1V}{100A} = 10m\Omega \tag{4-4}$$

If this is the value of the resistor, then at the worst case the power dissipated through it will be:

$$P_R = I^2 * R \tag{4-5}$$

$$P_R = (100A)^2 * (10m\Omega) = 100W \tag{4-6}$$

Equation 4-6 shows that the resistor will be dissipating 100W! This is far too large of a loss, not only does this destroy efficiency, but it also makes the design more expensive. A resistor with a higher power tolerance and a heat sink would have to be purchased to make this design, furthermore, the PCB size will have to increase to accommodate the heatsink and resistor.

Another problem is caused by the required DUT voltage range given. By applying KVL in the current sink loop the following problem is revealed:

$$V_{DUT} = V_{forward,MOSFET} + V_x \tag{4-7}$$

$$V_x = V_{DUT} + V_{forward,MOSFET} \tag{4-8}$$

Assuming the MOSFET has a very small Rds,on we can estimate:

$$V_x = V_{DUT} \tag{4-9}$$

Equation 4-9 shows that Vx is limited by V_{DUT}. This means that if an input of 1V is sent to the OpAmp, the inverting terminal will only be able to rise to V_{DUT}, and the desired current sunk will not appear. For the given specifications, this limits the design to Vx<0.5V.

To solve the problem seen through equation 4-6, a smaller R must be chosen. If the value of R decreases, the voltage Vx will decrease from 0-1V, which would also solve the problem seen through equation 4-9.

$$R = \frac{P_R}{I^2} \qquad (4-10)$$

The resistor should not be consuming more than 1W, so the largest value possible is:

$$R = \frac{1W}{(100A)^2} = 100\mu\Omega \qquad (4-11)$$

With this new R value, the largest value for Vx becomes:

$$V_x = I * R \qquad (4-12)$$

$$V_x = 100A * 100\mu\Omega = 10mV \qquad (4-13)$$

This fits our constraint of Vx < 0.5V, unfortunately it sacrifices another requirement. As seen on figure 3-5, the design should have a sense voltage range of 0-1V, but this design will only be able to go up to 10mV. Additionally, if Vx can only go up to 10mV, then the way 0-100A is pulled would be by adjusting the output of a Function Generator from 0-10mV. This is a very small signal and is more prone to noise, causing the current sunk to be less accurate. To fix this, an attenuation and amplification stage should be added, as shown on figure 4-3.

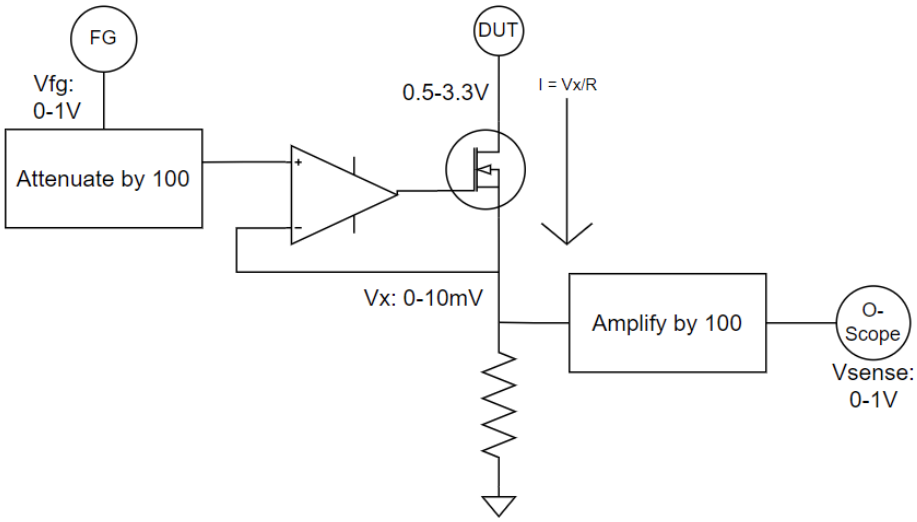

Figure 4- 3: Precise Voltage to Current Sink Version 3

An additional point of concern is having one MOSFET handling all 0-100 Amps. This is too stressing on the MOSFET, so we will add another MOSFET in parallel. MOSFETs have inherit thermal runaway protection, meaning they will evenly balance how much current and heat they experience when in parallel. Paralleled MOSFETs also allow us to reduce the Rdson seen by the circuit, making it more favorable to parallel MOSFETs.

The MOSFET chosen for this project is the IRF2903ZS by Infineon Technologies. This MOSFET is able to handle a continuous current of 75A and a drain-source voltage of 30V, it has a small Rdson of 2.4mΩ, and thanks to its TO-220 package it has a thermal resistance of 0.51°C/W. The larger a MOSFET is, the lower the Rdson can be, however it also leads to a larger parasitic capacitance. This parasitic capacitance is important because it determines how much current needs to be pumped into the MOSFET for it to turn on.

$$I = \frac{\Delta Q}{\Delta t} \qquad (4-14)$$

From the datasheet we know:

$$Q_g = 240\,nC \qquad (4-15)$$

From the requirements illustrated on figures 3-1 and 3-5 we know:

$$\Delta t = 10us\ to\ 1ms \qquad (4-16)$$

So the current the MOSFET requires is:

$$I = 24mA\ to\ 0.24mA \qquad (4-17)$$

Figure 4-4 shows the Safe Operating Area (SOA) of this MOSFET. As seen on figures 3-1 and 3-5, the LoadSlammer will have a pulse of 10us-1ms, with a worst case scenario of DC when pulse width is 1ms and period is 1ms. The LoadSlammer also calls for a drain voltage of 0.5V-3.3V as seen on figure 4-3. The SOA assures us that for the required drain voltage and current support needed, this MOSFET will be able to handle the waveforms going through it.

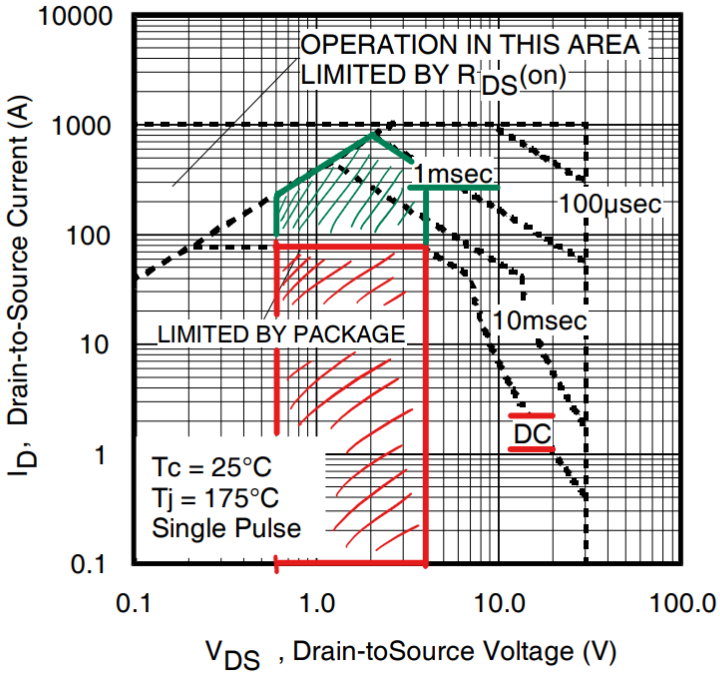

Figure 4- 4: SOA of the IRF2903ZS [10]

Because we plan on having two MOSFETs in parallel, each MOSFET should only bear the burden of 50A, making a max of 75 at worst case scenario acceptable. Unfortunately, having two MOSFETs in parallel also means they will demand more current. Instead of drawing 0.24-24 mA as predicted in equation 4-16, the MOSFETs will draw 0.48-48mA for pulse widths of 1ms–10us.

As seen on figures 3-1 and 3-5, this design must be able to handle a high slew rate of up to 100A/us. Two OpAmps to consider to meet these requirements are the LT1351s and LT1468s. The LT1468 advertises a slew rate of 22v/us and a GBW of 90MHz while the LT1351 offers 200V/us and 3MHz. The Gain bandwidth for both is acceptable since the maximum frequency we plan on operating our load slammer with is 1kHz. What makes the LT1351 special is its ability to drive capacitive loads, an important thing to have considering the parasitic capacitance of MOSFETs, making it our choice for our input and control OpAmps. The control OpAmp, LT1351, is able to supply 12mA with supply voltages of 15V, this means the design will have a hard time powering the MOSFETs during the smaller pulse width cases. The LT1468 is classified as a precision instrument with high accuracy, making it our choice for the output stage amplifier to allow us to have an accurate reading from the sense resistor.

As derived earlier with equation 4-10, the maximum sense resistance we can use is $100\mu\Omega$. This lets us use Vishay's 15W, $100\mu\Omega$ sense resistor, the WSLP3931.

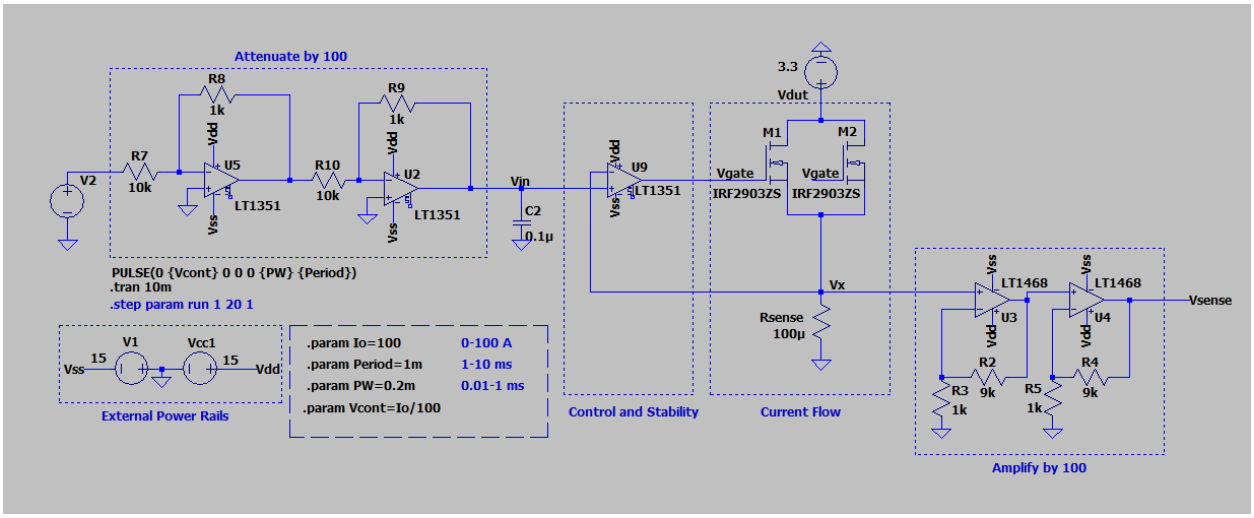

Figure 4- 5: LTSPICE LoadSlammer Version 1

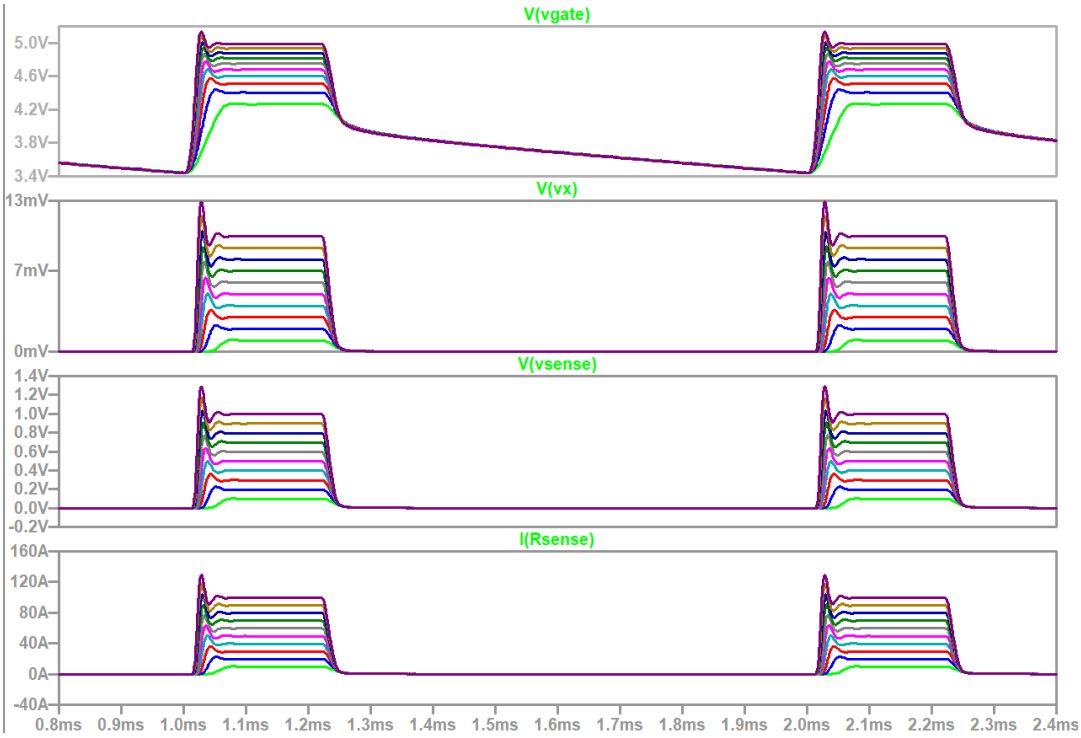

Figure 4- 6: LTSPICE LoadSlammer Version 1: 10-100A Cases

Figure 4-5 shows the LoadSlammer design produces waveforms similar to what is required by figures 3-1 and 3-5. The LT1351 prevents ringing on the square wave because of its ability to drive capacitive loads, but there is a short overshoot that needs to be taken care off. As

required, a current rise of 0-100A leads to a sense voltage from 0-1V. The voltage on the gate of the MOSFET does not go down to zero, which could be a sign that the switch will never turn off and keep conducting. This might result in both MOSFETs experiencing 50A DC, which is safe as seen by figure 4-4. The waveforms for the lower current cases show little overshoot, but take longer to rise up to their correct values, meaning the Slew Rate has been reduced.

OpAmps can source current, but cannot sink it. This means there is a voltage stored by the parasitic capacitance of the MOSFET, leading to the V(vgate) waveform seen on figure 4-6. To solve this, a small resistor can be placed from Gate to Source of the MOSFET.

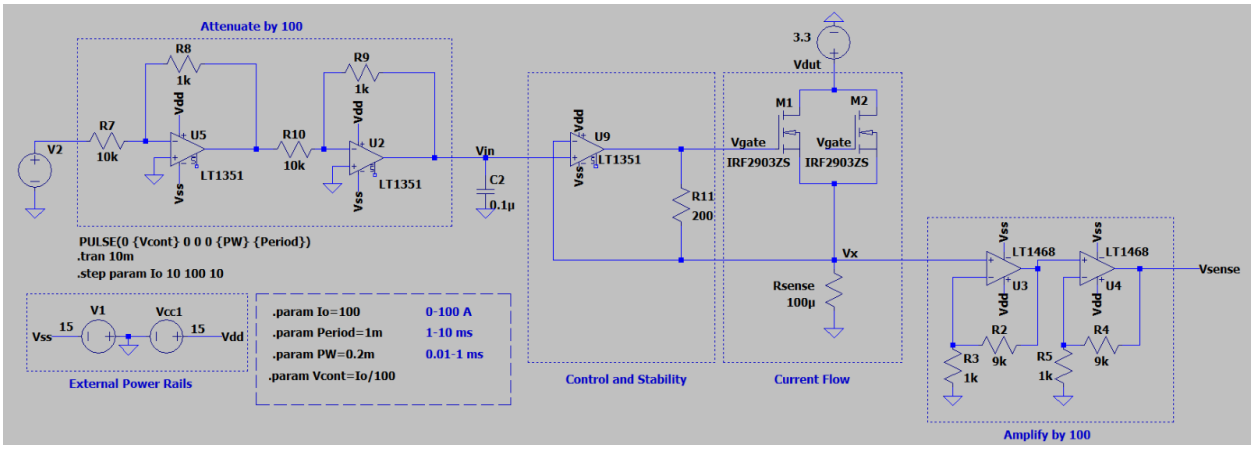

Figure 4- 7: LTSPICE LoadSlammer Version 2

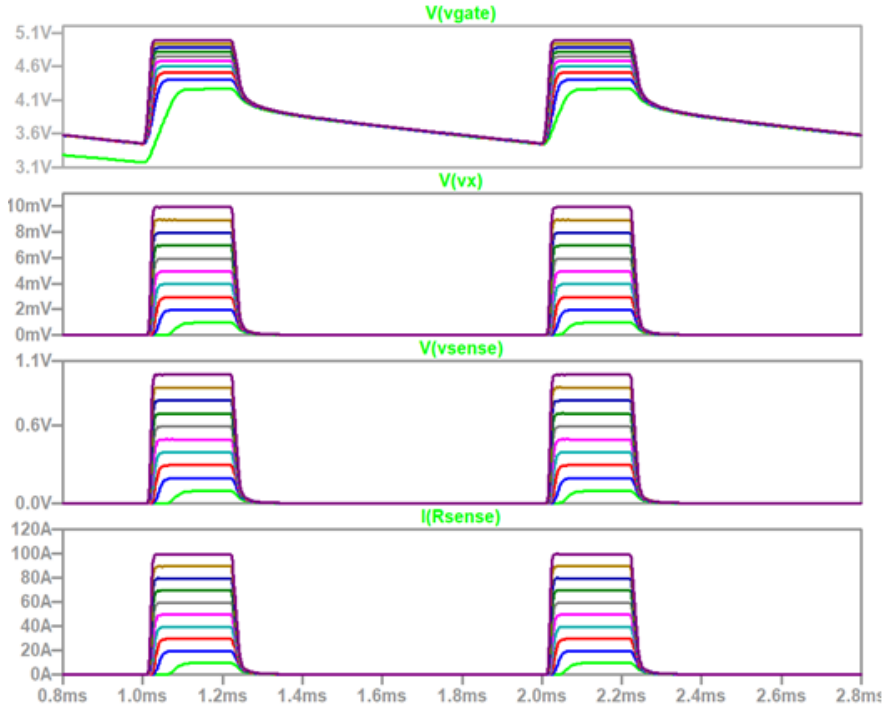

Figure 4- 8: LTSPICE LoadSlammer Version 2: 10-100A Cases

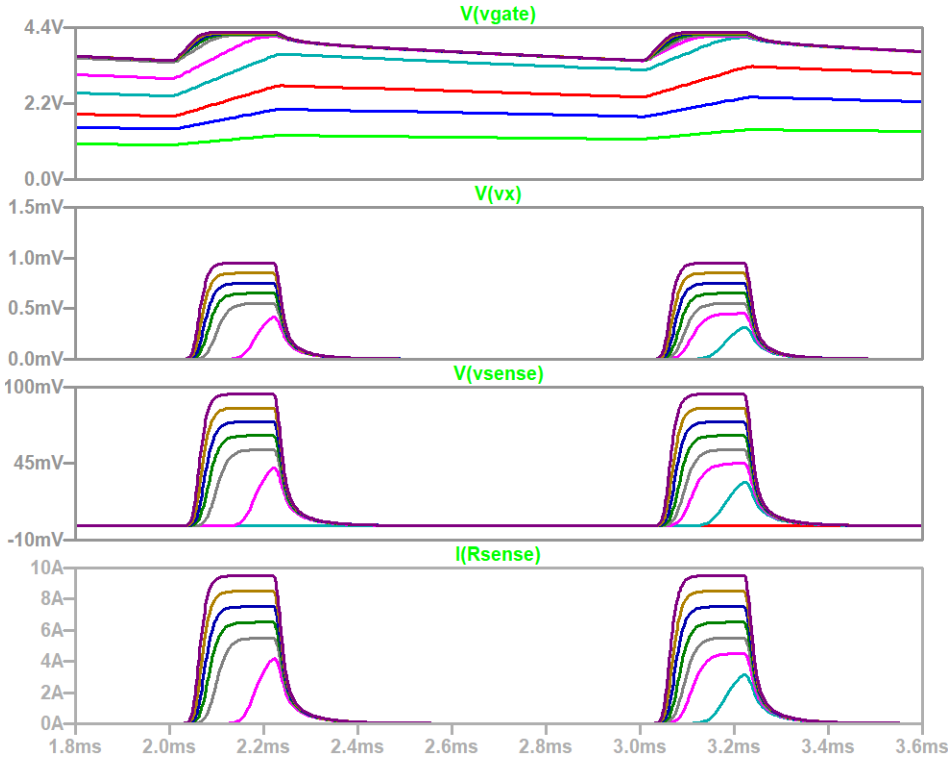

Figure 4- 9: LTSPICE LoadSlammer Version 2: 1-10A Cases

As seen on figure 4-8, the new addition of the resistor has allowed the overshoot to be completely removed. The Gate voltage of the MOSFETs still follows a strange pattern where the signal does not dive down to zero, instead it rises from 4-5 V as current is drawn 10-100A.

While the 10-100A cases look amazing, figure 4-9 shows this design is weak when it comes to anything below 6A. The voltage at the Gate of the MOSFETs for the 0-5A cases does not follow the pattern the other cases show, and as a result the LoadSlammer is incapable of pulling these currents.

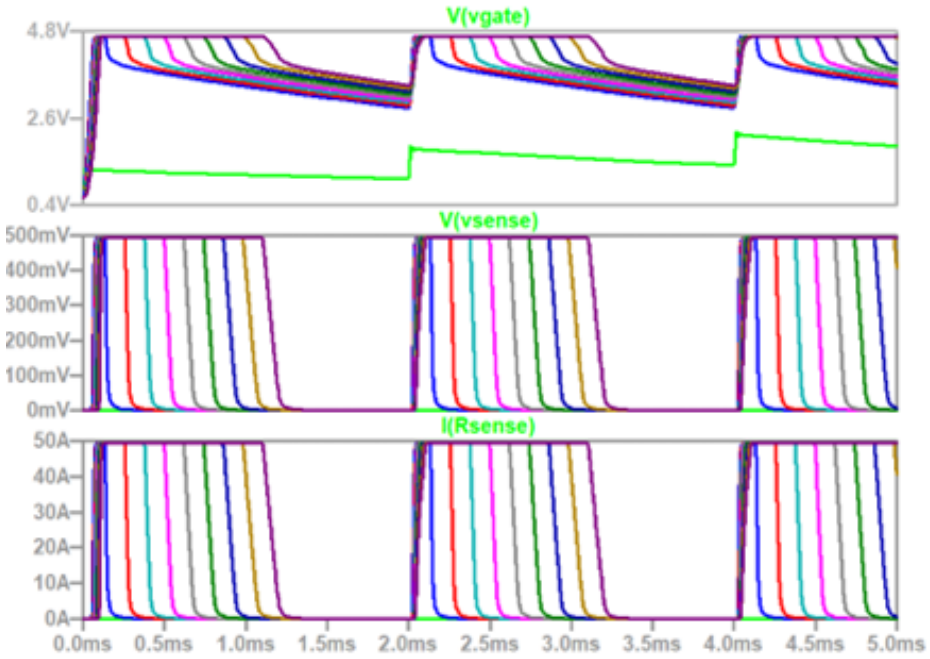

Figure 4- 10: LTSPICE LoadSlammer Version 2: 10us-1ms steps of 110us Cases

Another specification that this design does not meet lies in the pulse width requirements. The design should be able to have a pulse width within the range of 10us to 1ms. Figure 4-10 shows the 10us pulse width (green waveform) does not work, but pulses with 120us and onward do work.

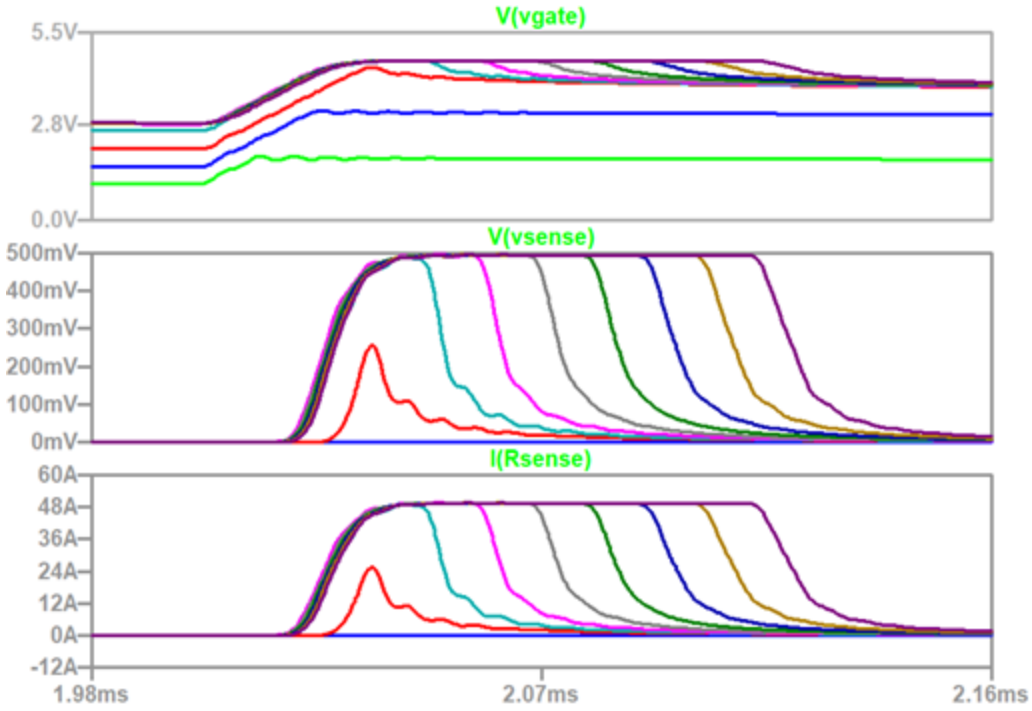

Figure 4- 11: LTSPICE LoadSlammer Version 2: 10us-100us steps of 10us Cases

With figure 4-11 it can be seen the design only works well for pulse widths of 40us (cyan waveform) and over. This makes sense because by using 40us on equation (13) we see that 6mA is demanded by the MOSFET. Having two MOSFETs in parallel means 12mA is needed, which is the maximum amount of current the LT1351 can supply. According to this design and its corresponding simulations, table 4-1 was able to be made.

Table 4- 1: Simulation Results vs Requirements

	Requirements	Simulated Results
Sink Current	0-100A	6-100A
Sense Voltage	0-1V	0-1V
Pulse Width	10us-1ms	40us-1ms
Period	1-10ms	1-10ms
Slew Rate	Up to 100A/us	-Not Tested-
Vout	0.5-3.3V	0.5-3.3V

Chapter 5: Hardware Tests and Results

Figures 4-8 and 4-9 show a square-like waveform that does not settle down to 0 at the gate voltage of the MOSFETs. This is concerning because the lowest voltage the gate sees is about 3.6V, this is within the turn on voltage range of our selected MOSFETs, meaning the MOSFETs might continue to conduct during times we do not want them to conduct. Before spending time and money on a PCB design, we decided it best to test the design using a perfboard. A perfboard is more favorable than a breadboard in our case because of the required high slew-rates and high currents, and the lack of breadboard parasitic capacitance [11].

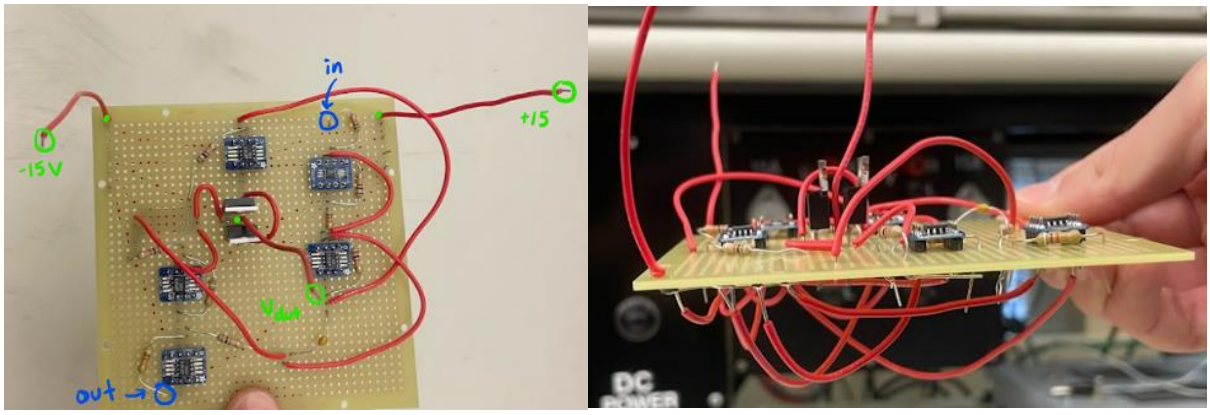

Figure 5- 1: Perfboard Design

To test our design, we used the test setup seen on figure 5-2. All the OpAmp rails were powered by the power supply, the control signal was manually selected with a waveform generator, and the output waveform was measured with an oscilloscope. The DC/DC converter the Load Slammer is meant to test is simulated by the power supply, with it we can choose an output voltage of 0.5-3.3V, however the power supply model in the lab is only able to provide up to 3A. As seen on figure 4-9, our design is not functional for such low currents.

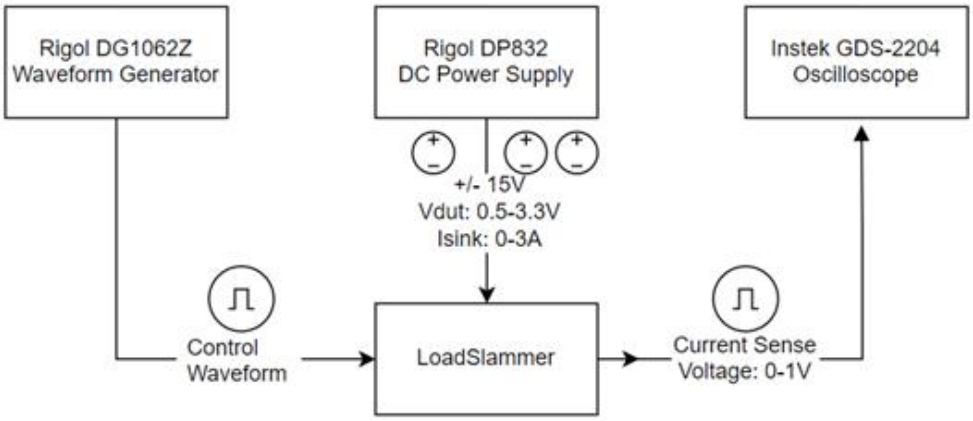

Figure 5- 2: Load Slammer Test Setup

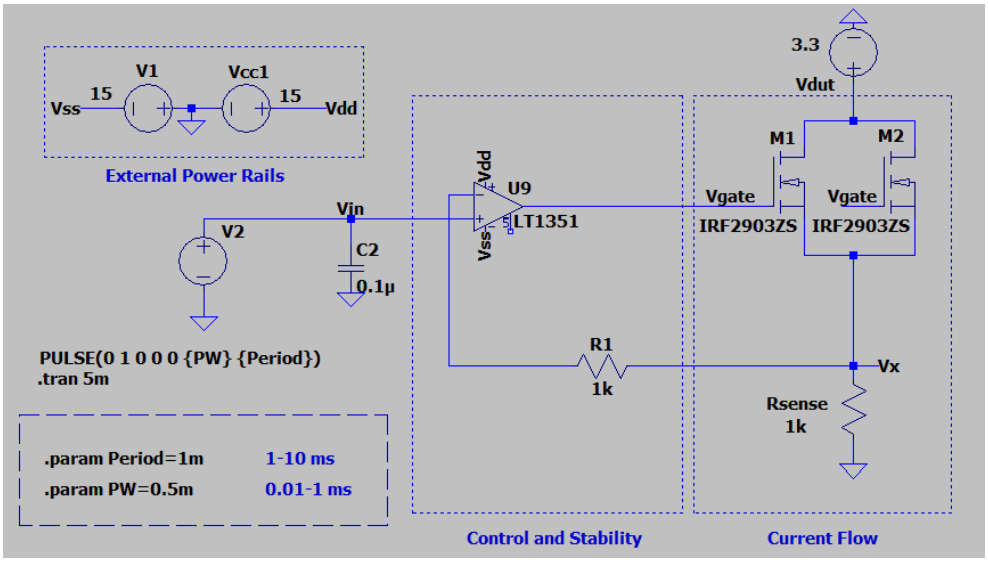

Figure 5- 3: Modified Load Slammer Design

Because we could not test out sinking high currents, we decided to change our Load Slammer design. By implementing figure 5-3, we could test if our design concept works. By inputting a voltage of 0-1V, we will be able to control the current sink of 0-1mA which we will read in an oscilloscope as a voltage signal of 0-1V. Because the sense resistor is higher than before, a 1k resistor is added to the inverting node of the OpAmp, this ensures current does not flow into the OpAmp.

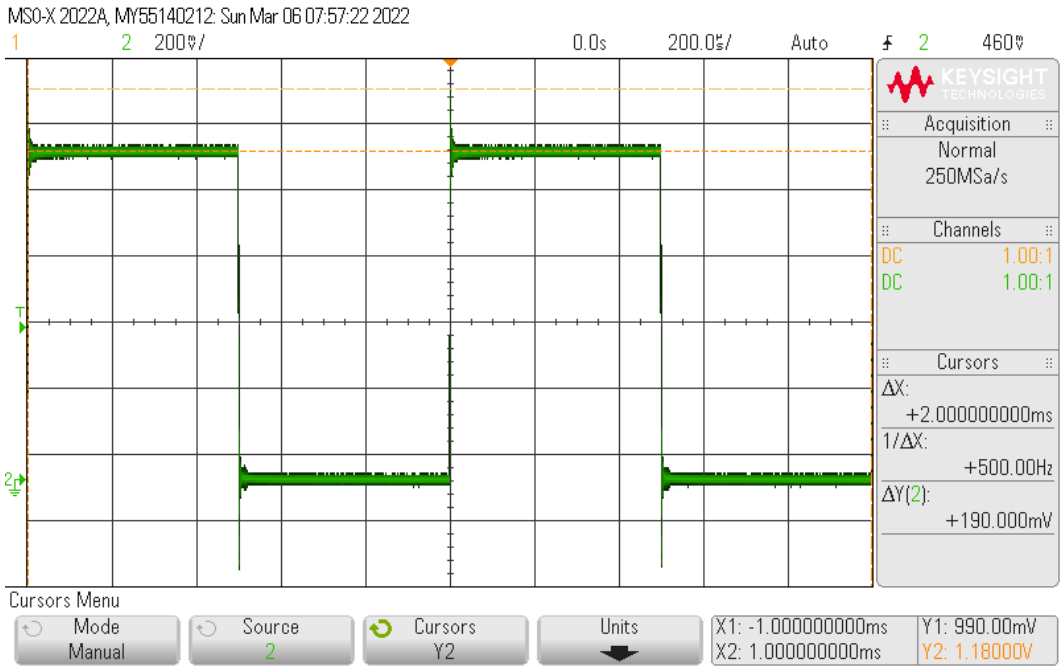

Figure 5- 4: Overshoot 1V input, 50% D, 1kHz, 3.3V drain

Figure 5-4 shows the output sense voltage, which does follow the predicted 0-1V rise. It can also be seen there is a quick overshoot of 0.19V on the peak and bottom of the square wave. This could be because of the lack of Gate-Source resistor in this design.

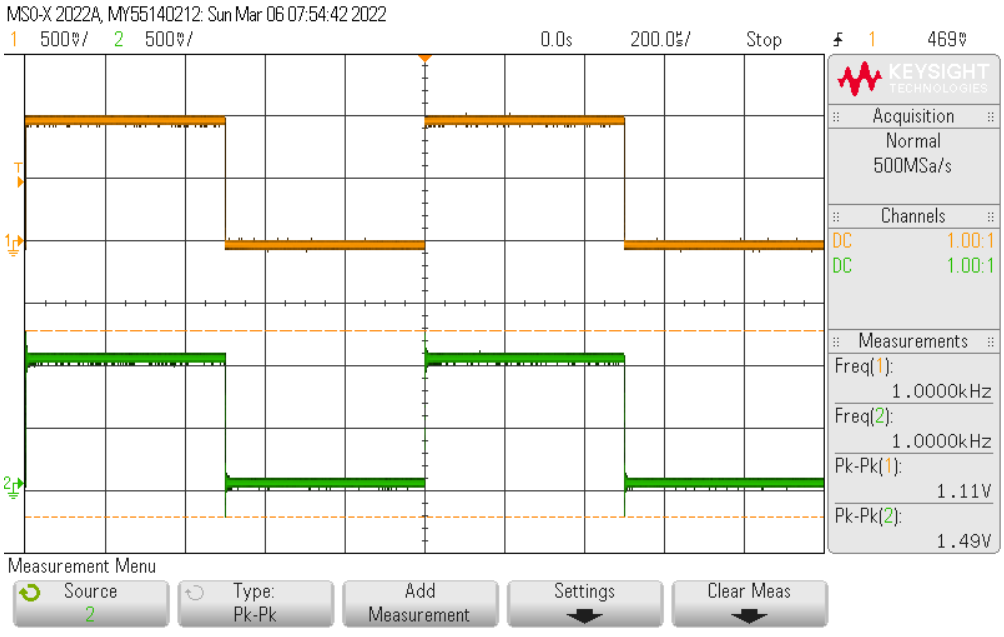

Figure 5- 5: 1V input, 50% D, 1kHz, 3.3V drain case

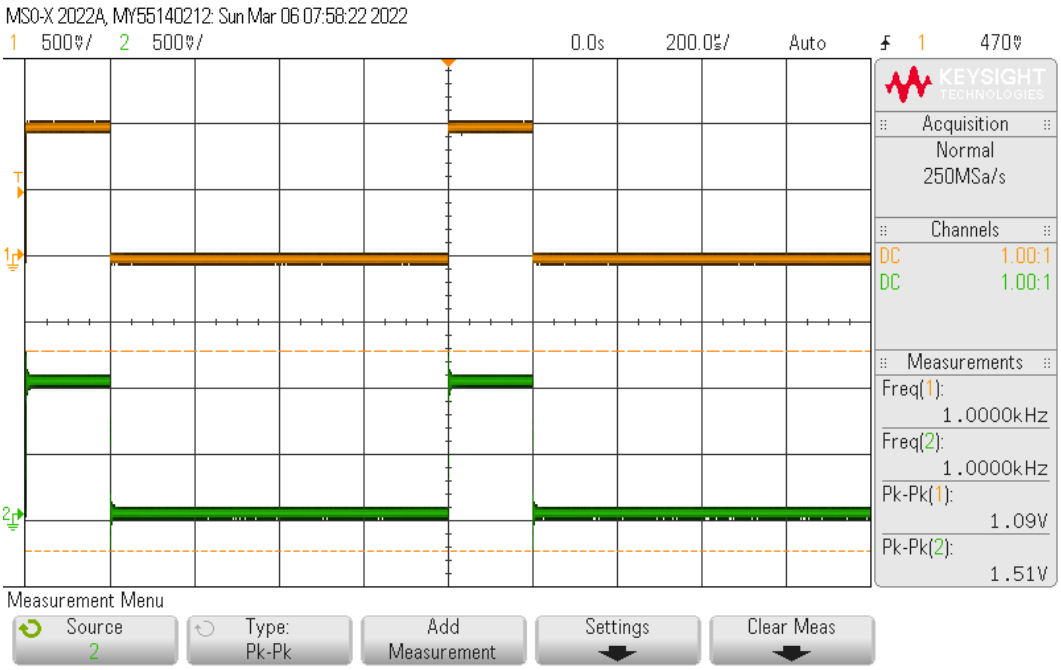

Figure 5- 6: 1V input, 20% D, 1kHz, 3.3V drain case

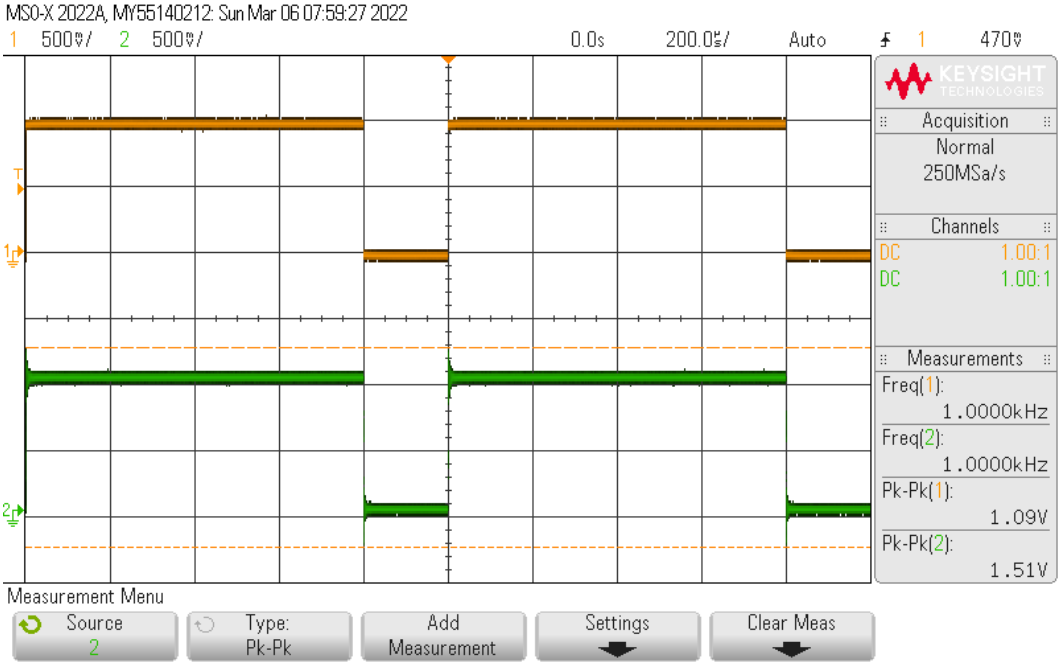

Figure 5- 7: 1V input, 80% D, 1kHz, 3.3V drain case

Figures 5-5 through 5-7 demonstrate the ability of the Load Slammer to accurately follow the input control signal. As the duty cycle of the input control waveform is changed, the output

follows those changes and produces a waveform with the desired profile as shown on figure 3-1 and 3-5.

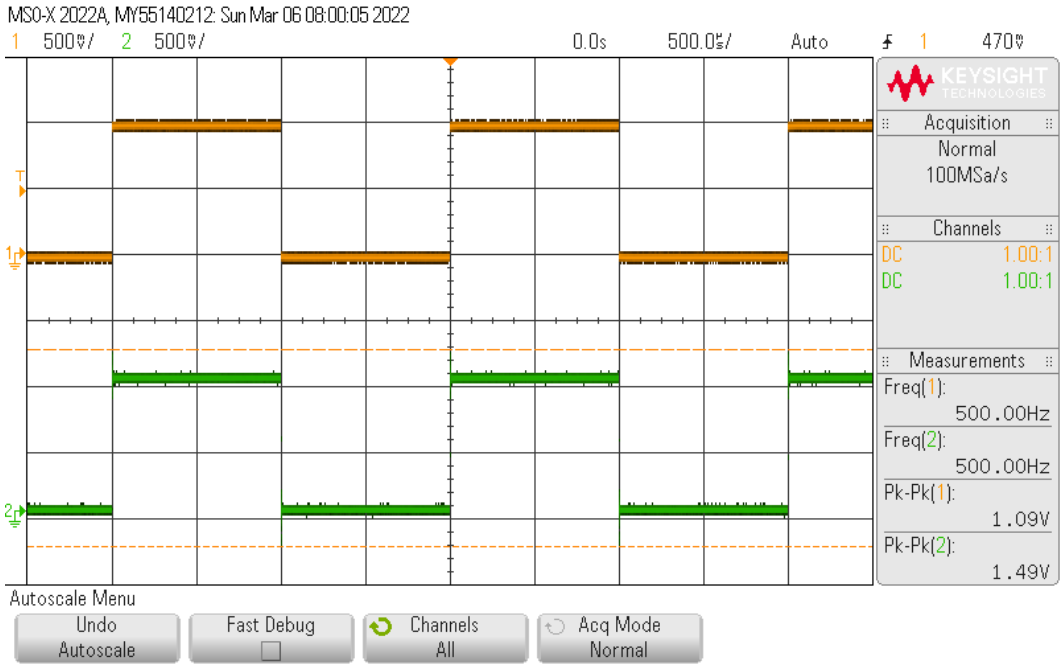

Figure 5- 8: 1V input, 50% D, 500Hz, 3.3V drain case

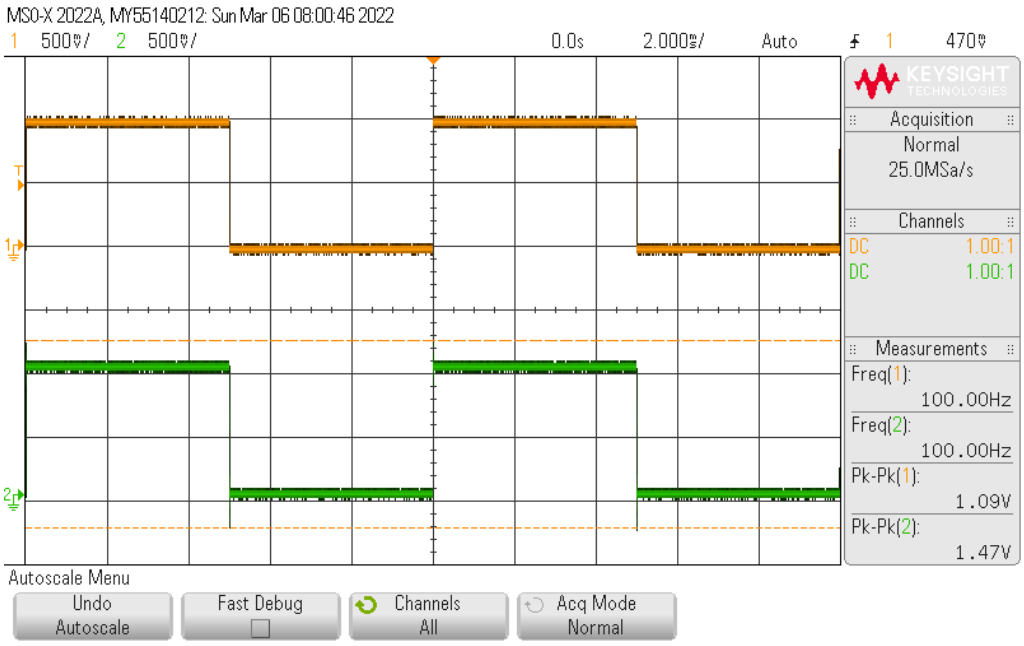

Figure 5- 9: 1V input, 50% D, 100Hz, 3.3V drain case

Figures 5-8 and 5-9 show the output sense voltage can follow the input control voltage, even as the input frequency changes. The lowest frequency required is tested on figure 5-9, and the maximum frequency of 1kHz was shown with figure 5-5.

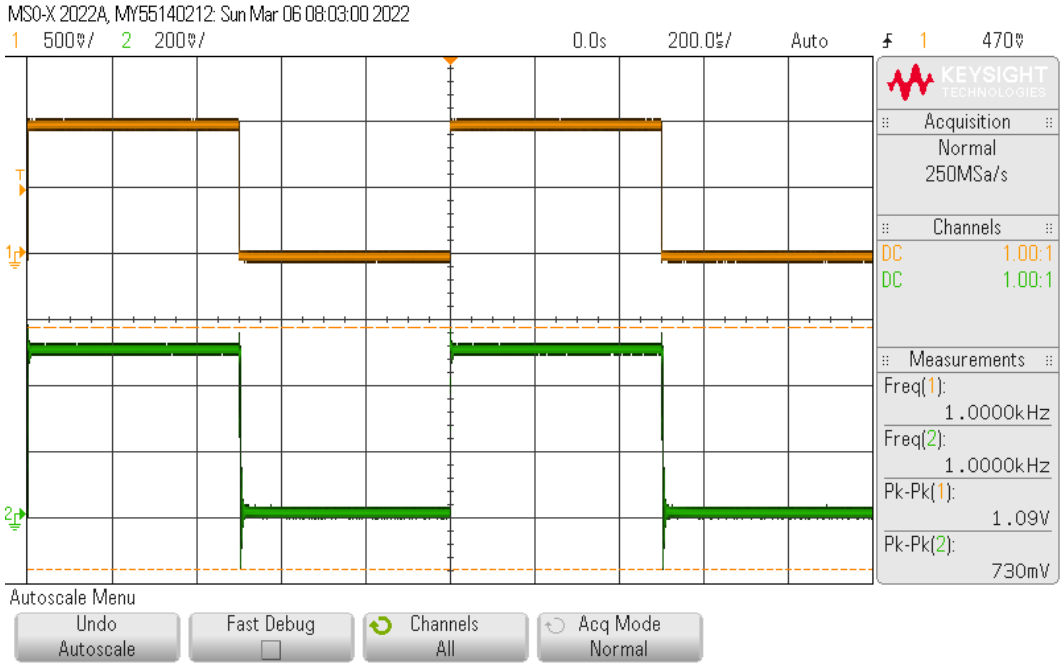

Figure 5- 10: 1V input, 50% D, 1kHz, 0.5V drain case

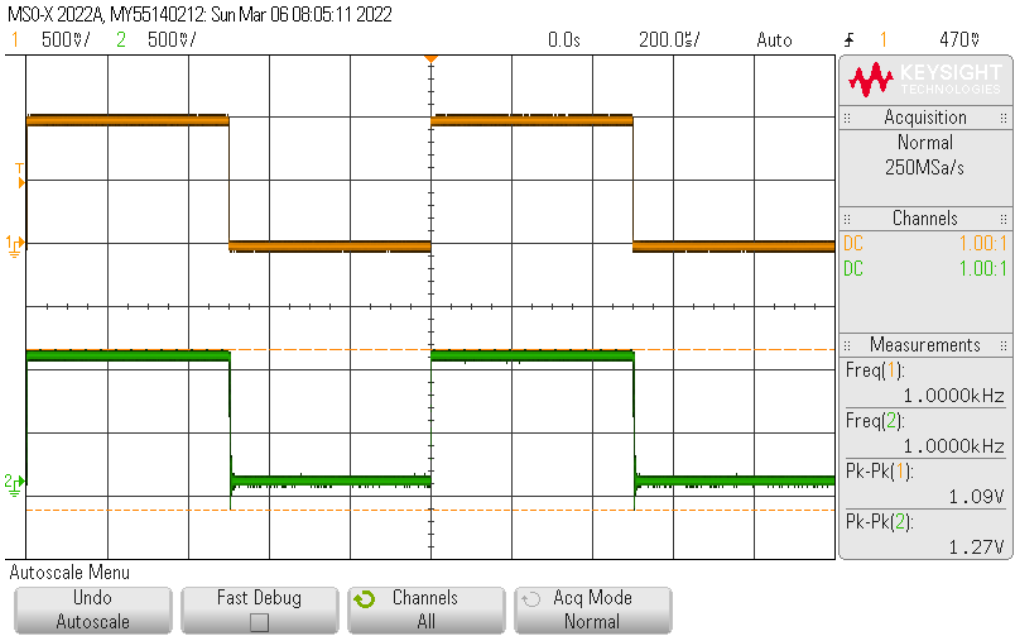

Figure 5- 11: 1V input, 50% D, 1kHz, 1V drain case

With figures 4-10 and 4-11, the effects of the drain voltage are shown. As proved by equation 4-9, the drain voltage of the MOSFET will limit how much the control voltage can be. In figure 5-10, we are sending a 0-1V input waveform as the control waveform, however the output can only rise to about 0.5V. The oscilloscope reads a peak-peak value of 0.73V because it is incorporating the overshoot values, without them the waveform should be no greater than the drain voltage, which is 0.5V in figure 5-10. Figures 5-11 and 5-12 have no problem producing an output that follows a 0-1V input waveform. This is because both figures have a drain voltage of at least 1V.

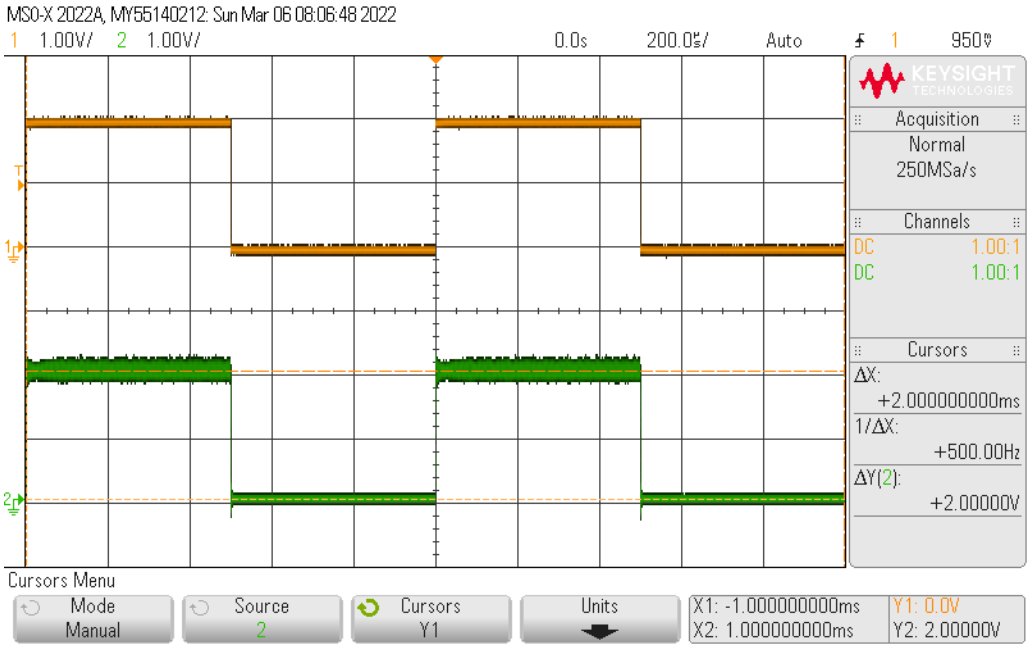

Figure 5- 12: 2V input, 50% D, 1kHz, 3.3V drain case

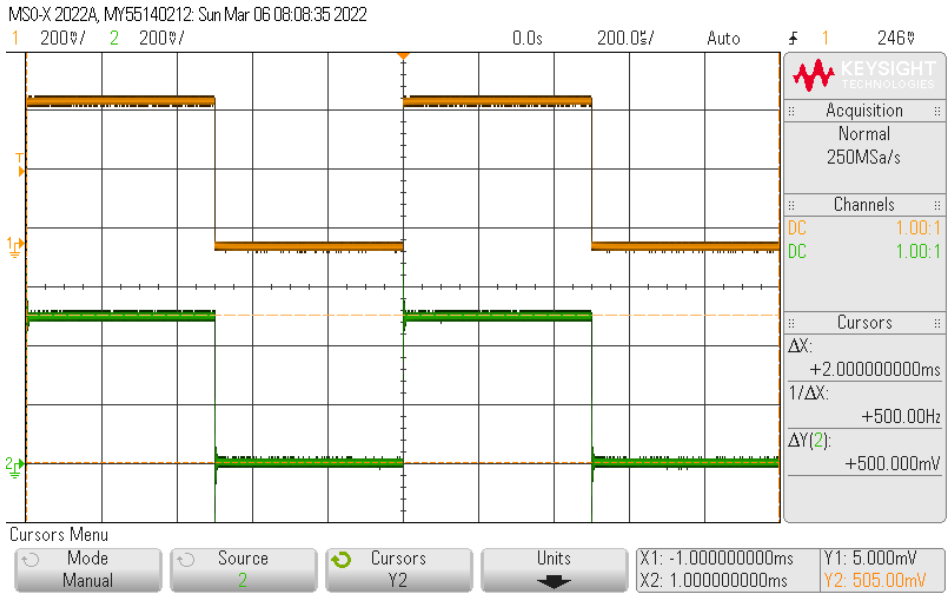

Figure 5- 13: 0.5V input, 50% D, 1kHz, 3.3V drain, overshoot case

Figures 5-12 and 5-13 show a similar effect to figures 5-10 and 5-11. With figures 5-10 and 5-11, the drain voltage was changed while allowing the input control voltage to remain constant. With figures 5-12 and 5-13, the input control voltage waveform is changed, and the output voltage can follow these changes. Again, the output can match the input because for both figures the input voltage does not exceed the drain voltage.

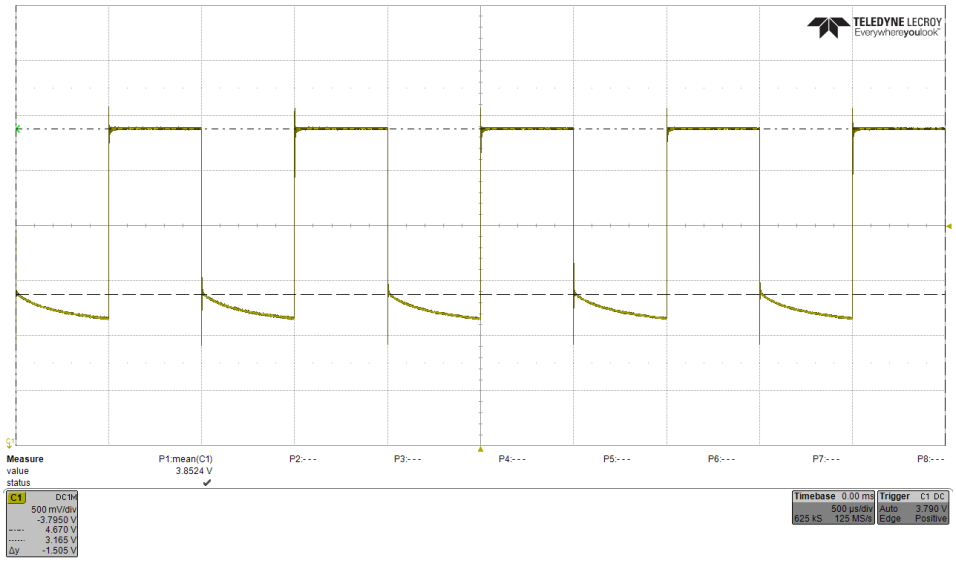

Figure 5- 14: Gate Voltage for 1V input, 50% D, 1kHz, 3.3V drain

Figure 5-14 shows the strange gate voltage seen on simulation occurs in real life. This voltage follows the waveform predicted, with a minimum value of 2.955V. Even though the MOSFET sees 2.955V at the gate, it does stop conducting when the input signal is at 0.

Chapter 6: Conclusion

By using an OpAmp in an error amplifier configuration as a MOSFET driver, a circuit where the output waveform matches the input waveform can be achieved. While we get excellent control over the output waveform, equation 4-14 shows the problems that can arise with the use of an OpAmp as a MOSFET driver. MOSFETs need a current to turn on, not just a voltage, as seen through equation 4-14 and figure 4-11. Another important consideration when designing a load slammer is the range of drain voltage required. As seen on equation 4-9, the drain voltage limits the voltage that is seen across the sense resistor.

To improve the Load Slammer design, a single LT1352 can be used to replace the input stage of two LT1351s, since the LT1352 contains two LT1351s inside it. The OpAmp MOSFET driver should also be replaced with a better OpAmp or a MOSFET driver IC. With a MOSFET driver IC, current will be able to quickly source and sink from the IC, thus fixing the strange MOSFET gate voltage seen throughout the report. A challenge with the MOSFTET gate driver IC would be finding a way to accurately control the output waveform to match the input waveform.

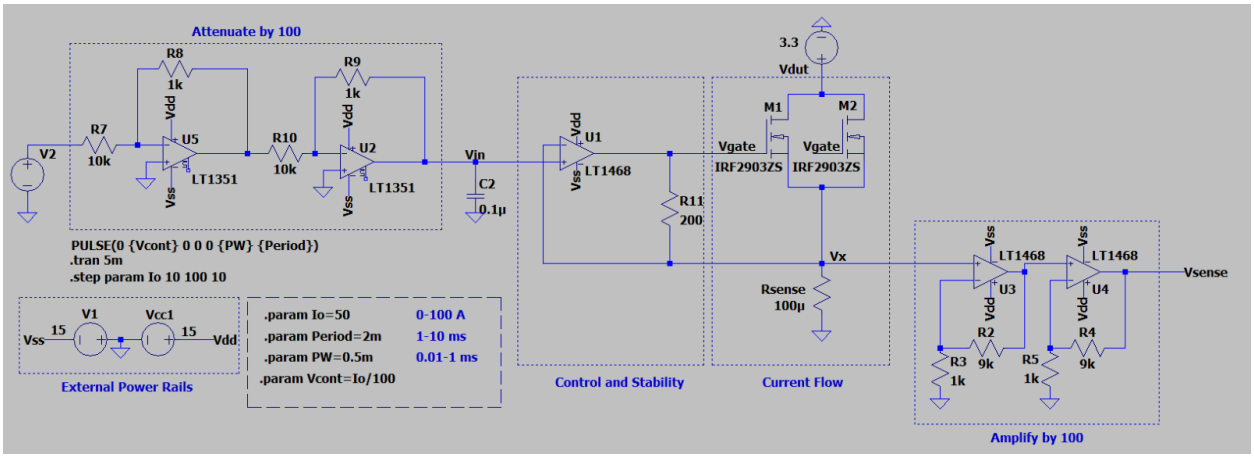

Figure 6- 1: Improved Load Slammer Design

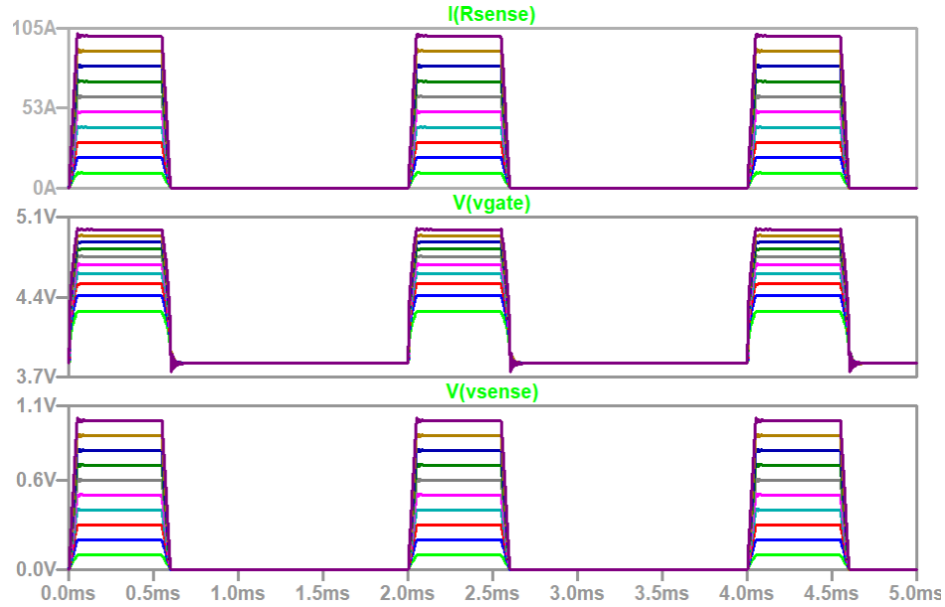

Figure 6- 2: LTSPICE LoadSlammer Version 3: 10-100A Cases

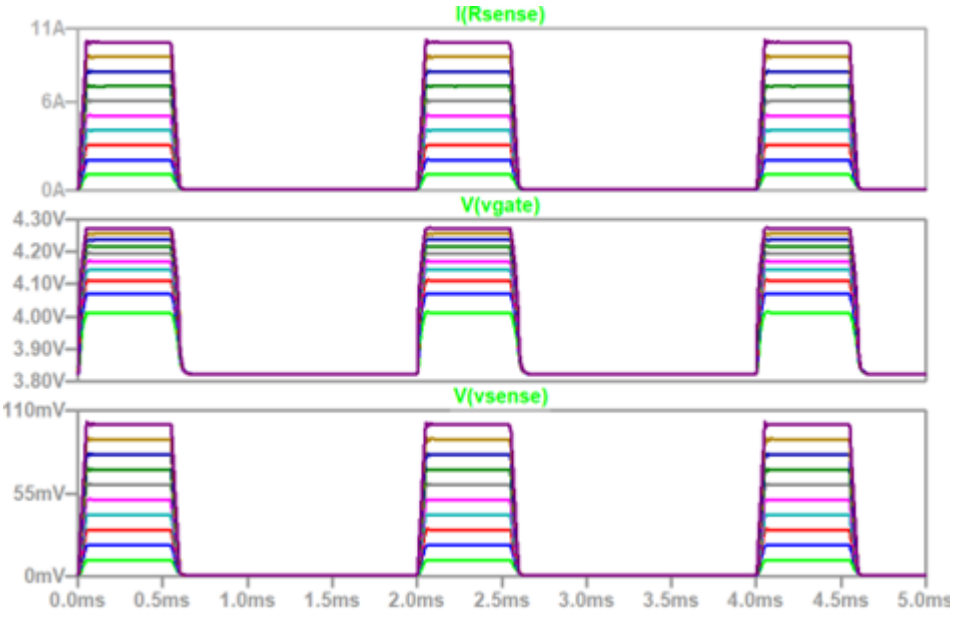

Figure 6- 3: LTSPICE LoadSlammer Version 3: 1-10A Cases

Figure 6-1 shows a new Load Slammer design, where the OpAmp gate driver controller is changed from the LT1351 to the LT1468. With this change, the current waveforms now seem to work for all 0-100A cases, as shown by figure 6-2 and 6-3. This design would be able to be

tested in the lab, since it provides clear waveforms for 0-3A cases, unlike the older design. It should be noted that the LT1468 supplies less current than the LT1351, so having all the current amplitude cases work would sacrifice more of the pulse width requirements.

More research needs to be done to select a better gate driver, whether it be a gate-driver IC or an OpAmp, in order to successfully meet all requirements shown on figure 3-1 and 3-5. Further research also needs to be done on the occurrence of the strange gate voltage and why it always seems to not go down to 0. Even with the new design, figures 6-2 and 6-3 show a gate voltage that does not go down to zero but follows a clean square-wave unlike before.

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Appendix A – Analysis of Senior Project Design

I. Summary of Functional Requirements

The circuit designed in this project acts as a variable load to test DC/DC converters. The user inputs a wave which then determines the amount of current drawn from the device under testing (DUT). The project is capable of drawing 0 to 100 amps of current with a slew rate between 1 and 100 amps per microsecond and an input voltage from the DUT of anywhere between 0.5 and 3.3 volts. The circuit functions with input waveforms anywhere between 100 and 1000 Hertz.

II. Primary Constraints

This project runs into many constraints that are difficult to design around. First, the device that the circuit is loading is more often than not a switching DC/DC converter. This generates lots of noise that may negatively influence control circuitry, which is often small signals. This will require the use of a power ground and signal ground. Furthermore, the maximum current the system will output is 100 amps, which will generate lots of heat, making temperature control and heat dissipation a vital portion of the circuitry. In addition, many of the constraints from the project sponsor are in ranges, meaning that there are a lot of variables that need to be accounted for in design. Finally, the size isn't constrained which may lead to bigger and more expensive parts being used. If not controlled carefully, the cost per device could easily start to add up.

III. Economic

The most significant impact that this project holds is on human capital. Similar circuits have already been built to test equipment more rigorously, but the sponsoring of this project allows for the student team to develop skills in teamwork, design, simulation, testing, verification, and documentation. Moving forward, the students involved in this project will be more capable engineers that will be helpful in the workplace both as leaders and as team members. They will be able to go from a project definition to a tested and verified circuit due to the experience garnered within this project, which is invaluable to any engineer and the company or organization that hires them.

The real capital also plays a large role. Completing the circuits in this project requires simulation tools as well as advanced lab equipment such as oscilloscopes and function generators. Such tools can end up being quite expensive, but the costs are abated to some extent by the ability to use Cal Poly's electronics labs to test the circuits.

Financial capital is significant as well, as money is needed to buy the parts and PCBs and to pay the students involved. This project is also being developed in a silicon shortage, which may increase the price due to rising prices of components. However, the project's completion results in a variable load that is much cheaper than many that are commercially available, which can cost $1500 or more [1]. If sold, the circuit may be able to generate a decent profit, therein returning some capital back to the company.

Finally, natural capital can play a large role. As mentioned above, the depletion and/or over-consumption of natural resources have a significant impact on the ability to procure the parts necessary to carry out the project in full. On the same note, the completion of this project

relies on these resources, therein contributing to their shortage itself. However, the goal of this project is to test circuitry in order to ensure its capabilities before mass market consumption. If this goal is achieved then the products that are tested using the project will ideally be more efficient, thus helping to reduce the impact on the environment.

It's worth noting that the product's life cycle may contribute quite heavily to the financial and natural capital. Its use of high currents may lead to significant wear and tear, meaning that the project will have to be replaced after two to three years of use. This means that there will have to be more products manufactured, but that in itself will generate further profit if they are sold commercially. However, the disposing of these products will impact the environment, and disposing of them safely may cost the company time and/or money.

IV. If Manufactured on a Commercial Basis

As the electronics industry grows, more and more products are required to test and verify circuitry that companies wish to produce and sell. As mentioned above, electronic loads can also be incredibly expensive. Therefore, if this project was meant to be widely sold as a cheap alternative to many other commercially available electronic loads, then it may be a conservative estimate to say that 1000 units would be sold in a year. Considering the usage of high-power components and PCBs, the cost to manufacture one device would likely be between $40 and $75. If they were to be sold for $100, then that could lead to a yearly profit of $25,000 to $60,000.

However, both paying the students as well as the cost of using factories or other such manufacturing plants to produce the devices can contribute quite heavily too. Assuming that the students work for 100 hours each at an agreed upon $20 per hour, their labor cost alone is

$4,000. Furthermore, the costs to maintain a factory and its workers can be significant. However, since the manufacturer of the device will likely already have modes of production in place, the costs of making it mass production may actually be more sustainable in the long run than producing the product in small quantities.

The product's life cycle is expected to be between two and three years due to wear and tear acquired from high current and high temperature operating conditions. Therefore, it can be expected that there will be a surge in purchases every two to three years. Disposing of the product in a sustainable fashion may also cost money, but the amount should be negligible.

V. Environmental

The construction of circuits inherently affects the environment negatively due to the construction, processing, and shipping of parts. The parts used for this project will include plastics, metals, and semiconductors. The most damaging of these will be the plastics, as they degrade poorly and actively damage the environment. In addition, the development of PCBs requires excessive chemical usage which also contributes to pollution. Shipping materials internationally also requires fuel use regardless of airplane or ship usage. The generation of electricity is also unsustainable in most locations. In California, where the product will be designed and tested, the majority of electricity is still generated through the burning of natural gas [2]. The product also has an expected life cycle of two to three years, meaning that the devices will have to be disposed of over that period of time. If not properly down, this could be a waste of reusable components or materials.

However, this project can also contribute positively to the environment. Through the testing of DC/DC converters, our project may inspire more efficient designs or catch fatal design

flaws before products reach mass market, meaning that these products may make a smaller environmental footprint than they may have otherwise. Furthermore, through the use of RoHS compliant components and lead-free solder are steps that are being taken to lessen the impact of this project on the environment.

VI. Manufacturability

Once properly designed, tested, and verified, the project will be able to transition to mass production quite easily. The construction of the product involves producing a PCB and placing parts on it, which is already commonly done by most large companies in the electronics industry. However, the circuit uses a lot of current at its maximum setting which will generate a lot of heat and thus require heat dissipation. Parts that dissipate heat are often either large or screwed onto compatible parts, which may require them to be individually assembled.

VII. Sustainability

This project should easily accomplish both the economic and social aspects of the "triple bottom line" of sustainability, which is composed of economic, social, and environmental requirements. As its goal is to help test circuitry that will likely be implemented in projects that are oriented to distributing power in a quicker and more efficient way, it therefore contributes to both public well-being as well as reducing costs.

However, the use of circuitry that involves plastics, metals, and semiconductors is inherently bad for the environment. Steps can be taken to reduce the impact through using RoHS compliant components and lead-free solder, thereby reducing some of the stress and benefiting the environment. Furthermore, the project should allow for more efficient circuits to be built, which would also help to reduce the stress on the ecosystem.

VIII. Ethical

In accordance with the IEEE Code of Ethics [3], the project is being designed as well as possible and its goal is to better the lives of the general public. The project was built with utilitarianism in mind, therefore hoping to contribute to the greater good. In the design process, much criticism was listened to and acted upon in order to make the project as good as possible. The users' manual included with the project will outline the safety risks involved with operating at such high currents and will thus uphold safety standards.

The students involved with the project have striven not to accept any bribes or break any laws, therefore upholding the legal and moral integrity of the project itself. However, the end product could be sold commercially, meaning it could be used to test converters that will go on to be used in violent products, such as guidance systems for missiles or other such military applications. Furthermore, the development of this project uses vital components that are in short supply due to a shortage of silicon in the current marketplace. As such, the parts that went towards the development of the end product may have been better used in the development of products that directly aid the public, such as medical equipment.

IX. Health and Safety

Because the project deals with currents of up to 100 amps, misuse could lead to serious injury. The project aims to abate this concern by including a users' manual so that the user can avoid using the module in a dangerous fashion. Furthermore, over-current and over-voltage protections will be put in place to ensure that the circuit does not operate beyond the expected scope and in more dangerous voltage and current areas.

Another concern is the heat that the project will have to dissipate. The usage of such high current will generate an enormous amount of heat, which will then be moved to heat sinks in the circuit. These sinks will become very hot as the circuit is used, which may burn a person if they touch them after continued use. As such, there will be an enclosure in place so that one cannot easily touch the heat sinking components and a warning in the users' manual.

X. Social and Political

This project has many stakeholders in both a direct and indirect fashion. The main stakeholders are the company that is sponsoring it and the students designing it. The company is paying the students, which directly benefits them immediately. Furthermore, the skills imparted on the students, such as problem solving, circuit design, documentation, and project planning will contribute to their development and benefit them in the long run.

As for the company involved, if the product that is made is sold then the company can generate profit depending on the cost per unit and the price that is set. Based on the price points outlined in III, the company could see profits of tens of thousands of dollars per year. Selling such a product will also boost the product portfolio of the company and allow them to enter the electronic load market.

The manufacturing of electronics, however, is environmentally unsustainable. Not only does the production and shipping of parts and components use fuels and materials that are non-renewable, but companies that produce parts are often taxed for their carbon footprint in certain countries. Seeking to save money, this can drive companies to buy products from or produce products in countries that have a lower carbon tax [4], resulting in disproportionate emissions in those areas. This can cause select locations to experience the drawbacks of the pollution involved

with electronics manufacturing much more severely than the locations where companies are based.

XI. Development

Completion of the project requires skills in designing the circuitry involved, simulating said circuitry, building the circuits, and then testing and verifying their working order. This involves the use of OrCAD software, which is not often learned during the curriculum offered by Cal Poly. The use of heat sinks is also not often emphasized in coursework, so the application of the heat dissipation circuitry had to be learned in the course of the project. Furthermore, the testing of heat sink capabilities through the use of an infrared thermal imaging camera is a new concept as well. Finally, is PCB design, which is taught very briefly. Good design practices had to be learned through advising with professors and other such resources.

Appendix B – Project Timelines and Milestones

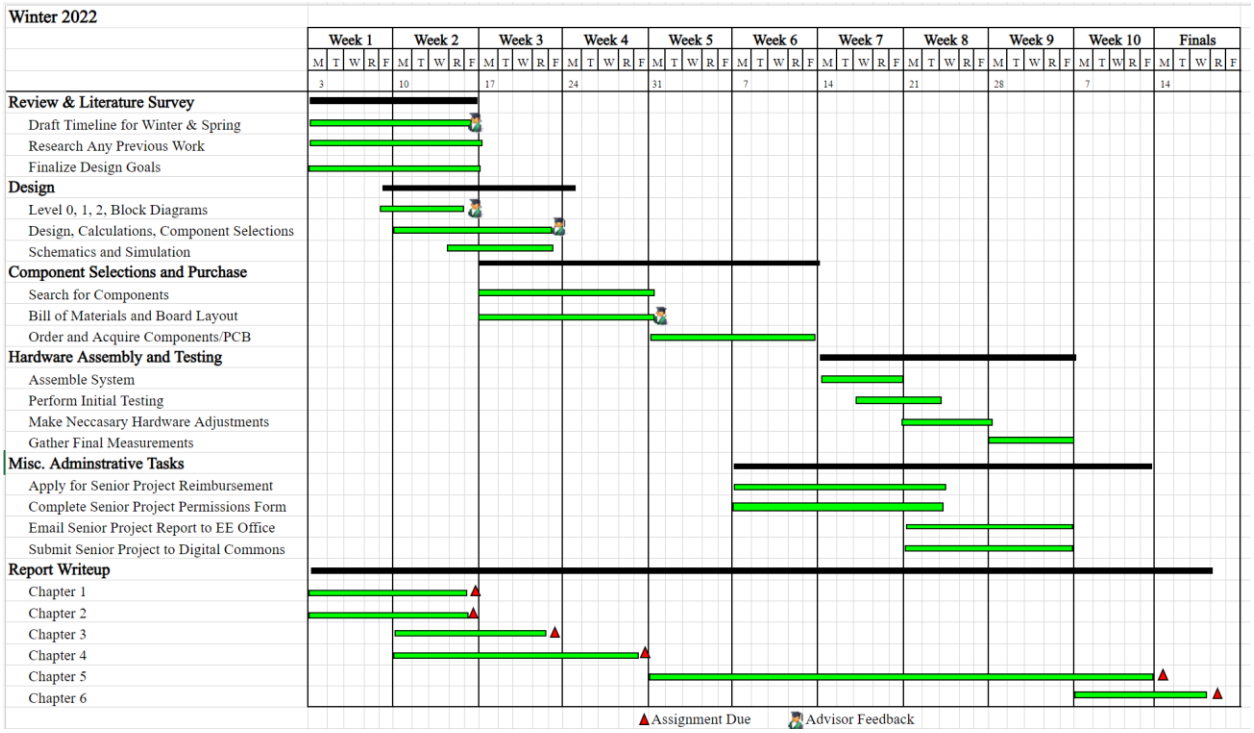

Figure B- 1: Senior project timeline

Appendix C – Bill of Materials

Table C-1: Bill of materials for the updated project, as seen in Figure 6-1

Index	Quantity	Part Number	Manufacturer Part Number	Description	Unit Price	Extended Price USD
1	2	LT1351CMS8#TRPBFCT-ND	LT1351CMS8#TRPBF	IC VOLTAGE FEEDBACK 1 CIRC 8MSOP	$7.59	$15.18
2	3	505-LT1468IDD#PBF-ND	LT1468IDD#PBF	IC OPAMP GP 1 CIRCUIT 8DFN	$9.94	$29.82
3	2	IRF2903ZPBF-ND	IRF2903ZPBF	MOSFET N-CH 30V 75A TO220AB	$1.95	$3.90
4	1	541-10366-1-ND	WSLP5931L1000FEA	RES 100 UOHM 1% 15W 5931	$2.97	$2.97
5	1	273-KDV08FR200ETCT-ND	KDV08FR200ET	RES 0.2 OHM 1% 1/4W 0805	$0.29	$0.29
6	2	RNCP0805FTD10K0CT-ND	RNCP0805FTD10K0	RES 10K OHM 1% 1/4W 0805	$0.10	$0.20
7	4	RNCP0805FTD1K00CT-ND	RNCP0805FTD1K00	RES 1K OHM 1% 1/4W 0805	$0.10	$0.40
8	2	738-RMCF0805FT9K10CT-ND	RMCF0805FT9K10	RES 9.1K OHM 1% 1/8W 0805	$0.10	$0.20
9	1	PCF1126CT-ND	ECP-U1C104MA5	CAP FILM 0.1UF 20% 16VDC 0805	$0.70	$0.70
					Total Price	$53.66