The Design, Characterization, and Testing of the CRYO ASIC Front End Motherboard for the Deep Underground Neutrino Experiment

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Dedicated to all of the ice cream made via excess liquid nitrogen

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Abstract

The Deep Underground Neutrino Experiment is currently in its design and testing stages where two sets of detectors will be used, 1300 km apart. The Far Detector will be the largest liquid argon neutrino detector ever built, and will incorporate 4 separate modules, each containing 10 kilotons of liquid argon. The electronics internal to these modules make use of wire planes that interface to a Front End Motherboard. Here we design a potential board which incorporates the CRYO ASIC.[18] We discuss the testing of this design, as well as the revisions made for the most recent version. We present the noise measurements across the electronics and all input channels and determine them to meet the specifications of < 1000 electrons per channel. We compare the power spectra to simulation and determine the level of capacitance and external shielding needed to yield the desired results. Further testing within liquid nitrogen models predicted performance at liquid argon temperature, and these tests expose areas where better quality yield is required. The continuation of design of these electronics will be tested within the ICEBERG detector at Fermilab, and become one of the potential solutions to be incorporated in the DUNE Far Detector, 2029.

Table of Contents

List of Figures

Chapter 1

Introduction

1.1 Neutrino Detectors

The current neutrino frontier reaches out to locations around the world, with a variety of experiment/detector types. Some notable experiments have been conducted by the Department of Energy's Fermilab, where they have searched for the existence of sterile neutrinos.[1] The MINOS experiment in Soudan, Minnesota has measured the rates at which neutrinos change their types, or oscillate using a particle accelerator.[19] Japan has a large detector known as Super-Kamiokande that uses 12.5 million gallons of water [2] to detect interactions; and Antarctica has a project known as IceCube that uses detectors within the ice to create a neutrino telescope.[3]

The study of neutrinos hopes to answer questions related to the existence of matter, why neutrinos oscillate and change flavor, and the hierarchy of the masses of these different flavors. Sources of neutrinos can be cosmic, or created using a proton accelerator, though some have been emitted from atoms in the surroundings. Some of these potential emissions may yield answers regarding the decay of protons. With all of the desires to study this particle, the neutrino is elusive as it is a particle with no charge and minuscule mass, less than one electronvolt [4], which makes it difficult to capture and observe. Every new set of experiments have improved on the previous ones and this decade plans to see three major next-generation neutrino experiments: The Jiangmen Underground Neutrino Observatory

(JUNO) in China, which is expected to begin collecting data in 2021, Hyper-Kamiokande, an upgrade to Japan's Super-Kamiokande neutrino detector, and the Deep Underground Neutrino Experiment (DUNE), due to start in the United States in 2029.[5]

1.2 Overview of DUNE

DUNE will be a leading-edge, international experiment for neutrino science and proton decay studies.[6] Specific discoveries hope to include the origin of matter, unification of forces, and black hole formation. Studies of neutrino oscillations will lead to a better understanding of their role in the universe. Proton decay can show a relationship of matter and the forces that interact and hold everything together. The detectors will also serve to look out towards supernova in the Milky Way and potentially see neutrinos from newly-formed neutron stars or black holes.[6]

DUNE will make use of a proton accelerator at the Fermi National Accelerator Laboratory in Batavia, Illinois. A neutrino beam will be aimed from Fermilab towards Sanford Underground Research Laboratory in Lead, South Dakota as shown in Figure 1.1. Along this 1300km path, the neutrino beam will pass through two individual detectors. The first will record particle interactions near the source at Fermilab, while the second, larger detector will be the Far Detector (FD) at Sanford.[6] Most of the neutrinos sent from Fermilab will begin as the muon type, and DUNE will measure these particles as they travel the 1300km, transforming and passing through the FD.[7] For the remainder of this thesis, we will focus on the DUNE FD.

1.3 The DUNE Far Detector

The FD will be the largest and most technologically advanced liquid argon neutrino detector in the world, more than 20 times larger than existing detectors of this kind.[10] It is being built 1.5 kilometers underground at Sanford and will consist of four individual modules, as seen in Figure 1.2. Each module will be filled with 10 kilotons of liquid argon and be cooled

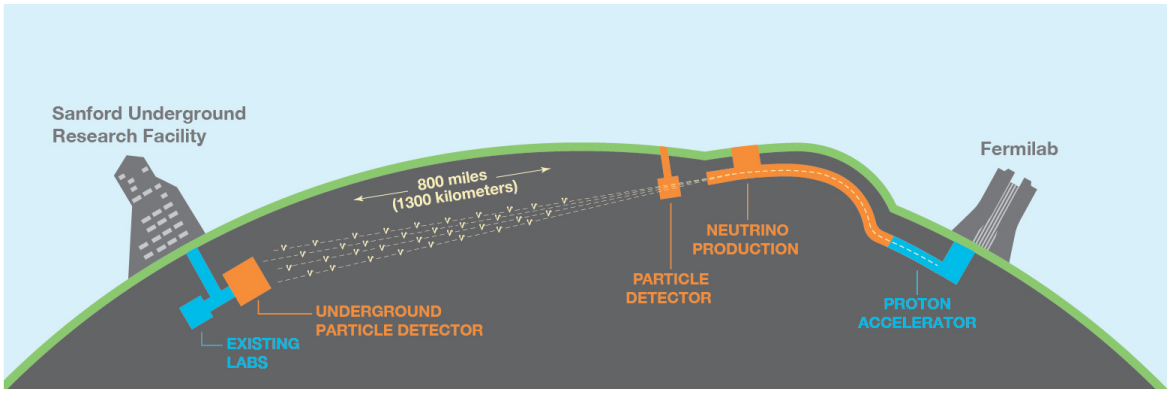

Figure 1.1 An illustration of the path that neutrinos will take, traveling 1300km from Fermilab to Sanford. The near and Far detectors of DUNE will measure the traveling neutrinos and compare oscillations and other attributes. Though generated as muon neutrinos, oscillations will increase the probability of detecting mostly tau neutrinos at Sanford, with a small chance at seeing electron neutrinos.

to -184 degrees Celsius. Liquid argon — cooled to that state from its gaseous form — is so dense that neutrinos interact at an enhanced rate.[9]

As the neutrinos interact with the argon atoms, they create charged particles that traverse the liquid argon detector. This happens within a time projection chamber (TPC) where charged particles ionize argon atoms that then release electrons. These newly minted electrons are then swept by an electric field and collected by wires. Using advanced electronics and software, DUNE scientists can reconstruct and analyze a complete 3-dimensional picture of each neutrino interaction to precisely measure the phenomena of neutrino oscillations.[7] A high voltage draws these electrons to wire planes installed inside each detector module. This results in a distinctive, precise signal that yields important information about the neutrino interaction and allows for a 3D reconstruction of the particles' trajectories.[10]

The wire planes within the detectors will lead to the electronics that are supported by large metallic racks, called Anode Plane Arrays (APAs), and shown in Figure 1.3. Multiple

sections of these APAs will hold the cold electronics, those operating within the liquid argon, which will then interface to the warm electronics, those outside of the detector modules.

DUNE Far Detector

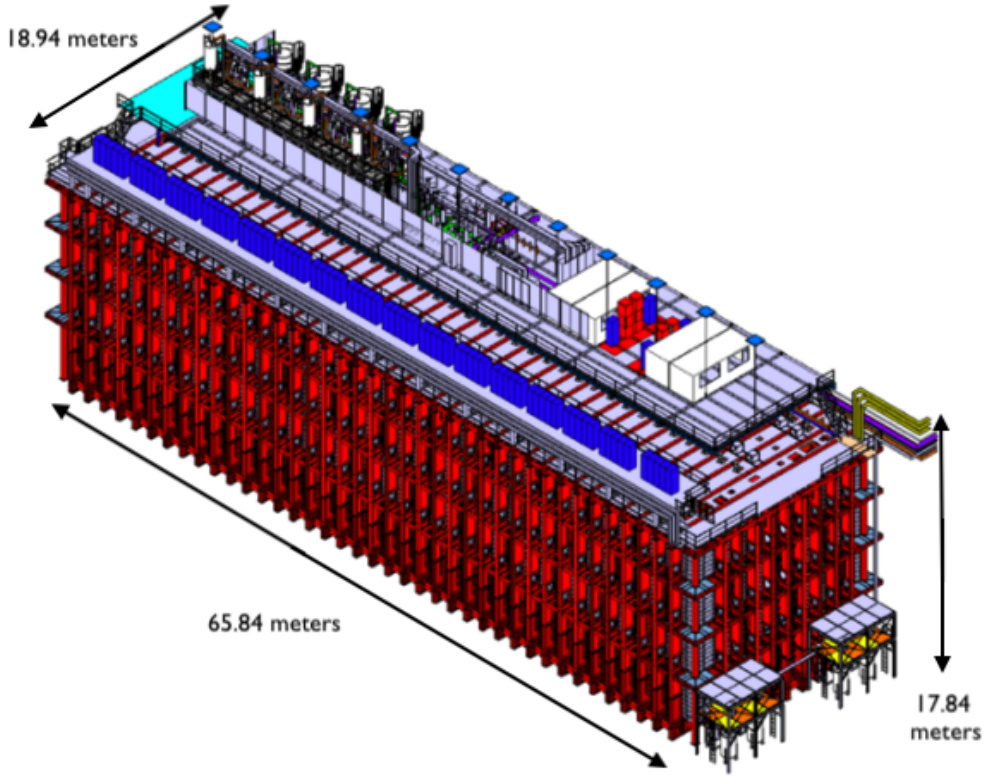

Figure 1.2 A 3D render of a single module for the proposed FD. Each module holds 10 kilotons of liquid argon and four modules will be used in total. The entire FD will include 40 kilotons of liquid argon and become the world's largest liquid argon time projection chamber.
The external warm structure measures 65.84 m long, 18.94 m wide, and 17.84 m high, and its internal dimensions are 63.6 m long, 16.7 m wide, and 15.6 m high. It is a welded and bolted structure constructed of I-beam elements and a 12 mm inner steel plate reinforced with ribs.

DUNE Anode Plane Array

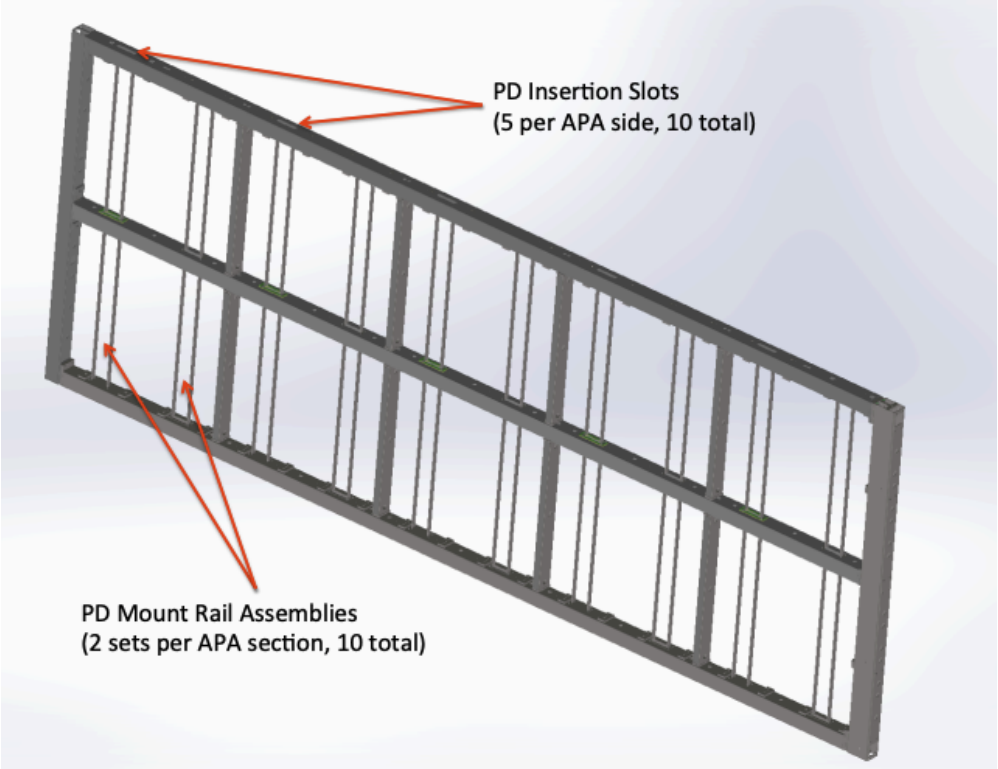

Figure 1.3 The anode plane array (APA) that will hold and support the cold electronics within the neutrino detector. Each APA will support 10 individual circuit boards used in the detection of neutrinos.

Chapter 2

Build and Testing Status

2.1 Build Status

Current tests are exploring multiple ways of using argon as a detection medium. The DUNE Collaboration is prototyping two detector concepts: a single phase version that uses only liquid argon, and a two-phase detector that uses argon as both a liquid and a gas. These ProtoDUNE detectors have been constructed at CERN, the European particle physics laboratory that is a partner in DUNE.[10]

There will be multiple designs of electronics that will be used within the detectors, first to capture the electrons from the wire planes and then several stages to interface to external computers and data storage.

Multiple Warm Interface Boards (WIBs) bridge the cold electronics within the liquid argon to external computers. The WIBs control the power and register interface to the cold electronics, while also reading digitized data back from the TPC. Each WIB will connect to 4 circuit boards within the detector, and a total of 1500 WIBs are planned to be used per FD module.[12]

Many APAs will be used to support and house all of the cold electronics, which then distribute the wire arrays within the detector medium. Every 2 APAs will hold 5 WIBs, which in turn will connect to 20 circuit boards within the detector. These cold circuit

boards are named the Front End Motherboards (FEMBs), and are the initial electronics used to detect the neutrino interactions within the detector.[13]

Several FEMB designs are being prototyped by the collaboration's teams and laboratories. Other teams are also designing a suitable Application-Specific Integrated Circuit (ASIC) for the FEMBs. The FEMB and ASIC designs in this thesis have been done in collaboration with the teams at Stanford Linear Accelerator Center (SLAC) and Brookhaven National Laboratory (BNL).

2.2 Testing plans

Testing of the cold electronics along with the WIBs will be done at Fermilab using the Integrated Cryostat and Electronics Built for Experimental Research Goals, or ICEBERG, shown in Figure 2.1.

ICEBERG uses liquid argon but in a smaller volume than DUNE. It has already tested several FEMB solutions and characterized the performance of the electronics. Currently, ICEBERG is awaiting the arrival of a novel FEMB that incorporates two identical copies of a novel ASIC. This FEMB has been designed at the University of Hawaii and is completing tests at both Hawaii and SLAC.

ICEBERG Detector Technology Test Bed

Figure 2.1 Fermilab's ICEBERG test bed is effectively a miniature version of the component that tracks neutrinos in the international DUNE experiment. ICEBERG is used to evaluate performance of potential components of DUNE.
Photo: Reidar Hahn, Fermilab

Chapter 3

Technical Design

3.1 FEMB - Device Design

The Front End Motherboard designed here is a 10-layer printed circuit board (PCB) that incorporates power regulators, input circuitry, and the "CRYO" ASICs designed by SLAC.[11] While initially designed to be used in the nEXO neutrinoless double beta decay experiment [16], small modifications have been made to make it suitable in the DUNE FD. Each FEMB has two copies of the CRYO ASIC which integrates the functions of amplification, digitization and transmission into a single integrated circuit. A block diagram of the CRYO is shown in Figure 3.1 and all further mentions of the FEMB refer to the version with this CRYO ASIC.

Block Diagram of the CRYO ASIC

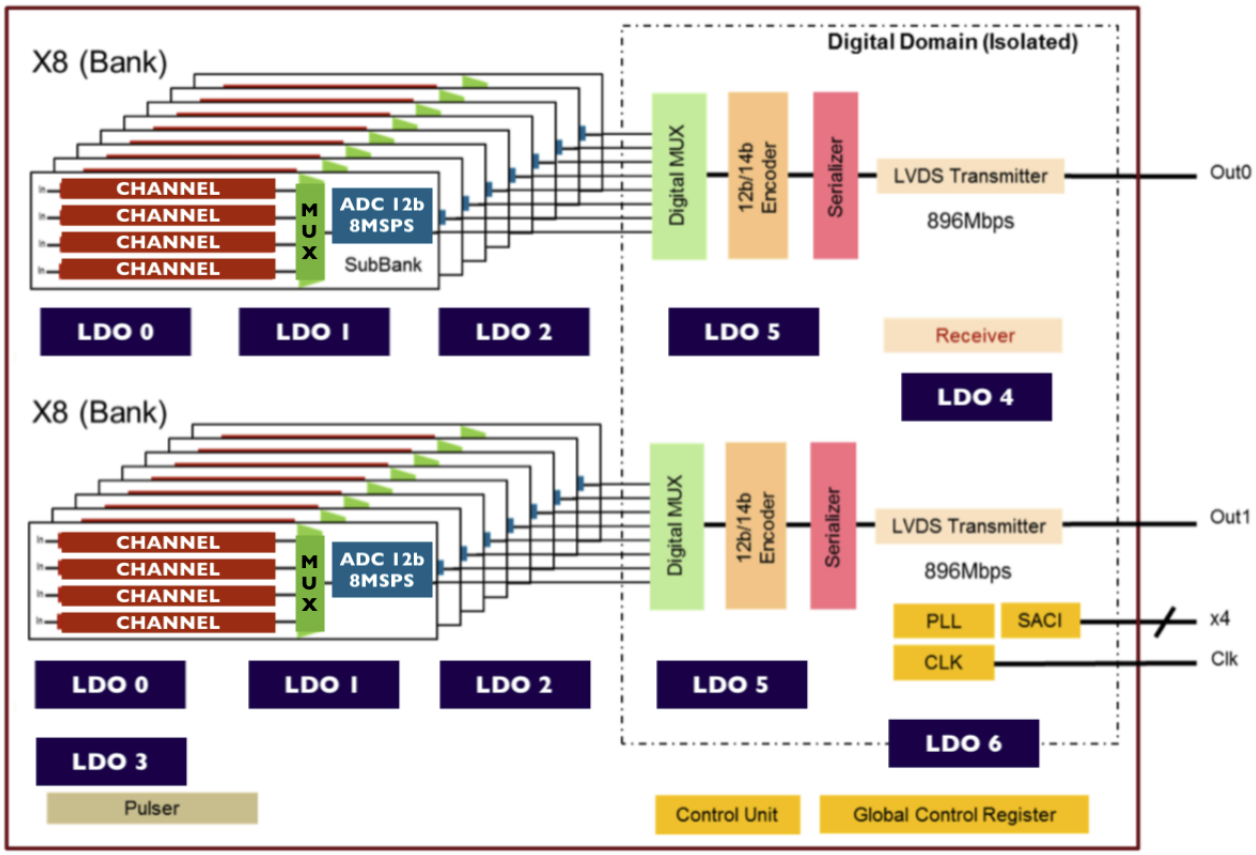

Figure 3.1 The architecture of the CRYO ASIC. It functions for both the DUNE neutrino experiment as well as the nEXO neutrinoless double beta decay. We use two CRYOs per FEMB to handle the amplification, digitization and transmission of signals for the DUNE project. Two banks of 32 channels are included within each CRYO, for a total of 64 channels per ASIC and 128 channels per FEMB.

Description	Specification(Goal)	Rationale
Peaking Time	$1\mu s$	resolution for wire spacing in detector (5mm)
Power Consumption	$< 50mW$/channel	Avoid bubbles in liquid Ar
Noise per channel	$< 1000\ e^-$	Provides signal to noise ratio greater than 5:1
ADC sampling frequency	2MHz	Match $1\mu s$ shaping time
ADC bits	12	low noise and match signal saturation
Channel Yield	$> 99\%$	Long term use of detector, greater than 20year operation

Table 3.1 Key requirements established by the DUNE Technical Design to be met by the FEMB.

3.2 Required Performance

Table 3.1 lists the specifications required for the design of the FEMB.

For a complete list of DUNE electronic specifications, see table A.9 in the recent Technical Design Review V3[13].

3.3 FEMB Revision A

The FEMB was designed based on the specifications and dimensions of a preliminary board from BNL, which had four ASICs as well as a mezzanine card attached. The main circuit components and mezzanine card were all replaced by the CRYO chips from SLAC, and the input circuitry was adapted to be compatible with the rest of the design. This was reworked into a new board design. Following the desired 2.5V input power rails [18], multiple DC linear voltage regulators, or low-dropout regulators (LDO), were added to reduce noise from the incoming raw power. Digital and analog LDOs were kept separate from one another as a means to isolate the respective power rails on the CRYOs. Each CRYO also had its own digital and analog LDOs, rather than sharing single LDOs per rail among both CRYO ASICs. Data buffers are used to strengthen the digitized data stream that gets sent to an external interface. Table 3.2 provides a list of features of the FEMB and the groups that contributed to the design.

Front End Motherboard Features and Contributions

FEMB Feature	Function	Credit
Board External Dimensions	Placement within the DUNE experiment	BNL [7]
Input Circuitry	Protection for the inputs of the CRYOs	BNL
ASIC (CRYO x2)	Detector readout: amplification, digitization, and transmission	SLAC [11]
Active Component Selections	Functionality in FD conditions	BNL and SLAC
Modified power network	Incorporation of CRYOs	This work
Component Placement	Placement of components on FEMB	This work
Analog and Digital Routing	Connecting wires internal to FEMB	This work
Internal LDO Capacitance	Reference capacitors for internal CRYO design Reduction in data noise	SLAC and This work
PCB Layers	10 layer board	This work
Updates and Revisions for RevB	Second iteration of the FEMB	This work

Table 3.2 Component contributions that this work merged together to create an FEMB using the CRYO ASIC for the DUNE experiment. Credit is given here for the designs of individual portions of the board. Designs and research done in support of this thesis are labeled under column "Credit" as "This work".

This first revision of this novel FEMB included multiple power schemes, with several LDOs to provide load options to the CRYOs. This allowed several conditions of operation ASICs. The nominal configuration had the ASICs receiving regulated power from the 2.5V LDOs, and everything else was bypassed. However, the user could choose to feed the raw input voltage to the ASICs instead of regulated if the raw input was well controlled. Another LDO option provided was to power the internal banks of the CRYO ASICs with external LDOs, ranging from 2V, and 1V inputs. This feature was primarily used for testing and debugging purposes.

Figure 3.2 here shows a mock up of the design with sections highlighted, and a detailed schematic is available upon request.

3.4 FEMB Revision B

Several months after the design and testing of the Revision A FEMB, updates were made and a Revision B FEMB was fabricated. The major changes included updated power

FEMB Revision A

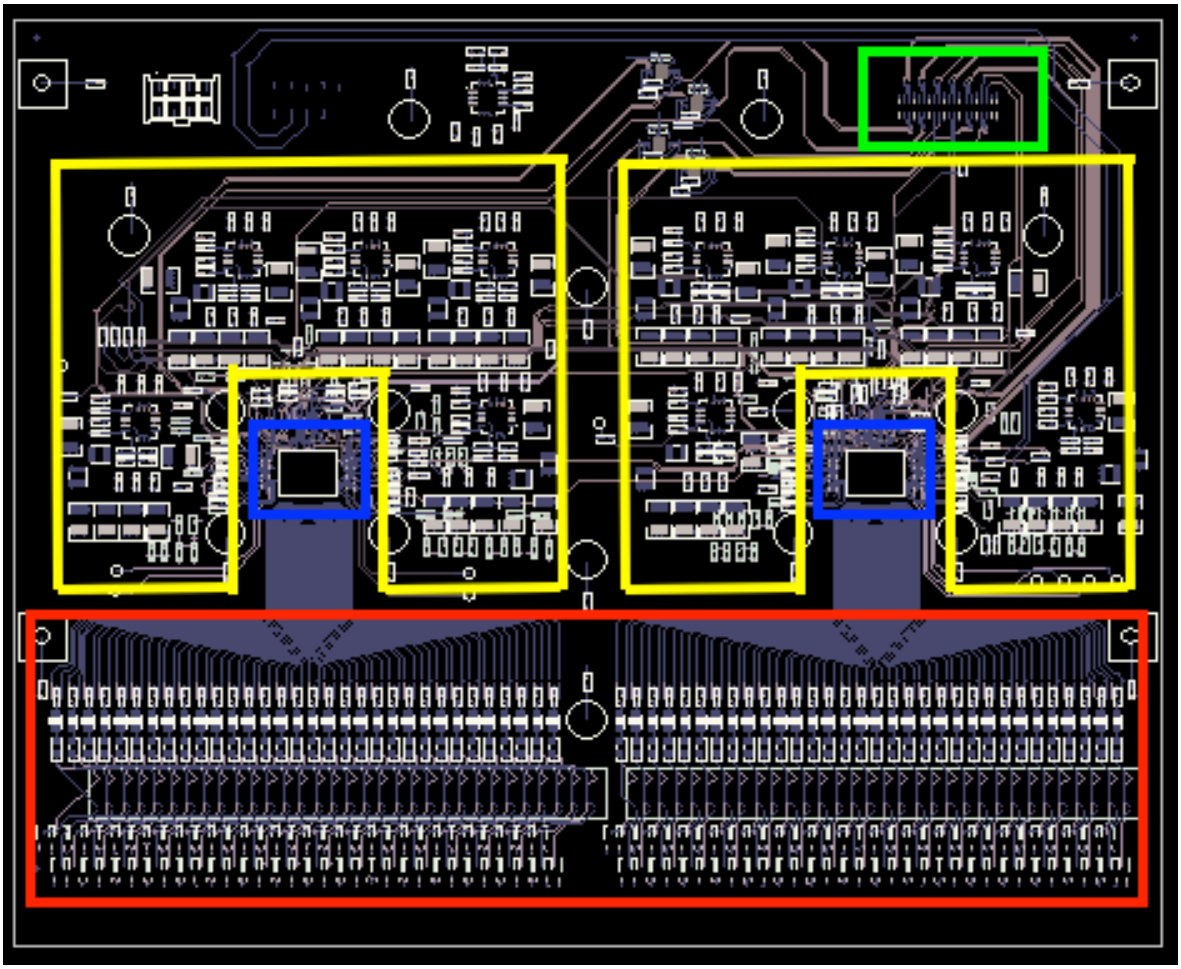

Figure 3.2 Layout of the FEMB Revision A. The highlighted sections are as follow: yellow shows the power options, blue shows the two CRYO ASICS, green is the data input/output connector, and red highlights the input circuitry.

schemes, capacitance increases, component changes, diode grounding options, data buffer efficiency, testing and debug options, and the capability to use newer versions of the CRYO.

Through testing, many power options that the RevA FEMB allowed were either redundant or unnecessary. The nominal scheme, 2.5V input power with a 5V bias rail, was kept and made permanent in the second revision/design without other options.

The discovery that additional capacitance helped to stabilized the CRYOs also led to RevB implementing many additional capacitors, each generally of higher tolerance and temperature capabilities. Each internal LDO circuit within the ASICs now had 247μF worth of external capacitance. In addition to increased capacitance, larger capacitor component sizes were used as a means to have an increased tolerance, from 6V to 10V, even in cold environments.

The RevA board had the diodes in the input circuitry tied to ground on both terminals. The RevB board was updated with an additional plane internally with loading options for one of the diode inputs. This allowed the protection diodes to either be tied to ground and ground, or power and ground.

Data buffers were reworked to have the option of being bypassed. This bypass was implemented to have minimal impact on signal integrity. Further testing will be done to see if the buffers were necessary or not for communication with the warm electronics that interface to external data processing.

Finally, the last few changes included additional testing points, debugging connectors, and a data cable cutout. These input and output connections were not present on the Revision A FEMB but were added to provide further observations. An updated footprint was also used for the next generation of the CRYO ASIC, yet backward compatible with the original CRYO.

Figure 3.3 shows a mock up of the design with sections highlighted, and a detailed schematic is available.[20]

FEMB Revision B

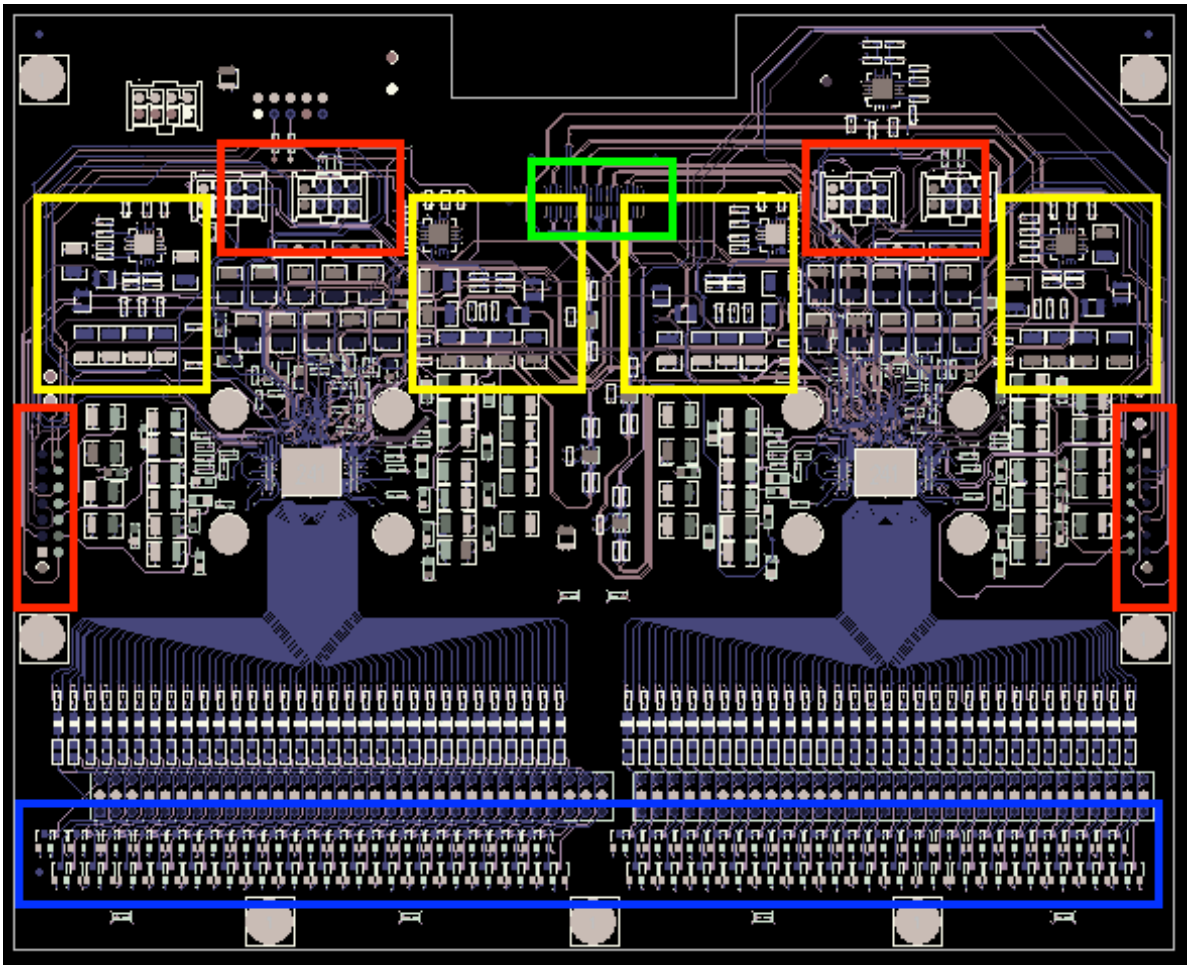

Figure 3.3 Layout of the FEMB Revision B. The highlighted sections are as follow: yellow shows the new power options, red highlights the debug and test connections, green shows the relocated data input/output connector, and the blue section shows the updated protection diodes.

Chapter 4

Setup and Conditions

4.1 Lab Setup

Figure 4.1 demonstrates the physical setup used to interface to the FEMBs. Due to costs and access, no WIBs were readily available, and a temporary setup was used. All of the programming and testing was done using a Linux machine which was connected by fiber to a Xilinx board, model KCU105 [15]. The KCU105 paired with an adapter board for communication between the Linux machine and the FEMB, shown in Figure 4.2.

In collaboration with SLAC, firmware was written for use with the adapter board and the Xilinx KCU105. The clock is generated by an on board PLL and the SLAC SACI interface is implemented for control of the FEMB ASIC registers.

Using a Linux machine running Ubuntu, a terminal was setup with the SLAC SURF and ROGUE environments. This is necessary for proper working of the software and graphical interface. Installation instructions, packages, and documentation are found at [17].

4.2 Peripherals

BNL provided a metal box that will be used to house each individual FEMB within the APAs. These aid in the shielding of any external noise as well as structural support of the electronics.

Figure 4.1 Lab space for the communication and testing of the FEMB. CTS unit on left allows shielding and submergence into liquid nitrogen. Power supplies on top for multiple voltage rails. Scope and multi meter for debugging signals. Linux interface on the right.

The final testing setups include the peripherals added to the FEMB. We plug in another two circuit boards into the inputs of the data channels, with the intention of replicating attributes of the actual detector. The capacitance values that would be seen within the detector time projection chambers (TPC) are replicated on these toy TPC's as shown in Figure 4.4.

4.3 Testing Environments

While the final FEMB will reside within liquid argon at 87K in the FD, liquid nitrogen was used in current testing due to cost constraints, and being close in temperature at 77K [14].

Nitrogen remains inactive when in contact with the FEMB, and the temperature is close enough to liquid argon, that it was sufficient in replicating liquid argon conditions.

To safely handle liquid nitrogen, as well as accurately control the cooling and submergence of the electronics within liquid nitrogen, a storage dewar and test system was used. This Cryogenic Testing System (CTS) was designed by Dean Shooltz [footnote] of Michigan State University. Operation and safety concerns are defined in Appendix A.

An Oxygen Deficiency Monitor is also recommended to alert users if conditions become non-optimal in a lab with liquid nitrogen testing. Additional personal protective equipment includes gloves, aprons, and face shields all rated for cryogenic testing.

When not testing cold, quick tests were done at "warm". These were conducted in the lab that is temperature controlled to about 21C/290K. Conditions were meant for constant changes/adjustments that may not be easily done when the electronics are submerged in liquid nitrogen.

Xilinx FPGA and SLAC Adapter Board

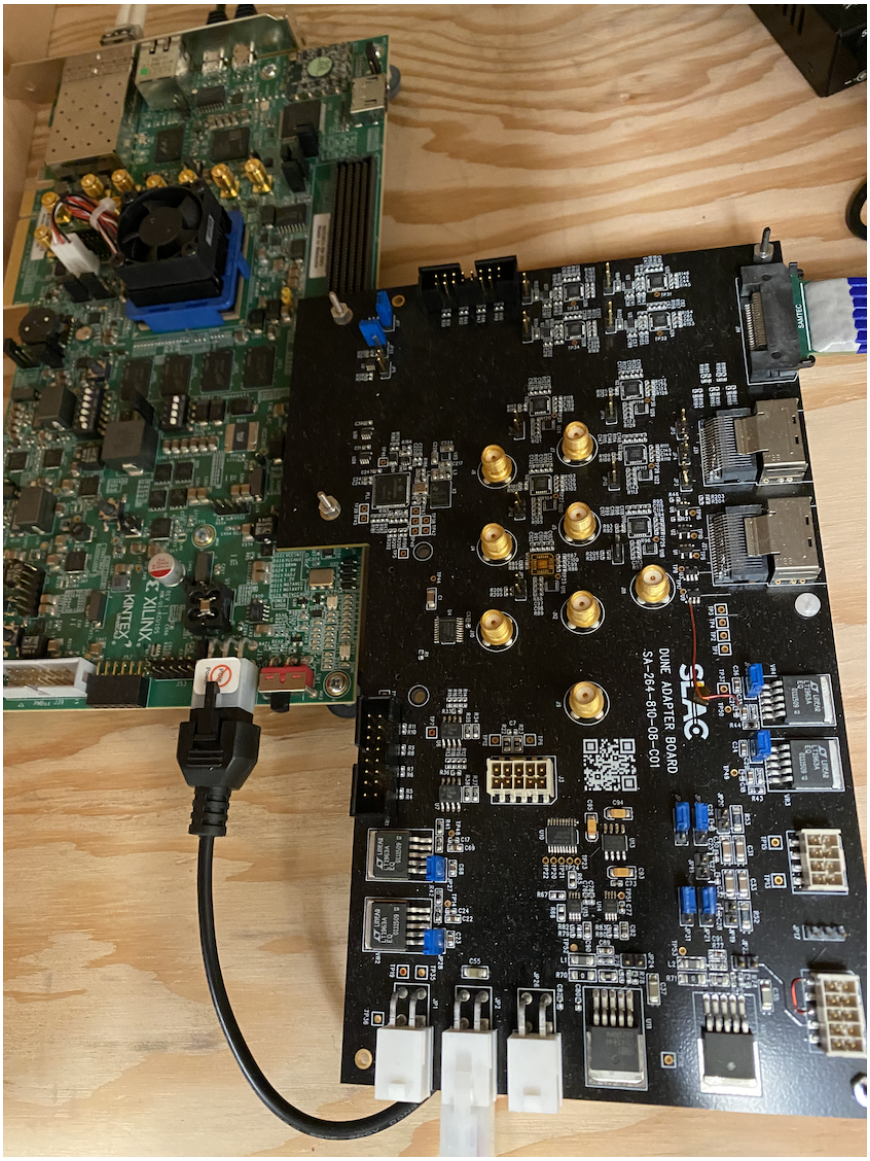

Figure 4.2 Left board: The Xilinx KCU105 FPGA is used to program and communicate with the FEMB
Right board: An adapter Board made at SLAC was used to bridge the KCU105 FPGA to the FEMB data cable. An on board phase lock loop (PLL) control system generates the clock that is used to run the FEMB.

RF Box

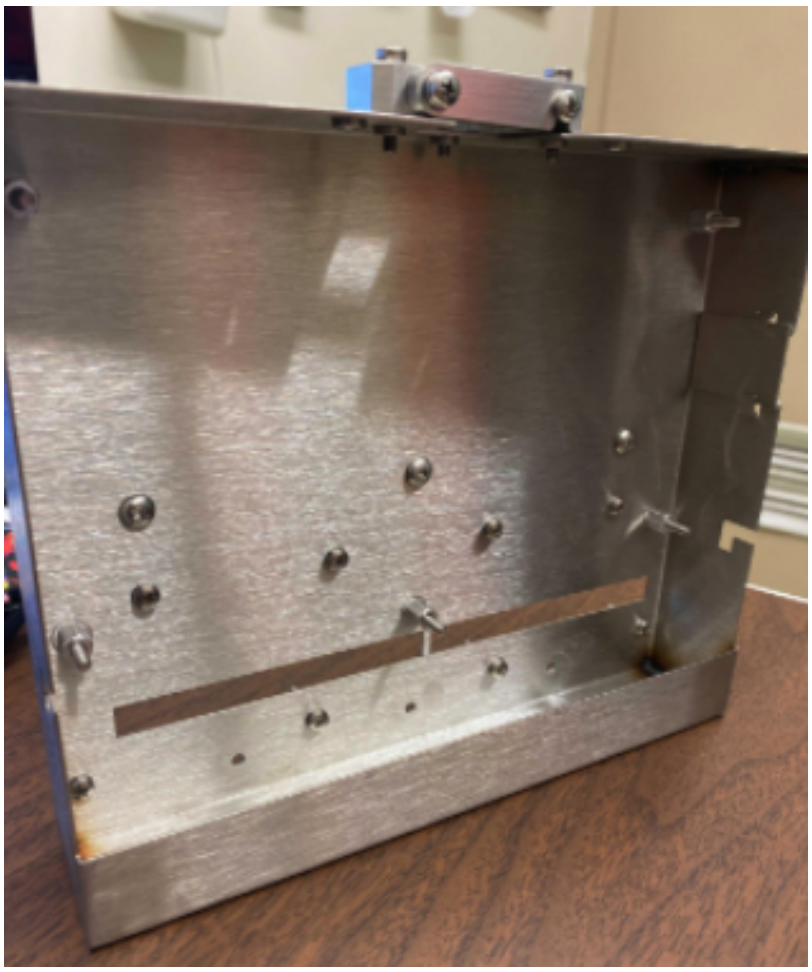

Figure 4.3 A stainless steel housing to be used to shield the FEMB. Each individual board will have its own RF box which will be supported by the APAs in the detector. As mentioned, each APA will support 10 FEMBs.

Toy Time Projection Chamber Card

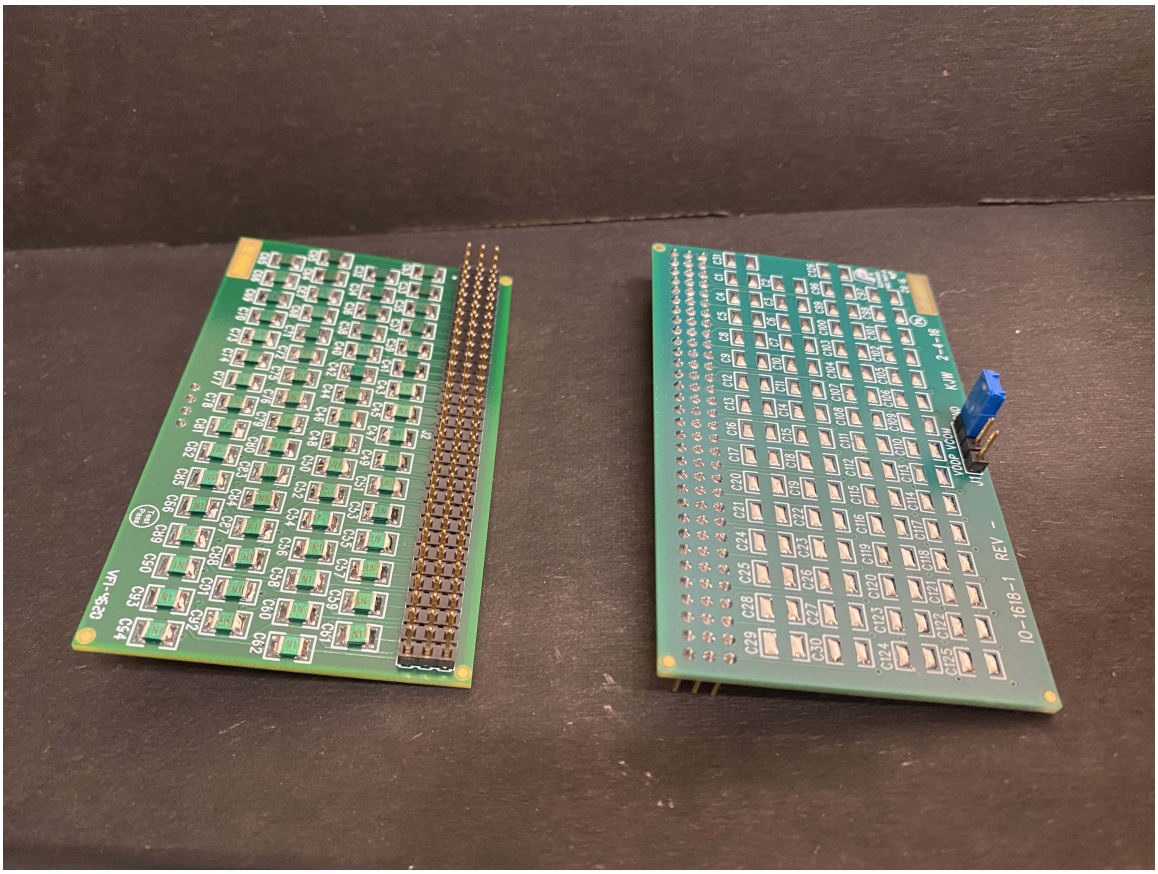

Figure 4.4 These toy TPCs model the same input conditions that would be seen when the FEMB is placed within the actual DUNE detectors. 22pF capacitors are used for each input channel, and each board has 64 channels worth of capacitance. Both toy TPCs are connected to the rear of the FEMB for testing.

Cryogenic Testing System

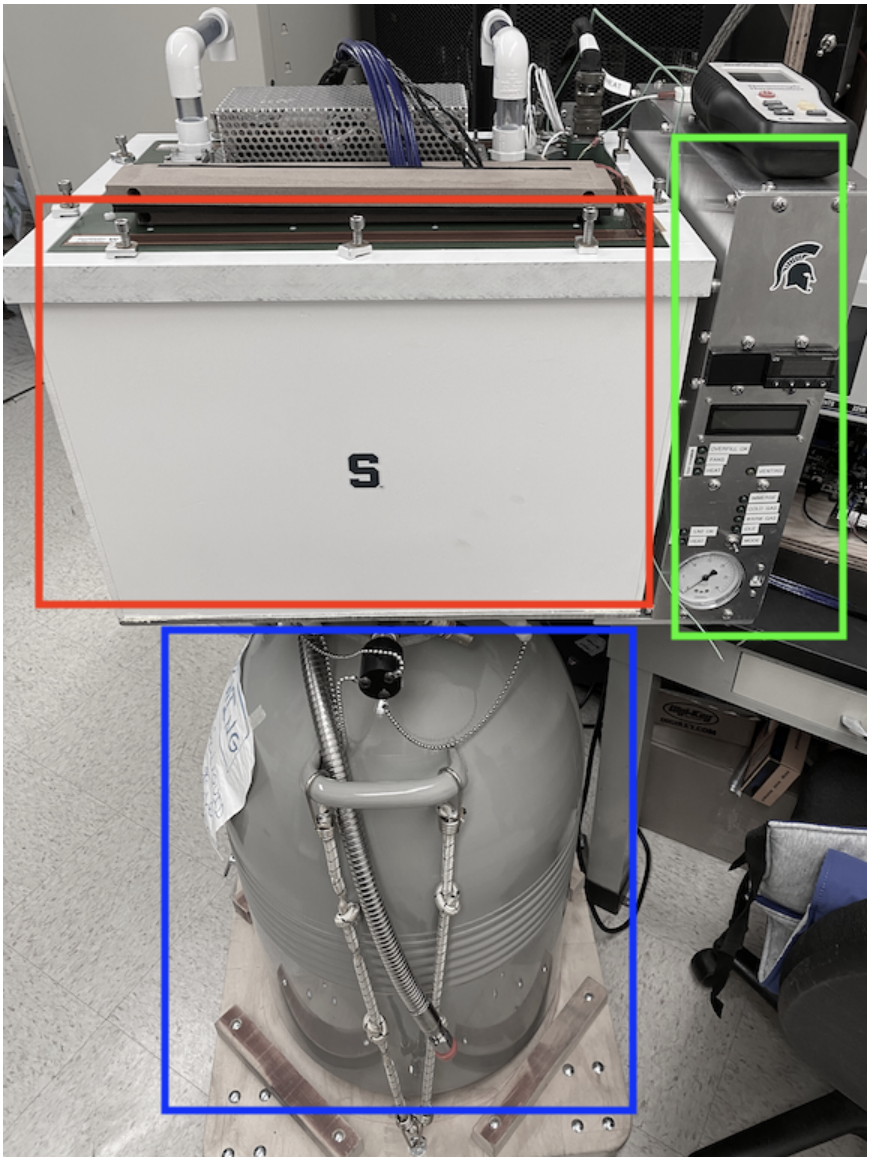

Figure 4.5 The CTS designed for testing the electronics while submerged in liquid nitrogen. Blue highlighted section is the 50L dewar that stores the nitrogen. Red highlighted section is the test sink in which the user places the device under test. Green highlighted section is the control interface.

Chapter 5

Operation Procedures

The user should begin operation by setting up all needed communication with the KCU105 FPGA. Proper connection voltages are need as well as a fiber interface for high speed data. The firmware is then loaded either from a computer or from internal flash memory. Once connections are established, the adapter board can be powered from external power supplies.

A proper terminal environment should then be brought up to run the proprietary software interface. A python based environment is used with the SURF and ROGUE packages from SLAC as mentioned in Chapter 4 [17].

The FEMB is connected to power and data cable and placed within the RF box if necessary. The user may also consider placing the FEMB/RF box within the CTS sink regardless of nitrogen use (additional shielding from external noise). With the lab environment safe for testing and all connections established, the software may be started.

An autonomous initialization process is started using the autoinit register in the commands tab. Multiple initialization configurations are included depending on testing temperatures and data speed operation. After this process, the user sets the ASICs to send ADC data and will see a live feed of data on their monitor.

From this point on, different testing can be done depending on user commands. Data can be either monitored on the multiple live feed options and plots, or saved out to an external file. The saving of data is done on the last tab of the software. An example view

of the software is included in Figure 5.1. A further detailed set of operation instructions are laid out in Appendix B.

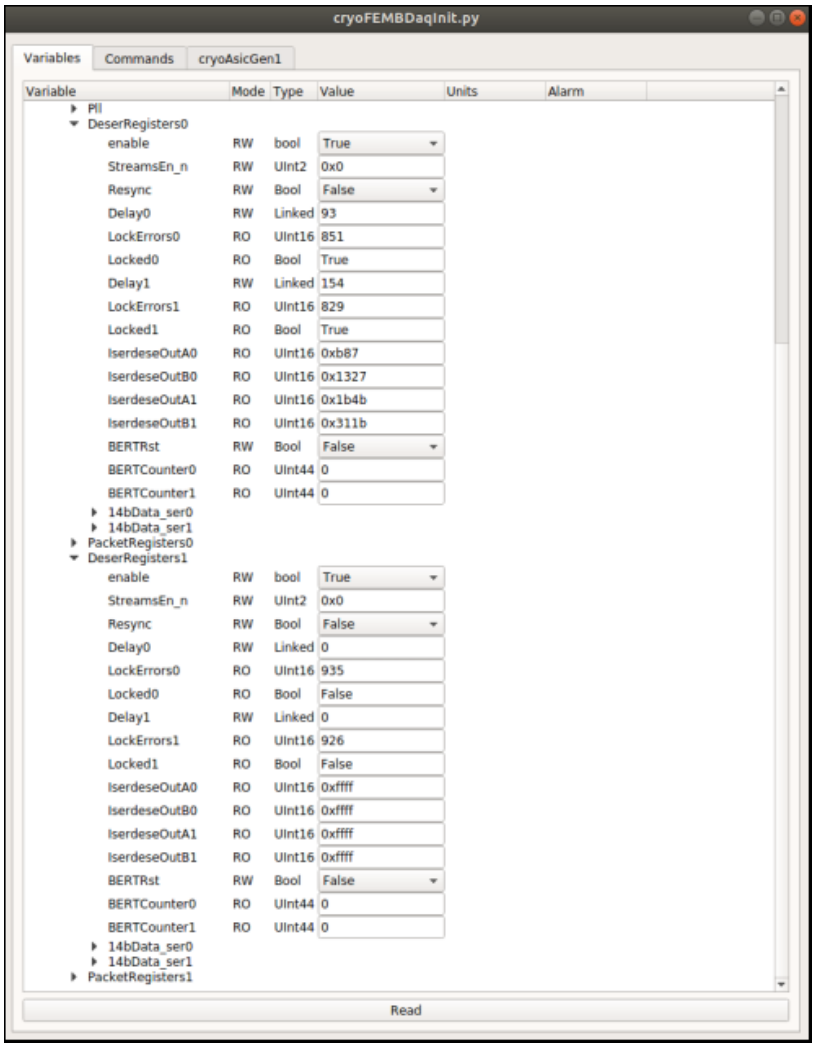

Figure 5.1 The graphical interface used to control and communicate with the connected FEMBs. The first tab and sections support individual register configurations. Setup of the board and ASICs is done here. The second tab holds the data commands to the board as a whole, and is used for pulsing and setting baselines. The final tab contains the configuration files, as well as data saving options.

Chapter 6

Testing & Characterization

6.1 FEMB Revision A Tests and Results

Once initial designs were completed and reviewed, the FEMB was sent out for fabrication and assembly. Figure 6.1 shows the fabricated and assembled FEMB Revision A with all components and ASIC covers. Initial tests were done on the board to verify connectivity of nets and planes within the board. With no noticeable issues communication with the board can be established.

This is first done by connecting and confirming the SACI interface to communicate with the ASIC registers. Figures 6.2 and 6.3 show the SACI clock and command signals that are observed between the KCU105 FPGA and the FEMB. Following communication, the clocks and registers were setup, however a full speed data clock was not achieved. A half speed version of 224 MHz was used to achieve a proper connection with plans to revert to 448MHz at a later test.

Regardless of configuration, a consistent connection to the FEMB was not able to be established. Only 10% of conducted testing had any clear communication and response between the Linux terminal and the FEMB. Test patterns were infrequently achieved but no data could be seen from the ASICs. Observations in the initialization process showed that no data could be due to no communication lock or timing delays.

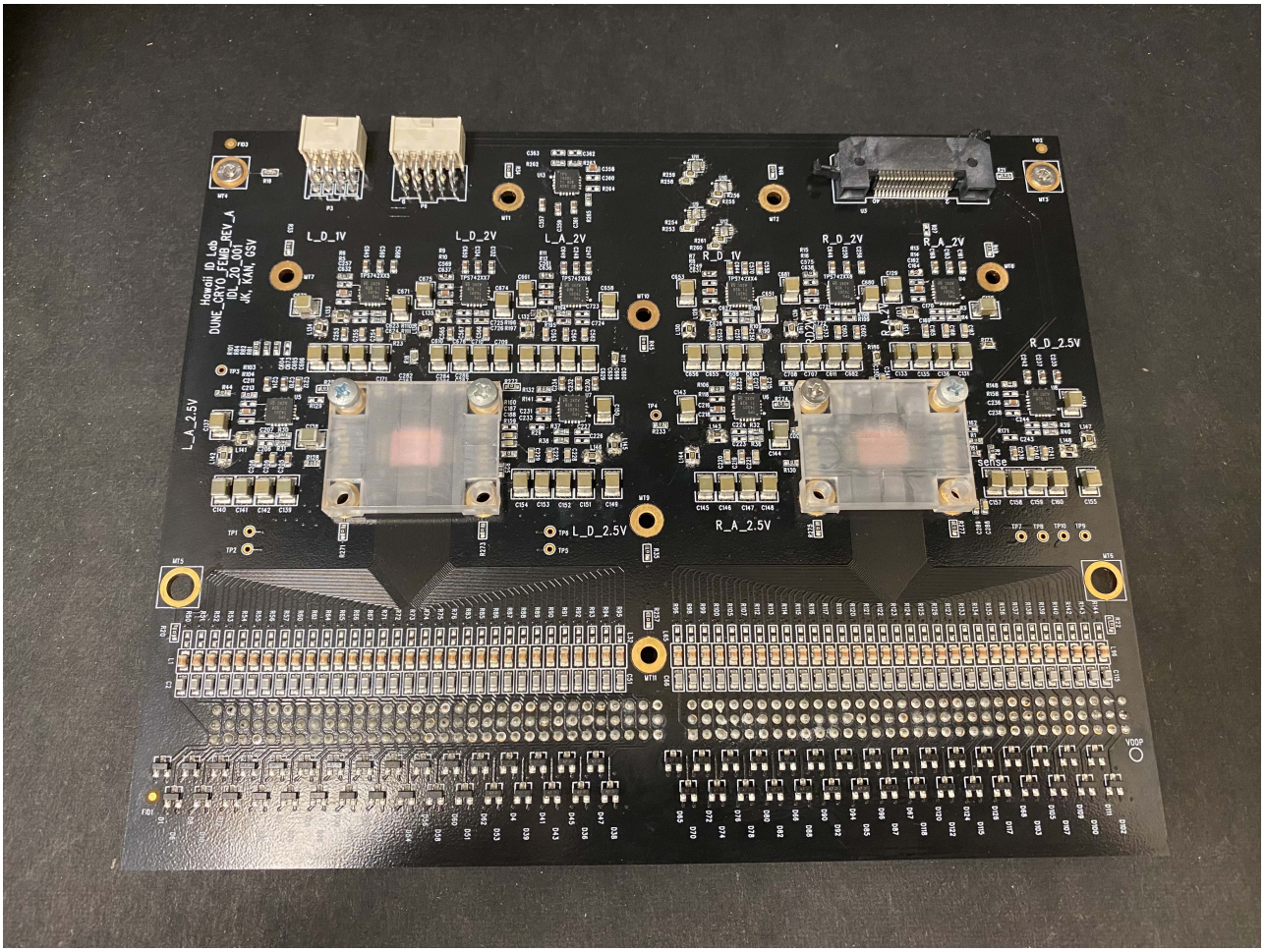

Figure 6.1 FEMB Revision A: Fabricated and assembled, with CRYOs wire bonded to the board; 240 wire bonds per ASIC. Plastic covers are placed over the ASICs to protect from accidents. Mounting holes located around the board for support within the potential RF box.

Picture of SACI signals

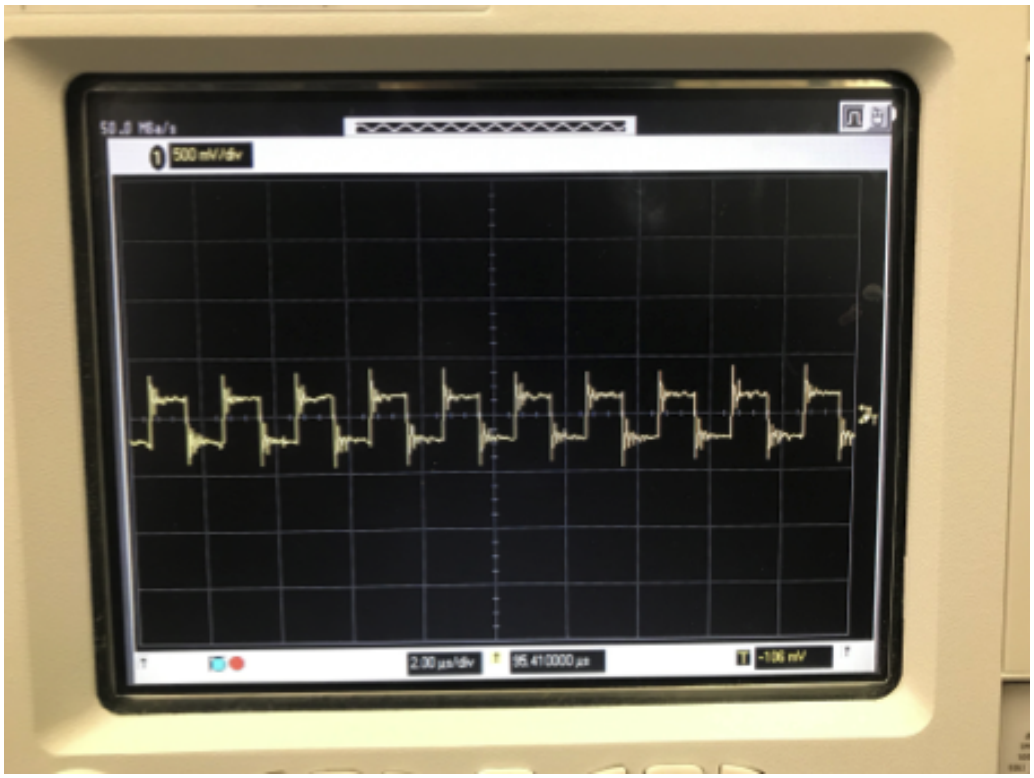

Figure 6.2 SACI clock; Confirmation of communication with Xilinx FPGA and FEMB CRYO ASICs. Clock set to 56MHz, with all SACI command and response functions following.

Picture of SACI signals

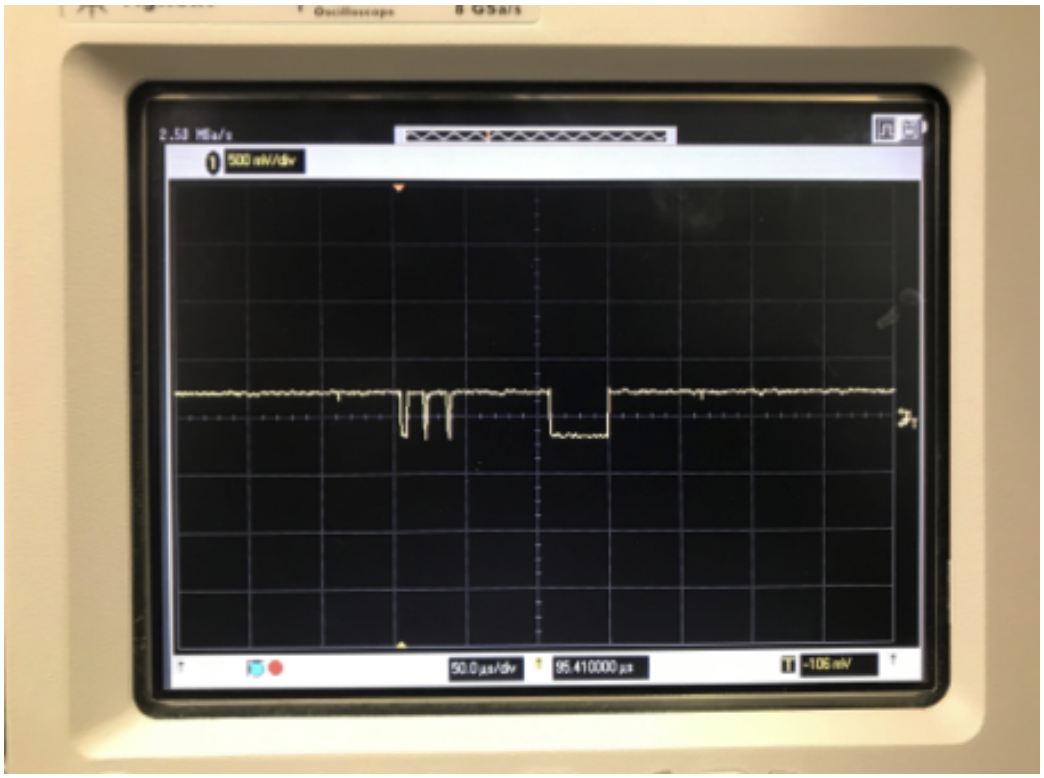

Figure 6.3 SACI command; Confirmation of commands between Xilinx FPGA and FEMB CRYO ASICs. A measurable signal to confirm proper signals to the chips and programming of the registers.

SAMTEC Custom Data cables

Figure 6.4 The longer cable is 11 meters, while the shorter is 3 meters long. The 3 meter cable will be used in the ICEBERG tests, while the longer cables are planned for the final DUNE FD. As communication with FEMB is currently reliant on the 3m cable, drivers will be tested to upgrade to a 11m cable in the future.

By trial and error, the communication issues were determined to be due to the data cable used to connect to the FEMB. The cables shown in Figure 6.4 are custom made by Samtec. The current in use long cable had an unreliable connection, and once we switched to a shorter 3 meter cable, all communication became active. With the shorter (3m) cable in use, the FEMB was able to pulse signals across all input channels, now shown in Figure 6.5.

Our next initialization tests for the ASICs were to confirm that they were responding with a test pattern, output from the CRYOs. Figure 6.6 shows the output patterns on each ASIC as it flips across high and low voltage signals. This confirms the digital portions of the CRYOs are working and the full analog input to digital data out could now be tested.

ASIC Channel Pulse

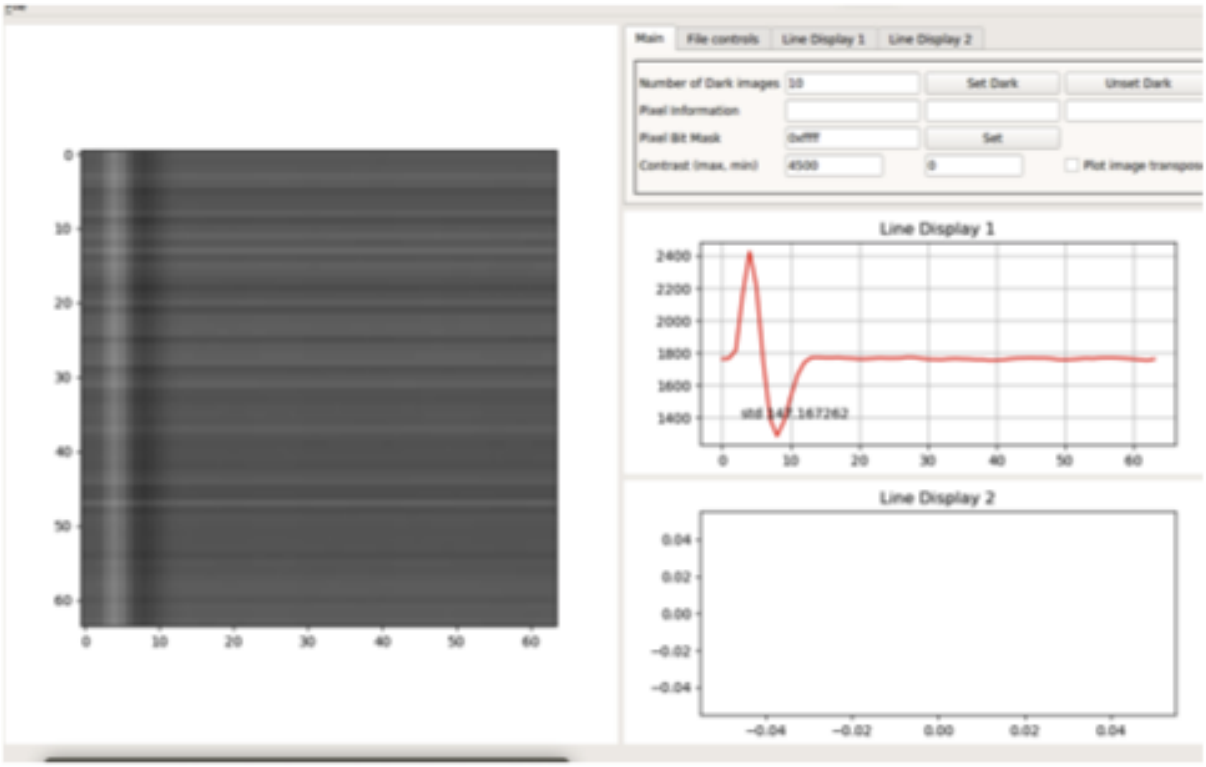

Figure 6.5 Using the GUI to pulse the channels on the leftmost ASIC. The left block shows channels over time, with the channels on the y-axis and time on the x-axis. The pulse can be seen with a lighter peak followed by a darker dip in voltage. The rightmost line display plots the pulsed signal across a chosen channel which matches the view of the left.

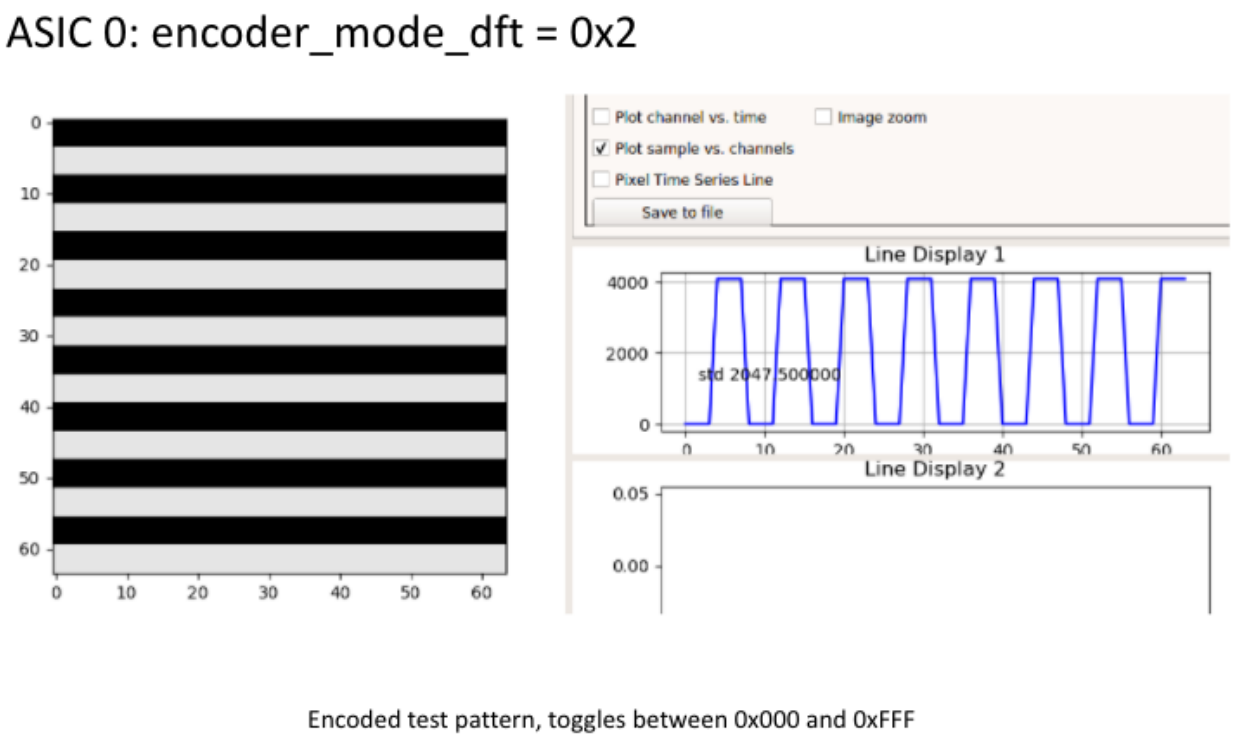

Figure 6.6 Live feed as seen on GUI of a test pattern on left ASIC, with the channels on the y-axis and time on the x-axis. Voltage oscillates between high and low voltages to confirm internal workings of the digital side of the CRYO.

An initialization script was implemented and the CRYOs registers were responding as needed. With both ASICs working at room temperature, we pulsed the 128 input channels and took data across all peaking times: 0.6us, 1.2us, 2,4us, 3,6us as shown in Figure 6.7. For further analysis, we plot the power spectra across all of the peaking times as well; seen in Figure 6.8. This gives us a comparison to simulated noise for the CRYO ASIC and its data taking.

With preliminary tests passed and full data taking ability, we begin to analyze the noise across channels, as well as their wave forms. Figure 6.9 shows the overall noise analysis across multiple channels within the ASICs, and all are seen to have random spikes in the

Peaking times STD and noise

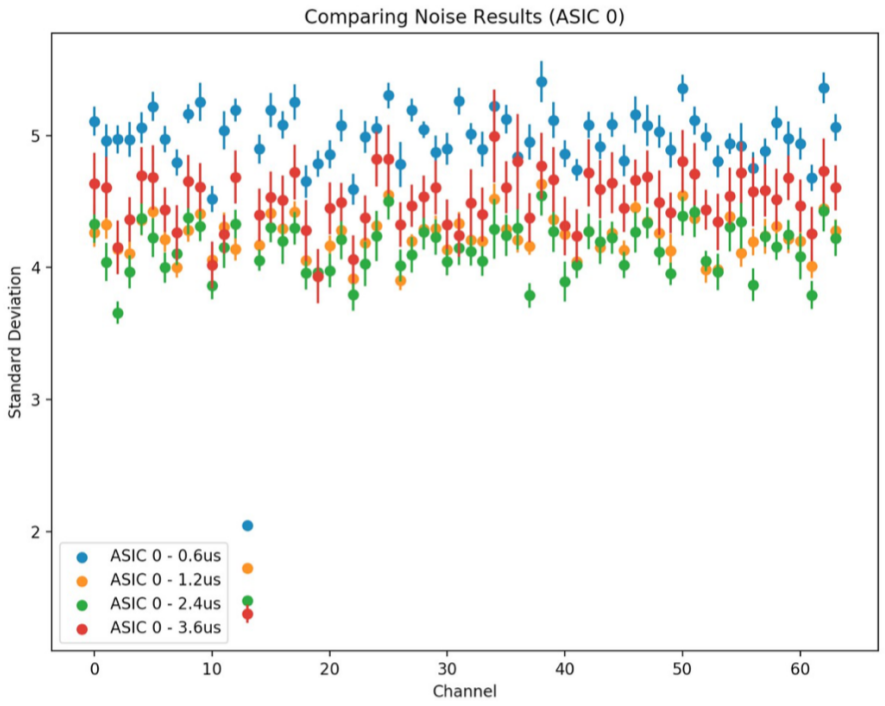

Figure 6.7 Initial noise measurements. Standard deviation of the noise of the channels and internal ADCs of the CRYO ASICs. Noise typically reduces with increased peaking times, with the exception of 3.6us rising slightly.

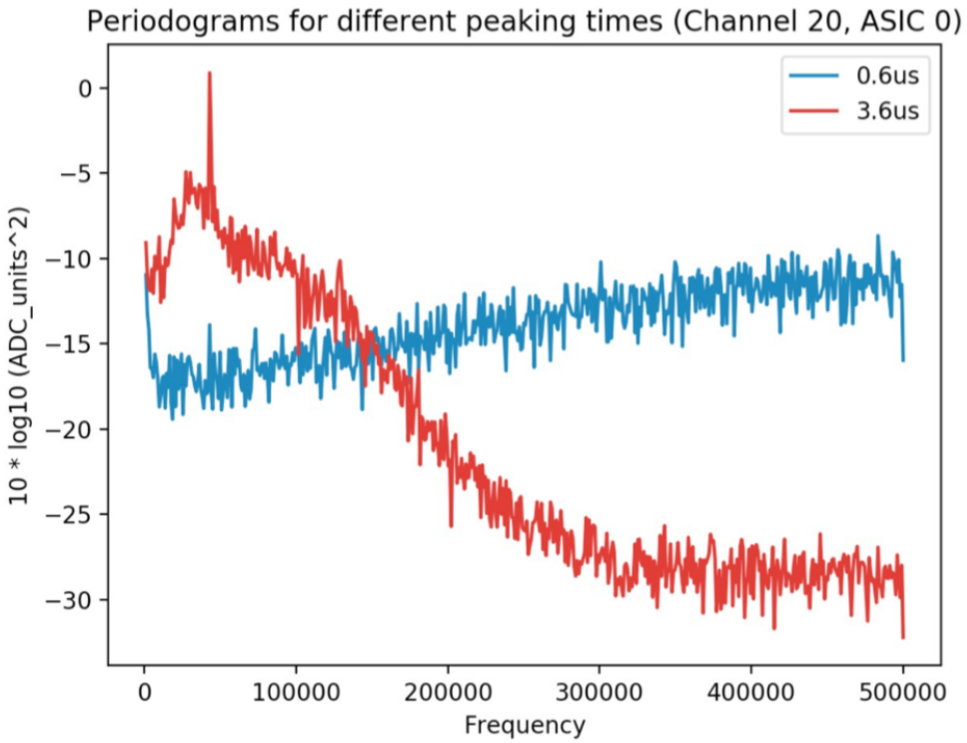

Figure 6.8 Power spectra measurements. We plot the power over frequency to visualize noise across different peaking times. Longer peaking times have a higher noise in the low frequencies, and lower in the higher frequency range.

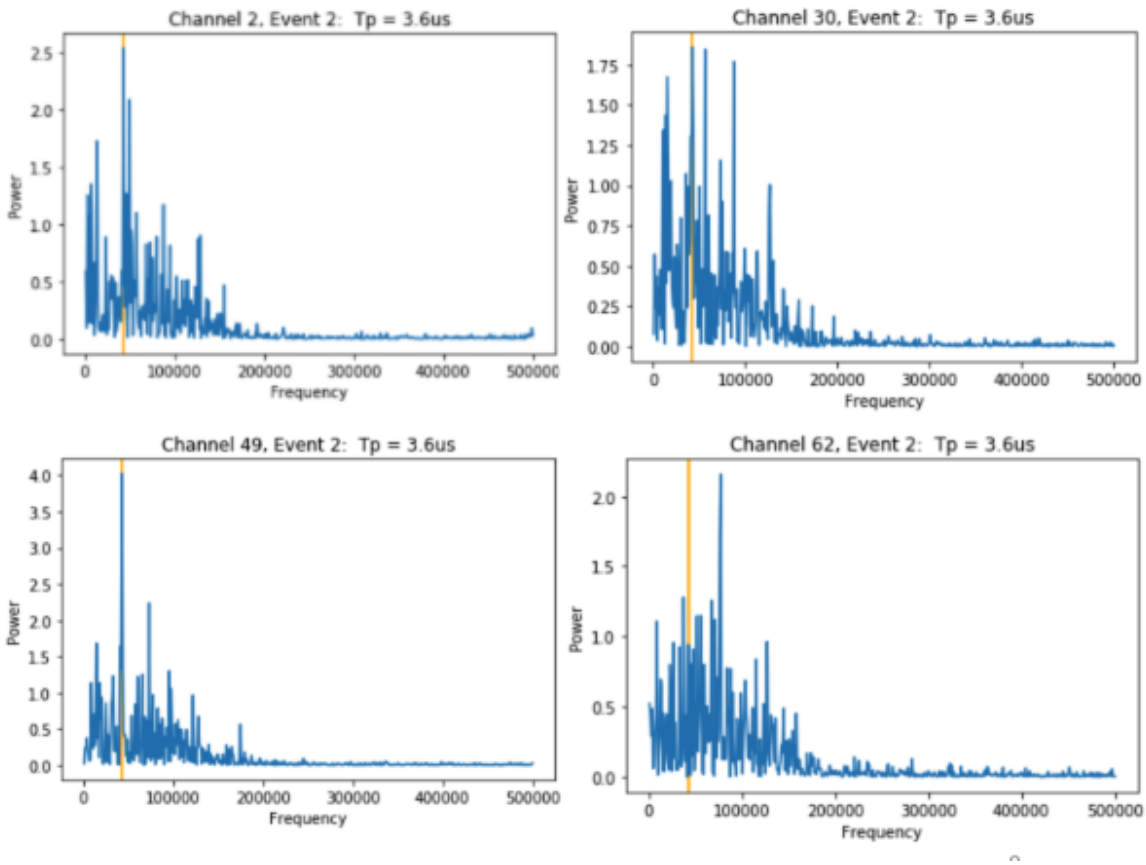

Figure 6.9 A Fourier Transform of multiple channels done to investigate further abnormalities. Many noise peaks are seen in the lower frequencies, with highest powers at 43kHz. This is seen across many channels, and strengthens and wanes over time.

lower frequencies. We investigate all channels of both ASICs and doing so lets us notice a repeated large peak at 43kHz along several power spectra. We take the Fourier analysis of the noise to pinpoint it, shown for an individual channel in Figure 6.10.

As we attempted to remove the 43kHz noise, we explored different grounding schemes and shielding options. Figure 6.11 shows the best grounding setup where the least noise is seen. We also placed the FEMB within the CTS sink in hopes to clean up noise by blocking it similar to a Faraday cage. The CTS dramatically cleaned up the noise spectra as seen in Figure 6.12. However, across all attempts, the 43kHz noise would remain present.

43 kHz noise

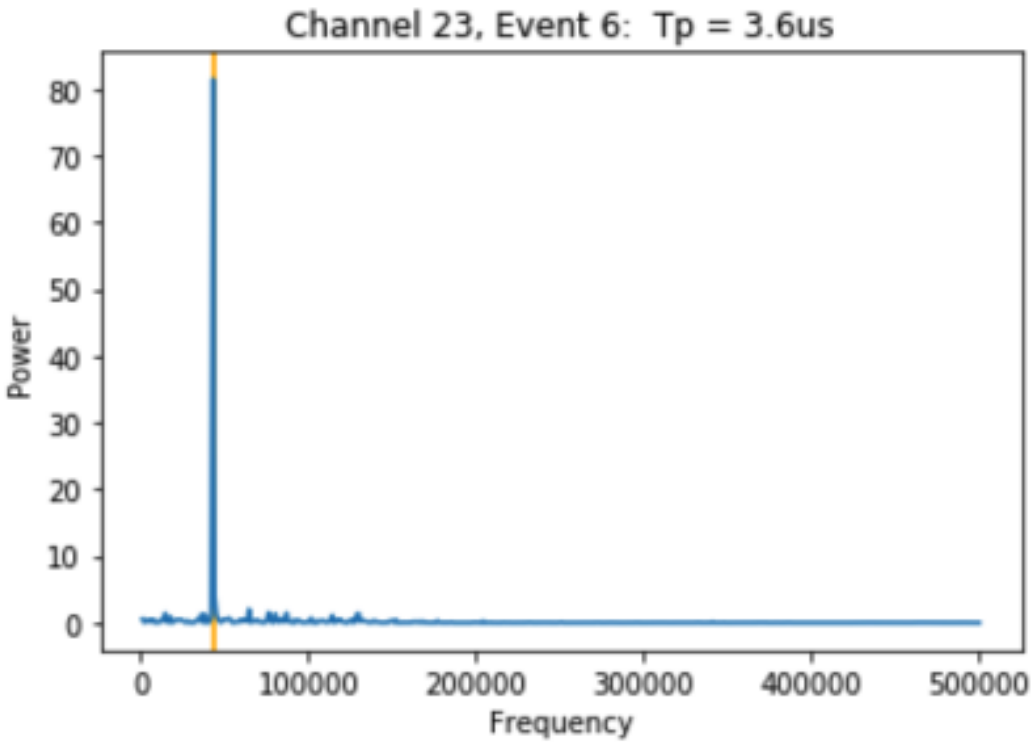

Figure 6.10 We investigate channels looking for abnormalities. Fourier analysis shows that when plotting noise over frequencies, some channels include an intense peak at 43kHz. Here we see channel 23 showing this peak with a shaping at 3.6us. Visual inspection of the waveform is sinusoidal and matches this frequency result.

Grounding block diagram

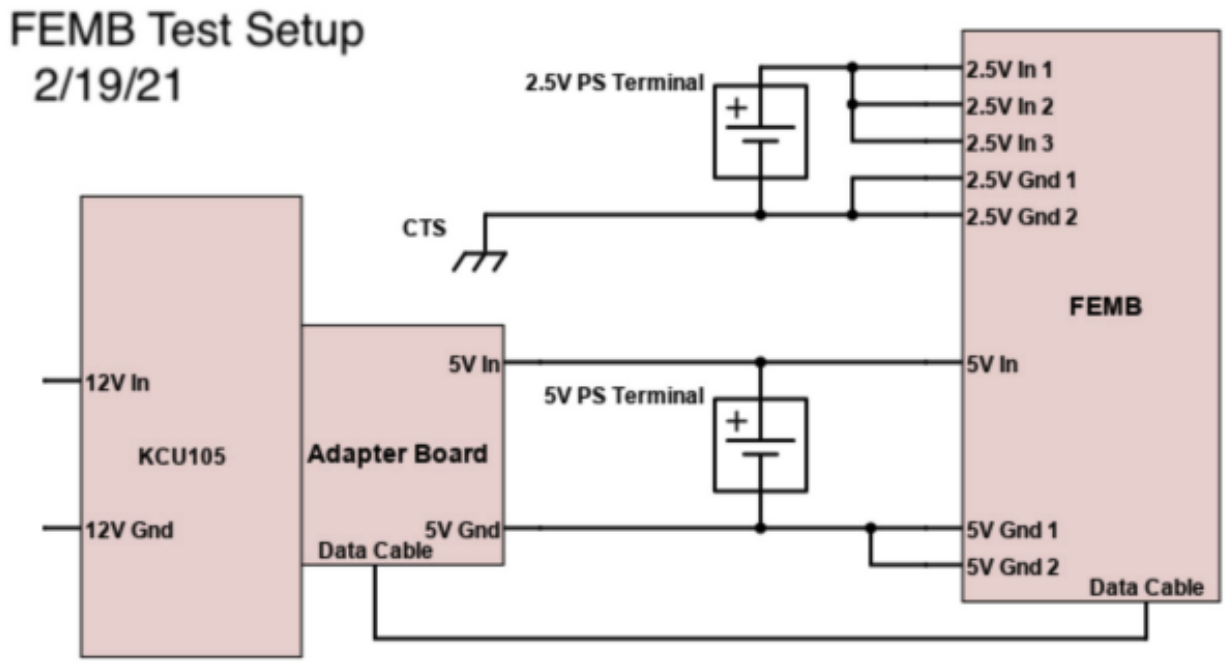

Figure 6.11 Block diagram of components, boards, and power scheme for ground. The FPGA and adapter board have their own power source and the floating grounds are tied together by ground braid to the CTS ground. This is then tied to a wall outlet and to earth.

Speculation for causes narrowed down to interference in the testing environment, so a different building was used for another test. This resulted in the same observations, and hopes for improvement were left for a new Revision B FEMB.

Further testing of the FEMB and ASICs performance is seen in Figure 6.13 where we compare the noise values of both ASICs separately. We can see that they are similar in value and performing as expected. Figure 6.14 compares the average noise with and without the toy TPCs installed on the FEMB inputs and allows.

Final tests including bypassing internal CRYO LDOs and supplying the ASICs with power from external 1 volt and 2 volt FEMB options. Unfortunately, no change in

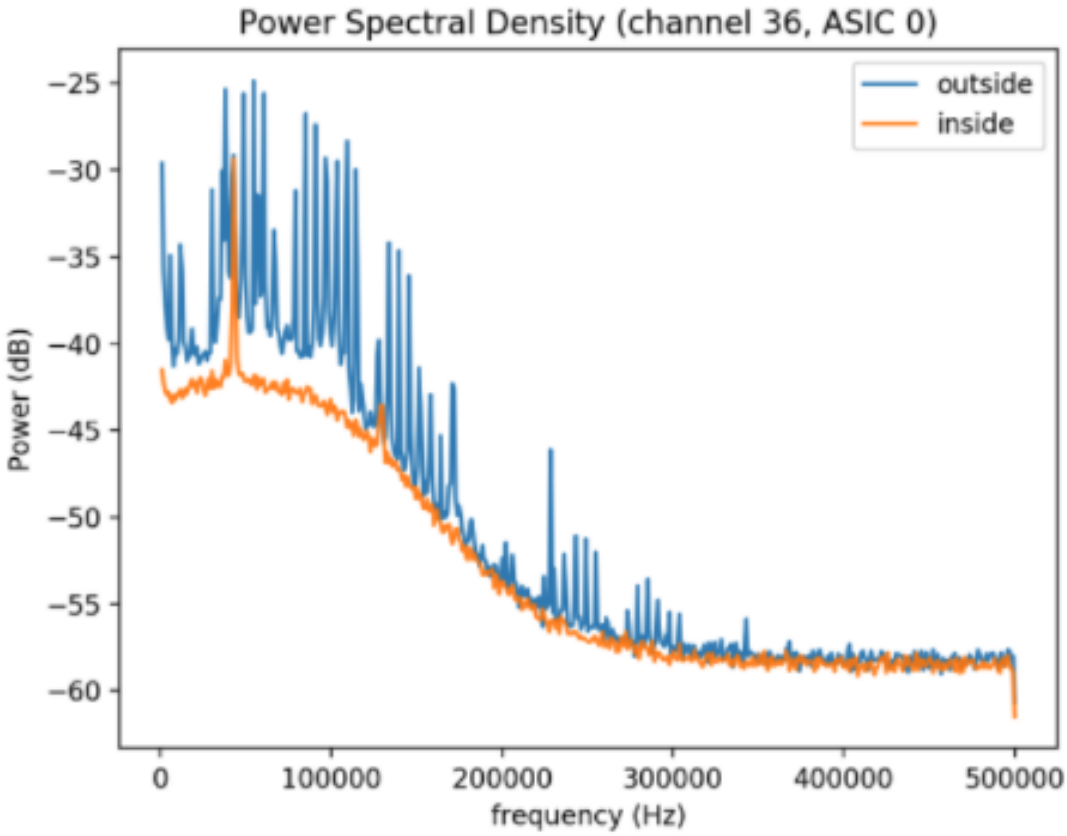

Figure 6.12 Noise spectra comparison of the FEMB either inside or outside the CTS test sink. The additional shielding of the sink cleans up external noise and produces a more nominal power spectra. With the FEMB responding at this sensitivity, proper shielding needs to be done to isolate the FEMBs from any outside interference. Orange plotted results show a clean power spectra, with the repeated 43kHz noise peak still observed.

Comparison of the STDs

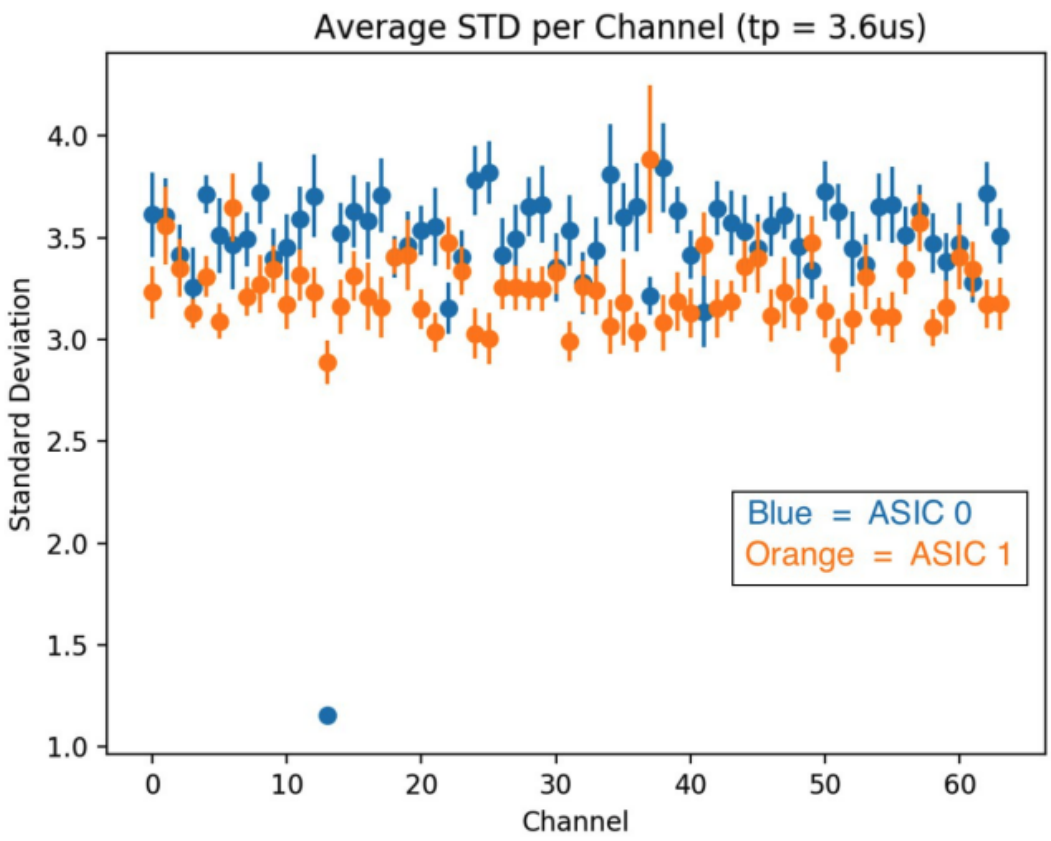

Figure 6.13 A comparison of the standard deviations of noise on both ASICs. Similar noise is seen with both left and right (0 and 1) CRYO ASICs. Expected results due to symmetry of the FEMB.

performance or noise were observed. Final analysis using the Revision A FEMB shows that additional capacitance is needed to reduce noise, as well as better shielding and grounding options.

Toy TPC Comparison

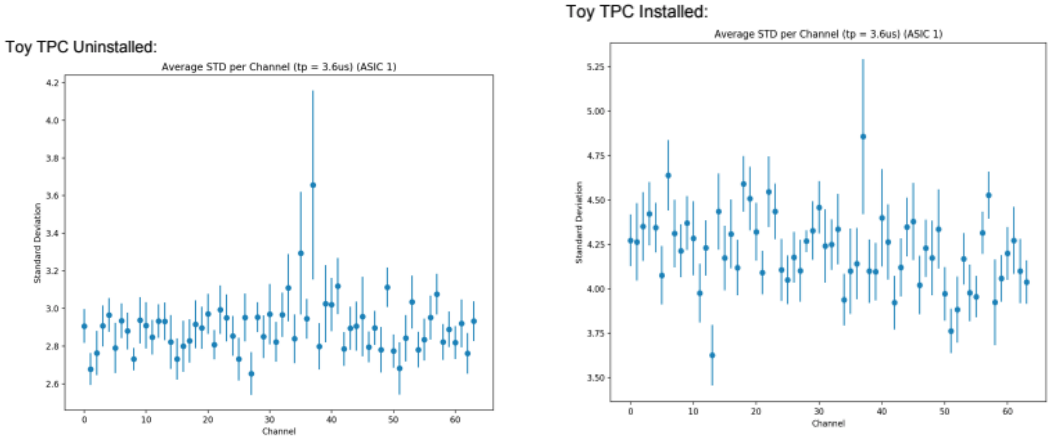

Figure 6.14 Comparison of the noise with a toy TPC installed on the FEMB channel inputs. The left plot shows the noise with no TPC on the 64 channel inputs. The right plot has the TPC installed on the same ASIC in a new test trial with all other conditions kept the same.

6.2 FEMB Revision B Tests and Results

Following the testing of the Revision A board, updates were made to the design as mentioned in Chapter 3. After reviews were done, the new design was sent out for a production of a few boards. Figure 6.15 shows the fabricated and assembled FEMB Revision B.

Upon receiving the assembled Revision B FEMBs, minor usability tests were started. Similar to the tests done with Revision A, SACI interface and register tests were all passed. A 224MHz data clock was still in use since connection failures occurred at full speed. Final usability tests included the test patterns at the digital level of the CRYOs and everything performed as expected.

With proper connection and performance, the boards were placed within the CTS sink for shielding. The first data run produced a power spectra and we compared them to similar spectra from Revision A, compared in Figure 6.16. Along with the spectral comparison, the standard deviations of input channels were plotted and Figure 6.17 compares the new revision to the previous FEMB.

We test the new FEMB across all peaking times and see expected performance at lower noises, as shown in Figure 6.18. Figure 6.19 now shows the power spectra of the same conditions and peaking times. Figure 6.20 plots the same data from the second ASIC, this time with a toy TPC attached at the channel inputs.

As expected, the increase in overall board and ASIC capacitance lowered the baseline noise, and provided a power spectra that matched the expected performance from ASIC test simulations. All tests here showed better performance, however the previously seen 43kHz noise was still present. We consider the option that this noise may be auditory, though outside the reach of human hearing. Plans to continue tests, next within liquid Nitrogen were begun.

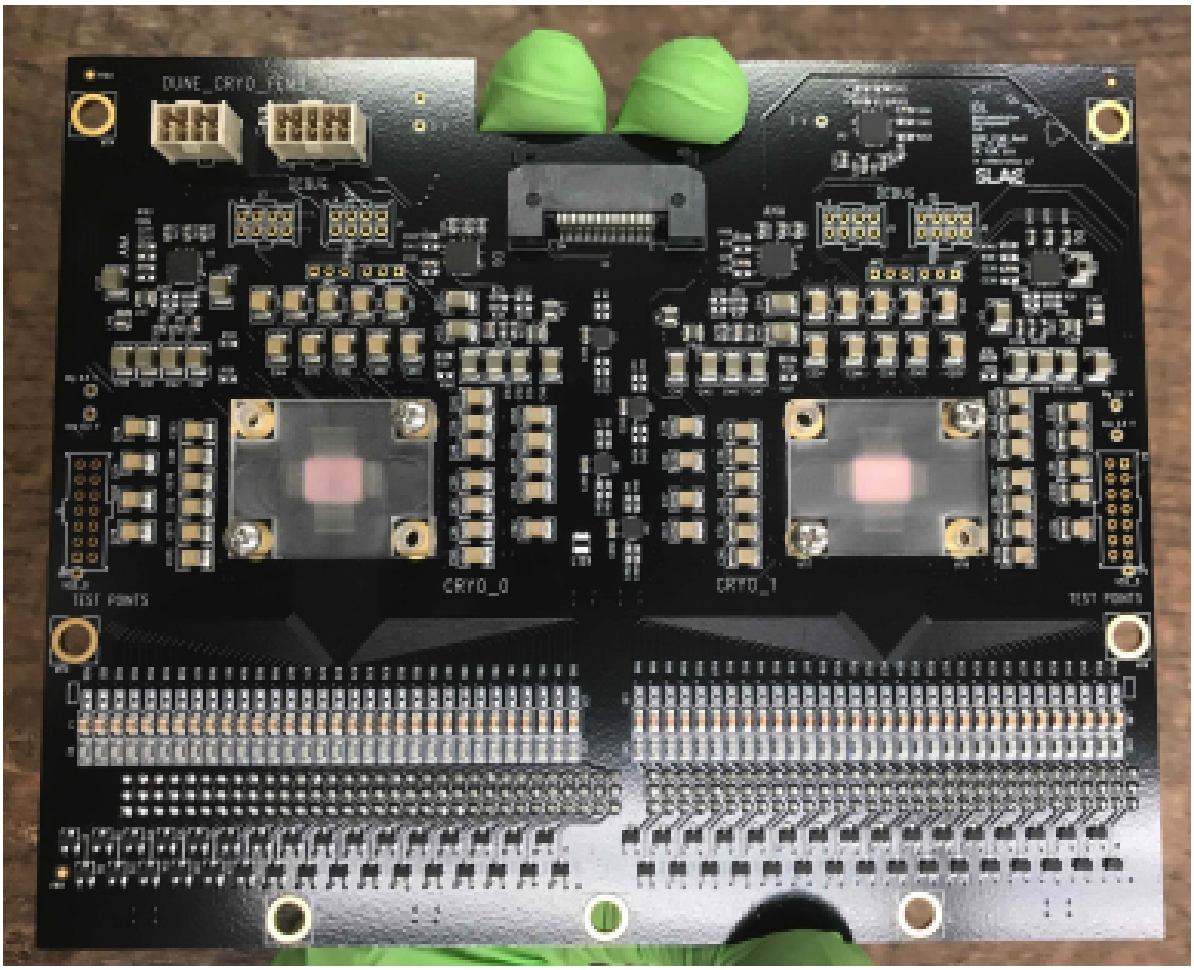

Figure 6.15 FEMB Revision B: Fabricated and assembled, with CRYOs wire bonded to the board; 240 wire bonds per ASIC. Plastic covers again are used, however with various sets of spacers to provide more space above the ASIC. Mounting holes are now finalized in quantity and location.

Comparison of Revision A and B spectra

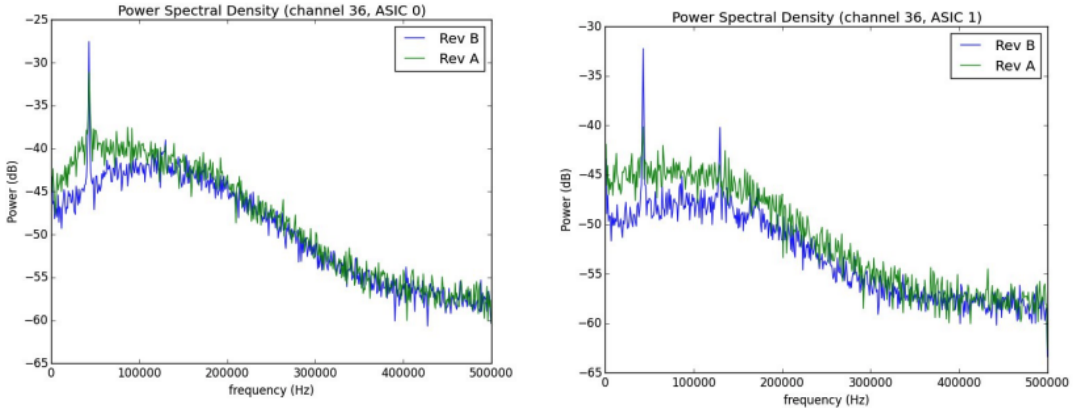

Figure 6.16 Comparison of the spectra of Revision A and Revision B. Left plot is ASIC 0 and right is ASIC 1. Revision B results in lower noise from initial tests and no additional changes.

Comparison of Revision A and B std

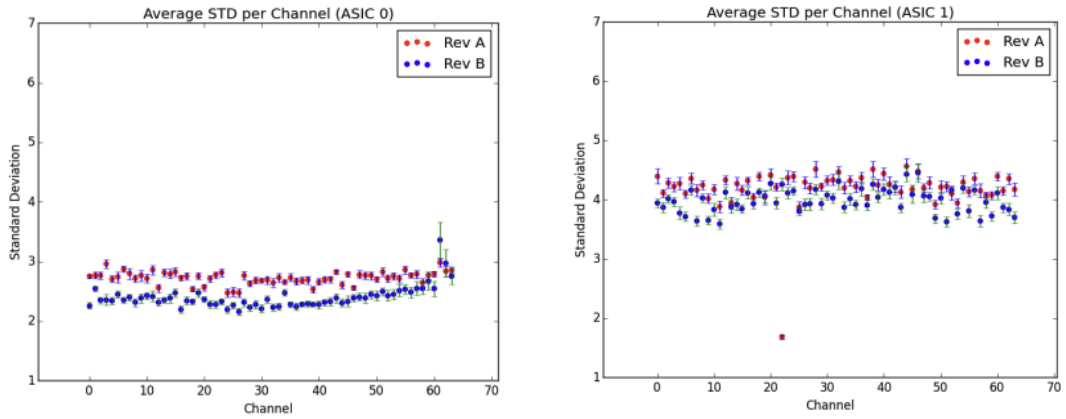

Figure 6.17 Comparison of the standard deviations of Revision A and B. Left plot is ASIC 0 and right is ASIC 1 where a toy tpc is installed. Revision B out performs Revision A in both cases, with no additional changes to the testing setup.

Comparison of Peaking Times

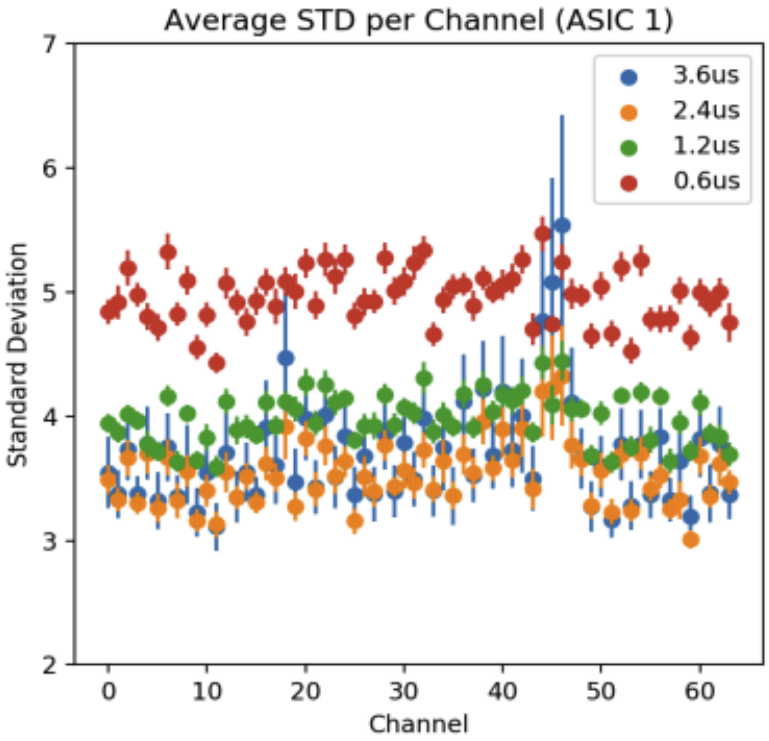

Figure 6.18 A comparison of different peaking times for FEMB Rev B. The standard deviation reduces on average, with some channels showing higher noise. Causes are attributed to dirt or fingerprints on the PCB itself.

Power Spectra Asic 0

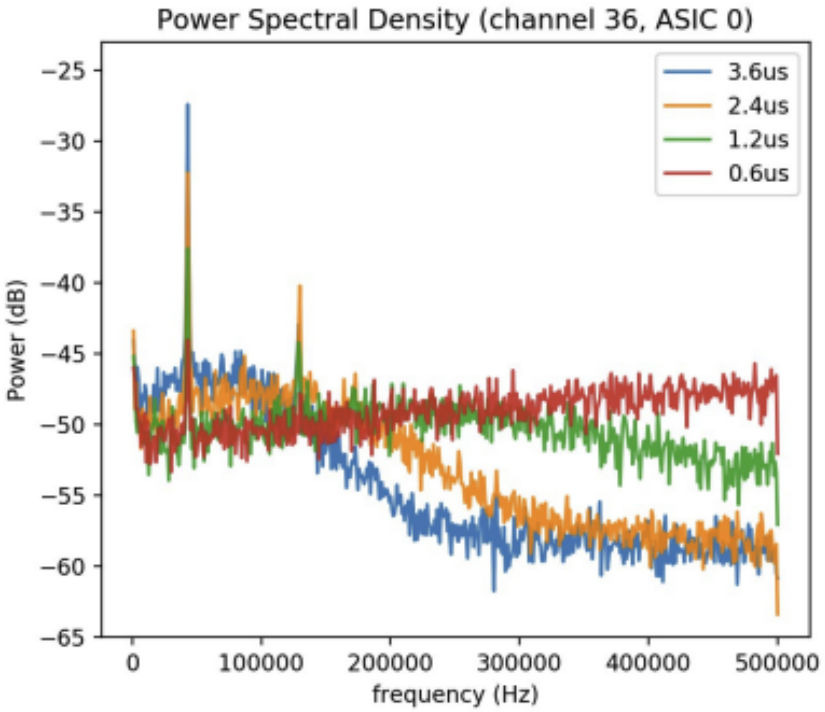

Figure 6.19 A power spectral analysis on the FEMB ASIC 0 (left). No toy tpc attached. Overall shape of all peaking times is as expected. 43kHz still present.

Power Spectra Asic 1

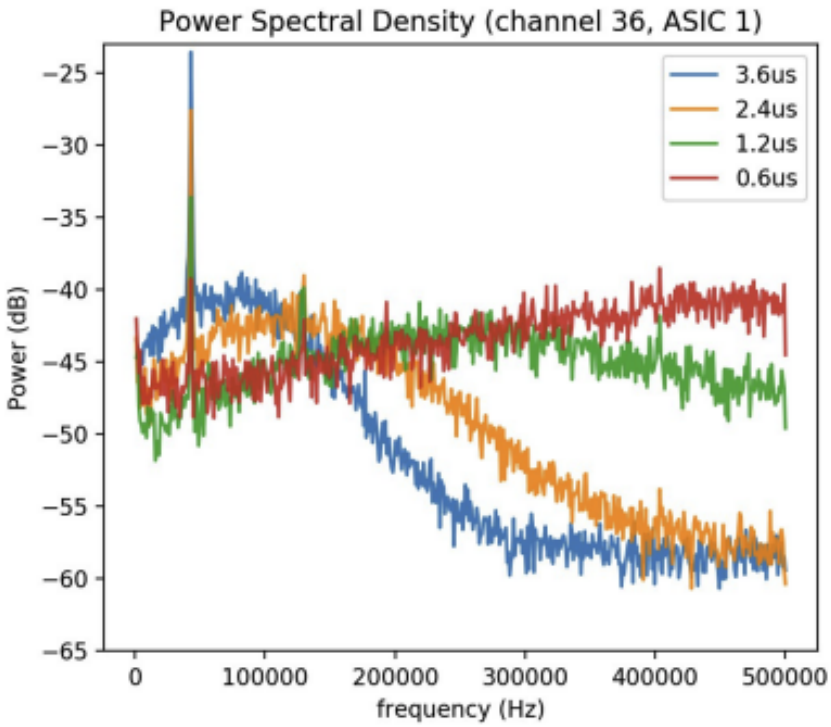

Figure 6.20 A power spectral analysis on the FEMB ASIC 1 (right). Toy tpc attached which results in higher noise and power. 43kHz still present.

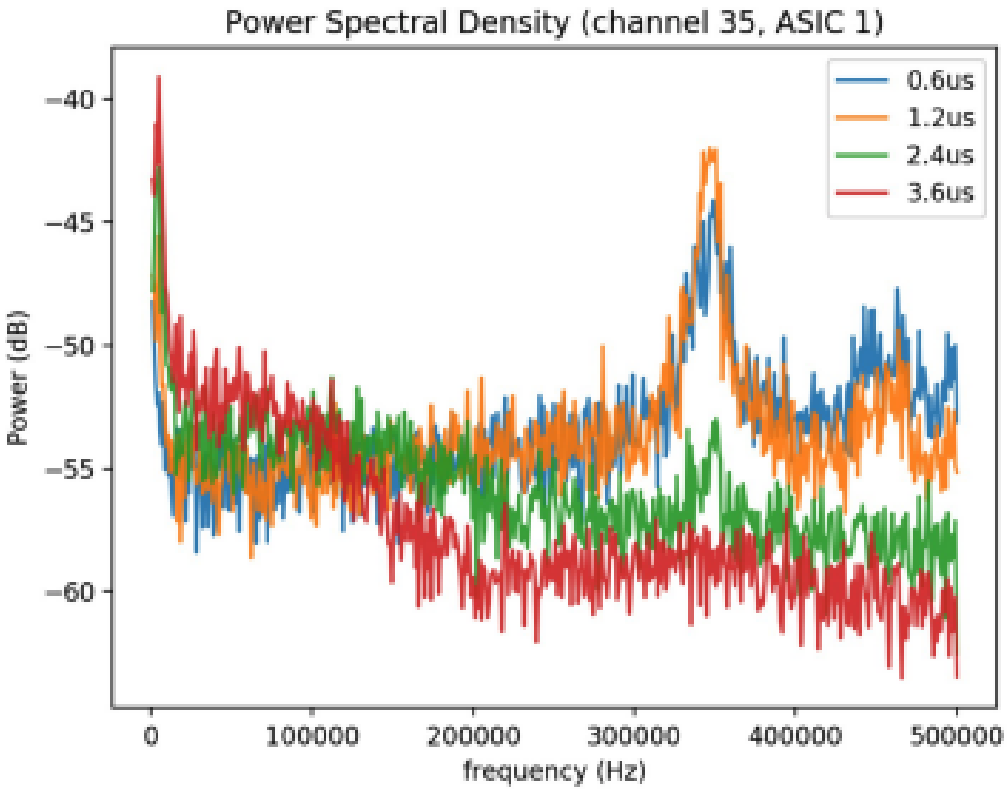

Figure 6.21 Initial power spectra from cold tests - liquid Nitrogen submersion. Noise seen in lower frequencies across all peaking times. Noise also clearly seen in lower peaking times around 350kHz.

6.3 Cold Testing within CTS - Liquid Nitrogen Submersion

Setup and fill of the CTS is outlined in Appendix A. With the FEMB Revision B placed within the CTS sink, it was slowly cooled down to liquid Nitrogen temperatures, and then fully submerged. Initialization occurred normally, and the first set of cold data was able to be taken. Figure 6.21 shows the spectral analysis of this data and two sections of noise stand out. A low frequency spike is seen within the plot, as well as a high peak centered at 350kHz.

Attempts were made to remove this noise, all unsuccessful with the initial set of testing. Further cold tests resulted in similar data, and we investigated components on the FEMB. Temperature cycles might impact the components, or de-rate some of their values. After further testing, a ferrite that was used to bridge the digital and analog ground planes of the FEMB was removed and replaced with a 0ohm resistor. This change was successful and directly removed the 350kHz noise.

We also decided to tie the input protection diodes on the FEMB to the CRYO 2.5V power, rather than the raw input from the power supplies as they had been previously. The power path was reworked warm tests showed no issues. We conducted a new test within the liquid Nitrogen and discovered the low frequency noise was removed. Figure 6.22 shows this change with the new diode power scheme as well as the removal of the 350kHz noise.

With overall tests reaching desired performance, we attempted to bring our data work to full speed, 448MHz. Minor firmware changes were needed and additional initialization script updates solved the communication problems seen previously. This now gave the FEMB Revision B the required full data speed capabilities.

We also decided to make use of the RF box in a cold test, and mounted the FEMB as shown in Figure 6.23. With hopes of the best shielding possible for the board, and in combination with the CTS shielding, our results showed a full removal of the previous 43kHz spike. This occurred in both warm and cold tests, as long as the FEMB was within the RF box, and that box was placed within the CTS. We took data of the best observed results with the toy tpcs attached; power spectra and standard deviation shown in Figure 6.24 and Figure 6.25.

The results here are to simulation, and able to be reproduced with multiple tests and trials in warm/room temperatures. Cold tests show similar good results, however not across all 128 channels of the FEMB. An overall yield issue of channels occurs the moment the board is submerged within the Nitrogen. Our first cool down and cold run yielded mixed results across the two CRYOs. ASIC 0 lost the top bank of data, and only had results for the bottom bank/channels 33-64. ASIC 1 provided low noise and a full set of working

diode change

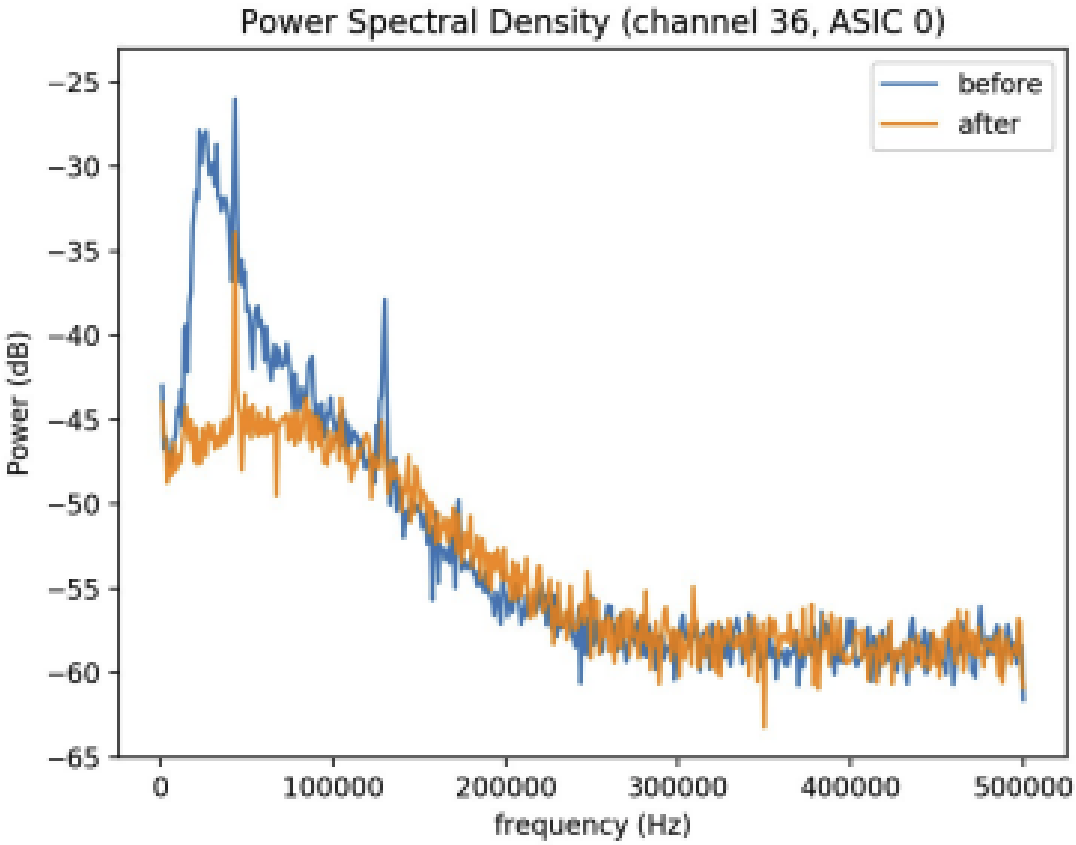

Figure 6.22 Cold power spectra, before and after diode power rail rework. We see the lower frequency noise is removed with the new diode power.

64 channels as seen in Figure 6.26. We also show the standard deviation of the noise in Figures 6.27 and 6.28.

Tests of board capacitance changing due to temperature cycles did not provide different results or revival of the dead channels. We further tested this performance within the liquid Nitrogen, and determine that an issue may lie with the analog portion of the CRYO ASICs. The digital side is confirmed to be operational, as when the test patterns are looked at, all channels behave normally. We have been able to produce these test patterns of high and low alternating voltages in all cold trials.

RF Box

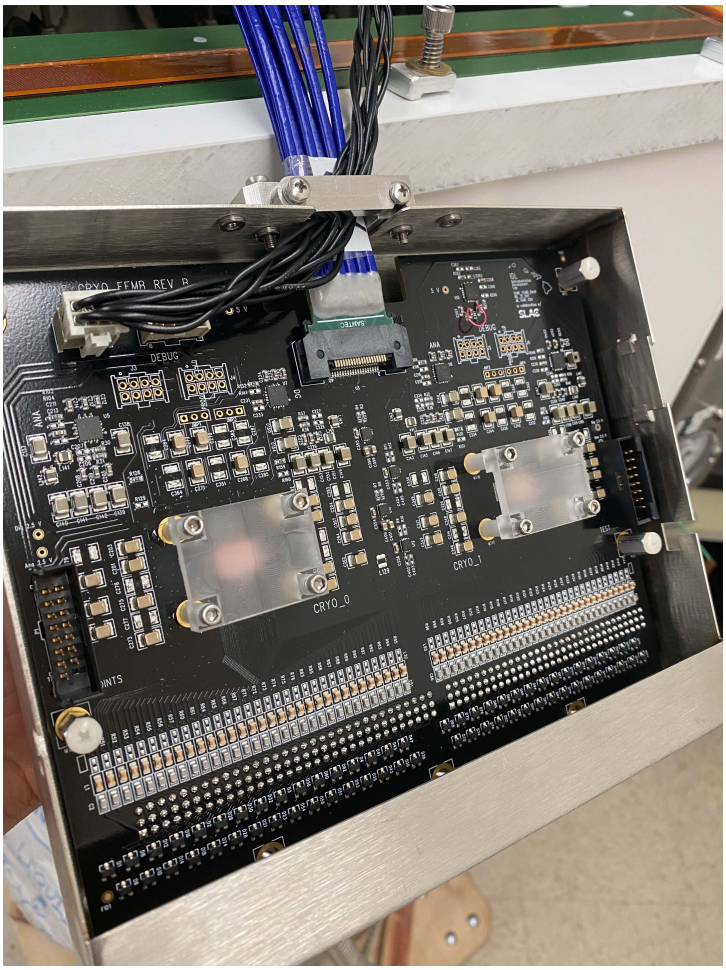

Figure 6.23 RF box with FEMB Revision B installed. The RF box cover is removed for viewing, though installed and sealed when under test or placed within CTS sink. Fully enclosed box has ports for power and data cables as well as the 128 channel inputs. RF box is also grounded to the shared ground of the test apparatus.

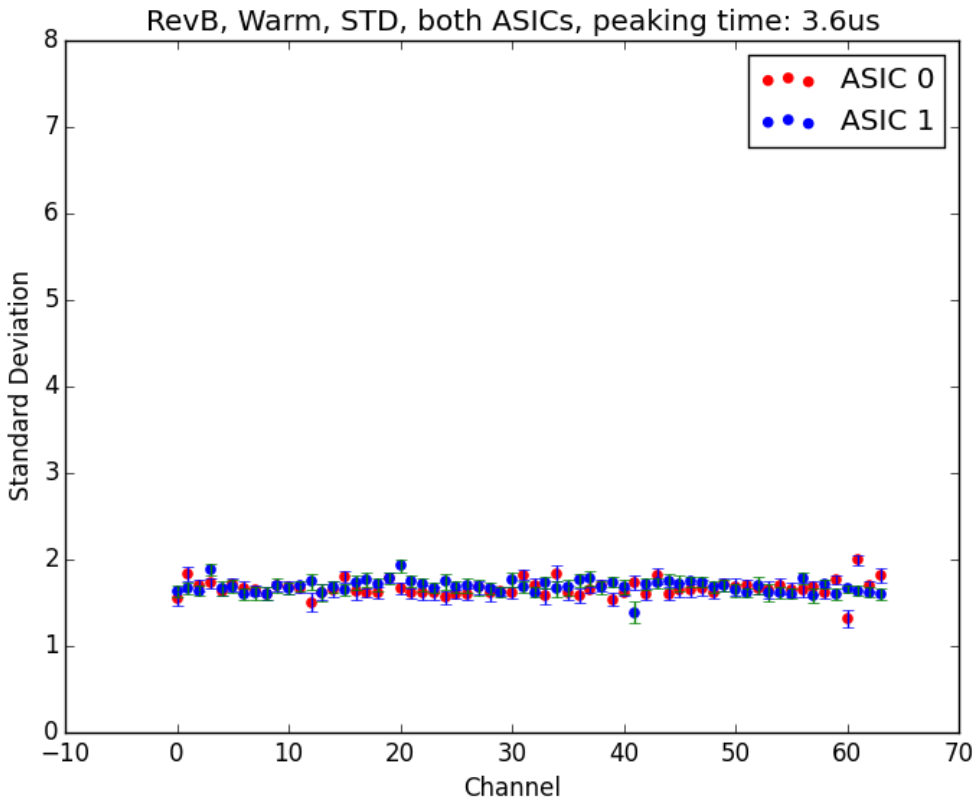

Figure 6.24 Lowest noise measurements with the FEMB at full speed of both ASICs. Lowest recorded noise at warm, and maintains uniform results across many tests.

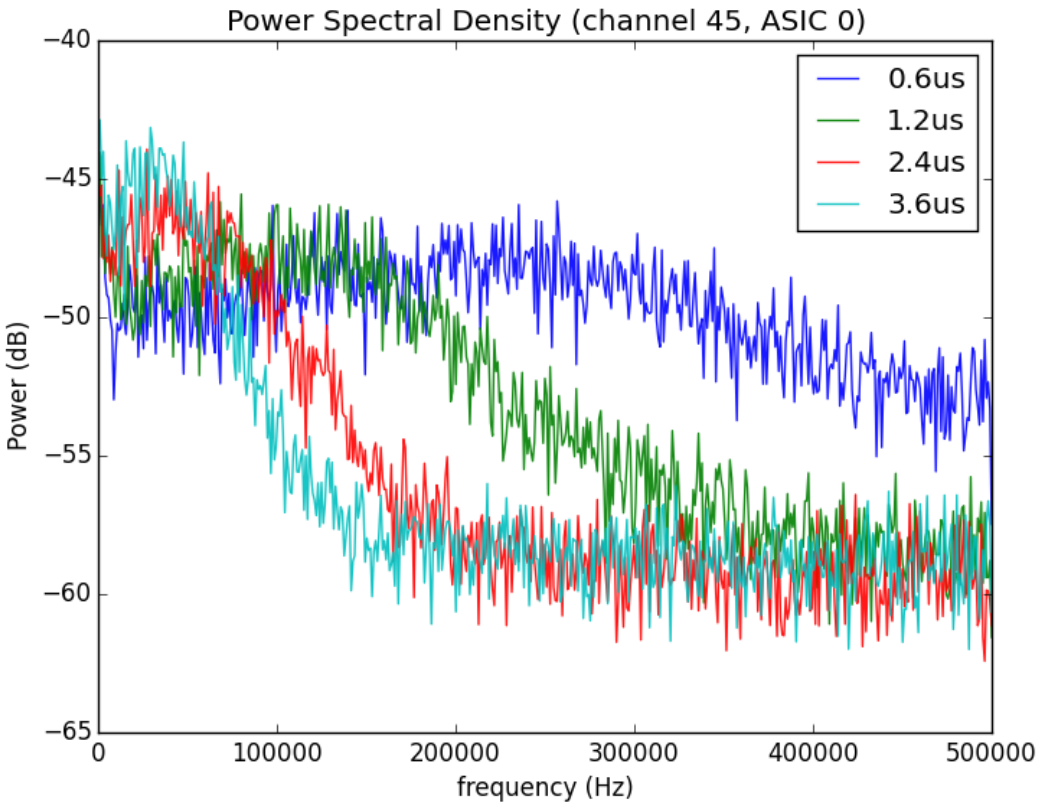

Figure 6.25 Best Spectra with the FEMB at full speed, with all shielding and toy tpcs. Matches expected results of simulations.

cold live

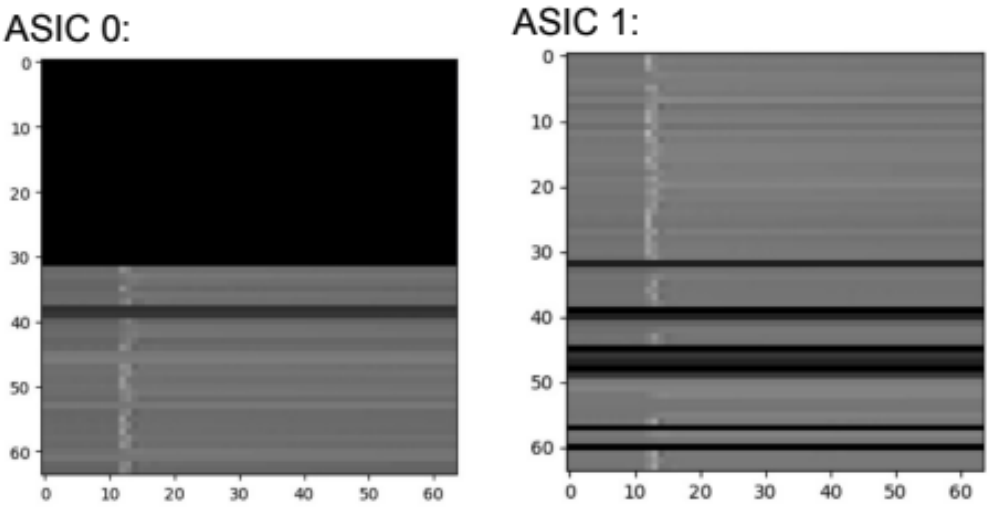

Figure 6.26 Live feed as seen on GUI of both CRYO ASICs. Top bank of ASIC 0 is not providing any data, while some channels in ASIC 1 are dead, potentially due to dirt on board.

FEMB Cold ASIC 0

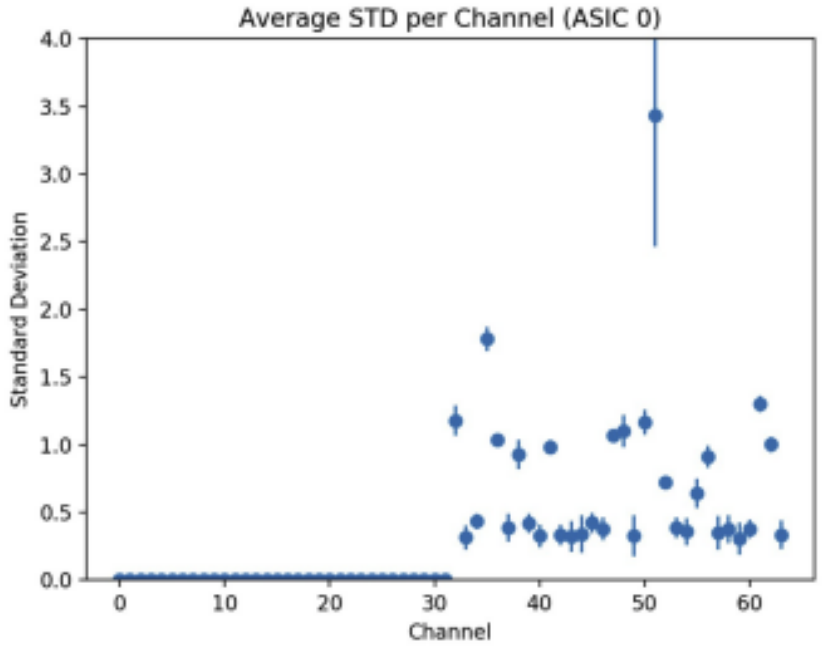

Figure 6.27 FEMB Revision B, cold and submerged in liquid nitrogen. ASIC 0 shows the first 32 channels as unresponsive with no wave forms. Upper bank does not have a fully clear noise level, though is still performing cleaner than when warm

FEMB Cold ASIC 1

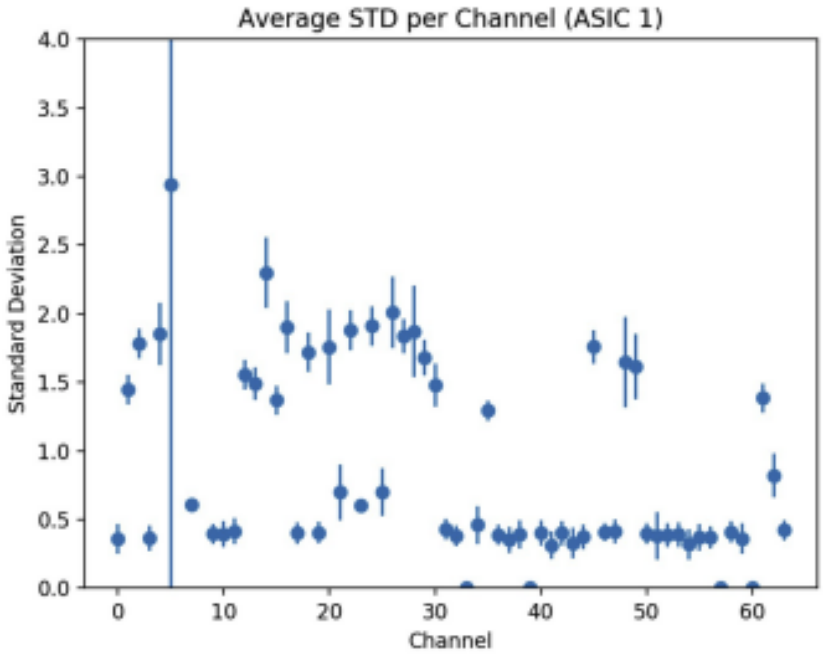

Figure 6.28 FEMB Revision B, cold and submerged in liquid nitrogen. ASIC 1 with a TPC installed, and both banks are working. No quantifiable noise level, though still performing cleaner than when warm.

Chapter 7

Summary and Future Perspectives

7.1 Conclusion

The Deep Underground Neutrino Experiment will be the premier experiment in the coming decades for neutrino science and proton decay studies. The Far Detector in Sanford will also be the largest argon neutrino detector ever built and will not just capture neutrinos as planned from Fermilab, but also extend towards cosmic particles for additional science and discovery.

The design and building of DUNE is being conducted and tested with plans of at least 20 years of operation. The cold electronics that will be used within the detector modules need to survive and operate at liquid argon temperatures, with noise not exceeding 1000 electrons per second per channel. As a potential solution, a 10 layer Front End Motherboard was designed using the CRYO ASIC, to take the captured electron/neutrino interactions, digitize the data and interface to external computers for saving data and reconstructing the neutrino interactions.

The design of the FEMB started with an initial Revision A board, where all of the brute testing was done. The connection and programming of the CRYO ASICs was accomplished and resulted in the needed updates for a Revision B FEMB. This new board was able to achieve noise measurements within specifications and match the desired outcome that was seen in simulations of the electronics. Warm tests with this Rev B board produced the best

power spectral analysis and lowest noise measurements, once many layers of shielding was used. The RF box was a mandatory shield as well as the additional shielding of the CTS.

Cold tests of the FEMB RevB provided decent, yet non-uniform results. The board was able to perform overall within liquid nitrogen submersion however the channel yield fluctuated between 50% - 75%. As requirements state a $> 99\%$ yield for long term use of detector, further ASIC and FEMB testing needs to be conducted to ensure proper channel yield prior to being implemented in ICEBERG tests. Avenues to explore here may include internal powering of the CRYO and its LDOs. While cold temperatures may not necessarily de-rate component values to the point of failure, higher tolerance components might provide additional results. A final test may come from the power sequencing of the CRYO. These ideas are all currently being investigated.

7.2 Future Steps

An FEMB Revision C board will be submitted to include these following changes: Higher capacitance on all of the internal LDO circuits, separated diode planes for the input circuitry for each ASIC, and minor silk screen updates. These updates will make permanent any needed reworks from testing, as well as incorporating results for the best possible performance. The Bill of Materials for this design will be updated to include better specifications on components, mainly temperature and voltage tolerances of the capacitors.

With good yields in future CRYO ASIC quality and an FEMB Revision C tested, multiple boards can be produced and verified to operate to specification. After ICEBERG tests, a mass production of these CRYO FEMBs will be considered in the design of the cold electronics for the DUNE FD, with first light currently set for year 2029.

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Appendix A

CTS Operation & Refill

Normal operation procedure

The operation of the CTS is controlled by a up/down switch which selects one of the four operating modes of the device. This is the only control provided to the operator. An LCD display provides diagnostic information, shows the amount of LN2 remaining in the storage dewar, and provides error messages in case of any detected malfunction.

Definitions:

CTS is the Cryogenic Testing System

DUT is the Device Under Test (for instance a ProtoDUNE circuit board, or ProtoDUNE FEMB)

In case something goes wrong:

The CTS is designed to be intrinsically safe. In the case of unexpected system behavior simply turn off the system power switch. The CTS can be safely powered off from any of the operating states of the machine.

For a typical cycle follow these steps:

(1) The machine, when not in use, should be set to IDLE or powered off

(2) Place the DUT and its fixture into the top plate of the CTS

(3) Select WARM GN2 mode and wait at least 5 minutes for warming and purging

(4) Select COLD GN2 mode and wait until the test chamber temperature decreases to the desired value

(5) Select LN2 IMMERSE mode and wait until the display indicates that the device is immersed

(6) Perform electrical tests of the DUT

(7) Select WARM GN2 mode. Note: the CTS will drain the test chamber before warming up.

(8) Wait until the chamber temperature warms up and then an additional 5-10 minutes to thoroughly warm up the DUT

(9) Select IDLE mode

(10) Remove the DUT from the top plate Note: Many of the steps above involve waiting for temperatures to equilibrate on the DUT. The proposed times should be explored experimentally to determine sufficient durations.

Storage dewar refill procedure:

The storage dewar will need occasional liquid nitrogen refilling. The frequency of refills depends on many factors including frequency of use, timing of the different stages of operation, and the thermal mass of the DUT.

Important: Ensure that the CTS is filled from a source that supplies a LN2 at a maximum pressure of 22 psig. Supplying LN2 from a source delivering higher pressures may cause LN2 to be emitted from the safety relief valve at the CTS filling port.

Procedure for storage dewar refilling:

(1) Locate a liquid nitrogen transfer dewar that holds a pressure of 22 psig. This is a common pressure for transfer dewars. Do not fill the CTS from a liquid nitrogen source with over 22 psig pressure.

(2) Disconnect the three silicone rubber plugs from the SD adapter. These are attached to the LN2 filling port with bead chain lanyards. The opening of these ports allows sufficient venting of the system to prevent LN2 from being pushed into the test chamber.

(3) Remove the black plastic cap from the liquid fill port.

(4) Connect the liquid nitrogen transfer line to the filling port on the CTS

(5) Open the valve on the transfer dewar.

(6) Monitor the venting port on the side of the CTS. This port is connected to a tube that extends partway into the dewar. When the liquid level in the storage dewar reaches the short fill tube this port will start to emit LN2. At this point the storage dewar is full and the valve on the transfer dewar should be closed.

(7) Remove the LN2 transfer line from the CTS.

(8) Replace the blanking plug over the LN2 fill port.

(9) Replace the three silicone rubber plugs on the SD adapter.

Appendix B

Operation Procedures

Setup

-Xilinx board gets set up with proper Universal Asynchronous Receiver Transmitter (UART) settings with 1.8V at the interface to the adapter board.

-Firmware is already preloaded in flash, but the .bit file is always accessible.

-The FEMB is then placed in the RF box for shielding, and placed in the test chamber of the CTS.

-If cold tests are being conducted, the CTS is brought up as noted in Appendix A and used to cool the board down to liquid nitrogen temperatures prior to any power supplies being turned on, otherwise nothing here for a warm test

-Power supplies are used to provide 2.5V and 5.1V to their respective power cables and devices.

-Software ran from terminal

GUI

An autonomous pipeline is usually used, where the initialization includes proper register settings (.yml files included in Appendix C).

The ASICs are set to start reading out data

The triggering is set on with time as 100000000

The length of the data frames is set to 32768

The baseline is set to a value of 0x4

Trigger registers are changed to 0x8000

Data is then taken and saved with signals either pulsing across the channels, or a steady baseline and peaking time set for noise measurements.

The .dat files are processed and converted to .hdf5 files and then can be investigated

Appendix C

YML Configuration Files

We attach here a sample .yml configuration file used for initialization. The current one here is used to program the left/0 ASIC on the FEMB while at room temperature.

When programming the right/1 ASIC, only labels are changed, CryoAsic0 becomes CryoAsic1.

When testing within the CTS and in liquid Nitrogen, the internal LDO values slightly change. The user here should adjust the values of registers: LDO VTBias B0, LDO VTBias T0, LDO VTBias Br0, and LDO VTBias Tr0

```
cryoAsicGen1:
  enable: True
  ForceWrite: False
  KCU105FEMBCryo:
    enable: True
    CryoAsic0:
      enable: True
      TPS_DAC: 0x3c
      TPS_GR: 0x1
      TPSMux: 0x0
      Bias_TPS_Buffer: 0x5
      Bias_TPS: 0x4
      Bias_TPS_DAC: 0x4
      Bias_LVDS_Rx: 0x0
      Bias_LVDS_Tx: 0x0
      RbiasEn: False
      Pulser: 0x370
      test: True
      atest: False
      hrtest: False
      sbatest: False
      pbit: False
      Pulser_Reset: False
      PPbit: True
      test_BE: False
      DelEXEC: False
      DelCCKreg: False
      sync_exten: False
      sync_role_sel: True
      RO_Bk0_disable: False
      RO_Bk1_disable: False
      DM1en: False
      DM2en: False
      Pulser_Monost: 0x0
      cs_LVDS_Tx: 0x0
      DCycle_en: False
      DCycle_bypass: False
      DCycle_polarity: False
      DCycle_DAC: 0x20
      Bias_DCycle_DAC: 0x4
      PLL_RO_OutDivider: 0x0
      PLL_DCycle_Bypass_B0: 0x3
      PLL_RO_Reset: True
      PLL_RO_Itune: 0x3
      PLL_RO_KVCO: 0x1
      PLL_RO_filter1: 0x5
      PLL_RO_filter2: 0x4
      Dcycle_DAC_gain: 0x3
      VTBias_B0: 0x2
      VTBias_T0: 0xe
      SAH_B0: 0x0
      SAH_VcmBuf_B0: 0x0
      SigBuf_B0: 0x0
      ADC_VrefBuf_B0: 0x0
      ADC_B0: 0x3
```

```
ADC_VcmBuf_B0: 0x0
bamp: 0x4
bleak: 0x2
brstVref: 0x4
SAH_Ctrl_Visel: False
ADC_Ocen_Bk0: True
ADC_Ocen_Bk1: True
VrefBuffExt_En_Bk0: True
VrefBuffExt_En_Bk1: True
ROsLVDS_bit: True
SACIsLVDS_bit: True
emph_bc: 0x0
emph_bd: 0x0
DM1sel: 0x0
DM2sel: 0x0
SubBnkEn: 0xFFFF
LDO_VTBias_B0: 0x2
LDO_VTBias_T0: 0x7
LDO_VTBias_Br0: 0x1
LDO_VTBias_Tr0: 0x2
TPS_DAC_Gain: 0x3
LDO0TB_En: True
LDO0rTB_En: True
LDO1TB_En: True
LDO2TB_En: True
LDO46_En: True
encoder_mode_dft: 0x0
En_BankClk_Bk0_LVDS: False
En_BankClk_Bk1_LVDS: False
En_SerClk_out_Bk0_LVDS: True
En_SerClk_out_Bk1_LVDS: True
rtrimLVDS_b0: 0x2
SACItristateLVDS_bit: False
VrefGen_B0_1v2: 0x3
VrefGen_Br0_1v2: 0x3
VrefGen_T0_1v2: 0xf
VrefGen_Tc0_1v2: 0xf
VrefGen_Tr0_1v2: 0x0
VrefBuf_Ext_B0_1v2: 0x3
VcmBuf_Ext_B0_1v2: 0x0
FE_Amp_B0_1v2: 0x2
bifb: 0x3
bbaseref: 0x3
blcoarse: 0x3
ctrl_pulser: False
Pulser_Bias_DAC_b0: 0x4
PP_Pulser_Bias_DAC: True
Pulser_Bias_Monost_b0: 0x3
ensdps: False
enrefps: False
Ana_Mon_Cal: False
ADC_B3B2: 0x2
CRYO_ID: 0x0
AppFpgaRegisters:
  enable: True
  Version: 0x2
```

GlblRstPolarity: True
GlblRstDelay: 0
GlblRstWidth: 0
AcqPolarity: False
AcqDelay1: 1000
AcqWidth1: 100000
AcqDelay2: 0
AcqWidth2: 0
TPulsePolarity: False
TPulseDelay: 0
TPulseWidth: 0
StartPolarity: False
StartDelay: 0
StartWidth: 0
PPbePolarity: False
PPbeDelay: 0
PPbeWidth: 0
SampClkEn: False
SyncPolarity: True
SyncDelay: 0
SyncWidth: 0
SaciSyncPolarity: False
SaciSyncDelay: 0
SaciSyncWidth: 0
SR0Polarity: False
Vid: 0
ResetCounters: False
AsicPwrEnable: True
AsicPwrManual: False
AsicPwrManualDig: False
AsicPwrManualAna: False
AsicPwrManualIo: False
AsicPwrManualFpga: False
DebugSel1: 9
DebugSel2: 3
StartupReq: True