View-Based Owicki-Gries Reasoning for Persistent x86-TSO (Extended Version)*

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Abstract. The rise of persistent memory is disrupting computing to its core. Our work aims to help programmers navigate this brave new world by providing a program logic for reasoning about x86 code that uses low-level operations such as memory accesses and fences, as well as persistency primitives such as flushes. Our logic, Pierogi, benefits from a simple underlying operational semantics based on *views*, is able to handle *optimised* flush operations, and is mechanised in the Isabelle/HOL proof assistant. We detail the proof rules of Pierogi and prove them sound. We also show how Pierogi can be used to reason about a range of challenging single- and multi-threaded persistent programs.

1 Introduction

In our era of big data, the long-established boundary between 'memory' and 'storage' is increasingly blurred. Persistent memory is a technology that sits in both camps, promising both the durability of disks and data access times similar to those of DRAM. Embracing this technology requires rethinking our decades-old programming paradigms. As data held in memory is no longer wiped after a system restart, there is an opportunity to write *persistent* programs – programs that can recover their progress and continue computing even after a crash.

However, writing persistent programs is extremely challenging, as it requires the programmer to keep track of which memory writes have become persistent, and which have not. This is further complicated in a multi-threaded setting by the intricate interplay between the rules of memory *persistency* (which determine

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the order in which writes become persistent) and those of memory *consistency* (which determine what data can be observed by which threads).

To address this difficulty, we provide a foundation for persistent programming. We develop a program logic, PIEROGI, for reasoning about x86 code that uses low-level operations such as memory accesses and fences, as well as persistency primitives such as flushes. We demonstrate the utility of Pierogi by using it to reason about a range of challenging single- and multi-threaded persistent programs, including some that demonstrate the subtle interplay between optimised flush (flush_{opt}) and store fence (sfence) instructions. Using the Isabelle/HOL proof assistant, we have mechanised the PIEROGI rules and proved them sound with respect to an operational semantics for x86 persistency [7]. One benefit of our Isabelle/HOL formalisation is that PIEROGI is already partially automated: once the user has produced a proof outline (i.e. annotated each instruction with a postcondition), they can simply use Isabelle/HOL's sledgehammer, which automatically decides which axioms and rules of the proof system need invoking to verify the whole program. Our mechanisation, which includes all the example programs discussed in this paper, is available as auxiliary material [3]. State of the art To our knowledge, the only program logic for persistent programs is POG (Persistent Owicki-Gries) [23]. As with Pierogi, POG enables reasoning about persistent x86 programs and is based on the Owicki-Gries method [22]. However, unlike Pierogi, POG is not mechanised in a proof assistant, and does not support optimised flush (flush_{opt}) instructions. Optimised flush instructions are an important persistency primitive as they are considerably faster than ordinary flush instructions. Indeed, Intel's experiments on their Skylake microarchitecture indicate that they can be nine times faster when applied to buffers that hold tens of kilobytes of data [14, p. 289], and hence programmers are impelled, "If $flush_{opt}$ is available, use $flush_{opt}$ over flush." However, $flush_{opt}$ is a tricky instruction for programmers and program logic designers alike: compared to flush, flush_{opt} can be reordered with more instructions under x86.

PIEROGI can reason efficiently about x86 persistency (including **flush**_{opt} instructions) thanks to two key recent advances: 1) Px86_{view} [7], the view-based operational semantics of x86 persistency; and 2) the C11 Owicki-Gries logic [9–11] to reason about view-based operational semantics, which we adapt to Px86_{view}.

Our contributions 1) We present a program logic, called Pierogi, for reasoning about persistent x86 programs. 2) We mechanise (and partially automate) Pierogi in Isabelle/HOL, and prove it sound relative to an established operational semantics for x86 persistency. 3) We demonstrate the utility of Pierogi by using it to verify several idiomatic persistent x86 programs.

Outline We begin with an overview of memory consistency and persistency in x86 and provide an example-driven account of PIEROGI reasoning (§2). We describe the assertion language and proof rules of PIEROGI in §3, and verify a selection of programs using PIEROGI in §4. We present the view-based operational semantics of x86 persistency and prove the soundness of PIEROGI in §5.

Auxiliary material Our Isabelle/HOL mechanisation is available as auxiliary material [3].

2 Overview and Motivation

Recent operational models for weak memory use *views* to capture relaxed behaviours of concurrent programs [7,9,15,16], where the memory records the entire history of writes that have taken place thus far. This way, different threads can have different subsets of these writes (i.e. different *views*) visible to them. In what follows, we review $Px86_{view}$, a view-based operational semantics for x86 persistency (§2.1); we then describe PIEROGI using a series of running examples.

2.1 Px86_{view} at a Glance

In the literature of concurrency semantics, consistency models describe the permitted behaviours of programs by constraining the volatile memory order, i.e. the order in which memory writes are made visible to other threads, while persistency models describe the permitted behaviours of programs upon recovering from a crash (e.g. a power failure) by defining the persistent memory order, i.e. the order in which writes are committed to persistent memory. To distinguish between the two, memory stores are differentiated from memory persists: the former denotes the process of making a write visible to other threads, whilst the latter denotes the process of committing writes to persistent memory (durably).

 $Px86_{view}$ Consistency The consistency semantics of $Px86_{view}$ is that of the well-known TSO (total store ordering) [25] model, where later (in program order) reads can be reordered before earlier writes on different locations. This is illustrated in the *store buffering* (SB) example below (left):

Specifically, assuming x=y=0 initially, since $a := \mathbf{load} y$ (resp. $b := \mathbf{load} x$) can be reordered before $\mathbf{store} \ x \ 1$ (resp. $\mathbf{store} \ y \ 1$), it is possible to observe the weak behaviour $a=0 \land b=0$. A well-known way of modelling such reorderings in TSO is through $\mathit{store} \ \mathit{buffers}$: when a thread τ executes a write $\mathit{store} \ x \ v$, its effects are not immediately made visible to other threads; rather they are delayed in a thread-local (store) buffer only visible to τ , and propagated to the memory at a later time, whereby they become visible to other threads. For instance, when $\mathit{store} \ x \ 1$ and $\mathit{store} \ y \ 1$ are delayed in the respective thread buffers (and thus not visible to one another), then $a := \mathit{load} \ y \ and \ b := \mathit{load} \ x \ may \ both \ read \ 0$.

Cho et al. [7] capture this by associating each thread τ with a coherence view (also called a thread-observable view), describing the writes observable by τ . Distinct threads may have different coherence views. For instance, after executing **store** x 1 and **store** y 1, the coherence view of the left thread may include **store** x 1 and not **store** y 1, while that of the right may include **store** y 1 and not **store** y 1. This way, $a := \mathbf{load} y$ (resp. $b := \mathbf{load} x$) may read the initial value 0, as its coherence view does not include **store** y 1 (resp. **store** x 1).

After SC (sequential consistency) [19], TSO is one of the strongest consistency models and supports synchronisation patterns such as message passing, as shown

store x 1; store y 1	store x 1; flush x ; store y 1	store x 1; flush _{opt} x ; store y 1	sfence;	flush x ;	a := load y; if (a=1) store z 1
(a)	(b)	(c)	(d)	(e)	
	$ \sharp : y = 1 \Rightarrow x = 1 $		$ \sharp : y = 1 \Rightarrow x = 1 $		$\Rightarrow x=1$

Fig. 1: Example $Px86_{view}$ programs and possible values after recovery from a crash ($\frac{t}{2}$). In all examples x, y, z are distinct locations in persistent memory such that x=y=z=0 initially, and a is a (thread-local) register.

in MP above (right), where $a=7 \land b=0$ cannot be observed. Specifically, (assuming x=y=0 initially) if the right thread reads 7 from y (written by the left thread), then the left thread passes a message to the right. Under TSO, message passing ensures that the instruction writing the message and all those ordered before it (e.g. $store\ x\ 42; store\ y\ 7$) are executed (ordered) before the instruction reading it (e.g. $a:=load\ y$). As such, since $b:=load\ x$ is executed after $a:=load\ y$, if a=7 (i.e. $store\ x\ 42$ is executed before $a:=load\ y$), then b=42.

Px86_{view} Persistency Cho et al. [7] recently developed the Px86_{view} model, a view-based description of the Intel-x86 persistency semantics, which follows a buffered, relaxed persistency model. Under a buffered model, memory persists occur asynchronously [8]: they are buffered in a queue to be committed to persistent memory at a future time. This way, persists occur after their corresponding stores and as prescribed by the persistency semantics, while allowing the execution to proceed ahead of persists. As such, after recovering from a crash, only a prefix of the persistent memory order may have persisted. (The alternative is unbuffered persistency in which stores and persists happen simultaneously.)

Under relaxed persistency, the volatile and persistent memory orders may disagree: the order in which the writes are made visible to other threads may differ from the order in which they are persisted. (The alternative is *strict* persistency in which the volatile and persistent memory orders coincide.)

The relaxed and buffered persistency of $Px86_{view}$ is shown in Fig. 1a. If a crash occurs during (or after) the execution of Fig. 1a, at crash time either write may have persisted and thus $x,y \in \{0,1\}$ upon recovery. Note that the two writes cannot be reordered under Intel-x86 (TSO) consistency and thus at no point during the normal (non-crashing) execution of Fig. 1a is x=0,y=1 observable. Nevertheless, in case of a crash it is possible to observe x=0,y=1 after recovery. That is, due to the relaxed persistency of $Px86_{view}$, the store order (x before y) is separate from the persist order (y before x). More concretely, under $Px86_{view}$ the writes may persist 1) in any order, when they are on distinct locations; or 2) in the volatile memory order, when they are on the same location.⁴

⁴ Given a *cache line* (a set of locations), writes on distinct cache lines may persist in any order, while writes on the same cache line persist in the volatile memory order. For brevity, we assume that each cache line contains a single location, thus forgoing the need for cache lines. However, it is straightforward to lift this assumption.

To afford more control over when pending writes are persisted, Intel-x86 provides explicit persist instructions such as **flush** x and **flush**_{opt} x that can be used to persist the pending writes on x.⁵ This is illustrated in Fig. 1b: executing **flush** x persists the earlier write on x (i.e. **store** x 1) to memory. As such, if the execution of Fig. 1b crashes and upon recovery y=1, then x=1. That is, if **store** x 1 has executed and persisted before the crash, then so must the earlier **store** x 1; **flush** x. Note that $y=1 \Rightarrow x=1$ describes a crash invariant, in that it holds upon crash recovery regardless of when (i.e. at which program point) the crash may have occurred. Observe that this crash invariant is guaranteed thanks to the ordering constraints on **flush** instructions. Specifically, **flush** instructions are ordered with respect to all writes; as such, **flush** x in Fig. 1b cannot be reordered with respect to either write, and thus upon recovery $y=1 \Rightarrow x=1$.

However, instruction reordering means that persist instructions may not execute at the intended program point and thus not guarantee the intended persist ordering. Specifically, $\mathbf{flush}_{\mathrm{opt}}\ x$ is only ordered with respect to earlier writes on x, and may be reordered with respect to later writes, as well as earlier writes on different locations. This is illustrated in Fig. 1c: $\mathbf{flush}_{\mathrm{opt}}\ x$ is not ordered with respect to $\mathbf{store}\ y\ 1$ and may be reordered after it. Therefore, if a crash occurs after $\mathbf{store}\ y\ 1$ has executed and persisted but before $\mathbf{flush}_{\mathrm{opt}}\ x$ has executed, then it is possible to observe y=1, x=0 on recovery. That is, there is no guarantee that $\mathbf{store}\ x\ 1$ persists before $\mathbf{store}\ y\ 1$, despite the intervening $\mathbf{flush}_{\mathrm{opt}}\ x$.

In order to prevent such reorderings and to strengthen the ordering constraints between flush_{opt} and later instructions, one can use either fence instructions, namely **sfence** (store fence) and **mfence** (memory fence), or atomic readmodify-write (RMW) instructions such as compare-and-set (CAS) and fetchand-add (FAA). More concretely, sfence, mfence and RMW instructions are ordered with respect to all (both earlier and later) flush_{opt}, flush and write instructions, and can be used to prevent reorderings such as that in Fig. 1c. This is illustrated in Fig. 1d. Unlike in Fig. 1c, the intervening **sfence** ensures that \mathbf{flush}_{opt} in Fig. 1d is ordered with respect to **store** y 1 and cannot be reordered after it, ensuring that **store** x 1 persists before **store** y 1 (i.e. $y=1 \Rightarrow x=1$ upon recovery), as in Fig. 1b. Note that replacing **sfence** in Fig. 1d with **mfence** or an RMW yields the same result. Alternatively, one can think of flush_{opt} x executing asynchronously, in that its effect (persisting x) does not take place immediately upon execution, but rather at a later time. However, upon executing a barrier instruction (i.e. **mfence**, **sfence** or an RMW), execution is blocked until the effect of earlier **flush**_{opt} instructions take place; that is, executing such barrier instructions ensures that earlier flush_{opt} behave synchronously (like flush).

The example in Fig. 1e illustrates how message passing can impose persist orderings on the writes of *different* threads. (Note that the program in the left thread of Fig. 1e is that of Fig. 1b.) As in MP, if a = 1, then **store** x 1; **flush** x is executed before $a := \mathbf{load} y$ (thanks to message passing). Consequently, since **store** x 1 is executed after $a := \mathbf{load} y$ when a = 1, we know **store** x 1; **flush** x

⁵ Executing flush x or flush_{opt} x persists the pending writes on all locations in the cache line of x. However, as discussed, we assume cache lines contain single locations.

Fig. 2: A PIEROGI proof sketch of message passing (MP), where the // annotation at each step identifies the PIEROGI proof rule (in §3.4) applied, and the highlighted assertions capture the effects of the preceding instruction.

is executed before **store** z 1. Therefore, if upon recovery z=1 (i.e. **store** z 1 has persisted before the crash), then x=1 (**store** x 1; **flush** x must have also persisted before the crash). As before, replacing **flush** x in Fig. 1e with **flush**_{opt} x; C yields the same result upon recovery when C is an **sfence/mfence** or an RMW.

2.2 Pierogi: View-Based Owicki-Gries Reasoning for Px86_{view}

Sequential Reasoning about Consistency using Views In Fig. 2 we present a PIEROGI proof sketch of MP. Recall that in order to account for possible write-read reorderings on Intel-x86 architectures, $Px86_{view}$ associates each thread τ with a coherence view, describing the writes visible to τ . To reason about such thread-observable views, PIEROGI supports assertions of the form $[x]_{\tau} = S$, stating that τ may read any value in the set S for location x. That is, the coherence view of τ for x consists of the writes whose values are those in S.

In the remainder of this article we enumerate the threads in our examples from left to right; e.g. the left and right threads in Fig. 2 are identified as 1 and 2, respectively. Moreover, we assume the registers of distinct threads have distinct names. The precondition P in Fig. 2 thus states that both threads may initially only read 0 for both x and $y: \forall \tau \in \{1,2\}, [x]_{\tau} = [y]_{\tau} = \{0\}.$

In the case of thread 1, we can weaken P (using the standard rule of consequence of Hoare logic – see Cons in §3) to obtain P_1 . Upon executing **store** x 42 (1) we weaken the resulting assertion by dropping the a=0 conjunct; and (2) we update the observable view of thread 1 on x to reflect the new value of x: $[x]_1 = \{42\}$; that is, after executing **store** x 42, the only value observable by thread 1 for x is 42. Similarly, after executing **store** y 7, we could assert $[y]_1 = \{7\}$; however, this is not necessary for establishing the final postcondition Q, and we thus simply weaken the postcondition to true (P_3) .

Analogously, in the case of thread 2 we weaken P to obtain Q_1 : $[y]_2 = \{0\}$ implies $[y]_2 \subseteq \{0,7\}$ and $7 \in [y]_2 \Rightarrow \langle y,7 \rangle [x]_2 = \{42\}$. Note that $7 \in [y]_2 \Rightarrow \langle y,7 \rangle [x]_2 = \{42\}$ yields a vacuously true implication as $[y]_2 = \{0\}$ and thus $7 \notin [y]_2$. The $\langle y,7 \rangle [x]_2$ denotes a *conditional view assertion* [9], capturing the essence of message passing by stating how reading a value on one location (y) affects the thread-observable view on a different location (x). More concretely,

Fig. 3: Proof sketches of Fig. 1b (left) and Fig. 1d (right)

 $\langle y,7\rangle[x]_2=\{42\}$ states that if thread 2 executes a load on y and reads value 7, it subsequently may only observe value 42 for x. This is indeed the essence of message passing in MP: once thread 2 reads 7 from y, it may only read 42 for x thereafter. As such, after executing the read instruction $a:=\operatorname{load} y$ (1) we apply the LP₁ rule (in Fig. 7) which simply replaces $[y]_2$ with the local register a in which the value of y is read; and (2) we replace the conditional assertion $\langle y,7\rangle[x]_2=\{42\}$ with the implication $a=7\Rightarrow [x]_2=\{42\}$, stating that if the value read by thread 2 for y (in a) is 7, then its observable view for x is $\{42\}$. Similarly, upon executing $b:=\operatorname{load} x$ we simply apply LP₁ to replace $[x]_2$ with the local register b in which the value of x is read. Lastly, the final postcondition Q is given by the conjunction of the thread-local postconditions $(P_3 \wedge Q_3)$.

Concurrent Reasoning and Stability In our description of the PIEROGI proof sketch in Fig. 2 thus far we focused on sequential (per-thread) reasoning, ignoring how concurrent threads may affect the validity of assertions at each program point. Specifically, as in existing concurrent logics [9, 18, 22, 23], we must ensure that the assertions at each program point are stable under concurrent operations. For instance, to ensure that P_1 remains stable under the concurrent operation $a := \mathbf{load} y$, we require that executing $a := \mathbf{load} y$ on states satisfying the conjunction of P_1 and the precondition of $a := \mathbf{load} y$ (i.e. Q_1) not invalidate P_1 , in that the resulting states continue to satisfy P_1 ; that is, $\{P_1 \wedge Q_1\}a := \mathbf{load} y\{P_1\}$ holds. Similarly, we must ensure that P_1 is stable under $b := \mathbf{load} x$, i.e. $\{P_1 \wedge Q_2\}b := \mathbf{load} x\{P_1\}$ holds. Analogously, we must establish the stability of P_2 , P_3 , P_4 , P_4 , P_4 , P_4 , and P_4 , and P_4 , and P_4 , i.e. P_4 , P_4 ,

Reasoning about flush Persistency To reason about the relaxed, buffered persistency of Px86_{view}, Cho et al. [7] introduce persistency views, determining the possible persisted values for each location; i.e. the values of those writes that may have persisted to memory. Note that the persistency view determines the possible values observable upon recovery from a crash. By contrast, the (perthread) coherence views determine the observable values during normal (noncrashing) executions, and have no bearing on the post-crash values.

Analogously, we extend PIEROGI with assertions of the form $[x]^P = S$, stating that the persistent view for x includes writes whose values are given by S. To see this, consider the PIEROGI proof sketch of Fig. 1b in Fig. 3 (left). Initially, y holds 0 in persistent memory: $[y]^P = \{0\}$. (Note that the precondition could additionally include $[x]_1 = [y]_1 = \{0\} \land [x]^P = \{0\}$ to denote that initially the thread may only observe 0 for x and y and that x holds 0 in persistent memory; however, this is not needed for the proof and we thus forgo it.)

As before, after executing **store** x 1, the observable value for x is updated, as denoted by $[x]_1 = \{1\}$. Moreover, after executing **flush** x, the persisted value for x, as denoted by $[x]^P = \{1\}$, by committing (persisting) the observable value for x ($[x]_1 = \{1\}$) to memory (see FP₁ in Fig. 7). Finally, after executing **store** y 1, the observable value for y is updated, as denoted by $[y]_1 = \{1\}$.

Crash Invariants Recall that $\xi \colon y=1 \Rightarrow x=1$ in Fig. 1b denotes a crash invariant in that it describes the persistent memory upon recover from a crash at any program point. This is because we have no control over when a crash may occur. To capture such invariants, in PIEROGI we write quadruples of the form $\{P\}$ C $\{Q\}$ $\{\{\xi : I\}\}$, where $\{P\}$ C $\{Q\}$ denotes a Hoare triple and I denotes the crash invariant. If C is a sequential program, I must follow from every assertion (including P and Q) in the proof. For instance, in the proof outline of Fig. 3 (left) all four assertions imply the invariant $[y]^P = \{1\} \Rightarrow [x]^P = \{1\}$. We discuss the meaning of crash invariants for concurrent programs below.

Reasoning about flush_{opt} **Persistency** Recall that unlike flush, flush_{opt} instructions (due to instruction reordering) may behave asynchronously and their effects may not take place immediately after execution. As such, unlike for flush x, after executing flush_{opt} x we cannot simply copy the observable view on x to the persistent view on x.

To capture the asynchronous nature of $\mathbf{flush}_{\mathrm{opt}}$, Cho et al. [7] introduce yet another set of views, namely the thread-local asynchronous view: the asynchronous view of thread τ on x describes the values (writes) that will be persisted at a later time (asynchronously) by τ upon executing a barrier instruction. That is, 1) when thread τ executes $\mathbf{flush}_{\mathrm{opt}} x$, its asynchronous view of x is advanced to at least its observable view of x; and 2) when τ executes a barrier (sfence, **mfence** or RMW), then its persistent view for each location is advanced to at least its corresponding asynchronous view. We model this in PIEROGI by 1) setting $[x]_{\tau}^{\mathbf{A}}$ to be a subset of $[x]_{\tau}$ when $\mathbf{flush}_{\mathrm{opt}} x$ is executed; and 2) setting $[x]_{\tau}^{\mathbf{P}}$ to be a subset of $[x]_{\tau}^{\mathbf{A}}$ (for each location x) when a barrier is executed.

This is illustrated in the proof sketch of Fig. 1d in Fig. 3 (right). In particular, unlike the proof sketch of Fig. 1b in Fig. 3 (left), after executing $\mathbf{flush}_{\mathrm{opt}} x$ we cannot simply copy the thread-observable view to the persistent view. Rather, we copy the thread-observable view $[x]_1$ to its asynchronous view and assert $[x]_1^{\mathsf{A}} = \{1\}$; and upon executing the subsequent **sfence**, we copy the thread-asynchronous view to the persistent view and assert $[x]_1^{\mathsf{P}} = \{1\}$.

Putting It All Together We next present a PIEROGI proof sketch of Fig. 1e in Fig. 4. The proof of the left thread is analogous to that in Fig. 3 (left); the proof of the right thread is straightforward and applies standard reasoning

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P: \left\{a = 0 \land \forall o \in \{x, y, z\}, \tau \in \{1, 2\}, [o]_{\tau} = [o]^{\mathsf{P}} = \{0\}\right\}
P_1: \left\{[y]_2 = \{0\} \land [z]^{\mathsf{P}} = \{0\} \land a = 0\}\right\}
\text{store } x \ 1; / / \mathsf{SP}_1
P_2: \left\{[y]_2 = \{0\} \land [z]^{\mathsf{P}} = \{0\} \land a = 0 \land [x]_1 = \{1\}\right\}
\text{flush } x; / / \mathsf{FP}_1, \mathsf{Cons}
P_3: \left\{[x]^{\mathsf{P}} = \{1\}\right\}
\text{store } y \ 1; / / \mathsf{SP}_1, \mathsf{Cons}
P_4: \left\{[x]^{\mathsf{P}} = \{1\}\right\}
Q: \left\{[x]^{\mathsf{P}} = \{1\}\right\}
I: \left\{\{\xi: [z]^{\mathsf{P}} = \{1\}\right\}\right\}
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Fig. 4: A Pierogi proof sketch of Fig. 1e

principles. The final postcondition Q is obtained by weakening the conjunction of per-thread postconditions.

Note that the crash invariant I follows from the assertions at each program point of thread 1 (i.e. $P_1 \vee P_2 \vee P_3 \vee P_4 \Rightarrow I$). That is, the crash invariant must follow from the assertions at all program points of some thread (e.g. thread 1 in Fig. 4). In the case of sequential programs (e.g. in Fig. 3), this amounts to all program points (of the only executing thread). Intuitively, we must ensure that the crash invariant holds at every program point regardless of how the underlying state changes. As the assertions are stable under concurrent operations, it is thus sufficient to ensure that there exists some thread whose assertions at each program point imply the crash invariant.

3 The Pierogi Proof rules and Reasoning Principles

We proceed with a description of our verification framework. As with prior work [9], the view-based semantics for persistent TSO [7] allows us to use the standard Owicki-Gries rules [2, 22] for compound statements. The main adjustment is the introduction of a new specialised assertion language capable of expressing properties about the different "views" described intuitively in §2. As such, since view updates are highly non-deterministic, the standard "assignment axiom" of Hoare Logic (and by extension Owicki-Gries) is no longer applicable. Moreover, unlike SC, reads in a weak memory setting have a side-effect: their interaction with the memory location being read causes the view of the executing thread to advance. Therefore, we resort to a set of proof rules that describe how views are modified and manipulated, as formalised by our view-based assertions.

3.1 The Pierogi Programming Language

We present the programming language in Fig. 5. Atomic statements (in AST) comprise **skip**, assignment, memory reads and writes, barrier instructions and explicit persists. Specifically, a := e evaluates expression e and returns it in

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\begin{array}{lll} v,u \in \operatorname{VAL} \triangleq \mathbb{N} & x,y,\ldots \in \operatorname{Loc} & a,b,\ldots \in \operatorname{Reg} & \tau \in \operatorname{Tid} \triangleq \mathbb{N} & i,j,k,\ldots \in \operatorname{Lab} \\ \hat{a},\hat{b},\ldots \in \operatorname{AuxVar} & \hat{e} \in \operatorname{AuxExp} ::= v \mid \hat{a} \mid \hat{e} + \hat{e} \mid \cdots \\ & e \in \operatorname{Exp} ::= v \mid a \mid e + e \mid \cdots & B \in \operatorname{BExp} ::= \operatorname{true} \mid B \wedge B \mid \cdots \\ & \alpha \in \operatorname{AST} ::= \operatorname{skip} \mid a := e \mid a := \operatorname{load} x \mid \operatorname{store} x \ e \\ & \mid a := \operatorname{CAS} x \ e \ e \mid \operatorname{sfence} \mid \operatorname{mfence} \mid \operatorname{flush} x \mid \operatorname{flush}_{\operatorname{opt}} x \\ & ls \in \operatorname{LST} ::= \alpha \ \operatorname{goto} \ j \mid \operatorname{if} \ B \ \operatorname{goto} \ j \ \operatorname{else} \ \operatorname{to} \ k \mid \langle \alpha \ \operatorname{goto} \ j, \hat{a} := \hat{e} \rangle \\ & \Pi \in \operatorname{Prog} \triangleq \operatorname{Tid} \times \operatorname{Lab} \to \operatorname{LST} & \overrightarrow{pc} \in \operatorname{PC} \triangleq \operatorname{Tid} \to \operatorname{Lab} \end{array}
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Fig. 5: The Pierogi domains and programming language

(thread-local) register a; $a := \mathbf{load} x$ reads from memory location x and returns it in register a; and **store** x e writes the contents of register a to location x. The $a := \mathbf{CAS} \ x \ e_1 \ e_2$ denotes 'compare-and-set' on location x, from the evaluated value of e_1 to the evaluated value of e_2 , and sets a to 1 if the CAS succeeds and to 0, otherwise. Finally, **mfence** denotes a memory fence, **sfence** denotes a store fence, and **flush** x and **flush** x denote explicit persist instructions (see §2).

Formally, we model a program Π as a function mapping each pair (τ, i) of thread identifier and label to the labelled statement (in LST) to be executed. A labelled statement may be 1) a plain statement of the form α **goto** j, comprising an atomic statement α to be executed and the label j of the next statement; 2) a conditional statement of the form **if** B **goto** j **else to** k to accommodate branching, which proceeds to label j if B holds and to k, otherwise; or 3) a statement with an auxiliary update $\langle \alpha \text{ goto } j, \hat{a} := \hat{e} \rangle$, which behaves as $\alpha \text{ goto } j$, but in addition (in the same atomic step) updates the value of the auxiliary variable \hat{a} with the auxiliary expression \hat{e} . It is well known that Owicki-Gries proofs require auxiliary variables to record the history of executions to differentiate states that would otherwise not be distinguishable [22]. We show how auxiliary variables are used in PIEROGI in the flush buffering example (§4).

We track the control flow within each thread via the program counter function, \vec{pc} , recording the program counter of each thread. We assume a designated label, $\iota \in \text{LAB}$, representing the initial label; i.e. each thread begins execution with $\vec{pc}(\tau) = \iota$. Similarly, $\zeta \in \text{LAB}$ represents the final label. Moreover, if $\vec{pc}(\tau) = i$ at the current execution step, then: 1) when $H(\tau, i) = \alpha$ goto j or $H(\tau, i) = \langle \alpha \text{ goto } j, a := \hat{e} \rangle$, then $\vec{pc}(\tau) = j$ at the next step; 2) when $H(\tau, i) = if B$ goto j else to k at the current step, then if B holds in the current state, then $\vec{pc}(\tau) = j$ at the next step.

Example 1. The program in Fig. 4, assuming that the left thread has id 1, is given as follows. The formalisation of the right thread is omitted, but is similar.

$$\varPi \triangleq \begin{cases} (1,\iota) \mapsto \mathbf{store} \ x \ 1 \ \mathbf{goto} \ 2, (1,2) \mapsto \mathbf{flush} \ x \ \mathbf{goto} \ 3, \\ (1,3) \mapsto \mathbf{store} \ y \ 1 \ \mathbf{goto} \ \zeta, \dots \end{cases}$$

3.2 View-Based Expressions

As with prior work on the RC11 model [15], we interpret PIEROGI expressions directly over a view-based state. We use expressions tailored for the view-based Px86_{view} model [7], which allow us to express relationships between different system components, including the persistent memory.

Our expressions fall into one of four categories: 1) current view expressions, which describe the current views of different system components (e.g. the persistent view); 2) conditional view expressions [9], which describe a view on a location after reading a particular value on a different location; 3) last view expressions, which hold if a component is viewing the last write to a location; and 4) write-count expressions, which describe the number of writes to a location.

Our current view expressions comprise $[x]_{\tau}$, $[x]^{\mathsf{P}}$ and $[x]_{\tau}^{\mathsf{A}}$, as described below; as shown in §2, each of these expressions describes a *set* of possible values.

- $[x]_{\tau}$ denotes the *coherence view* of thread τ : the set of values τ may read for x. $[x]^{\mathsf{P}}$ denotes the *persistent memory view*: the set of values that x may hold in (persistent) memory.
- $[x]_{\tau}^{\mathbf{A}}$ denotes the asynchronous memory view of thread τ : the set of values that can be persisted after a barrier instruction (sfence/mfence/RMW) is executed by τ (see rule OP in Fig. 7). Asynchronous views are updated after executing a flush_{opt}; however, unlike persistent memory views, the values in asynchronous views are not guaranteed to be persisted until a subsequent barrier is executed by the same thread.

Conditional view expressions are of the form $\langle x, v \rangle[y]_{\tau}$, as described below. As discussed in §2, conditional expressions capture the crux of message passing.

 $\langle x, v \rangle [y]_{\tau}$ returns a set of values that τ may read for y after it reads value v for x. In particular, if $\langle x, v \rangle [y]_{\tau} = S$ holds for some set S and τ executes $a := \mathbf{load} x$, then in the state immediately after the load, if a = v, then $[y]_{\tau} \subseteq S$ (see LP₂ in Fig. 7).

Last-view expressions (cf. [12]) are boolean-valued and hold if a particular component is synchronised (i.e. observes the latest value) on the given location. Such expressions provide determinism guarantees on **load** and **flush**. For instance if the view of τ is the last write on x, then a read from x by τ will load this last value. Last-view expressions comprise $[\![x]\!]_{\tau}^{\mathsf{F}}$:

- $[\![x]\!]_{\tau}$ holds iff τ is currently viewing the *last* write to x. Thus, for example, if $[\![x]\!]_{\tau}$ holds, then a **load** from x by τ reads the last write to x. Note that unlike architectural operational models [25], in the view model [7], writes are visible to all threads as soon as they occur.
- $[x]_{\tau}^{\mathsf{F}}$ holds iff a **flush** of x by τ is guaranteed to flush the *last* write to x to persistent memory.

Lastly, write-count expressions are of the form |x, v|, as described below. Such assertions are useful for inferring view expressions from known facts about the number of writes in the system with a particular value (see Fig. 11).

|x,v| returns the number of writes to x with value v. If |x,v| holds and τ writes to $y \neq x$, or writes a value $u \neq v$, then |x,v| continues to hold afterwards.

3.3 Owicki-Gries Reasoning

We present the PIEROGI proof system, as an extension of Hoare Logic with Owicki-Gries reasoning to account for concurrency. The main differences are that 1) our program annotations contain view-based assertions that allow reasoning about weak and persistent memory behaviours; and 2) we define a crash invariant to describe the recoverable state of the program after a crash. We proceed by first defining proof outlines, then providing syntactic rules for proving their validity. Our proof rules are *syntactic*, and thus can be understood and used without having to understand the details of the underlying Px86_{view} model.

We let ASSERTION_{PV} be the set of assertions (i.e. predicates over Px86_{view} states) that use view-based expressions (§3.2). A crash invariant, $I \in INV \subset ASSERTION_{PV}$, is defined over persistent views only, i.e. it only comprises the persistent view expressions of the form $[x]^P$. We model program annotations via an annotation function, $ann \in ANN = TID \times LAB \rightarrow ASSERTION_{PV}$, associating each program point (τ, i) with its associated assertion. A proof outline is a tuple (in, ann, I, fin), where $in, fin \in ASSERTION_{PV}$ are the initial and final assertions.

Example 2. The annotation of the proof in Fig. 4 is given by ann, with the mappings of thread 1 as shown below; the mappings of thread 2 are similar.

```
ann \triangleq \big\{ (1, \iota) \mapsto P_1, (1, 2) \mapsto P_2, (1, 3) \mapsto P_3, (1, \zeta) \mapsto P_4, \dots \big\} Additionally, we have in \triangleq a = 0 \land \forall o \in \{x, y, z\}, \tau \in \{1, 2\}. [o]_{\tau} = [o]^{\mathsf{P}} = \{0\}, fin \triangleq [x]^{\mathsf{P}} = \{1\} \text{ and } I \triangleq [z]^{\mathsf{P}} = \{1\} \Rightarrow [x]^{\mathsf{P}} = \{1\}.
```

Definition 1 (Valid proof outline). A proof outline (in, ann, I, fin) is valid for a program Π iff the following hold:

```
Initialisation. For all \tau \in \text{TID}, in \Rightarrow ann(\tau, \iota). Finalisation. (\bigwedge_{\tau \in \text{TID}} ann(\tau, \zeta)) \Rightarrow fin. Local correctness. For all \tau \in \text{TID} and i \in \text{LAB}, either:  -H(\tau,i) = \alpha \text{ goto } j \text{ and } \left\{ \frac{ann(\tau,i)}{\alpha} \right\} \alpha \left\{ \frac{ann(\tau,j)}{\alpha} \right\}; \text{ or } -H(\tau,i) = \text{ if } B \text{ goto } j \text{ else to } k \text{ and both } ann(\tau,i) \land B \Rightarrow ann(\tau,j) \text{ and } ann(\tau,i) \land \neg B \Rightarrow ann(\tau,k) \text{ hold; or } -H(\tau,i) = \langle \alpha \text{ goto } j, \hat{a} := \hat{e} \rangle \text{ and } \left\{ \frac{ann(\tau,i)}{\alpha} \right\} \alpha \left\{ \frac{ann(\tau,j)[\hat{e}/\hat{a}]}{\alpha} \right\}. Stability. For all \tau_1, \tau_2 \in \text{TID} such that \tau_1 \neq \tau_2 and i_1, i_2 \in \text{LAB}:  -\text{ if } H(\tau_1, i_1) = \alpha \text{ goto } j, \text{ then } \left\{ \frac{ann(\tau_2, i_2) \land ann(\tau_1, i_1)}{\alpha} \right\} \alpha \left\{ \frac{ann(\tau_2, i_2) \land ann(\tau_1, i_1)}{\alpha} \right\}. Persistence. There exists \tau \in \text{TID} such that for all i \in \text{LAB}, ann(\tau, i) \Rightarrow I.
```

Intuitively, Initialisation (resp. Finalisation) ensures that the initial (resp. final) assertion of each thread holds at the beginning (resp. end); Local correctness establishes annotation validity for each thread; Stability ensures that each (local) thread annotation is *interference-free* under the execution of other threads [22]; and Persistence ensures that the crash invariant holds at every program point for some thread.

$$\begin{array}{lll} P'\Rightarrow P & Q\Rightarrow Q' \\ \operatorname{Cons} & \begin{array}{c} \{P\} & \Pi & \{Q\} \\ \hline \{P'\} & \Pi & \{Q'\} \end{array} \end{array} & \operatorname{Conj} \frac{ \begin{array}{c} \{P_1\} & \Pi & \{Q_1\} \\ \{P_2\} & \Pi & \{Q_2\} \end{array}}{ \begin{array}{c} \{P_2\} & \Pi & \{Q_2\} \end{array}} & \operatorname{Disj} \frac{ \begin{array}{c} \{P_1\} & \Pi & \{Q_1\} \\ \{P_2\} & \Pi & \{Q_2\} \end{array}}{ \begin{array}{c} \{P_1\} & \Pi & \{Q_1\} \\ \hline \{P_2\} & \Pi & \{Q_2\} \end{array}} \\ \end{array}$$

Fig. 6: Standard decomposition rules of Pierogi

Example 3. Given the program in Example 1 and its annotation in Example 2, both Initialisation and Finalisation clearly hold. Moreover, Persistence holds for thread 1. For Local correctness of thread 1, we must prove (1)–(3) below; Local correctness of thread 2 is similar.

$$\{P_1\} \mathbf{store} \ x \ 1 \ \{P_2\} \tag{1}$$

$${P_2}$$
 flush x ${P_3}$ (2)

$$\{P_3\} \text{ store } y \mid P_4$$
 (3)

For Stability of P (the precondition of store x 1 in thread 1) against thread 2 we must prove:

$$\{P_1\}\ a := \mathbf{load}\ y\ \{P_1\} \tag{4}$$

$$\{P_1 \wedge a = 1\} \text{ store } z \ 1 \ \{P_1\}$$
 (5)

Stability of other assertions (i.e., P_2-P_4) is similar. We prove (1)–(5) in §3.4.

3.4 Pierogi Proof rules

One of the main benefits of PIEROGI is the ability to perform proofs at a high level of abstraction. In this section, we provide the set of proof rules that we use. The annotation within a proof outline is, in essence, an invariant mapping each program location to an assertion that holds at the program location. Thus, we prove local correctness by checking that each atomic step of a thread establishes the assertions in that thread. Similarly, we check stability by checking each assertion in one thread against each atomic step of the other threads. To enable proof abstraction, we introduce a set of proof rules that describe the interaction between the assertions from §3.2 and the atomic program steps. We will use the standard decomposition rules from Hoare Logic to reduce proof outlines and enable our rules over atomic steps to be applied.

Standard Decomposition Rules The standard decomposition rules we use are given in Fig. 6, which allow one to weaken preconditions and strengthen postconditions, and decompose conjunctions and disjunctions.

Rules for Atomic Statements and View-Based Assertions Weak and persistent memory models (e.g. Px86) are inherently non-deterministic. Moreover in contrast to sequential consistent, in view-based operational semantics (such as $Px86_{view}$) instructions such as a := load e have may a side-effect since they may update the view of the thread performing the load (cf. [9]). Therefore, unlike Hoare Logic, which contains a single rule for assignment, we have a

Precondition	Const.	Ref.		
$\{[x]_{ au}=S\}$	}	$\{a \in S \land [x]_{\tau} \subseteq S\}$		LP_1
$\left\{u\in[x]_{ au}\Rightarrow\langle x,u angle[y]_{ au}=S ight\}$		$\{a=u\Rightarrow [y]_{ au}\subseteq S\}$		LP_2
$\{ x,u = 1 \land \ x\ _{\tau'} \land [x]_{\tau'} = \{u\}\}$	}	$\left\{a = u \Rightarrow [x]_{\tau} = \left\{u\right\}\right\}$		LP_3
$\{true\}$	}	$\{[x]_{\tau} = \{v\}\}$		SP_1
$\left\{ [x]_{\tau'} = S \right\}$	}	$\left\{ [x]_{\tau'} = S \cup \{v\} \right\}$	$\tau \neq \tau'$	SP_2
$\left\{[x]_{ au'}^{A} = S\right\}$	}	$\left\{ [x]_{\tau'}^{A} = S \cup \{v\} \right\}$		SP_3
$\{[x]^{P} = S\}$	store $x v$	$\{[x]^{P} = S \cup \{v\}\}$		SP_4
$\{[y]_{\tau} = S \land v \notin [x]_{\tau'}\}$	}	$\{\langle x, v \rangle [y]_{\tau'} \subseteq S\}$	$\tau \neq \tau'$	SP_5
$\{true\}$	}	$\left\{ \ x\ _{\tau} \wedge \ x\ _{\tau}^{F} \right\}$		SP_6
$\{ x,v =n\}$	}	$\{ x,v =n+1\}$		SP_7
$\left\{ [x]_{ au}=S ight\}$	}	$\{[x]^{P} \subseteq S \land [x]^{A}_{\tau} \subseteq S\}$		FP_1
$\left\{ \left[x\right]^{P}=S\right\}$	flush x	$\{[x]^{P} \subseteq S\}$		FP_2
$\left\{ \llbracket x \rrbracket_{\tau'} \wedge [x]_{\tau'} = \{u\} \wedge \llbracket x \rrbracket_{\tau}^{F} \right\}$	}	$\{[x]^{P} = \{u\}\}$		FP_3
$\left\{ [x]_{\tau} = S \vee [x]_{\tau}^{A} = S \right\}$	$\mathbf{flush}_{\mathrm{opt}} x$	$\{[x]_{\tau}^{A} \subseteq S\}$		OP
$\left\{ [x]_{\tau}^{A} = S \vee [x]^{P} = S \right\}$	sfence	$\{[x]^{P} \subseteq S\}$		SFP

Fig. 7: Selected proof rules for atomic statements executed by thread τ

set of rules for atomic statements, describing their interaction with view-based assertions. Each of the rules in this section has been proved sound with respect to the view-based semantics in Isabelle/HOL.

A selection of these rules for the atomic statements is given in Fig. 7, where the statement is assumed to be executed by thread τ . The first column contains the pre/post condition triple, the second any additional constraints and the third, labels that we use to refer to the rules in our descriptions below. Unless explicitly mentioned as a constraint, we do not assume that threads, locations and values are distinct; e.g. rule LP₃ (referring to τ and τ') holds regardless of whether $\tau = \tau'$ or not.

The rules in Fig. 7 provide high-level insights into the low-level semantics of $\operatorname{Px86_{view}}$ without having to understand the operational details. The $\operatorname{LP_i}$ rules are for statement $a:=\operatorname{load} x$. Rule $\operatorname{LP_1}$ states that if τ 's view of x is the set of values S, then in the post state a is an element of S and moreover τ 's view of x is a subset of S (since τ 's view may have shifted). By $\operatorname{LP_2}$, provided the conditional view of τ on y (with condition x=u) is S, if the load returns value u, then the view of τ is shifted so that $[y]_{\tau} \subseteq S$. We only have $[y]_{\tau} \subseteq S$ in the postcondition because there may be multiple writes to x with value u; reading x read may shift the view to the latter write, thus x reducing the set of values that τ can read for y. $\operatorname{LP_3}$ describes conditions for a deterministic load by thread τ . The precondition assumes that there is only one write to x with value u, that x some thread x sees the last write to x with value x. Then, if x reads x its view of x is also constrained to just the set containing x.

The store rules, SP_i , reflect that fact that a new write modifies the views of the other threads as well as the persistent memory and asynchronous views. The first four rules describe the interaction of a **store** by thread τ with current view assertions. By SP_1 , the **store** ensures that the current view of τ is solely the

Statement	Stable Assert.	Const.	Ref.	Statement	Stable Assert.	Const.	Ref.
	$\{[y]_{\tau'} = S\}$	$\tau \neq \tau'$	LS_1	,	$\{[y]_{\tau'} = S\}$	$x \neq y$	WS_1
	$\{[y]^{P} = S\}$		LS_2		$\{[y]^{P} = S\}$	$x \neq y$	WS_2
$a := \mathbf{load} x$	$\{[y]_{\tau'}^{A} = S\}$		LS_3		$\{[y]_{\tau'}^{A} = S\}$	$x \neq y$	WS_3
	$\{a=k\}$		LS_4	store $x \ v$	$\{a=k\}$		WS_4
	$\{ \llbracket y Vert_{ au'} \}$		LS_5		$\{ \llbracket y Vert_{ au'} \}$	$x \neq y$	WS_5
	$\{[y]_{\tau'} = S\}$		FS_1		$\left\{ \ y\ _{\tau'}^{F} \right\}$	$x \neq y$	WS_6
flush x	$\{[y]^{P} = S\}$	$x \neq y$	FS_2		$\{ y,v' =n\}$	$x \neq y \vee$	WS_7
	$\{ \llbracket y rbracket_{ au'} \}$		FS_3			$v \neq v'$	
	$\left\{ \llbracket y \rrbracket_{\tau'}^{F} \right\}$		FS_4		$\{[y]_{\tau'} = S\}$		OS_1
	$\{ y,v =n\}$		FS_5	$\mathbf{flush}_{\mathrm{opt}} x$	$\{[y]^{P} = S\}$		OS_2
sfence	$\{[x]_{\tau'} = S\}$		SFS_1		$\{ y,v =n\}$		OS_3
sience	$\{ x,v =n\}$		SFS_2			-	•

Fig. 8: Selection of stable assertions for atomic statements executed by thread τ

value v written by τ . This is because in $Px86_{view}$, new writes are introduced by the executing thread, τ , with a maximal timestamp (see STORE rule in Fig. 12), and τ 's view is updated to this new write. SP_2 , SP_3 and SP_4 are similar, and assuming that the view (of another thread, persistent memory and asynchronous view, respectively) in the pre-state is S, shows that the view in the post state is $S \cup \{v\}$. Rule SP_5 allows one to *introduce* a conditional observation assertion $\langle x, v \rangle [y]_{\tau'}$ where $\tau' \neq \tau$. The pre-state of SP_5 assumes that τ 's view of y is the set S, and that τ' cannot view value v for y. Rule SP_6 introduces last-view assertions for τ after τ performs a write to x, and finally SP_7 states that the number of writes to x with value v increases by 1 after executing **store** x v.

Rules $\mathsf{FP_i}$ describe the effect of $\mathsf{flush}\ x$ on the state. $\mathsf{FP_1}$ states that, provided that the current view of τ for x is the set of values S, after executing $\mathsf{flush}\ x$, we are guaranteed that both the persistent view and asynchronous view of τ for x are subsets of S. We obtain a subset in the post state since the $\mathsf{Px86}_{\mathsf{view}}$ semantics potentially moves the persistent and asynchronous views forward. Similarly, by $\mathsf{FP_2}$ if the current persistent view of x is S, then after executing $\mathsf{flush}\ x$ the persistent view will be a subset of S. Finally, $\mathsf{FP_2}$ provides a mechanism for establishing a deterministic persistent view u for x. The precondition assumes that some thread's view of x is the last write with value u and that τ 's view is such that the flush is guaranted to flush to this last write to x.

Rule OP describes how the asynchronous view of τ in the postcondition of $\mathbf{flush}_{\mathrm{opt}}$ x is related to the current view of τ and the asynchronous view in the precondition. Finally, rule SFP describes the relationship between the persistent view in the postcondition and the asynchronous view and persistent view in the precondition for an **sfence** instruction.

Our Isabelle/HOL development contains further rules for the other instructions, including **mfence** and **cas**, which we omit here for space reasons. In addition, we prove the stability of several assertions (see Fig. 8 for a selection). An assertion P is stable over a statement α executed by τ iff $\{P\}$ α $\{P\}$ holds.

Well-formedness The final major aspect of our framework is a well-formedness condition that describes the set of reacable states in the $Px86_{view}$ semantics. The condition is expressed as an invariant of the semantics: it holds initially, and is stable under every possible transition of $Px86_{view}$. In fact, the rules in Figs. 7 and 8 are proved with respect to this well-formedness condition.

The majority of the well-formedness constraints are straightforward, e.g. describing the relationship between the views of different components. The most important component of the well-formedness condition is a non-emptiness condition on views, which states that $[x]_{\tau} \neq \emptyset \wedge [x]^{\mathsf{P}} \neq \emptyset \wedge [x]^{\mathsf{A}}_{\tau} \neq \emptyset$. For instance, a consequence of this condition is that, in combination with LP_1 , we have:

$$\{[y]_{\tau} = \{v\}\}\ a := \text{load}\ x\ \{[y]_{\tau} = \{v\}\}\$$
 (6)

Worked Example We now return to the proof obligations from Example 3 and demonstrate how they can be discharged using the proof rules described above. For Local correctness, condition (1) holds by Conj (from Fig. 6) together with stability rules WS₁, WS₂ and WS₄ (from Fig. 8) which establish the first three conjunctions in the postcondition, and SP₁ from Fig. 7, which establishes the final conjunction. Condition (2) holds by FP₁ in Fig. 7 together with Cons (from Fig. 6). Finally, condition (3) holds by WS₂ (from Fig. 8).

Both the Stability conditions (4) and (5) from Example 3 hold by the stability rules in Fig. 8 together with Cons and Conj (from Fig. 6). In particular, for (4), we use rules LS_1 , LS_2 and LS_4 , and for (5), we use WS_1 , WS_2 and WS_4 .

4 Examples

In this section we present a selection of programs that we have verified in Isabelle/HOL. These examples highlight specific aspects of Px86, in particular, the interaction between **flush**_{opt} and **sfence**, as well as aspects of our view-based assertion language that simplifies verification.

Optimised Message Passing We start by considering a variant of Fig. 1e, which contains two optimisations. First, we notice that flushing of the write to x in thread 1 can be moved to thread 2 since the write to z is guarded by whether or not thread 2 reads the flag y. Second, it is possible to replace the flush by a more optimised flush_{opt} followed by an **sfence**. We confirm correctness of these optimisations via the proof outline in Fig. 9. The optimised message passing in Fig. 9 ensures the same persistent invariant as Fig. 1e. However, the way in which this is established differs. In particular, in Fig. 1e, the persistent invariant holds due to thread 1, whereas in Fig. 9 it holds due to thread 2.

With respect to the persistent invariant, the most important sequence of steps takes place in thread 2 if it reads 1 for y. Note that by the conditional view assertion in the precondition of a := load y, thread 2 is guaranteed to read 2 for x after reading 1 for y. Thus, if the test of **if** statement succeeds, then thread 2 must see 1 for x. This view is translated into an asynchronous view after the **flush**_{opt} is executed, and then to the persistent view after executing

Fig. 9: Proof outline for optimised message passing

sfence. Note that until this occurs, we can guarantee that $[z]^P = \{0\}$, which trivially guarantees the persistent invariant.

Flush Buffering Our next example is a variation of store buffering (SB) and is used to highlight how writes by different threads on different locations interact with flushes. Here, thread 1 writes to x and flushes y, while thread 2 writes to ythen flushes x. The writes to w and z are used to witness whether the flushes in both threads have occurred. The persistent invariant states that, if both w and z hold 1 in persistent memory, then either x or y has the new value (i.e. 1) in persistent memory. If both threads perform their flush operations, then at least one must flush value 1 since a **flush** cannot be reordered with a **store**.

Although simple to state, the proof is non-trivial since it requires careful analysis of the order in which the stores to x and y occur. In the semantics of Cho et al. [7], the flush corresponding to the second store instruction executed synchronises with writes to all locations. Thus, for example, if thread 1's store to x is executed after thread 2's store to y, then the subsequent flush in thread 1 is guaranteed to flush the new write to u.

The above intuition requires reasoning about the order in which operations occur. To facilitate this, we use auxiliary variables \hat{a} and b to record the order in which the writes to x and y occur; $\hat{a} = 1$ iff the write to x occurs before the write to y, and $\hat{a} = 2$ iff the write to x occurs after the write to y. W.l.o.g., let us now consider the precondition of flush y (the reasoning for flush x is symmetric). There are two disjuncts to consider.

- The first disjunct describes the case in which thread 1 executes its store before thread 2. From here, there is a danger that the thread 1 can terminate having flushed 0 for y. However, from this state, thread 2 is guaranteed to flush 1 for x before setting z to 1, satisfying the persistent invariant, as described by the second disjunct of each assertion in thread 2.

⁶ Note that the **flush** operations here are analogous to the **load** instructions in SB.

Fig. 10: Proof outline for flush buffering

The second disjunct describes the case in which thread 1 executes its store after thread 2. In this case, thread 1 is guaranteed to flush 1 for y, and this fact is captured by the conjunct $[y]_2 \wedge [y]_2 = \{1\} \wedge [y]_1^F$, which ensures that 1) thread 2 sees the last write to y; 2) the only value visible for y to thread 2 is 1; and 3) a flush performed by thread 1 is guaranteed to flush the last write to y. Note that by 1) and 2), we are guaranteed that the last write to y has value 1. We use these three facts to deduce that $[y]^P = \{1\}$ in the second disjunct of the postcondition of **flush** y using rule P_3 .

Epoch Persistency In our next example, we demonstrate how writes of different threads on the same location interact with an optimised flush in the same location, as well as how the ordering of optimised flushes/loads alters the persistency behaviour. The crash invariant of Fig. 11 states that if z and y hold the value 1 in persistent memory then x has the value 2 in persistent memory.

In order for thread 2 to read value 2 for x, the **store** of 2 at x must be performed before the **store** of 1 and $[x]_2 = \{1,2\}$. Unlike the previous example, establishing the persistent invariant for thread 2, requires reasoning about the view of thread 2 for address x (i.e. $[x]_2$) after the execution of the instruction $a := \mathbf{load} x$. Notice here that $a := \mathbf{load} x$ is ordered with respect to the later $\mathbf{flush}_{\mathrm{opt}} x$ instruction. Consequently, any impact of the execution of the \mathbf{load} on $[x]_2$, will also affect $[x]_2^{\mathsf{A}}$. Taking into account the ordering of the writes at the address x, we can conclude that if thread 2 reads the value 2, it reads the value of the last write at x. This is expressed with the assertion $[x]_1$ in the precondition of $a := \mathbf{load} x$, which states that the threads 1's view of x is the last write to x. By rule LP_3 , if a thread τ 's view of an address x contains only the last write

Fig. 11: Proof outline for epoch persistency

at this address, and the last value written at this address appears only once at the memory, then if a thread τ read this value at x, its view of x (i.e. $[x]_{\tau}$) is guaranteed to contain only the last written value at x. Consequently, after reading value 2, thread 2's view of x contains only the value 2 (i.e. $[x]_2 = \{2\}$). Execution of $\mathbf{flush}_{opt} x$ ensures $[x]_2^{\mathsf{A}}$ (by rule OP). As a result, in the case that the if statement succeeds, after the execution of the sfence it is guaranteed that the value 2 is persisted at x (i.e. $[x]^P = \{2\}$). In the case that the **if** statement fails, $[y]^P = \{0\}$ must hold, thus the persistent invariant holds trivially.

Pierogi Soundness 5

In this section we present the Px86_{view} model from [7] (§5.1), formally interpret our assertions as predicates on states of that model ($\S5.2$), and establish the soundness of the proposed reasoning technique (§5.3).

The Px86_{view} Model 5.1

Like previous view-based models, Px86_{view} employs a non-standard memory capturing all previously executed writes, alongside with so-called "thread views" that track several position(s) of each thread in that history and enforce limitations on the ability of the thread to read from and write to the memory. In addition, the thread views contain the necessary information for determining the possible contents of the non-volatile memory upon a system crash. Formally, Px86_{view}'s memory and thread states are defined as follows.

$$\begin{array}{c} \alpha = a := e \\ v = T.\operatorname{regs}(e) \\ V = T.\operatorname{regs}(e) \\ T' = T[\operatorname{regs}(a) \mapsto v] \\ \hline (T,M) \xrightarrow{\alpha} \langle T',M \rangle \\ \hline (LOAD-EXTERNAL) \\ \alpha = a := \mathbf{load} x \\ M[t] = \langle x := v \rangle \\ T.\operatorname{coh}(x) \neq t \\ T.\operatorname{coh}(x) \neq t \\ \hline (T,M) \xrightarrow{\alpha} \langle T',M \rangle \\ \hline (DAD-EXTERNAL) \\ \alpha = a := \mathbf{load} x \\ M[t] = \langle x := v \rangle \\ T.\operatorname{coh}(x) \neq t \\ T.\operatorname{coh}(x) \neq t \\ \hline (T,M) \xrightarrow{\alpha} \langle T',M \rangle \\ \hline (T,M) \xrightarrow{\alpha} \langle T',$$

(STORE)

 $\alpha = \mathbf{store} \ x \ e$

(ASSIGN)

(LOAD-INTERNAL)

 $\alpha = a := \mathbf{load} \, x$

Fig. 12: Transitions of $Px86_{view}$ for a program Π

Definition 2 (Px86_{view}'s memory). A memory $M \in \text{MEMORY}$ is a list of messages, where each message has the form $\langle x := v \rangle$ for some $x \in \text{Loc}$ and $v \in \text{VAL}$. We use w.loc and w.val to refer to the two components of a message w. We use standard list notations for memories (e.g. $M_1 + M_2$ for appending memories, [w] for a singleton memory, and |M| for the length of M). We refer to indices (starting from 0) in a memory M as timestamps, and denote the t'th element of M as M[t]. We use \sqcup for obtaining the maximum among timestamps (i.e. $t_1 \sqcup t_2 = \max(t_1, t_2)$), and extend this notation pointwise to functions. We write $x \notin M(t_2..t_1]$ for the condition $\forall t_2 < t \le t_1. M[t]. \text{loc} \ne x$.

Definition 3 (Px86_{view}'s thread states). A thread state $T \in \text{THREAD}$ is a record consisting of the following fields: $\text{coh} : \text{Loc} \to \mathbb{N}, \, \text{v}_{\text{rNew}} : \mathbb{N}, \, \text{v}_{\text{pReady}} : \mathbb{N},$

 $\mathsf{v}_{\mathsf{pAsync}} : \mathsf{Loc} \to \mathbb{N}$, and $\mathsf{v}_{\mathsf{pCommit}} : \mathsf{Loc} \to \mathbb{N}$. We use standard function/record update notation (e.g. $T' = T[\mathsf{coh}(x) \mapsto t]$ denotes the thread state obtained from T be modifying the x entry in the coh component of T to t). In addition, \mapsto_{\sqcup} is used to incorporate certain timestamps in fields (e.g. $T[\mathsf{v}_{\mathsf{rNew}} \mapsto_{\sqcup} t]$ denotes the thread state obtained from T be modifying the $\mathsf{v}_{\mathsf{rNew}}$ component of T to $T.\mathsf{v}_{\mathsf{rNew}} \sqcup t$). We denote by $T.\mathsf{maxcoh}$ the maximum among the coherence view timestamps $(T.\mathsf{maxcoh} = \bigsqcup_{T} T.\mathsf{coh}(x))$.

The two components, together with program counters and the "ghost memory", are combined in $Px86_{view}$'s machine states as defined next.

Definition 4 (Px86_{view}'s machine states). A machine state is a tuple $\sigma = \langle \vec{pc}, \vec{T}, M, G \rangle$ where \vec{pc} : TID \rightarrow LAB is a mapping assigning the next program label to be executed by each thread, \vec{T} : TID \rightarrow THREAD is a mapping assigning the current thread state to each thread, $M \in$ MEMORY is the current memory, and $G: \text{AuxVar} \rightarrow \text{Val}$ is storing the current values of the auxiliary variables. Below we assume that G is extended to expressions $\hat{e} \in \text{AuxExp}$ in a standard way. We denote the components of a machine state σ by $\sigma.\vec{pc}, \sigma.\vec{T}, \sigma.M$, and $\sigma.G$. In addition, we denote by $\sigma.\text{maxpCommit}(x)$ the maximum among the persistency view timestamps for location x ($\sigma.\text{maxpCommit} = \bigcup_{\tau} \sigma.\vec{T}(\tau).\text{v}_{\text{pCommit}}(x)$).

The transitions of Px86_{view} are presented in Fig. 12. These closely follow the model in [7] with minor presentational simplifications. Note, however, that, for simplicity and following [17], we conservatively assume that writes persist atomically at the location granularity (representing, e.g. machine words) rather than at the granularity of the width of a cache line. We refer the interested reader to [7] for a detailed discussion of the transitions rules in Fig. 12.

The above operational definitions naturally induce a notion of a execution (or a "run") of $Px86_{view}$ on a certain program Π starting from some initial state of the form $\langle \lambda \tau, \iota, \vec{T}, M, G \rangle$. A system crash might occur at any point during the execution. Again, following the model of [7], the non-volatile memory (NVM) is not modeled as a concrete part of the state. Instead, the possible contents of the NVM can be inferred from the machine state (specifically from the memory and the $v_{pCommit}$ views of the different threads), as defined next. This definition is presented as "crash transition" in [7].

Definition 5. A non-volatile memory $NVM: Loc \to Val$ is possible in a state σ if for every $x \in Loc$, there exists some t such that $\sigma.M[t] = \langle x := NVM(x) \rangle$ and $x \notin \sigma.M(t..\sigma.maxpCommit(x)]$.

5.2 The Semantics of Pierogi Assertions

We present the formal definitions of the expressions introduced in $\S 3.2$ in terms of $Px86_{view}$'s machine states.

Current and conditional views When formalising the current and conditional view expressions, we start with auxiliary functions that return the sets of

observable timestamps visible to the components in question, then extract the values in memory corresponding these timestamps. To facilitate this, we define

$$\mathsf{Vals}(M, TS) \triangleq \{M[t].\mathsf{loc} \mid t \in TS\}$$

where $M \in MEMORY$ and TS is a set of timestamps.

Thread view To define the meaning of the thread view expression, $[x]_{\tau}$, we use:

$$\mathsf{TS}^{\mathsf{OF}}_{\tau}(\sigma, x, t) \triangleq \{t' \mid \sigma.M[t'].\mathsf{loc} = x \land \sigma.\vec{T}(\tau).\mathsf{coh}(x) \leq t' \land x \not\in \sigma.M(t'..t]\}$$

$$\mathsf{TS}_{\tau}(\sigma, x) \triangleq \mathsf{TS}^{\mathsf{OF}}_{\tau}(\sigma, x, \sigma.\vec{T}(\tau).\mathsf{v}_{\mathsf{New}})$$

 $\mathsf{TS}^{\mathsf{OF}}_{\tau}(\sigma,x,t)$ returns the set of timestamps that are observable from timestamp t for thread τ to read for location x in state σ ; and $\mathsf{TS}_{\tau}(\sigma,x)$ returns the set of timestamps that are observable for τ to read x in σ . Note that after instantiating t to $\sigma.\vec{T}(\tau).\mathsf{v}_{\mathsf{rNew}}$ in $\mathsf{TS}^{\mathsf{OF}}_{\tau}(\sigma,x,t)$, we obtain the premises of the load rules in Fig. 12. Then, $[x]_{\tau} \triangleq \lambda \sigma. \mathsf{Vals}(\sigma.M, \mathsf{TS}_{\tau}(\sigma,x))$, i.e. is the set of values in $\sigma.M$ corresponding to the timestamps in $\mathsf{TS}_{\tau}(\sigma,x)$.

Persistent memory view For the persistent memory view expression, $[x]^P$, we use:

$$\mathsf{TS^{P}}(\sigma, x) = \{t \mid \sigma.M[t].\mathsf{loc} = x \land x \not\in \sigma.M(t..\sigma.\mathsf{maxpCommit}(x))\}$$

which returns the set of timestamps that are observable to the persistent memory for x in σ . Then, $[x]^{\mathsf{P}} \triangleq \lambda \sigma$. $\mathsf{Vals}(\sigma.M, \mathsf{TS}^{\mathsf{P}}(\sigma, x))$. Note that the second conjunct within the definition of $\mathsf{TS}^{\mathsf{P}}(\sigma, x)$ is precisely the condition that links $\mathsf{Px86}_{\mathsf{view}}$ states to NVM states (Definition 5). Given this definition, we have:

Proposition 1. A non-volatile memory $NVM : Loc \rightarrow Val$ is possible in a state σ iff $NVM(x) \in [x]^{P}(\sigma)$ for every $x \in Loc$.

Asynchronous memory view To define the meaning of the asynchronous memory view, $[x]_{\tau}^{\mathsf{A}}$, we use:

$$\mathsf{TS}^\mathsf{A}_\tau(\sigma,x) \triangleq \{t \mid \sigma.M[t].\mathsf{loc} = x \land x \not\in \sigma.M(t..\sigma.\vec{T}(\tau).\mathsf{v}_{\mathsf{pAsync}}(x)]\}$$

which returns the timestamps of the asynchronous view of thread τ in location x and state σ . Then, as before, $[x]_{\tau}^{\mathsf{A}} \triangleq \lambda \sigma$. $\mathsf{Vals}(\sigma.M, \mathsf{TS}_{\tau}^{\mathsf{A}}(\sigma, x))$.

Conditional view The functions used to define conditional memory view, $\langle x, v \rangle [y]_{\tau}$, are slightly more sophisticated than those above. We define:

$$\begin{split} \mathsf{TS}^{\mathsf{OV}}_{\tau}(\sigma, x, v) &\triangleq \left\{ \begin{matrix} t' \\ \\ \end{matrix} \middle| \begin{array}{l} \exists t \in \mathsf{TS}_{\tau}(\sigma, x). \ \sigma.M[t].\mathsf{val} = v \land \\ t' &= \mathbf{if} \ t = \sigma.\vec{T}(\tau).\mathsf{coh}(x) \ \mathbf{then} \ \sigma.\vec{T}(\tau).\mathsf{v}_{\mathsf{rNew}} \\ \end{aligned} \right\} \\ \mathsf{TS}^{\mathsf{CO}}_{\tau}(\sigma, x, v, y) &\triangleq \bigcup \{ \mathsf{TS}^{\mathsf{OF}}_{\tau}(\sigma, y, t) \mid t \in \mathsf{TS}^{\mathsf{OV}}_{\tau}(\sigma, x, v) \} \end{split}$$

where $\mathsf{TS}^{\mathsf{OV}}_{\tau}(\sigma, x, v)$ returns the set of timestamps that τ can observe for x with value v. Assuming t is a timestamp that τ can observe for x, and the value for x at t is v, the corresponding timestamp t' that $\mathsf{TS}^{\mathsf{OV}}_{\tau}(\sigma, x, v)$ returns is $\sigma.\vec{T}(\tau).\mathsf{v}_{\mathsf{rNew}}$ if τ 's coherence view for x is t, and the maximum of t and $\sigma.\vec{T}(\tau).\mathsf{v}_{\mathsf{rNew}}$, otherwise.

Given this, $\mathsf{TS}^\mathsf{CO}_\tau(\sigma, x, v, y)$ returns the timestamps that τ can observe for y, from any timestamp $t \in \mathsf{TS}^\mathsf{OV}_\tau(\sigma, x, v)$. Finally, the set of conditional values is defined by $\langle x, v \rangle[y]_\tau \triangleq \lambda \sigma$. $\mathsf{Vals}(\sigma.M, \mathsf{TS}^\mathsf{CO}_\tau(\sigma, x, v, y))$.

Last view assertions We use the following auxiliary definition:

$$\mathsf{Last}(M, x) \triangleq \bigsqcup \{t \mid M[t]. \mathsf{loc} = x\}$$

which returns the timestamp of the last write to x in M. Then, the last view assertions are given by:

- $\|x\|_{\tau} \triangleq \{\sigma \mid \mathsf{TS}_{\tau}(\sigma, x) = \{\mathsf{Last}(\sigma.M, x)\}\}, \text{ i.e. } \tau\text{'s view of } x \text{ in } \sigma \text{ is the last write to } x \text{ in } \sigma.$
- $\|x\|_{\tau}^{\mathsf{F}} \triangleq \{\sigma \mid \mathsf{Last}(\sigma.M, x) \leq \sigma.\vec{T}(\tau).\mathsf{maxcoh} \sqcup \sigma.\mathsf{maxpCommit}(x)\}, \text{ i.e. the maximum of } \tau\text{'s maximum coherence view and the maximum commit view of } x \text{ (over all threads) is beyond the last write to } x \text{ in } \sigma. \text{ This means that executing a flush } x \text{ operation in } \tau \text{ will cause the last write of } x \text{ to be flushed (see Flush rule in Fig. 12).}$

Value count Finally, the value count expression is defined as follows:

$$|x, v| \triangleq \lambda \sigma. |\{t \mid \sigma. M[t] = \langle x := v \rangle\}|$$

5.3 Soundness of Pierogi

Given the above building blocks, the soundness of the proposed reasoning technique is stated as follows.

Theorem 1 (Soundness of Pierogi). Suppose that a program Π has a valid proof outline $\langle in, ann, I, fin \rangle$. Let σ be a state of $Px86_{view}$ that is reachable in an execution of Π from some state σ_{init} of the form $\langle \lambda \tau. \iota, \vec{T}_{init}, M_{init}, G_{init} \rangle$ such that $\sigma_{init} \in in$. Then, the following hold:

- 1) For every $\tau \in \text{Tid}$, we have that $\sigma \in ann(\tau, \sigma.\vec{pc}(\tau))$.
- 2) If $\sigma.\vec{pc}(\tau) = \zeta$ for every $\tau \in \text{Tid}$, then $\sigma \in \text{fin}$.
- 3) Every non-volatile memory NVM that is possible in σ satisfies the crash invariant I.

Finally, it is straightforward to show the soundness of a standard "auxiliary variable transformation" [22] which removes all auxiliary variables from a program Π (translating each command $\langle \alpha \ \mathbf{goto} \ j, \hat{a} := \hat{e} \rangle$ into $\alpha \ \mathbf{goto} \ j$) provided that the crash invariant and the final assertion do not contain occurrences of the auxiliary variables. Indeed, it is easy to see that the auxiliary memory G in the operational semantics in Fig. 12 serves only as an instrumentation, and does not restrict the possible runs. (Formally, if Π' is obtained from Π by removing all auxiliary variables and $\langle \vec{pc}, \vec{T}, M, G' \rangle$ is reachable in $\Rightarrow_{\Pi'}$ from some initial state, then $\langle \vec{pc}, \vec{T}, M, G \rangle$ is reachable in \Rightarrow_{Π} from the same state for some G.)

6 Mechanisation

Perhaps the greatest strength of our development is an integrated Isabelle/HOL mechanisation providing a fully fledged semi-automated verification tool for $Px86_{view}$ programs. This mechanisation builds on the existing work on Owicki–Gries for RC11 by Dalvandi et al [9,10] applying it to the $Px86_{view}$ semantics. We start by encoding the operational semantics of Cho et al. [7], followed by the view-based assertions described in §3.2. Then, we prove correctness of all of the proof rules for the atomic statements, including those described in §3.4. These rules can be challenging to prove since they require unfolding of the assertions and examination of the low-level operational semantics and their effect on the views of different system components.

Once proved, the rules provided are highly reusable, and are key to making verification feasible. In particular, when showing validity of a proof outline (Definition 1), Isabelle/HOL is able to generate the necessary proof obligations (after some minor interactions), then *automatically* able to find the set of high-level proof rules needed to discharge each proof obligation via the built-in sledgehammer tool [4]. This facility enables a high degree of experimentation and debugging of proof outlines, including the ability to reduce the complexity of assertions once a proof outline has been validated.

The base development (semantics, view-based assertions, and soundness of proof rules) comprise ~ 7000 lines of Isabelle/HOL code. With this base development in place, each example comprises 200–400 lines of code (including the encoding of the program, the annotations, and the proofs of validity). The entire development took approximately 3 months of full-time work.

7 Related Work

The soundness of Pierogi is proven relative to the Px86_{view} of Cho et al. [7]; there are however other equivalent models in the literature [1, 17, 24]. While the original persistent x86 semantics has explicit asynchronous persist instructions [24], the underlying model assumed in this work is the one due to Cho et al. [7], whose persist instructions are synchronous. Nevertheless, Khyzha and Lahav [17] formally proved that the two alternatives are equivalent when reasoning about states after crashes (e.g. using our "crash invariants").

As mentioned in §1, the only existing program logic for persistent programs is POG [23], which (as with PIEROGI) is a descendent of Owicki-Gries [22]. PIEROGI goes beyond POG by handling examples that involve \mathbf{flush}_{opt} instructions, which cannot be directly verified using POG. Raad et al. [23] provide a transformation technique to replace certain patterns of \mathbf{flush}_{opt} and \mathbf{sfence} with \mathbf{flush} . Specifically, given a program Π that includes \mathbf{flush}_{opt} instructions, provided that Π meets certain conditions, this transformation mechanism rewrites Π into an equivalent program Π' that uses \mathbf{flush} instructions instead, allowing one to use POG. However, there are three limitations to this strategy: 1) the rewriting is an external mechanism that requires stepping outside the POG logic;

2) the rewriting is potentially expensive and must be done for every program that includes $\mathbf{flush}_{\mathrm{opt}}$; and 3) the transformation technique is incomplete in that not all programs meet the stipulated conditions (e.g. Epoch Persistency 2), and thus cannot be verified using this technique. PIEROGI has no such limitations, as we showed in the examples in Section 4. Moreover, POG has no corresponding mechanisation, and developing a mechanisation that also efficiently handles the program transformation for $\mathbf{flush}_{\mathrm{opt}}$ instructions would be non-trivial.

The Owicki–Gries method was first applied to non-SC memory consistency by Lahav et al. [18]. One way that their approach, which targets the release/acquire memory model, is different from ours is that they aim to use standard SC-like assertions; in order to retain soundness under a weak memory model, they had to strengthen the standard stability conditions on proof outlines. Dalvandi et al. [9, 11] took a different approach when designing their Owicki–Gries logic for the release/acquire fragment of C11: by employing a more expressive, view-based assertion language, they were able to stick with the standard stability requirement. In our work, we follow Dalvandi et al.'s approach. However, our assertions are fine-tuned to cope with the other types of view present in Px86_{view}, such as those corresponding to the persistent and the asynchronous views. It is interesting that some of the principles of view-based reasoning apply to different memory models, and future work could look at unifying reasoning across models.

Dalvandi et al. [11] have developed a deeper integration of their view-based logic using the Owicki–Gries encoding of Nipkow and Prensa Nieto [20] in Isabelle/HOL. Such an integration would be straightforward for PIEROGI too, allowing verification to take place without translating programs into a transition system. This would be much more difficult for POG since Owicki–Gries rules themselves are different from the standard encoding in Isabelle/HOL, in addition to the transformation required for **flush**_{opt} instructions discussed above.

The idea of extending Hoare triples with crash conditions first appeared in the work of Chen et al. [6]. However, that work supports neither concurrency nor explicit flushing instructions. Related ideas are found in the works of Ntzik et al. [21] and Chajed et al. [5]. However, in contrast to PIEROGI, both of these works 1) assume sequentially consistent memory, as opposed to a weak memory model such as TSO; 2) assume strict persistency (where store and persist orders coincide); and 3) assume there is a synchronous **flush** operation, which is easier to reason about than the asynchronous **flush** operation.

Besides program logics, there have been other recent efforts to help programmers reason about persistent programs. For instance, Abdulla et al. [1] have proven that state-reachability for persistent x86 is decidable, thus opening the door to automatic verification of persistent programs, and Gorjiara et al. [13] have developed a model checker for finding bugs in persistent programs.

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A Additional examples

A.1 Second message passing example with a flush instruction

```
 \left\{ a = 0 \land \forall v \in \{x, y, z\}, \tau \in \{1, 2\}. \ [v]_{\tau} = [v]^{\mathsf{P}} = \{0\} \right\}   \left\{ (7 \in [y]_2 \Rightarrow \langle y, 7 \rangle [x]_2 = \{42\}) \land [y]_2 \subseteq \{0, 7\} \land [z]^{\mathsf{P}} = \{0\} \right\}   a := \mathbf{load} \ y;   \left\{ (a = 7 \Rightarrow [x]_2 = \{42\}) \land [z]^{\mathsf{P}} = \{0\} \right\}  if (a \neq 0)  \left\{ [x]_2 = \{42\} \land [z]_P = \{0\} \right\}  flush x;  \left\{ [x]^{\mathsf{P}} = \{42\} \right\}  store z \ 1;  \left\{ [z]^{\mathsf{P}} = \{0\} \lor [x]^{\mathsf{P}} = \{42\} \right\}   \left\{ [z]^{\mathsf{P}} = \{0\} \lor [x]^{\mathsf{P}} = \{42\} \right\}   \left\{ [z]^{\mathsf{P}} = \{0\} \lor [x]^{\mathsf{P}} = \{42\} \right\}   \left\{ [z]^{\mathsf{P}} = \{0\} \lor [x]^{\mathsf{P}} = \{42\} \right\}
```

Fig. 13: Message passing with a flush instruction

A.2 Flush buffering with flushopt

A flush buffering variation where the **flush** instructions are replaced with **flush**_{opt} and **sfence** instructions is given in §A.2. Notice here, that because of the reodering that can occur between **store** and **flush**_{opt} instructions on diffrent addresses, both the value of x and y can be 0 in persistent memory even if the value 1 is persisted at w and z.

Fig. 14: A flush buffering variation with **flush**_{opt} and **sfence** instructions

```
 \left\{ a = 0 \land \forall o \in \{x,y,z\}, \tau \in \{1,2\}. \ [o]_{\tau} = [o]^{\mathsf{P}} = \{0\} \right\}   \left\{ [y]^{\mathsf{P}} = \{0\} \land [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ \text{store } x \ 1; \right. \\ \left\{ ([x]_2 = \{1\} \lor [x]_2 = \{1,2\}) \land [y]^{\mathsf{P}} = \{0\} \land [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2 = \{0\} \lor [x]_2 = \{1\} \right\}   \left\{ [x]_2^{\mathsf{A}} = [x]_2 = \{1\} \lor [x]_2^{\mathsf{A}} \subseteq [x]_2 = \{1,2\}) \land \right. \right\}   \left\{ [x]_2^{\mathsf{A}} = [x]_2 = \{1\} \lor [x]_2^{\mathsf{A}} \subseteq [x]_2 = \{1,2\} ) \land \right.   \left\{ [y]^{\mathsf{P}} = \{0\} \land [z]^{\mathsf{P}} = \{0\} \right\}   a := \mathbf{load} \ x;   \left\{ (a = 2 \Rightarrow [x]_2^{\mathsf{A}} \subseteq \{1,2\}) \land [y]^{\mathsf{P}} = \{0\} \land [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{A}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \land [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [y]^{\mathsf{P}} = \{0\} \lor [z]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [x]^{\mathsf{P}} = \{0\} \lor [x]^{\mathsf{P}} = \{0\} \right\}   \left\{ [x]_2^{\mathsf{P}} \subseteq \{1,2\} \lor [x]^{\mathsf{P}} = \{1\}
```

Fig. 15: Proof outline for second epoch persistency example

Epoch persistency

We now consider a second epoch persistency example in Fig. 15. The only difference between the example Fig. 15 and Fig. 11 is the ordering of the operations $flush_{opt}$ and load. The write to z in both examples is used to witness whether the instructions of thread 2 has occurred. The crash invariant of Fig. 15 states that if z and y hold the value 1 in persistent memory then x has either the value 1 or 2 in the persistent memory.

The first **store** of thread 2, and the **flush**_{opt} that follows, are performed at the same address, therefore cannot be reordered. Reading the value 1 at y implies that the **store** of value 2 at x is performed before the **store** of value 1 at x. Otherwise, thread 2 would only have the option to read the value 1 at x. Given the aforementioned store order, the flush_{opt} of thread 2 can view either the value 1 or 2 at x. The **load** instruction that follows does not have any impact on the values that the flush_{opt} instruction can view as it can not be reordered before it. The subsequent **sfence** ensures that either 1 or 2 is persisted at x.

In this example, the crash invariant holds due to thread 2. The initialisation clearly satisfies the precondition of the program. The postcondition of the instruction store x 1 obtains two disjuncts regarding the view of thread 2 at x. This disjuction is necessary to establish the stability of the precondition of threads 2's instruction flush_{opt} x, against threads 1's instruction store x 2. In the case that **store** x 2 precedes **store** x 1, after executing **store** x 1, $[x]_2 = \{1\}$ holds. This follows by rule SP_1 . If the order is flipped, $1 \in [x]_2$ before the execution of **store** x 2, and execution of this store results in a new observable value $2 \in [x]_2$. After the flush_{opt} is executed, $[x]_2$ is translated into an asynchronous

$$\alpha = \mathbf{mfence}$$

$$T' = T \begin{bmatrix} \mathsf{V}_{\mathsf{rNew}} \mapsto_{\sqcup} T.\mathsf{maxcoh}, \\ \mathsf{V}_{\mathsf{pReady}} \mapsto_{\sqcup} T.\mathsf{maxcoh} \end{bmatrix}$$

$$\langle T, M \rangle \xrightarrow{\alpha} \langle T', M \rangle$$

$$(CAS)$$

$$\alpha = a := \mathbf{CAS} \ x \ e_1 \ e_2$$

$$v_1 = T.\mathsf{regs}(e_1)$$

$$v_2 = T.\mathsf{regs}(e_2)$$

$$M[t] = \langle x := v_1 \rangle$$

$$x \notin M(t..|M|]$$

$$M' = M + [\langle x := v_2 \rangle]$$

$$T' = T \begin{bmatrix} \mathsf{regs}(a) \mapsto \mathsf{true}, \\ \mathsf{coh}(x) \mapsto_{|M|}, \\ \mathsf{V}_{\mathsf{rNew}} \mapsto_{\sqcup} |M|, \\ \mathsf{V}_{\mathsf{pReady}} \mapsto_{\sqcup} |M| \end{bmatrix}$$

$$M' = M + [\langle x := v_2 \rangle]$$

$$\langle T, M \rangle \xrightarrow{\alpha} \langle T', M' \rangle$$

$$(CAS\text{-FAIL-INTERNAL})$$

$$\alpha = a := \mathbf{CAS} \ x \ e_1 \ e_2$$

$$M[t] = \langle x := v \rangle$$

$$T.\mathsf{coh}(x) = t$$

$$(x \in M(t..|M|] \lor v \neq T.\mathsf{regs}(e_1))$$

$$T' = T [\mathsf{regs}(a) \mapsto_{\mathsf{false}}]$$

$$(CAS\text{-FAIL-EXTERNAL})$$

$$\alpha = a := \mathbf{CAS} \ x \ e_1 \ e_2$$

$$M[t] = \langle x := v \rangle$$

$$T.\mathsf{coh}(x) < t$$

$$T' = T [\mathsf{regs}(a) \mapsto_{\mathsf{false}}, \\ \mathsf{coh}(x) \mapsto_{\mathsf{them}} \mathsf{them} \mathsf{t$$

Fig. 16: Additional instructions

view (by rule OP). Specifically, if $[x]_2 = \{1\}$ then after the execution of $\mathbf{flush}_{\mathrm{opt}}$, $[x]_2^{\mathsf{A}} = \{1\}$. If $[x]_2 = \{1,2\}$ then after the execution of $\mathbf{flush}_{\mathrm{opt}}$, $[x]_2^{\mathsf{A}} \subseteq \{1,2\}$ holds. Notice that in order for thread 2 to read value 2 for x, this value should be contained in $[x]_2$. As a result, in the case where the **if** statement succeeds, $[x]_2 = \{1,2\}$ and consequently $[x]_2^{\mathsf{A}} \subseteq \{1,2\}$. The execution of **sfence** translates the asynchronous view $[x]_2^{\mathsf{A}} \subseteq \{1,2\}$ to the corresponding persistent view $[x]_2^{\mathsf{P}} \subseteq \{1,2\}$ (by rule SFP). In case that the **if** statement fails, we are certain that $[y]_2^{\mathsf{P}} = \{0\}$, thus the crash invariant holds trivially.

```
\{\forall v \in \{lx, x, y, z\}, \tau \in \{1, 2, 3\}. [v]_{\tau} = \{0\} \land [v]^{\mathsf{P}} = \{0\}\}
                                                                                                                                        \int (\lceil lx : 0 \rceil \land a_1 = 0) \lor
  \left( \left\| lx : 2 \right\| \wedge a_1 = 0 \right)
                                                                                                                      a_2 := \mathbf{CAS} \ lx \ 0 \ 2;
a_1 := \mathbf{CAS} \ lx \ 0 \ 1;
                                                                                                                           \begin{cases} (\|[lx:2]\| \land a_2 = 1 \land 1 \notin [x]_2 \land [z]^P = \{0\}) \lor \\ (\|[lx:2]\| \land [x]^P = [y]^P = \{1\} \land \\ [z]^P = \{0\} \land a_2 = 1 \land [x]_2 = \{1\} \end{cases} \lor \\ (a_2 = 0 \land [z]^P = \{0\}) \end{cases}
 \{(a_1 = 1 \land [[lx : 1]]) \lor a_1 = 0\}
if (a_1 = 1)
 \{ [[lx:1]] \}
                store x 1;
                  \int [[lx:1]] \wedge

\begin{cases}
([[lx:2]] \land 1 \notin [x]_{2} \land [z]^{P} = \{0\}) \lor \\
([[lx:2]] \land [x]^{P} = \{1\} \land [y]^{P} = \{1\} \land \\
[z]^{P} = \{0\} \land [x]_{2} = \{1\})
\end{cases}

a_{3} := load y;
                  \int ||x||_1 \wedge [y]_1 = \{1\}
                                                                                                                                            \begin{cases} \left(a_{3} = 1 \Rightarrow \lceil lx : 2 \rceil \land \lceil x \rceil^{\mathsf{P}} = \{1\} \land [y]^{\mathsf{P}} = \{1\} \land [x]_{2} = \{1\} \\ \lceil lx : 2 \rceil \land [z]^{\mathsf{P}} = \{0\} \end{cases}
                 flush x;
                    \begin{cases} \lceil \lceil lx : 1 \rceil \rceil \wedge [x]^{\mathsf{P}} = \{1\} \wedge \\ \lceil x \rceil \rceil_1 \wedge [y]_1 = \{1\} \end{cases}
                    \wedge [x]_1 = \{1\}
                                                                                                                                                            \{[x]^{\mathsf{P}} = \{1\} \land [y]^{\mathsf{P}} = \{1\} \land [[lx:2]]\}
                 flush y;
                                                                                                                                                              \left\{ \begin{bmatrix} x \end{bmatrix}^{\mathsf{P}} = \{1\} \land [y]^{\mathsf{P}} = \{1\} \land \\ \begin{bmatrix} lx : 2 \end{bmatrix} \land [z]_1 = \{1\} \end{bmatrix} \right\} 
                                                                 \left\{ \left[ z \right]^{\mathsf{P}} = \left\{ 0 \right\} \lor \left( \left[ x \right]^{\mathsf{P}} = \left\{ 1 \right\} \land \left[ y \right]^{\mathsf{P}} = \left\{ 1 \right\} \right) \right\} 
 \left\{ \left\{ \dot{x} : \left[ z \right]^{\mathsf{P}} = \left\{ 1 \right\} \Rightarrow \left( \left[ x \right]^{\mathsf{P}} = \left\{ 1 \right\} \land \left[ y \right]^{\mathsf{P}} = \left\{ 1 \right\} \right) \right\}
```

Fig. 17: CAS-based locking

B Additional Px86_{view} instructions

B.1 Example with cas

Our next example use the compare and set (**cas**) instruction. Notice that from the semantics of **cas** given in Fig. 16 it can be inferred that a **cas** on address x ($a := \mathbf{CAS} \ x \ e_1 \ e_2$) succeeds only if the value that is read in x is e_1 , and e_1 is the last written value on x. In order to facilitate reasoning about **cas** we introduce another view expression, namely [x : v]. This expression is boolean-valued and holds if the last written value on x is v.

Fig. 18 and Fig. 19 present a selection of rules for atomic statements and view-based assertions regarding **cas**. The selection is based on the rules that are

Precondition S	tatement	Postcondition	Const.	Ref.
$\{true\}$		$\{(a = 1 \land [x : e_2]) \lor a = 0\}$		CP_1
$\left\{ [y]_{ au'}=S ight\}$		$\{[y]_{\tau'} \subseteq S\}$	$x \neq y$	CP_2
$\{ \llbracket x : v \rrbracket \} \ a := \mathbf{C}$	$\mathbf{CAS} \ x \ e_1 \ e_2$	$\left\{ \left\ x:e_{2} \right\ \lor \left\ x:v \right\ \right\}$		CP_3
$\left\{ \llbracket y \rrbracket_{\tau'} \land [y]_{\tau'} = \{v\} \right\}$		$\{(a = 1 \land [y]_{\tau} = \{v\}) \lor a = 0\}$	$x \neq y$	CP ₄
$\left\{ \left\ x:v ight\ ight\}$		$\{a=0\}$	$v \neq e_1$	CP_5
$\{true\}$ st	$\mathbf{core} \ x \ v$	$\{ \llbracket x : v rbracket \}$		SP ₈

Fig. 18: Selected proof rules for atomic statements executed by thread τ regarding cas. Note τ may be equal to τ' unless explicitly ruled out.

Statement	Stable Assert.	Const.	Ref.	Statement	Stable Assert.	Const.	Ref.
$a := \mathbf{load} x$	$\{ \llbracket y : v rbracket \}$		LS_6		$\left\{v\notin[y]_{\tau'}\right\}$	$x \neq y$	CS_1
flush x	$\{ \llbracket y : v rbracket \}$		FS ₆	$a := \mathbf{CAS} \ x \ e_1 \ e_2$	$\{ \llbracket x \colon v rbracket \}$	$v \neq e_1$	CS_2
store $x \ v$	$\{ \llbracket y : v rbracket \}$	$x \neq y$	WS ₈	$a := \mathbf{CAS} \ x \ c_1 \ c_2$	$\left\{ \left[y\right]^{P} = S\right\}$	$x \neq y$	CS_3
					$\{ \llbracket y rbracket_{ au'} \}$	$x \neq y$	CS_4

Fig. 19: Selection of stable assertions for atomic statements executed by thread τ regarding cas. Note x may be equal to y and τ may be equal to τ' unless explicitly ruled out.

used in the proof outline of the example Fig. 17. Each of these rules have been proved sound with respect to view-based semantics in Isabelle. For these rules the same conventions are made as for the rules in Fig. 7 and Fig. 8. Rule CP₁ states that after the execution of **cas** on x either a=1 (indicating that **cas** succeeded) and the last written value on x is e_2 , or a=0 (indicating that **cas** failed). By CP₂, providing that $x \neq y$ and τ 's view of y is the set of values S then in the postcondition τ 's view of y is a subset of S. By rule CP₃, given that the last written value on x is v then in the postcondition the last written value either remains the same (indicating that the **cas** failed) or $[x:e_2]$. Rule CP₄ states that given $x \neq y$ if τ ''s view of y is the last write on y and the value of this write is v then in the postcondition either the **cas** succeeds, so a=1 and τ 's view of y is $[y]_{\tau} = \{v\}$ or the **cas** fails and a=0. By rule CP₅ ifthe last written value on x is different from e_1 then a=0. By rule SP₈ after executing a store on x (**store** x v), the value of the last write on x is updated to v. We also prove the stability of several assertions regarding **cas** (see Fig. 19 for a selection).

Let us consider now the program of Fig. 11. In this example we use **cas** as a lock, in order to control accesses on x. The crash invariant here, states that if z holds the value 1 in persistent memory then x and y should also obtain the value 1 in persistent memory. In this example the invariant is establised by thread 2.

In order for the invariant to hold, we must ensure that the **flush** instructions of thread 1, are executed before thread 2 executes **store** z 1. The **cas** instructions in the beginning of the two threads program ensure that the threads are not executing in parallel. In particular, in order for thread 1's **cas** to succeed the value of the last write on x should be 0. If the value of the last write on x is 2, it means that thread 2's **cas** is executed and the execution point hasn't reached

yet the thread 2's instruction **store** lx 0. In this case the thread 1 **cas** fails, and its execution stalls. More concretely, by rule CP_1 , after the execution of **cas** in thread 1, we can obtain that either $a_1 = 1 \land \lceil lx : 1 \rceil$ (indicating that the **cas** succeed) or $a_1 = 0$. Respectively, in order for thread 2's **cas** to succeed the value of the last write on x should be 0. If the value of the last write on x is 1, it means that that thread 1's **cas** is executed and the execution point hasn't reached yet the thread 1's instruction **store** lx 0. In this case the execution of thread 2 stalls. There are two ways for $\lceil lx : 0 \rceil$ to hold for thread 2 before the execution of **cas**. Either the **cas** reads the initial value of lx or it reads the value that lx obtains after thread 1 executes the instruction **store** lx 0. In the second case, which is the desirable one, we are sure that before thread 2 executes **cas**, $[x]^P = [y]^P = [y]^2 = 1$. Those cases are described in the precondition of **cas** in thread 2.

The first disjunct of the precondition concerns the case in which thread 2's write on lx is not executed yet, but the value of the last write on lx is 0. From this it can be inferred that lx obtains is initial value. In this case we are sure that $1 \notin [x]_2$. The consecutive **cas** might succeed, although it is certain that thread 2 can not read 1 at x. As a result, the second **if** statement of thread 2 fails, thus $[z]^P \ne \{1\}$, consequently the invariant holds.

The second disjunct of the precondition concerns the case in which thread 2's **store** lx 0 has been executed. Because the store of 1 at x by thread 1 is ordered before the store of 0 at lx, it is certain that at this point of execution $[x]_1 \wedge [x]_1 = \{1\}$ holds. By rule $\mathsf{CP_4}$ if the consecutive **cas** succeeds, thread 1's view of x is transferred to thread 2. As a result the **if** statement that follows succeeds and **flush** z persists the value 1 at z. Because either $[x]^P = \{1\} \wedge [y]^P = \{1\}$ or $[z]^P = \{1\}$ for every state of thread 2's program, the invariant holds.

The third disjunct of the precondition concerns the case in which thread 1's cas has succeeded and thus [x:1]. In this case thread 2's cas can not succeed and the invariant holds trivially.

B.2 Example with mfence

Our next example use the **mfence** instruction. In order to facilitate reasoning about **mfence** we introduce another view expression, $[x]_{\tau}^{M}$. This expression is boolean-valued and holds iff after performing an **mfence** operation, the view of thread τ will be the last write on x. Specifically,

$$\|x\|_{\tau}^{\mathsf{M}} \triangleq \{\sigma \mid LAST(\sigma.M,x) \leq \sigma.\vec{T}(\tau).\mathsf{maxcoh}\}.$$

Fig. 21 and Fig. 22 extends the proof rules with rules regarding **mfence**. The proof outline of Fig. 20 follows closely the proof outline of the flush buffering example (Fig. 10). Instead of the assertion $\|x\|_{\tau}^{\mathsf{F}}$ we use the analogous assertion for **mfence**, $\|x\|_{\tau}^{\mathsf{M}}$. Two additional auxiliary variables are used to indicate if the **mfence**, of thread 1 (resp. thread 2) is executed. In the end of the execution either $a_1 = 1$ or $a_2 = 1$.

```
 \left\{ \forall o \in \{x,y\}, \tau \in \{1,2\}. \ [o]_{\tau} = \{0\} \right\} \\ \left\{ (\hat{a}, \hat{b} = 0, 0 \land \hat{d} = 0) \lor \\ \left( (\hat{a}, \hat{b} = 0, 1 \land ||y|||_2 \land) \\ \left( (y|_2 = \{1\}) \right) \right\} \\ \left\{ \text{(store } x \ 1, \hat{a} := \hat{b} + 1 \right); \\ \left\{ (\hat{a} = 1 \land \hat{b} \in \{0, 2\} \land) \lor \\ (\hat{d} = 0 \lor r_2 = 1) \lor \\ \left( (\hat{a}, \hat{b} = 2, 1 \land ||y|||_2 \land) \\ (y|_2 = \{1\} \land ||y|||_1 \land \hat{d} = 0) \right\} \\ \left\{ (\hat{a}, \hat{b} = 2, 1 \land ||y||_1 \land \hat{d} = 0) \right\} \\ \left\{ (\hat{a} = 1 \land \hat{b} \in \{0, 2\} \land) \lor \\ (\hat{a} = 0 \lor r_2 = 1) \lor \\ (\hat{a}, \hat{b} = 2, 1 \land ||y||_1 = \{1\}) \right\} \\ \left\{ (\hat{a} = 1 \land \hat{b} \in \{0, 2\} \land) \lor \\ (\hat{a} = 0 \lor r_2 = 1) \lor \\ (\hat{a}, \hat{b} = 2, 1 \land ||y||_1 = \{1\}) \right\} \\ r_1 := \mathbf{load} y; \\ \left\{ (\hat{a} = 1 \land \hat{b} \in \{0, 2\} \land) \lor \\ (\hat{a} = 0 \lor r_2 = 1) \lor \\ (\hat{a}, \hat{b} = 1, 2 \land ||x||_2 = \{1\}) \right\} \\ \left\{ (\hat{a}, \hat{b} = 1, 2 \land ||x||_2 = \{1\}) \right\} \\ r_2 := \mathbf{load} x; \\ \left\{ (\hat{b} = 1 \land \hat{a} \in \{0, 2\} \land) \lor \\ (\hat{c} = 0 \lor r_1 = 1) \lor \\ (\hat{c}, \hat{b} = 1, 2 \land ||x||_2 = \{1\}) \right\} \\ \left\{ (\hat{c} = 0 \lor r_1 = 1) \lor \\ (\hat{a}, \hat{b} = 1, 2 \land r_2 = 1) \right\} \\ \left\{ (\hat{c} = 0 \lor r_1 = 1) \lor \\ (\hat{a}, \hat{b} = 1, 2 \land r_2 = 1) \right\}
```

Fig. 20: Proof outline for flush buffering

Precondition Statement Postcondition				
$\{true\} $ store $x \ v \ \{ \llbracket x \rrbracket_{\tau}^{M} \}$	SP ₉			
$ \begin{cases} \llbracket x \rrbracket_{\tau'} \land \llbracket x \rrbracket_{\tau}^{M} \land [x]_{\tau'} = \{u\} \\ \{[x]_{\tau} = S\} \end{cases} $ mfence $ \begin{cases} [x]_{\tau} = \{u\} \\ \{[x]_{\tau} \subseteq S\} \end{cases} $	MFP_1			
$\left\{[x]_{\tau} = S\right\}$ intence $\left\{[x]_{\tau} \subseteq S\right\}$	MFP_2			

Fig. 21: Selected proof rules for atomic statements executed by thread τ regarding **mfence**. Note τ may be equal to τ' unless explicitly ruled out.

Statement	Stable Assert.	Const.	Ref.
$a := \mathbf{load} x$	$\{ \llbracket y Vert_{ au'}^{M} \}$		LS ₇
store $x \ v$	$\{ \llbracket y Vert^M_{ au'} \}$		WS_9
mfence	$\{[x]^{P} = S\}$		MFS_1
	$\{ \llbracket x \rrbracket_{\tau'} \}$		MFS_2
	$\left\{ \left\ x \right\ _{\tau'}^{M} \right\}$	$\tau \neq \tau'$	MFS_3
	$\{ x,v =n\}$		MFS_4

Fig. 22: Selection of stable assertions for atomic statements executed by thread τ regarding **mfence**. Note x may be equal to y and τ may be equal to τ' unless explicitly ruled out.

C Proof of Theorem 1

Theorem 1 (Soundness of Pierogi). Suppose that a program Π has a valid proof outline $\langle in, ann, I, fin \rangle$. Let σ be a state of $Px86_{view}$ that is reachable in an execution of Π from some state σ_{init} of the form $\langle \lambda \tau. \iota, \vec{T}_{init}, M_{init}, G_{init} \rangle$ such that $\sigma_{init} \in in$. Then, the following hold:

- 1) For every $\tau \in \text{Tid}$, we have that $\sigma \in ann(\tau, \sigma.\vec{pc}(\tau))$.
- 2) If $\sigma . \vec{pc}(\tau) = \zeta$ for every $\tau \in \text{Tid}$, then $\sigma \in \text{fin}$.
- 3) Every non-volatile memory NVM that is possible in σ satisfies the crash invariant I.

Formally, when checking if NVM satisfies I, one has to translate every $[x]^{\mathsf{P}}$ expression in I to $\{x\}$. For example, $I = [y]^{\mathsf{P}} = \{1\} \Rightarrow [x]^{\mathsf{P}} = \{1\}$ is translated into $\{y\} = \{1\} \Rightarrow \{x\} = \{1\}$, and $NVM : \mathsf{Loc} \to \mathsf{VAL}$ satisfies I if $NVM(y) = 1 \Rightarrow NVM(x) = 1$ holds. Recall that we assume that the only "specialised" logical expressions in persistent invariants are of the form $[x]^{\mathsf{P}}$.

Proof. We prove the item first by induction on the length of the trace. The basis of the induction follows from the Initialisation condition in the definition of a valid outline (Definition 1). Now, for each step in the trace performed by thread θ (i.e. a transition obtained by PROGRAM-NORMAL or PROGRAM-IF with $\tau := \theta$), the inductive step follows from the Local correctness condition for $\tau = \theta$, or for the Stability condition for $\tau \neq \theta$. The second item follows form the first using the Finalisation condition. Finally, to see that the third item holds, let $NVM : Loc \rightarrow VAL$ be a non-volatile memory that is possible in σ . By the Persistence condition, we know that there exists $\tau \in TID$ such that $ann(\tau, \sigma.\vec{pc}(\tau)) \Rightarrow I$. By the first item, we have $\sigma \in ann(\tau, \sigma.\vec{pc}(\tau))$, and so, it follows that $\sigma \in I$. The fact that NVM satisfies I satisfies the persistent invariant I follows from Proposition 1.