Imperial College of Science, Technology and Medicine
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Resource-Constrained Acquisition Circuits for Next Generation Neural Interfaces

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Declaration of Originality

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Abstract

The development of neural interfaces allowing the acquisition of signals from the cortex of the brain has seen an increasing amount of interest both in academic research as well as in the commercial space due to their ability to aid people with various medical conditions, such as spinal cord injuries, as well as their potential to allow more seamless interactions between people and machines. While it has already been demonstrated that neural implants can allow tetraplegic patients to control robotic arms, thus to an extent returning some motoric function, the current state of the art often involves the use of heavy table-top instruments connected by wires passing through the patient's skull, thus making the applications impractical and chronically infeasible.

Those limitations are leading to the development of the next generation of neural interfaces that will overcome those issues by being minimal in size and completely wireless, thus paving a way to the possibility of their chronic application. Their development however faces several challenges in numerous aspects of engineering due to constraints presented by their minimal size, amount of power available as well as the materials that can be utilised.

The aim of this work is to explore some of those challenges and investigate novel circuit techniques that would allow the implementation of acquisition analogue front-ends under the presented constraints. This is facilitated by first giving an overview of the problematic of recording electrodes and their electrical characterisation in terms of their impedance profile and added noise that can be used to guide the design of analogue front-ends.

Continuous time (CT) acquisition is then investigated as a promising signal digitisation technique alternative to more conventional methods in terms of its suitability. This is complemented by a description of practical implementations of a CT analogue-to-digital converter (ADC) including a novel technique of clockless stochastic chopping aimed at the suppression of flicker noise that commonly affects the acquisition of low-frequency signals. A compact design is presented, implementing a 450 nW, 5.5 bit ENOB CT ADC, occupying an area of 0.0288 mm^2 in a 0.18 µm CMOS technology, making this the smallest presented design in literature to the best of our knowledge.

As completely wireless neural implants rely on power delivered through wireless links, their supply voltage is often subject to large high frequency variations as well voltage uncertainty

making it necessary to design reference circuits and voltage regulators providing stable reference voltage and supply in the constrained space afforded to them. This results in numerous challenges that are explored and a design of a practical implementation of a reference circuit and voltage regulator is presented. Two designs in a 0.35 µm CMOS technology are presented, showing respectively a measured PSRR of ≈60 dB and ≈53 dB at DC and a worst-case PSRR of ≈42 dB and ≈33 dB with a less than 1% standard deviation in the output reference voltage of 1.2 V while consuming a power of ≈7 µW.

Finally, ΣΔ modulators are investigated for their suitability in neural signal acquisition chains, their properties explained and a practical implementation of a ΣΔ DC-coupled neural acquisition circuit presented. This implements a 10-kHz, 40 dB SNDR ΣΔ analogue front-end implemented in a 0.18 µm CMOS technology occupying a compact area of 0.044 μm^2 per channel while consuming 31.1 µW per channel.

Acknowledgements

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List of Acronyms

ADC	Analogue-to-Digital Converter
AFE	Analogue Front-End
BCD	Bipolar-CMOS-DMOS
BCI	Brain-Computer Interface
BJT	Bipolar Junction Transistor
BMI	Brain-Machine Interface
CDMA	Code-Division Multiple Access
CDS	Correlated Double Sampling
CIC	Cascaded Integrator-Comb
CL-LDO	Capacitor-less Low Dropout Regulator
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CSF	Cerebrospinal Fluid
CT	Continuous Time
CTAT	Complementary to Absolute Temperature
DAC	Digital-to-Analogue Converter
DC	Direct Current
DT	Discrete Time
DUT	Device Under Test
EAP	Extracellular Action Potential
ECG	Electrocardiogram
ECoG	Electrocorticography
EEG	Electroencephalogram
ENGINI	Empowering Next Generation Implantable Neural Interfaces
ENOB	Effective Number of Bits
ESR	Equivalent Series Resistance
FDA	Food and Drug Administration of the United States
FOM	Figure of Merit

ISM	Industrial, Scientific and Medical
JFET	Junction Field Effect Transistor
LDO	Low Dropout Regulator
LFP	Local Field Potential
LSB	Least Significant Bit
LSK	Load Shift Keying
MEA	Multi-Electrode Array
MEG	Magnetoencephalography
MOM	Metal Oxide Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NEF	Noise Efficiency Factor
NGNI	Next Generation Neural Interfaces
NMOS	n-Channel Metal Oxide Semiconductor
OSR	Oversampling Ratio
PBS	Phosphate Buffered Saline
PCB	Printed Circuit Board
PMOS	p-Channel Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
PSD	Power Spectral Density
RMS	Root Mean Squared
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SNDR	Signal to Noise and Distionrtion Ratio
SNR	Signal to Noise Ratio
SRS	Stanford Research Systems
STD	Standard Deviation
STFT	Short Time Fourier Transform

UVLO	Undervoltage Lockout
ZTC	Zero Temperature Coefficient
$\Sigma\Delta$	Sigma Delta

List of Symbols

K^+	Potassium Cation
Cl^-	Chlorine Anion
Na^+	Sodium Cation
TnO_5	Tantalum Pentoxide
NaCl	Sodium Chloride
A	Amplitude
A_g	Geometric Area
A_s	Surface Area
A_{in}	Input Attenuation Factor
B	Bandwidth
$B(t)$	Time-Varying Bandwidth
B_{avg}	Average Bandwidth
B_c	Comparator Bandwidth
B_{max}	Maximal Bandwidth
BW	Bandwidth
C	Compression Ratio
C_{dl}	Double-Layer Capacitance
C_{dl0}	Zero Potential Double-Layer Capacitance
C_{DS}	Drain-Source Capacitance
C_H	Helmholtz Capacitance
C_{GC}	Gouy-Chapman Capacitance
C_L	Load Capacitance
C_{ox}	Oxide Capacitance
C_p	Parasitic Capacitance
d_{ec}	Eletrode-Cell Distance
e_q	Quantisation Error
E	Young's Modulus
f_c	Corner Frequency or Clock Frequency

f_s	Sampling Frequency
f_t	Tone Frequency
g_{mx}	Small Signal Transconductance of Device x
G_m	Transconductance
$H(f)$	Transfer Function
$X(f)$	Fourier Transform of x(t)
$X(s)$	Laplace Transform of x(t)
i_{out}	Output current
I_0	BJT Reverse Saturation Current
I_D	Drain Current
I_{tot}	Total Consumed Current
I_s	Sunk Current or Sourced Current
J_0	Exchange Current Density
$J_{0,Nb}$	Exchange Current Density of Niobium
$J_{0,Pt}$	Exchange Current Density of Platinum
k	Boltzmann Constant
K_f	Flicker Noise Constant
N	Resolution (Bits)
N_q	Number of Quantisation Levels
P	Power
P_N	Noise Power
P_S	Signal Power
q	Electron Charge
r_{ox}	Small Signal Output Resistance of Device x
r_{out}	Output Resistance
R	Noise Reduction Factor
$R_x(\tau)$	Autocorrelation of x(t)
R_{ct}	Charge Transfer Resistance
R_{DS}	Drain-Source Resistance

R_L	Load Resistance
R_s	Spreading Resistance
$S_c(f)$	Chopper Spectrum
$S_x(f)$	Spectrum of x(t)
$S_{ni}(f)$	Input Noise Spectrum
SR_{in}	Input Slew Rate
t_d^{max}	Maximal Time Delay
t_p	Pulse Length
T	Ambient Temperature
T_s	Sampling Period
v_s	Signal Voltage
v_{dd}	Supply Voltage
v_{nadc}	Quantisation Noise
v_{nbio}	Biological Noise
v_{nel}	Electrode Noise
v_{nfe}	Front-End Noise
V_{el}	Potential Across Electrode
V_{gs}	Gate-Source Voltage
V_{out}	Output Voltage
$V_{rms,in}$	Input-Referred RMS Noise
V_{supply}	Supply Voltage
V_t	Thermal Voltage or Threshold Voltage
WL	Gate Area
z	Valence of Ions
Z_{ey}	Electrolyte Impedance
Z_{ey}^{cyl}	Electrolyte Impedance, Cylinder Approximation
Z_{el}	Electrode Impedance
Z_{in}	Input Impedance
Z_w	Warburg Impedance

Δ_q	Size of Quantisation Level
δq	Excess Charge
δV_q	Potential of One Quantisation Level
κ	Gate Coupling Coefficient
ω	Angular Frequency
ω_p	Pole Frequency
ω_z	Zero Frequency
ω_G	Pole Located at Transistor Gate
ω_L	Pole Located at The Output of a Circuit
ρ_{ey}	Electrolyte Conductance
σ_f	Frequency Standard Deviation
σ_t	Time Standard Deviation
σ^2	Variance
τ_w	Window Width
sinc(x)	Sinc Function sin(x)/x
$\cosh(x)$	Hyperbolic Cosine
$\delta(t)$	Dirac Delta
$\Re(\cdot)$	Real Part
$\lvert\cdot\rvert$	Magnitude
$\angle\cdot$	Angle
$E[\cdot]$	Energy of a Signal
$\Longleftrightarrow$	Transform Pair

Chapter 1

Introduction and Motivation

The human brain has captured the curiosity of scientists and people ever since the early days of mankind and interest in its anatomy can be traced back as early as Ancient Greece [1] when people started observing brain injuries in soldiers wounded in battles and their effect on health and resulting disabilities. This led to the first steps in understanding the anatomy of the neural system and the function of some of its individual parts as well as the understanding that the brain is the center of thinking and intelligence. The science of the time, however, could not understandably answer deeper questions about the true nature of the neural system's operation and was limited to rudimentary observations.

This to a large extent remained the case throughout many centuries to come but was interrupted by an increased interest in the human body brought by the Renaissance which led to some of the first modern brain dissections and resulting advances in anatomy [2]. A deeper insight into the functioning of the brain and its tissue was, however, enabled by discoveries in a seemingly unrelated field - physics, more specifically the physics of electricity. This led to the, now notoriously known, experiment of Luigi Galvani conducted in 1791 [3] that perhaps for the first time showed a clear connection between electricity and the neural system by inducing movement in dissected frog legs using electrical stimuli. Galvani's experiment not only started a wave of interest in the research of electricity but also started a new scientific field of electrophysiology, a study of electric processes in the human body and their observation, eventually leading to

the development of such diagnostic tools as Electrocardiograms (ECG), Electroencephalograms (EEG) and many others.

The understanding of a neuron as the basic building block of the neural system, would however only come about a hundred years later when J. E. Purkyne described the Purkinje cell which then became the first documented neuronal cell. The first recording of electrical activity observed in neurons was then reported in 1928 by E. Adrian [4] who was able to obtain it using a capillary electrometer. This gave the first insight into the inner functioning of the neural system and started an endeavour that would eventually lead to the development of a multitude of medical applications relying on electronics interfacing with the neural tissue to aiding people's well-being and helping in the treatment of various medical conditions and ailments.

1.1 Motivation

While the publication of E. Adrian was perhaps the first documented example of a successful recording of electrical activity in neural tissue, there have at the time already been several publications documenting the effects of the opposite, the stimulation of the neural tissue with electricity. One of the early, most historically significant, results in this space can be attributed to E. Hitzig who demonstrated that electrical stimulation of brain tissue leads to involuntary eye movement in people, dogs and other animals in 1870 [5].

Arguably, this head start of about 60 years, when compared to recording efforts, was reflected in the earlier medical adoption and feasibility of brain stimulation as opposed to the use of neural recordings. One of the notable examples of the early pioneers of neurostimulation is W. Penfield who in 1936 demonstrated [6] a medical procedure based on stimulation of the brain to relieve epilepsy in patients. Building on this work, C.N. Shealy et al. [7] have demonstrated the use of a chronically implanted stimulator to reduce chronic pain in terminally ill cancer patient.

Those successful demonstrations soon led to the research of the possibility of stimulating other areas of the brain, thus enabling additional applications. As the brain is the center of cognition,

it is only natural to ask ourselves whether it is possible convey information into the brain by stimulating the neural system and thus replacing or enhancing one of the five basic senses. While inducing the sense of touch with electrical stimulation is arguably simple and most likely the first sense to have ever been electrically induced, hearing is another sense that early on became successfully interfaced to electronic circuits by means of stimulating the neural system in the form of cochlear implants restoring hearing in people with certain hearing impairments by directly stimulating the cochlear nerve.

1.1.1 Cochlear Implants

The history and research of cochlear implants [8] on its own is a long and very elaborate topic that is seeing major contributions and additions until this day. Some of the original breakthrough work was done independently by W. House and A. Djourne with C. Eyries in the late 1950s and early 1960s having described the possibility of implanting a patient with a single-electrode implant stimulating the cochlea and to some extent returning the sensation of hearing. Some of the early experimental results of implanting those devices in people were obtained by P. Michelson who implanted [9] single-channel stimulators which led to the subjects being able to distinguish the pitch and amplitude of the played auditory stimuli. Those early implants were however not advanced enough to allow comprehension of natural language.

To understand how to improve on this, let us consider that the biological cochlea mechanically decomposes any sound-induced vibrations into various frequency bands in turn stimulating various sections of the auditory nerve [10]. Achieving better performing cochlear implants thus necessitates an increase in the amount of stimulating channels and therefore allowing more information to be conveyed to the neural system. To achieve this, it is necessary to decompose the auditory signal into separate frequency bands which requires the development of novel signal processing methods that would efficiently decompose the input sounds into individual spectral bands, all within the domain of an implanted device, resource-constrained both in terms of space as well as energy. As we will demonstrate throughout this thesis, the need to invent novel methods that solve engineering problems working around those limitations is a recurrent topic

in the space of neural implants.

The earliest devices achieved spectral separation by employing analogue filter banks [10] but the fast-paced development of microprocessors soon led to them being replaced by more versatile digital processing techniques. One of the first multi-channel implants was demonstrated and implanted by G. Clark in 1979 [11] which led to initial successes in speech recognition within patients with cochlear prostheses [12]. Those advances eventually led to the FDA (Food and Drug Administration of the United States) approving the Nucleus 22 [13] as the first cochlear implant for general use in 1985. Nowadays, cochlear implants are arguably the most commonly used neural implants and an example of what the field can bring to improve lives and well-being of patients.

1.1.2 Retinal Implants

Another example of neroprosthetics can be found in retinal implants that interface the nerve endings in the retina, thus allowing the return of the sense of vision to patients with some forms of visual impairments. The required complexity in terms of the needed amount of stimulation points as well as the signal processing arguably makes the development of those implants comparably more complicated to the cochlear implants which is reflected by their lengthier development and the current state of the art. Some of their earliest history [14] dates back to the late 1920s and early 1930s when B.O. Foerster demonstrated that electrically stimulating the visual cortex can lead to visual sensations perceived by the test subject. Another breaktrough was achieved in 1968 by G. S. Brindley et al. [15] having inserted an array of 81 electrodes touching the visual cortex of a blind patient allowing him to identify visible visual spots in consistent areas of the visual field upon their stimulation. This followed their previous estimation that 50 individual visual channels should provide sufficient visual clarity to allow the identification of letters. It is also interesting to note that this work presents early considerations for chronic implantation of electrode arrays and mentions the need for wireless data transmission in order to prevent a permanent puncture of the skin otherwise needed for wired connections.

While the early retinal prosthetic devices relied on direct stimulation of the visual cortex, later attempts at tackling the problem instead resorted to stimulating the neural endings in the retina, thus leading to a clearer mapping between electrode location and the corresponding point in the patient's visual field. Although leading to more successful implants, this also reduced the number of patients this technology can be indicated for as it e.g. excludes patients with a damaged optical nerve.

The research efforts have resulted in the development of Argus II [16], the first commercially available retinal prosthetic that was cleared by the FDA in 2013 for normal clinical usage prescribeable as a treatment for retinitis pigmentosa, a genetic disease that leads to a degradation of photoreceptor cells and a gradual visual loss. The Argus II relies on an array of 60 electrodes, thus providing a fairly limited resolution but, equally to the case of cochlear implants starting with a single channel, further research and development [17] is already leading to increases in the amount of channels and creation of more advanced devices is expected in the near future.

Both the state-of-the-art cochlear as well as retinal implants typically rely on the stimulation of nerve endings in the respective centres of the senses and while some of the early experiments with retinal prostheses attempted direct stimulation of the visual cortex in the brain, this is not an approach that is used in today's commercial products such as the Argus II. Similarly direct stimulation of the auditory cortex to treat deafness is not something that is typically attempted and is not used by clinically used cochlear implants although it has been researched in the past [18]. On the other hand, there is research suggesting that direct electrical stimulation of the auditory cortex can lead to relief in patients suffering from chronic tinnitus [19]. Although those applications are not very common, deep brain stimulation (DBS) has found extensive use in the relief of symptoms of Parkinson disease and suppression of tremors.

1.1.3 Recording Implants

So far we have considered neuroprostheses that convey information to the neural system by means of its stimulation. Let us now consider devices that achieve the opposite, the extraction of information from the neural system. While the first signs of electrical activity in the brain

and the neural system were observed as long as several hundred years ago and E. Adrian was able to obtain a recording of a single neuronal activity in 1928, there was still a long way to being able to perform useful functions using the recorded neural signals. Before we dive into the discussion of how this can be achieved, let us consider some of the possible applications of such technologies, typically referred to as Brain-Machine Interfaces (BMI) or Brain-Computer Interfaces (BCI).

Perhaps the most obvious is the possibility of controlling a machine using one's thoughts. Barring various ideas from the world of science fiction, one of the applications receiving the biggest amount of interest is the possibility to aid people with spinal cord injuries [20] that lead to various levels of immobility in patients or, even more severely, patients with the locked-in syndrome [21] who are completely unable to communicate with the outside world and for whom a BCI becomes the only possible method of communication. This can come in the very rudimentary form of allowing control of a cursor [22] on a computer screen or lead to more advanced prostheses replacing the function of some muscles or limbs while allowing the patient to control a robotic arm using their thoughts [23]. Although the locked-in syndrome is not very common, spinal cord injuries leading to partial paralysis are a lot more frequent occurrence. Their incidence varies around the world but is typically between 10 and 50 cases per million people [24] and rises with age but notably peaks in people between 15 and 29 years old being mainly caused by falls and accidents in the respective age groups.

Aside from medical applications, it is easy to imagine that future BCIs could be used to facilitate other functions such as more natural control of computers using thoughts rather than using mice and keyboards [25], new forms of entertainment [26] made possible by more immersive virtual reality experience or even driving vehicles using thoughts [27]. Those possibilities have lately led to increased interest not only from the research community but also from commercial projects such as from Kernel and Neuralink who are hoping to capitalise on the expected growth of the BCI market. Arguably, the science and level of understanding of the human brain is still in its early days, making the research of BCIs a very interesting field, while at the same time having a great potential in improving the well-being and clinical outcomes of many patients.

1.2 Neural Signals

Before exploring some of the more detailed aspects of BCIs' operation, let us briefly consider the nature and origin of neural signals, as well as their typical stratification. Since the early days of the discovery of the Purkinje cell, it was understood that the activity of the neural system stems from the neuron as its basic building block. As described by S. Gibson [28], the operation of neurons is electrochemical in nature and can be described by reactions involving the exchange of K^+, Cl^- and Na^+ ions. In a largely abstract sense, a neuron can be considered a biochemical device that performs a series of some of the most basic mathematical operations, an integration and thresholding.

1.2.1 Extracellular Action Potentials

In its resting state, a neuron has a large concentration of K^+ and Cl^- ions inside its body. Following the mathematical integrator analogy, it receives its inputs from synapses, connections with other neurons, and when one of the synapses gets excited by an output of a neighbouring neuron, an ion channel is opened allowing an influx of Na^+ ions leading to a rising potential inside its body. At a certain point, the neuron reaches its peak polarisation and K^+ ions start flowing out of the neuron's body, thus returning its potential to a resting state. This results in a typical electrical potential response measurable outside the neuron's body termed the Extracellular Action Potential (EAP), also more colloquially referred to as a neural spike. This is the most elementary neural signal that gives us information about the activity of a single neuron and at the same time arguably is the most accurate and granular source of information about brain activity.

Inserting an electrode into neural tissue and obtaining a recording however leads to the acquisition of a far more complex signal as demonstrated by Figure 1.1. Due to the close proximity of neurons, it is typically impossible to obtain action potentials from isolated neurons and the recorded signal rather contains spikes generated by several neurons in the proximity of the inserted electrode. A technique called spike sorting [29; 28] is then typically employed to split

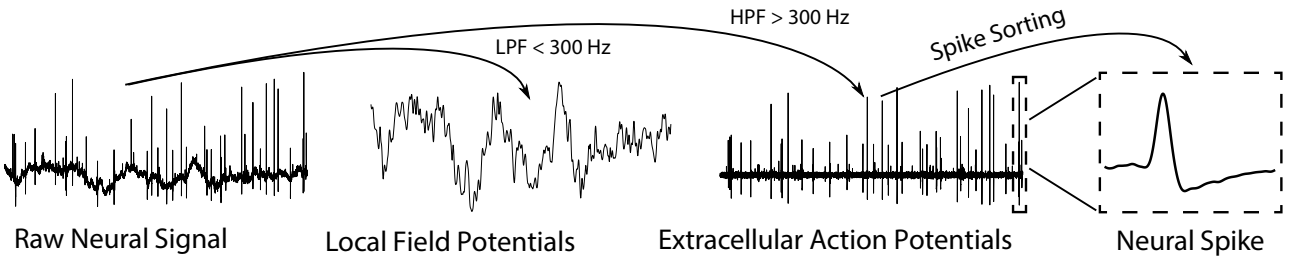

Figure 1.1: Illustration of a raw neural signal recorded by an invasive deep-subdural implant decomposed into LFPs, EAPs and individual spikes.

the EAP signal into spikes from individual neurons relying on the fact that each neuron has slightly different morphology resulting in different shape of the spikes it generates. A variety of algorithms and methods can then be employed to sort the recorded spikes and identify individual firing neurons.

1.2.2 Local Field Potentials

In addition to EAPs from several neurons, a subdural neural recording also contains another signal called the Local Field Potential (LFP) as seen in Figure 1.1. The LFPs, as opposed to EAPs, give us information about general activity in the proximity of the inserted electrode. While there is still some discussion ongoing about the locality of LFPs [30], it is typically accepted that LFPs are representative of activity in the area of a 200-400 µm diameter around the inserted electrode. It is generally believed that the origin of LFPs is difficult to precisely explain [31], it is however accepted that its basis lies in mass activity of neurons surrounding the area, although its nature is more complicated than simply adding EAPs of surrounding neurons together.

EAPs and LFPs are separated in frequency which makes their separation for signal processing purposes simple. While the exact frequency threshold varies depending on used literature, one example [32] quotes LFPs and EAPs occupying frequency ranges of 1-300 Hz and 300 Hz to 3 kHz respectively. Similarly, the amplitudes of the two signals can largely differ. Although [32] states that both LFPs and EAPs can have an amplitude between 10 - 1 mV, it is typically agreed that neural spikes are an order of magnitude (20 dB) smaller than LFP signals. In addition to

valuable signals, a typical signal obtained from a neural electrode will also contain noise from a variety of sources as well electrode offset, both of which will be described in more detail later.

1.2.3 Non-Invasive Recordings

While subdural neural recordings contain a large amount of information allowing the identification of individual neuronal activity, their acquisition requires the insertion of electrodes deep into the neural tissue, thus leading to an invasive surgery. This has led to the research of alternative methods of recording neural activity that are less invasive and offer a compromise between the amount of data that is acquired and the level of their invasiveness. From the methods that are still more invasive, we can mention recent research effort [33] exploring the possibility of recording neuronal activity using optical methods, thus potentially preventing the need to insert an electrode into the tissue directly. This would, however, still require an invasive operation to install the implant.

From the less invasive methods of neural signal recording, we can mention Electrocorticography (ECoG), Electroencephalography (EEG) [34] and Magnetoencephalography (MEG). ECoG involves placing an array of electrodes directly on the exposed tissue of the brain if done subdurally or above the dura if done epidurally and thus still requires an invasive operation needing an opening in the skull. EEG and MEG are, on the other hand, completely non-invasive and study neural signals by observing magnetic fields outside the skull in the case of an MEG or recording electrical signals on the surface of the skull in EEG's case. The simplicity of EEG recordings has led not only to its propagation in medicine but also in consumer devices offering a multitude of functions ranging from entertainment to well-being improvements.

In the case of non-invasive methods, any tissue inserted between the source of the signals, neurons, and the recording electrodes acts as a low-pass filter in both temporal as well as spatial sense and therefore leads to a loss of information. As demonstrated by Figure 1.2, there is therefore a trade-off between how invasive a neural recording method is and how much information can be obtained. This in turn limits the functions that can be performed based on the recorded signals. While it has been successfully demonstrated that EEG can be used

to control a cursor of a computer [22] or even a robotic arm [35] to a limited extent, it is generally accepted that the limited amount of independent channels and filtered nature of the acquired signals prohibits the creation of more advanced prostheses allowing e.g. the control of individual fingers on a robotic hand. To this end, it is necessary to explore invasive brain implants that allow the recording of LFPs and EAPs directly.

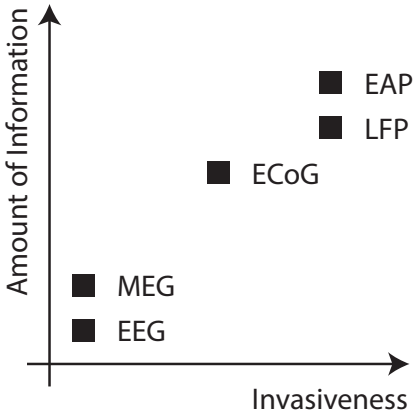

Figure 1.2: Demonstration of a trade-off between the invasiveness and the amount of information obtained from various neural recording methods.

1.3 Recording Neural Implants

As earlier mentioned, the recording of EAP and LFP signals requires the insertion of an electrode or an electrode array into the brain and thus an invasive operation involving creating an opening in the skull of the patient. Most of the historically early recordings [4; 36; 37] were obtained using a set of microwires that would be connected to an external amplifier, in the form of a large immobile table-top instrument, prohibiting any chronic use of such a setup. In addition, the early microwires were hindered by their lack of reproducibility i.e. their susceptibility to production variations and difficulties in their insertion, especially the insertion of their multitude in an array.

Since those early days, the aim of further research and development, therefore, has been to create devices that would allow chronic use by the patient while at the same time being easy to install. This has steered the direction of the development to the creation of fully integrated

implants that would be as small possible, while at the same time facilitating recordings from as many channels as possible without the need to connect external instruments, thus leading to a close link between the increased interest in the field of neural recordings and advances in microelectronics and semiconductor technology, permitting the creation of increasingly small electronic circuits [38]. The origins of those attempts can be traced to the 1970s when K.D. Wise and J.B. Angell presented [39] a multi-electrode array based on a silicon substrate that would eventually be called the Michigan probe, seen in Figure 1.3a. While the electrode array did not include a complete acquisition circuit on its substrate, it did contain a Junction Field Effect Transistor (JFET) pair that would form an amplifier when connected to external circuitry. This has significantly improved the state of the art at the time by reducing the dependence of the recording on the length of the wires as well as reducing its susceptibility to any induced interference.

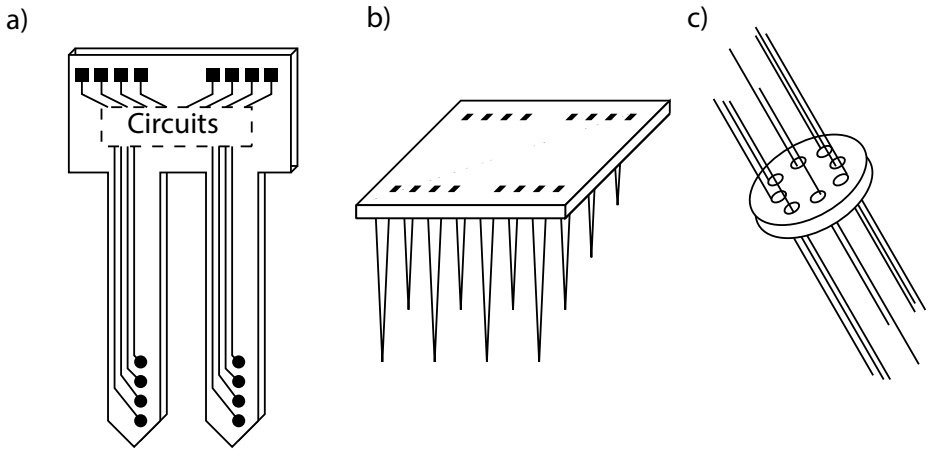

Figure 1.3: Illustration of commonly used recording electrode configurations - a) Michigan probe, b) Utah array, c) Microwire array.

Another version of the probe [40] from the University of Michigan already contained amplifiers on the same substrate as the electrodes themselves.

An alternative method going in a similar direction and equally allowing the creation of an electrode array on a silicon substrate was devised in 1991 at The University of Utah leading to the creation of the Utah array [41]. As opposed to Michigan probes making use of planar electrodes, Utah arrays are composed of a grid of needles stemming from a silicon substrate as seen in Figure 1.3b. Similarly to the way electronic circuits can be integrated in Michigan

probes, there have been neural implant designs integrating electronic circuits with Utah arrays in a single implant [42]. While Michigan probes are better suited for recordings at various depths of the brain using their planar electrodes, Utah arrays can provide better lateral coverage but are limited to a single depth per needle site, although different needles can have various lengths. The commercially available Neuroport Array by Blackrock Microsystems is an example of a Utah array and, according to the manufacturer, is the only FDA-cleared chronic electrode array at the time of writing.

Finally, there have been designs based on arrays of microwires that are typically held together in a grid using a mechanical contraption such as [43]. A challenge in using a grid of microwires often stems from the difficulty in their connection to additional circuitry and the reproduction of such a process in addition to the difficulty of their insertion [44] due to the limited stiffness of the microwires.

1.4 Brain Machine Interfaces

So far we have discussed the possibility of integrating an amplifier in a neural implant to create a minimal neural recording device. This is however typically not sufficient to create a fully functional BMI performing a useful function. As shown in Figure 1.4, the entire BMI is typically composed of a multitude of recording electrodes, a set of amplifiers or complete analogue front-ends, a signal processing unit and finally a controller giving inputs to actuators, i.e. a robotic arm or a computer to facilitate the movement of a cursor.

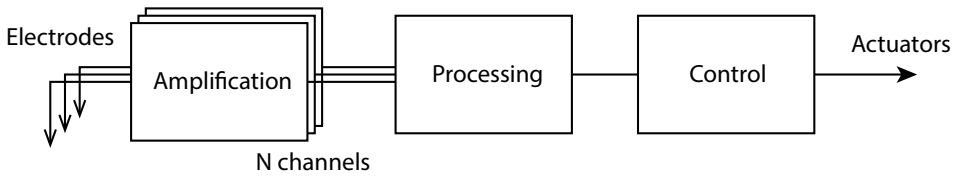

Figure 1.4: Basic blocks typically employed in a functional BMI.

Integrating the analogue front-end in the implant directly is a step in a good direction because it leads to higher fidelity of the recordings but it does not solve the problem of the need to have

a set of wires passing through the skull. To alleviate that, there has been a drive to create fully wireless implants that would not need any physical connection. This results in many challenges starting from the extraction of data from the implant to providing power to it. Some of those concepts were explored from early 2000s such as in the work by M Mojarradi et al. [45] that proposed a heterogeneous combination of an electrode array, a processing integrated circuit and a wireless transceiver bonded to a single block.

1.4.1 Data Transmission

The challenges involved in the facilitation of data transmission begin in the amount of data that has to be transmitted. Although we previously mentioned that a neural spike occupies a bandwidth of up to 3 kHz, many acquisition circuits such as [46; 47] employ a sampling rate of 16 or even 20 kHz. Assuming that the transmission of a simple sample requires 16 bits in the data stream, we arrive at a data rate of 320 kbps. If an array of 96 electrodes, such as the commercially available Neuroport Array, is considered, the data rate rises to 30.7 Mbps, demonstrating how complicated the engineering challenge can become.

It is thus often advantageous to perform a degree of processing in the implant directly. A popular method involves the employment of spike sorting [48] which then limits the transmission to a simple bit sequence identifying a spike when it occurs. Other approaches involve various compression algorithms [49; 50] exploiting some properties of the neural signals and reducing the amount of data that has to be transmitted. Some solutions go a step further [51] and implement a circuit decoding intentions of the user, the output of which can be used to directly control a motorised prosthetic.

1.4.2 Power Delivery

Arguably an even larger challenge stems from the need to provide power to the implant aggravated by the fact that the amount of power available is often the limiting factor for the design of prostheses and one of their main constraints. In addition, even if the engineering

challenge of continuously delivering power is solved, there is still a limit to how much power can be dissipated as the neural tissue is very sensitive to temperature changes, and heating it by more than a fraction of a kelvin can lead to its necrosis. It is usually quoted that this results in a limit to power dissipation of neural implants of 80 mW/cm^2 [52].

As the drive to develop completely wireless implants intensifies, a range of different approaches to the delivery of their power has been investigated, starting from the use of batteries. Although this might not seem a very suitable option, there is a precedent in their use for chronically implanted deep brain stimulators [53], quoting a typical lifetime of 3-5 years for single-use implants and more than 10 years for implants using rechargeable batteries. While technically feasible and used, the concept of implanting batteries inside the cranial cavity, however, still presents a large variety of issues as even rechargeable batteries have limited longevity and most kinds of chemical energy storage will involve the use of hazardous, biologically incompatible, materials.

Over the recent years many alternatives to using batteries have, therefore, been proposed, instead relying on wireless power delivery. The typically used methods [54] can be divided into three categories: ultrasound using a piezoelectric receiver, electromagnetic induction using a set of coils or light converted using photovoltaic cells. At the same time there have been initial attempts [55] to use biological fuel cells to power BMIs. Those would be connected to the patients's blood stream and generate electrical power from glucose contained in blood. While arguably still far from being practical with currently reported harvested steady-state power of 3.4 $\mu W/cm^2$ [54], this is a very promising approach for the future.

All other methods relying on conventional power delivery typically rely on a combination of a headstage mounted on the patient's head and subdural implants as seen in Figure 1.5. The headstage can be used both for the storage of energy, which might be in the form of easily replaceable batteries, as well as for performing of additional processing on the acquired signal outside of the constraints presented by implanted devices. As there is an inherent trade-off between how directional the link between the two system parts is and how efficient the link is, there is a need for accurate alignment between the headstage and the implant which can often

be difficult to achieve given the amount of natural movement of the tissue causing displacement between individual parts of the system.

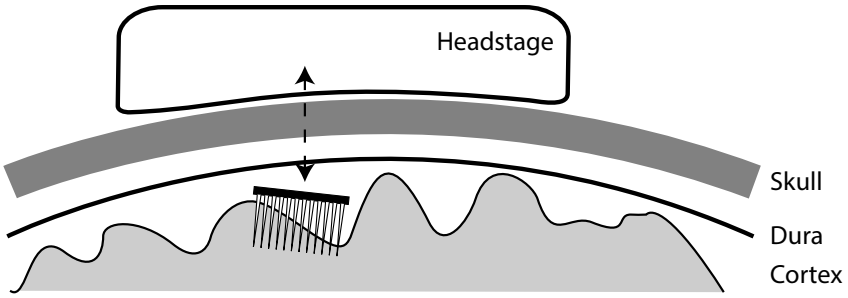

Figure 1.5: Illustration of head cross-section with an implanted Utah array wirelessly coupled to a headstage.

1.4.3 Chronicity and Failures

Although successful brain machine interfaces have already been constructed and demonstrated such as in the case [56] of a tetraplegic patient who was able to control a robotic arm using her thoughts, the current state-of-the-art BMIs suffer from limited chronicity and the impossibility of their deployment for everyday use. The BMI application presented in [56] involved the use of a commercially available Utah array connected by wires to a desktop computer used to decode the signals and control a robotic arm, a setup that is rather distant from a practical application. Nevertheless, the experiment demonstrated the feasibility of making a BMI that could help tetraplegic patients control robotic arms.

To understand the challenges faced by long-term chronic applications, we have to look at studies that have been conducted over extended periods of time. Some of the earlier examples can be found in work by P.J. Rousche and R.A. Normann [57] from 1998 who implanted 10 cats with Utah arrays and observed that after a period of 6 months, 60% of electrodes still showed some activity. At the same time the study revealed a range of issues that remain some of the biggest challenges of chronic implantations until today. The constant movement of the implant due to it being anchored in the soft brain tissue, has led to general instability of the recordings and inability to observe the same neuron for more than a few weeks. In addition, once the electrodes were explanted, most of them were covered in scar tissue grown as a reaction of the

organism to a foreign body. This phenomenon was explored in more detail by V. S. Polikov et al. [58], who have identified it as one of the most prominent barriers to the creation of truly chronic implants and it is generally believed that factors such as electrode shape and material contribute to the extent of the response.

A study by D. H. Szarowski et al. [59] has examined the effect of electrode geometry on the foreign body response and failed to show any significant relationship between the two. The authors however argue that the response can be divided into two separate processes - early and prolonged reactions, where the earlier is triggered by the immediate damage to the tissue caused by the insertion and is therefore dependent on the shape of the electrode, and the latter that is more affected by prolonged interactions and therefore more related to the material and general bio-compatibility of the electrode.

To improve the bio-compatibility of the implant, various methods have been explored, such as the incorporation of bioactive molecules to prevent growth of scar tissue. An interesting concept can be seen in work of D. R. Kipke et al. [60] who have developed a Michigan-style electrode incorporating a small cavity in the shank for the deployment of bioactive compounds such as drugs suppressing the foreign body response. A more recent review by J. W. Salatino et al. [61] mentions some successes of those methods in addition to stressing the importance of the use of materials that have similar mechanical properties to the brain tissue itself. It is argued that using softer materials results in smaller reaction but at the same time presents a challenge with insertion of the implant into the tissue. Importantly, it is noted that smaller feature sizes are preferred and keeping the volume of the implant to a minimum in general helps to reduce any adverse response of the organism.

In general, there is a limited amount of studies with implants left in the host for more than a couple of years. An example of such is a study by J. C. Barresse et al. [62] who have implanted 27 non-human primates with 78 multi-electrode arrays (MEA) and observed their performance over a period of 5.75 years. This provides us with a unique insight to typical reasons for electrode failures as well as expected lifetime of electrodes. As seen in Figure 1.6, the amount of functional implants approximately follows exponential decay with a majority of

devices failing within the first year from implantation and the last MEA failing after 6 years of operation. It is noted that the main reason of failures were mechanical issues (30 MEAs) followed by biological causes (15 MEAs). While the main aim of this study was to observe the performance in recording of EAPs, it was observed that the LFP signal was still present for a longer period after EAPs were no longer observable from a particular recording electrode.

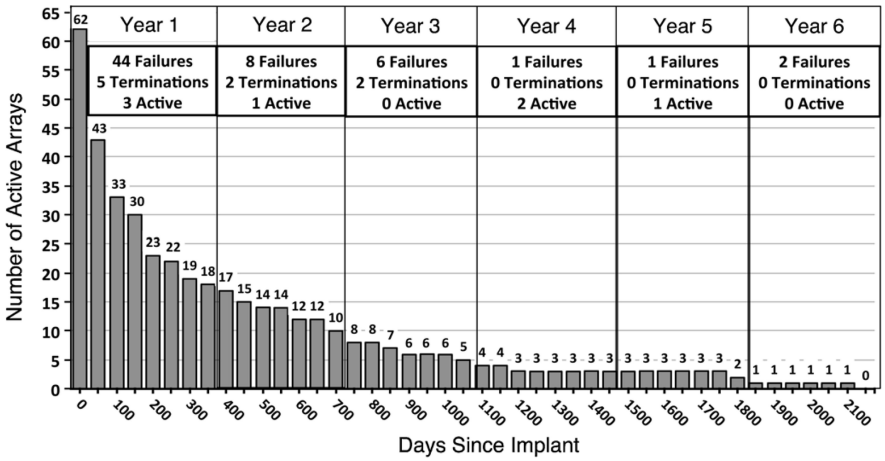

Figure 1.6: Number of operational multi-electrode arrays (MEA) after implantation in a study by J. C. Barresse et al. [62] (78 Utah-type MEAs implanted in non-human primates over a period of 6 years). Figure reproduced from [62].

To our best knowledge, the longest chronic recording achieved to date was 9 years long, done by N. Hatsopoulos [63] in non-human primates using a commercially available Utah array. Those reports of years-long recordings are however more a product of statistic deviation rather than a common occurrence.

Although the Utah array has to a large extent become the standard choice of MEA both for research and clinical practice, and is the only commercially produced FDA-cleared MEA, there is a multitude of arguments saying that they might not be the optimal solution for the next generation of recording implants. The study of J. C. Barrese et al. [62], having shown a median time to failure of just 182 days (mean of 387 days), can as well be considered one of them. It is, however, in general difficult to judge the chronicity of various types of MEAs due to a small number of studies that have been conducted over the period of several years.

Another study, conducted by R. J. Vetter [64] who implanted rodents with 12 multi-site Michigan probes, showed 11 of 12 probes still operational after a period of 127 days, also illustrating

the potential of Michigan probes for chronic implantation. Similarly, some understanding of the potential of microwire-based MEAs can be found in studies of J. Kruger et al. [65] and M. A. Nicolelis et al. [66] who have both documented studies that observed microwire implants in non-human primates for extended periods of time.

M. A. Nicolelis et al. [66] have implanted three rhesus monkeys with a multitude of stainless, teflon-coated microwire implants in various cortical areas. In one monkey, the implant was left implanted for an extended period of 18 months after which it was still possible to identify EAPs of 58 individual neurons from 34 microwires (out of 96 implanted). The authors also note that no significant differences were observed in data collected immediately after surgery and after an additional period of 30 days.

J. Kruger et al. [65] have implanted one monkey with a 64-channel Ni-Cr-Al microwire array and observed the implant for a period of 7 years. A recording was then obtained in periodic intervals and the number of observe-able neurons was recorded as seen in Figure 1.7. This shows that there is no immediately apparent decrease in performance over the length of the study. The authors note that on some occasions the number of observe-able neurons increased and overall there was only a limited amount of amplitude decrease over time that would normally be associated with the growth of scar tissue and the foreign body response.

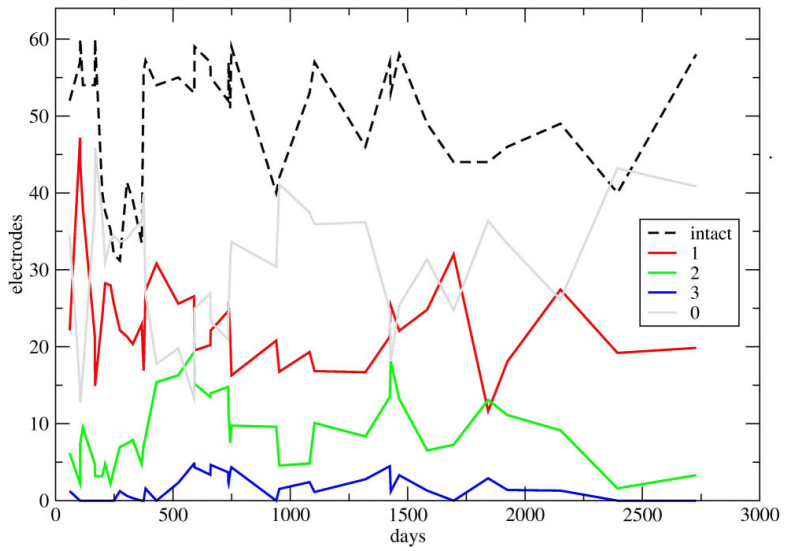

Figure 1.7: Number of observe-able neurons in a study by J. Kruger et al. [65] over period of 7 years using a 64-channel Ni-Cr-Al microwire array implanted in a monkey. Dashed line indicates the number of technically intact channels. Figure reproduced from [65].

While there is only a limited amount of studies conducted and a limited amount of data available to make a judgement, the results of those two studies examining microwire arrays [65; 66] as opposed to results obtained by J. C. Barresse et al. and R. J. Vetter et al. using Utah arrays and Michigan probes respectively, indicate that microwires might be more successful in performing chronic recordings. It is also worth noting that although both the microwire studies were only conducted with a limited amount of implanted animals, the implants did not fail completely in either of those studies. This is in contrast to what was reported by J. C. Barresse et al. [62] where all implants failed within a period of 6 years. The success of microwires can to some extent be connected with the earlier identified need to create implants that have mechanical properties similar to the host tissue. This is further supported by a study of Z. J. Du et al. [67] who have implanted stiff tungsten electrodes and ultrasoft polymer based electrodes into the cortex of rats for a period of 8 weeks. It was observed that the damage to the tissue was significantly smaller in the case of ultrasoft electrodes than when tungsten electrodes were used. It was also noted that the use of ultrasoft electrodes led to reduced foreign body response as evidenced by reduced glial cell growth.

The use of soft materials is difficult to achieve with rigid silicon-based structures such as Michigan probes or Utah arrays but significantly simpler with flexible metallic or polymer-based microwires. It can be argued that even microwire arrays made of stiff metals such as tungsten will be less rigid than a silicon-based structure. Those, on the other hand, achieve better manufacturing reproducibility and simplicity of implantation which led to their popularity and preferred usage but there is evidence to suggest that microwire arrays lead to better performance when used for chronic recordings.

1.4.4 Local Field Potentials

Most of the studies presented so far have focused on obtaining recordings of EAPs and were looking at the amount of individually identifiable neurons as a measure of success. The study of J. C. Barresse et al. [62] however suggested that even after the EAP signal has disappeared in a particular channel due to extensive scar tissue growth, it is often still possible to record local

field potentials (LFPs). Those findings have further been noted by B. Pesaran et al. [68] and R. R. Harrison et al. [69] and can be explained by the fact that the glial cells that form the scar tissue result in the creation of a low-pass filter between the electrode and surrounding neurons, blocking the higher-frequency EAP but still allowing the lower-frequency LFPs to pass. If it is possible to obtain more chronic LFP recordings, a question then arises, whether it is possible to make brain machine interfaces solely reliant on LFPs and therefore less dependent on successful recording of high-frequency signals.

The relationship between local field potentials and spiking rates have been a subject to some debate in the community but it is generally believed that there is a close relationship between the two. To this end, B. Pesaran et al. [68] have observed neural activity in the cortex of macaque monkeys and observed correlations between certain LFP bands and spiking rates of individual neurons. A more recent work by A. Jackson and T. M. Hall [70] describes a method of extracting features from local field potentials, including features showing a high degree of correlation with unit spiking rates. In addition, there are other publications such as [71] by N. Ahmadi et al. that demonstrate algorithms for derivation of motor intentions from LFPs.

A more practical demonstration of the use of LFPs in BMIs can be seen in work by S. D. Stavisky et al. [72] who have implemented a practical BMI allowing a rhesus monkey implanted with a 96-channel Utah array to control a robotic arm. The decoder of the BMI was implemented in the form of a Kalman filter with both spiking activity and local field potentials as its inputs. It was then shown that a 99% success rate in conducting a randomised target task can be achieved even if all spiking input is removed from the filter and the BMI purely relies on LFP input.

More examples of work done in this field and similar results can be found in a study by J. Zhuang et al. [73] who have identified that high frequency LFP bands (100 Hz) in particular contain a large amount of information about motor intent. R. D. Flint et al. [74] went a bit further and suggested that "local field potentials can decode velocity with nearly the same accuracy as spikes, and likely with greater longevity", equally pointing out that higher frequency LFP bands are of more value in decoding motor intent.

BMIs based purely on recording of LFPs, therefore, seem to be a viable option and an alternative

to BMIs decoding neural spikes that promise the potential of extended chronicity. Additional advantage lies in their smaller bandwidth and thus more relaxed constraints placed on the design of the acquisition electronics as well as data rates needed for transmission of the acquired information. This in turn allows relaxation of the power budget of the implant.

1.4.5 Next Generation of Neural Interfaces

Some of the findings presented above related to previous generations of implants have led several research groups to work on the next generation of neural implants that would alleviate some of the issues identified in previous generations. This is especially the case when it comes to improvements leading to chronicity of implants and their practicality for everyday deployments. This can be summarised as a need to alleviate the necessity to use physical wires passing through patient's skull and novel methods that would allow the suppression of the foreign body response.

For a long time, there has been a drive to create neural implants with as many recording channels as possible. This is however not in line with our knowledge about the effects of the foreign body response that seems to be made worse by introductions of large objects. To this end, there is a new paradigm emerging and being explored.

Pioneered by D. Seo et al. [75], the next generation approach suggests that rather than creating one large implant, it might be better to create implants of minimal size that would each only record a small amount of channels but would be deployed in large numbers to form a mesh of distributed implanted devices. An example of such is a concept of D. Seo et al. [75] termed Neural Dust. As seen in Figure 1.8a, this would be in the form of a mm-sized implant coated in polymer encapsulation and therefore hermetically sealed. The power would be delivered using an ultrasonic link and recovered using a piezo cell. The implant would contain a couple of surface electrodes and a polymer tail allowing for recordings from more distant sites.

An alternative concept presented by W.Biederman et al. [76] and seen in Figure 1.8b shows an inductively powered sub-mm-sized (0.125 mm^2) implant formed of a CMOS (Complementary Metal-Oxide-Semiconductor) inductor-on-chip bonded to a set of silicon electrodes. While this

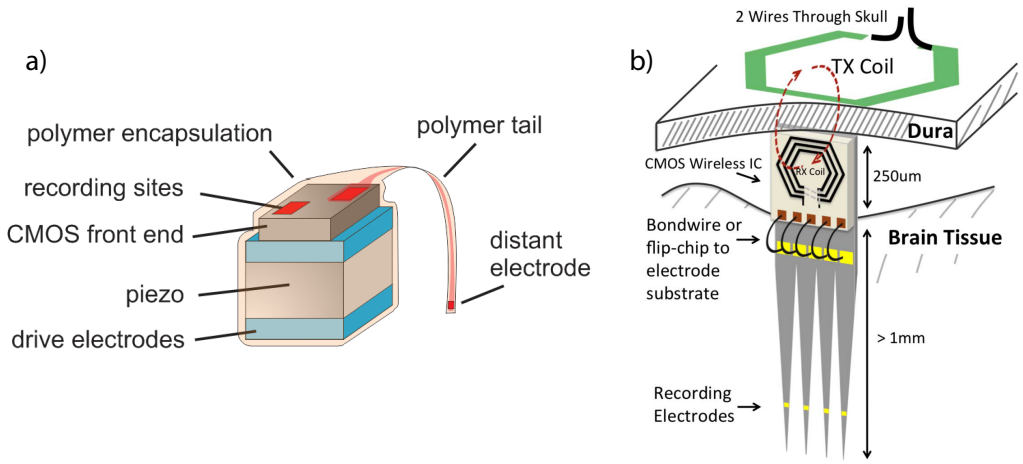

Figure 1.8: Illustrations of distributed recording implants, a) Concept of Ultrasonically powered neural implant "Neural Dust" proposed by Seo et al. [75]; Figure from [75]. b) Inductively powered distributed implant proposed by W. Biederman et al. [76]; Figure from [76].

concept only anticipates wireless connection through the dura and wires passing through the skull, it demonstrated the concept and the possibilities.

It is also worth noting that a similar concept has been explored for stimulating devices, such as "Stimdust" presented in [77] relying on ultrasonic power transfer.

1.4.6 Project ENGINI

The most recent developments and trends in the field of neural recordings have led to the creation of Project ENGINI (Empowering Next Generation Implantable Neural Interfaces) at Imperial College London. The project is a collaboration of several researchers and PhD students who are a part of the NGNI (Next Generation Neural Interfaces) research group with the aim to develop the next generation of recording neural implants that would tackle the most prominent issues encountered by the current generations of neural implants and would pave a way to achieving a truly chronic and practical solution.

ENGINI, the artist's impression of which can be seen in Figure 1.9 aims to go in the direction of creating a distributed network of implants, each only recording a small amount of channels, similarly to the concepts presented in subsection 1.4.5. Each implant takes the shape of a pin that is hermetically sealed to ensure its biological compatibility and inertness. The head of the

pin contains all electronic circuits in the form of a CMOS integrated circuit handling power recovery, signal acquisition, signal conditioning and signal transmission.

The network of implants is powered using a wireless inductive link that, as seen in Figure 1.9 is formed of a headstage coupled to a flexible inductor array consisting of a large inductor placed above the skull, wires passing through the skull and a set of smaller inductors coupled to the implants forming a resonator also referred to as "electromagnetic lens" [78] allowing for more efficient power transfer between the head stage and the implants. The inductive link is at the same time used for the transmission of the acquired data in the form of back-scattering induced by load shift keying (LSK). The implant itself uses an integrated inductor inside the hermetic seal formed either by micromachining or fabricated directly on a silicon substrate alongside other electronic circuits. The link operates at a frequency of 433 MHz which is a free industrial, scientific and medical (ISM) band alleviating regulatory issues.

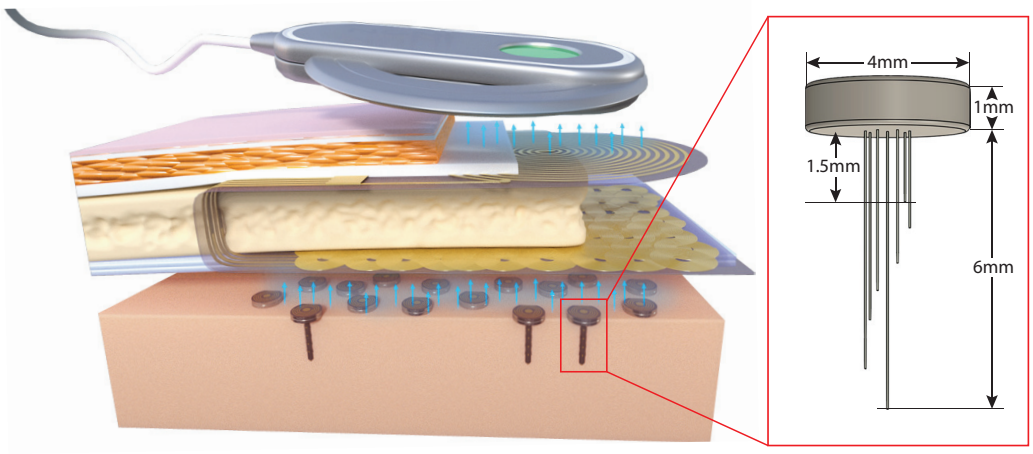

Figure 1.9: Illustration of the concept of ENGINI, a distributed neural implant network; Figure reproduced from [79].

Although this configuration still requires wires passing through the skull, two wireless links are formed through the skin and the dura that can remain chronically unpunctured and therefore prevent infections. The implants are freely floating and not physically connected to any part of the system above the dura, thus reducing mechanical stress on the tissue and hence preventing its damage as well as reducing the foreign body response.

In line with the evidence presented in subsection 1.4.3, the ENGINI implant makes use of an array of 8 microwires that can be cut to different lengths to facilitate recordings from various

cortical depths, which has been suggested [70] to be beneficial in obtaining useful information from local field potentials. Although the initial aim of the project was to create implants purely recording local field potentials to benefit from their simpler acquisition and extended chronicity, later versions have shifted to more conventional recordings of both EAP and LFP.

The implants are designed with an aim to be as autonomous and simple as possible, to which end, there is no downlink present in the system and the implants are only able to transmit information to the headstage. Code-Division Multiple Access (CDMA) has been explored [78] as a method of communication allowing multiple implants transmit information at the same time. CDMA is particularly suitable for this setting because of the relative simplicity of construction of CDMA modulators, placing much of the complexity needed to decode the signals to the receiver that is located in the headstage and therefore subject to significantly less constrained resources.

While the concept leads to a creation of an implant that is as simple as possible, there is a number of research questions spanning several disciplines of engineering that have to be answered, some of which are:

- What microfabrication techniques can be used to reproducibly manufacture such an implant and ensure it is hermetically sealed?
- How can it be verified that the hermetic seal has not been broken and internal circuits not compromised?
- Is the inductively coupled wireless power transfer feasible and how can it be designed for maximal efficiency?
- There are several challenges with the use of recording microwires as opposed to silicon probes. This includes the difficulty of implantation and connection to the rest of the system while ensuring hermeticity. How is the implant going to be implanted in a way that prevents buckling of the wires? How are the wires going to be connected to the rest of the system?

- What modulation method can be used such that the needed amount of information can be transferred from all implants?

- If CDMA is used, each implant needs to have a unique code to allow for separation of channels. How can we ensure the generation of codes suitable for CDMA modulation that are unique for each implant while keeping the implants autonomous and without introducing a downlink?

- Which electrode material and geometry should be used to ensure the best possible performance of the recording in terms of both quality of the obtained signal as well as ensuring maximal chronicity?

- How can an analogue front-end be designed such that its power consumption is minimised while delivering the required performance? This design is going to face numerous challenges such as dealing with the characteristics of the electrodes, the need for a large dynamic range while at the same time keeping to a stringent power budget governed both by the limited capacity of the inductive power link as well as limits on heat dissipation.

- Since the entire system is wirelessly powered and its power is recovered from a high-frequency carrier, it can be difficult to obtain a stable voltage reference and therefore operate an analogue front-end capable of recording signals on sub-µV levels. How can such a reference circuit be designed in the absence of space and resource for utilisation of large capacitors, typically employed in such reference circuits?

1.5 Objectives

The scope of this PhD work is to try to answer some of the questions related to the design of circuits and other aspect of the design of electronics, especially focused on the last three points and questions raised above. In more detail, we would like to focus on the following areas and answer some of the following questions:

- **Recording Electrodes** - The recording electrodes used for the creation of neural recordings have historically been researched separately from the circuits employed in the recording front-ends both from the point of view of chemistry as well as biological compatibility and the effects of their insertion into tissue. The quality of the obtained recording and the design of the analogue front-end is however strongly influenced by the electrical properties of the electrode such as its impedance and amount of noise generated. The two are therefore closely related and the design of one affects the other. The aim of this work is, therefore, to explore basic properties of electrodes and the relationships between their geometric and electrical properties that will help guide design of an analogue front-end.

- **Neural Recording Front-Ends** - As discussed earlier, recording neural implants have been a reality for several decades during which the electronic circuits employed have seen large amounts of development. At the same time there is a significant amount of challenges that a successful neural recording front-end has to overcome, meaning there is still a lot of area for improvement. The challenges begin with having to facilitate a large dynamic range large able to accommodate both EAP and LFP signals that often exhibit vastly different amplitudes in addition to having to reject large Direct Current (DC) offsets. Moreover, all this has to be achieved with extremely constrained resourced both in terms of available power as well as area. Exploring previously employed topologies and methods, the aim of this work is to investigate novel methods of acquiring neural signals and introduce practical implementations. The methods investigated include continuous time acquisition and sigma-delta modulation.

- **Reference Circuits** - Wirelessly powered neural implants typically have to recover power for their operation from some form of alternating physical quantity, be it electromagnetic waves or mechanical vibration in the case of ultrasonic power transmission. This means that the supply voltage has to be rectified and regulated to allow powering of most useful circuitry and act as a reference. Most typically used regulator topologies rely on large blocking capacitors (on the order of µF) at the output, a solution that is not practical in the resource-constrained world of neural implants, especially if the entire circuit is to be contained on a single CMOS chip. We would therefore like to explore solutions that

bypass those constraints and implement a practical circuit.

In more practical terms, the objectives of this work in each of the above-mentioned areas include:

- To investigate and gain understanding of electrode materials, geometry and their effect on the quality of neural recordings.
- To investigate the feasibility of using Niobium as a novel material for the manufacturing of neural recording electrodes.
- To investigate the feasibility of using Continuous Time (CT) sampling as an alternative sampling scheme for the acquisition of neural signals. This is to be done by designing a CT Analogue-to-Digital Converter (CT-ADC), characterising it and analysing its operation in light of neural signal acquisition.
- To investigate possible methods of flicker noise removal that would be compatible with Continuous Time sampling without leading to a loss of some its advantages. This is to be done by proposing a new flicker noise removal scheme, designing and measuring a circuit demonstrating its operation.
- To design, manufacture and measure a reference circuit that could be used in a wirelessly powered neural implant to provide a stable reference voltage and power supply.
- To investigate the feasibility of using $\Sigma\Delta$ modulation for the design of neural implant analogue front-ends (AFEs). This is to be done by designing a recording AFE based on $\Sigma\Delta$ modulation, manufacturing it and demonstrating the suitability of the topology for this problem.

The design objective of those circuits is to advance the possibilities of neural interfaces, paving a way to their next generation. One of the greatest challenges remains achieving as small power consumption as possible. While there is an absolute limit of thermal dissipation of 80 mW/cm^2 [52], the power consumption is often more limited by the amount of power that

can be transferred to the circuit by the available link. The smaller the power consumption and smaller the area, the more recording channels can be integrated in a single implant. Each recording channel still has to be able to digitise a wide range of signals, including EAPs of smaller than 10 µV magnitude and LFPs of mV magnitude while rejecting DC offsets of up to 100 mV, resulting in requirements for a large dynamic range and fidelity of the acquired signal.

To allow for comparison of the designed circuits with the state-of-the-art found in literature, a summary of neural recording AFE design of other authors can be found in Table 1.1. This shows that there is often a trade-off between the achieved power consumption and area as mentioned in [80]. Designs with the lowest power consumption, such as [81] require less than 1 µW to operate while the most compact designs occupy less than 0.02 mm^2 of silicon area. Acquisition bandwidth of 10 kHz is almost universally adopted and the input referred rms noise of AFEs is typically between 4-8 µVrms. Most designs achieve SNDR between 40-60 dB.

	[32]	[82]	[83]	[84]	[80]	[81]
Description	LFP+EAP AFE	LFP+EAP Array	LFP+EAP Array	LFP+EAP Array	LFP+EAP Array	LFP+EAP Array
Year	2012	2011	2014	2021	2017	2013
Tech	65 nm	0.35 µm	0.35 µm	180 nm	180 nm	180 nm
Power	5 µW	13.5 mW	75 mW	13.5 mW	390 µW	73 µW
Area	0.013 mm^2	12.775 mm^2	8.085 mm^2	4.118 mm^2	8.93 mm^2	25 mm^2
N Ch	1	256	1024 (26,400 mux)	256	128	100
Power/Ch	5 µW	52.7 µW	73.2 µW	52.7 µW	3.05 µW	0.73 µW
Area/Ch	0.013 mm^2	0.035 mm^2	0.012 mm^2	0.016 mm^2	0.069 mm^2	0.25 mm^2
SNDR	45 dB	32.18 dB	59 dB	55.6 dB	67.4 dB	51.5 dB
IR Noise (rms)	4.9 µV	7.99 µV	2.4 µV	6.32 µV	3.32 µV	3.2 µV
BW	10 kHz	10 kHz	10 kHz	10 kHz	10.9 kHz	10 kHz

Table 1.1: Summary of Performance of State-of-The-Art Neural Interfaces in Literature.

1.6 Thesis Outline

Having broadly introduced the background of neural implants and a brief history leading to the current state of the art, upcoming chapters are going to introduce some of the aspects and issues mentioned above in more detail and describe original work that took place to expand knowledge in those areas. The rest of this work is going to be covered in the following chapters:

- **Chapter 2: Overview of Analogue Front-Ends and Electrodes for Neural Implants**

This chapter is going to introduce the reader to the problematic of design of analogue front-ends in recording neural implants, giving a scope to the issues faced in terms of constraints and required performance. To put those into perspective, an electrical model describing the behaviour of a neural recording electrode is going to be presented alongside experimental work identifying a possible novel material for creation of microwires aimed at recordings of LFPs. A review of currently used analogue front-end topologies is then going to be presented.

- **Chapter 3: Continuous Time Acquisition of Neural Signals**

  Continuous time (CT) acquisition, also called level-crossing or event-driven is an alternative to the more commonly used discrete time (DT) sampling. This chapter is going to introduce the basic principles of this method, noting the differences against conventional techniques demonstrating why this method is particularly suitable for the acquisition of neural and other biological signals. Current literature often notes that continuous time acquisition intrinsically ensures that aliasing is prevented. A counter-example disproving this is presented and a novel theorem of a sufficient condition to prevent aliasing in continuous time acquisition is presented. Finally, a practical implementation of a continuous time analogue-to-digital converter (ADC) is presented alongside measured results.

- **Chapter 4: Clockless Chopping Scheme for CT Acquisition of Neural Signals**

  Flicker noise is often a limiting factor in circuits used for acquisition of low-frequency signals. Conventional DT ADCs typically employ techniques such as auto-zeroing or chopping to alleviate this issue. Such an approach however requires the employment of a high frequency clock to modulate the input signal. One of the advantages of CT signal acquisition is the absence of clock leading to signal-dependent power consumption. While the use of clocked chopping in those circuits is possible, it introduces a source of signal-independent power consumption which is indesirable. A novel method permitting the use of chopping in CT ADCs without the need to introduce a fixed-frequency clock signal is presented alongside the theory of its operation. This is followed by a practical implementation in a CMOS circuit improving on the circuit presented in Chapter 3.

- **Chapter 5: Reference Circuits and Voltage Regulators for Neural Implants**

  As noted above, the design of reference circuits and voltage regulators for neural interfaces presents a unique challenge due to the constraints presented by the unique application. This chapter explores some of those constraints in more details in light of typically used techniques. Methods often employed to overcome those issues are presented and a practical implementation of a resource-limited combined CMOS reference circuit and a regulator is presented alongside measured results.

- **Chapter 6: Sigma-Delta Modulator for DC-Coupled Neural Interfaces**

  Sigma-Delta modulators have recently become an emerging technology used to design analogue front-ends in neural interfaces. The basis of their operation is presented followed by a design of a Sigma-Delta modulator intrinsically solving some of the challenges faced by neural recording front-ends, such as rejection with comparatively large DC offsets and low-frequency signals. Measured results of the designed circuit are presented.

- **Chapter 7: Conclusions**

  Conclusion of the thesis is presented and final evaluation of the presented work is made alongside thoughts on possible future expansion of the presented findings.

Chapter 2

Overview of Analogue Front-Ends and Electrodes for Neural Implants

The results presented in this chapter considering the use of niobium as a material for the creation of recording electrodes have been previously published in [85]. While the paper presents the findings alongside work of other authors, the results on the use of niobium have been my original contribution.

Although there are emerging alternative modalities of obtaining neural activity recordings, such as methods relying on optical [33] or magnetic (MEG) response of active neurons, contact-based methods based on the direct measurement of electrical signals are still the most commonly used. As described in the previous chapter, the measurement of either EAP or LFP signals requires the insertion of electrodes into the tissue of the brain and their connection to an analogue front-end to facilitate signal acquisition. Having briefly explored some of the commonly used configurations such as the Utah and Michigan arrays as well as microwire-based solutions in the previous chapter, the aim of this chapter is to link the mechanical properties of electrodes to their electrical properties to help us understand the constraints placed on the design of analogue front-ends (AFE). This knowledge will additionally allow us to gain an insight into what materials and electrode geometries are most suitable for maximising the quality of obtained neural recordings.

2.1 Electrode Model

In order to understand how to interface an electrode to an analogue front-end, we need to gain a deeper understanding of its impedance in relation to its geometric properties and how it affects the quality of the obtained recording as quantified by the Signal to Noise Ratio (SNR), typically denoted as:

$$SNR = \frac{P_S}{P_N} \tag{2.1}$$

where P_S is the power of the neural signal and P_N the power of noise in the acquired signal. This assumes that all noise is purely additive and omits any harmonic distortion as we will for the purpose of the presented analysis assume that the electrode's behaviour is purely linear. Although, as shown later, there are limitations to this assumption in general, the small magnitude of typical neural signals justifies it.

To aid us in analysing the signal path and sources of noise, we can refer to Figure 2.1 showing a simplified neural acquisition chain. The potentials resulting from electrochemical reactions in neurons such as EAPs and LFPs are marked v_s. These pass through the intracranial space filled with cerebrospinal fluid (CSF) [86], an electrolyte acting as a conductor between the neuron and the inserted electrode, the impedance of which is denoted Z_{ey}. When an electrode is inserted into tissue, an interface between the material of the electrode and the CSF is formed. In a typical microwire-based grid made of metal, we can refer to this as a metal-electrolyte or an electrode-electrolyte interface and denote its impedance Z_{el} The signal then appears at the input of an AFE of impedance Z_{in} leading to its attenuation by factor A_{in}:

$$A_{in}(\omega) = \frac{Z_{in}(\omega)}{Z_{in}(\omega) + Z_{ey}(\omega) + Z_{el}(\omega)} \tag{2.2}$$

It should be noted that the involved impedances are complex and frequency variable and therefore the signal is subject to attenuation and phase shift that varies with frequency.

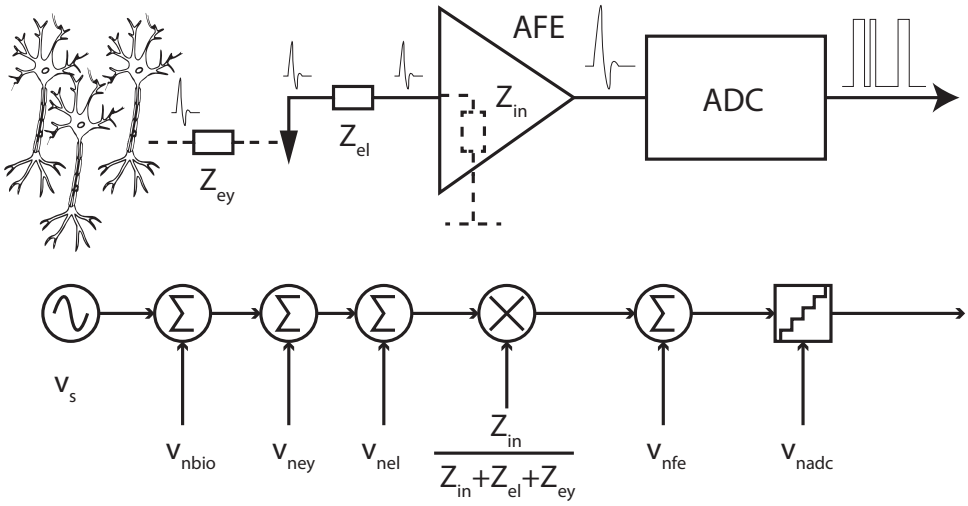

Figure 2.1: Top: Diagram of a typical neural recording acquisition chain consisting of electrolyte impedance Z_{ey}, electrode impedance Z_{el}, analogue front end (AFE) of input impedance Z_{in} and an ADC. Bottom: Signal flow diagram representing neural signal v_s and sources of noise and attenuation along the chain.

In addition to the attenuation of the signal, the PSD is further affected by noise from several sources added to the signal in the acquisition chain starting with biological noise generated inside the neuron itself. This is denoted v_{nbio} in Figure 2.1 and originates from the processes taking place inside the neuronal cell such as the random opening of ion channels and the randomness of ongoing diffusion [87]. Similarly to many other biological processes, this typically follows a 1/f decay in its power spectral density (PSD) [88], resulting in its classification as pink noise.

The signal then passes through electrolyte of impedance Z_{ey} which leads to addition of thermal noise of PSD of:

$$\overline{v_{ney}^2} = 4kT \times \Re(Z_{ey}) \tag{2.3}$$

While it is difficult to obtain a precise expression for Z_{ey} due to a large variety of possible geometries and configurations of the cell and electrode positions, we can obtain an estimate Z_{ey}^{cyl} assuming the majority of conduction takes place in a cylinder of top face area A_g and length d_{ec} where A_g and d_{ec} respectively represent the geometric area of the electrode and

distance between the cell and the electrode. Denoting the electrolyte conductance ρ_{ey}, we can then express Z_{ey}^{cyl}:

$$Z_{ey}^{cyl} = \frac{d_{ec}}{\rho_{ey} A_g} \tag{2.4}$$

In practice, it is however often assumed that the counter-electrode is infinitely large and the signal spreads towards it, giving rise to the notion of spreading resistance [89].

Similarly, the noise added by the electrode-electrolyte interface of impedance Z_{el} is thermal in nature and its PSD can be denoted:

$$\overline{v_{nel}^2} = 4kT \times \Re(Z_{el}) \tag{2.5}$$

The signal is then further corrupted by noise v_{nfe} added by the analogue front-end and quantisation noise v_{nadc} added in the ADC that are going to be addressed in more detail later when we explore the problematics of the design of analogue front-ends. Before doing that, let us, however, consider the electrode-electrolyte interface in more detail, and explore the physical processes facilitating its conduction and how those can be translated into an equivalent electrical circuit.

2.1.1 Capacitive Conduction

Electrical conduction across the electrode-electrolyte interface takes place due to two different processes - capacitive conduction and reduction-oxidation based Faradaic currents that are respectively represented by a capacitance and resistance in an equivalent model seen in Figure 2.2. The capacitive conduction forming a high-frequency signal path, is a result of a layer of solvated ions appearing at the electrode interface when submerged into an electrolyte, forming a dielectric layer [89]. Since both the metal electrode and electrolyte on either side of the dielectric are conductors, double-layer capacitance C_{dl} is formed. This is typically described as

a series combination of Helmholtz and Gouy-Chapman capacitances C_H and C_{GC} [90].

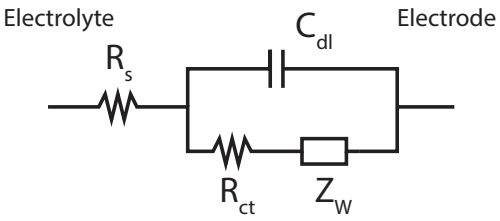

Figure 2.2: Small signal equivalent schematic of an electrode-electrolyte interface consisting of spreading resistance R_s, double-layer capacitance C_{dl}, charge transfer resistance R_{ct} and Warburg impedance Z_w. Model based on [91; 92]

As described in [90], the Helmhotz capacitance C_H is based on a model assuming that there is a finite-width layer of solvated ions of no charge termed the Inner Helmholtz Plane. This is one of the oldest models of the interface and typically overestimates its capacitance. This is corrected by the addition of the Gouy-Chapman capacitance in series reflecting the fact that the density of solvated ions gradually decreases away from the electrode due to diffusion, forming the Outer Helmhotz Plane.

It is worth noting that there are more accurate and complex models in literature such as the Stern's model [90]. The combination of Helmholtz and Gouy-Chapman capacitances is however sufficient for the needs of an elementary analysis. As noted by [89], both C_H and C_{GC} are approximately of the same magnitude, $C_H \approx C_{GC} \approx 1.4$ pF/µm^2 and therefore $C_{dl} \approx 0.7$ pF/µm^2.

The resulting capacitance per area is very large when compared to what is typically seen in manufactured capacitors. This is caused by the large dielectric constant of the layer of solvated ions, reported close to 20 [90] or sometimes as high as 78 [89]. This can be compared to a dielectric constant of 25 reported [93] for tantalum pentoxide (TnO_5) typically used for production of capacitors. The large dielectric constant coupled with the small thickness of the solvated ion layer (on the order of 0.5 nm [94]) gives us a sense of how large the capacitance formed on the interface is.

Although we assumed that the behaviour of the electrode is purely linear, as described in [89] the double-layer capacitance C_{dl} varies with the potential applied across the interface as:

$$C_{dl} = C_{dl0} \cosh\left(\frac{zV_{el}}{V_t}\right) \tag{2.6}$$

where V_{el} is the potential across the interface, z the valence of ions and V_t the thermal voltage defined as:

$$V_t = \frac{kT}{q} \tag{2.7}$$

where k is the Boltzmann constant, T the ambient temperature and q the charge of an electron. For a body temperature of 310 K (36.85 °C), V_t is approximately 26.7 mV and therefore at least an order of magnitude larger than typical neural signals, meaning that C_{dl} can be assumed constant and the effect of its variance on the distortion of the acquired signal negligible. To put this into perspective, a signal of a 1 mV amplitude would result in a variation of C_{dl} of ≈0.07%. If the input of the AFE had the same capacitance as C_{dl}, the power of the resulting first harmonic would be ≈80 dB smaller than the fundamental.

To allow for a connection of C_{dl} with physical properties of the electrode, it is easy to see that its magnitude is linearly proportional to the surface area A_s of the electrode given the nature of double-layer capacitance and the fact that its material does not affect the formation of the Helmholtz plane. We can thus denote the relationship as:

$$C_{dl} \propto A_s \tag{2.8}$$

2.1.2 Faradaic Current

The parallel path in Figure 2.2 consisting of R_{ct} and Z_W represents a direct current path that is a result of oxidation-reduction reactions at the surface of the electrode. As described in [94], this can be described as a resistive element R_{ct}:

$$R_{ct} = \frac{V_t}{zJ_0A_s} \tag{2.9}$$

where all variables have the same meaning as before and J_0 is the exchange current density, a property of the used material. The resistance is inversely proportional to the surface area of the electrode and for future reference we can therefore note the relationship

$$R_{ct} \propto \frac{1}{J_0A_s} \tag{2.10}$$

In addition, the model contains an element Z_W, termed Warburg impedance related to the presence of diffusion processes and exerts a constant phase of $\pi/4$ [89; 92]. It is noted [94] that its magnitude is negligible for materials and frequencies typically involved in electrophysiological experiments.

2.1.3 Spreading Resistance

Finally, the last element of Figure 2.2, R_s models the spreading resistance. As described in [89], this is a result of assuming that the counter electrode is infinitely large and the signal spreads towards it. For a circular electrode this can be derived [94] as:

$$R_s = \frac{\rho_{ey}}{4R_{el}} \tag{2.11}$$

where R_{el} is the electrode radius. Since R_{el} is proportional to the square root of the area of the circular electrode surface, we note that:

$$R_s \propto \frac{1}{\sqrt{A_g}} \tag{2.12}$$

where A_g is the geometric area of the electrode, as opposed to surface area A_s that is present in expressions for C_{dl} and R_{ct}.

2.2 Analysis of Electrode Model

Reusing the model of Figure 2.2 and following the assumption that Z_w can be neglected, we can now express the composed electrode impedance as:

$$Z_{el} = R_s + \frac{R_{ct}}{1 + j\omega R_{ct} C_{dl}} = \frac{R_{ct} + R_s + j\omega C_{dl} R_s R_{ct}}{1 + j\omega C_{dl} R_{ct}} \tag{2.13}$$

Assuming that $R_{ct} >> R_s$, this expression tends to R_{ct} at small frequencies and to R_s at large frequencies. Empirically this can be explained by the signal passing through the interface due to Faradaic processes at small frequencies and therefore subject to charge transfer resistance R_{ct}. At high frequencies, R_{ct} is bypassed by the double-layer capacitance C_{dl} and the impedance becomes dominated by the spreading resistance R_s.

Since our aim is to minimise the amount of noise in the recording, following equation 2.5, we are interested in an expression for $\Re(Z_{el})$ that gives rise to thermal noise:

$$\Re(Z_{el}) = \frac{R_{ct} + R_s + \omega^2 C_{dl}^2 R_s R_{ct}}{1 + \omega^2 C_{dl}^2 R_{ct}^2} \tag{2.14}$$

As illustrated by Figure 2.3, this expression has two poles at ω_p and two zeros at ω_z:

$$\omega_p = \frac{1}{R_{ct} C_{dl}} \tag{2.15}$$

$$\omega_z = \omega_p \sqrt{\frac{R_s + R_t}{R_s}} \tag{2.16}$$

As expected, $\Re(Z_{el})$ tends to R_{ct} at small frequencies and to R_s at large frequencies. In order to understand how to design electrodes that lead to minimisation of the amount of generated thermal noise, we can now use the relationships of section 2.1 showing the relationships of model parameters C_{dl}, R_{ct} and R_s to physical electrode properties A_g, A_s and J_0 that respectively

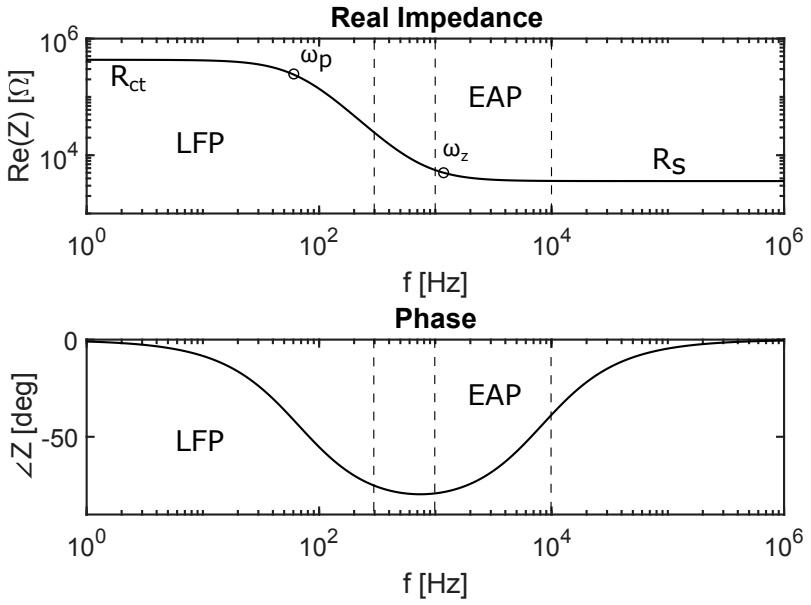

Figure 2.3: Plots of $\Re(Z_{el}(f))$ and $\angle Z_{el}(f)$ for a planar circular platinum electrode of a 100 µm diameter, using parameter values from [89].

represent the geometric area of the electrode, its surface area and exchange current density, a quantity affected by the used material. The effects of changing these parameters can be observed in Figure 2.4, showing families of curves of $\Re(Z_{el})$ for various parameters.

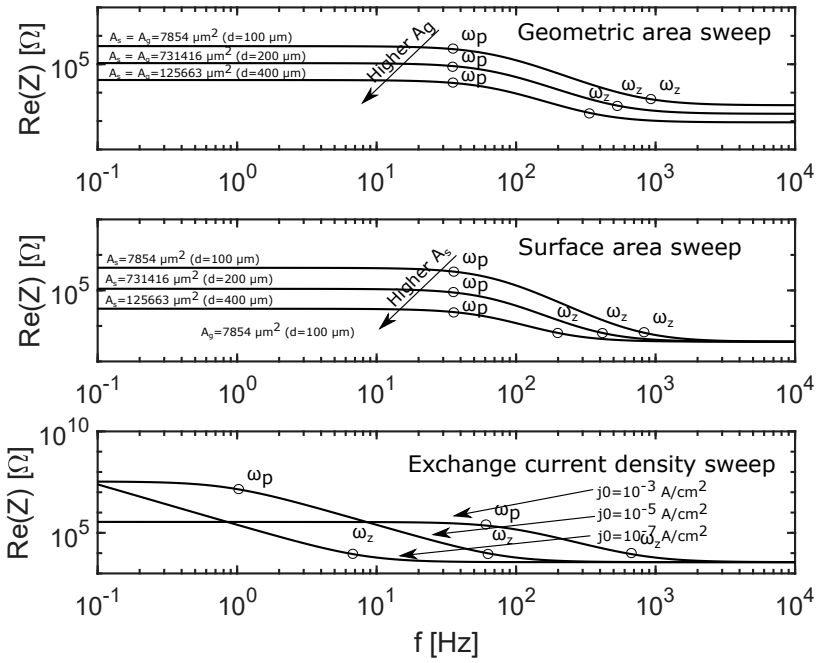

Figure 2.4: Family of curves of $\Re(Z_{el}(f))$ for a Pt electrode showing sensitivity of impedance to a change of A_g, A_s and J_0. Unless otherwise stated $J_0 = 7.94{\cdot}10^{-4}\ A/cm^2$, $A_g = A_s = 7854\ \mu m^2$ (100 μm diameter).

2.2.1 Effects of Increasing Electrode Geometric Area on Recording Noise

It can be seen that increasing the geometric area while assuming $A_g = A_s$ leads to a reduction of $\Re(Z_{el})$ across all frequencies. This is an expected and intuitive result indeed indicating that larger electrodes are less noisy and vice versa, small electrodes lead to more noise. This takes us to a question of whether increasing the electrode size is universally leading to improvements in quality of the recorded signal.

To consider that, we also have to explore how the size of the electrode affects the signal power and therefore the resulting SNR. While increasing the electrode size leads to a reduction of thermal noise generated by the interface, it also leads to shunting of the surrounding tissue and therefore spatial averaging of the recording signal. An interesting insight can be found in a study by S. F. Lempka et al. [95] who have created a finite element model simulating an ensemble of neurons and an electrode of various sizes inserted into the simulated tissue environment. The model was then used to estimate both the electrode noise and signal power to plot a relationship between the electrode size and the estimated SNR. As expected, it was found that the thermal noise power decreases linearly with the electrode area. In addition, it was observed that the power of the acquired biological noise also decreases with increased electrode sizes, an effect connected to an increased amount of spatial averaging inherently present in larger electrodes.

It was also found that the recorded signal power increases with decreasing electrode size. The authors note that within the studied range of electrode areas (177 - 1250 µm^2), equivalent to a square of side lengths 13.3 - 35.4 µm, the observed SNR marginally increases with decreasing electrode size. At the same time, the difference in SNR observed between an electrode of 177 µm^2 and 1250 µm^2 only amounts to approximately 6%.

Additional insights can be gained from a study by V. Viswam et al. [96] who have manufactured a CMOS electrode array with planar electrodes of varying sizes between (1 x 1 µm^2 - 100 x 100 µm^2) and performed in-vitro measurements of mice brain slices observing the amount of recorded noise and signal power.

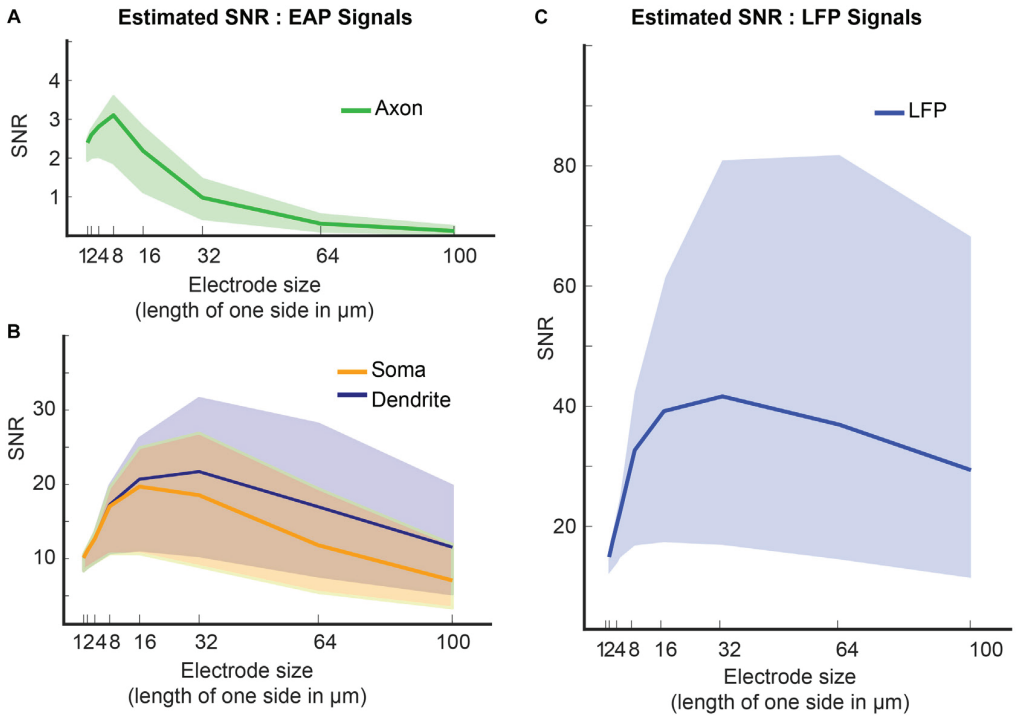

Figure 2.5: Measured SNR vs electrode size for various types of recorded signals - A) Axonal EAP, B) Somatic and Dendritic EAP, C) LFP; Shaded area represents different levels of present background activity (min 1 µVrms, median 3 µVrms, max 8 µVrms); Figure reproduced from [96].

As seen in Figure 2.5, the measured SNR generally increases with decreasing electrode sizes as predicted by the simulated model of S. F. Lempka et al. [95], however at a certain threshold this relationship breaks and further decreases in size do not lead to SNR gain but rather to its deterioration. The authors note that in the case of EAP recordings, this is largely caused by the increase of the electrode impedance and the resulting attenuation due to the input impedance of the used instrumentation circuits as described by Equation 2.2.

The results presented in the study could however have been caused by inadequate input impedance of the used circuitry rather than being a property of the electrodes themselves. It is noted that the same integrated circuit as described in [97] was used. While the publication does not explicitly state the input impedance of the acquisition circuit, it is possible to conclude that the used architecture of the first stage (operational amplifier with a passive feedback network) does not warrant the highest possible input impedance and therefore there is a possibility that smaller electrodes might still result in higher SNR if a different front-end with a higher input impedance was used. Possible architectures that achieve this are going to

be discussed in upcoming chapters.

On the other hand, the authors mention that in general larger electrodes perform better for LFP recordings as demonstrated by Figure 2.5. It is argued that LFPs are spatially significantly more coherent and therefore the reduction of signal amplitude due to tissue shunting and spatial averaging is not as prominent. At the same time, there is a gain in reduction of both electrode thermal noise and biological noise.

In conclusion, it can be said that although the presented electrode model suggests there is an advantage in using larger electrodes due to the reduced thermal noise power, evidence in literature shows that this is not a valid result. As shown, an increase in electrode size at the same time leads to a reduction of the power of the acquired signal, diminishing the gains in SNR caused by the reduction in noise power. While arguably EAP recordings benefit from smaller electrodes, there seems to be an ideal size for LFP recordings around 32 µm x 32 µm, or around 1000 μm^2.

2.2.2 Effects of Increasing Electrode Surface Area on Recording Noise

Although increasing the geometric area of the electrode might not lead to the expected results, it is also possible to alter the electrode's surface area while keeping its geometric area fixed. As demonstrated in Figure 2.4, this leads to a reduction of $\Re(Z_{el}(f))$, as well as associated reduction of impedance magnitude, at frequencies smaller than ω_z. At those frequencies, the impedance is dominated by R_{ct} and C_{dl} which as shown by equations 2.10 and 2.8 is inversely proportional to the surface area of the electrode. This is, of course, an intuitive result as the larger surface area leads to a formation of a larger area of solvated ions, increasing C_{dl} and a larger area permitting oxidation/reduction decreasing R_{ct}. At the same time, if the geometric area remains fixed, this gain does not come at the cost of reduction to signal amplitude as was the case in the use of a larger electrode geometry.

Literature contains many examples of methods that achieve such an increase in surface area such

as electrochemical roughening [98], patterning [99] or growth of nanostructures on the electrode surface. An example of such is electrochemical deposition of "platinum black" [100; 101], leading to growth of platinum microstrustructures as seen in Figure 2.6. It is worth noting that this process can also be applied to microwire arrays [102], leading to a reduction of the electrode impedance by an order of magnitude. Another example of a nanostructure targeted at increasing the electrode surface area is "platinum grass" [103] created using an electrochemical process that has been shown to lead to a reduction of electrode impedance by two orders of magnitude.

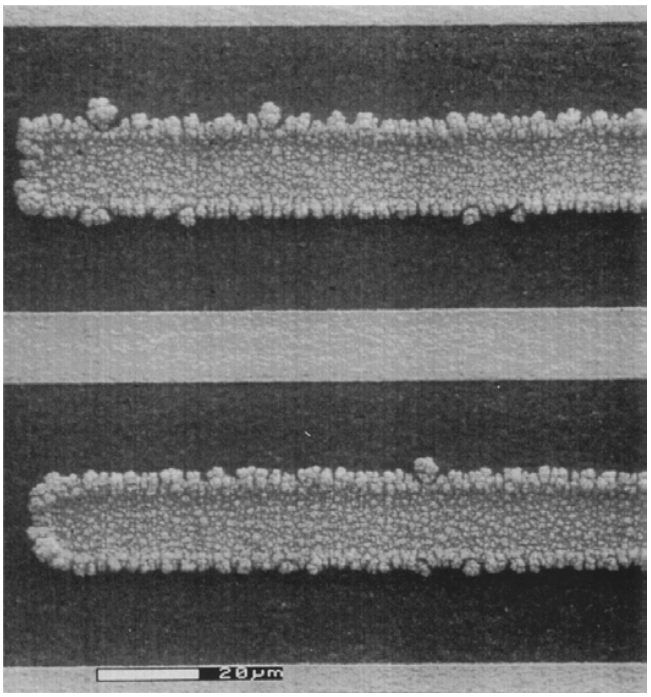

Figure 2.6: Scanning electron microscope picture of two planar finger elecrodes with platinum black deposition; Figure reproduced from [101].

Although the usage of methods increasing the surface area of electrodes seems to be universally leading to improvements, there are still several issues hindering this method. While there are well-described processes of creating nanostructures on platinum surfaces, this might not be replicable in other materials. In addition, there are issues with adhesion [102] of the added microstructures and to our best knowledge, there has not been a study evaluating the longevity of such coatings in chronically implanted electrodes.

2.2.3 Effects of Electrode Materials on Recording Noise

Having considered the effects of varying the electrode geometry, such as its surface and geometric area, we should also explore the results of using various materials on the SNR of the recording. Observing the previously presented expressions for C_{dl}, R_{ct} and R_s we note that the only component with a parameter dependent on the electrode material is R_{ct} which is inversely proportional to J_0, the exchange current density. This quantity describes the rate of oxidation/reduction occurring at the surface of the electrode at zero potential and therefore the ease of faradaic conduction. This is dependent on both the electrode material as well as the electrolyte and is a basis on which electrodes can be divided into the categories of polarisable and non-polarisable.

A polarisable electrode is made of materials of small exchange current density J_0 and only permits a limited amount of current passing through its interface and therefore behaves more like a capacitive element rather than a resistive one. The opposite is true for non-polarisable electrodes made of materials of large J_0 leading to small R_{ct} and therefore having their impedance dominated by their resistance.

Many studies evaluating electrodes found in the literature only assess electrodes based on impedance measured at a single frequency (typically 1 kHz for EAP recordings) [104; 105] and the choice of electrodes is then often driven by the impedance measured at this single frequency. Observing the effects of varying J_0 in Figure 2.7, however, shows that this is not sufficient to gain a complete understanding of the electrode's behaviour.

In addition, electrode impedance is often evaluated in terms of its magnitude to make comparisons. Although its minimisation is important to ensure minimal signal attenuation due to input impedance of the analogue front-end, the importance of that is reduced with the use of fully integrated brain implants as opposed to the use of table-top instruments utilised for neural recordings in the past. As will be demonstrated in upcoming chapters, it is feasible to create analogue front-ends with input impedance on the order of 10^{10} Ω, reducing the problem of signal attenuation at their input.

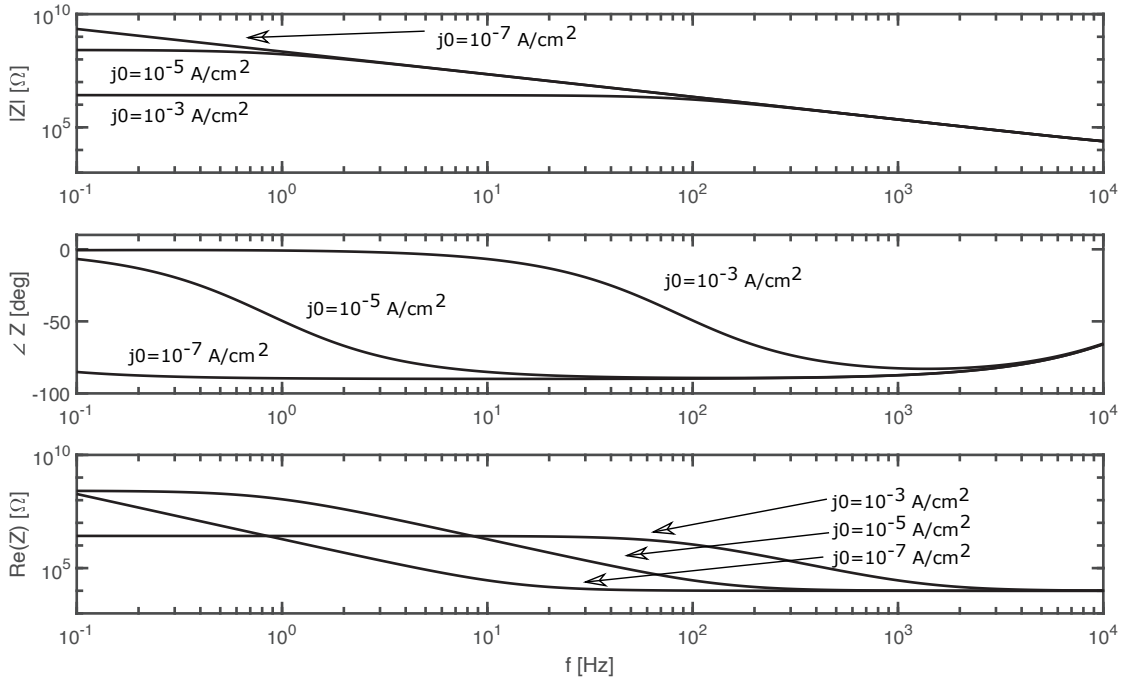

Figure 2.7: Family of curves of $|Z_{el}(f)|$, $\angle Z_{el}(f)$ and $\Re(Z_{el}(f))$, demonstrating the effect of using electrodes with various J_0 (10^{-3} A/cm^2, 10^{-5} A/cm^2 and 10^{-7} A/cm^2). $A_g = A_s = 32 \times 32$ µm^2.

If the magnitude of electrode impedance is not of concern, the main design target then becomes the minimisation of noise power that as shown by Equation 2.5 is proportional to real impedance. As seen in Equation 2.14, $\Re(Z_{el}(f))$ tends to the same value as $|Z_{el}(f)|$ at high and low frequency asymptotes (R_s and R_{ct} respectively) and the position of their pole ω_p is the same. The position of the zero ω_z in $\Re(Z_{el}(f))$ is at a lower frequency than the zero ω_{z0} of $|Z_{el}(f)|$. This is caused by a faster 40 dB/dec roll-off of $\Re(Z_{el}(f))$ as opposed to 20 dB/dec decay in $|Z_{el}(f)|$.

As demonstrated by Figure 2.7, this leads to an interesting and unintuitive behaviour of $\Re(Z_{el}(f))$ in the case of highly polarisable electrodes of very small J_0 and subsequently large R_{ct}. Even though the magnitude of impedance of such an electrode $|Z_{el}(f)|$ is always higher when compared to a less polarisable electrode with higher J_0, the same does not hold for its real impedance $\Re(Z_{el}(f))$ that is smaller in a highly polarisable electrode for a range of frequencies. If this range of frequencies happens to be within the frequency band of interest (LFP or EAP) then a polarisable electrode is going to lead to a better noise performance than a non-polarisable one despite its higher impedance magnitude.

To demonstrate this effect, we can consider a relationship between the integrated root mean squared (rms) noise in both EAP and LFP bands and the exchange current density J_0:

$$N_{LFP,EAP}(J_0) = \sqrt{\int_{LFP,EAP} \overline{v_{nel}^2}(f)\ df} \tag{2.17}$$

This can be seen plotted in Figure 2.8 for both the LFP band and the EAP band. To reflect findings presented in subsection 2.2.1 regarding an optimal electrode size, an electrode area of 32 µm x 32 µm area was chosen for the evaluation of noise power in LFP band and an electrode of 8 µm x 8 µm area was chosen for the evaluation of noise in the EAP band. The result demonstrates that within the range of studied values of J_0 it is indeed preferable to choose a more polarisable material of smaller J_0.

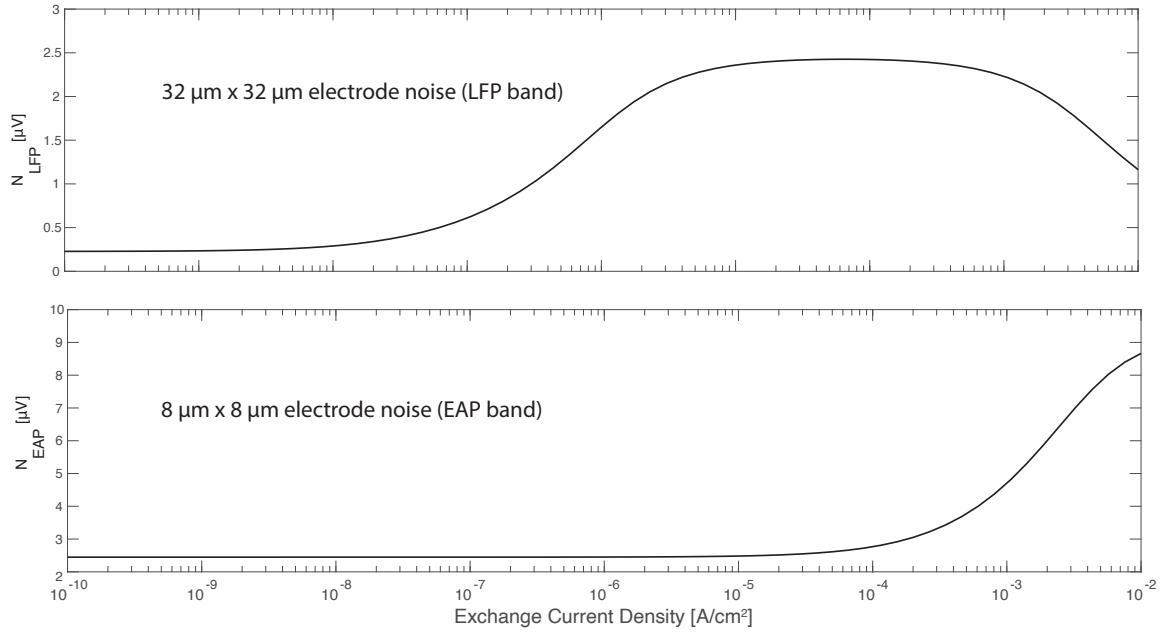

Figure 2.8: Relationship between rms electrode noise and exchange current density. Top: Noise integrated in LFP band for a 32 µm x 32 µm electrode. Bottom: Noise integrated in EAP band for a 8 µm x 8 µm electrode.

To put this into perspective, we have to explore values of J_0 for materials typically used in neural recordings. This is however arguably a difficult task as J_0 is dependent on both the electrode material as well as the electrolyte. Since to the best of our knowledge there has not been a study conducted evaluating the exchange current density of typically used electrode materials in cerebrospinal fluid (CSF), we have to resort to alternative results for comparison between

Material	J_0 [A/cm^{-2}]	E [GPa]
Platinum (Pt)	$10^{-3.0}$	168
Iron/Steel (Fe)	$10^{-5.6}$	211
Tungsten (W)	$10^{-6.4}$	411
Gold (Au)	$10^{-6.5}$	78
Titanium (Ti)	$10^{-8.3}$	116
Niobium (Nb)	$10^{-8.4}$	105

Table 2.1: Exchange current density J_0 for hydrogen evolution reaction in 0.5 M H_2SO_4 and Young's modulus E of selected metals used for manufacturing of neural recording electrodes. Values of J_0 taken from [106], values of E taken from [107].

the materials. Some insight can be gained from J_0 of hydrogen evolution reaction in a diluted solution of sulphuric acid (0.5 M H_2SO_4), a quantity that is well reported in literature [106].

Referring to values of J_0 for chosen materials often used for manufacturing of neural recording microwires in Table 2.1 we note that J_0 of platinum (Pt) is on the order of $10^{-3.0}$ A/cm^{-2}. Pt is often been the material of choice for neural recordings due to its biocompatibility and chemical inertness ensuring its stability when implanted. However, as seen in Figure 2.8 this would result in a large rms noise compared to the use of materials of smaller J_0.

2.3 Niobium as a Potential Novel Electrode Material

Having shown that the use of Pt as a material for recording electrodes might not be ideal from the point of view of reducing the amount of noise generated in the electrode/electrolyte interface, we can consider alternative materials that might be suitable for the creation of microwire electrodes. We require this material to be biocompatible, result in as small J_0 in CSF as possible in addition to having favourable mechanical properties. While, as mentioned in Chapter 1, many sources argue that it is favourable to use electrodes that have mechanical properties as similar to the neural tissue as possible in order to prevent the growth of scar tissue, it can at the same time be difficult to insert those electrodes into the cortex due to buckling of the wires [44], sometimes leading to Tungsten (W) becoming the material of choice. From the materials in Table 2.1, Titanium (Ti) and Niobium (Nb), however strike as a promising choice due to their high polarisability.

From those two materials, Ti has previously [105] been used for creation of neural recording electrodes due to its stiffness and perceived biocompatibility. Recently, there has, however, been a growing amount of evidence [108] suggesting that Ti might be toxic under some conditions.

This brings our attention to Nb as a material of interest. To the best of our knowledge, Nb has not been previously reported as a material used for the creation of neural recording microwires. Its small value of J_0 however suggests that it might be a good candidate for minimising the amount of noise in recordings. At the same time its stiffness quantified by the Young's Modulus E as seen in Table 2.1 is comparable to materials that are already being used (Pt, Fe, Ti). Although no study exploring the compatibility of Nb when implanted in brain tissue is known to us, there is evidence to suggest that Nb is in general biocompatible.

H. Matsuno et al. [109] have implanted various materials, including Nb, into bone marrow and have reported no adverse results. Similarly, a study by R. Olivares-Navarrete et al. [110] demonstrated that niobium coatings were more biocompatible than uncoated surgical stainless steel. Additionally, Nb implants are being used for dental implants [111].

2.3.1 Verification of Suitability of Nb as an Electrode material

To verify the theory that Nb is a suitable material for the manufacturing of neural recording microwires, an experiment has been conducted to measure the impedance of Nb electrodes in comparison with Pt. This was conducted using a CH 660E electrochemical workstation as seen in Figure 2.9. Phosphate-buffered saline (PBS) was used as an electrolyte that roughly simulates the chemical properties of CSF. This is reasonable as CSF is a solution dominated by a concentration of more than 150 mmol/L of NaCl [112] similar in composition to that of PBS.

The solution was placed in a beaker alongside a large-area Pt electrode acting as a counter electrode and an Ag/AgCl electrode acting as a reference electrode. Short sections of a 100 µm-diameter microwire were cut, held by crocodile clips with leads connecting the electrode to the electrochemical workstation. The microwire electrode was held using a ring stand such that

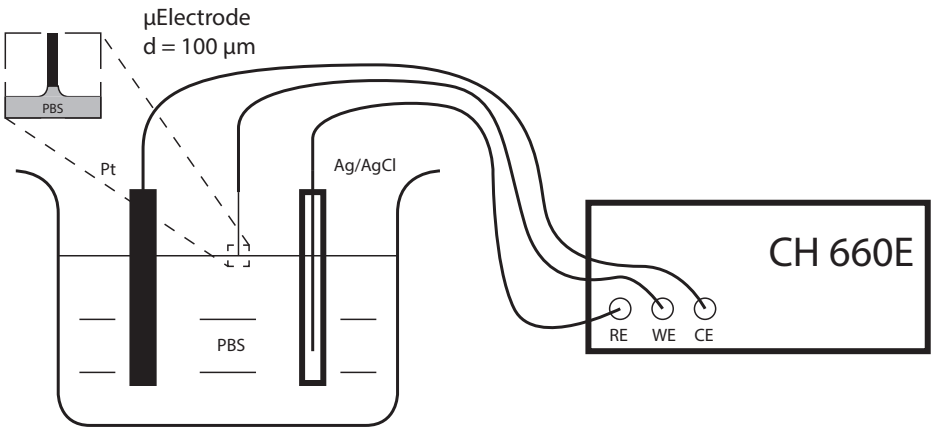

Figure 2.9: Experimental setup used for impedance characterisation of microwire electrodes using a CH 660E electrochemical workstation, a large area Pt Counter Electrode (CE) and an Ag/AgCl Reference Electrode (RE).

its end surface was just about touching the solution but the body of the electrode was not immersed at all.

A pure sinewave frequency sweep between 0.1 Hz and 100 kHz was then used to measure a relationship between the electrode impedance and frequency and |Z(f)|, $\Re$(Z(f)) and $\angle Z(f)$ was obtained for both Nb ($Z_{Nb}(f)$) and Pt ($Z_{Pt}(f)$) microwires. The obtained curves seen in Figure 2.10 show that the behaviour of the electrodes roughly follows the predicted curves of Figure 2.7. There is a visible mismatch in high-frequency values of both $Z_{Nb}(f)$ and $Z_{Pt}(f)$. This should however be equal to R_s and therefore independent of the used material.

The discrepancy is caused by a mismatch between the immersed area of both the Pt and Nb electrode due to limitations of the experimental setup in its inability to achieve its precise control. Using estimated values of $R_{s,Pt}$, $R_{s,Nb}$ and following equation 2.12, the ratio between the immersed geometric areas can be estimated as:

$$\frac{A_{g,Nb}}{A_{g,Pt}} \approx \left(\frac{R_{s,Pt}}{R_{s,Nb}}\right)^2 = \left(\frac{345.3}{200.4}\right)^2 \approx 2.97 \tag{2.18}$$

The accuracy of this estimate is however limited, since equation 2.12 is derived under the assumption that the electrode is a planar circular electrode and the counter-electrode is infinitely large.

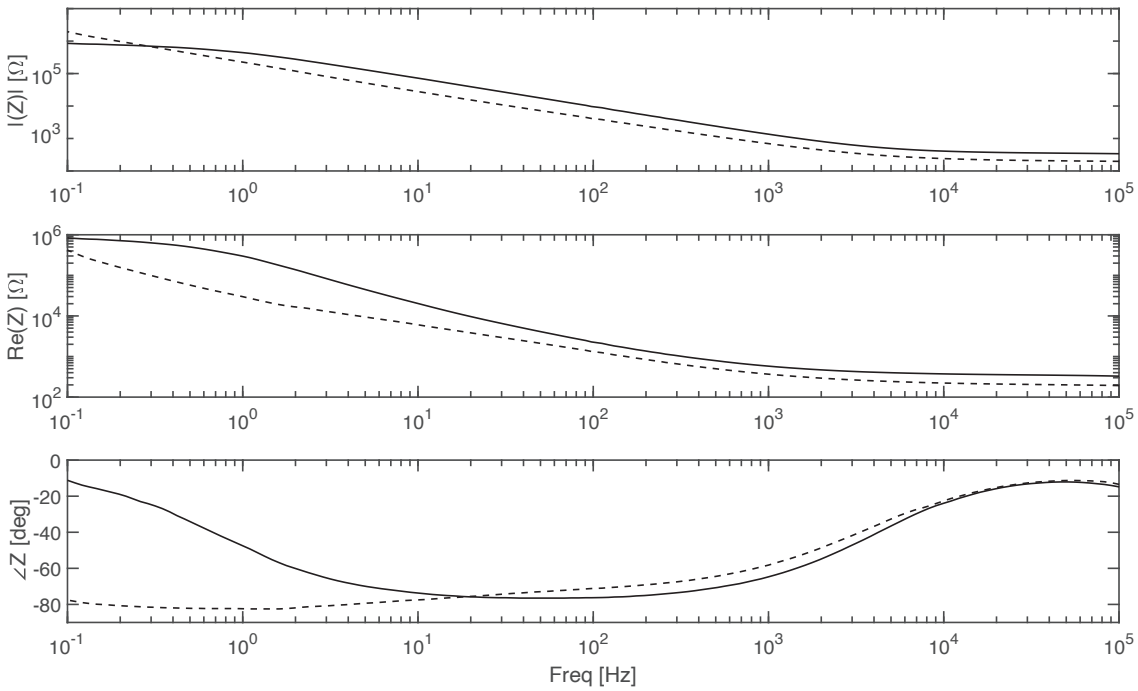

Figure 2.10: Measured impedance of 100-µm-diameter Pt (solid) and Nb (dashed) electrodes; top - |Z(f)|, center - $\Re$(Z(f)) , bottom - $\angle Z(f)$

Although the result of this experiment can be difficult to interpret due to the differences in immersed area of the two electrodes, it is sufficient to show that the exchange current density of Nb is smaller than that of Pt and therefore Nb immersed in PBS behaves in a more polarisable manner than Nb. This is due to the fact that the position of pole ω_p, that is the same for both Z(f) and $\Re$(Z(f)), is independent of the area of the electrode. Denoting the double-layer per-area capacitance C_{dl0} such that $C_{dl} = A_s C_{dl0}$ and reusing equations 2.15 and 2.9, we obtain:

$$\omega_p = \frac{1}{R_{ct} C_{dl}} = \frac{z J_0 A_s}{V_t C_{dl0} A_s} = \frac{z J_0}{V_t C_{dl0}} \tag{2.19}$$

Figure 2.10 shows that at small frequencies the phase of $Z_{Nb}(f)$ approaches 90°, whereas that of $Z_{Pt}(f)$ approaches 0°. Since the position of ω_p does not depend on the immersed electrode area this conclusively shows that a Nb electrode is more polarisable than a Pt one when immersed in PBS. It can also be seen that the magnitude of $\Re(Z_{Pt}(f))$ is significantly larger than that of $\Re(Z_{Nb}(f))$ at a wide range of frequencies in the LFP band. As seen in Table 2.2, this difference reaches an order of magnitude at f = 1 Hz, which is larger than what can be attributed to the estimated difference of immersion area. This is the case as the impedance scales with A_s at

small frequencies, when dominated by R_{ct} and with $\sqrt{A_g}$ at large frequencies when dominated by R_s.

f [Hz]	$\Re(Z_{Nb})$ [kΩ]	$\Re(Z_{Pt})$ [kΩ]
1	29.84	298.2
3	12.59	77.98
10	6.05	20.25
30	2.85	6.21
100	1.33	2.29
300	0.64	1.02

Table 2.2: Measured values of $\Re(Z_{Nb})$ and $\Re(Z_{Pt})$ for a range of frequencies in the LFP band.

Although it is not possible to estimate J_0 of Nb from the recorded data, due to $\omega_{p,Nb}$ being outside the measured frequency range, $\angle Z_{Pt}(f)$ equals 45° at a frequency of 0.91 Hz and therefore we obtain an estimate $\omega_{p,Pt} \approx 0.91$. Using equation 2.19, we can thus estimate $J_{0,Pt} \approx 5 \times 10^{-6}$. This is smaller than that of Table 2.1 for hydrogen evolution reaction but in line with value presented in [113] when measured in PBS.

2.3.2 Conclusion

The experiment helped verify some of the fundamentals of the presented electrode-electrolyte interface model, such as it being a system of a single pole and a single zero in addition to demonstrating that Nb might be an interesting material to be used for manufacturing of electrodes that has been largely unnoticed by the community. Despite that, it is a biocompatible material that is less stiff than currently used materials and might therefore lead to a reduction of the foreign body response if the increased difficulty of its insertion can be overcome.

As demonstrated above, its electrical properties should lead to lower noise power when used for recordings in LFP bands, a result that would have to be further verified in another experiment making use of electrodes manufactured with precisely controlled area such that a direct comparison can be made between different materials. The high low-frequency impedance of a strongly polarisable material such as Nb would require the electrodes to be manufactured on a single substrate alongside a high-input-impedance low-noise amplifier. This work is outside of the scope of this project and is reserved for future additions.

2.4 Introduction to Analogue Front-Ends

Presenting an electrical model of the electrode-electrolyte interface has given us an understanding of its behaviour that is going to be helpful in outlining the requirements for the design of a neural recording analogue front-end and the associated challenges. The aim of the analogue front-end is to interface with the electrodes, condition and amplify the signal such that it can be transmitted outside of the neural interface without further corruption in terms of added noise and distortion. While there have been many purely analogue designs, it has recently been a trend to digitise the signal inside the implant, thus simplifying further transmission and processing.

Broadly speaking, the analogue interface has to be able to interface with a recording electrode of high impedance, often on the order of 10s-100s of MΩ, if not close to 1 GΩ and therefore itself have a very high input impedance. The recorded signals can vary in magnitude between 10s of µV to mV and therefore a large dynamic range, typically around 60 dB, is needed. In addition, the input signal is often subject to large DC offsets, on the order of up to 100 mV [114], caused by the formation of electrochemical half-cells at the electrode-electrolyte interface. The offset potential also typically varies in time due to chemical and other processes resulting in changes of the electrode structure and therefore its potential.

As the electrode-electrolyte interface is of large impedance, it leads to generation of thermal noise. This can often act as a guideline for the needed noise floor of the analogue front-end, such that it is not over-designed. As a reference, noise power in Pt and Pt-black electrodes measured by V. Viswam et al. [96] can been seen in Figure 2.4. This shows noise floor on the order of 100 nV/$\sqrt{}$Hz for a reasonably sized electrode that rises to up to 1 µV/$\sqrt{}$Hz in the LFP band. Another challenge stems from the the nature of neural signals and their occupation of low frequencies. This is problematic from the point of view of creation of analogue filters and the associated need for large passive components that are not feasible within the limited area of a neural implant. In addition, instrumentation circuits processing small frequency signals, such as LFPs and to a lesser extent EAPs, are often hindered by the presence of flicker noise. Techniques of its reduction are therefore an important aspect of neural acquisition circuits.

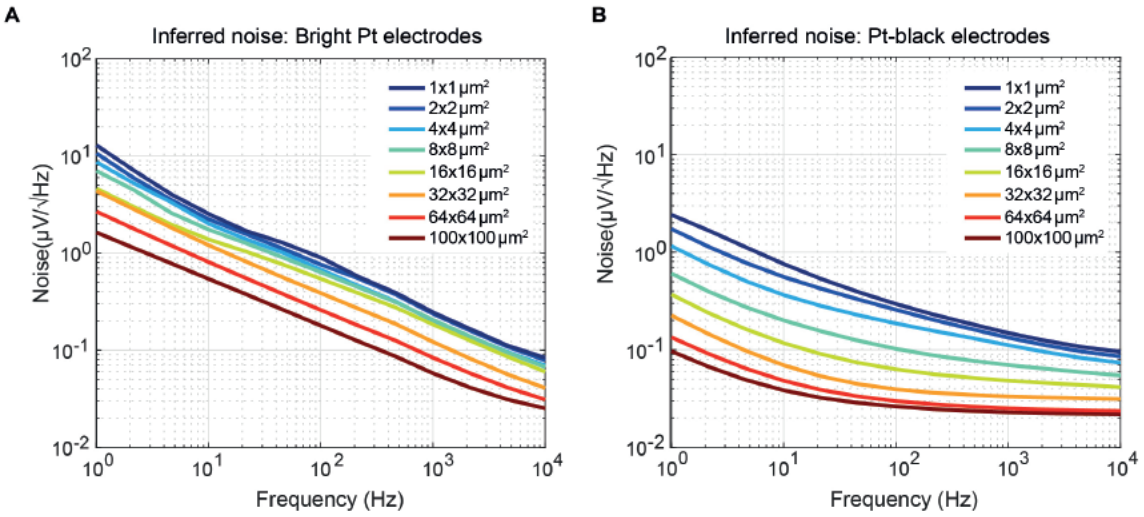

Figure 2.11: Measured noise power density of Pt (A) and Pt-Black (B) electrodes of various sizes. Figure reproduced from [96].

Modern analogue front-ends can typically be decomposed into a low-noise input amplifier and an ADC, although as we will see later, those are sometimes merged into a single block in some topologies where the ADC itself has properties that allow it to directly quantise the neural signal without the need for any preamplification or conditioning.

The input amplifier is one of the most critical components as it directly interfaces with the recording electrodes. It has to remove any input offset, apply additional filtering if the separation of EAP and LFP and is needed and amplify the signal to a level that is suitable as an input to the ADC.

To compare the efficiency of input amplifiers, a Figure of Merit (FOM), termed the Noise Efficiency Factor (NEF) [115] is typically used. This is defined as:

$$NEF = V_{rms,in}\sqrt{\frac{2I_{tot}}{\pi \times V_t \times kT \times BW}} \tag{2.20}$$

where $V_{rms,in}$ is the rms of input-referred noise, I_{tot} the total consumed currect, V_t the threshold voltage and BW the bandwidth of operation.

2.4.1 Harrison's Amplifier

As mentioned earlier, one of the greatest challenges of creating a fully integrated neural acquisition systems is the need to create a DC rejection filter removing the electrode offset. Since the frequency band of LFPs begins at around 1 Hz, this requires the implementation of a high-pass filter with a sub-Hz cut-off frequency. In a conventional setting, this would typically be implemented by the use of large DC-blocking capacitors (such as [115] requiring a 300 nF capacitor), a solution that is not practical in CMOS without the use of external components.

An alternative method to achieving a sub-Hz filter cut-off is the introduction of a large resistance combined with a smaller capacitance. Assuming the use of a practically implementable input capacitor of 100 pF capacitance, the resistance to achieve a 1 Hz cut-off would have to be ≈1.6 GΩ. Although it is not possible or practical to create such a large linear on-chip resistor, a popular method to implement such a large resistance is the use of a reverse-biased semiconductor junction forming a small-signal "pseudoresistor". Some of the earliest examples of this method can be found in the work of M. G. Dorman et al. [116] of 1985 or J. Ji and K. D. Wise [117] of 1992 who have both shown implementations of fully integrated neural recording analogue front-ends using reverse-biased diodes in combination with capacitors to implement low-frequency filter cut-offs.

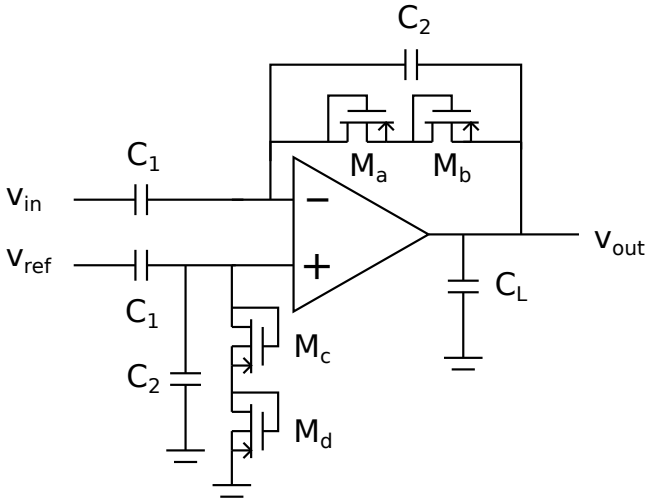

Figure 2.12: Schematic of Harrison's amplifier topology Figure previously published in [118]; Schematics from [119].

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One of the most cited practical solutions making use of pseudoresistors was however presented by R. R. Harrison [119] in 2003 who has the proposed the circuit of Figure 2.4.1. This achieves the creation of the sub-Hz corner frequencies by the use of reverse-biased PMOS transistors forming a "pseudoresistor" of very large resistance ($> 10^{11}\ \Omega$) used in combination with a 200 pF input capacitor giving rise to a cut-off frequency of 0.015 Hz. Additionally, this topology has a well-defined in-band gain, that is set by the ratio of the used capacitors:

$$A = \frac{C_1}{C_2} \tag{2.21}$$

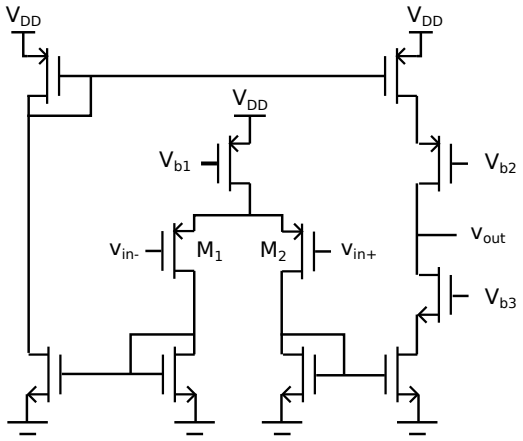

Figure 2.13: Schematic of the OTA used in Harrison's amplifier. Figure previously published in [118]; Schematics from [119].

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An improvement of Harrison's design over many previously presented solution has been the outline of the design's optimisation for noise performance. The circuit uses a simple OTA topology seen in Figure 2.4.1, the NEF expression of which, as derived in [119], can be reduced to:

$$NEF = \sqrt{\frac{4}{\kappa V_t}\frac{I_{D1}}{g_{m1}}} \tag{2.22}$$

Where I_{D1} is the drain current of the input pair, g_{m1} its transconductance and κ the gate coupling coefficient. This ratio and the NEF is minimised by placing transistors M_1 and M_2 into deep sub-threshold region, at which point the transconductance efficiency g_{m1}/I_{D1} reduces

to κ/V_t and therefore, as shown in [119], the NEF expression becomes:

$$NEF = \sqrt{\frac{4}{\kappa^2}} \approx \sqrt{\frac{4}{0.7^2}} \approx 2.9 \tag{2.23}$$

Although this topology achieved significant success in the research world, as well as in commercial use marketed by Intan Technologies LLC, it has limitations that are overcome by more recent designs. Those are mainly caused by the use of pseudoresistors that expose the design to a large amount of issues that can be divided into the categories of resistance variations, non-linearity and unreliability.

The resistance of pseudoresistors is often difficult to predict due to factors including large temperature dependence [120] and susceptibility to manufacturing process variations [121]. In addition, they suffer from non-linearity [122] that reduces the achievable Signal to Noise and Distortion Ratio (SNDR) in circuits employing them [123]. Those effects can to some extent be mitigated by the employment of feedback circuits tuning the gate voltage of the pseudoresistor such that its resistance is better controlled [121; 124]. The utilisation of pseudoresistors in a clinical setting is however still problematic due to the difficulties faced obtaining regulatory clearance [125] caused by limited long-term stability and susceptibility to radiation and other interference.

2.4.2 DC-Coupled Amplifiers

The issues faced by the employment of pseudoresistors have been a driving force behind the search for alternative methods allowing the implementation of a fully integrated front-end without the need for external components. An alternative to the direct implementation of a high-pass filter removing the DC offset is the use of a feedback loop extracting the DC offset and feeding it back to the input from which it is subtracted. This allows the input signal to be directly DC-coupled to the amplifier's input, thus preventing the need for DC-blocking capacitors.

As opposed to topologies based on Harrison's implementation, this has several advantages starting with the exclusion of pseudoresistors from the design, thus increasing their reliability. If a feedback loop is present, the high-pass filter can be implemented by placing an integrator in the loop itself. Although the resulting low-pass filter still needs to have a very low frequency corner, its displacement from the input allows for a larger spectrum of possible solutions. One possibility is the implementation of a digital loop [32] and therefore the use of a digital filter avoiding the need for large components. Another alternative is the use of Gm-C filters [126] exploiting the fact that the implementation of small Gm elements is not prohibitively difficult. Other techniques that can be used include switched-capacitor filters [127] or switched-current filters [128].

Another advantage of the DC-coupled approach stems from the fact that the signal is directly coupled to the input of the amplifier. This means that in the case of CMOS amplifiers the input impedance can be reduced to the impedance of the gate only. This means the input resistance can be on the order of TΩ making the input impedance dominated by the gate's capacitance.

A slight challenge arises in the selection of the method used to feed the filtered signal back to the input. In digital-based solutions this often involves the need for a DAC that can be expensive in terms of the needed area. A mechanism allowing the injection of the signal to the first stage of the analogue front-end then has to be devised. To keep the advantage of high input impedance, it is undesirable to inject the signal directly to the input. Previously presented solutions [114] include the use of difference-differential amplifiers [129] or width modulation of the input pair [32]. Another method is the modulation of the input pair's bulk potential as demonstrated later.

Some designs [130] have proposed making use of the fact that the electrode-electrolyte interface itself acts as a large capacitor in parallel with large resistance when a polarisable electrode is used. This proposes biasing the input node by a sub-threshold transistor providing large small-signal resistance and, therefore, effectively acting as a pseudoresistor. This has the advantage of removing the need of an input DC-blocking capacitor and therefore reducing the needed amount of area but creates uncertainty around the actual position of the cut-off frequency

due to instability of the electrode impedance itself. In addition, the direct connection of the electrode to the drain of a transistor creates a potential safety risk in case of failures.

2.4.3 Digitisation

Although there are examples of fully analogue designs making use of an analogue transmitter such as [131; 132] employing an FM modulator, it has lately been a trend to employ an ADC inside the implant allowing for digital wireless transmission of the acquired data or additional processing in the digital domain. This has the advantage of simplifying further transmission and processing as well ensuring that the signal is not subjected to further addition of noise in the communication channel. Although there are countless ADC topologies available, the nature of requirements of neural implant circuits such as the handling of low frequencies, limited area and limited power budget result in a handful of topologies being particularly popular.

While it is possible to find examples of circuits that quantise both LFP and EAP at the same time, this is often not desirable because of the need for a larger dynamic range of approximately 60 dB resulting in an Effective Number of Bits (ENOB) of approximately 10 bits. To this end, many designs employ band-pass filters that divide the signal into respective frequency band which can then be quantised individually, thus reducing the required ENOB. If the aim is the acquisition of neural spikes for further processing by spike sorting, ENOB can be reduced to as low as 5 bits [133; 134].

Those properties have led to a particular popularity of Successive Approximation Register (SAR) ADCs that operate on the basis of sampling the input by storing its potential on a holding capacitor and continually dividing it by 2 for each bit of resolution required. Since each conversion requires at least one clock cycle for each resolution bit, this topology is suitable for digitisation of low-frequency signals such as LFPs and EAPs. An example of a complete system of 100 recording channels making use of an SAR ADC can be found in work of R. R. Harrison [135]. The simplicity of SAR ADCs allows for implementations of particularly impressive power consumption, such as [136] implementing a 160 nW ADC operating at a sampling rate of 25 kHz and a resolution of 9 bits.

To allow for comparison between various ADC topologies relating their performance to power, we define a Figure of Merit (FOM)

$$FOM = \frac{P}{2^{ENOB} \times BW} \tag{2.24}$$

where P is the consumed power and BW the quantised bandwidth. The result is given in J/conversion, or more typically pJ/conversion, indicating the energy consumed per every quantisation level and sample produced. In Nyquist-rate converters, such as SAR ADC, the bandwidth would be defined as a half of the ADC's sampling rate.

Recently, the emerging new generations of neural implants have also started exploring alternative methods to Nyquist-rate conversion. This includes over-sampling converters such as Sigma-Delta ($\Sigma\Delta$) ADCs making use of a low-resolution quantiser digitising the input signal at a sampling rate significantly higher than the Nyquist rate while at the same time shaping the quantisation noise into out-of-band frequencies. The low-resolution digital signal is then filtered to remove out-of-band components and downsampled allowing for an increase of its resolution. Those converters are typically superior when it comes to achieved dynamic range. In addition, the low requirements placed on the internal quantiser mean that a larger portion of this topology lies on digital processing and therefore better benefits of scaling of feature sizes in modern CMOS processes. More details about $\Sigma\Delta$ ADCs as well as an example of a practical implementation are going to be covered in Chapter 6.

Another alternative to Nyquist-rate converters that are also suitable for the quantisation of neural signals are so-called Continuous-Time (CT) converters. Rather than sampling the signal at a fixed sampling rate, those converters react to changes in the signal and report a significant change resulting in the instantaneous sampling rate following the spectral content of the input signal. This makes the method particularly interesting for quantisation of neural signals (especially EAPs) due to their sparsity. The principle is going to be further explored in Chapter 3 alongside examples of implementations.

2.5 Summary

This chapter has presented a simplified model of an electrode-electrolyte interface, presented its components and explained how they relate to physical properties of electrodes. This has been used to analyse the sources of noise in a recording electrode in addition to steps needed for its reduction. The gained understanding is useful in better comprehension of the requirements for the design of analogue front-ends.

In addition, the presented analysis has led to identification of Niobium as a promising material for creation of neural recording electrodes whose high exchange current density results in smaller amount of noise in LFP and EAP frequency bands. To verify the validity of the claim, an experiment has been conducted measuring the impedance of Pt and Nb microwire electrodes. This has revealed that the use of Nb results in the expected impedance profile proving that it is a more polarisable material than platinum in PBS.

A more advanced experiment would however be needed to directly show that the use of the material leads to a reduction in the amount of noise. This would require the manufacturing of Nb and Pt micro-electrodes of the same area connected to a low-noise amplifier. This is challenging from the point of view of manufacturing the electrodes and depositing the different materials and is outside of the scope of this project and left for further research.

Finally, a short overview of analogue front-ends and challenges their implementations are facing has been presented including some examples of solutions found in literature. This is going to be followed up by an in-depth exploration of the problematics of CT and $\Sigma\Delta$ conversion in upcoming chapters alongside presentation of practical circuit implementation and results. A short summary of commonly used AFE topologies outlining their advantages and disadvantages can be seen in Table 2.3. While the separation between an AFE and a subsequent ADC can often be blurred, such as in the case of DC-Coupled AFEs with a digital servo loop, a table comparing typically employed ADC topologies can be seen in Table 2.4. Additional overview of popular AFE and ADC topologies employed in neural acquisition can be seen in [118], a previously published book chapter addressing this problematic.

Topology	Examples	Advantages (+) & Disadvantages (-)
Conventional AC-Coupled	[115; 137]	+Safety +Reliability +Design Control +Linearity -Large External Capacitors
Harrison's Amplifier (Pseudoresistor-based)	[135; 138; 139]	+No External Components -Limited Linearity [123] -Limited Reliability [125]
DC-Coupled (Servo Loop, GmC Filters, Switched Capacitor, Continuous Time, $\Sigma\Delta$)	[32; 126; 114; 129]	+No External Components +Design Control +Linearity +Superior Input Impedance +Reliability -More Complex Design

Table 2.3: Brief Comparison of Analogue Front-End Topologies.

Topology	Examples	Advantages (+) & Disadvantages (-)
SAR	[135; 136]	+Power Consumption -Limited Resolution ($\approx$ 9-12[140] bits) -Component Matching Dependent
Single-Slope	[83; 82]	+Compact Area -Limited Resolution
$\Sigma\Delta$	[141; 142; 126; 32; 80], Chapter 6	+Superior Resolution (Up to $\approx$24 bits) +Benefits from Technology Scaling +Superior Dynamic Range -Complicated Implementation
Continuous Time (CT)	[143; 144; 145; 146; 147], Chapters 3 and 4	+Activity-Dependent Power Consumption +Inherent DC Rejection Possible -Subject to Time Drift -Oversampling

Table 2.4: Brief Comparison of Analogue to Digital Converter Topologies.

Chapter 3

Continuous Time Acquisition of Neural Signals

The work presented in this chapter builds on a circuit that was designed during previous studies as a part of an MEng final year project. While the presented circuit was designed before starting the PhD studies, all presented measurements and results, as well as novel theory related to CT sampling are a result of PhD work. Results presented herein have been previously published in [148] and [147].

3.1 Introduction

This chapter is going to cover the problematic of continuous-time (CT) sampling, a method that has recently caught the attention of the neural implants community as an alternative sampling scheme to the, otherwise, almost universally used discrete-time (DT) sampling. When DT sampling is used, the signal is sampled at fixed periods of time, termed the sampling period T_s, the reciprocal of which is called the sampling frequency or sampling rate f_s.

If this is done at a sufficiently high frequency and a sample of the input signal is obtained at a frequency equal to twice the frequency of the highest-frequency component in the signal, no information is lost and the signal can be perfectly reconstructed from the samples. This is, of course, a result of the well-known Nyquist theorem, first presented by Harry Nyquist in

1928 [149] and independently by other authors around the same time, such as V. A. Kotelnikov in 1933 [150].

While this principle has seen widespread use in every aspect of our modern lives, such as the digitisation of music, video and any other signal imaginable, it has a limitation in its assumption of signals being of time-invariable frequency spectrum and therefore of constant bandwidth. It can, however, easily be seen that this is not the case in a large amount of biological signals, including the EAPs that exhibit long periods of silence interrupted by occasional spikes. If DT sampling is employed, the signal is significantly oversampled during the quiet periods, while the high sampling rate is only needed when a spike is present.

3.1.1 Non-Uniform Sampling

If we want to achieve a more efficient sampling scheme, it is necessary to start exploring methods that sample the input signal at irregular intervals, thus leading to non-uniform sampling. Some of the earliest work on the theory of that can be found in a publication by H. J. Landau [151] of 1967, which has generalised the Nyquist theorem to such cases. It says that the signal is still reconstructable without loss of information if at least the average sampling rate is twice the frequency of the highest-frequency component.

This still, however, assumes that the signal remains of constant spectrum that does not change over time. The problem of sampling a signal, whose spectrum changes over time has been studied by K. Horiuchi [152] who has proposed an alternative sampling scheme following the spectral content of the signal. The author however agrees that the presented scheme might not be practical unless the future changes of the spectrum are known in advance.

This brings us to a problem of determining the instantenous spectral content of a given signal. Indeed, if it was possible to know the instantenous spectral content of a signal, it would be possible to simply adjust the sampling rate such that it is always equal to twice the highest-frequency of the signal. Such an approach is however impossible as the notion of instantenous spectrum or instantenous bandwidth is fundamentally incorrect. In the traditional sense, the

bandwidth of a signal is based on the Fourier transform of $F(\omega)$ of signal $f(t)$ given as:

$$F(\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \tag{3.1}$$

the solution of this integral, however, requires the knowledge of the signal for its entire duration going into the future. It can also be seen that $F(\omega)$ is independent of time and therefore does not permit any time variation of the signal's spectrum.

To alleviate this problem, we can multiply the signal by a window, only reducing the time of interest to a fixed period:

$$F(\omega, \tau) = \int_{-\tau_w/2}^{\tau_w/2} f(t)w(t-\tau)e^{-j\omega t}dt \tag{3.2}$$

where τ_w is the width of the window, if it vanishes. Such a transform is termed Short-Time Fourier Transform (STFT) and allows an estimation of the signal's spectrum at a specific point in time. Many examples of potentially used windows can be found in the literature. One example of such is a Gaussian window giving rise to Gabor transform [153] defined as:

$$F(\omega, \tau) = \int_{-\infty}^{\infty} f(t)e^{-\pi(t-\tau)^2}e^{-j\omega t}dt \tag{3.3}$$

Although the used Gaussion function does not completely vanish in time, it rapidly diminishes and therefore its use makes the contribution of the signal's behaviour far away from the observed instant increasingly irrelevant. The STFT can, however, be alternatively viewed as finding the Fourier transform of the original signal multiplied by the window. Multiplication by a window in time domain results in convolution in frequency domain and therefore, if we denote the window's Fourier transform $W(\omega, \tau)$, the STFT can also be expressed as:

$$F(\omega, \tau) = F(\omega) * W(\omega, \tau) \tag{3.4}$$

This, however, means that the accuracy of the spectrum estimate is limited by the bandwidth of the window. If $F(\omega)$ contains a single tone, it is going to appear as a signal of twice the bandwidth of the window, resulting in uncertainty of the estimate. The only window that has zero bandwidth, and therefore leads to no uncertainty is $w(t, \tau) = k$, a constant infinitely long window. Such a window, however does not give any time selection and reduces the STFT to ordinary Fourier Transform. Conversely, if a window consisting of a single impulse in time is used, $w(t, \tau) = \delta(t - \tau)$, the resulting bandwidth is infinite and STFT is reduced to only obtaining the energy of the signal with no frequency resolution. Any window between the two extremes is going to lead to some resolution in frequency and some resolution in time but there is always a compromise between the two, meaning that instantenous bandwidth can not be known.

This problem has been observed by D. Gabor in 1946 [153] which has resulted in the notion of Gabor uncertainty, stating the product of standard deviation of frequency and time, σ_f and σ_t, respectively, is limited by:

$$\sigma_f \sigma_t \geq \frac{1}{4\pi} \tag{3.5}$$

This result is fascinating as it is analogous to that of the Heisenberg uncertainty principle despite covering an entirely different problematic, the bandwidth of signals being a purely mathematical construct, while the behaviour of particles a physical one.

Having demonstrated that it is not in principle possible to devise a sampling scheme that would ideally adapt its sampling rate to the instantaneous spectral content of the input signal without knowing the signal wholly in advance, we can ask ourselves, whether it might be possible to devise a practical sampling scheme that would adapt the sampling rate to the signal's bandwidth at least to some extent. The relationship of Inequality 3.5 suggests that this might be possible if we relax the requirements on ideality of the scheme. To that end, we can accept that the sampling rate might follow a relationship:

$$f_s(t) = k \times B(t), \tag{3.6}$$

where B(t) is the theoretical concept of instantenous bandwidth and k a constant that would be equal to 2 in an ideal scenario but has to be larger than 2 in a practical sampling scheme.

3.1.2 Introduction to Continuous-Time Sampling

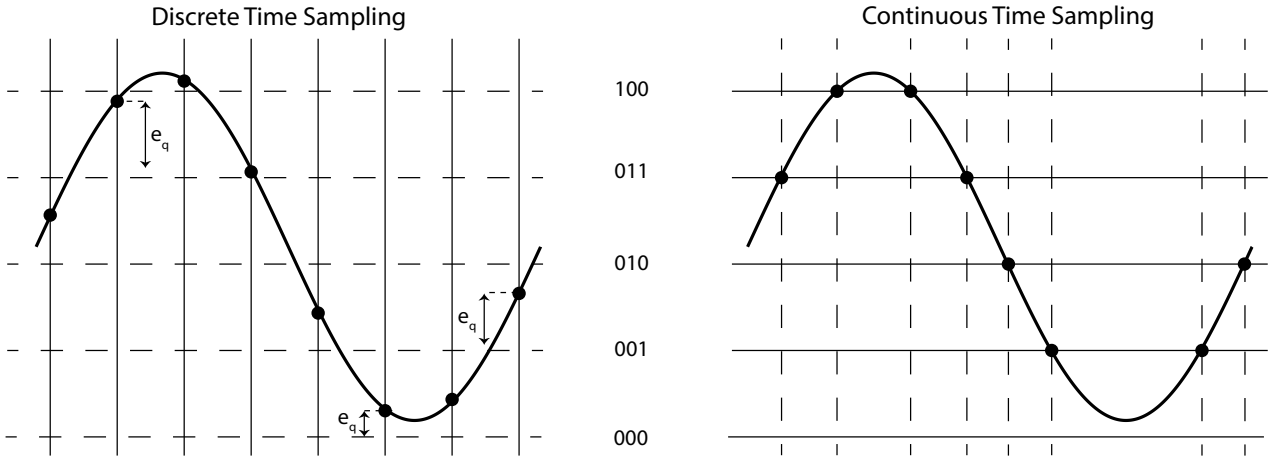

Figure 3.1: Demonstration of Discrete-Time (DT) Sampling (Left) and Continuous-Time (CT) Sampling (Right). Solid lines indicate the underlying driver of both sampling schemes - time in DT Sampling, quantisation levels in CT Sampling; e_q indicates the quantisation error present in DT sampling.

An example of a sampling scheme that has such properties can be found in Continuous-Time sampling. This, as illustrated by Figure 3.1 operates on the basis of detecting the input signal crossing a quantisation level and generating a sample precisely at that time, as opposed to Discrete-Time sampling that takes a sample at fixed periods of time. As seen in the example of Figure 3.1, the average sampling rate of such a scheme has to follow the bandwidth of the input signal. If a pure tone passes through N_q quantisation levels, it is going to be sampled $2 \times N_q$ times per the tone's period and, therefore the average sampling rate can be denoted:

$$\bar{f_s} = 2 \times N_q \times f_t \tag{3.7}$$

where f_t is the tone's frequency. It can be seen that this result takes the same form as Equation 3.6 at least for a pure tone and it can easily be seen that the relationship would hold for varying-frequency signals such as chirps as well. How this holds for other more complex signals is going to be explored later in this chapter.

While not as often employed as uniform sampling, the notion of CT sampling has been known for a long time under different names, often resurfacing as an interesting choice for new applications and alternative solution to various engineering problems. Perhaps one of the earliest mentions comes from 1966 when H. Inose et al. [154] called it "Asynchronous delta modulation" and proposed it as an alternative to uniform sampling of digital signals that might lead to more efficient transmissions. The scheme is reviewed again by J. Mark and T. D. Todd [155] who refer to it simply as "Nonuniform sampling approach". Additionally, Sayiner et al. [156] referred to it as "Level-crossing sampling" in 1996 and finally Y. Tsividis [157] calls it "Event-driven sampling".

Apart from introducing a sampling rate following the bandwidth of the input signal, CT sampling comes with additional advantages when compared to DT sampling. A CT sampler is essentially a signal-to-time converter as the signal is translated into intervals between individual quantisation level crossings. This brings an advantage in that the level-crossing can be encoded by a single bit determining whether the quantisation level was crossed upwards or downwards, as opposed to DT sampling requiring N bits per sample. Additionally, it is often claimed [158] that CT sampling does not result in addition of quantisation noise to the signal. This can be seen demonstrated in Figure 3.1, where the quantisation error in DT sampling is denoted e_q. Such an error is not created in a CT sampling process because samples are always taken whenever the signal crosses a quantisation level and therefore no error can be present by definition.

This is arguably unfair because in a DT sampling process, the signal is quantised both in time, due to the fixed sampling rate, as well as in value by the employment of a quantiser. In a CT sampling process, quantisation only occurs on the value of the signal, while time remains unquantised. If the time between samples was quantised, an error would arise the same way

it does in DT sampling. This is, however, often not required as analogue time value can be transmitted significantly easier and subject to less distortion than an analogue amplitude. It is, for example, possible to imagine a Code-Division Multiple Access (CDMA), or other spread-spectrum transmitter asynchronously transmitting pulses. The main advantage is that the time difference between two pulses can be allowed a dynamic range ranging from less than a nanosecond to any extended period of time, thus significantly superior to the dynamic range afforded to voltage signals.

3.2 Aliasing in Continuous-Time Sampling

Similarly to the claim that a CT-sampled signal is not subject to quantisation noise, it is common to find claims in literature [157] saying that a CT-sampled signal is not subject to aliasing because the sampling frequency follows the bandwidth of the signal. As we have demonstrated before, this is the case for a certain group of signals, but we will show a counter-example that disproves this statement and will formulate a proposition, the satisfaction of which, will guarantee that the signal is not subject to aliasing.

Let us consider two signals $y_1(t)$ and $y_2(t)$:

$$y_1(t) = \sin(0.7 \times 2\pi t) + 0.4\sin(0.2 \times 2\pi t) \tag{3.8}$$

$$y_2(t) = 0.4\sin(0.7 \times 2\pi t) + \sin(0.2 \times 2\pi t) \tag{3.9}$$

and let us evaluate a scenario under which the signals are sampled by a CT process of a quantisation level size $\Delta_q = 1.4$ and ideally reconstructed to form signals $y_r^1(t)$ and $y_r^2(t)$. Those can be seen plotted in Figure 3.2 demonstrating that the reconstruction $y_r^1(t)$ of $y^1(t)$ is correct, while the reconstruction $y_r^2(t)$ results in a signal different from $y_2(t)$ due to aliasing, thus disproving the common claim that continuous sampling always prevents the occurrence of aliasing.

It can be be seen that while the process resulted in 21 samples taken during a period of 10

seconds in the case of $y_1(t)$, only 13 samples were taken in the case of $y_2(t)$. This corresponds to average sampling rates of 2.1 Hz and 1.3 Hz respectively. Since both signals contain two components at 0.7 Hz and 0.2 Hz, the average sampling rate of 2.1 Hz is sufficient, while 1.3 Hz is not. It is interesting to observe that as the average sampling rate changes in various stages of the process, so does the aliased image and it no longer holds that an image of a pure tone is a pure tone of smaller frequency as in DT sampling. Observing Figure 3.2, it can be seen that the signal can be reconstructed in the first second, due to the higher amount of samples taken, but no longer after that, demonstrating that the frequency of the image changes.

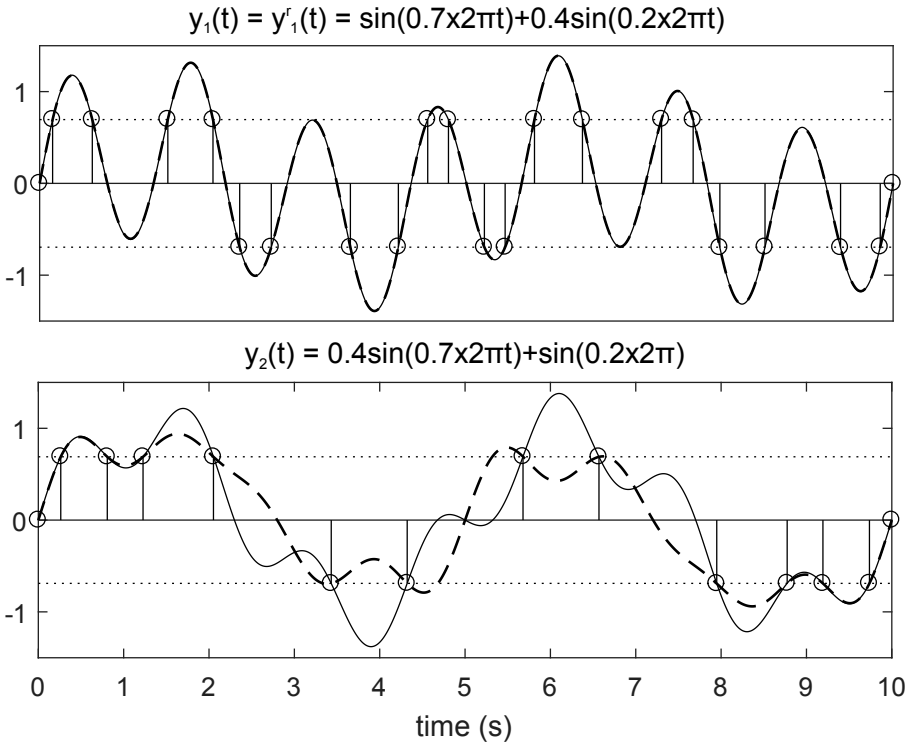

Figure 3.2: Plots of signals $y_1(t)$ and $y_2(t)$ (solid), samples obtained by CT sampling (circles), quantisation levels (dotted) and reconstructed signals $y_1^r(t)$ and $y_2^r(t)$ (dashed) illustrating aliasing occurring when $y_2^r(t)$ is reconstructed. Previously published in [147]

To understand this, let us consider the properties of the signal that give rise to its average sampling rate under CT sampling. As shown by Equation 3.7 and demonstrated by Figure 3.2, the oversampling ratio depends on the ratio of the signal's amplitude and the size of one quantisation level. The smaller the quantisation level is, the larger the oversampling factor becomes. In an extreme scenario, we can consider the case when only one quantisation level is employed, thus reducing the sampling to zero-crossing detection. In the case of a pure tone, this would lead to the average sampling rate exactly equal to the Nyquist rate and would therefore

result in maximally efficient sampling.

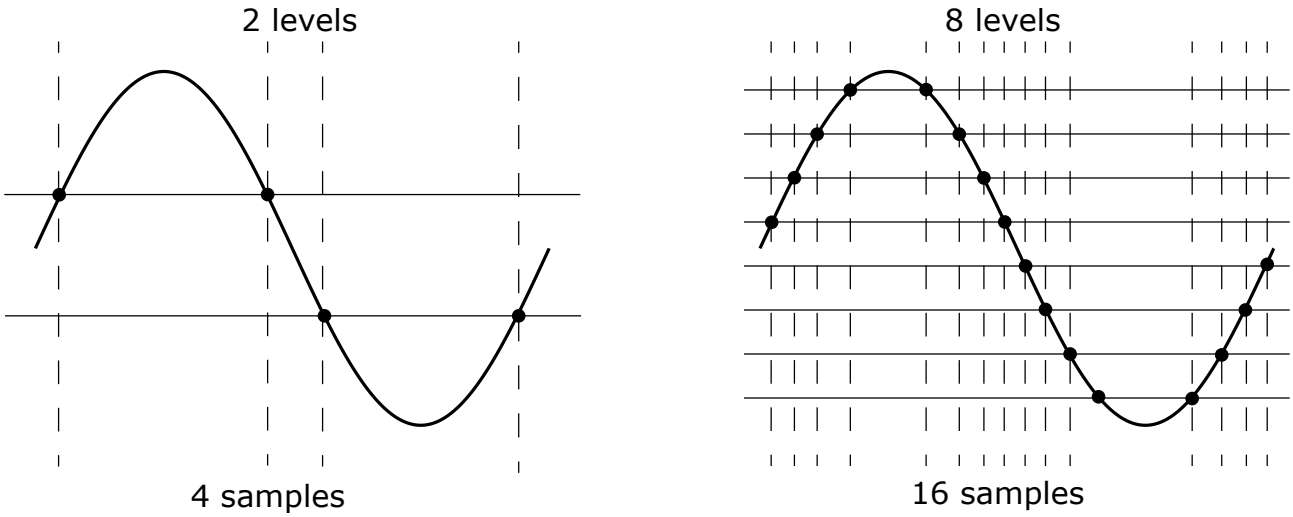

Figure 3.3: Illustration of oversampling property of CT Sampling Process - 2 Quantisation levels lead to oversampling by a factor of 2, 8 levels lead to oversampling by a factor of 16. Previously published in [147], modified.

It can, however, easily be seen that adding another signal of higher frequency and smaller amplitude on top of the pure tone will result in an insufficient amount of zero crossings and therefore aliasing. Formulating a minimal condition that has to be satisfied to prevent aliasing in CT sampling, analogous to the Nyquist theorem is however very difficult, if not impossible, as it would require knowing the average amount of zero crossings at each point in time for each signal. While such a result can be obtained for some signal classes, such as Gaussian processes [159], it is in general difficult to obtain a generic result applicable to all signals [160].

It is, however, possible to formulate a sufficient condition that when satisfied guarantees that the quantised signal will not be subject to aliasing:

Proposition 1 *A bandlimited signal sampled by a CT sampling process is going to be free of aliases if the input signal is band-limited and its highest-frequency content has a peak-to-peak amplitude of at least the size of a quantisation step.*

To show that this is the case, we note that every real signal $s(t)$ can be expressed in terms of its Fourier transform $S(\omega)$, that can be further expanded to a sum of an infinite amount of components, each one being a pure tone:

$$s(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S(\omega)e^{j\omega t}d\omega = \lim_{\delta\omega\to 0}\sum_{n=-\infty}^{n=\infty} a_n cos(n\delta\omega t + \phi_n) \tag{3.10}$$

Since any two tones of differing frequencies are orthogonal to one another, the highest-frequency tone larger than the size of a quantisation step must on its own result in a sufficient amount of quantisation level crossings guaranteeing that the tone is sampled at at least the Nyquist rate and also meaning that any other component at smaller frequencies can not be subject to aliasing.

3.3 Continuous-Time Sampling for Biological Signals

Having introduced the CT sampling process as a concept and having explored some of its basic properties, we can investigate its behaviour when used for quantisation of biological signals. To this end, we would mainly like to understand whether CT sampling can potentially be beneficial for the digitisation of signals of interest in terms of reduction of the amount of resources needed.

As previously discussed, one of the greatest limitations of DT sampling is the fact that the sampling rate remains fixed, introducing a significant disadvantage for the quantisation of signals that have varied spectral content throughout time such as many classes of biological signals. To investigate how significant this effect is, let us consider signals such as ECG, EEG, LFP and EAP and observe how their spectral content changes over time.

While it is not possible to precisely know the bandwidth of the investigated signals at any point in time due to Gabor uncertainty, we can obtain an estimate in line with the limit given by the relationship. To estimate the bandwidth we use continuous-time wavelet transform (CWT) employing Morse wavelets [161] of symmetry and decay parameters $\gamma = 3$ and $\beta = 60$ respectively. This results in an estimate of spectrum $S_w(a, b)$, where a and b respectively denote the translation and scale of the wavelet, corresponding to time and frequency. To estimate the instantaneous bandwidth we apply thresholding on $|S_w(a, b)|^2$ such that the estimated bandwidth of the signal is defined as the highest frequency bin above the threshold T_s

defined as $T_s = \mu_S + 3\sigma_S^2$ where μ_S and σ_S^2 are the mean and variance of the spectrum energy function$|S_w(a,b)|^2$, such that T_s acts as an estimate of the signal's noise floor.

Sample ECG and EEG signals have been obtained from [162] and [163] respectively using an online database [164]. The used EAP and LFP signals are based on a simulated neural signal, filtered respectively by a high-pass and a low-pass filter of sharp 300 Hz cut-off. The obtained estimated spectrum for sample signals can be seen plotted in Figure 3.3. This demonstrates that various biological signals show varying levels of spectrum non-stationarity. In the case of ECG, it can be seen that the majority of the signal's spectral content is concentrated around the occurrence of each QRS complex, while the bandwidth decreases during quiet periods. This is even more prominent in the case of EAP signals that exhibit large spikes in bandwidth whenever a neural spike occurs, while remaining quiet throughout the remainder of time. It can be seen that EEG and LFP, on the other hand, remains relatively stationary. The spikes seen in the spectrum of LFP are caused by remnants of EAP spikes that were not completely removed by the filter. The stationarity of LFP and EEG, a temporally and spatially filtered image of LFP, is fully expected as, as those signals are well known to exhibit a stable 1/f power spectral density (PSD) profile [165].

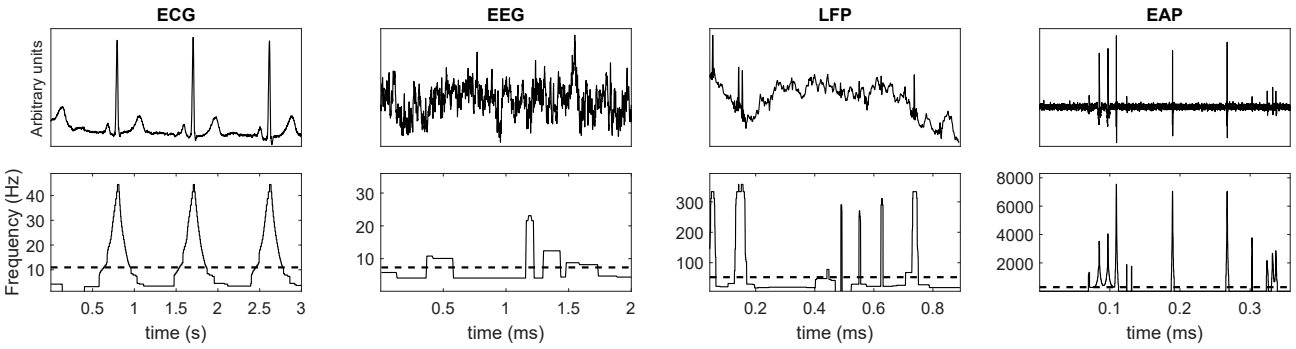

Figure 3.4: Illustration of spectral content changes in chosen examples of biological signals (ECG, EEG, LFP, EAP). Previously published in [147].

To assess the potential savings achieved by a non-uniform sampling scheme as opposed to uniform sampling, we calculate the average and maximal bandwidth, denoted B_{avg} and B_{max} based on the estimate described above. We can then define a compression ratio C = B_{max}/B_{avg} estimating the proportion of samples that can be saved if a an ideal non-uniform sampling is used as opposed to uniform Nyquist rate sampling. The obtained values can be seen in

Table 3.1.

	ECG	**EEG**	**LFP**	**EAP**
Maximal Bandwidth f_{max} (Hz)	51.07	40.24	357.52	7548.09
Average Bandwidth f_{avg} (Hz)	10.97	7.32	52.38	289.46
Compression Ratio C	4.65	5.49	6.8	26.3

Table 3.1: Summary of biological signals' bandwidth. Previously published in [147].

This demonstrates that, as expected, significant savings can be achieved during the quantisation of neural spikes when non-uniform sampling is used. The estimated compression ratio of 26.3 is a significant result that can potentially lead to an ADC power consumption reduction by the same factor, in addition to savings in transmission of the data if no further compression is used. There are examples of circuits in the literature that make use of this EAP property by increasing the sampling rate when a neural spike is detected. An example of such can be found in [46].

To consider the effectivity of CT sampling when applied for the quantisation of EAP signals, we simulate a CT sampling process, whereby the size of a quantisation step is set such that the peak-to-peak magnitude of the signal passes through 8 bits (256 steps). The obtained amount of samples and hence the instantaneous sampling rate can be seen plotted in Figure 3.5.

This shows that the average sampling rate follows the estimated bandwidth of the signal. The same experiment has been performed on a longer portion of the sample signal than what is visible in Figure 3.5 and a correlation of $\rho \approx 0.71$ was found between the two metrics. This confirms that CT sampling leads to a sampling rate that is adaptive to the spectrum of the signal. The average sampling rate for the sample signal was found to be ≈ 25.9 kHz. This on its own is higher than what is needed for quantisation of the signal if its average bandwidth is 289.5 Hz as seen in Table 3.1.

As shown before, the introduction of finer quantisation steps, however, reduces the occurrence of aliasing but at the same leads to oversampling of the signal. Since an 8-bit quantiser was applied, the signal is going to be subject to oversampling by a ratio of 256. Correcting for the oversampling, the signal would have therefore been sampled at a rate of ≈ 101 Hz, which is not

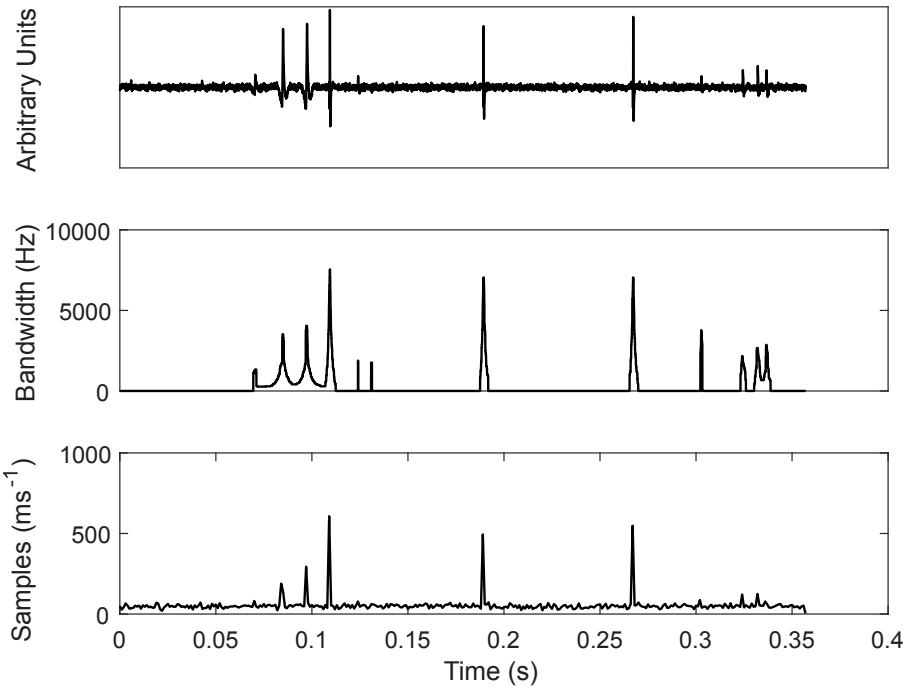

Figure 3.5: Top: Sample EAP Signal, Center: Estimated Bandwidth, Bottom: Instantenous sampling rate of a CT sampling process. Previously published in [147], modified.

sufficient.

This is caused by the fact that the signal does not employ the full dynamic range of the quantiser at all the time. If we instead measure the average peak-to-peak swing of the signal, where the peaks are the highest peak between two zero-crossings and the lowest trough between the subsequent two zero-crossings, we obtain an average swing of ≈ 7.37 quantisation levels. This would mean that the signal could be downsampled to an average sampling rate of ≈ 25.9 kHz / $7.73 \approx 3.35$ kHz. Considering the maximal bandwidth of EAP was found to be 7.5 kHz, uniform sampling would require a sampling rate of at least 15 kHz.

This shows that, in theory, a reduction of the sampling rate by a factor of ≈ 5 can be achieved when CT sampling, as opposed to uniform DT sampling, is used for the quantisation of EAP. Admittedly, several assumptions and estimates have been used to arrive at this result and the factor of 5 might not seem significant enough. However, as is going to be demonstrated in the subsequent section, the construction of a CT ADC can be comparably simpler than that of a conventional ADC, leading to additional savings both in terms of power, as well as area.

3.4 CT ADC Implementation

Having considered the effect of using a CT ADC for the quantisation of some classes of biological signals, we can consider practical implementations of ADCs and demonstrate their behaviour during acquisition of those signals, further identifying additional advantages of using this approach. There are several examples of prior implementations found in the literature, such as [143; 144; 145; 146].

The ADC is typically implemented using a pair of two continuous-time comparators, detecting when the input signal crosses a quantisation level followed by an accumulator, reconstructing the full N-bit value of the quantised signal. This is then fed back to the input to generate potentials of the two quantisation steps that are closest to the input signal. The methods used to achieve this vary between implementations and the most traditional ones employ the use of a complete N-bit DAC [146; 143] coming at a cost in terms of the used area as well as power consumption needed to generate a DAC output during each step.

Alternatively, [144] presented a solution relying on a capacitive array injecting an offset to the input signal that generates an output in the range of V_L and V_H, where V_L and V_H denote the voltage of a lower and upper quantisation level threshold. This means that the output of the capacitive array can be directly compared to V_H and V_L that are fixed, thus alleviating the need for a full N-bit DAC.

A very interesting solution has been presented in [145] which has implemented a CT quantiser based on an integrator, in a similar fashion to a CT unclocked Sigma-Delta ADC. The input signal is applied to the input of an integrator, the output of which is compared to two fixed thresholds that give rise to the upper and lower quantisation levels. If a quantisation level is crossed, the input to the integrator is inverted using a pair of switches and its output begins to move in the other direction. The employment of an integrator additionally adds the effect of shaping the quantisation noise, similarly to $\Sigma\Delta$ converters which leads to achievement of very impressive FOMs, not previously achieved by other CT sampling converters but sacrifices some properties achieved by other CT ADCs.

The employment of an integrator leads to the output of the ADC detecting quantisation level crossings of the integral of the input signal, rather than crossings of the signal itself. While having the advantage of shaping the quantisation noise and paving a way to a very elegant implementation, this results in the sampling rate becoming dependent on the DC offset of the input signal, due to its integration, resulting in consumption of additional energy and thus making such an approach difficult to use for the quantisation of signals acquired using electrodes operating in electrolytes introducing DC offsets.

3.4.1 Charge-Based Topology Implementation

An alternative topology that we have first presented [148] in a 2017 ISCAS conference can be seen in Figure 3.4.1. This alleviates the need for a full N-bit DAC in addition to only using a single comparator, thus making the implementation very simple and compact. This operates on the basis of reconstructing the quantised version of the input on a capacitor C_b connected to the inverting input of the comparator. If the input signal rises, the output of the comparator increases as well. This is used as an input to a threshold crossing detector that determines when the difference between the potential at C_b and the input voltage exceeds a certain threshold detecting the a crossing of quantisation level either up or down.

The threshold crossing detector is implemented using two CMOS inverters employing differently sized transistor pairs, leading to two different switching points. When one of those is crossed, a pulse generator is triggered, generating a pulse of length t_p that acts as an output of the ADC while also triggering a charge pump or sink of current I_s, adding or removing charge $I_s \times t_p$ to or from C_b. This results in the shift of the potential at C_b by one quantisation level, thus allowing the circuit to detect the next level crossing.

It is of course difficult to ensure the equality of charge $q^{up} = I_s^{up} \times t_p^{up}$ and $q^{down} = I_s^{down} \times t_p^{down}$ that is added and removed during a detected quantisation level crossing up and down respectively. To tackle this problem, the circuit contains configurable length pulse generators, allowing the tweaking of t_p^{up} and t_p^{down}. While this can to some extent alleviate the mismatch between q^{up} and q^{down}, it does not lead to a complete removal of the mismatch with the design

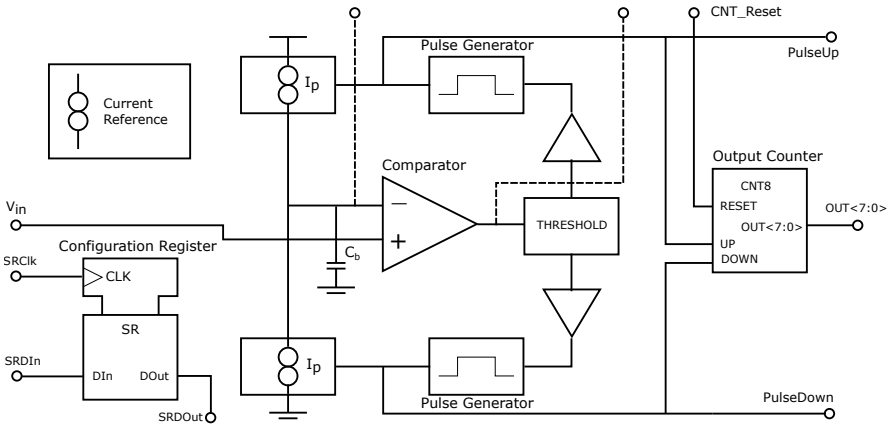

Figure 3.6: Block diagram of a CT ADC implementation. Previously published in [147].

allowing its correction to within approximately a half of one least significant bit (LSB). Any residual mismatch results in addition of a slope to the quantised signal that can easily be removed in post-processing without an adverse effect on the ENOB. The configuration of the pulse lengths, alongside other parameters such as the magnitude of I_s and the thresholds of the crossing detectors is stored in an internal shift register.

To help in understanding of the circuit's operation, some internal signals as well as outputs of the system can be seen in Figure 3.4.1 demonstrating its operation during the conversion of a pure tone. This shows V_b, the potential of C_b, demonstrating the quantised signal alongside the output of the comparator, V_{comp} and spike-domain outputs UP and DOWN indicating a crossing of a quantisation level up and down respectively.

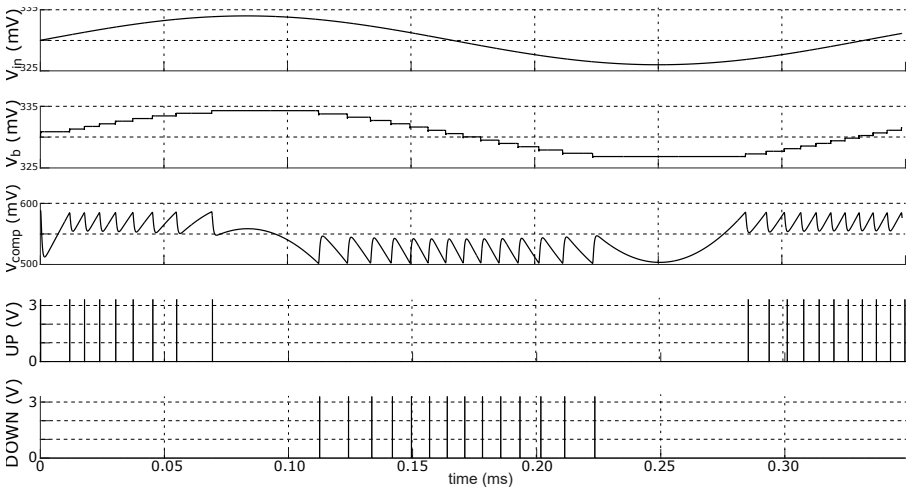

Figure 3.7: Simulated output and some selected internal signals of the proposed ADC when applied for digitisation of a pure tone. Previously published in [147].

Arguably, the circuit can be reduced to a single component that gives rise to static power consumption, the comparator. This has to be designed such that the induced delay is short enough to allow the loop of the circuit to settle before another quantisation level crossing can occur. The comparator therefore must be designed with a sufficient bandwidth to ensure that this condition is met. The principle of operation of this circuit means that it is not limited by the bandwidth of the input signal but rather by its slope, or slew rate. This is due to the fact that the circuit can only detect a finite amount of quantisation level crossings in a fixed amount of time, giving rise to a maximal slope.

If the input signal has a slew rate of SR_{in} and the quantiser is designed for a full-dynamic-range resolution of N bits and a peak-to-peak input range of 2A, the allowable maximal delay t_d^{max} can be denoted as:

$$t_d^{max} = \frac{A}{SR_{in} \times 2^{N-1}} \tag{3.11}$$

Assuming that the settling time of the comparator is approximately equal to three time constants, the required bandwidth can be expressed as $B_c \approx 3/2\pi t_d$. Combining this with Equation 3.11 results in the required comparator bandwidth:

$$B_c > \frac{3SR_{in} \times 2^{N-1}}{2\pi A} \tag{3.12}$$

However, since it is a standard practice to design circuits based on the bandwidth of the signals of interest, rather than the slew rate, we can obtain an estimate for the needed bandwidth assuming the worst-case scenario. For an ADC of a 3-dB bandwidth of B_{ADC} and the same peak to peak input range of 2A, this would be a pure tone of frequency B_{ADC} and amplitude $A/\sqrt{2}$. Such a signal has a highest slew rate of $2\pi B_{ADC} A/\sqrt{2}$ and therefore substituting to Equation 3.12 yields:

$$B_c > \frac{3B_{ADC} \times 2^{N-1}}{\sqrt{A}} \tag{3.13}$$

It however has to be noted that the specific behaviour of the presented CT ADC topology means that a design for a target 3-dB bandwidth using Equation 3.13 will allow the quantisation of signals containing spectral content at frequencies higher than the bandwidth as long as the slew rate of the input signal does not exceed the highest slew rate of $2\pi B_{ADC}A/\sqrt{2}$. As will be demonstrated later, this allows the circuit to be implemented with less stringent bandwidth requirements when employed for acquisition of neural signals than what would be required in a typical 3-dB bandwidth-limited system.

As mentioned in the previous chapter, a challenge that neural acquisition systems often have to face is the need to implement a method of removal of any electrode DC offset. The advantage of the presented system is the fact that this is done inherently without the need for additional circuitry. Assuming the common-mode voltage range (CMVR) of the comparator is sufficient, any DC offset applied at the input will be quantised by the system and the potential of the offset will be reproduced at C_b, leading to its suppression. This will lead to generation of additional output spikes before the system reaches its steady state, thus leading to saturation or overflows of any output counter forming an N-bit output. This can, however, easily be resolved by resetting the counter once steady state is reached. Another advantage of this is the fact that the system is not susceptible to offsets caused by mismatch between components and those can therefore be implemented using very small CMOS feature sizes, if other adverse issues such as the addition of flicker noise are dealt with. As will be demonstrated in Chapter 4, this problem can be overcome as well.

3.4.2 Implemented Circuit Testing

The described circuit has been implemented and manufactured in a commercially available 0.35 µm ams CMOS technology and designed for a resolution of 8 bits at a peak-to-peak input voltage of 100 mV and operating from a supply voltage of 1.5 V. The core occupies a compact area of 320 µm × 360 µm as seen in Figure 3.4.2. To allow acquisition of neural signals, the circuit was designed for a target bandwidth of 4 kHz. While this might appear smaller than what is needed for acquisition of EAPs, simulations on pre-recorded neural signals have shown

that the corresponding slew rate is sufficient.

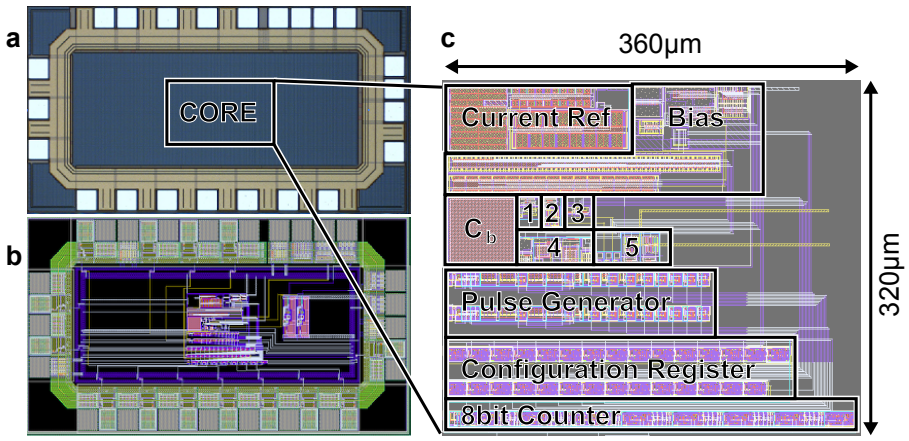

Figure 3.8: a) Microphotograph of the manufactured circuit, b) The layout of the circuit exported from Cadence Virtuoso, c) Close-up of the circuit's core; 1 - Input Comparator, 2 - Unity Gain Buffer, 3 - Threshold Crossing Detector, 4 - Charge Injection Circuits, 5 - Debugging Voltage Followers. Previously published in [147].

Once manufactured, the circuit was tested using a platform based on an NXP Freedom-K64F development board containing a K64F ARM-based controller and a UART-to-USB converter allowing control of the tested circuit from a PC by means of configuring its internal shift register setting properties such as pulse lengths used to charge capacitor C_b. The analogue input is passed to the circuit using a BNC connector through an optionally disable-able filter removing the input DC offset and instead adding an artificial offset controlled by one of the two resistive trimmers on the board. The second trimmer is used to configure the core supply voltage of the system.

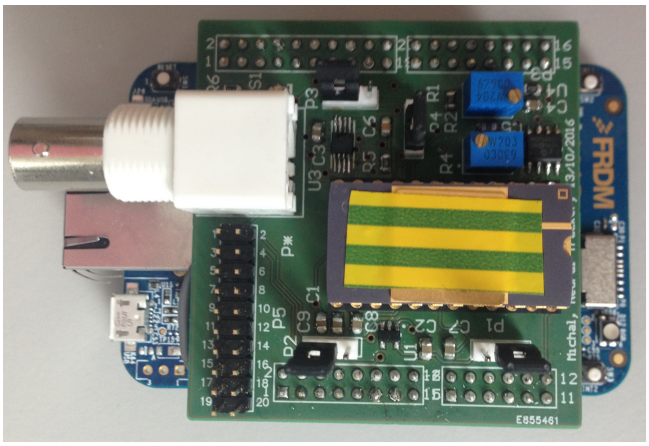

Figure 3.9: Photograph of the platform used to test the manufactured CT ADC.

The aim of the conducted testing was to determine the performance of the circuit giving rise

to standard metrics such as power consumption, ENOB and the verification of some of the properties of CT sampling ADCs, especially their activity-dependent power consumption. The power consumption has been first measured using an Agilent N6705B Modular DC Power Analyzer and was found to be 3.75 µW when no input was present. Based on simulated results, this can be broken down to individual contribution of components as seen in Table 3.2. This demonstrates that the power consumption is dominated by the input comparator and its unity-gain buffer that has been employed to limit the degradation in its bandwidth due to loading of its output by the threshold-crossing detector around its switching point amplified by the Miller effect. In addition, the measured power consumption is to some extend inflated by the employment of debugging voltage followers and a reference circuit that could respectively be omitted and shared across several recording channels if the circuit was employed in a neural implant. To further test the performance of the circuit, the input of the testing platform was

Component	**Power (µW)**	**Power (%)**
Input Comparator	1.9	41
Debugging Buffers	1.5	32
Comparator Buffer	0.75	16
Reference and Charge Injection	0.49	11

Table 3.2: Power consumption of individual components in the manufactured CT ADC.

connected to a Tektronix AFG3102 arbitrary signal generator and the spike-domain output signals UP and DOWN were recorded using a Salae Logic Pro 8 digital logic analyser sampling the outputs at a sampling rate of 100 MHz in addition to recording the power consumption. The signal generator was configured to produce a pure tone of frequency varying between 70 Hz and 4036 Hz and an amplitude set such that the signal passes through 256 quantisation levels (8 bits).

The acquired signal was then processed using a Matlab script that removed the mismatch between quantisation steps up and down and reconstructed the signal. The mismatch k_s between quantisation steps up and down, ΔV_{up} and $\Delta V_{down} = k_s \Delta V_{up}$, can simply be determined by observing the ratio of N_{up} and N_{down}, the amount of recorded steps in either direction in a signal of sufficient length. The signal is then reconstructed by calculating a cumulative sum of the signals DOWN and $k_s\times$ UP at the points where samples were taken, followed by spline

interpolation. The reconstructed signal was then used to obtain an estimate of the Signal to Noise and Distortion Ratio (SNDR) and the Spurious Free Dynamic Range (SFDR).

The obtained results can be seen plotted in Figure 3.10. This shows that, as expected, the power consumption of the circuit is activity dependent and rises linearly with increasing frequency of the input signal. The SNDR of the reconstructed signal reaches a maximum of 28.65 dB and SFDR of 38.8 dB at a frequency of 1794 Hz. The spectra of the reconstructed tones at 1794 Hz and 531 Hz can respectively be seen in Figures 3.11 and 3.12. Those results demonstrate the SNDR dominated by harmonic distortion in addition to flicker noise at small frequencies. The SNDR significantly decreases during acquisition of small frequency signals which is an unexpected result and therefore led to additional investigations based on simulations and measurements.

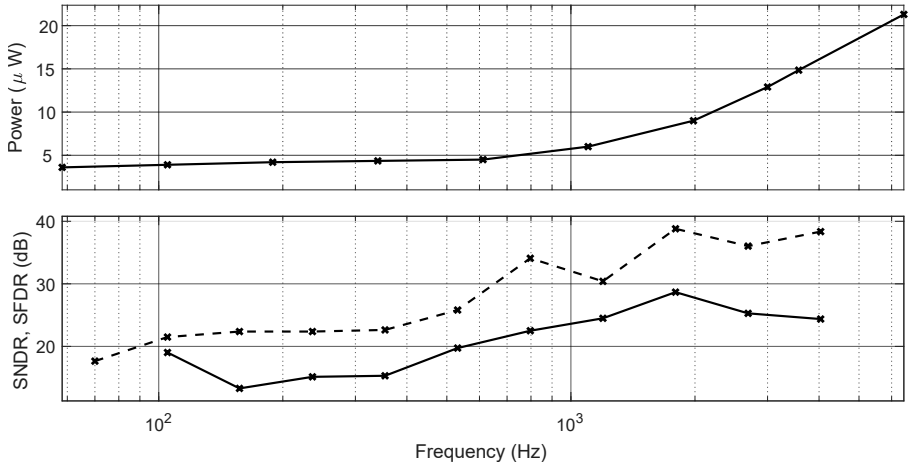

Figure 3.10: Top: Power, Bottom: SNDR (dashed), SFDR (solid) obtained during acquisition of a pure tone of varying frequency. Previously published in [147].

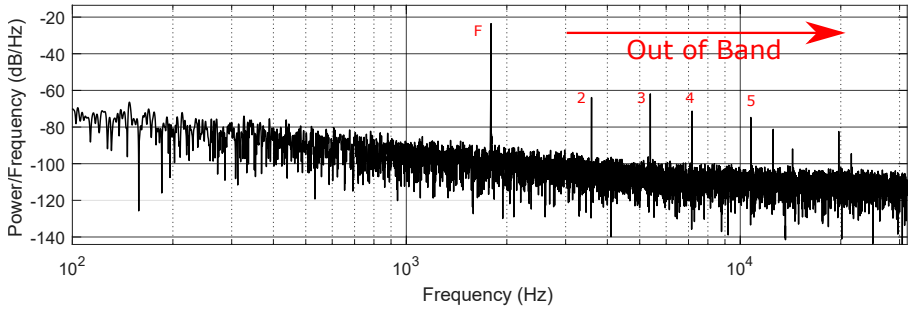

Figure 3.11: Spectrum of the reconstructed output during an acquisition of a 1794 Hz tone. Previously published in [147].

An examination of the reconstructed 531 Hz signal in time-domain seen in Figure 3.4.2 has

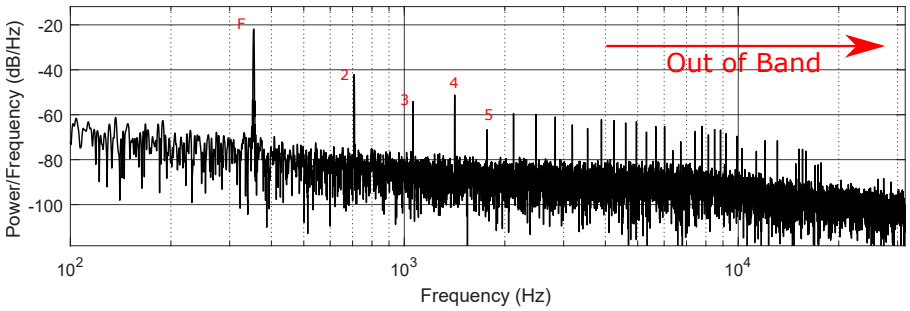

Figure 3.12: Spectrum of the reconstructed output during an acquisition of a 531 Hz tone. Previously published in [147].

revealed that the portions of the signal that do not contain large slopes are subject to added distortion. This was further investigated in Monte Carlo transition simulations and was found to be a result of instability in a feedback loop of the charge injection circuits used to add and remove charge to and from C_b that was caused by the design's insufficient margins for manufacturing process variations. It was further identified that this issue does not occur when a large slope is present in the input signal, explaining the increase in SNDR seen in higher frequency input signals.

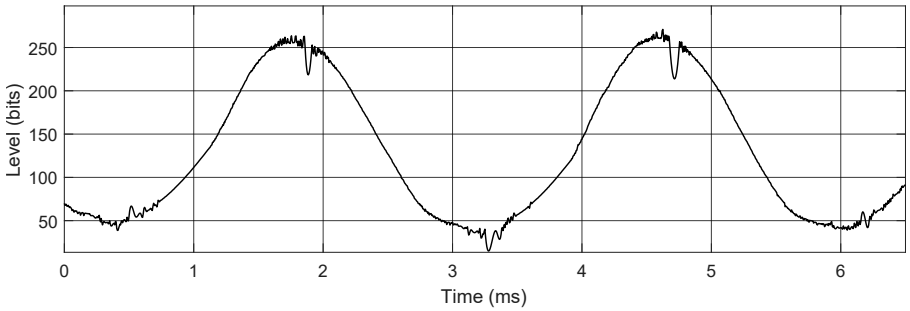

Figure 3.13: Reconstructed 200 mV, 531 Hz sine wave quantised by an 8-bit CT quantizer demonstrating added distortion. Previously published in [147].

To verify the behaviour of the circuit during acquisition of neural signals, a pre-recorded neural signal sample containing both EAP and LFP was loaded to an arbitrary signal generator and amplified such that it passes through 256 quantisation levels. The signal was then recorded and reconstructed following the same method as during the pure tone tests. A short section of both the original and reconstructed signals can be seen in Figure 3.4.2. The average power consumption of the ADC during this acquisition was measured to be ≈4.2 µW, only a small increase from the static consumption of ≈3.75 µW, thus demonstrating the effectivity of the sampling scheme and this topology for the acquisition of neural signals.

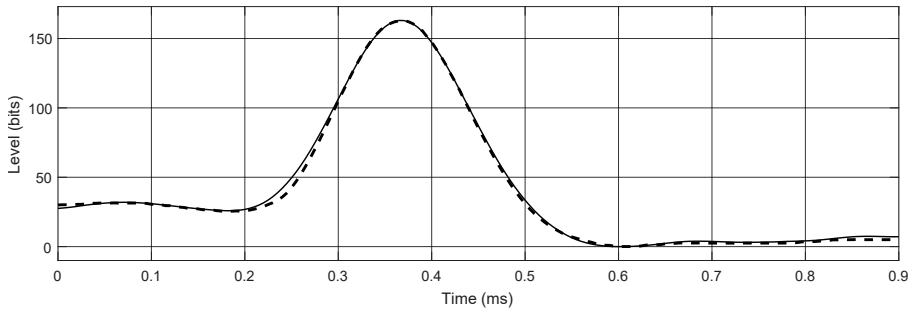

Figure 3.14: Reconstructed sample neural spike (dashed) alongside the original signal (solid). Previously published in [147].

An estimate of SNDR of this acquisition has been found by directly comparing the acquired signal with its reconstructed version:

$$SNDR = \frac{E[y(t)]}{E[y(t) - y^r(t)]} \tag{3.14}$$

where $y(t)$ is the original signal, $y^r(t)$ its reconstructed version following acquisition and $E[\cdot]$ an operator denoting the energy of the signal in square brackets. This was found to be ≈30.6 dB, equivalent to ENOB of 4.8 bits.

One of the concerns of this topology is the leakage current of capacitor C_b. The effect of this has been evaluated during measurements by applying a DC input to the system and observing the output. This has resulted in approximately one UP impulse being generated every second, thus showing that leakage adds a negligible slope to the output, not affecting its fidelity.

3.5 Comparison to Other Designs in Literature and Conclusion

To compare the design to other CT ADCs found in literature, we refer to Table 3.3, listing several designs of CT ADCs found in literature alongside some metrics measuring their performance. The used FOM is following that of Equation 3.15:

$$FOM = \frac{P}{2^{ENOB} \times BW} \tag{3.15}$$

	[units]	[143]	[166]	[167]	[144]	[168]	[169]	[170]	[171]	[145]	This work
N	[bits]	8	5	8	8	8	8	4-8	5	-	8
SNDR	[dB]	47-54	28.3	40-49	51.4	46-50	37-48	43.2	31	32-42	16-30.6
SFDR	[dB]	58.3	-	-	-	-	-	-	-	≈ 30	22-38.8
ENOB	[bits]	7.5-8.69	4.42	6.36-7.86	8.26	7.35-8.02	5.84-7.69	6.89	4.87	5-6.7	2.3-4.8
BW	[kHz]	20	≥ 0.35	5	0.11-10.5	0.95	1	1	0.2-5	10^4–5×10^4	4
Tech	[µm]	0.13	0.13	0.18	0.09	0.18	0.35	0.18	0.5	0.028	0.35
Area	[mm^2]	1.69	0.357	0.045	N/A	0.49	0.037	0.96	0.06	0.0032	0.115
Supply	[V]	0.8	0.3	0.8	0.5 & 0.7	1	1.8-2.4	0.7	3.3	0.65	1.5
Power	[µW]	3-9	0.22	0.31-0.58	0.54-0.73	8.49	0.6-2.0	25	118.8-501.6	8-24	$\approx$3.75-12.9
FOM	[pJ]	0.36-2.49	29.36	0.266-1.41	0.168-21.64	34.9-54.77	2.9-34.9	210.8	812.5-85778	$(1.5\text{-}75)\times10^{-3}$	33.7-654.9

Table 3.3: Comparison with Other CT ADC Implementations Previously published in [147].

This demonstrates that the circuit can be compared with solutions previously published in literature, although the achieved FOM, admittedly, has been surpassed by other solutions. This is mostly due to the fact that a design insufficiency and susceptibility to manufacturing variations caused additional distortion as discussed earlier. Although the demonstrated implementation has limitations, it acts as a proof of concept of the topology and demonstrates its feasibility. Its advantages over other solutions in the literature include the inherent possibility of DC offset rejection and its simplicity leading to the possibility of creating very compact designs. As seen in Figure 3.4.2, the majority of the used area is occupied by digital circuitry alongside reference and biasing circuits, some of which can be shared amongst several channels on a single die. In addition, the employed digital circuits would significantly benefit from scaling afforded with more modern CMOS technologies.

Chapter 4

Clockless Chopping Scheme for CT Acquisition of Neural Signals

The results presented in this chapter considering the clockless flicker noise removal method have been previously published in [147].

One of the issues that are commonly associated with the acquisition of low-frequency signals, such as LFPs or ECG is the presence of flicker noise added by CMOS devices [172]. This manifests itself as noise of 1/f (10 dB per decade) power spectral density (PSD) that is added on top of thermal noise of uniform PSD. This problem is also visible in the results obtained in the previous chapter, especially Figures 3.11 and 3.12 demonstrating the PSD of reconstructed signals acquired by the designed CT ADC. It can clearly be seen that the PSD of noise rises at small frequencies and would therefore affect the acquisition of some signals. Flicker noise is a result of a random process resulting from charge being trapped and released in the oxide of a MOS transistor [172].

To better understand noise in a MOSFET, we can refer to Figure 4.1. This demonstrates the two sources of noise in a MOSFET - thermal noise modelled as current source of PSD i_d^2 added to drain current and flicker noise modelled as voltage source of PSD v_g^2 added to gate voltage, where the two are defined as:

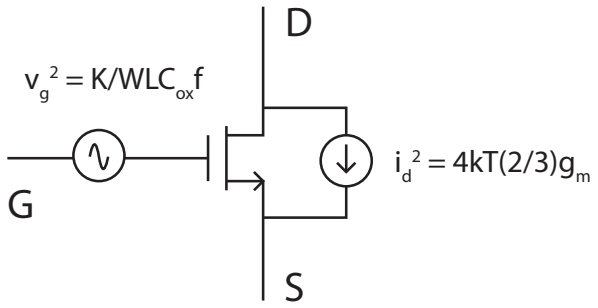

Figure 4.1: Model of noise in a MOS transistor based on [173].

$$i_d^2 = 4kT\left(\frac{2}{3}\right)g_m \tag{4.1}$$

$$v_g^2 = \frac{K_f}{WLC_{ox}f} \tag{4.2}$$

where k is the Boltzmann constant, T the ambient temperature, g_m the transconductance of the transistor, K_f the flicker noise constant, WL the area of the gate, C_{ox} the oxide capacitance per area and f the frequency. For convenience and added utility in circuit design, both those noise sources are often referred to the gate in the form of input-referred noise:

$$v_{n,in}^2 = \frac{K_f}{WLC_{ox}f} + \frac{8kT}{3g_m} \tag{4.3}$$

This demonstrates that the input-referred noise PSD decreases with rising frequency and is dominated by thermal noise beyond a certain corner frequency f_c. This is defined as a frequency at which the power of flicker and thermal noise is the same and is often used as a metric in circuit design. This relationship also shows that in order to reduce flicker noise, one can resort to increasing the gate area, which is often impractical, or use a transistor of smaller K_f. In this regard, it is advantageous to use PMOS transistors [174] that typically result in K_f smaller by an order of magnitude or resort to using JFET devices which were believed to not be prone to flicker noise at all [175] but are nowadays understood to have K_f several orders of magnitude smaller than MOSFETs.

Most solutions seen in circuits, however resort to active techniques allowing the suppression of flicker noise without the need to use large devices or resort to special manufacturing technologies. The most common techniques [176] include autozeroing, correlated double sampling (CDS) and chopping.

Autozeroing splits the operation of an amplifier, or another system, into two phases. In the first phase, the output of the amplifier is sampled under a no input condition, thus recording its DC offset and sampling the output noise, often in its input-referred form. In the next phase, the amplification phase, the sampled value is subtracted from the output of the circuit, thus removing the offset and reducing some of the noise added. While more suited for removal of time-invariable offsets, using this technique allows for limited suppression of flicker noise as well. This is permitted by its 1/f spectral characteristic, resulting in correlation between samples of the noise taken in a short time window. One of the disadvantages of autozeroing is the fact that the output is only available during the amplification phase. This is addressed by correlated double sampling which places another sample and hold circuit at the output of an autozeroing system, thus alleviating this issue [176].

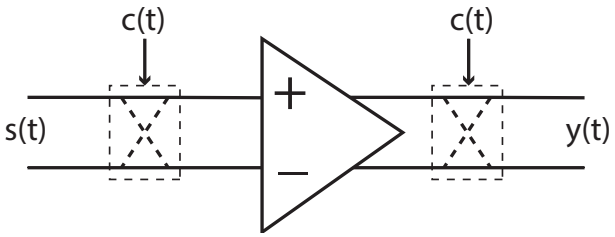

Figure 4.2: Schematic of a Chopper-Stabilised Amplifier - input signal s(t), chopper c(t) and output y(t).

Chopping is an alternative technique that works on the principle of up-modulating the input signal to a higher frequency, such that it occupies a frequency band outside of that affected by flicker noise and demodulating it back to its baseband after amplification, as seen in an illustration in Figure 4.2 alongside spectra of signals involved in the process. The input, a band-limited signal s(t) is first multiplied by a chopper c(t). For simplicity of circuit implementation, this is typically a square wave alternating between values of +1, -1, +1, -1, ..., thus implementable by a series of switches. The input signal is then upmodulated to the frequency of the square

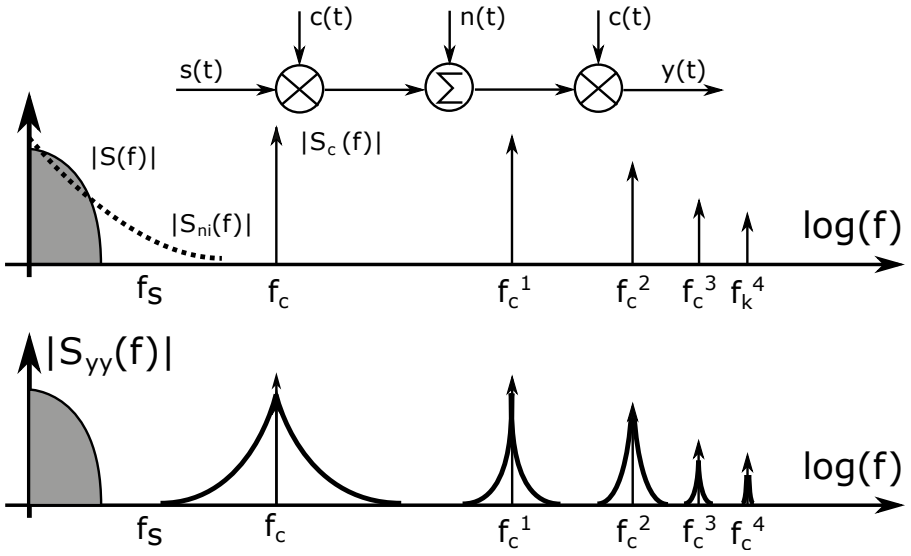

Figure 4.3: Spectra of signals involved in the process of chopping - Input band-limited signal S(f), chopper $S_c(f)$, Output $S_{yy}(f)$. Based on figures previously published in [177].

wave and its harmonic frequencies. When passed through an amplifier, noise n(t) is added to the signal. The output is then demodulated by being multiplied by c(t) again. If $c(t)^2 = 1$, the output y(t) is then the following:

$$y(t) = s(t) \times c(t)^2 + n(t) \times c(t) = s(t) + n(t) \times c(t) \tag{4.4}$$

It thus contains an unchanged version of the input signal and noise added by the amplifier modulated by the chopper with images at the fundamental frequency of the chopper and its harmonics. If the chopper frequency is chosen such that it is higher than the sum of the input signal's bandwidth and the flicker noise corner frequency, the signal of interest will only be corrupted by the amplifier's thermal noise and therefore not affected by flicker noise and DC offset of the amplifier at all.

The fact that chopping allows for complete removal of flicker noise, as opposed to its partial reduction by autozeroing, makes chopping the method of choice for amplification of low-frequency signals in many analogue front-end designs. One of the most prominent disadvantages of chopping is, however, the fact that it leads to a decrease of the system's input impedance. This is caused by any capacitance at the input of the amplifier before chopping is applied.

This is due to the fact that the capacitance has to be charged each time the polarity of the input is switched. If we denote it C_p, and the input voltage v_{in} we can see that charge $\delta q = 2C_p v_{in}$ is transferred during each change of the chopper's polarity. This thus leads to a charge transfer of $2\delta q$ during each cycle of the chopper resulting a DC current flow from the input leading to an input impedance Z_{in}:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{2f_c\delta q} = \frac{1}{4f_c C_p} \tag{4.5}$$

The chopping process thus converts a parasitic input capacitance to a resistive input impedance that depends on the chopper frequency and the magnitude of the parasitic impedance. This is an unfortunate result as unchopped amplifiers can achieve very high input resistance on the order of GΩ if JFET or MOSFET transistors are used as input devices. On the other hand, those have a fairly large gate capacitance that is proportional to the gate area which in turn often needs to be large enough to ensure sufficient matching between differential input devices as well as sufficiently high flicker noise corner frequency. As an example, an NMOS device of 10 µm x 10 µm gate area in a TSMC 180 nm BCD technology has a parasitic gate capacitance of ≈ 487 fF according to steady-state simulations. Assuming a chopping frequency of 100 kHz, this would give rise to input impedance of:

$$Z_{in} = \frac{1}{4 \times 100 \times 10^3 \times 487 \times 10^{-15}} \approx 5.1 \text{ MΩ} \tag{4.6}$$

Such an input impedance is relatively small when compared to impedance of some electrodes, as seen in Chapter 2. Many analogue neural front-ends found in literature therefore employ techniques that raise the input impedance lower by chopping. An example of such can be seen in [178; 179] which uses an additional buffer to pre-charge the parasitic capacitance when a change of the chopper's state occurs. [178] reports an achieved impedance boost of 540x, from 11 MΩ to 6 GΩ.

Another potential issue that arises when chopping is employed, is the need for a high-frequency

clock as well as potentially a higher amplifier bandwidth, leading to additional power consumption that is independent of the input signal, thus making such a scheme unsuitable for CT acquisition, resulting in a loss of its activity-dependent power consumption. Let us therefore consider if and how chopping can be applied to CT acquisition if we do not wish to lose some of the advantages of this novel sampling method.

4.1 Chopping in CT Acquisition

In theory, chopping can be applied in a CT sampling process the same way it is applied in conventional circuits, by chopping the signal at the input, letting it pass through the ADC and chop the output as well. In a spike-domain ADC with UP and DOWN outputs, such as one seen in Chapter 3, this can be done simply by changing the meaning of UP and DOWN. This will however result in the CT ADC seeing the chopped signal at its input, a signal of constantly high frequency, thus removing any advantage gained by the CT ADC's ability to adapt its power consumption to the spectrum of the input signal. In addition, the higher slew rates introduced in the signal by chopping, will require designing the ADC for a higher specification.

To mitigate those issues, we therefore have to invent a new method that will allow the circuit to maintain its properties while also permitting the suppression of flicker noise. To achieve this, we consider the effects of using a chopper signal derived from the signal itself. Following the previously presented CT ADC topology, we can consider using the digital output as a basis for generation of a chopping signal. Let us therefore consider a chopper c1(t) that changes its state whenever a quantisation level crossing (either UP or DOWN) is detected. Using such a signal would be advantageous as it would result in chopping of the signal at the same time a quantisation level crossing is detected and thus alleviating an issue of generating signal-independent high-frequency content seen by the amplifier.

To understand the effects of its usage, we have to know the spectrum of the new chopping signal. This is, however, difficult to estimate analytically as doing so would require knowing the probability of level crossing based on the properties of the input signal which, as discussed

in the previous chapter, is a result that is difficult to obtain for a generic signal. Based on numerical simulations, we have, however, been able to observe that such a chopping signal contains spectral content inside the band of the original signal in addition to its images at multiples of f_k, the average sampling rate of the CT process.

The visualisation of spectra involved in the process under such a scenario, when the input is a pure tone, can be seen in Figure 4.4. This demonstrates that in such a case, flicker noise is upmodulated to frequencies that are multiples of the average sampling rate. This is sufficient as during the operation of a CT ADCs, the input signal is oversampled as shown in Chapter 3. What is, however, problematic, is the presence of an image of the original signal in the chopper's spectrum. This leads to modulation of some of the flicker noise power within the bandwidth of the input signal and thus preventing its removal.

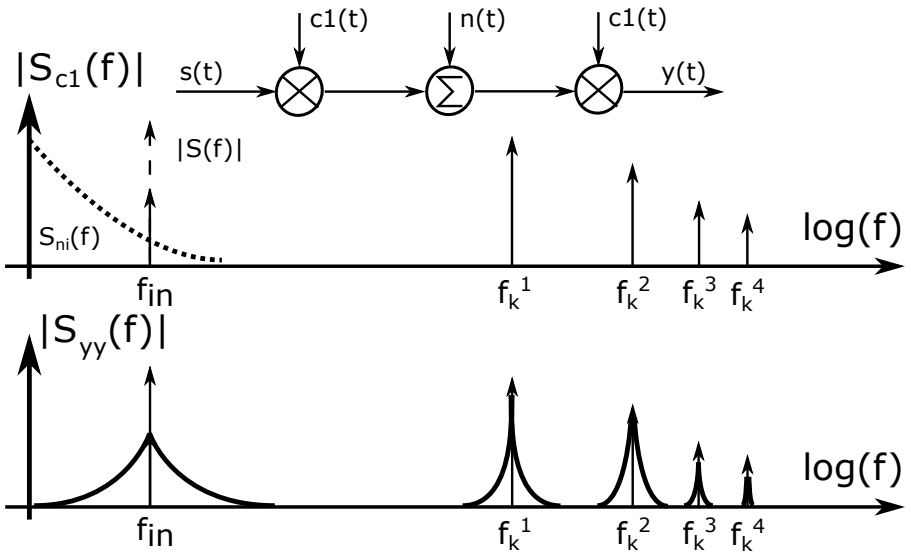

Figure 4.4: Spectra of signals involved in the process of chopping based on a chopper derived from a sine wave input - Visualised spectra: input S(f), chopper $S_{c1}(f)$, output $S_{yy}(f)$, added noise $S_{ni}(f)$. Previously published in [177], modified.

To evaluate the efficiency of a chopper, we can define a metric giving the proportion of flicker noise power that remains within the bandwidth B of the input signal:

$$R = \frac{\int_0^B |S_c(f) * S_{ni}(f)|^2 df}{\int_0^\infty |S_c(f) * S_{ni}(f)|^2 df} \tag{4.7}$$

If we wanted to achieve complete removal of flicker noise, we would have to chose a chopper that

has no spectral content at frequencies smaller than the sum of the input signal's bandwidth and the flicker noise corner frequency. This is, for example, the case of a fixed frequency square wave chopper. To ensure that we keep the signal-dependent properties of CT acquisition, a question then arises whether it is possible to modify the chopping signal such that a larger portion of its power lies at higher frequencies.

4.1.1 Stochastic Chopping

One of the simplest ways to modify the signal, while ensuring it only ever alternates between +1 and -1 while remaining fully derived from the input and only changing when the input signal crosses quantisation levels, is to introduce randomness. Previously we have considered the scenario under which the chopping signal changes each time a quantisation level crossing is detected. Let us now consider a chopper that has a probability of 0.5 changing its state whenever a level crossing takes places.

To analyse this chopper $q(t)$, we need to identify its power spectral density (PSD) $S_q(f)$. Knowing the power spectral density of the random process $r(t)$ that we denote $S_r(f)$, this can be obtained as $S_q(f) = S_r(f) * S_c(f)$. Since it is difficult to obtain an estimate of $S_r(f)$, let us first consider a simpler case of a signal g(t) that has a probability of 0.5 of changing its state after and only after a fixed period of time T_s. The autocorrelation $R_g(\tau)$ of such a signal can easily be obtained if we note that two samples of the signal taken τ apart are correlated only if they are both taken within the same period T_s. This means that $R_g(\tau)$ must be 0 for $\tau > T_s$ and equal to the probability of the two samples occurring within the same period T_s for $\tau < T_s$. $R_g(\tau)$ is thus a following a linear relationship for $0 < \tau < T_s$ as seen in Figure 4.5

Using the Wiener-Khinchin theorem, we can thus easily obtain the PSD $S_g(f)$:

$$R_g(\tau) = \Lambda(\tau/T_s) \tag{4.8}$$

$$S_g(f) = T_s \text{sinc}^2(f \times T_s) \tag{4.9}$$

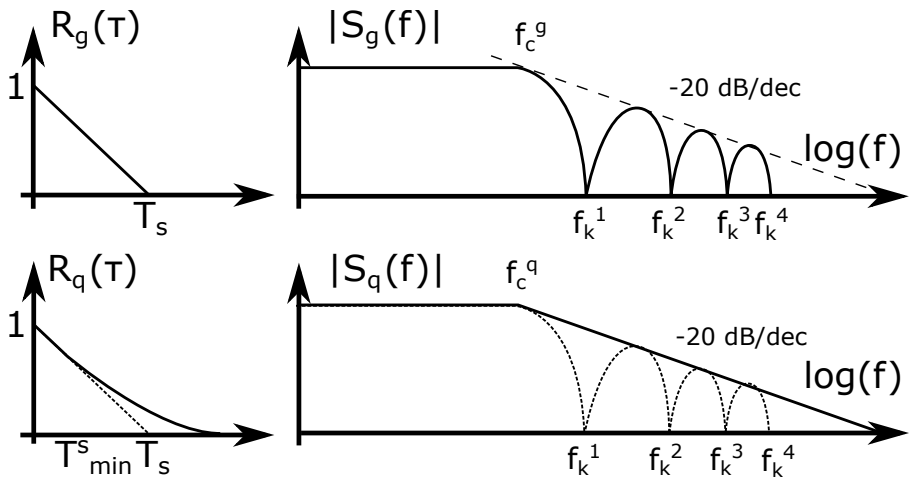

Figure 4.5: Autocorrelation and Spectra of Stochastic Choppers g(t) and q(t). Previously published in [177].

As seen in Figure 4.5, $S_g(f)$ is approximately flat up to a corner frequency f_c^{gg} when it starts to drop towards a zero occurring at frequency $f_k^1 = 1/T_s$. The PSD then contains spectral lobes of zeros at multiples of f_k^1 with the peaks of the lobes decaying at a rate of 20 dB/dec. The corner frequency f_c^g can be found by solving $|S_g(f)| = 1/2$, giving rise to $f_c^g \approx 0.44/T_s$.

To understand the behaviour of $S_q(f)$ randomly changing its state when a quantisation level is crossed, we can similarly start by considering the autocorrelation $R_q(\tau)$ of the signal. Since there is a limit to the frequency under which quantisation level crossings occur, giving rise to a period T^s_{min} during which no changes can occur, we note that the autocorrelation has to be identical to $R_g(\tau)$ for $\tau < T^s_{min}$. Its behaviour at frequencies higher than T^s_{min} is equal to the probability that any two samples taken τ apart occur between two quantisation level changes. Such a result would again require the knowledge of quantisation level crossing statistics that likely is not generalisable.

To obtain an estimate of $R_q(\tau)$ for $\tau > T^s_{min}$ numerical methods had to employed. Pre-recorded neural signals were evaluated for the likelihood of quantisation level crossings and the resulting autocorrelation was found to be exponentially decaying for $\tau > T^s_{min}$. In a scenario where the CT sampling process leads to significant oversampling, it can be assumed that linear portion of $R_q(\tau)$ is negligible and $R_q(\tau)$ can thus be estimated as a two-sided exponential decay.

We note the following Fourier pair:

$$e^{-a|t|} \Longleftrightarrow \frac{2a}{a^2+\omega^2} \tag{4.10}$$

this indicates that due to the Wiener-Khinchin theorem the PSD $S_q(f)$ has to follow the PSD of a single-pole system. This was verified by numerical simulations and it was additionally found that the $S_q(f)$ appears as an envelope of $S_g(f)$ if T_s was $1/f_s^{avg}$, the average sampling period. The corner frequency of the PSD f_c^q was found to be $f_c^q \approx 0.44 f_s^{avg}$, thus following the behaviour analogous with $S_g(f)$. The spectrum of the chopper therefore follows that of white noise filtered by a first-order low-pass filter and can be expressed as

$$S_q(f) = \frac{k}{f^2 + (f_c^q)^2} = \frac{f_c^q}{\pi \times (f^2 + (f_c^q)^2)} \tag{4.11}$$

The value of the constant k is found such that the power of $S_q(f)$ is 1, as dictated by the fact that the signal only takes discrete values of 1 and -1.

The effect of such a chopper can be seen in Figure 4.6 showing both the input-referred noise before chopping $|S_{ni}(f)|$ and the input-referred noise $|S_{no}(f)|$ modulated by the chopper. The relationship between the two spectra is $S_{no}(f) = S_{ni}(f) * S_q(f)$ and at the same time the power of both $S_{ni}(f)$ and $S_{no}(f)$ has to be the same as $|q(t)|^2 = 1$.

The use of chopper $q(t)$ thus leads to whitening of flicker noise at all frequencies smaller than $f_c^q - f_c$, the difference between the corner frequency of the chopper's spectrum and the corner frequency of flicker noise. As the overall power of the noise has to remain the same, this means that the noise is spread across a wider range of frequencies, thus potentially reducing its power in the bandwidth of the input signal. Since the PSD of the output noise is white, we can estimate the noise reduction factor R as:

$$R \approx \frac{B}{f_c^q - f_c} \approx \frac{B}{0.44 f_k - f_c} \approx \frac{B}{0.44 \times 2^N B - f_c} \tag{4.12}$$

If we assume that the corner frequency of flicker noise is smaller than the average sampling

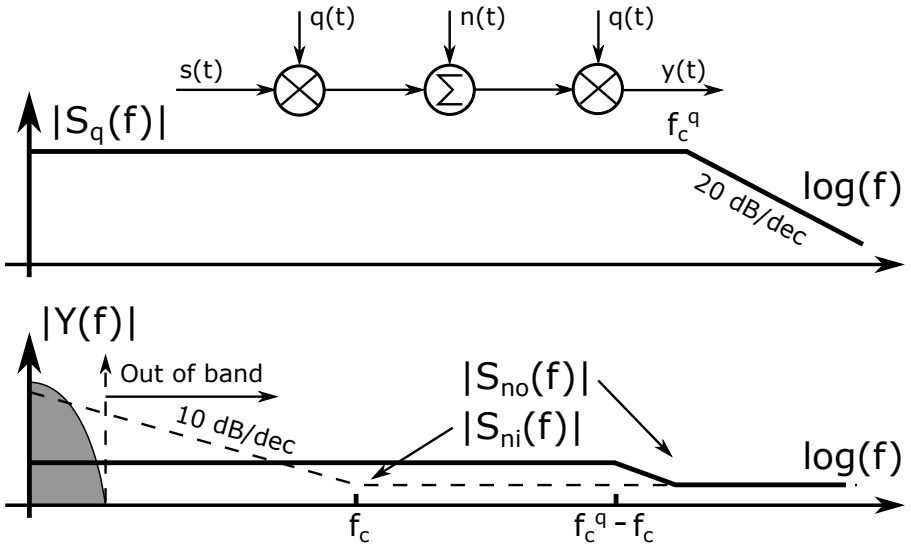

Figure 4.6: Top: Spectrum of stochastic chopper $|S_q(f)|$, Bottom: Spectra of input noise $S_{ni}(f)$ and output noise $S_{no}(f)$ following modulation by stochastic chopper $|S_q(f)|$. Previously published in [177], modified.

rate, we can further reduce to relationship to:

$$R \approx \frac{1}{2^N} \tag{4.13}$$

The reduction in flicker noise power is thus approximately proportional to the amount of quantisation levels the signal passes through during CT acquisition. This is the case as the oversampling ratio and hence the average sampling rate f_k increases with the amount of quantisation levels crossed.

4.2 Circuit Implementation

Having introduced a new concept of stochastic chopping, this section is going to describe a practical implementation of the scheme in a CMOS circuit building on the circuit shown in Chapter 3, mitigating some of its deficiencies and introducing improvements that lead to a reduction of its power consumption as well as the area footprint of the circuit.

The block diagram of the circuit implemented in a commercially available 180 nm TSMC

technology can be seen in Figure 4.7. In comparison with the previous version, reduction in both power consumption an area has been achieved mainly by simplifying the core of the circuit in addition to benefiting from the smaller feature sizes of the 180 nm process. Additional improvements have been permitted by using the triple-well option of the manufacturing process allowing individual driving of the NMOS devices' bodies.

While the previous implementation contained a configuration register allowing the setting of different pulse lengths triggering a charge pump or sink adding or removing charge from capacitor C_B, this implementation only uses a single pulse generator that is reused for both charging and discharging pulses. Such a decision is sensible as there can not be a state where both pulses would be generated at the same time. The impossibility to configure or tune the pulse length has to inevitably lead to a mismatch between the charge added or removed during a step up and down respectively. However, as discussed previously, this mismatch leads to addition of a slope in the quantised signal that can easily be determined and corrected for in post-processing without a loss of fidelity in the signal.

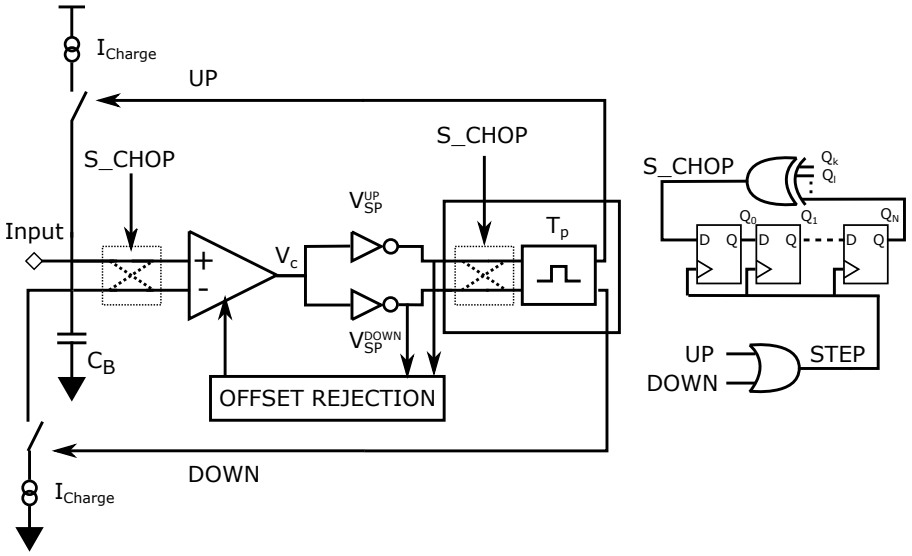

Figure 4.7: Implementation of the second generation of CT ADC building on the circuit presented in Chapter 3.

4.2.1 Threshold Crossing Detector

In the previous generation of the circuit, the threshold crossing detector was implemented using invertors of varied gate length to achieve different switching points. This has proven problematic as the use of long devices leads to decrease of the circuit's bandwidth and switching speed of the invertor. This is additionally made more problematic by an increase in the gate area leading to an increase of the gate capacitance that is amplified by the Miller effect around the switching point of the invertor. This previously resulted in the need to employ a unity-gain buffer to allow the comparator to drive the threshold crossing detector without a significant loss of bandwidth, leading to a significant increase of the overall static power consumption. The second version of the circuit mitigates this issue by using small-size devices in the invertors and instead controlling the switching point by driving the body of the PMOS and the NMOS in either of the two invertors as seen in Figure 4.8. This has led to a reduction of the gate capacitance and the load observed at the output of the comparator, making it possible to remove the unity-gain buffer from the design. In addition, both the transistor pairs have their drain current limited by a current source of 20 nA to reduce the power consumption resulting from shoot-through current caused by the input staying around the switching point for a long time. To ensure the output has a well-defined digital state, the signal is buffered by a number of digital invertors.

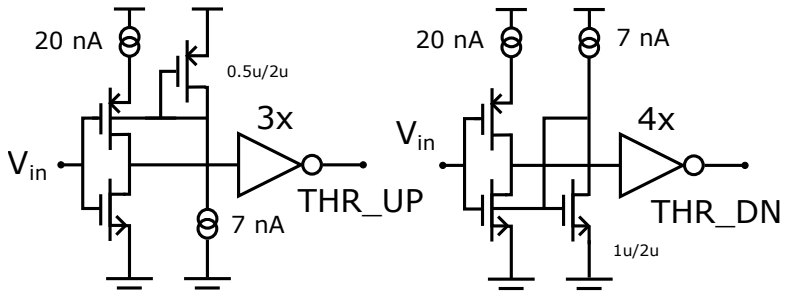

Figure 4.8: Implementation of the threshold crossing detector making use of the body effect to achieve different switching points.

4.2.2 Chopping

Chopping is implemented in the form of an analogue switch at the input while a digital multiplexer is used as a chopper at the output. A slight issue with implementing the chopper q(t) presented in the previous subsection is the fact that it requires the introduction of randomness. While this can be achieved with the use of true random number generators, such as [180] using noise as a source of entropy, those lead to additional static power consumption that is undesirable. As an alternative, we can therefore consider using methods leading to generation of pseudorandom numbers, such as linear-feedback shift register (LFSR). This allows for a solution that can be activity-dependent, as an LFSR can only be clocked whenever a new state is required, such as when a quantisation level is crossed.

Since the code generated by an LFSR repeats itself after 2^N_{SR} cycles, where N_{SR} is the amount of elements employed, the spectrum of the chopper has to be affected. Denoting the LFSR-generated chopper r(t), we note that it can be described as the result of multiplying the deterministic chopper c(t), changing state whenever a quantisation level crossing occurs, and a pseudorandom process m(t), denoting the output of the LFSR.

The spectrum of the new chopper $S_r(f)$ can therefore be found as $S_r(f) = S_c(f) * S_m(f)$ where $S_m(f)$ is the spectrum of m(t). To derive $S_m(f)$ we can again resort to first deriving its autocorrelation $R_m(\tau)$. If the LFSR is configured to generate a maximal-length sequence (m-sequence), the code is going to repeat after 2^N_{SR} cycles, or $2^N_{SR}/f_k$ seconds, and therefore the autocorrelation has to be $R_m(\tau) = 1$ for $\tau = k \times 2^N_{SR}, k \in Z$ and $R_m(\tau) = 0$ for all other τ. Alternatively, we can denote $R_m(\tau)$ as $R_m(\tau) = \sum_{k=-\infty}^{k=\infty} \delta(\tau - k \times 2^N_{SR}/f_k)$ where $\delta(t)$ is the Dirac impulse function. Since the autocorrelation is a train of impulses, so has to be the spectrum and hence:

$$S_m(f) = 2^{(N_{SR}+1)}\pi/f_k \sum_{k=-\infty}^{k=\infty} \delta(f - k \times f_k/2^N_{SR}) \tag{4.14}$$

Knowing that the spectrum of $S_c(f)$ contains several images of the input signal, the spectrum

of the chopper $S_r(f)$ has to contain images of the input signal centered at frequencies where $S_m(f) \neq 0$. To maximise the reduction of flicker noise, it is necessary to ensure that the spectrum is as flat as possible and therefore resembles $S_q(f)$ obtained if a true random number generator was used. To that end, it is advantageous to use LFSR of as high a length as possible. That is however not practical in terms of optimisation of the design.

Let us note that the images in $S_r(f)$ are located $f_k/2^N_{SR}$ apart and the average sampling rate f_k depends on the bandwidth B of the input signal such that $f_k = B \times 2^N$ where N is the oversampling ratio of the CT ADC. This means that if $N = N_{SR}$, the chopper images are going to be B apart, thus the spectrum will be filled as seen in Figure 4.9. The circuit should therefore be designed such that an LFSR of a length equal to at least the oversampling ratio is employed.

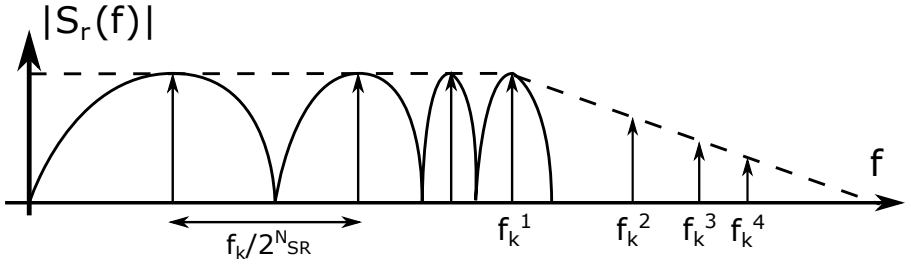

Figure 4.9: Spectrum of a Stochastic Chopper $|S_r(f)|$ Generated Using an LFSR. Previously published in [177].

To illustrate the operation of the stochastic chopper in the presented CT ADC topology, figure 4.10 shows chosen simulated internal signals of the circuit during acquisition of a 100 Hz sine wave. The input is denoted V_{in}, the chopper state S_CHOP, the comparator output V_c, the potential at capacitor C_b is V_B. The spike-domain outputs indicating a change in quantisation level are denoted UP and DOWN. This demonstrates the random, activity-dependent, nature of the chopper and the effect on the comparator's output.

4.2.3 Input Comparator

A schematic of the input comparator can be seen in Figure 4.11. This comprises of a simple CMOS operational transconductance amplifier (OTA) biased using a tail current of 480 nA

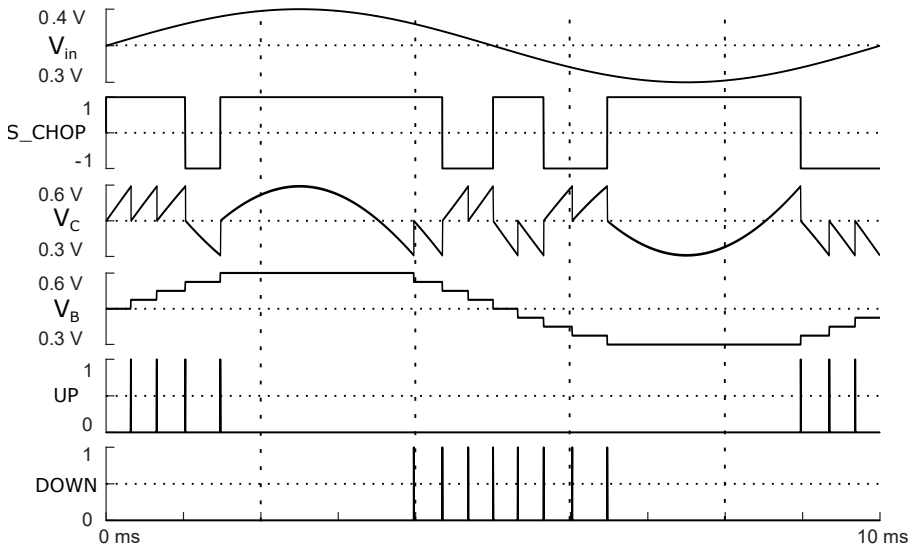

Figure 4.10: Illustration of some internal signals demonstrating the operation of a chopped CT-ADC during the quantisation of a sine-wave.

giving rise to a minimal bandwidth of $\approx$ 1.2 MHz according to Monte Carlo simulations, sufficient to enable the 8-bit quantisation of a signal of 3 kHz bandwidth in accordance with Equation 3.13. The transistor sizes employed and seen in Figure 4.11 were obtained using a global parameter search in Cadence Virtuoso with the aim of minimising power consumption while ensuring that the bandwidth requirement is met.

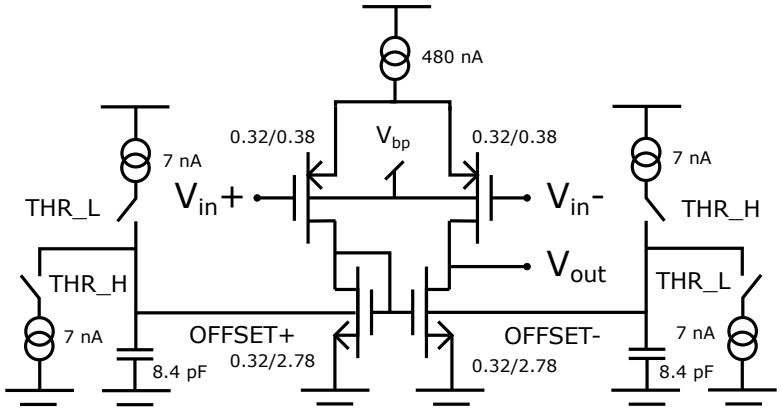

Figure 4.11: Schematic of the input comparator employed in the CT ADC.

An issue that arises with the use of a chopper, that was not present in the unchopped version is the design's susceptibility to offsets in the input comparator. If no chopper is used, this is added to any input DC offset and rejected by the tracking loop of the circuit. If a chopper is used, any DC offset would be chopped and modulated to higher frequencies and thus added to the output digitised signal which is undesirable as it leads to additional quantisation steps

or disables the operation of the circuit completely due to the addition of extra slopes that the circuit is unable to follow.

It is therefore necessary to employ another mechanism facilitating the rejection of the DC offset in the comparator. As seen in Figure 4.11, the circuit achieves this by feeding additional differential signal composed of OFFSET+ and OFFSET- to the bodies of the active load in the comparator. The offset is determined from observing the digital outputs of the threshold crossing detectors, THR_H and THR_L. Since those signals contain the chopped version of the input signal, they are not dependent on it and the average of THR_H - THR_L is proportional to the offset of the comparator and if there is no offset, THR_H - THR_L should be equal to zero. The design thus integrates those signals by having them drive constellation of charge pumps and sinks adding or removing charge to or from capacitors, the potential of which we call OFFSET+ and OFFSET-. By introducing those potentials to the bodies of the active load, the offset is rejected and does not affect the output.

Another cause for concern is the effect of the use of chopping on the charge held at capacitor C_b. As previously discussed, chopping leads to conversion of parasitic capacitances to resistances in the case of a chopped fully differential input. In the case of the presented circuit, the resulting effect is, however, slightly different. At the time of chopping, a quantisation level has just been crossed and therefore the potential difference between the two inputs of the comparator should be $\pm\delta V_q$ where δV_q is the potential corresponding to one quantisation level. Since on average the amount of quantisation level crossings up and down has to be the same, there is no net current flowing to the capacitor as a result of the chopper's operation. The effect can, however, lead to a slight rise in the output noise floor as some unwanted charge will be removed due to chopping during rising phases of the input signal and conversely extra charge will be added during falling phases when the chopper changes its state. This effect can, however, be minimised by maximising the ratio of C_b and the parasitic capacitance at the input of the comparator. Since the employed C_b is on the order of pF, the amount of extra injected charge is negligible.

4.2.4 Charge Injection

Since several aspects of the presented system rely on the ability to precisely inject a small amount of charge onto a capacitor, a circuit shown in Figure 4.12 has been employed. In general the biggest challenge in injecting a small amount of charge stems from the fact that if a current source is switched, any excess charge resulting from potential difference across the switch is going to be added to the output. To prevent this from happening, it has to be ensured that the potential across the switch is zero before the switch is closed. The circuit of Figure 4.12 ensures this by bootstrapping the switch using a voltage follower.

When the circuit is inactive, and the output capacitor is not being charged or discharged, the voltage follower is engaged and the potential across the switch is zero. When either of the CHARGE or DISCH inputs is asserted, the switch is closed and the voltage follower is disengaged, such that the output potential can start changing.

The circuit is still prone to errors resulting from mainly the input offset of the voltage follower and excess charge injected from the body of the transistors during a switch. While some authors [181] recommend mitigating this by employing dummy transistors to absorb the extra charge, this technique has not been used due to its limited effectiveness in small devices caused by limited matching. Instead, minimal size devices have been used, ensuring the excess channel charge is minimal. Any residual error has the same effect as an error in I_{Charge} and can equally be removed by post-processing of the digitised signal, due to it leading to an addition of a slope to the output signal.

4.3 Results

4.3.1 Flicker Noise Removal Method

The proposed principle of stochastic chopping has first been verified using numerical simulations using Matlab. To this end a pure 1 kHz tone of rms value of $1/\sqrt{2}$ was generated and finely

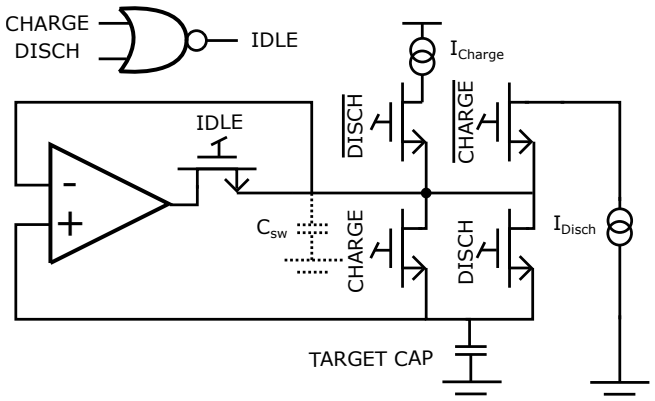

Figure 4.12: Schematic of a Circuit Allowing Precise Charge Injection. All devices are minimal size (W/L) = (220 nm/180 nm)

quantised at a sampling rate of 5 MHz, in addition to a vector containing 1/f pink noise of an input-referred 0.0179 rms value. To simulate the CT sampling process, the simulation described by Algorithm 1 has been employed.

This operates on a finely quantised discrete-time signal, calculating the error between the input and the last quantised version of the signal on each step. This is then multiplied by a chopper taking values of +1 and -1 followed by addition of noise. If the error exceeds one of the thresholds, a sample is generated with its polarity dependent on the state of the chopper and polarity of the comparator's output. Function LFSR_next() generates the next sample of an 8-bit LFSR register configured to generate an m-sequence.

The spike-domain signal output has then been reconstructed using spline interpolation to obtain the acquired waveform both with the chopper enabled and disabled and the estimated PSD of both the reconstructed signals can be seen in Figure 4.13. This shows a reduction of the noise floor by approximately 15 dB at small frequencies with the chopper enabled as well as the predicted effect of whitening the flicker noise and confirms the above presented hypotheses.

4.3.2 Circuit Implementation

The described circuit has been implemented in a commercially available 180 nm Bipolar-CMOS-DMOS (BCD) technology, encompassing a triple-well process allowing the implementation of NMOS devices at independent body potentials. Most crucially, this allows the implementation

```
input     : sig[N], noise[N]
output    : output[N]
parameter: ampl = 100
parameter: thr = 2
initial   : chop = 1
initial   : quant[0] = 0
for k = 1 → N do
    err[k] = ampl*chop*(sig[k]-quant[k-1])+noise[k];
    if err[k] > thr then
        output[N] = chop;
        chop = LFSR_next();
    else if err[k] < -thr then
        output[N] = -chop;
        chop = LFSR_next();
    else
        output[N] = 0;
    end
    quant[k] = quant[k-1] + output[N]*thr;
end
```

Algorithm 1: Algorithm used to simulate the proposed stochastic chopping scheme.

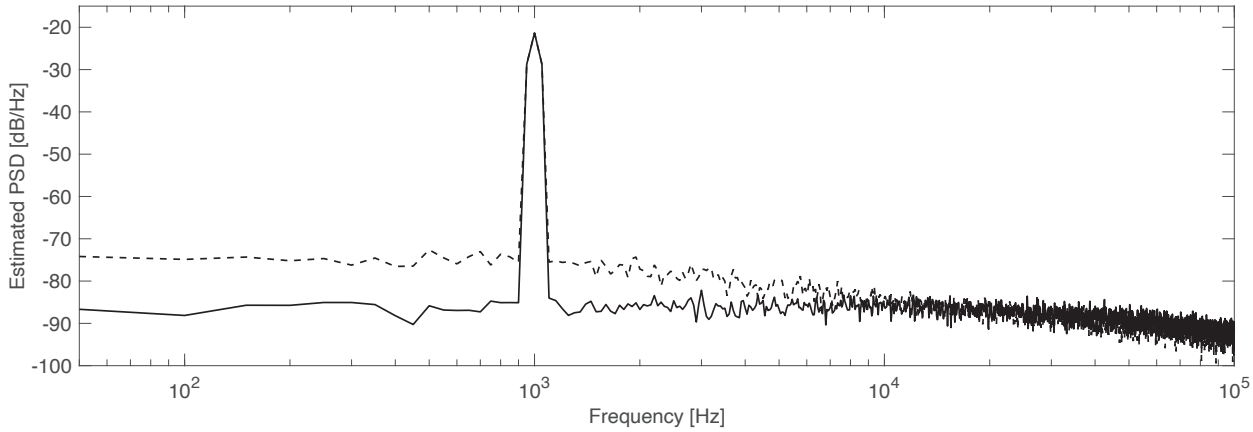

Figure 4.13: Simulated PSD of a reconstructed 1 kHz tone acquired using CT sampling scheme with (solid) and without (dashed) clockless chopping.

of an improved threshold crossing detector, described in subsection 4.2.1, using the body effect of both the NMOS as well as a PMOS to form invertors of two different switching points while using minimal size devices and thus reducing their parasitic capacitance and power consumption. In addition, the use of BCD technology allows for the removal of input and circuit offset by injecting an integrated output to the amplifier's input differential pair body potential, thus forming a DC servo loop without the need for additional devices. Finally, the body effect is used in both NMOS and PMOS devices to reduce their threshold voltages and allow operation

from a lower supply voltage, thus reducing the overall power consumption.

The layout of the implemented circuit can be seen in Figure 4.14 showing the core occupying an area of 240 µm×120 µm, an improvement by a factor of 4 over the previous implementation. The majority of area is occupied by the offset rejection circuit due to a need to use large capacitors facilitating sufficient attenuation.

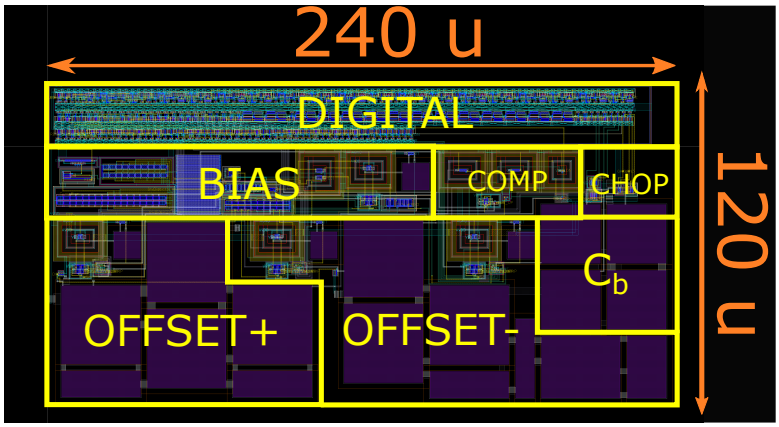

Figure 4.14: Layout of the Designed Circuit, occupying an area of 240 µm×120 µm

The circuit has at first been simulated in Cadence IC6.1.8 using foundry-supplied device models. The circuit consumes static power of ≈539 nW from a voltage supply of 0.8 V when no input is present, rising to ≈985 nW when a 1 kHz tone passing through 339 quantisation levels is presented at the input, leading to additional dynamic energy of 0.66 pJ consumed per every taken sample on top of static power consumed.

The simulated performance of the circuit was evaluated using two different input signals, pure tones of 200 mV peak-to-peak voltage and a respective frequency of 100 Hz and 1 kHz passing through ≈ 339 quantisation levels. To evaluate the effect of the implemented chopper, the simulations were performed with both the chopper enabled as well as disabled. Transient simulation including transient noise of 1 Hz to 1 MHz bandwidth was then performed for 100 cycles of the input signal, 1 s and 100 ms for both the respective tons, and the spike-domain outputs exported and further processed using Matlab.

The acquired signal was reconstructed using spline interpolation and converted to a finely quantised discrete-time sampled signal of a 100 kHz sampling rate. An estimate of power spectral density was obtained by directly performing discrete Fourier transform of the signals

as well as using the Welch's method, averaging spectra of shorter portions of the investigated signal, to obtain a smoother estimate. The resulting spectra can be seen in 4.15 and 4.16, while ENOB and SNDR under the various input conditions can be seen summarised in Table 4.1.

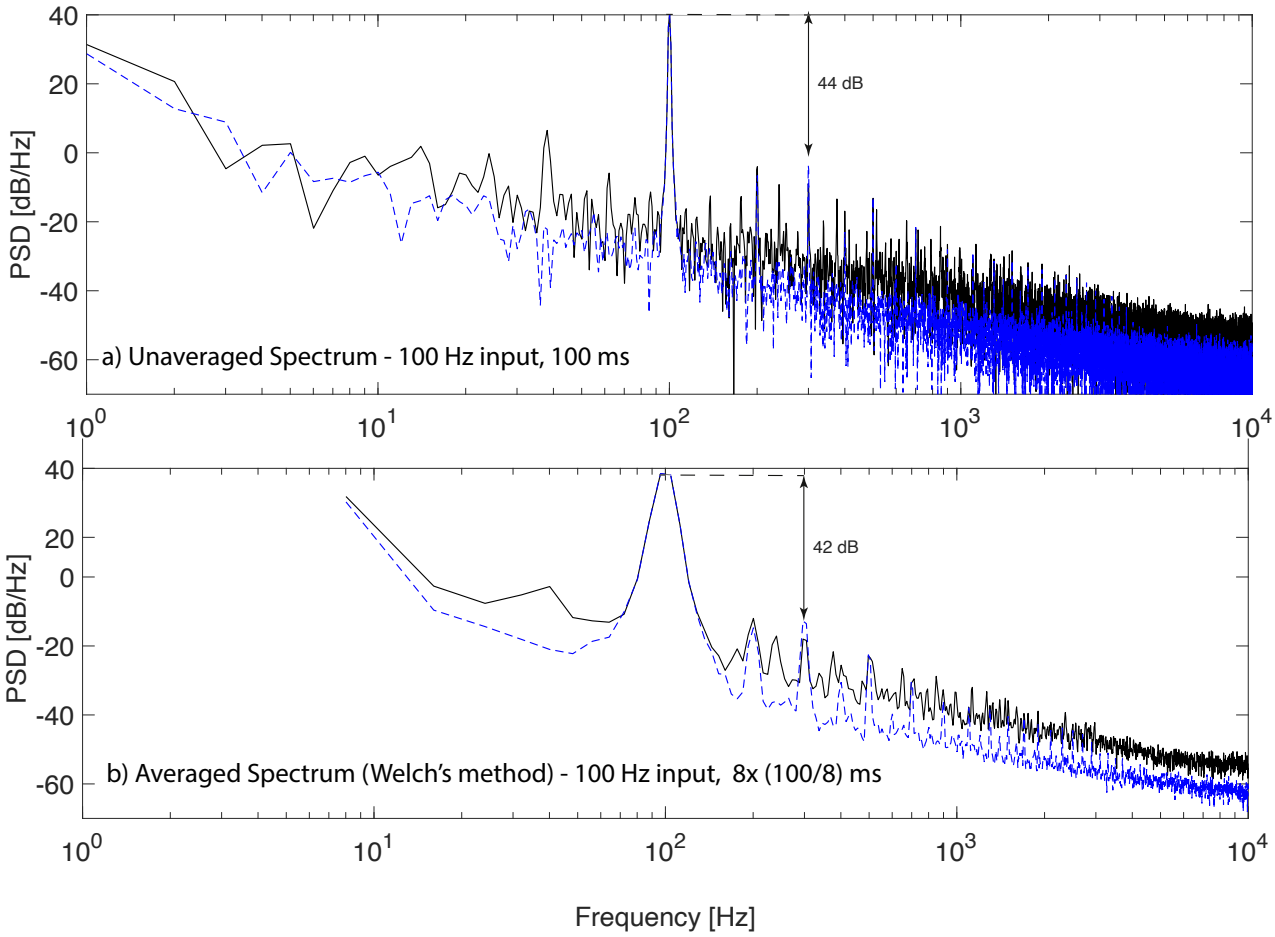

Figure 4.15: Simulated PSD of a reconstructed 100 Hz tone acquired using the designed CT ADC with (solid black) and without (dashed blue) clockless chopping. a) Top plot shows the unaveraged PSD estimated over a period of 1 s, b) bottom plot shows a PSD obtained using the Welch's method, averaging 8 spectra of 125 ms portions of the signal.

	SNDR [dB]	ENOB [bits]
100 Hz Unchopped	40.59	6.5
100 Hz Chopped	31.47	4.9
1 kHz Unchopped	38.90	6.2
1 kHz Chopped	29.33	4.6

Table 4.1: Simulated SNDR and ENOB of the 2nd Version of the CT ADC

Contrary to expectations, those results do not show any signs proving that the flicker noise removal method results in an improvement of SNR and are therefore inconclusive. In addition, there is a visible rise of ≈5 dB in the noise floor when the chopper is engaged, a result of

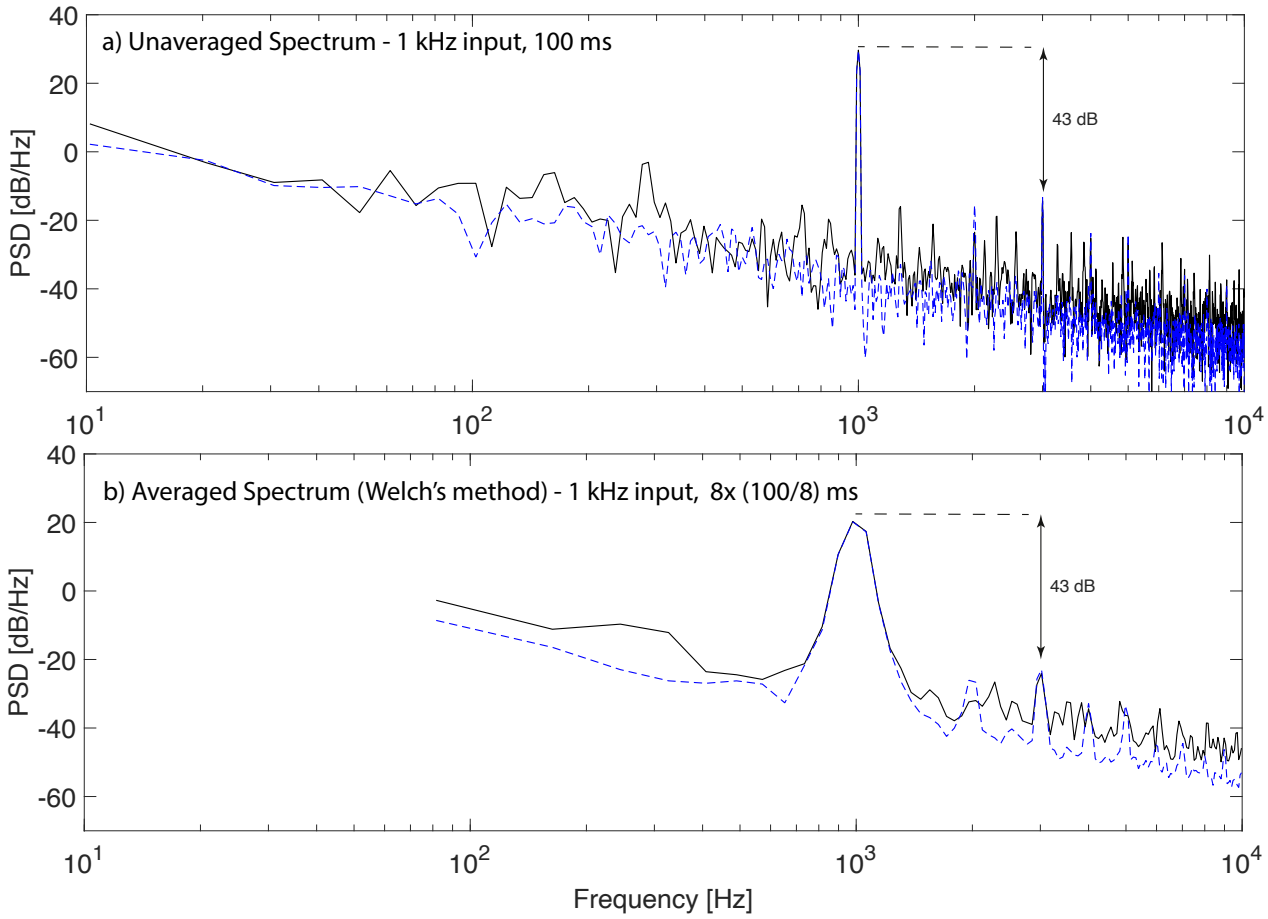

Figure 4.16: Simulated PSD of a reconstructed 1 kHz tone acquired using the designed CT ADC with (solid black) and without (dashed blue) clockless chopping. a) Top plot shows the unaveraged PSD estimated over a period of 100 ms, b) bottom plot shows a PSD obtained using the Welch's methodm, averaging 8 spectra of 12.5 ms portions of the signal.

detrimental contributions added by the chopper's operation such as extra charge injection. Interestingly, the noise profile is dominated by a $1/f^2$ profile.

While not as apparent in the results of testing the first version of the circuit, this can be explained as a property of this particular topology of CT ADC. A simple explanation stems from the fact that the circuit integrates the spike-domain output to form an estimate of the quantised signal. This leads to integration of the noise and the resulting $1/f^2$ frequency profile. Another way to look at this problem is to consider that each quantisation step results in a reproduction of the input signal at capacitor C_B together with an error that can be described by its variance σ^2. With each additional step, the variance of the accumulated error increases and the autocorrelation of the accumulated noise decreases with increasing lag, leading to an increased error at small frequencies and hence explaining the noise profile.

4.3.3 Measured Results

Having received the manufactured integrated circuit, experimental measurements have been carried out to evaluate its performance. The sample has been wirebonded to a JLCC68 package and a PCB seen in Figure 4.17 has been designed to allow the connection of a signal source as well as access to the system's outputs used to set up the measurements.

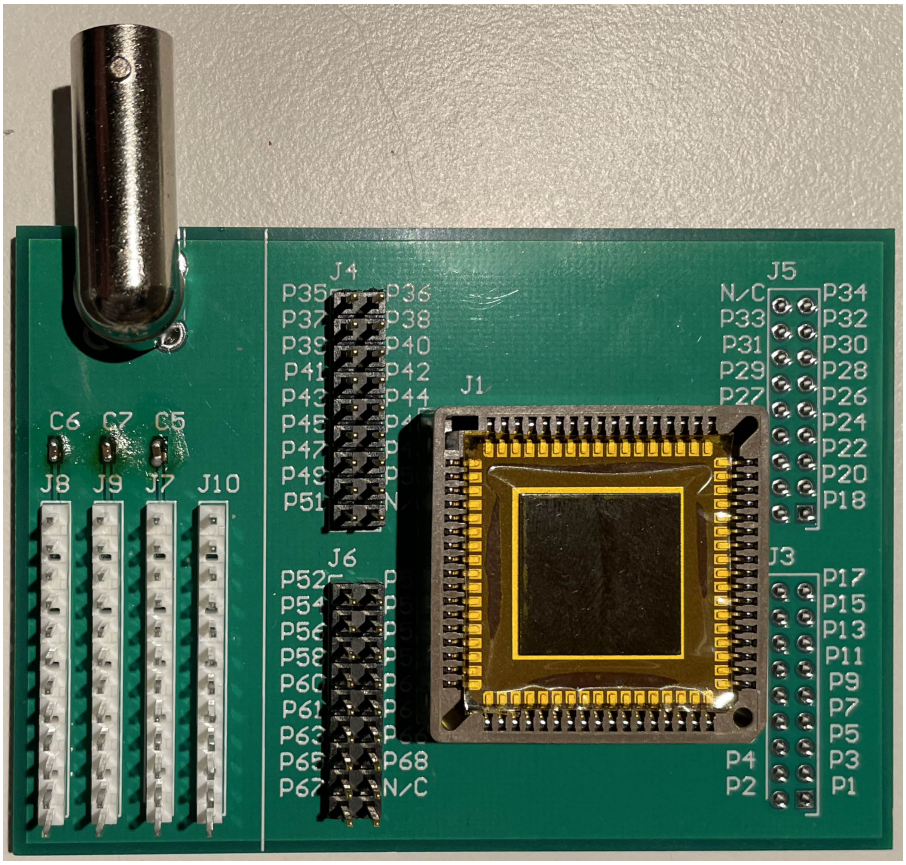

Figure 4.17: Photograph of a PCB used to evaluate the 2nd version of the designed CT ADC.

As seen in Figure 4.18, describing the measurement set up, a Tektronix AFG3102 arbitrary signal generator has been employed to generate the input stimuli for the ADC. The digital output spikes UP and DOWN have been acquired using a Salae Logic 8 Logic Analyser at a sampling rate of 500 MSPS. In each case the acquired outputs have then been stored on a computer for further reconstruction and analysis.

The DUT has been powered using an Agilent N6705B DC Power Analyser with an N6761A precision DC Power Module permitting accurate measurement of the power consumption on the order of nW. A DC power supply of 0.8 V has been applied to the core of the circuit and

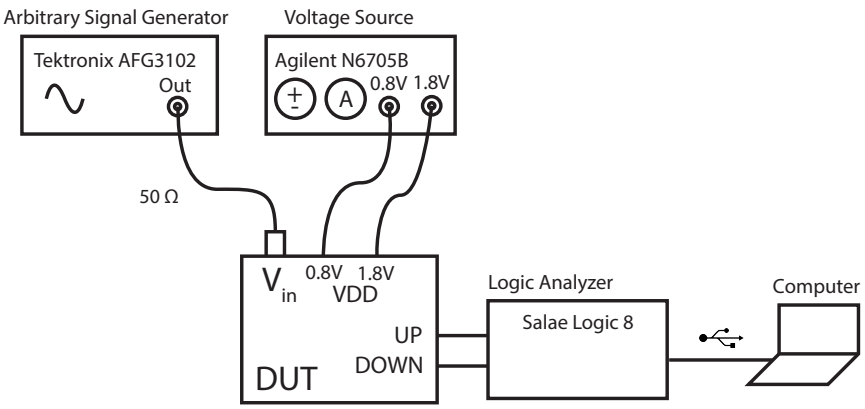

Figure 4.18: Test configuration used to evaluate the 2nd version of the designed CT ADC.

and 1.8 V to the I/O cells. Once powered on, the circuit core has been found to consume a current of 596 nA from the 0.8 V power supply, giving rise to a static power consumption of ≈ 0.5 µW.

In addition to static power consumption, the employed digital circuits consume additional energy when there is activity in the input signal and output spikes are generated. Due to a design error in the layout, the manufactured circuit contains a shorted digital invertor consuming a constant current of ≈ 2 mA preventing the measurement of dynamic power consumption. Since this is consumed from a power rail separate from analogue circuitry, it did not prevent the measurement of the static consumption. As described earlier, simulations have shown additional dynamic power consumption of ≈ 450 nW during acquisition of a 1 kHz tone passing through 339 quantisation levels.

A pure tone of a 600 Hz frequency, 100 mV peak-to-peak voltage and an offset of 140 mV has then been applied to the input of the circuit and the digital outputs recorded. The acquired signal has then been reconstructed in Matlab using a cumulative sum while estimating and removing the mismatch between a step taken up and down. This has been repeated with the chopper enabled and disabled and the resulting spectra have been plotted in Figure 4.19.

This shows a deterioration of the noise floor upon enabling of the chopper and its increase by about 20 dB caused by additional errors in quantisation introduced by the operation of the chopper and could be improved by changes to its implementation. Regardless of this result, the

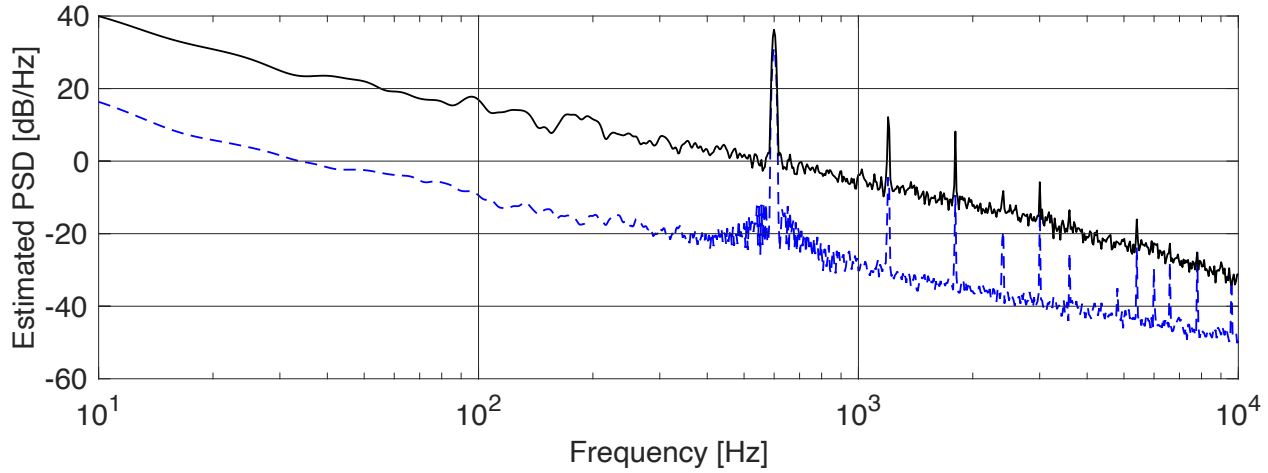

Figure 4.19: Comparison of measured spectra of the CT ADC's output acquiring a 600 Hz, 100 mV peak-to-peak input signal with the chopper enabled (solid black) and disabled (dashed blue).

20 dB/dec roll-off of the noise floor caused by the nature of this particular topology's operation dominates any possible contribution of flicker noise. As a result, it could therefore be argued that the presented topology can not benefit from the presented chopping scheme and it is not possible to verify its effectiveness by measuring this circuit.

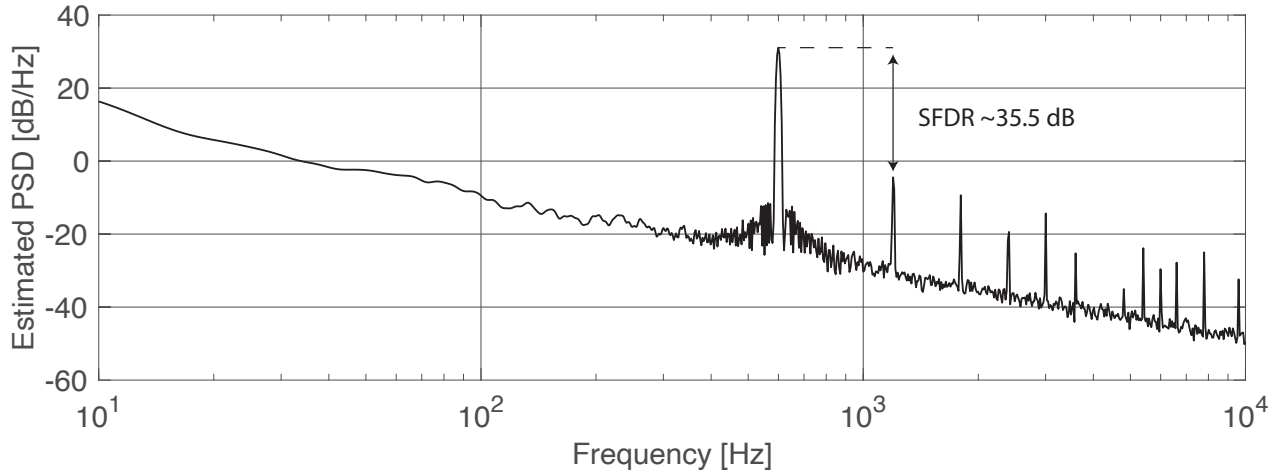

Figure 4.20: Measured spectra of the CT ADC's output acquiring a 600 Hz, 100 mV peak-to-peak input signal with the chopper disabled.

A detail of the output spectrum having disabled the chopper can be seen in Figure 4.20 and shows SFDR of $\approx$ 35.5 dB and SNDR of $\approx$ 29.3 dB estimated in a frequency band between 100 Hz and 10 kHz.

The input frequency has then been varied from 18 Hz to 4.8 kHz in order to evaluate the

performance of the circuit when acquiring various signals. The SFDR, in-band SNDR and "local" dynamic range (DR), defined as a ratio of spectral power at the fundamental frequency and its 1.5 multiple has been plotted in Figure 4.21 demonstrating nearly constant SNDR and SFDR for signals of varying frequency and an increase in "local" dynamic range with increasing input frequency, a result of the observed $1/f^2$ noise floor characteristic. This is an improvement over the previous design which failed to operate correctly in absence of slopes present in the signal.

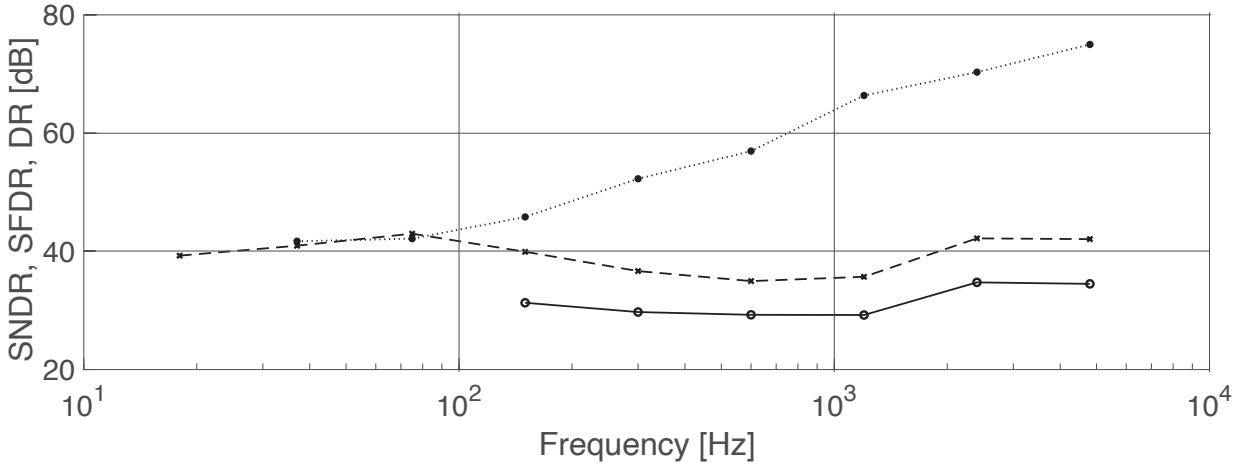

Figure 4.21: Variation of SNDR, SFDR and local dynamic range.

To observe the performance of the circuit during the acquisition of neural signals, a pre-recorded neural signal (EAP+LFP) has been loaded to the arbitrary signal generator, conditioned as to increase its peak-to-peak voltage and applied as an input to the ADC. Examples of two neural spikes (EAPs) acquired and reconstructed during the experiment can be seen in Figures 4.22 and 4.23. This demonstrates that the circuit is capable of following the slopes present in neural spike signals.

Similarly, Figure 4.24 shows a reconstructed sample LFP signal with intermittent spikes. Those figures demonstrate the capability of the topology to perform well in acquiring short signals of high frequency content while continuously accumulating an error during the acquisition of slow-changing signals.

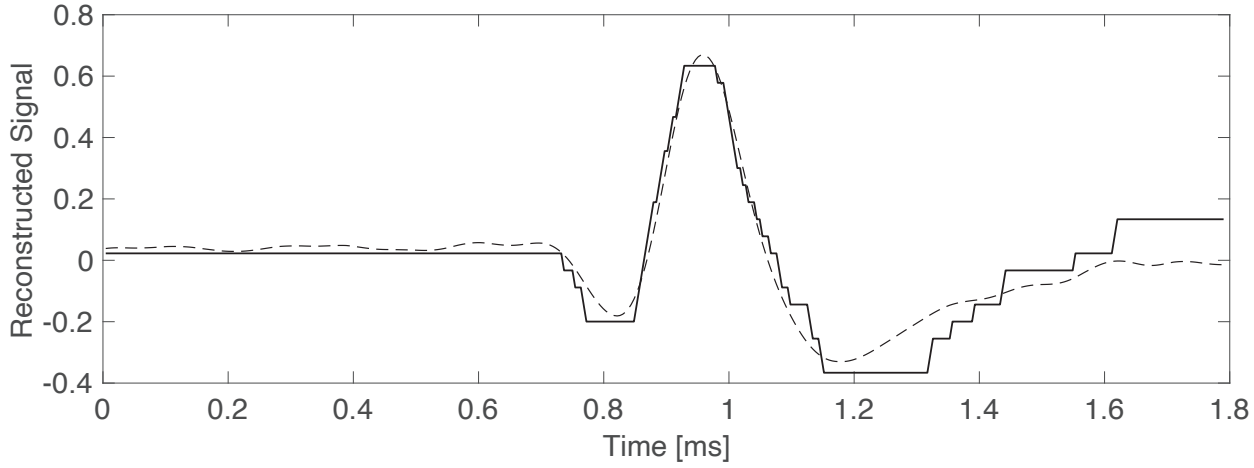

Figure 4.22: Reconstruction (solid) of a Sample EAP Recorded Using The CT ADC alongside the original signal (dashed).

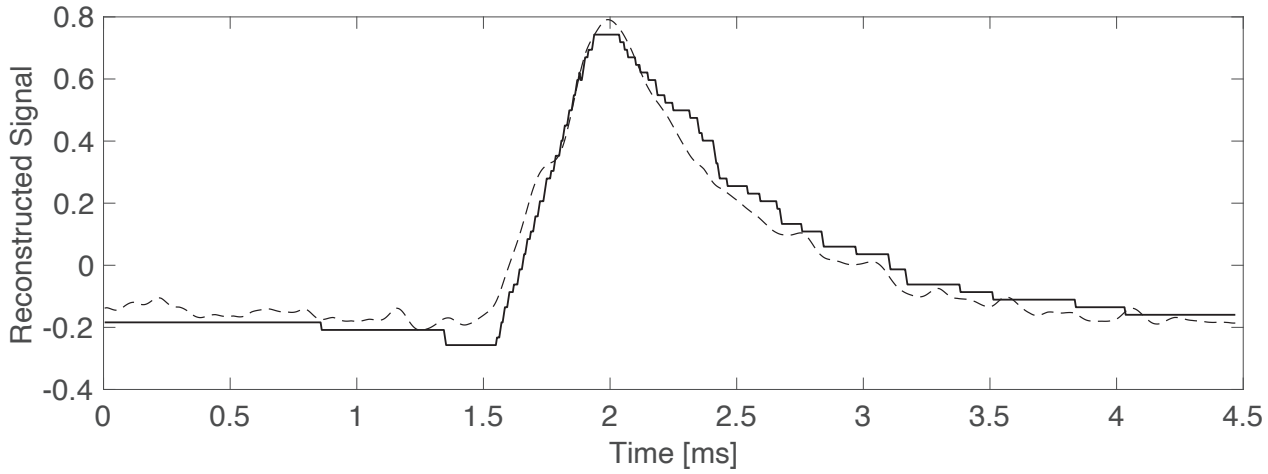

Figure 4.23: Reconstruction (solid) of a Sample EAP Recorded Using The CT ADC alongside the original signal (dashed).

4.3.4 Conclusion

A novel chopping scheme alleviating the need to use a fixed frequency chopping signal has been introduced and a circuit implementation proposed. While it was not possible to demonstrate the effectiveness of the scheme in a circuit implementation, the correctness of the flicker noise removal method was proven by numerical simulations in Matlab, demonstrating a 15 dB improvement in the noise floor at small frequencies. The observed rise in noise floor of the circuit implementation resulting from the operation of the chopping circuit remains to be investigated further but is most likely a result of additional errors introduced by the switches

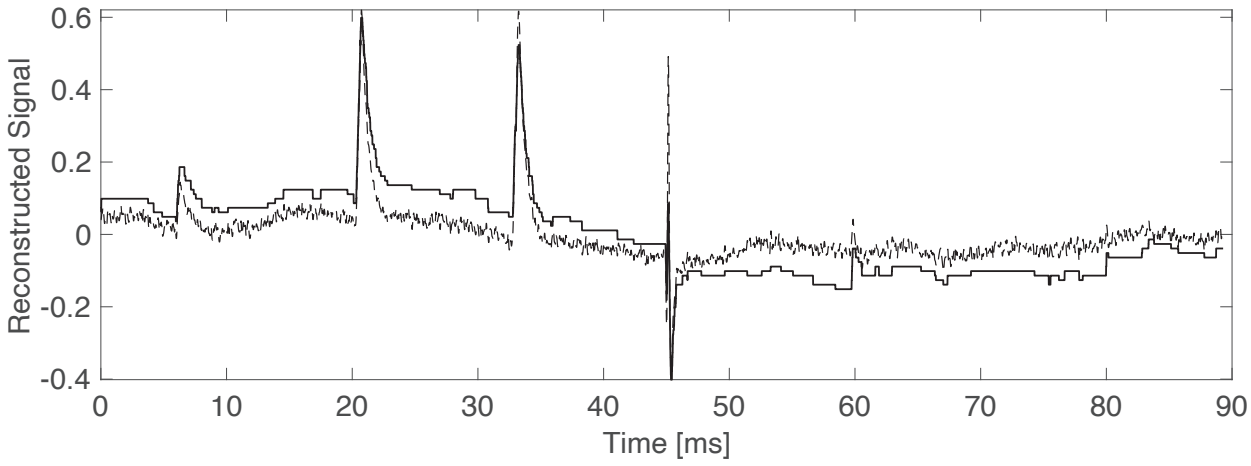

Figure 4.24: Reconstruction (solid) of a Sample LFP+EAP Signal Recorded Using The CT ADC alongside the original signal (dashed).

such as unwanted charge injection and the caused resistive loading of capacitor C_b caused by the switching. In addition, it is possible that the added noise is dominated by other sources outside of the input comparator such as jitter of the pulse generator. This also remains to be investigated in the future.

The proposed design is compared to other CT ADC implementations as well as the previous version of the circuit in Table 4.2. The FOM used for comparison is:

$$FOM = \frac{P}{2^{ENOB} \times BW} \tag{4.15}$$

This demonstrates that despite the inability to demonstrate the effectiveness of the chopping, the second generation of the circuit achieves significant improvement over the previous generation, making it comparable with the state of the art and one of the CT ADCs requiring less than 1 µW to operate. In addition, to our best knowledge, the design represents the smallest CT ADC implemented in a 0.18 µm CMOS technology presented in literature. Moreover, since a large portion of the layout, as seen in Figure 4.14 is occupied by capacitors needed for offset rejection used in the chopping scheme, the occupied area can be further reduced by $\approx 60\%$.

The second generation of the circuit also permitted gaining a deeper understanding of the presented charge-based topology as to its inherent noise characteristics and limitations. While it

	[units]	[143]	[166]	[167]	[144]	[168]	[169]	[145]*	V1	This work
N	[bits]	8	5	8	8	8	8	-	8	8
SNDR	[dB]	47-54	28.3	40-49	51.4	46-50	37-48	32-42	16-30.6	30-35
SFDR	[dB]	58.3	-	-	-	-	-	≈ 30	22-38.8	36-42
ENOB	[bits]	7.5-8.69	4.42	6.36-7.86	8.26	7.35-8.02	5.84-7.69	5-6.7	2.3-4.8	4.7-5.5
BW	[kHz]	20	≥ 0.35	5	0.11-10.5	0.95	1	10^4–5×10^4	4	4
Tech	[µm]	0.13	0.13	0.18	0.09	0.18	0.35	0.028	0.35	0.18
Area	[mm^2]	1.69	0.357	0.045	N/A	0.49	0.037	0.0032	0.115	0.0288
Supply	[V]	0.8	0.3	0.8	0.5 & 0.7	1	1.8-2.4	0.65	1.5	0.8
Power	[µW]	3-9	0.22	0.31-0.58	0.54-0.73	8.49	0.6-2.0	8-24	$\approx$3.75-12.9	0.45-0.95
FOM	[pJ]	0.36-2.49	29.36	0.266-1.41	0.168-21.64	34.9-54.77	2.9-34.9	$(1.5\text{-}75)\times10^{-3}$	33.7-654.9	2.5-9.1

Table 4.2: Comparison with Other CT ADC Implementations. Expanded version of Table 3.3. [145]* is an Integrator-CT ADC and cannot be fully compared with true CT ADC implementations.

brings significant advantages in the sense of allowing the creation of very small layout footprints, its largest disadvantage remains the introduction of $1/f^2$ noise caused by the continuous integration of the quantisation error. As a result, this can be potentially problematic if the ADC is used for the acquisition of low frequency signals but, arguably, might not necessarily prevent its use in neural implants. As we have demonstrated, the circuit performs particularly well during the acquisition of neural spikes while preserving their shape for the needs of subsequent spike sorting. Literature contains examples [182] of spike sorting schemes that operate without the need of a clock and on the basis of event-driven input signals ideal for combination with the presented topology. On the other hand, the quantisation of the low frequency LFPs is subject to more error, although this is to some extent mitigated by the $1/f^2$ spectral characteristic of the LFPs themselves [183], leading to a constant SNR frequency profile. Thanks to its minimal power consumption and extremely small footprint, in addition to the emergence of novel signal processing techniques, this ADC topology could therefore become a prime candidate for the use in the next generation of neural implants exploiting the sparse nature of neural signals.

Chapter 5

Reference Circuits and Voltage Regulators for Neural Implants

As the next generation of neural implants such as [79; 75] or [76] aims to deliver a solution that allows a completely wireless acquisition of neural signals, a number of challenges is presented to the designers of the electronic circuits used inside. Since many of those designs rely on power delivered through inductive coupling, the power supply is typically delivered to the circuit in the form of high-frequency alternating voltage. This has to be rectified [184; 185] and the output voltage stabilised such that a clean DC supply voltage is obtained and applied to the instrumentation circuits. Furthermore, it is also necessary to generate a stable reference voltage that can be used for the acquisition of the input signals. Since the magnitude of the input voltage recovered from the inductive link depends on a large number of factors, it is necessary to design the reference such that it is independent from the power supply and therefore has as large power supply rejection ratio (PSRR) as possible. As will be demonstrated, this challenge is, furthermore, made more complicated by the constraints of neural implants such as the impossibility of using large passive components in the design, especially capacitors, disallowing a lot of solutions that would typically be employed in circuit designs outside of neural implants.

In this chapter, we are going to detail the challenges involved in the design of reference circuits in the context of their use in neural implants as well as the compromises this leads to. We are

going to explore some solutions previously presented in literature, followed by presentation of a practical implementation of a reference circuit and a regulator that has been designed for the use in a wirelessly powered neural implant to provide a stable reference voltage in addition to providing a stabilised supply voltage that can be used to power any acquisition and telemetry circuits facilitating the operation of the implant.

5.1 Reference Circuits

A reference circuit is a critical part of many instrumentation circuits that require the precise measurement of a voltage signal that can be referred to a known potential. Arguably, in the context of neural implants, the knowledge of the precise magnitude of the input signal is not critical as much as the knowledge of its shape. This is partly caused by the magnitude of the signal depending on factors that are outside the scope of interest, such as the position of the electrode, as well as the current state of the electrode in terms of its electrochemical condition and mechanical wear and tear. However, in the space of completely wireless implants, the magnitude of the recovered supply voltage can either be entirely unknown or taking a wide range of values and it is therefore necessary to have means of generating a reference signal that is independent of the supply.

Voltage reference circuits achieve this by the use of electronic components' dependence on physical quantities independent of the applied voltage such as the silicon band gap energy, to derive a potential or current that is independent of the supply. The output of a voltage reference is however typically of high output impedance and can not be used to drive large loads. To that end, a voltage regulator, making use of the generated reference, is typically used to drive a large load with the use of a control loop.

5.1.1 Bandgap Reference

One of the most common examples of reference circuits, the schematics of which can be seen in Figure 5.1 can be found in work by A. P. Brokaw [186] from 1974. This circuit, typically called a bandgap reference, or sometimes a bandgap diode due to it being limited to two terminals, produces a stable output voltage close to the energy of a silicon band gap (1.2 eV). The output voltage of the circuit is equal to the sum of base-emitter potential at Q_3 and the voltage drop across R_2. The main feature of the circuit is the fact that the output can be made temperature independent as the base-emitter potential is proportional to absolute temperature (PTAT), while the resistor potential is complementary to absolute temperature (CTAT) and therefore their temperature dependence gradients can cancel out.

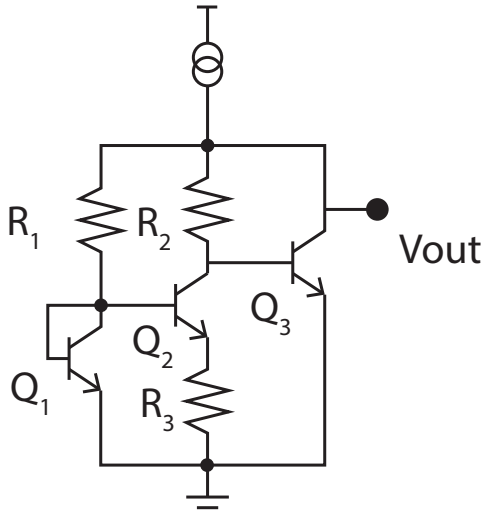

Figure 5.1: Schematic of a typical Bandgap Reference Circuit, based on [186].

Some of the issues that are presented by the use of this circuit include the requirement of using a relatively high supply voltage (higher than 1.2 V) and the problem of its manufacturability in modern CMOS technologies. This is arising from the need to use a fully-floating NPN bipolar transistor Q_2 requiring a deep N-well for its formation in a p-type substrate. Some of those challenges can be overcome by employing a slightly modified version of the circuit that uses other PTAT elements, such as diode [187] or a sub-threshold [188] MOSFET.

In general, the topology however does not solve most of the issues that have to be tackled

in neural implant designs. The main purpose of the bandgap reference is the achievement of temperature independence, a matter that is not necessarily an issue in implanted circuits due to the tissue temperature, and hence the circuit temperature, being regulated by the organism. As noted earlier, a more pressing issue in neural implants arises from the need to reject power supply variation and therefore achieve as high a power-supply rejection ratio (PSRR) as possible.

5.1.2 Beta-Multiplier Reference

Taking a step back, let us first consider the implementation of current references. As seen in Figure 5.1, a bandgap circuit requires a current source in order to generate the output voltage. If the supply voltage is not known, the generation of known currents is equally problematic to the generation of known voltages. A classical example of a self-biased current reference circuit that achieves this is the β-multiplier reference circuit that can be seen in Figure 5.2.

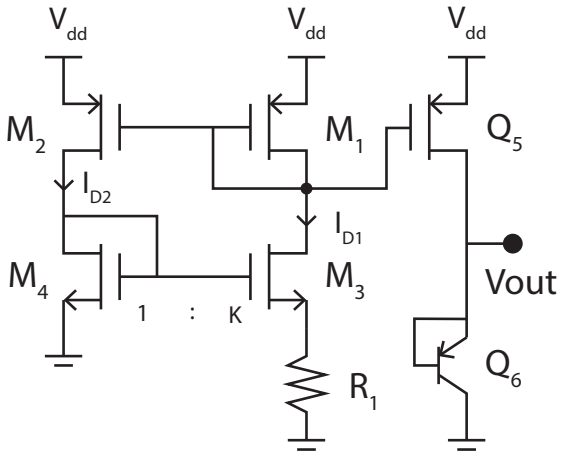

Figure 5.2: Schematic of a typical β-multiplier reference circuit

The current mirror formed of M_1 and M_2 ensures that the drain currents I_{D1} and I_{D2} are equal and so are the drain currents of M_3 and M_4. The gate voltages of M_3 and M_4 are equal as well, the introduction of R_1 however leads to a reduction in V_{gs} of M_3. We also note that the W/L ratio of M_3 is K times larger than that of M_4. If both M_3 and M_4 were operating in weak-inversion saturation, as can be expected in ultra-low-power circuits, the following relationship can be denoted:

$$I_0 \exp\left(\frac{V_g}{nV_t}\right) = I_0 K \exp\left(\frac{V_g - R_1 I_D}{nV_t}\right) \tag{5.1}$$

Solving this for I_D, the drain current can therefore be expressed as:

$$I_D = \frac{\ln(K) \times nV_t}{R_1} \tag{5.2}$$

where n is the gate coupling coefficient and V_t the thermal voltage.

It can be seen that Relationship 5.2 is independent of the supply voltage and therefore the circuit generates current that is only dependent on physical properties of devices and design parameters. It is also worth noting that the system has two possible equilibria, one given by Equation 5.2 and another one at $I_{D1} = I_{D2} = 0$. To prevent the circuit from settling in the undesired equlibrium, the addition of start-up circuits is often necessary. Those ensure that extra current is injected to the circuit if it settles in the undesirable state and are typically based on reverse bias leakage currents. This results in long time constants and therefore might induce a delay in bringing the reference circuit to its operational state after power is supplied to the circuit. This might be undesirable in some applications that require fast start-up time and can be solved by circuits such as [189] that are designed for fast start-up time at a cost of higher complexity.

5.1.3 Reference Voltage Generation

The reference current can then easily be used to generate a reference voltage by obtaining its replica using a current mirror and passing it through a load. A diode-connected PNP transistor, as seen in Figure 5.2, is often employed to make use of the logarithmic dependency of the base-emitter voltage on the collector current and hence reduced dependency of the output voltage on variations of the reference current, thus making the output voltage:

$$V_{out} = V_t \ln\left(\frac{I_D}{I_0}\right) \tag{5.3}$$

where I_0 is the reverse saturation current of the transistor.

There are other examples of reference circuits in the literature [190] that achieve superior temperature independence, such as [191] functioning on the basis of biasing the output transistor to operate in the zero temperature coefficient (ZTC) [192] point. This is a point where the threshold voltage and carrier mobility temperature coefficients cancel out thus leading to operation of the transistor that is independent of temperature. The lack of need for such temperature compensation in neural implants and added complexity of the circuits however does not make them feasible for our needs.

5.2 Voltage Regulators

Having described some of the typically employed circuits to generate supply-voltage independent current and voltage references, we have to consider the need to drive larger loads in order to be able to provide a stable supply voltage. This is achieved by voltage regulators that most commonly follow a structure visible in Figure 5.3. The regulator makes use of a reference voltage and an amplifier to drive a power transistor driving the load, ensuring that the output voltage follows the reference. It is also possible to generate voltages higher than the reference by introducing attenuation in the feedback network.

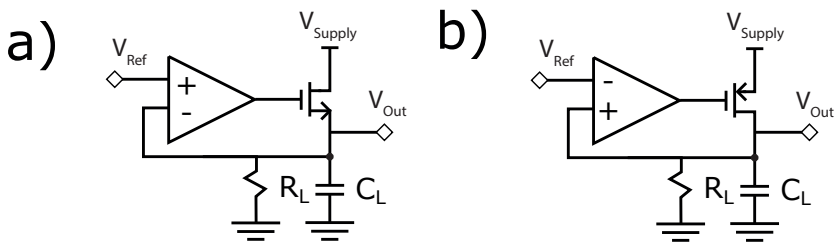

Figure 5.3: Illustration of commonly used basic regulator topologies - a) NMOS-driven regulator b) PMOS-driven regulator

5.2.1 NMOS and PMOS Regulators

In general, there are two structures of voltage regulators used, an NMOS-driven and a PMOS-driven structure. Figure 5.3 a) shows the scenario when an NMOS is used. This has the advantage of a smaller output resistance, given as $1/g_m$ of the output transistor that is further boosted by the gain of the feedback loop making this solution more suitable for driving larger resistive loads. The disadvantage however lies in the need for a higher gate driving voltage that has to be $V_{out} + V_{gs}$. This is not a problem if a large dropout (difference between V_{out} and V_{supply}) is acceptable but becomes an issue in the cases where small dropout and higher efficiency is needed. This issue is sometimes solved by employing a charge pump [193] to drive the gate of the NMOS at higher voltages than the supply. While an effective solution, this increases the complexity of the circuit in addition to opening the possibility of the charge pump operating frequency and harmonics appearing in the output signal.

An alternative solution, visible in Figure 5.3 b) instead relies on the use of a PMOS as the output power element. In this case the load is connected to the drain of the transistor and the output resistance is thus equal to the transistor's output resistance r_{out} multiplied by the gain of the loop. This would typically be larger than the output resistance of an NMOS source and therefore makes the circuit more suitable for powering of smaller loads. The advantage of this configuration is the fact that the gate voltage of the PMOS is independent of the output voltage and therefore the achieved dropout voltage can be smaller without the need to employ additional circuit techniques. To ensure the correct operation of the circuit, the output transistor has to remain saturated, thus not requiring a dropout voltage significantly larger than 100 mV. The simplicity of implementation and the fact that there usually is not a need to drive large loads in neural implants makes this topology often more suitable for those applications.

5.2.2 Feedback Loop Compensation

A challenge that arises in the space of resource-constrained voltage regulators is ensuring the stability of the regulator's feedback loop. As seen in Figure 5.4, the system has two poles

denoted ω_G and ω_L respectively located at the gate of the power transistor and the load. As is the case with any two-pole system, instability is of concern and precautions must be taken to ensure that the two poles are sufficiently separated or another technique, such as the introduction of a zero in the control loop, is employed.

Most conventional PCB-based voltage regulators ensure their stability by placing a large capacitor at the output, thus making ω_L the dominant pole. Such an approach is however not feasible if large external capacitors are not an option, as is the case of neural implants. The requirements placed on the capacitor size are further aggravated by the fact that the output needs to have as small output resistance as possible, resulting in the need for a larger capacitor to maintain the same pole frequency.

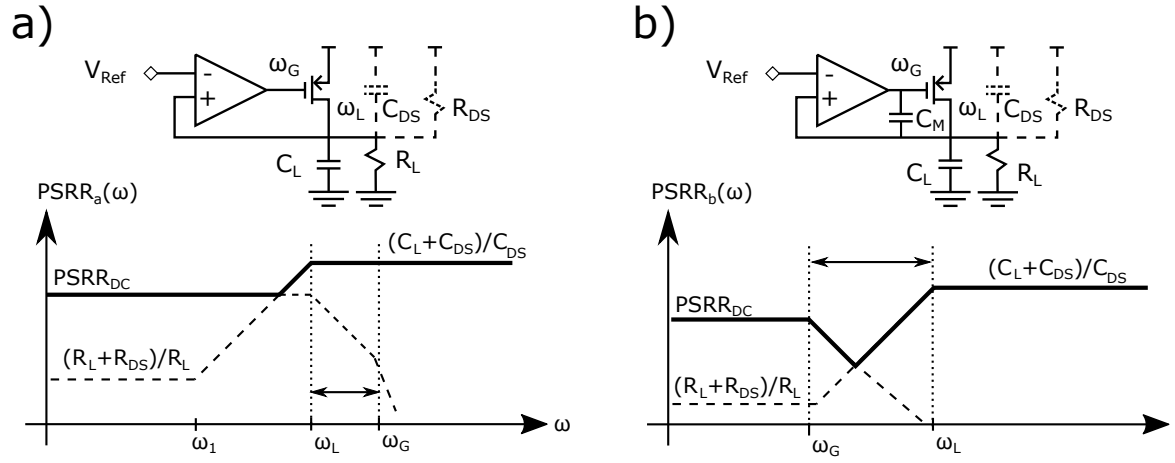

Figure 5.4: Illustration of commonly used regulator topologies alongside the plots of their PSRR - a) Conventional, load-compensated, b) Miller-compensated.

Since the amount of available area in neural implants is limited, the employed strategy often evolves around making ω_G the dominant pole. This is easier to achieve, as the gate of the driving transistor can be made a relatively higher impedance node. Additionally, Miller compensation can be employed making use of gain between the gate of the driving transistor and the load. This achieved boost is, however, often not very high due to the load having low impedance resulting in small overall gain between the gate and the drain of the output transistor. Furthermore, in the case of NMOS regulators, no gain is realised as the transistor operates as a source follower. This can to some extent be alleviated by the use of cascode Miller compensation, connecting the compensation capacitor to an internal node in the amplifier's cascode, thus increasing the

gain seen by the capacitor and the Miller gain factor.

Another issue with making the gate of the output transistor the dominant pole arises from the resulting power supply rejection ratio (PSRR) frequency profile. To evaluate this, we consider that there are two mechanisms that affect the PSRR of the regulator. The first mechanism is a result of passive isolation of the output given by the resistance of the power transistor and the resistance of the load. At the low-frequency asymptote this leads to a PSRR of $(R_L+R_{DS})/R_L$ where R_L is the load resistance and R_{DS} the channel resistance of the transistor. At the high-frequency asymptote the coupling is purely capacitive and is determined by the transistor's drain-source capacitance C_{DS} and the load capacitance C_L. This can be expressed as $(C_{DS}+C_L)/C_{DS}$. At the same time, the low-frequency behaviour is boosted by the feedback loop formed of an operational amplifier and the power transistor that it is driving. If the gain of the loop is sufficient, the PSRR then becomes limited by the either the gain of the loop or the PSRR of the reference itself, whichever is lower.

Let us now consider the behaviour of PSRR in both the cases when ω_L and ω_G are respectively the dominant poles, as illustrated by Figure 5.4. In the case of a more traditional, load-compensated regulator having a dominant pole at ω_L, the passive path dominates the PSRR at frequencies higher than ω_L. Since $\omega_G > \omega_L$, the loss of gain in the feedback loop occurring at frequencies higher than ω_G no longer affects the overall PSRR.

On the other hand, if ω_G is the dominant pole, the gain of the feedback loop becomes reduced in the resistive section of the passive isolation curve and therefore, leads to an undesirable reduction of the overall PSRR. This is restored at even higher frequencies when the capacitive isolation starts dominating the PSRR. The behaviour however leads to a reduction of the PSRR between ω_G and ω_L, an undesirable and largely unavoidable property of Miller-compensated regulators. It is interesting to note that the range of frequencies that see a deterioration of PSRR is dependent on the DC PSRR of the regulator.

This is due to the fact that if the gain of the feedback loop is high enough, the PSRR is determined by the gain of the feedback loop. To achieve stability, the non-dominant pole must lie at a frequency higher than the unity-gain bandwidth of the buffer. Since the gain rolls off

at a constant rate of 20 dB/dec between the two poles, it is easy to see that the separation of the two poles depends on the DC gain of the loop and therefore the DC PSRR. For example a regulator of 80 dB PSRR would require a separation of 4 decades between ω_G and ω_L.

In theory, the reduction of PSRR between the poles can be somewhat mitigated by ensuring the resistive passive rejection path $(R_L+R_{DS})/R_L$ provides as high a PSRR as possible. This is, however, not a practical solution as increasing R_{DS} is undesirable due to it also being linked to the output resistance that has to remain low and decreasing R_L requires a proportional decrease in R_{DS} to allow it to drive the added load.

5.2.3 Solutions Presented in Literature

As outlined above, the design of resource-constrained voltage regulators involves a number of trade-offs that are often difficult to balance. As we have seen, the use of a load-compensated structure is problematic due to the need for large capacitors that are not practical in a fully-integrated system without external components, while the employment of a Miller-compensated design results in a loss of performance at a range of frequencies between the two poles of the system.

There is a number of designs in the literature that attempt to tackle those issues by various techniques. The impossibility of using a large capacitor is solved in [194] by employing an active capacitor multiplier at a cost of increasing the power consumption and bandwidth of the PSRR. Another interesting solution can be found in [195]. This introduces compensation making use of a load replica mimicking the actual and thus partially removing it from the feedback loop. The downside of this implementation is the problematicity of creating the replica especially in cases where the behaviour of the load is difficult to predict.

Another challenge of Miller-compensated regulators is the fact that the maximal permissible amount of capacitive load at the output is limited. This is due to the fact that adding additional capacitance to the output leads to shifting the ω_L pole to smaller frequencies and hence reducing the stability margin. Some designs found in the literature address this problem such as [196]

employing weighted current feedback. Another solution [197] uses a multitude of feedback loops to introduce additional zeros in the system leading to an improvement in its stability. The design in [198] additionally improves the PSRR and drive capabilities by introducing a noise feed forward path driving the body of the power transistors.

5.3 Implementation of Version 1

Most of the reference circuits and regulators presented in literature are designed with the aim to create fully capacitor-less low dropout regulators (CL-LDO). While the use of no capacitors at the output leads to a maximal reduction of the used area, it also means that the high frequency PSRR, above the bandwidth of the feedback loop becomes severely affected. This is typically a problem for the use in wirelessly powered neural implants, as those are often powered by a carrier operating in the free ISM band of 433 MHz or other high frequencies resulting in showt wavelength, thus permitting the use of small power recovery coils. It is thus necessary for the circuit to provide sufficient PSRR at very high frequencies that cover the frequency of the carrier and its harmonics. In this frequency range, the rejection is limited to that given by passive capacitive isolation and is thus reduced to $(C_{DS}+C_L)/C_{DS}$ meaning that C_L has to be maximised.

Maximising C_L however leads to moving the pole ω_L towards smaller frequencies, bringing the circuit into instability and thus has to be compensated by an appropriate increase of the Miller compensation capacitor. If the position of the poles is, however, chosen such that the dominant pole ω_G is at a frequency higher than bandwidth of the acquired signal and ω_L is located below the frequency of the carrier, the effect of the reduction in PSRR between those frequencies can be reduced.

A voltage regulator and reference circuit that has been designed with the help of Dr. Lieuwe Leene as a part of the first prototype of a fully integrated wirelessly powered neural implant facilitating an 8-channel recording of LFPs can be seen in Figure 5.5. This has been created with the aim of achieving maximal simplicity, low power consumption and small area footprint.

The circuit is based on a beta-multiplier reference to generate a supply-independent current source which is then used to generate current passing through a diode-connected PNP transistor generating a reference voltage used by a cascode Miller-compensated PMOS-driven voltage regulator.

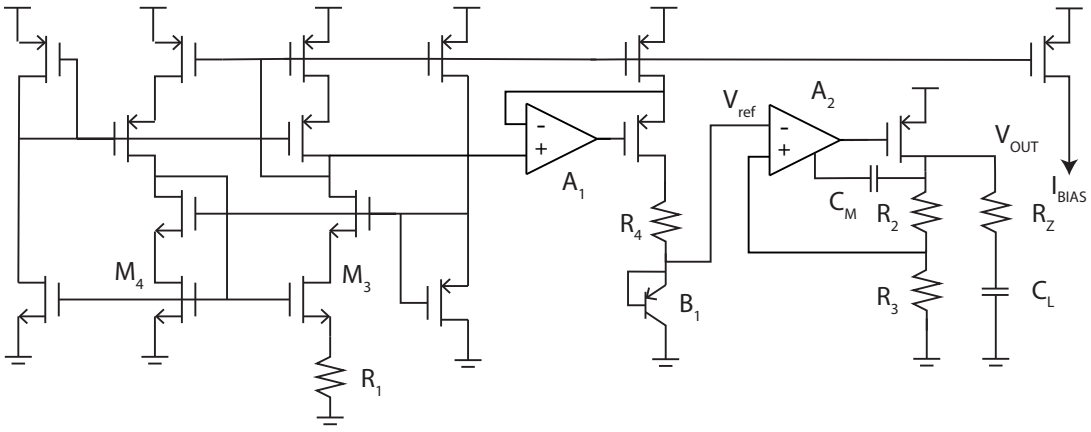

Figure 5.5: Schematic of the implemented reference and voltage regulator. Previously published in [126], modified. Designed with the help of Dr. Lieuwe Leene.

5.3.1 Beta Multiplier Analysis

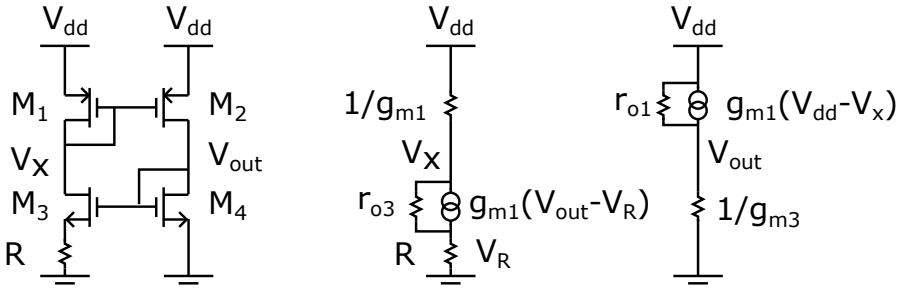

Figure 5.6: Left: Simplified schematic of a beta-multiplier current reference. Right: Small signal model of a beta-multiplier reference.

As the aim of the design is the maximisation of its PSRR, let us first consider how the design has to be adapted to ensure that PSRR is maximised in each of its parts. We begin the analysis by considering the beta-multiplier reference on its own based on a small-signal equivalent circuit seen in Figure 5.6. Assuming that transistor pairs M_1&M_2 and M_3&M_4 are matched, we can express the PSRR as:

$$\frac{v_{dd}}{v_{out}} = \frac{g_{m1}g_{m3}^2 r_{o1}r_{o3}R + g_{m1}g_{m3}R(r_{o1}+r_{o3}) + g_{m3}(r_{o3}+R) + g_{m3}r_{o1} + 1}{g_{m1}g_{m3}r_{o3}R + g_{m1}(r_{o1}+r_{o3}+R) + 1} \tag{5.4}$$

Assuming $g_m r_o >> 1$, $r_{o1} \approx r_{o3}$ and $r_o >> R$, this can be simplified to:

$$PSRR_\beta = \frac{v_{dd}}{v_{out}} \approx g_{m3}r_{o1} \tag{5.5}$$

The result means that the maximisation of PSRR can be achieved by the maximisation of output resistance of all devices in addition to transconductances of the NMOS devices in the circuit. In the design seen in Figure 5.5 this is achieved by the employment of cascodes and long devices in all transistor pairs maximising their output resistance, a result that is in line with an analysis of a similar circuit presented in [199].

The circuit was designed for a quiescent bias current of 800 nA in each branch. All transistors have been sized to operate in the sub-threshold region for maximal transcodundactance efficiency. M_3 and M_4 have been designed such that $(W/L)_4 = 4(W/L)_3$ and therefore, making use of Equation 5.2, resistor R_1 should be ≈39 kΩ. Following parameter sweep simulations, this has later been altered to ≈53.3 kΩ to achieve the desired current and the resistor has been made digitally trimmable to allow configuration in the region of +/- 7%.

The generated reference of 800 nA is copied using current mirrors of attenuation ratio 3/16 in order to generate 8 current sinks of a 150 nA current used to bias other circuitry that is a part of the same neural implant system.

5.3.2 V_{be} Reference Analysis

Having analysed the beta-multiplier reference, we have to perform a similar analysis on the V_{be} reference used to generate a reference voltage from the reference current. The output voltage of the reference circuit is affected by two different contributions v_{be1} and v_{be2} of power supply variation v_{dd}. One contribution is directly due to a potential divider formed by the current

mirror and the diode-connected transistor B_1 and can be denoted as:

$$v_{be1} = v_{dd} \times \frac{1}{1 + g_{mB}(R_o + R_4)} \tag{5.6}$$

where g_{mB} is the transcoductance of B_1 and R_o the output resistance of current mirror reflecting the current from the beta-multiplier reference.

The second contribution is caused by the transconductance between the power supply and the output current of the reference through a current mirror. The output of the current mirror can be expressed as:

$$i_o = G_m(v_{dd} - v_x) \tag{5.7}$$

where G_m is the transconductance of the current mirror's output transistor and v_x the potential at its input as seen in Figure 5.6. While obtaining a precise relationship between v_x and v_{out} or the beta-multiplier reference is complicated, it can easily be seen that $v_x/v_{dd} \approx (1-\alpha/PSRR_\beta)$ where α is on the order of -(3-6) dB. The contribution to the output of the voltage reference is thus:

$$v_{be2} = v_{dd} \times \frac{\alpha G_m}{PSRR_\beta \times g_{mB}} \tag{5.8}$$

The PSRR of the v_{be} reference can thus be denoted:

$$\frac{1}{PSRR_{BE}} = \frac{v_{be1} + v_{be2}}{v_{dd}} = \frac{1}{1 + g_{mB}(R_o + R_4)} + \frac{\alpha G_m}{PSRR_\beta \times g_{mB}} \tag{5.9}$$

This shows that the PSRR of the voltage reference circuit can not be higher than the PSRR of the current reference and can be further deteriorated by passive contributions due to v_{be1}. From the circuit design perspective this means that the beta-multiplier reference has to be designed for as high a PSRR as possible and the passive isolation of the v_{be} reference has to be on a

similar order to ensure the PSRR is not further deteriorated.

The design seen in Figure 5.5 maximises R_o and thus the passive isolation by employing a gain-boosted current mirror. While providing superior R_o, this design decision has led to unnecessary overdesigning of the circuit due to the PSRR of the overall reference circuit being limited by the PSRR of the beta-multiplier instead making use of plain cascodes rather than gain-boosted ones.

Resstor R_4 seen in Figure 5.5 has been added to the current path to slightly increase the passive isolation. According to simulated results, the v_{be} reference generates an output voltage of $\approx$ 585 mV.

5.3.3 Voltage Regulator

A voltage regulator has been implemented using the output of the v_{be} reference as a reference voltage in addition to employing a feedback loop with attenuation to ensure that the regulator outputs a nominal voltage of 1.2 V. A telescopic amplifier with NMOS input has been designed to drive the power transistor. The design employs a compensation capacitor C_M of 2 pF and a load capacitor C_L of 78.75 pF. Additionally a nulling resistor R_Z of 266.6 kΩ has been placed in series with the load capacitor as seen in Figure 5.5 to introduce an additional zero in the transfer function of the feedback loop, thus improving the stability margin.

5.3.4 Power Supply Indicators

The reference circuit has additionally been complemented with a circuit providing digital indications of the harvested power supply reaching a sufficient voltage. This is used to enable the operation of certain subsystems such that their operation is reliable and the inductive load is not prematurely subjected to load. Three different indicator levels - 1.05 V, 1.3 V and 1.5 V have been implemented to respectively enable the digital circuitry, the load shift keying (LSK) mechanism facilitating data transmission and power regulation mechanism if the supply voltage is to exceed 1.5 V.

Since 1.05 V is smaller than the output voltage of the LDO and the operation of the bandgap reference cannot be guaranteed at such a small supply voltage, an undervoltage lockout (UVLO) circuit described in [200] has been used. Since the value of the threshold voltage depends on threshold voltages of the employed transistors, this indicator is more susceptible to manufacturing process and temperature variations. The remainder of the indicators are implemented by comparing the supply voltage with the output of the v_{be} reference leading to significantly smaller variations in the indicator trigger voltage.

5.4 Results of Version 1

The described circuit has been implemented in a commercially available 0.35 µm CMOS technology and manufactured as a part of a complete neural implant prototype presented in [126] alongside contributions of other authors. A microphotograph of the designed circuit alongside a detailed view of the core layout, occupying an area of 750 µm × 250 µm can be seen in Figure 5.7.

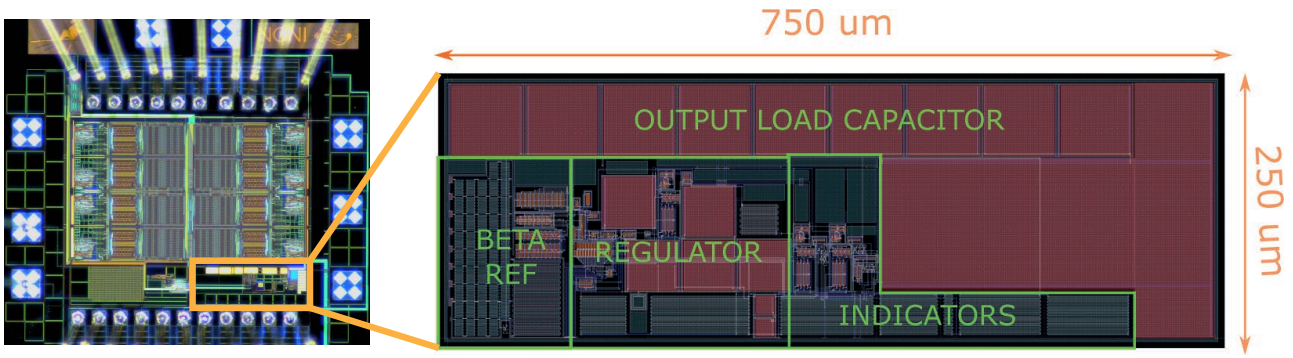

Figure 5.7: Left: Microphotograph of a manufactured system containing the implemented reference circuit and regulator. Right: Detail of the layout of the implemented reference circuit and regulator exported from Cadence Virtuoso

This section is going to present the results obtained during evaluation of the circuit including both simulations and measurements. While the circuit was evaluated by measurements, some metrics were obtained by simulations due to the inaccessibility of some internal signals for bench testing.

The measurements were done using a printed circuit board (PCB)-based platform seen in

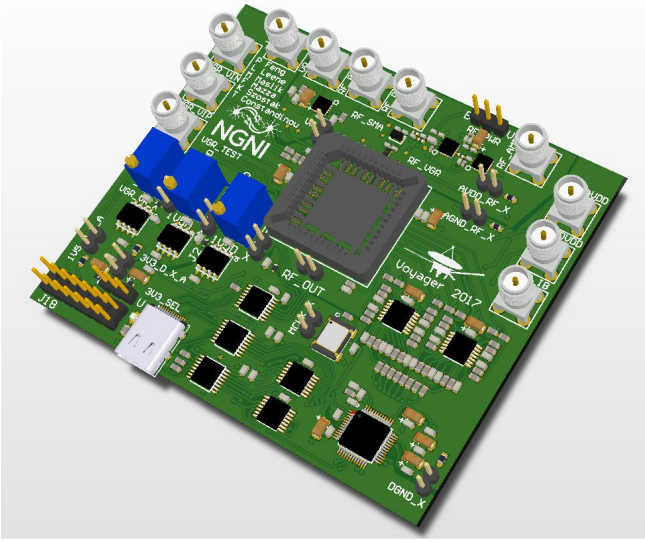

Figure 5.8: Platform Used for Testing of the Designed Reference Circuit

Figure 5.8 that was designed in order to perform measurements of the complete neural implant system that, apart from the designed regulator and reference circuit includes a power harvesting system, rectifier, and an 8-channel neural acquisition system with load shift keying. To enable the testing of all of the system's components, the platform contains a 24-bit 8-channel $\Sigma\Delta$ DAC to provide input stimuli and a set of 3 low-dropout regulators (LDOs) to generate supply voltage in three different domains to power all circuits on the platform itself as well as to provide power supply to the device under test if the internal regular is to be bypassed. During testing, the platform is connected to a Raspberry Pi platform which provides the stimuli signals over an I2S bus.

To test the performance of the on-chip voltage regulator, all decoupling capacitors on the PCB were disconnected using the on-board jumpers and the power supply to the integrated circuit was provided from an external power supply injecting a sinusoidal signal at various frequencies. The output was then recorded using an oscilloscope and the results analysed to obtain an estimate of PSRR across the tested range of frequencies. The measured result can be seen in Figure 5.9 alongside simulated results obtained by performing a Monte Carlo analysis of 500 runs simulating both device mismatch and process variations.

This showed that the measured PSRR follows the predicted frequency profile, with a reduction at frequencies higher than ω_G. The measured PSRR is, however, about 15-20 dB worse than

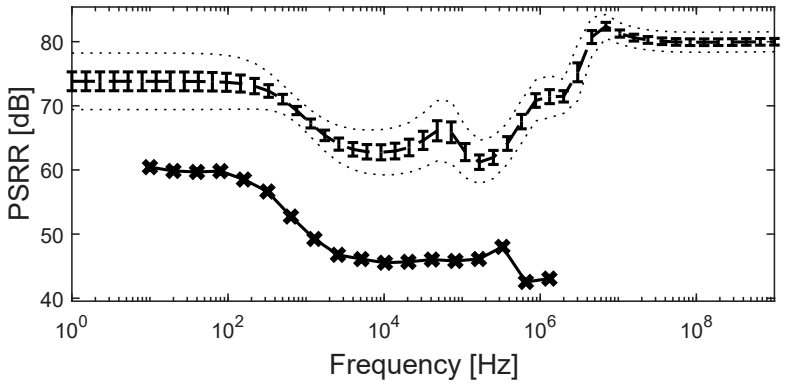

Figure 5.9: Top (Dashed): Simulated results of the designed voltage reference obtained during 500 Monte Carlo Iterations alongside standard deviation (Error Bars) and Min/Max (Dotted). Bottom (Solid): Measured PSRR

expected from the simulation results. This was subjected to further simulation analysis that showed this to be a result of insufficient substrate grounding leasing to added resistance in ground paths as well as the equivalent series resistance (ESR) of the used poly-silicon-based capacitors. Those deficiencies were addressed in the second version of the circuit alongside other improvements.

	μ	σ	σ/μ	min	max
V_{REF}	1.207 V	9.9 mV	0.82%	1.174 V	1.241 V
I_{Out}	150.0 nA	15.1 nA	10.06%	101.6 nA	195.1 nA
I_{dd}	5.17 μA	407.7 nA	7.89%	4.2 μA	6.4 μA
ΔI_{Out}	0.3 nA	5.3 nA	5.66%	-16.7 nA	15.6 nA
V_1	1.053 V	91.84 mV	8.71%	826 mV	1.264 V
V_1_3	1.295 V	11.66 mV	0.90%	1.254 V	1.334 V
V_1_5	1.495 V	13.66 mV	0.91%	1.453 V	1.495 V

Table 5.1: Summary of obtained Monte Carlo post-layout simulation results. ΔI_{Out} represents the difference between any two copies of I_{Out}.

To assess the variation of some of the generated signals a Monte Carlo analysis of runs was performed and the resulting statistics recorded in Table 5.1. This shows that the current consumption of the circuit is approximately 5.17 µA under no-load conditions and a supply voltage of 1.4 V. The standard deviation (std) of the output reference voltage is smaller than 1% of the mean value, demonstrating the small susceptibility of v_{be} references to process variations. The std of the output current, and the output of the beta-multiplier reference, is approximately 10% of the mean value. Such a result is expected [201] as the output current of the reference depends on the threshold voltage of the used devices in addition to resistance of the on-chip poly-silicon resistors, both of which are subject to significant process variations. However, if

we consider the variation between two different current sinks on the same chip, ΔI_{Out}, we see that the the std reduces to approximately 3.3%, a more favourable result.

This also shows the difference in variations between the voltage level indicator derived from the threshold voltage of a transistor used to implement a 1.05 V UVLO, reaching an std of 8.7% and the voltage level indicators derived from the output of the v_{be} reference. Both of those indicators, configured for the detection of the power supply crossing 1.3 V and 1.5 V show an std of less than 1%.

Another metric that is a cause for concern with regards to manufacturing variations is the stability of the control loop in the voltage regulator. This was evaluated by Monte Carlo simulations and the magnitude and phase plots of the loop gain can be seen in plotted in Figure 5.10 under a no-load condition and under a load of 1 µA. This demonstrates that the control loop remains stable under all corners in addition to demonstrating the effect of zero ω_z added by the use of a nulling resistor R_z.

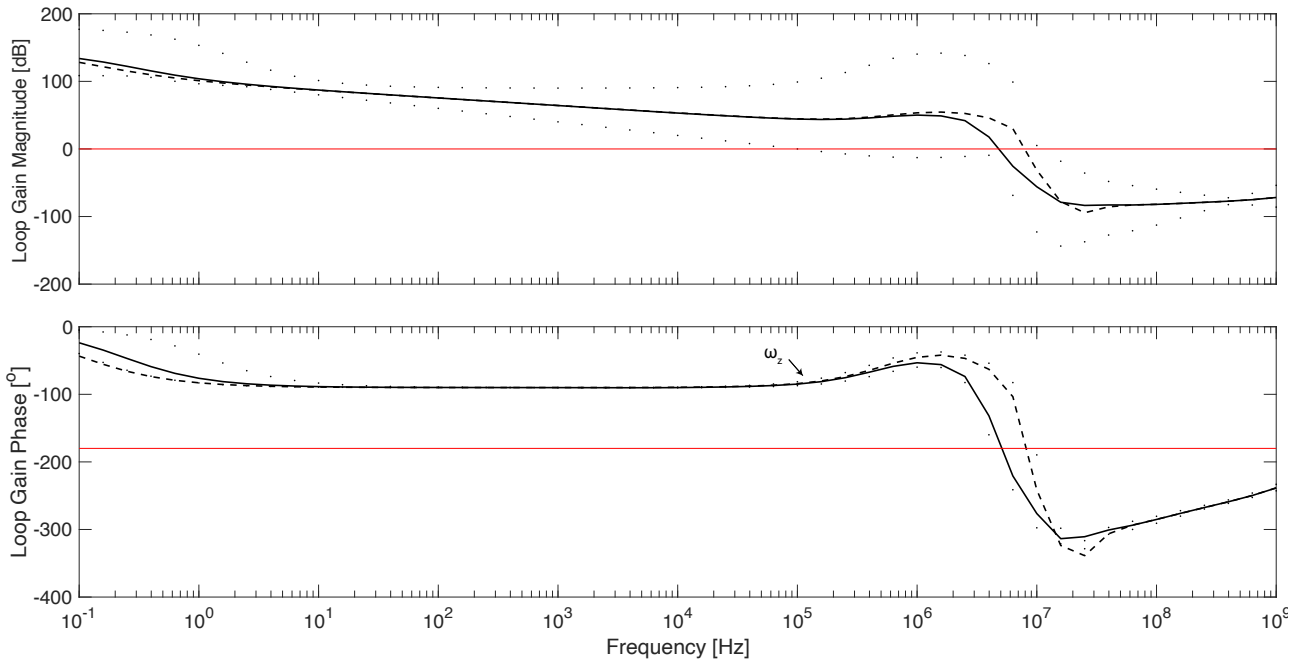

Figure 5.10: Loop gain of the control loop - Top: Magnitude, Bottom: Phase; Solid line: Mean (No load), Dashed line: Mean (1 µA Load), Dotted: Minima and maxima, Red line: 0 dB Magnitude, -180^o Phase.

The phase margin statistics obtained from Monte Carlo simulations can be seen in Table 5.2. This shows that the circuit remains stable under all corners with a phase margin of at least 90^o.

In addition, both Figure 5.10 and Table 5.2 demonstrate an increase in stability under load conditions. This is due to the fact that higher current passing through the output transistor results in a decrease of its resistance and therefore pole ω_L shifts to higher frequencies, further away from ω_G. This is an advantage of Miller-compensated regulators resulting in their stability increasing under heavier load, as opposed to traditional regulators, the stability of which deteriorates under heavy loads.

	μ	σ	σ/μ	min	max
Phase Margin (No Load)	98.14^o	0.92^o	0.94%	94.7^o	100.5^o
Phase Margin (1 µA Load)	99.18^o	0.68^o	0.69%	96.7^o	101.0^o

Table 5.2: Results of Monte Carlo simulations of the control loop's phase margin.

Furthermore, the testing revealed another issue of this design which became apparent only when used in connection in a particular load exerted by the the complete neural implant. Since a part of the neural acquisition front-end relies on the use of switched capacitor circuits, transient currents are sometimes injected into the output of the regulator. The designed topology is, however, unable to perform under such a condition as it is only able to sink current through the feedback resistor on the order of MΩ resulting in output voltage spikes and transients if the output current is negative.

5.5 Implementation of Version 2

Since the first version of the circuit did not perform as expected in some areas, such as the PSRR being smaller than expected in addition to it being unable to facilitate the powering of circuits injecting current into the output of the regulator, a second version of the circuit was designed.

The schematic of the new circuit can be seen in Figure 5.11. The changes include the removal of amplifier A_1 and the replacement of a gain-boosted current mirror in the v_{be} reference by a simple cascode which, as explained earlier, does not lead to deterioration of PSRR. To allow the regulator to operate under a negative output current, or negative load, the PMOS-driven voltage regulator has been replaced by a push-pull structure inside amplifier A_2 seen in

Figure 5.12. Additionally, the poly-silicon load capacitor C_L has been replaced by a combination of a Metal-Oxide-Semiconductor (MOS) capacitor C_{L2} providing high capacitance of high ESR and a Metal-Oxide-Metal (MOM) capacitor C_{L1} providing a smaller resistance of small ESR.

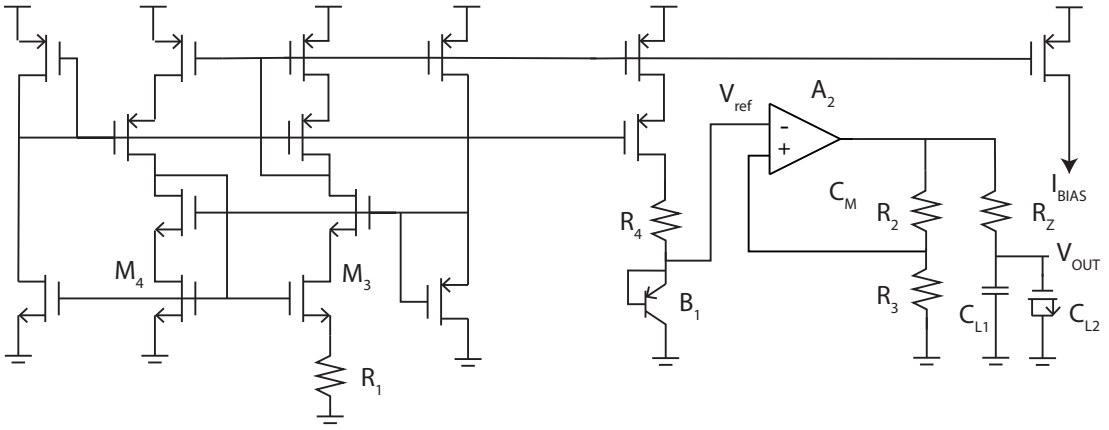

Figure 5.11: Schematic of the implemented 2nd version of the reference and voltage regulator. Designed with the help of Dr. Lieuwe Leene.

5.5.1 Output Amplifier Implementation

The implementation of amplifier A_2 providing the output of the LDO can be seen in Figure 5.12. The amplifier consists of three stages, where the purpose of the first stage is to facilitate a fully differential input and a small gain, the second stage leads to high gain and the third stage is designed to drive the output load.

In order to ensure that the control loop remains a two-pole system, the input stage is designed to have a small gain and a small output impedance. To this end, a fully differential structure with a diode-connected load is used. Assuming that transistor pairs M_1&M_2 and M_3&M_4 are matched, the gain of the structure can be denoted $\approx g_{m1}/g_{m3}$ and the output impedance is $\approx 1/g_{m3}$ ensuring that the pole of this stage lies at a high frequency.

The second stage consists of a high gain common-source configuration with a cascode load that ensures high gain of the feedback loop leading to high PSRR. The output pole of this stage, ω_G, is the dominant pole of the circuit, similarly to the previous implementation.

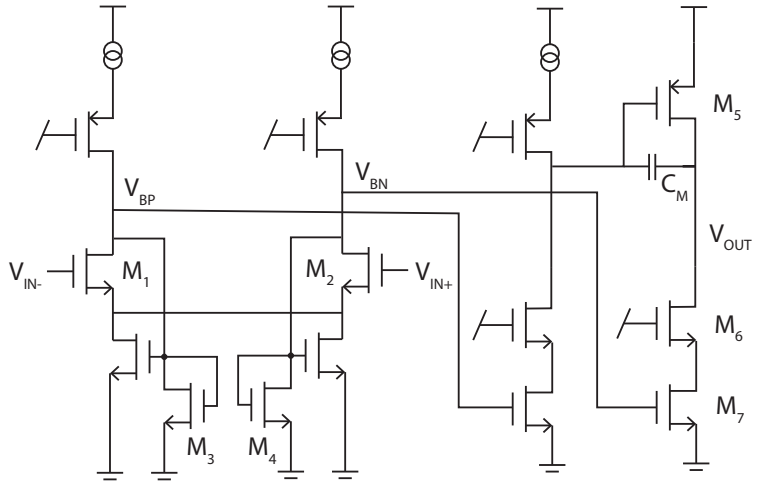

Figure 5.12: Schematic of the implemented output amplifier A_2.

The last stage driving the load consists of a power PMOS M_5 driving current to the load. A capacitor C_M is connected between the output of the third stage and the second stage, thus introducing Miller compensation. To prevent the issue of the earlier design that was unable to support negative load current, transistor M_7 is added facilitating the sinking of current from the output. This is driven by signal V_{BN}, the inverting output of the first stage. If the output voltage rises as a result of injected current, V_{BN} rises as well, increasing the gate voltage of M_7, rising the drain current and thus providing a return path for the injected current.

5.5.2 Load Capacitor

As the previous implementation showed unexpectedly low PSRR which was partly identified to have been caused by high ESR of the employed polysilicon load capacitors, the 2nd version of the circuit instead uses a combination of MOS and MOM capacitors occupying an area of 420 µm × 450 µm. A total of 99 MOS capacitors of 39.5 µm × 42.8 µm each of 7.71 pF (4.56 fF/µm^2) were used, leading to a total of 763.3 pF capacitance. The area occupied by the MOS capacitors was additionally filled by a 4-layer structure of interdigitated metal fingers creating a MOM capacitor of 81.4 pF (0.43 fF/µm^2).

5.6 Results of Version 2

The 2nd generation of the designed circuit has been implemented in a commercially available CMOS 0.35 µm technology similar to that used in version 1. The core occupies area of 634 µm × 450 µm and a microphotograph of the manufactured circuit alongside a detail of the layout can be seen in Figure 5.13. It can be seen that the majority of the circuit's area is occupied by the load capacitor. This can potentially be reduced depending on the amount of spare area available.

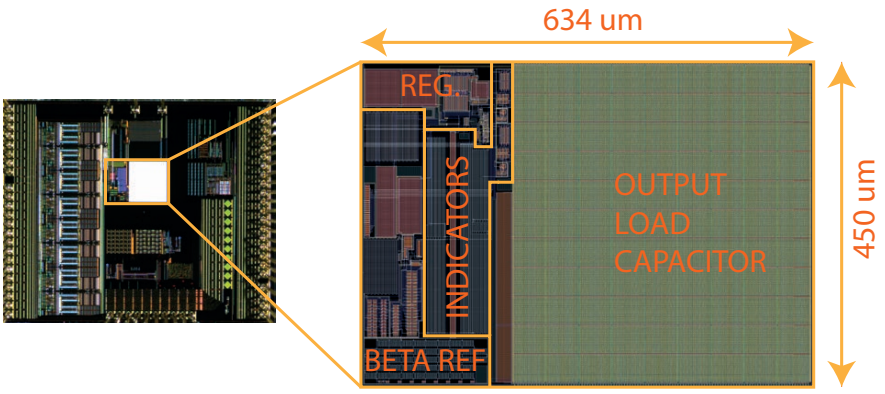

Figure 5.13: Left: Microphotograph of a manufactured system containing the implemented 2nd generation of the reference circuit and regulator. Right: Detail of the layout of the implemented reference circuit and regulator exported from Cadence Virtuoso.

The performance of the design was at first evaluated using post-layout Monte Carlo simulations of 500 runs having extracted parasitic capacitances as well as resistances to prevent the degradation of PSRR seen in the previous design due to insufficient substrate grounding. The obtained PSRR, including the statistics resulting from the Monte Carlo run can be seen in Figure 5.14. This shows a mean low-frequency PSRR of ≈72 dB and a high-frequency PSRR of ≈53 dB in addition to a reduction of PSRR between the frequencies of ≈ 1 kHz and ≈ 1 MHZ that correspond to the locations of poles ω_G and ω_L respectively.

The statistics of other output metrics due to process variations, obtained in post-layout Monte Carlo simulations can be seen in Table 5.3. These results do not significantly differ from those observed in the first version of the circuit since a majority of the components affecting those remains the same. The output bias current has been reduced to ≈ 95 nA due to changes in the

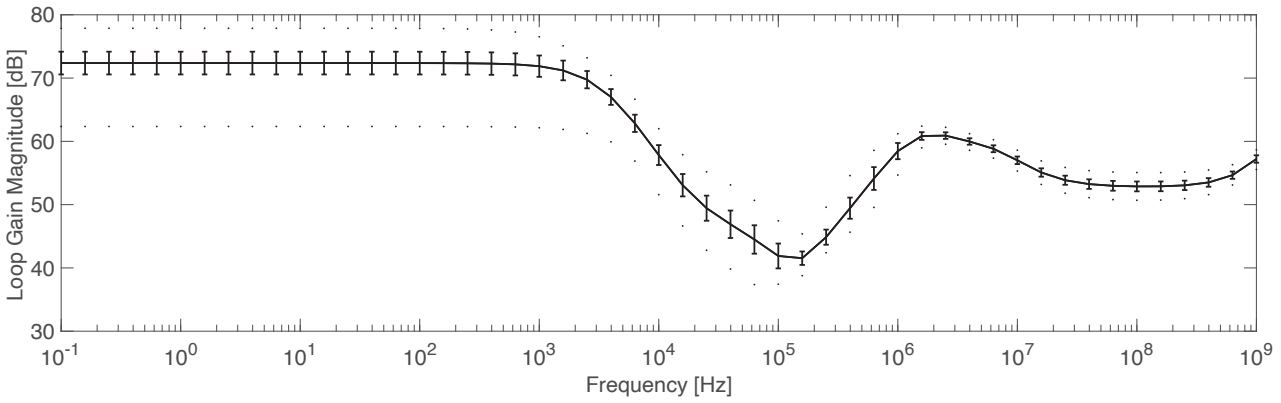

Figure 5.14: PSRR of the 2nd version of the voltage reference and regulator. Statistics are obtained from a post-layout Monte Carlo simulation of 500 runs. Solid line - mean, error bars - standard deviation, dotted line - min and max

circuit the reference and regulator is used by.

	μ	σ	σ/μ	min	max
V_{REF}	1.199 V	10.14 mV	0.85%	1.167 V	1.226 V
I_{Out}	93.8 nA	10.81 nA	11.52%	66.6 nA	124.1 nA
I_{dd}	5.68 μA	477.5 nA	8.41%	4.4 μA	7.0 μA
ΔI_{Out}	0.0 nA	5.9 nA	0%	-20.2 nA	17.3 nA
V_1	1.065 V	89.56 mV	8.41%	875 mV	1.264 V
V_1_3	1.3 V	11.45 mV	0.88%	1.334 V	1.334 V
V_1_5	1.5 V	14.17 mV	0.94%	1.543 V	1.495 V

Table 5.3: Summary of obtained Monte Carlo post-layout simulation results of the circuit's 2nd version. ΔI_{Out} represents the difference between any two copies of I_{Out}.

To evaluate the improvement in performance in the use case when current is pushed to the output of the regulator, a transient simulation has been carried out demonstrating the effect of injecting a 1 µs pulse of 10 µA to the output. The resulting voltage transient of the output voltage in both the old and the new version of the circuit can be seen in Figure 5.15. This shows a reduction of the transient from $\approx$ 148 mV to $\approx$ 28 mV in addition to a reduction of the settling time from $\approx$ 100 ns to $\approx$ 17 ns.

The stability of the control loop has been evaluated by performing a post-layout Monte Carlo simulation establishing the phase margin under no load conditions and under a load of 1 µA. The obtained phase margin and gain of the loop can be seen in Table 5.4 and Figure 5.16 respectively. This shows that the phase margin remains above 59.75^o in all cases, thus providing a sufficient margin of stability.

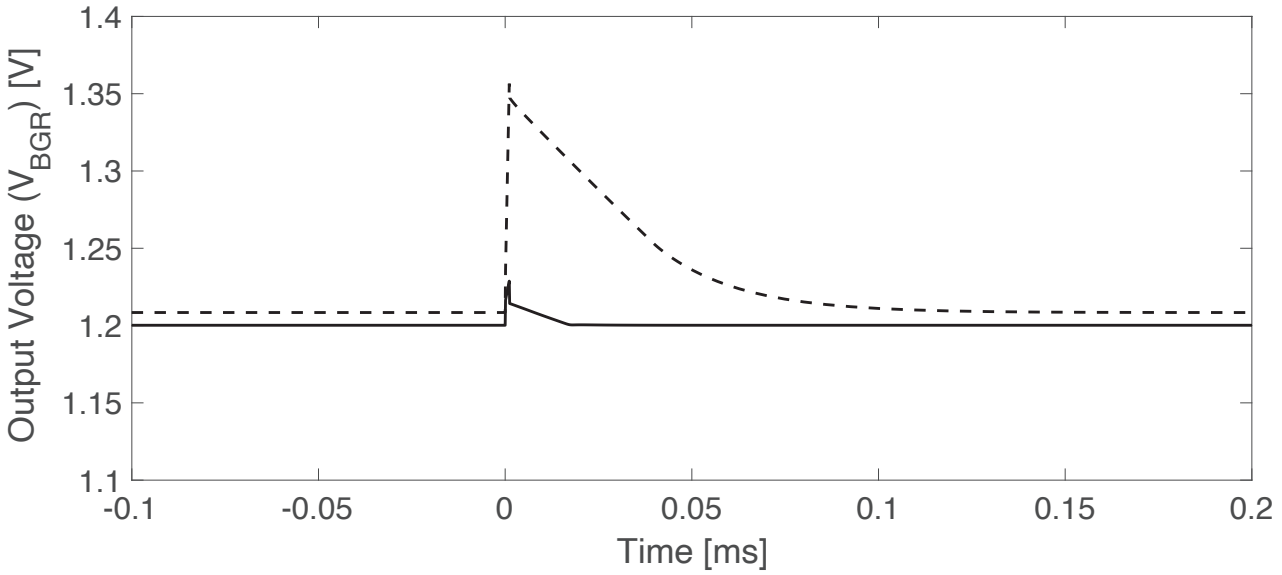

Figure 5.15: Plot of a transient at the output of the regulator resulting from an injection of a 1 µs pulse of 10 µA, simulating the effect of using a switched-capacitor circuit. Solid line - Version 2, Dashed line - Version 1

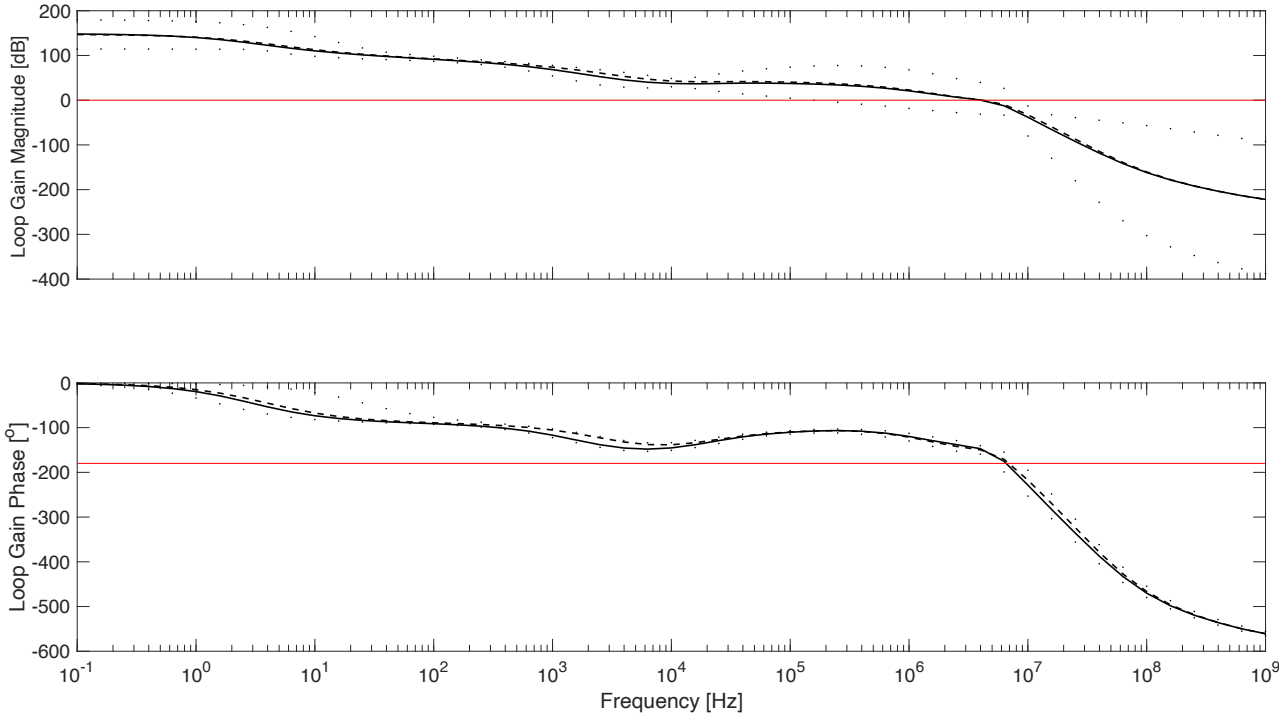

Figure 5.16: Loop Gain of Version 2 of the Control Loop - Top: Magnitude, Bottom: Phase; Solid Line: Mean (No Load), Dashed Line: Mean (1 µA Load), Dotted: Minima and Maxima, Red Line: 0 dB Magnitude, -180^o Phase.

5.6.1 Voltage Reference Measurements

Following simulations and having received the manufactured integrated circuit, the design has been further evaluated by measurements. At first a fixed supply voltage V_{dd} of 1.4 V was

	μ	σ	σ/μ	min	max
Phase Margin (No Load)	68.61^o	3.17^o	4.62%	59.75^o	75.98^o
Phase Margin (1 µA Load)	72.66^o	2.03^o	2.79%	67.1^o	77.6^o

Table 5.4: Results of Monte Carlo Simulations of Version 2 of the Control Loop's Phase Margin

applied and the output reference voltage V_{bgr} was measured to be ≈1.187 V. A bias of 1 V was then applied to one of the internal current sinks and the sunk current was measured to be 96.57 nA.

To measure the PSRR, an experimental setup visible in Figure 5.17 has been used. A Tektronix AFG3102 arbitrary signal generator has been used to generate a pure tone of 1 V peak-to-peak voltage and a a 2 V offset. The output frequency has been varied and the output of the reference circuit has been recorded using a LeCroy Wavesurfer 434 oscilloscope. The Device Under Test (DUT) was packaged in an JLCC84 package and placed in a test PCB seen in Figure 5.18 allowing for a connection of both the input power supply and the output reference voltage using BNC connectors.

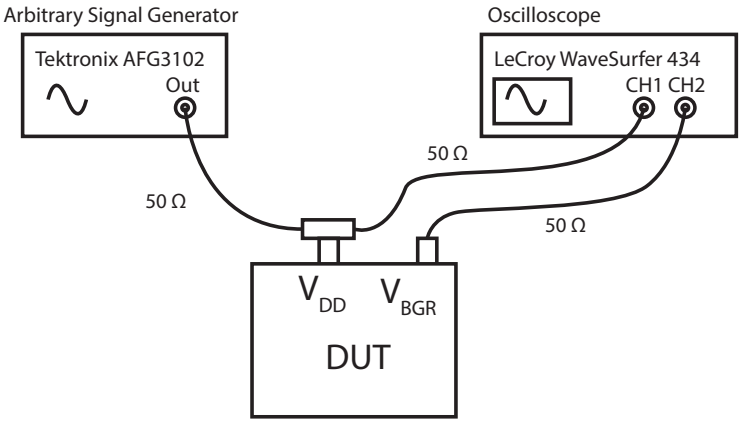

Figure 5.17: Test setup used to measure the PSRR of the reference circuit.

The recorded signals have then been analysed in Matlab extracting the power of the carrier signal in both the input as well as the output and calculating the PSRR as their ratio. The resulting PSRR seen plotted in Figure 5.19 shows a low frequency measured value of ≈53 dB, decreasing to a minimum of ≈33 dB at high frequencies before rising again. While the frequency profile roughly follows the results expected from simulations, the resulting PSRR is lower than what was expected.

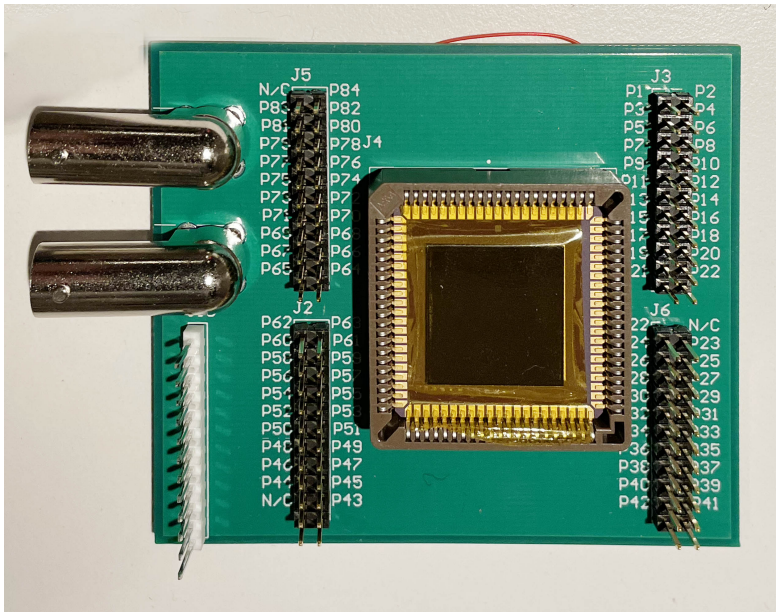

Figure 5.18: Photograph of the Used Testing PCB.

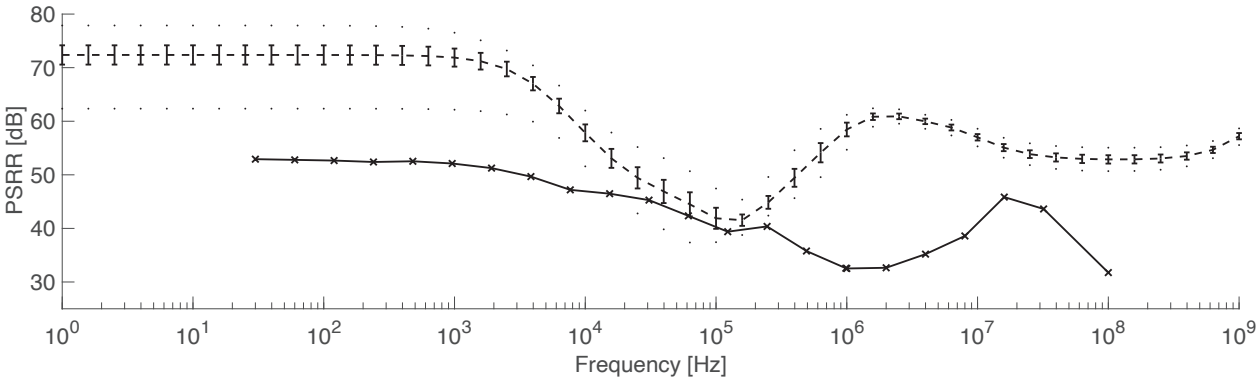

Figure 5.19: Top (Dashed): Simulated results of the designed voltage reference V2 obtained during 500 Monte Carlo Iterations alongside standard deviation (Error Bars) and Min/Max (Dotted). Bottom (Solid): Measured PSRR

This has been subjected to further analysis in an attempt to determine the reasons. To rule out any influence of the oscilloscope's 1 MΩ input impedance, the measurement has been repeated using an SRS SR560 Low-Noise Voltage Amplifier of a 100 MΩ input impedance as a buffer. This has produced the same result as the original measurement. Furthermore, to ensure the discrepancy is not caused by experimental setup problems, the low-frequency PSRR has been verified by applying a varying DC supply voltage and measuring the output reference voltage. This has confirmed the result obtained by applying a sinusoid.

Further simulations in Cadence Virtuoso with extracted parasitics as well as foundry-provided

models of the used I/O cells with ESD protection were carried out. Even with extended Monte Carlo runs it has not been possible to explain the reduced performance as all simulation results suggest higher PSRR than the measured result.

5.6.2 Current Source Measurements

Following the characterisation of the voltage reference, the current source has been characterised as well using experimental setup seen in Figure 5.20. A Keithley 2000 precision multimeter has been set up to supply a voltage of 1.0 V and connected through a 2 MΩ shunt resistor to the current sink of the DUT located on the testing PCB. The voltage drop across the 2 MΩ resistor has then been amplified using an SRS SR560 low noise amplifier of a 100 MΩ input impedance and recorded using a Lecroy WaveSurfer 434 oscilloscope.

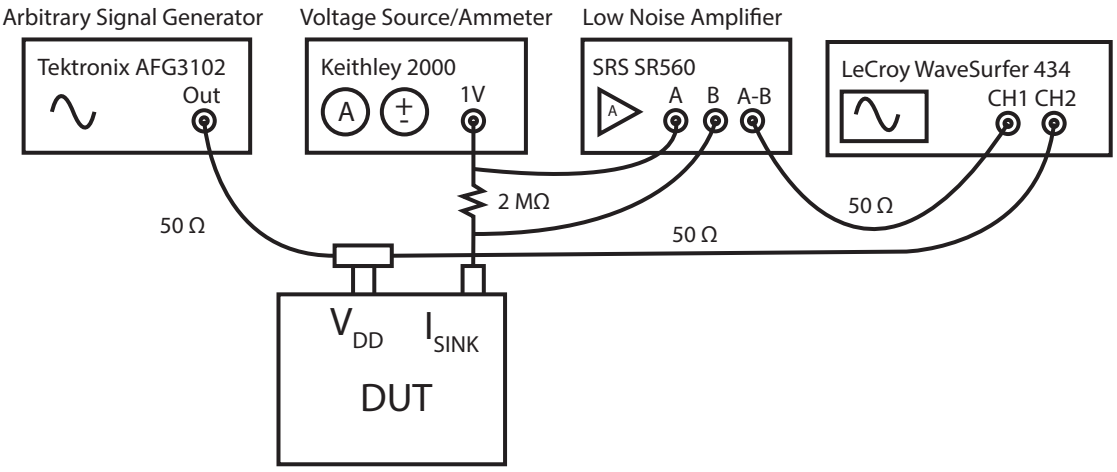

Figure 5.20: Test Setup Used to Measure the PSRR of the Current Reference Circuit.

This setup has been used to obtain the PSRR of the current sink defined as PSRR = v_{vdd}/i_{out} by generating a 1 V peak-to-peak sinusoid with a 2 V offset of varying frequency and applying it as a supply voltage to the DUT while recording the variations in the sunk current. The measured PSRR in relation to frequency can be seen in Figure 5.21 alongside simulated results obtained in a post-layout Monte Carlo run of 500 samples.

This shows that the low-frequency (<1 kHz) PSRR is in agreement with simulations, while the measured values at higher frequencies are better than expected. Such a result can be explained

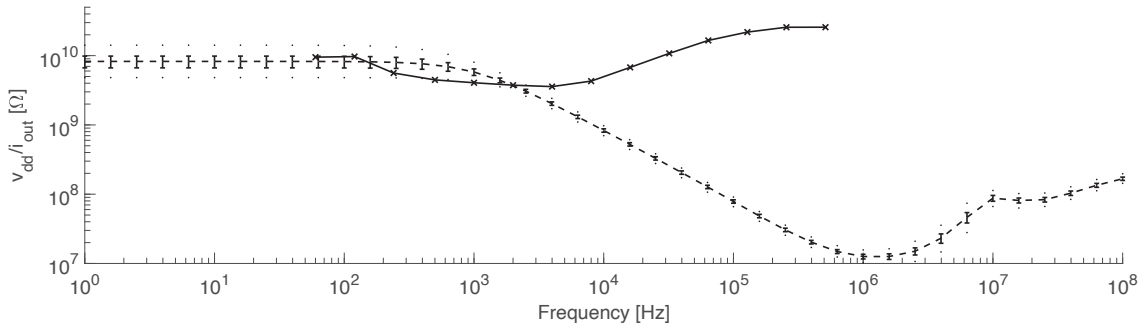

Figure 5.21: Top (Dashed): Simulated PSRR of the designed current reference V2 obtained during 500 Monte Carlo Iterations alongside standard deviation (Error Bars) and Min/Max (Dotted). Bottom (Solid): Measured PSRR.

and is likely caused by the inductance of the leads connecting the DUT to the shunt resistor preventing current variations and modifying the high frequency behaviour of the system.

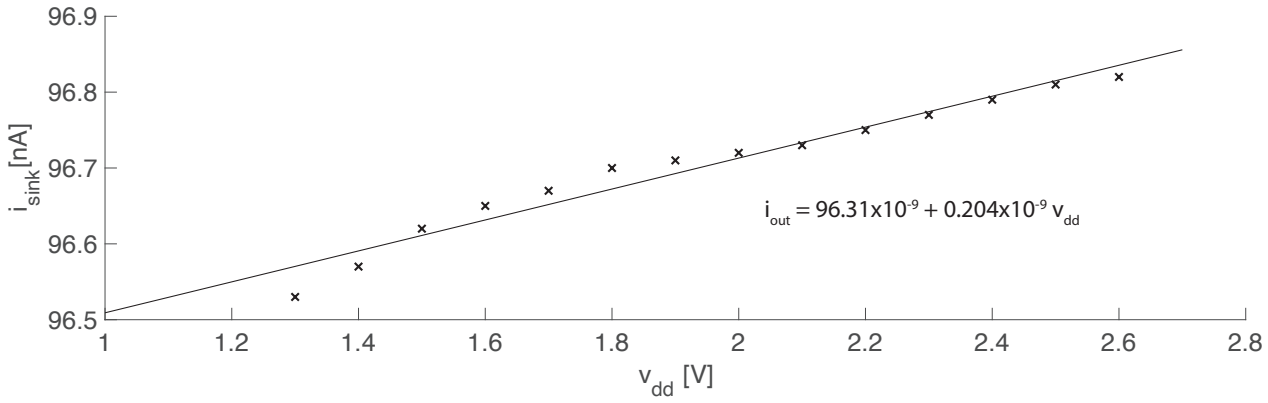

Figure 5.22: Crosses: Measured reference current sink vs supply voltage under V_{bias}=1.0 V. Solid: Linear line fitted through the measurements.

In a further experiment, DC supply voltage has been applied and varied while recording the output sunk current. The obtained values can be seen plotted in Figure 5.23 alongside the best linear least-square fit. The slope of the curve indicates a DC PSRR of $\approx 4.9 \times 10^9$ Ω, a value in agreement with the result obtained in low-frequency AC measurements.

Finally, the supply voltage has been fixed at 1.4 V and the bias voltage applied at the current sink varied from 0 to 1.0 V while recording the sunk current. The measured values visible in Figure 5.23 show the current sink requires a bias voltage of $\approx$ 0.2 V to saturate and once saturated has an output resistance of $\approx$ 346.5 MΩ.

Those results demonstrate that while the voltage reference showed a smaller PSRR than ex-

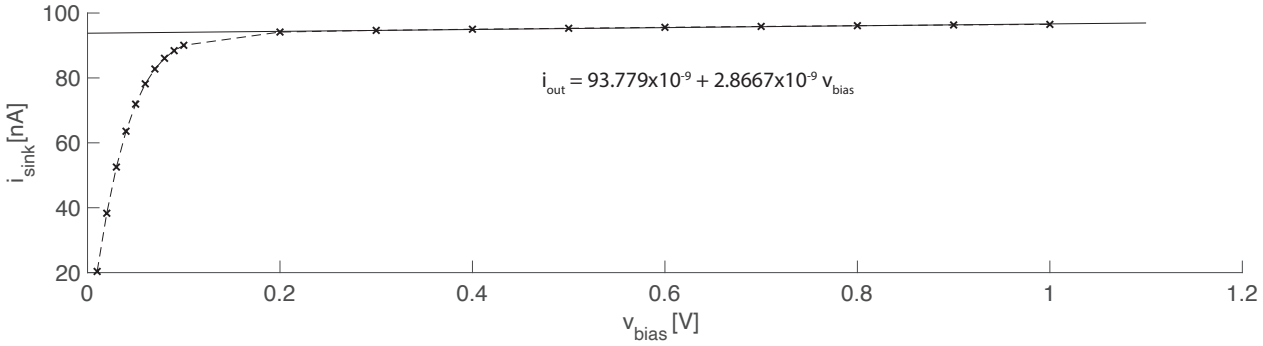

Figure 5.23: Crosses: Measured Reference Current Sink vs Applied Bias, V_{dd}=1.4 V. Solid: Linear line fitted through the measurements.

pected, the current reference performs fully as predicted by simulations.

5.7 Conclusion

Some of the challenges that arise in the development of reference circuits and voltage regulators in the constrained space of neural implants have been explored in this chapter. It has been shown that some of the greatest challenges stem from the inability to manufacture large capacitors leading to impossibility of using the classical strategy of achieving the stability of the regulators' control loop by placing a large capacitive load at the output. An alternative approach to compensation of the loop using the Miller effect has been explored and its properties outlined.

This principle has then been employed to design a reference circuit and a voltage regulator to be used in a prototype of the next generation of a wirelessly powered neural implant allowing multichannel recording of local field potentials. Having manufactured and tested the first version of the circuit, the identified shortcomings have led to the second generation which improved on the identified issues such as the inability to operate when current is injected to the output and the smaller than expected PSRR due to insufficiently simulated substrate resistive coupling.

Despite the improvements in design and simulation methodology the second version of the design still demonstrated smaller than expected PSRR. In spite of multiple additional simulations it has not been possible to find an explanation for this. The behaviour can be explained by

simulating a 10 MΩ coupling between the power supply and the reference output, its origin however remains unknown. The performance of the circuit is fully as expected in all the other aspects, including the PSRR of the current reference. The circuit has been used as a reference in a larger neural recording system designed by other collaborators on the ENGINI project, further demonstrating its functionality. The redesigned push-pull structure of the 2nd version led to alleviation of issues created by current pushed to the output of the reference.

For reference, a comparison with other regulator circuits employed in wireless neural implants found in literature can be seen in Table 5.5. This demonstrates that despite the measured results being worse than the expected simulated results, the designed circuits still favourably compare with those found in literature.

Design	**Description**	**Output**	**Area**	**Power**	**PSRR (DC)**	**PSRR (HF)**
This work (V1)	LDO/Ref	1.2 V	0.187 mm^2	6.7 µW	≈60 dB	≈ 42 dB@1 MHz
This work (V2)	LDO/Ref	1.2 V	0.285 mm^2	7.4 µW	≈53 dB	≈ 33 dB@100 MHz
[202]	LDO	1.0 V	0.0234 mm^2	2.02 µW	53.4 dB	≈16-22 dB@100-200 MHz
[202]	Reference	1.0 V	0.025 mm^2	13.91 µW	64.4 dB	≈16-22 dB@100-200 MHz
[203] (Used in [204])	Reference	1.2 V	0.07 mm^2	1 mW	95 dB	40 dB @ 1 MHz
[76]	Reference	0.5 V	0.031 mm^2	300 nA	40 dB @ 10 kHz	27 dB @ 100 kHz (Worst Case)

Table 5.5: Comparison of Neural Acquisition Reference Circuits in Literature.

A question arises, whether the designed circuit provides sufficient PSRR despite the worse than expected measured results. Observing the performance of other reference circuits employed in similar systems, seen in Table 5.5, it could be argued that this is the case. We should, however, consider the achieved performance in light of the task of acquiring neural signals. As described earlier, a neural spike can be of as small peak-to-peak voltage as 10 µV. Although the peak-to-peak voltage of the carrier used to power the neural implant has to reach a couple of V, this is rectified and filtered resulting in the reference circuit seeing a reduced voltage ripple. A system of [76] using a wireless link operating at a carrier frequency of 1.5 GHz and an active rectifier with a 120 pF output capacitance is reported to have a supply ripple of 31.25 mV at 2 MHz due to modulation.

Assuming the worst measured PSRR of 33 dB, the designed reference circuit would therefore output a ripple of at most 694 µV. This is propagated to the acquired signal both through the power supply and by being used as a reference. A ripple of such magnitude in the power supply should not be of significant concern as it could reasonably be expected for the AFE

to itself have a PSRR of at least 60 dB, thus making the acquisition of sub-10 µV signals feasible. In addition, the ripple is going to be propagated to the acquired signal as it is going to be present in the reference signal directly added to the input of the acquisition chain. We should, however, consider that the ripple, caused by the carrier and modulation frequency, is occupying a significantly higher frequency than the signals of interest. Depending on the used AFE topology, this can thus be rejected from the output.

As seen in the next chapter, in the case of a ΣΔ ADC, out-of-band signals would be rejected either by a decimation filter or the inherent anti-aliasing property of ΣΔ ADCs. A second order ΣΔ ADC designed for an acquisition bandwidth of 10 kHz would require at least a third-order decimation filter having an attenuation of 120 dB at 1 MHz, thus safely rejecting this kind of ripple. As such, we can conclude that the presented design would be sufficient and is still comparable to designs found in literature despite the shortcomings of the measured performance.

Chapter 6

Sigma-Delta Modulator for DC-Coupled Neural Interfaces

6.1 Introduction

As mentioned in previous chapters, one of the notable topologies of analogue front-ends that are recently gaining a lot of interest [141; 142; 126; 32; 80] are based on sigma-delta ($\Sigma\Delta$) modulators [205]. The aim of this chapter is to introduce the operating principle of $\Sigma\Delta$ ADCs, compare it with other topologies in terms of its advantages and disadvantages and finally introduce a practical CMOS implementation that has been created for the use in neural implants and manufactured.

6.1.1 Principle of Operation

A block diagram of a typical continuous time (CT) $\Sigma\Delta$ ADC demonstrating its operation can be seen in Figure 6.1. This is based on a feedback loop that subtracts the last obtained sample from the input to form an error signal representing the quantisation error and change in the signal between taken samples. This is subsequently integrated using an analogue integrator and the output of the integrator is quantised using a conventional clocked ADC.

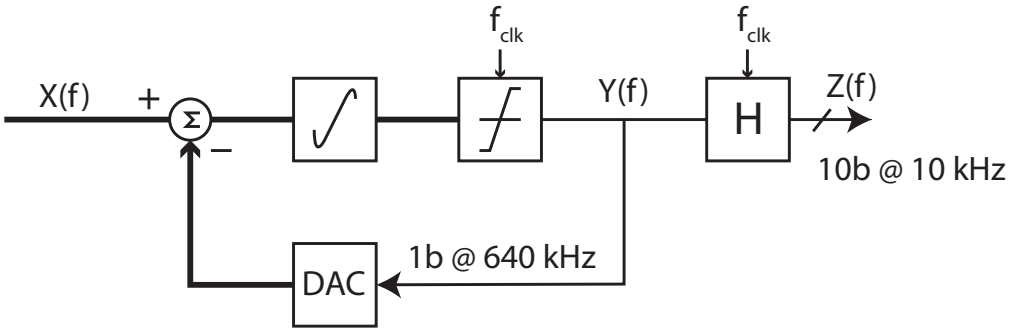

Figure 6.1: Block diagram of a typical sigma-delta modulator illustrating an integrator, a threshold crossing detector, downsampling filter $H_d(f)$ and a DAC. Bold lines indicate analogue signals. Previously published in [118], modified.

This quantised signal forms the output of the system, in addition to being fed back to the input after conversion to an analogue signal using a DAC. As shown in [205], the transfer function $H_s(f)$ between the output Y(f) and input X(f) formed by the feedback loop can be denoted:

$$H_s(f) = \frac{Y(f)}{X(f)} = e^{-j\pi f}\,\mathrm{sinc}(f) \tag{6.1}$$

The quantisation process leads to addition of quantisation noise N(f) that is shaped by the feedback loop and the transfer function $H_n(f)$ from N(f) to Y(f) can be denoted:

$$H_n(f) = \frac{Y(f)}{X(f)} = 1 - e^{-j2\pi f} \tag{6.2}$$

Both $H_s(f)$ and $H_s(f)$ can be seen plotted in Figure 6.2. This shows the nature of $\Sigma\Delta$ operation and demonstrates one of the greatest advantages of the mechanism. It can be seen that $H_s(f)$ exhibits a low-pass behaviour, while $H_n(f)$ is high-pass in nature. This means that if the input signal occupies a bandwidth significantly smaller than the sampling rate, the quantised signal can be in a frequency band that is not affected by quantisation noise.

Since the frequency response of the transfer functions scales with the sampling frequency, it follows that the higher the sampling frequency is, the more quantisation noise is removed from the bandwidth of interest. This places $\Sigma\Delta$ ADCs into a larger group of oversampling ADCs.

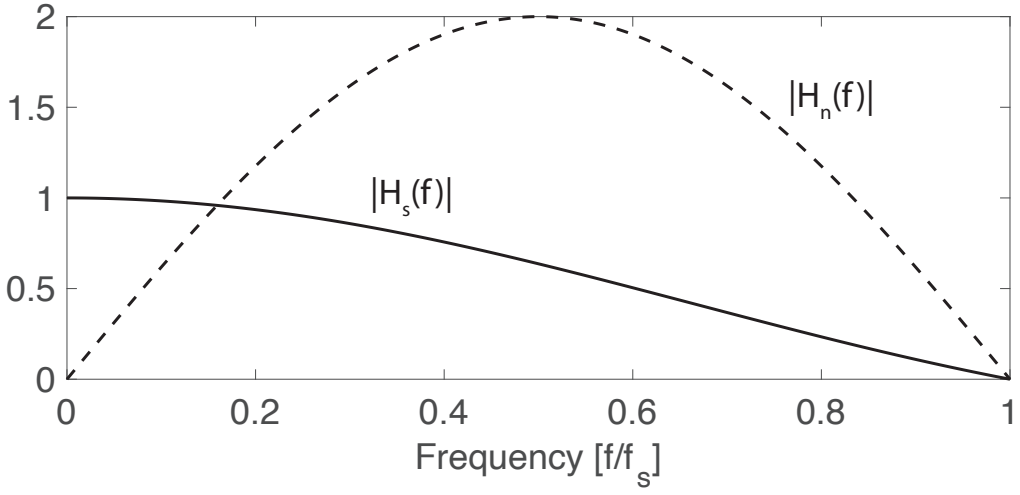

Figure 6.2: Magnitude plots of the signal transfer function $H_s(f)$ (solid) and the noise transfer function $H_n(f)$ (dashed).

As a large part of the output digital signal Y(f)'s badnwidth is formed by signal outside of interest, mostly occupied by quantisation noise, a decimation filter $H_d(f)$ as seen in Figure 6.1 is employed at the output to filter out the unwanted out-of-band portions of the signal and reduce the sampling rate to the Nyquist rate needed to represent the baseband input signal.

As seen in Figure 6.2 the signal transfer function $H_s(f)$ has a zero at the sampling frequency as well as its integer multiples due to the magnitude spectrum being a sinc function as seen in Equation 6.1. This means that spectral contents of the input signal, that would be aliased to the baseband of the signal of interest, are suppressed and the $\Sigma\Delta$ ADC thus has an inherent anti-aliasing property, often allowing its operation without additional anti-aliasing filter at the input.

6.1.2 Design Considerations

Having explored the theoretical properties of a $\Sigma\Delta$ ADC, we can now consider some of the practicalities of its implementation. One of its favourable properties is the fact that it often requires a limited amount of analogue circuitry, as the system is mostly formed of digital components and in a simple design the integrator facilitating a differential input can be the sole analogue component.

The complete structure, however, also requires an ADC and a DAC, components that are at least partly analogue in nature. The quantisation noise shaping property of the converter, though, allows for a trade-off between the resolution of the employed quantiser and the required oversampling ratio (OSR) to achieve a target SNDR. If a quantiser of small resolution is used, the added quantisation noise has a higher power. The amount of in-band noise power can, however, be reduced by increasing the OSR and if taken to the extreme, the quantiser can have a resolution of a single bit if sufficiently compensated by a high-enough OSR.

This approach is often favoured, as the implementation of a single-bit ADC, as well as a single-bit DAC, is practically simple. In addition, their inherent linearity removes the possibility of distortion being introduced in the quantiser as noted in [205]. In terms of practical implementation, a single-bit ADC can be realised by the use of a comparator. As opposed to the previously discussed CT ADCs which required a continuous time comparator, the comparator in this case is clocked and therefore can be designed such that it only consumes power at a rising edge of a clock. A single-bit DAC can similarly be implemented trivially, either by directly using the digital level as an analogue value or by using a potential divider to scale the voltage.

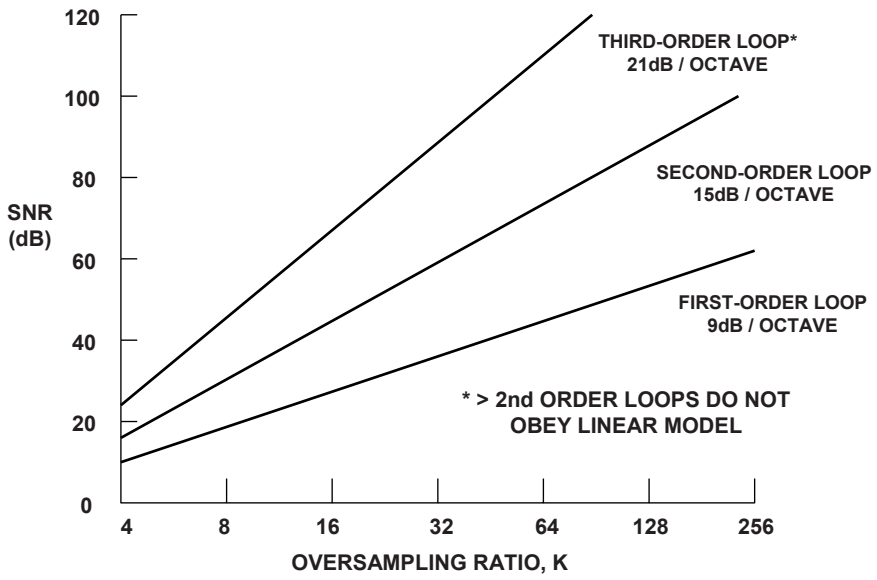

Figure 6.3: Relationship between the oversampling ratio and the SNDR in a $\Sigma\Delta$ ADC of various orders. Figure reproduced from [206].

As noted in [206], and seen in Figure 6.3, the achieved SNDR increases by 9 dB for each doubling

in the OSR starting at ≈ 10 dB for an OSR of 4. The construction of a neural acquisition front-end aimed at recording of both LFP and EAP, however requires a dynamic range in the region of 60 dB to permit it to distinguish components in signals whose amplitude differs by three order of magnitude. If a first-order ΣΔ ADC was to be used to achieve such specifications, the OSR would have to be larger than 128. For a baseband sampling rate of 20 kHz, typical for the acquisition of EAPs, the ΣΔ loop would thus have to operate at a sampling frequency of 2.56 MHz.

While such a frequency is not prohibitively high in terms of its implementability, it could lead to unnecessarily high power consumption of the circuit. Another alternative that would allow the achievement of high SNDR without the need to raise the OSR is to increase the resolution of the internal ADC and DAC. An increase of a single bit in resolution would lead to an increase of SNDR by ≈6 dB. We would however lose the advantage of inherent linearity present in single bit converters in addition to having to face difficulties with a more complicated implementation.

6.1.3 2nd Order Sigma-Delta Modulators

As demonstrated in Figure 6.3, higher SNDR can also be achieved by the employment of higher-order ΣΔ modulator loops. As explained in [205] this effectively amounts to replacing the ADC inside the feedback loop by another ΣΔ modulator and results in a structure seen in Figure 6.4 that contains two integrators in addition to a feed-forward path that ensures stability of the structure. The factor of 1.5 seen in the feed-forward path is derived [205] to ensure that the impulse response of the CT ΣΔ modulator's noise transfer function follows that of a discrete time ΣΔ modulator that forms a basis for the derivation of continuous time modulators.

The system's signal and noise transfer functions $H_{s2}(f)$ and $H_{n2}(f)$ now become [205] the following:

$$H_{s2}(f) = (1 + 1.5(j2\pi f))e^{-j2*pif}\,\mathrm{sinc}^2(f) \tag{6.3}$$

$$H_{n2}(f) = (1 - e^{-j2*pif})^2 \tag{6.4}$$

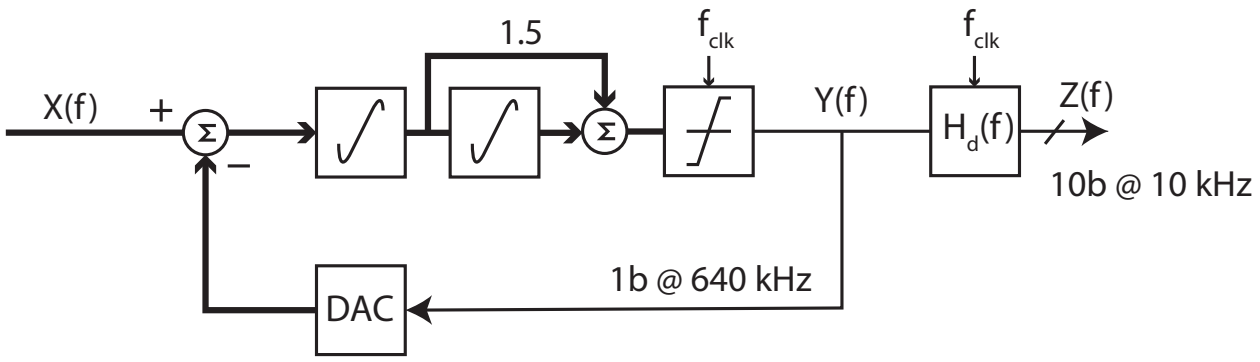

Figure 6.4: Block diagram of a typical 2nd order sigma-delta modulator illustrating 2 integrators, a threshold crossing detector, downsampling filter $H_d(f)$ and a DAC. Bold lines indicate analogue signals.

The magnitude plots of those transfer functions seen in Figure 6.5 demonstrate the steeper slope of $H_{n2}(f)$ resulting in a larger portion of the quantisation noise removed from the baseband of the acquired signal. It can also be seen that, although $H_{s2}(f)$ has a gain of 0 dB at DC, its gain rises to 6 dB at higher frequencies. Since the input signal occupies a small portion of the full bandwidth visible in Figure 6.5, the effect of the gain is minimal.

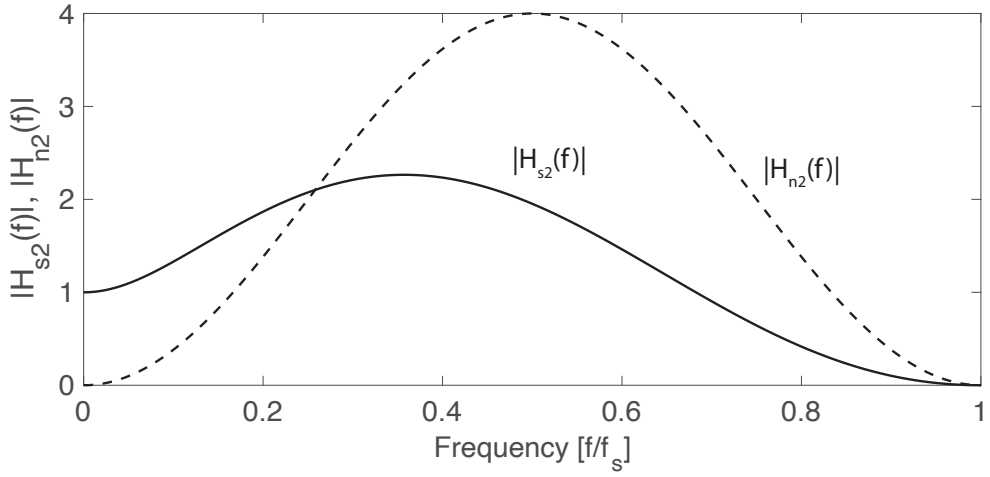

Figure 6.5: Magnitude plots of the signal transfer function $H_{s2}(f)$ (solid) and the noise transfer function $H_{n2}(f)$ (dashed) of a 2-nd order CT $\Sigma\Delta$ modulator.

As seen in Figure 6.3, the use of a 2nd order $\Sigma\Delta$ modulator reduces the required OSR for an SNDR of 60 dB down to ≈ 32, a reduction by a factor of 4. In terms of implementation cost, the addition of the second integrator is not necessarily very expensive with regard to an increase of silicon area or power consumption. This is due to the fact that the first integrator has a high gain at DC and small frequencies resulting in any noise added after the first integrator having

limited effect when referred to the input. The input referred noise is therefore dominated by the first integrator and the second integrator can thus be implemented following a more relaxed noise performance and thus have a smaller power budget as well as occupy a smaller area.

6.1.4 Decimation Filters

So far we have considered the formation of a $\Sigma\Delta$ modulator operating at a high sampling rate without giving much thought to the process of downsampling the output to the baseband frequency. The output of a single-bit $\Sigma\Delta$ modulator, often referred to as bitstream, is typically processed by a digital filter that performs the function of filtering out the shaped quantisation noise outside the frequency band of interest while at the same time reducing the sampling rate by the oversampling ratio to produce a multi-bit output at a baseband sampling rate.

The implementantion of the filter itself can often present challenges and its sharpness affects the achieved SNDR of the ADC, adding to the trade-offs available in the design of a $\Sigma\Delta$ ADC. Due to sharper slopes present in the shaped noise of higher-order modulators, a higher-order filter is required to achieve the suppression of the noise. At the same time, it is possible to compromise on the used decimation filter by employing a higher OSR.

Since it is in general expensive to implement digital multiplication elements, the strategy for implementing the decimation filter often evolves around the use of filters that avoid their need. A popular example of such are Cascaded Integrator-Comb (CIC) filters [207], a class of multi-rate filters that are only composed of comb stages, adding or subtracting a delayed version of the signal itself and integrator stages forming accumulators. Alternative solutions such as [208] aim to improve on the performance of CIC filters by using weight coefficients in parts of the filter that are the most crucial to the overall performance. This would typically apply to the initial stages of the CIC filter, before the first decimation, improving the suppression of noise between $0.25f_s$ and $0.5f_s$, where the magnitude of the noise transfer function is the highest, to prevent it from being aliased to the baseband.

6.1.5 Comparison with Other ADC Topologies

As opposed to more commonly employed methods such as successive approximation register (SAR) ADCs, ΣΔ ADCs present the advantage of permitting the achievement of higher SNDR in the acquired signal. This is allowed by the fact that in an SAR ADC, the ENOB, or SNDR, becomes limited by the possibility of precisely matching elements in a CMOS manufacturing process. Some techniques to overcome this include the use of dynamic element matching (DEC) [209; 210] or digital trimming of elements [211]. Even when those methods are employed, to the best of our knowledge, there has not been an SAR ADC design in the literature that would achieve ENOB higher than 16-17 bits, while a majority of designs does not exceed an ENOB of 12 bits. On the other hand, SAR ADCs have the advantage of achieving superior power consumption to many of the alternative topologies.

Another class of ADCs that we explored, the CT ADCs, or level-crossing ADCs, are also typically implemented with a small design resolution, given in terms of number of output bits. However, as explained in Chapter 3, CT ADCs have the potential to acquire the input signal without any quantisation noise regardless of the bit resolution. Their ENOB limit is, therefore often given by distortion introduced by non-idealities of the circuit implementation. In the designs presented in Chapters 3 and 4, the ENOB is mainly limited by the ability of the circuit to ensure linearity of the input comparator and independence of the magnitude of injected charge from the common mode voltage. Other designs such as [146] rely on an N-bit DAC and therefore face the same limits as SAR ADCs caused by matching of elements. On the other hand, they present the advantage of activity-dependent power consumption that can lead to a very favourable power performance. At the same time, the designs that do not rely on a full N-bit implementation such as those of Chapters 3 and 4 essentially form a continuous-time delta modulator that has the ability to reject any input DC offset without an adverse effect on the dynamic range as long as the input signal remains within the common mode range of operation.

When compared to those topologies, ΣΔ ADCs mainly offer the ability to create designs of superior resolution and SNDR. There are commercially available integrated circuits, such as

MAX11200, that offer ENOB as high as 24 bits [212]. As explained above this is made possible by the trade-offs allowed by the use of oversampling that removes the issues with the linearity of multi-bit DACs and ADCs and transfers a lot of circuit design complexity into the requirement of creating simpler high speed, high bandwidth circuits that benefit from the scaling brought by modern CMOS technologies and feature scaling. This is additionally boosted by the fact that a large part of the implementation, mainly the decimation filter, remains digital. The limit to SNDR is instead often presented by the amount of clock jitter and the limited possibility of creating jitter-free clock signals [213].

While there often is not a need for the very high SNDR that ΣΔ ADCs can deliver in neural implants, it can be advantageous for the implementation of a single ADC to quantise both EAP and LFP without their prior separation. In theory, ΣΔ ADCs can be designed for SNDR sufficient to quantise EAPs, LFPs as well as the electrode offset at the same time. Permitting an electrode offset of 100 mV and considering the smallest distinguishable signal to be 1 µV, we arrive at a dynamic range of 100 dB, the ENOB equivalent of which is 16.32 bits. This approach is, however, not typically adopted due to the required complexity of the circuit and separate techniques are used for the removal of the DC offset.

6.2 Implementation

Having explored some of the basic principles of ΣΔ ADCs and their properties, we are now going to describe a practical implementation of a ΣΔ modulator designed for the use in neural implants. The target of the design is the creation of ΣΔ-based analogue quantiser to be used for the joint acquisition of both LFP and EAP signals while at the same time being able to reject electrode DC offset without the need to employ capacitive coupling.

To facilitate the acquisition of both LFP and EAP, the design has to have a dynamic range of at least 60 dB while being able to quantise signals of on the order of mV peak-to-peak voltage without the need for additional amplification. The baseband sampling rate is 20 kHz, as is typical in EAP acquisition front-ends. To achieve those specifications, a 2nd order ΣΔ mod-

ulator of an OSR factor of 64 is going to be used. As seen in Figure 6.3, this is sufficient to achieve an SNDR higher than 60 dB (ENOB of 9.7 bits) as needed to satisfy the dynamic range requirement.

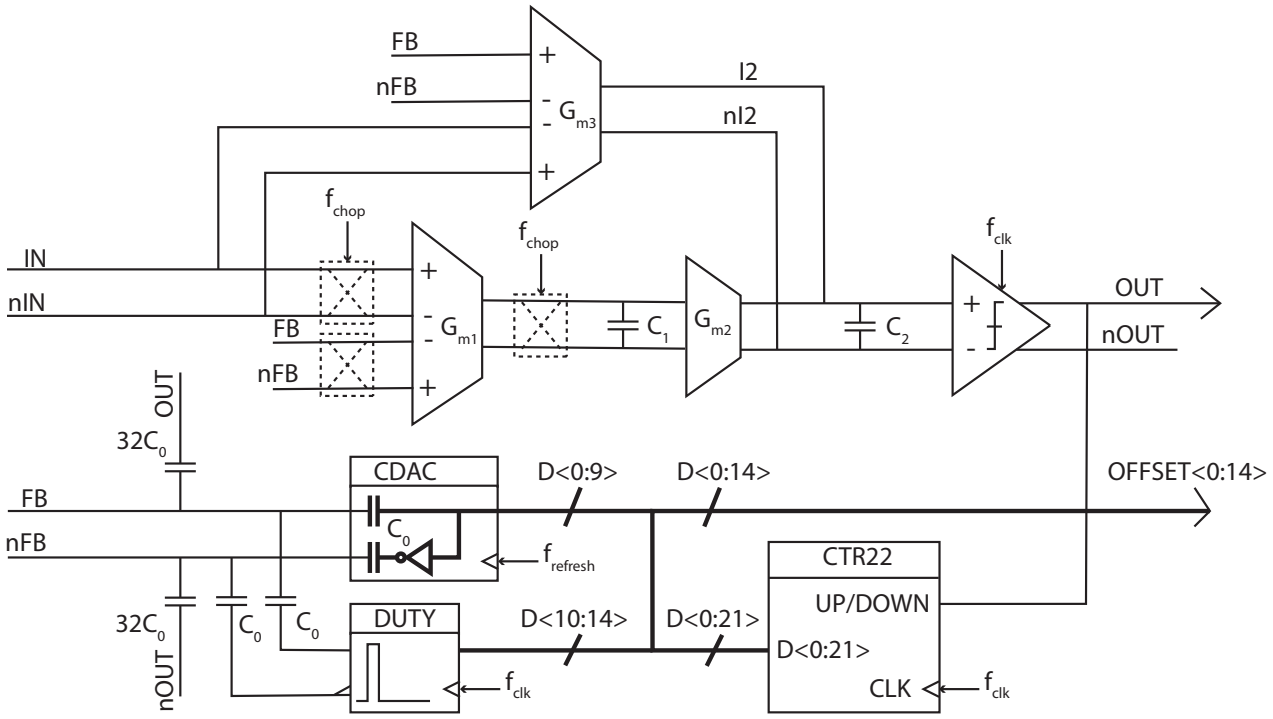

Figure 6.6: Schematic of the implemented ΣΔ modulator. Bold lines indicate digital buses.

A block diagram of the proposed circuit can be seen in Figure 6.6. This comprises a fully differential continuous time ΣΔ modulator clocked at a frequency of 1.28 MHz to implement an ADC of an OSR of 64 and baseband sampling rate of 20 kHz. The rejection of DC offsets is facilitated by the employment of a DC servo loop making this design completely DC-coupled. Since the aim is the quantisation of both EAP as well as LFP signals, chopper stabilisation is employed to suppress the disruption caused by flicker noise at low frequencies.

6.2.1 Feedback Loop

As it is necessary to implement a DC servo loop to reject the electrode offset, let us consider the effect of altering the feedback loop in the modulator. The block diagram of the modulator can be simplified as seen in Figure 6.7 where X(s) is the input signal, Y(s) is the output and N(s) the added quantisation noise. H(s) denotes the transfer function of the integrator, while

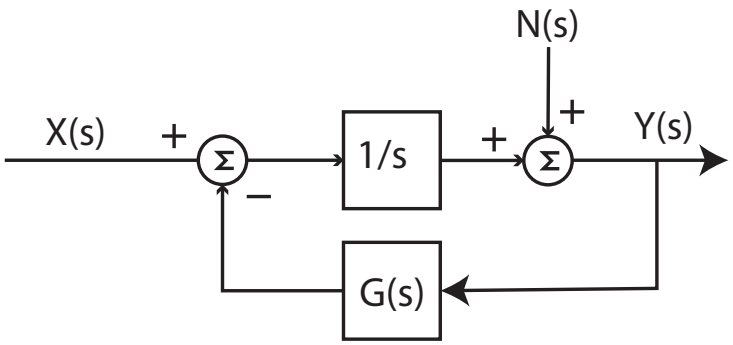

Figure 6.7: Block diagram of signal flow in a ΣΔ modulator.

G(s) is the transfer function of the feedback filter. The transfer function between the input and the output can thus be denoted:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)G(s)} \tag{6.5}$$

Since H(s) is an integrator, or a higher-order system consisting of several integrators, it is expected, and is required for the correct operation of the ADC, to have an infinite gain at DC and a high gain throughout the bandwidth of the input signal. The signal transfer function within the baseband of the signal can thus be approximated as:

$$\frac{Y(s)}{X(s)} \approx \frac{1}{G(s)} \tag{6.6}$$

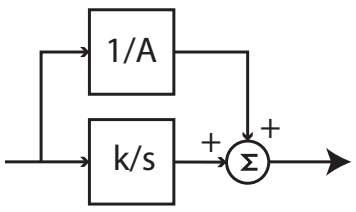

Figure 6.8: Block diagram of signal flow in the feedback signal path.

If we now implement the feedback loop such that G(s) consists of an attenuation alongside an integrator as seen in Figure 6.8, the baseband signal transfer function becomes:

$$\frac{Y(s)}{X(s)} \approx \frac{sA}{s+kA} \tag{6.7}$$

A Bode plot of the resulting transfer function seen in Figure 6.9 demonstrates the implemented low-pass filter with a gain of 0 at DC. The roll-off seen at high frequencies is caused by the modulator's forward signal path filter H(s) and is a result of one of the properties of ΣΔ modulators.

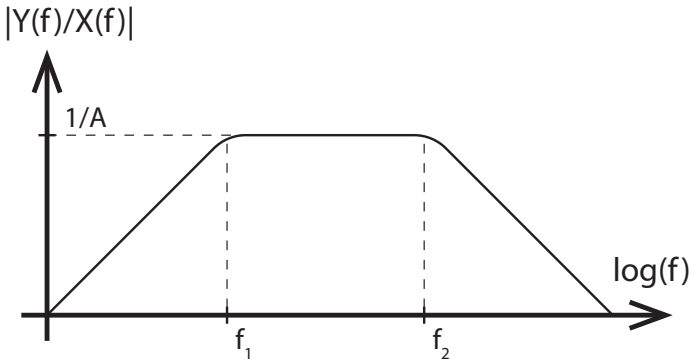

Figure 6.9: Bode plot of the modulator's transfer function.

This shows that the feedback filter configuration allows the implementation of a high-pass filter facilitating the rejection of a DC offset in addition to having the ability of introducing gain to the acquisition chain by introducing an attenuation in the feedback loop.

As seen in Figure 6.6, the feedback loop in the proposed system is implemented using a combination of digital elements and a capacitive charge redistribution network. The integrator is formed of a 22-bit UP/DOWN ripple counter that increments or decrements its count on each clock cycle depending on the value of the current bit in the bitstream. The highermost 10 bits of the count are then converted to an analogue voltage using a capacitive DAC. To increase the resolution of the reconstructed analogue offset, additional 5 bits of the counter's state are converted into a duty cycle and added to the output of the DAC.

In z-domain the transfer function of the formed feedback loop is:

$$\frac{Y(z)}{X(z)} = A + \frac{z^{-1}}{1-z^{-1}} \times k \tag{6.8}$$

where A is the attenuation factor of the direct bitstream path and k the attenuation factor of the counter. The used charge redistribution network can be seen in Figure 6.10. This implements a 10-bit split-capacitor binary-weighted DAC additionally summing the output with signals DUTY and OUT, respectively representing the duty cycle corresponding to additional 5 bits of the integrator's output and the bitstream.

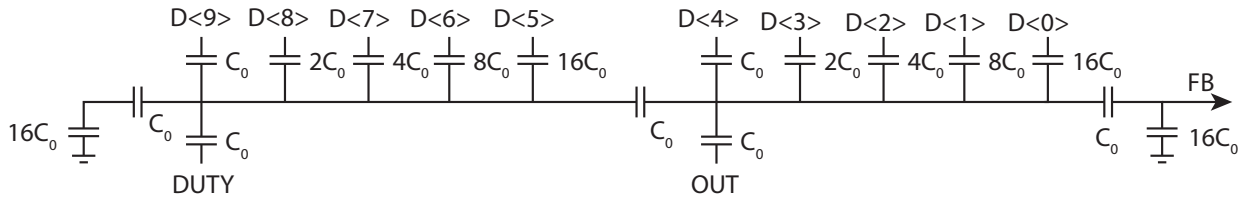

Figure 6.10: Half-circuit of the charge redistribution network used in the implementation of the feedback.

This results in an attenuation factor A' of $\approx 1/578$, thus leading to an overall bandpass gain of ≈ 55 dB. The duty cycle signal has a magnitude $\approx 1/34$ smaller than that of the bitstream and equal to one least significant bit (LSB) of the capacitive DAC's output. In addition, the LSB of the DAC's input is connected to the 12th LSB of the counter's output and thus an additional attenuation factor of 2^{12} is introduced to the output of the integrator. The value of constant k' is thus $\approx 1.24\times10^{-8}$.

Those values are however dependent on the voltage level of the digital power supply VDD that drives the capacitors. To make the derivation of the transfer function simpler, we can refer the output gain to the full baseband input swing of the modulator which can be expressed as $\pm$A'$\times$VDD. In the case of the implemented circuit, using a power supply of 1.2 V leads to a swing of $\approx \pm 2.1$ mV. As explained later, the output of the DAC is, however, only present for three quarters of the sampling cycle due to the need to refresh the charge at the DAC's capacitors, and is held at ground potential otherwise. This means that the effective maximal input swing is reduced by 25% and is thus $\approx \pm 1.6$ mV. In addition, the circuit allows the rejection and quantisation of low frequency electrode offset 32 times larger than the baseband signal. This equals to a maximal offset of $\approx \pm 51$ mV.

Applying the scaling, we now obtain values of A=1 and k$\approx 7.17\times10^{-6}$. Assuming the signal is

filtered by a 2nd order CIC filter, the transfer function of both the signal path and the noise path can be seen plotted in Figure 6.11. This shows a baseband gain of 0 dB and two corner frequencies located at ≈1.5 Hz and 6.5 kHz, a result of the integrator in the feedback path and the CIC filter respectively.

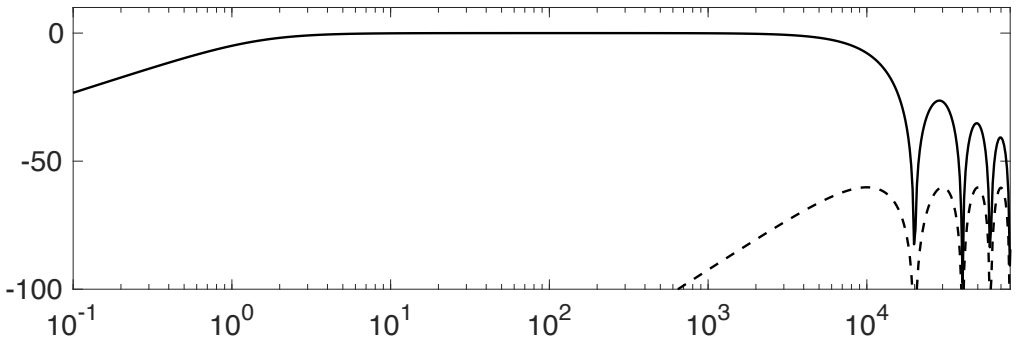

Figure 6.11: Transfer functions of the designed modulator. Solid Line - Signal Transfer Function, Dashed Line - Noise Transfer Function.

6.2.2 Integrator Implementation

As seen in Figure 6.6, the implementation of the 2nd order integrator is different from the theoretical implementation of Figure 6.4 using 2 integrators and a feedforward factor. If we denote the feedforward coefficient $k_1 = 1.5$ and scale the function for a sampling rate f_{clk}, the transfer function $H_1(s)$ of the filter can be expressed as:

$$H_1(s) = \frac{f_{clk}}{s} \times \left(\frac{f_{clk}}{s} + k_1 \right) = \frac{k_1 s + 1}{s^2} \tag{6.9}$$

The transfer function of the filter in Figure 6.6, $H_2(s)$ defined as the transfer function between the difference of differential inputs FB, IN and the output of the filter I2 can be denoted:

$$H_2(s) = \frac{G_{m1}}{s f_{clk} C_1} \times \frac{G_{m2}}{s f_{clk} C_2} + \frac{G_{m3}}{s f_{clk} C_2} = \frac{G_{m1} G_{m2}}{f_{clk}^2 C_1 C_2} \times \frac{s \frac{G_{m3} C_1 f_{clk}}{G_{m1} G_{m2}} + 1}{s^2} \tag{6.10}$$

To make sure that $H_1(s) = H_2(s)$, we thus have to design the circuit such that

$$\frac{G_{m1}}{f_{clk}C_1} = 1, \frac{G_{m2}}{f_{clk}C_2} = 1, \frac{G_{m3}}{G_{m1}} = 1.5 \tag{6.11}$$

This is achieved by combining the transconductors G_{m2} and G_{m3} into a single transconductor seen in the schematic of Figure 6.12. This shows a fully differential folded cascode transcoductor employing multiple inputs. The input devices M_1-M_6 are biased in the weak inversion region and therefore their transconductance g_m follows a linear relationship:

$$g_m = \frac{I_d}{nV_t} \tag{6.12}$$

where I_d is the drain bias current, n the gate coupling coefficient and V_t the thermal voltage. Ensuring the design condition of $G_{m3}/G_{m1} = 1.5$ is met is thus satisfied by making the drain current of the G_{m3} input pair 1.5 times larger than the current of the G_{m2} input pair.

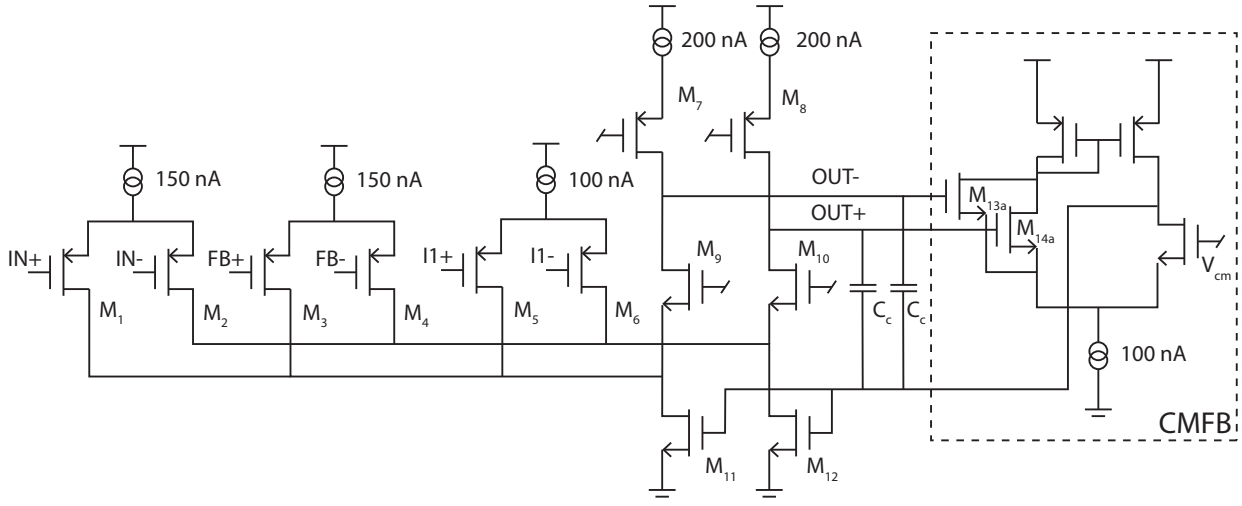

Figure 6.12: Schematic of the combined second stage transconductor G_{m2} and G_{m3}.

Common mode feedback is used to set the common-mode output voltage. This is implemented using an operational transconductance amplifier using two parallel input devices M_{13a} and M_{13b} to calculate the common-mode output voltage from the differential output. The common-mode feedback loop is compensated by capacitors C_c to ensure its stability.

The first stage transconductor implementation follows a similar structure and can be seen in

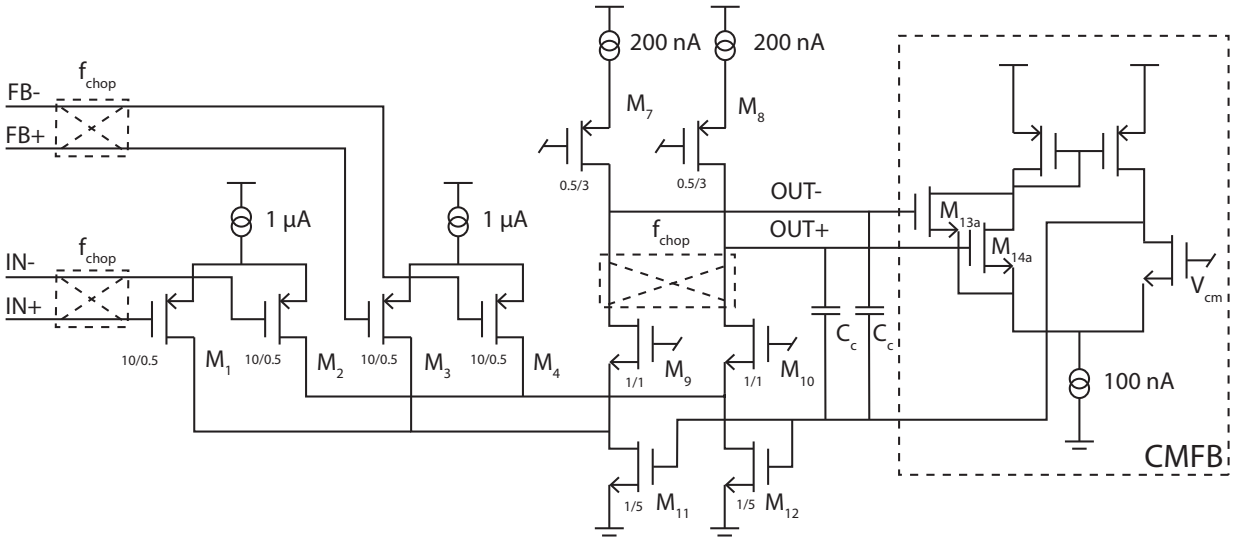

Figure 6.13: Schematic of the first stage transconductor G_{m1}.

Figure 6.13. This is implemented as a folded cascode transconductor with multiple input pairs to implement the differential difference input needed for the implementation of the filter. The circuit additionally integrates a chopper modulator at the inputs to aid with the suppression of low-frequency flicker noise.

The first stage transconductor is critical in terms of the noise performance of the modulator. This is caused by the fact that it is the main contributor of the input referred noise due to the contribution of latter stages being attenuated by the gain of prior stages. Since each stage of the modulator is an integrator, its gain $A_{gmC}(f)$ varies with frequency as:

$$|A_{gmC}(f)| = \frac{g_m}{2\pi f C} = \frac{f_{clk}}{2\pi f} \tag{6.13}$$

As the ratio of g_m/C is a function of the clock frequency, the in-band gain becomes a function of the oversampling ratio. In the case of the presented design, the OSR is 64 and hence the gain of the first stage at the edge of the highest frequency of the baseband is ≈ 20 or ≈ 26 dB. The noise of the second stage when referred to the input of the modulator is thus going to be supressed by at least 26 dB.

To optimise the noise performance of the transconductor used in both the stages, we first

consider the output current noise $\bar{i_n^2}$. The shot noise contribution of each device is given by $\bar{i_{n0}^2} = 4kT(2/3)g_m$ and is thus proportional to its transconductance. When referred to either of the inputs, the contribution of each device can be denoted:

$$\bar{v_{nix}^2} = \frac{8kTg_{mx}}{3g_{my}^2} \tag{6.14}$$

where g_{mx} denotes the transconductance of the noise contributor and g_{my} the transconductance of either of the transistors in each respective input pair the noise is to be referred to. This suggests that it is advantageous to maximise the transconductance of the input pair. Those are, however, constrained by the requirements of Equation 6.11 meaning that an increase in the g_m of the input transistors has to be compensated by an increase of the integrator capacitor area leading to an increase of the overall design area as well as power consumption. The first and second stage transconductors are sized such that the bias current of the first stage, and subsequently the load capacitor, is 10 times larger than those used by the second stage. This follows the fact that the gain of the first stage, and hence the scaling of noise, is approximately twice that of the scale between the bias currents.

The most significant contributors to the noise power are, however, transistors M_{11} and M_{12} seen in Figure 6.12. This is caused by the fact that those devices conduct the sum of current from all the input and output branches of the folded cascode, leading to an increase of their g_m, in turn increasing the input referred noise as described by Equation 6.14. As a result, the input pairs M_1 - M_6 are biased in the weak inversion region to maximise the g_m/I_d efficiency. Contrary to this, devices M_{11} and M_{12} are biased in the strong inversion saturation region so that the g_m/I_d efficiency is minimised and the noise efficiency maximised. The circuit has been designed to achieve a target input-referred noise of 40 nV/√Hz giving rise to a 4 µV rms noise integrated from 0 Hz to 10 kHz, in line with similar designs found in the literature [32] and below the level of noise that can be expected from the electrode-electrolyte interface as seen in Chapter 2.

As mentioned earlier, the first stage additionally uses chopper stabilisation to suppress flicker

noise in the baseband. However, the application of chopper stabilisation in ΣΔ modulators is surprisingly a more complicated problem than might initially appear. The problematic is studied in depth in [214] and [215] exploring the factors that contribute to the deterioration of SNDR introduced by chopping. Those are mainly caused by extra injected charge from the switching circuit leading to demodulation of some of the quantisation noise. It is suggested that those effects can be reduced by using a chopping frequency of $f_{clk}/2$ as its even multiples lie at frequencies where the noise transfer function of the ΣΔ modulator has a spectral zero as seen in Figure 6.4. As explained in [214], mismatch in the differential circuits can, however, lead to demodulation of signals at odd multiples of $f_{clk}/2$ which is problematic. It is suggested by the author that this can be reduced by employing a notch filter in the feedback loop suppressing the quantisation noise at those frequencies. Interestingly, work presented in [216] suggests the use of pseudorandom chopping, similar to the method presented in Chapter 4, that has been demonstrated to lead to SNDR improvements due to reduction of correlation between the chopping signal and the modulator's clock.

The chopper has been applied to modulate both the differential input signals by switching their polarity, in addition to switching the output of the transconductor at the output of the bottom half of the cascode as seen in Figure 6.13. This configuration does not facilitate the removal of flicker noise from devices M_7, M_8 and those employed in the current source. While the contribution of M_7 and M_8 is attenuated by the gain of the cascode and therefore not very significant, this does not apply to the contribution of the current source. This can remediated by the addition of an additional chopper at the output of the top half of the cascode. This has, however, not been applied as it would lead to addition of extra injected charge in addition to having a limited effect due to the flicker noise being dominated by contributions of devices M_{11} and M_{12} caused by their large transconductance. Additionally, since the current source is based on PMOS devices, the contribution of flicker noise power is expected to be approximately an order of magnitude smaller than that of the NMOS devices.

6.2.3 Comparator Implementation

The output of the integrator filter has to be fed to a quantiser which in the case of our implementation is in the form a single-bit comparator. The simplification in the case of a $\Sigma\Delta$ modulator, as opposed to continuous time ADCs presented in Chapters 3 and 4 is the fact that the circuit is clocked. It is therefore possible to employ a clocked comparator that only consumes power on a change of the clock signal and otherwise leads to no static power consumption.

A circuit satisfying such a requirement, based on a StrongARM latch [217], that has been employed in the design, can be seen in Figure 6.15. During the low phase of the clock the output is precharged through transistors M_7 and M_{10}. On a rising edge of the clock, one of the arms of the circuit settles to a low output depending on the difference of gate voltage applied at M_1 and M_2.

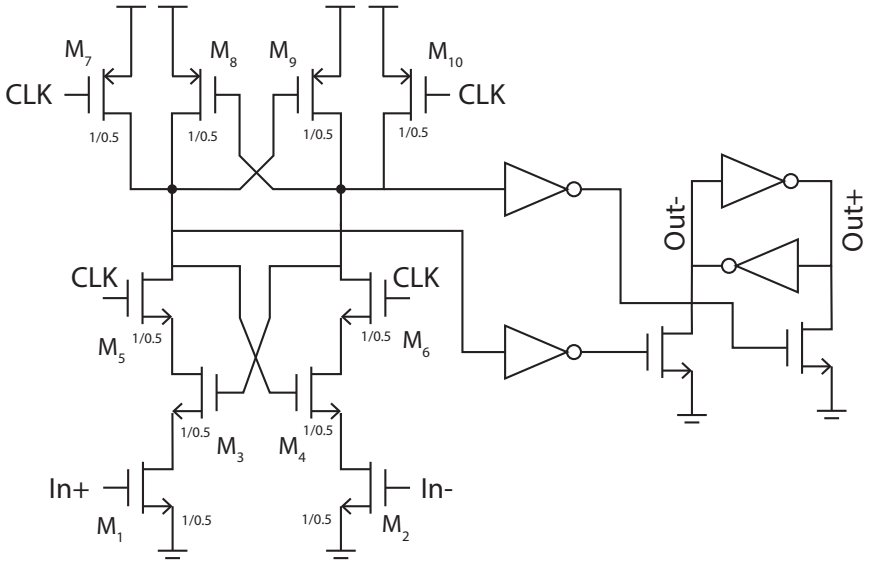

Figure 6.14: Schematic of the used StrongARM comparator.

Since the output is only available during the high phase of the clock, an additional latch formed of CMOS invertors is added at the output of the circuit alleviating the problem. Additionally, this acts as a buffer driving the capacitive DAC and other circuits relying on the bitstream.

6.2.4 Timing Diagram

A concern that arises with the use of a chopper is the introduction of real resistance caused by the switching of the parasitic capacitances at the output of the chopper. This is problematic especially in the case of chopping the output of a capacitive DAC such as the one used in the feedback of this design. If the potential at the capacitors is not refreshed regularly, each change of the chopper will result in a small reduction of the differential potential, eventually reducing the differential voltage to a zero. To completely suppress this effect, it is necessary to refresh the output of the DAC during each change of the chopper.

The timing diagram seen in Figure 6.15 shows the operation of the state machine synchronising the sampling with the chopper and the refresh of the DAC. The system is controlled by a master clock (MCLK) of twice the sampling frequency. This is then divided by 2 and 4 to generate the sampling clock (SDMCLK) and chopper clock (CHOPCLK) respectively. The DAC refresh signal (DACRESET) is asserted on every odd (first, third, fifth, ...) rising edge of the master clock and is deasserted immediately on the next falling edge, thus meaning that the output is available for three quarters of the modulator's clock period.

This results in DACRESET being asserted on every change of the chopper. As seen in the timing diagram, both plates of every capacitor in the DAC are tied to the ground during the refresh and therefore the output of the feedback loop remains zero. Since the chopper changes its state during the refresh state of the DAC, there is no adverse effect on the signal and, additionally, any extra charge injected by the chopper is absorbed.

While providing advantages in terms of reduced distortion, this approach has the disadvantage of increasing the overall power consumption. This is particularly the case given the large amount of capacitors employed in the DAC. The unit capacitance of each element is 130 fF and each half of the differential capacitor bank contains 66 capacitors and the entire bank 132 capacitors. Given the differential nature of the system, a half of the capacitors is always going to be charged. Since this design uses the power supply as the reference voltage, the resulting power consumption is thus:

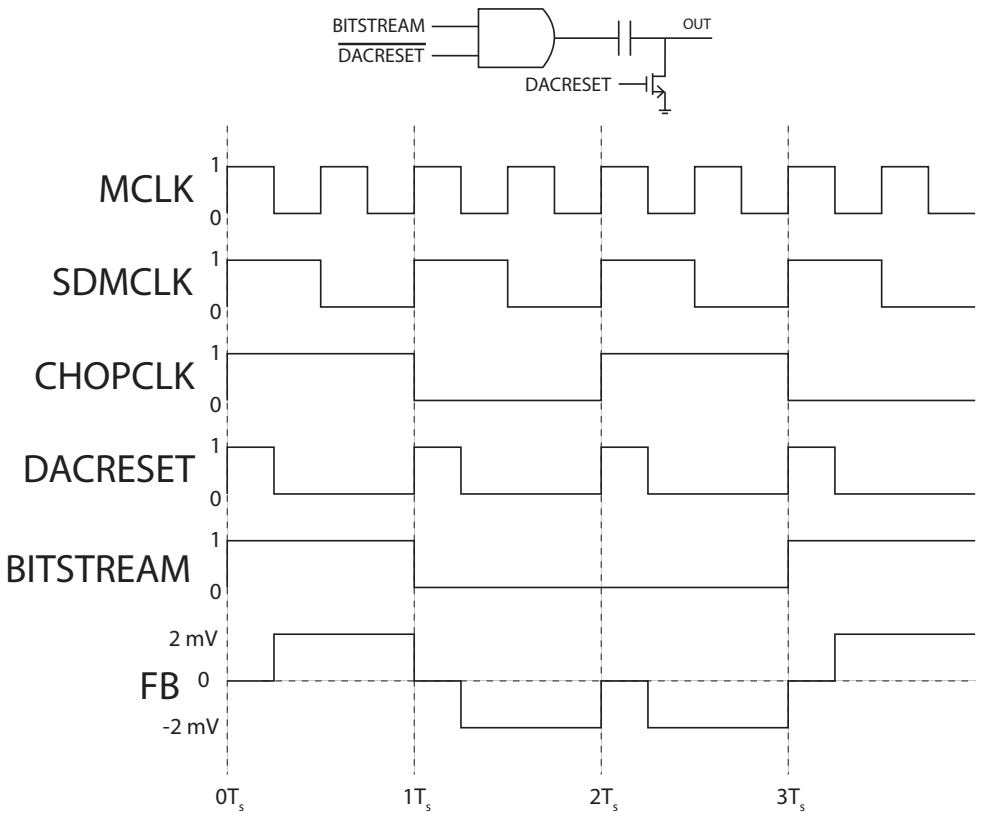

Figure 6.15: Timing diagram showing some internal signals. MCLK - Master clock (2560 kHz), SDMCLK - $\Sigma\Delta$ modulator sampling clock (1280 kHz), CHOPCLK - Chopper clock (640 kHz), DACRESET - Capacitive DAC reset signal, BITSTREAM - Output of the comparator latch, FB - Output of the Capacitive DAC.

$$P_{DAC} = \frac{1}{2} N_C C_0 V_{dd}^2 f_{ref} = \frac{1}{2} \times 66 \times 130 \times 10^{-15} \times 1.2^2 \times 320 \times 10^3 \approx 1.98\ \mu W \qquad (6.15)$$

This can potentially be reduced by reducing the refresh rate of the capacitive DAC while ensuring that the chopper does not lead to a too large deterioration of the SNDR. To this end that it would have to be ensured that the error introduced by the operation of the chopper is below the noise floor of the ADC. This is, however, not necessarily a practical solution as there is an obvious limit to the reduction of the parasitic capacitance while an increase of the capacitive DAC's output capacitance leads to an increase in the needed power consumption due to refresh.

Alternatively, a voltage buffer could be employed to alleviate the problem altogether. Its introduction would however equally lead to an increase in power consumption in addition to

creating another source of flicker noise, thus itself requiring chopper stabilisation and defeating the purpose.

6.3 Results

The described design has been manufactured in a commercially available TSMC 180 nm CMOS technology. The layout exported from Cadence Virtuoso can be seen in Figure 6.16 demonstrating the core occupying an area of 306 µm×145 µm. It can be seen that the majority of the layout is occupied by the digital circuitry, especially the digital counter used for the implementation of an integrator rejecting the DC offset and the control circuitry of the capacitive DAC, including all digital logic and analogue switches. The DAC is formed of metal-insulator-metal (MIM) capacitors placed between Metal 3 and Metal 4 layers of the integrated circuit allowing its positionining above active circuits as seen in Figure 6.16.

The circuit was simulated in Cadence Virtuoso using foundry-supplied device models. The power consumption of the circuit was found to be 16.8 µW which includes a static consumption of 4.8 µW.

The performance of the circuit was evaluated by applying a fully differential 2 mV peak-to-peak sinewave, at the input for a period of 60 ms, 180 periods of the test signal performing a transient simulation using foundry-supplied device models including transient noise simulation of 1 Hz - 1 MHz bandwidth. The swing of the test signal is thus 62.5% of the maximal input swing of the ADC. The output bitstream was then recorded and analysed using Matlab to obtain an estimate of the output PSD seen in Figure 6.17.

This shows a flat noise frequency profile, demonstrating the effectiveness of flicker noise removal due to the implemented chopper and a dynamic range (SFDR) of ≈ 56 dB. The input-referred integrated noise over the full bandwidth, 0 Hz - 10 kHz was found to be of ≈ 7.74 µV rms, thus not significantly exceeding the design target of the first stage of the input integrator of 4 µV.

The output SNDR was found to be ≈ 39.8 dB, thus giving rise to ENOB of ≈ 6.3 bits, while

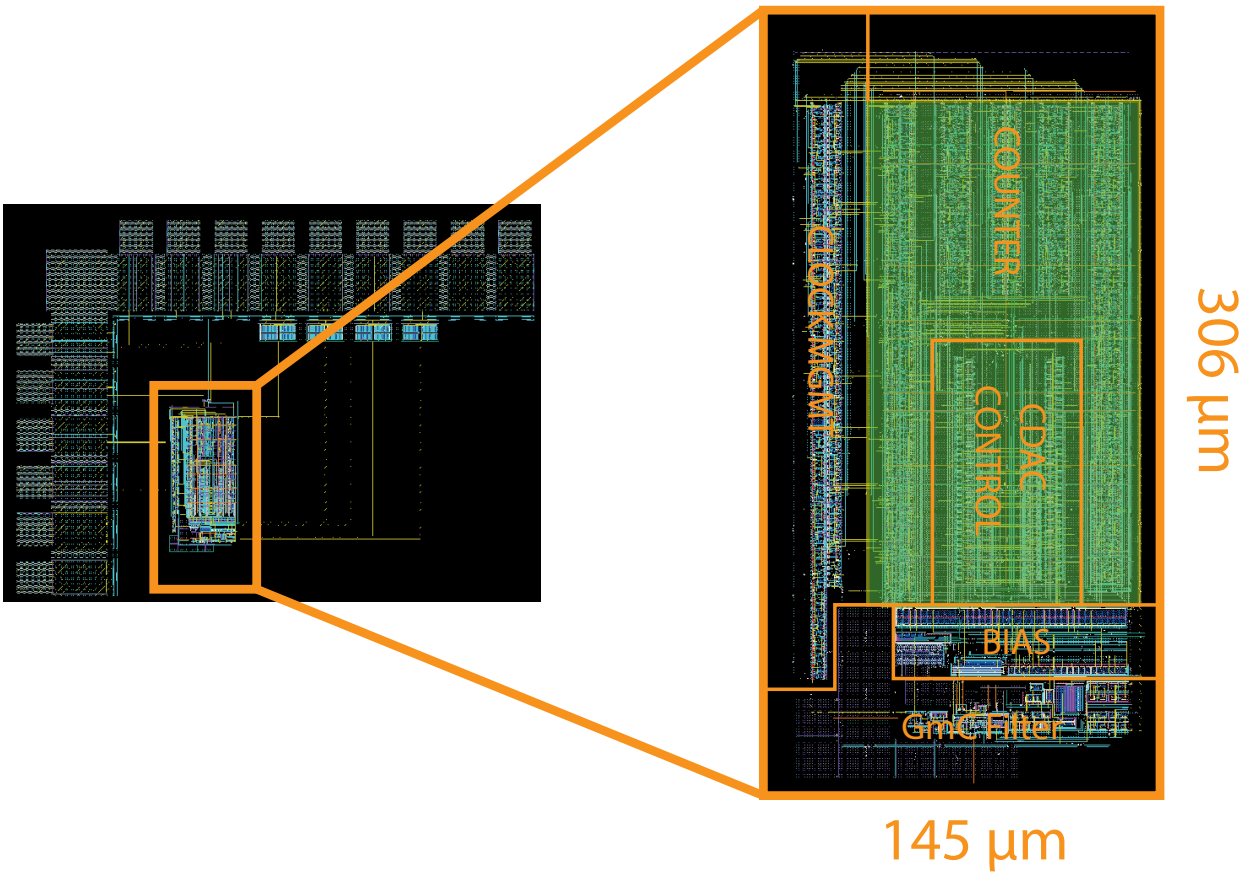

Figure 6.16: Layout of The Designed Circuit exported from Cadence Virtuoso. Light green area shows the position of the DAC capacitive array placed on top of active circuits.

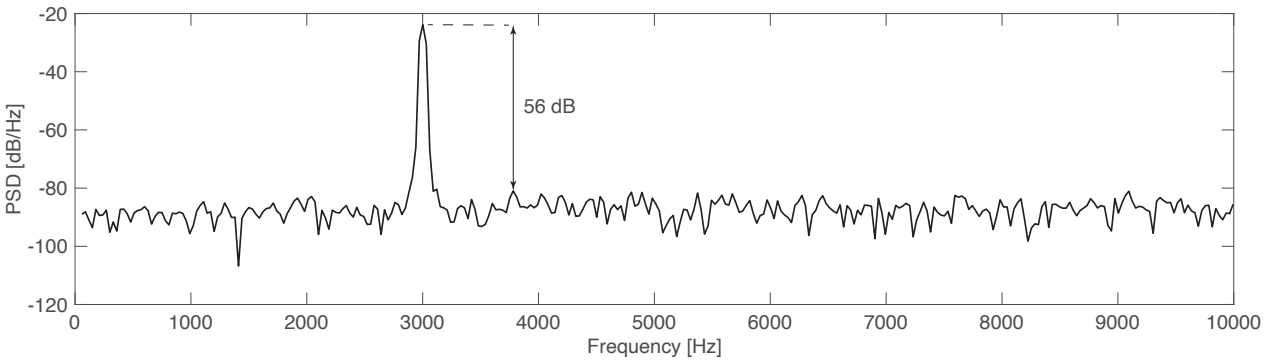

Figure 6.17: Simulated output PSD having applied a 2 mV peak-to-peak fully differential 3 kHz tone at the input.

the observed SFDR gives rise to a linearity of ≈ 9 bits. It was additionally verified that the performance is not affected by addition of an offset and the circuit is able achieve its rejection due to the employed feedback loop.

6.3.1 Measurements

The manufactured integrated circuit has been wirebonded to a DIP48 package and a PCB seen in Figure 6.18 designed and manufactured. This allows for the connection of input stimuli as well as the connection of the power supply and outputs. A diagram of the measurement setup used can be seen in Figure 6.20. A Stanford Research Systems (SRS) DS360 Low Distortion Signal Generator has been used to generate the fully differential input signal. To verify the ability of the system to reject DC offsets and since the DS360 does not support the generation of a DC voltage in a fully differential output mode, a Keithley 2000 Precision Voltage Source has additionally been used to inject a DC voltage to the negative output of the signal generator. The output bitstream has been sampled using a Salae Logic 8 Logic Analyzer at a sampling rate of 500 MSPS and recorded to a computer for future analysis and processing. A Tektronix AFG3102 Arbitrary Signal Generator has been used to generate a system clock signal of 2.56 MHz. The DUT has been powered using an Agilent N6705B DC Power Analyser with an N6761A precision DC Power Module permitting accurate measurement of the power consumption.

A core power supply of 1.2 V and an I/O power supply of 1.8 V have been applied to the DUT. With no system clock present, this resulted in a static current consumption of 3.66 µA which rose to 26.12 µA once system clock of 2.56 MHz has been applied to the DUT.

To characterise the system, a pure tone of 2 mV peak-to-peak and a frequency of 2640 Hz has been applied to the input. Initially, the observed output bitstream indicated that the $\Sigma\Delta$ modulator is saturated. This should not be the case regardless of the applied DC offset given the employed DC rejection mechanism, thus pointing to an issue with the employed servo loop. This has been explained by a possible timing issue with some of the employed digital latches, preventing the system from updating the DC offset. It has, however, been possible to characterise the modulator by modifying the applied input offset until the modulator was no longer saturated. The value of the offset stored in the register is random upon each startup of the circuit which allowed for validation of the employed CDAC offset rejection scheme. By continually restarting the circuit, it has been possible to verify its ability to reject a DC bias of $\approx \pm 45$ mV.

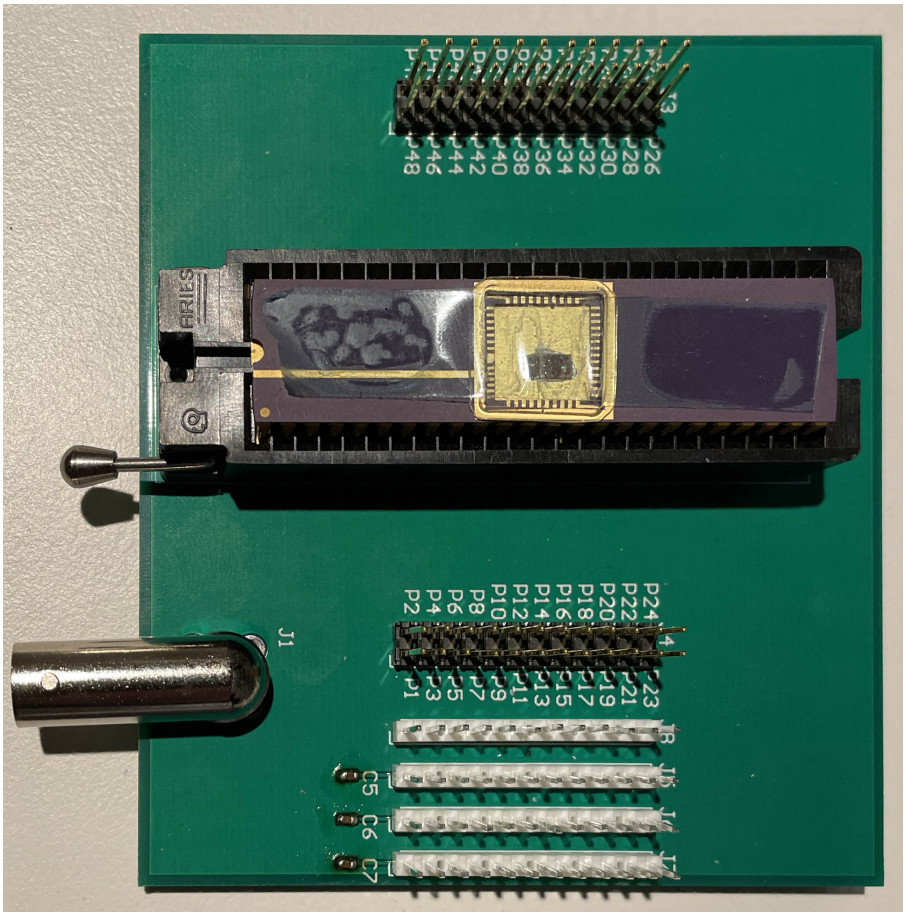

Figure 6.18: Photograph of a PCB with the manufactured integrated circuit used to obtain measured results.

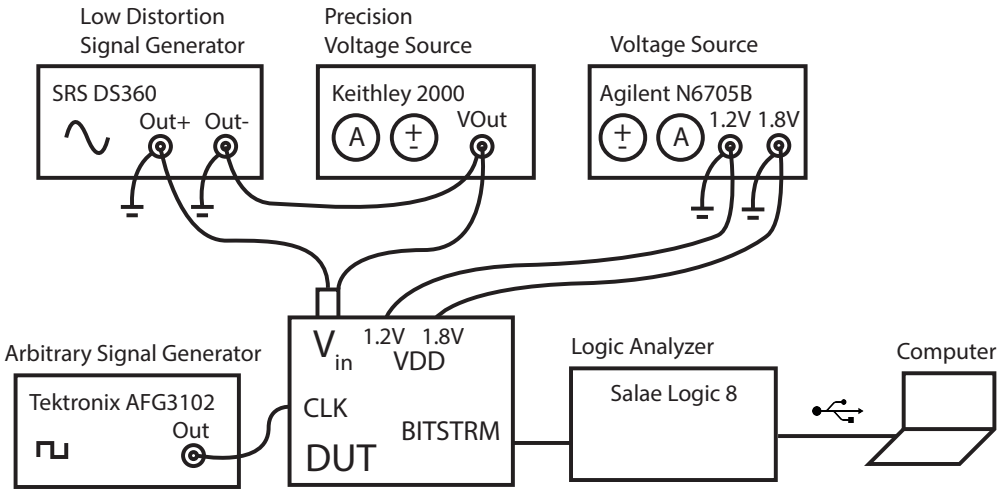

Figure 6.19: Test setup used to characterise the manufactured ΣΔ modulator.

The acquired bitstream has been processed in Matlab and the resulting spectrum plotted in Figure 6.20. This shows an SFDR of ≈51 dB at high frequencies. The encountered digital latch design issue has furthermore resulted in inoperability of the chopping mechanism which led to

the presence of flicker noise visible in the output spectrum.

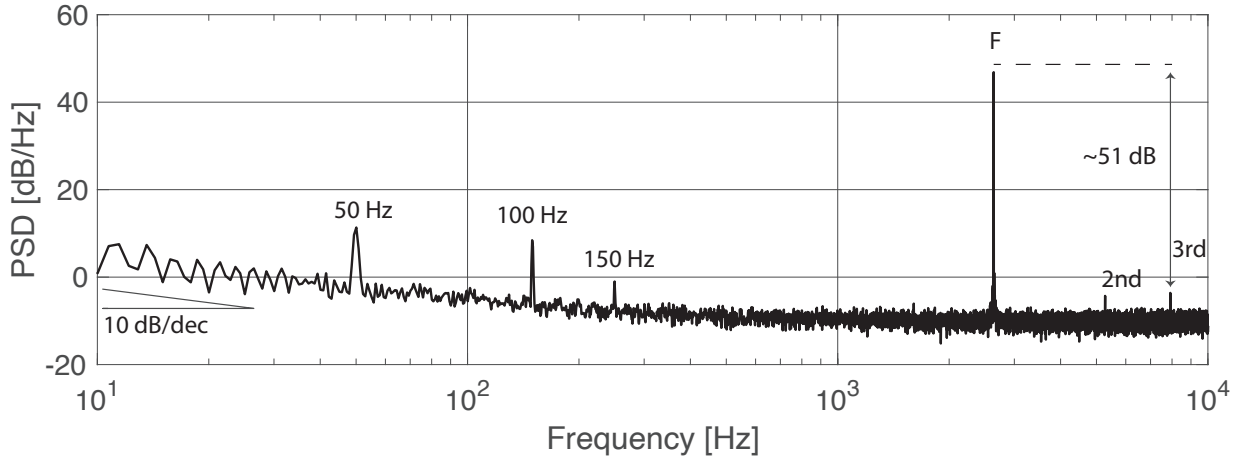

Figure 6.20: Measured output spectrum of the designed ΣΔ Modulator during acquisition of a pure tone of 2640 Hz. F - Fundamental frequency, 2nd, 3rd - Harmonics.

6.4 Conclusion

The performance of the circuit was compared to other digitising neural recording front-end designs found in literature as seen in Table 6.1. The table contains designs that are capable of directly interfacing neural recording electrodes without the need for a pre-amplifier and are capable of rejecting electrode offsets either using AC coupling or alternative methods, such as DC servo loops. The performance of the circuit is comparable with other designs found in the literature, although some of the achieved metrics are comparably slightly worse. The design can, however, be favourably compared in terms of the area occupied by the core. The only design of smaller core than the one presented is found in [32], making use of smaller feature sizes.

An advantage of the presented design over alternatives is the unique way the DC offset of the electrodes is isolated and rejected. Since it is quantised using an up/down counter, its value is stored in a register that can be read out and the value transmitted out of the implant. This is a unique feature amongst neural recording front-ends found in literature allowing the study of electrochemical changes on the surface of the electrodes, possibly paving a way to assessing

[units]	[32]	[126]	[218]	[219]	This work
Power/ch (µW)	5.04	11.5	19.3	67.7	31.3
Bandwidth (kHz)	10	0.825	10.74	10	10
IR Noise (µW rms)	4.9	1.8	2.9	2.2	7.7*
Supply Voltage (V)	0.5	1.5	1.8	1.2	1.2
Technology (nm)	65	350	350	130	180
Area/ch (mm^2)	0.013	0.26	0.29	0.26	0.044
NEF	5.99	13.69	8.8	12.96	22.59*
SNDR	45	63	50.05	60.3	40
SFDR	58	66	66	-	51
Modality	LFP + EAP	LFP	LFP + EAP	LFP or EAP	LFP + EAP

Table 6.1: Comparison of the designed digitising analogue front-end with some designs found in the literature. *Based on simulation results.

the condition of the electrodes.

The largest factor contributing to the lower than expected measured SNDR figure is the failure of the chopping circuit to operate correctly, resulting in the output signal being hindered by flicker noise. This can easily be rectified by redesigning the digital blocks in the circuit and ensuring their correct operation under process manufacturing variations. It is possible to further reduce the amount of thermal noise generated in the circuit by increasing the bias current of the employed transconductor cell. This will, however, come at a cost of slightly increased area due to the need to maintain the operating regions of some devices as detailed in subsection 6.2.2. Similarly, it would be worth further increasing the size of some devices, such as the input pairs, to ensure they are operating deeper in the sub-threshold region. Such a change would result in a possible improvement of the NEF.

Additional aspect of the circuit that remains to be improved on is the rise in the power consumption caused by the frequent resetting of the capacitive DAC, dominating the power consumption. It should be possible to reduce this by employing circuit techniques allowing the DAC to operate without a reset on every clock cycle. Another approach would lie in reducing the unit capacitance of each element in the DAC where the detrimental effects of such could be mitigated e.g. by employing the technique of dynamic element matching (DEM) [220]. This approach would, moreover, make the design more reliant on digital circuits which would allow it to benefit more from the scaling afforded by more advanced CMOS technologies.

Chapter 7

Conclusion

Throughout this thesis, we have explored several aspects of circuit design aimed for deployment in neural implants investigating the constraints presented by the unique environment such as the limited amount of space, available power and the need to operate with signals of small amplitudes composed of components of significantly different magnitudes. While those challenges have always been tackled by designers of neural acquisition circuits, the drive to build even smaller and more efficient circuits has lately been accentuated by the drive to develop a new generation of implants that are minimal in size and wirelessly powered.

To this end, we began by exploring the electrical properties of electrodes and the sources of noise to help us better understand the requirements placed at the design of analogue front ends. This led to the identification of niobium as a novel material for the manufacturing of neural electrodes due to its favourable properties when compared to the more often used platinum. This includes the higher stiffness of the material, lower cost and, more crucially, the possibility to achieve lower recording noise in lower frequency bands occupied by neural signals.

Continuous Time sampling was then explored as a novel sampling scheme, alternative to the more commonly used discrete time sampling, permitting the development of ADCs with activity-dependent power consumption suitable for the quantisation of many classes of biological signals due to their sparse nature exhibited by long quiet periods interrupted by short bursts of activity. The sampling scheme has been explored theoretically to show some of its

properties and its suitability for the acquisition of neural signals and a practical implementation of a novel charge-based ADC topology has been implemented. Measured results have demonstrated the suitability of the sampling scheme and the implementation for the reduction of power consumption in neural acquisition systems in addition to demonstrating its inherent capability of suppressing DC electrode offsets and thus permitting the creation of a DC-coupled front-ends without the need for additional consideration for the removal of offsets.

The work was then expanded by considering the possibility of facilitating flicker noise removal without the need to introduce a fixed frequency clock and thus a source of static power consumption. This has led to the development of stochastic chopping based on reusing the randomised version of the input signal for its modulation and spreading of its spectrum such that a smaller portion of its bandwidth is affected by flicker noise added by the analogue circuits. The theory of its operation has been derived and a circuit implementation presented. While it was not possible to conclusively demonstrate the effectivity of flicker noise removal in a transistor-based implementation, the validity of the proposed method has been verified and proven by numerical models and simulations. In addition, to the best of our knowledge, the presented CT ADC implementation is the smallest implementation found in literature while at the same time offering competitive power consumption.

Since wirelessly powered implants often recover their power supply from physical phenomena resulting in periodic variations of some physical quantity, most typically oscillating electromagnetic fields or mechanical vibrations, the recovered voltage is unknown and variable at a high frequency, leading to the need for the creation of supply-independent voltage references and regulators able to operate under in the constrained space of neural implants. This precludes the possibility of the use of large capacitors that are conventionally employed to stabilise the control loops of voltage regulators and achieve high power supply rejection. Alternative methods, evolving around the use of Miller compensation to ensure the stability of the control loop, have therefore been investigated and a practical implementation of a combined voltage reference and low-dropout regulator developed and manufactured as a part of a complete neural acquisition system. The performance of the circuit was measured and although it was found to be functional, the results were worse than expected, which led to the development of a 2nd

version of the circuit improving on some of the identified shortcomings.

Finally, the use of $\Sigma\Delta$ modulation was investigated for the suitability of its use in neural recording front ends arguing that the possibility of creating designs of high dynamic range and linearity makes the approach particularly suitable for the direct quantisation of neural signals. A practical implementation of a neural implant analogue front end making use of the technique has been presented, making use of a feedback loop allowing the rejection and quantisation of a DC offset, thus allowing the creation of a DC-coupled recording front-end alleviating the need to use large input coupling capacitors and pseudoresistor-based biasing. The presented implementation is unique in its ability to digitise the DC offset and allow its readout in addition to demonstrating one of the smallest core sizes of designs found in literature while achieving comparable performance.

7.1 Original Contributions

Original contributions that have been made as a part of the presented work in each of the chapters can be summarised as:

Chapter 2: Overview of Analogue Front-Ends and Electrodes for Neural Implants

- The use of niobium as a suitable material for the manufacturing of neural recording electrodes has to the best of our knowledge not been previously suggested in literature. We have shown that the material is suitable due to its physical properties and biocompatibility. The hypothesis that the use of a niobium electrode results in a lower noise floor than using a platinum electrode has been indirectly confirmed, although a more direct study remains to be carried out to fully prove this.

Chapter 3: Continuous Time Acquisition of Neural Signals

- It has been shown that continuous time sampling can result in the reduction of the amount of samples taken during the acquisition of EAP signals by a factor of $\approx$20.

- A common claim found in literature saying that the use of CT sampling precludes the appearance of aliasing has been disproved and a condition for alias-free acquisition has been formulated.

- A novel charge-based CT ADC topology that was designed as a part of previous work was tested, demonstrating the feasibility of the method and reduction in the amount of generated samples during the acquisition of EAP signals.

Chapter 4: Clockless Chopping Scheme for CT Acquisition of Neural Signals

- A novel method of activity-dependent flicker noise removal based on the randomised version of the input signal has been presented, removing the need for a fixed frequency clock in chopper stabilised systems.

- The validity of the method has been verified by a numerical model, demonstrating a reduction of noise PSD at small frequencies.

- Building on the CT ADC presented in Chapter 3, an improved version of the circuit was presented, implementing the novel chopping scheme alongside other improvements resulting in the creation of a compact-area sub-µW CT ADC.

Chapter 5: Reference Circuits and Voltage Regulators for Neural Implants

- A Miller-compensated reference circuit and an voltage regulator for use in neural implants was designed with the help of Dr. Lieuwe Leene. Its operation was analysed to gain understanding into Miller-compensated voltage regulators and verified by measurements.

- Building on the limitations of the previous topology, a second version of the circuit was created allowing its for switched-capacitor circuits achieving a simulated low-frequency PSRR of > 70 dB and a PSRR > 50 dB at 433 MHz, often used as a carrier frequency for wirelessly powered implants.

Chapter 6: Sigma-Delta Modulator for DC-Coupled Neural Interfaces

- A novel topology of a neural recording analogue front end based on $\Sigma\Delta$ modulation and digital rejection of DC offsets has been implemented and optimised for minimal power consumption.

- The circuit has been shown to allow the quantisation of LFP+EAP signals with a dynamic range of 51 dB and an SNDR of 40 dB while consuming a power of 31.1 µW. The occupied core area of 0.044 mm^2/channel makes this one of the smallest circuits of the kind found in literature.

A list of all research publications resulting from the presented work can be found in Appendix A.

7.2 What Could Have Been Done Differently

All the work carried out during the described research has allowed me to learn a lot about the practicalities and intricacies of integrated circuit design which I to this day believe to be an art as much as an engineering challenge. Looking back at some designs that were created, it is possible to see many areas where I would have done things differently given the experience and knowledge this project allowed me to gain.

Perhaps the most significant learning point for me was the fact that it can often be very challenging to try to push the possibilities of designs to their edge in terms of achieving minimal power consumption and occupied area. Although there are tools to simulate the performance of circuits that take into account manufacturing and other variations, measuring the manufactured circuits has revealed that the performance does not necessarily have to be the same as in simulations especially when minimal size devices are used. This is very much going to affect how I design circuits in the future in the sense of being more conservative. Likewise, if the circuits presented in this thesis were to be redesigned, I believe that being slightly more conservative with the target power consumption and used area would have resulted in overall better figures of merit.

7.3 Thoughts About Future Work

There are undoubtedly many ways in which the presented work can be expanded, starting from further investigation of the properties of electrodes and the suitability of niobium as a material for recording electrodes. It would be extremely interesting to conduct a more controlled study integrating precisely manufactured micro-fabricated electrodes of various materials and a low-noise analogue front-end on a chip allowing the direct measurement of noise profiles and obtaining a more direct conclusion on the presented hypothesis.

Having spent a considerable amount of time investigating the method of CT sampling, I remain very much interested in the topic and believe there is a lot to be researched both in terms of its fundamental theory as well as the practicalities of its implementation. One of the issues of the method that prevent the creation of even more efficient circuits is the fact that its application results in oversampling of the input signal. It remains a question if this can be prevented e.g. by the use of an adaptive quantisation level size or another method.

Additionally, the presented circuits always relied on a continuous time comparator that resulted in static power consumption. I have spent a lot of time thinking whether it is possible to create a CT ADC that would be completely activity-driven such that it would consume no power unless there was activity present in the input signal. This in the end boils down to a question of whether it is possible to compare two potentials without continually consuming power. Fundamentally, it seems that this should be possible if the power to trigger an action was drawn from the input signal upon its change. This arguably is a principle that is seen in balance weight scales that, equally, do not consume any power apart from the potential energy of the measured "input".

In theory it should be possible to apply a similar principle to the comparison of electrical charge, perhaps in the form of a MEMS balance charge scale. Another example of a circuit that in theory allows the implementation of a comparator not consuming any static power can be found in the CMOS Schmitt trigger. I believe it should be possible to create a CT ADC based on either of those methods that would only consume power upon a change in the input

signal, thus potentially leading to the first ADC of zero static power consumption.

Appendix A - List of Publications

First Author - Journal Papers

- M. Maslik, Y. Liu, T. S. Lande and T. G. Constandinou, "Continuous-Time Acquisition of Biosignals Using a Charge-Based ADC Topology," in IEEE Transactions on Biomedical Circuits and Systems, vol. 12, no. 3, pp. 471-482, June 2018.

First Author - Conference Papers

- M. Maslik, Y. Liu, T. S. B. Lande and T. G. Constandinou, "A Charge-Based Ultra-Low Power Continuous-Time ADC for Data Driven Neural Spike Processing," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, 2017, pp. 1-4.
- M. Maslik, T. S. B. Lande and T. G. Constandinou, "A Clockless Method of Flicker Noise Suppression in Continuous-Time Acquisition of Biosignals" 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), Cleveland, OH, 2018, pp. 1-4.

First Author - Book Chapters

- M. Maslik, L. Leene and T. G. Constandinou, "Analog Front-End Design for Neural Recording" Handbook of Neuroengineering, Springer, 2020, Springer, Singapore, pp 1-26

Additional Publications

- K. M. Szostak, F. Mazza, **M. Maslik**, L. B. Leene, P. Feng and T. G. Constandinou, "Microwire-CMOS integration of mm-scale neural probes for chronic local field potential recording," 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), Turin, 2017, pp. 1-4.
- L. B. Leene, **M. Maslik**, P. Feng, K. M. Szostak, F. Mazza and T. G. Constandinou, "Autonomous SoC for Neural Local Field Potential Recording in mm-Scale Wireless Implants," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-5.
- Luan, Song, Ian Williams, **Michal Maslik**, Yan Liu, Felipe De Carvalho, Andrew Jackson, Rodrigo Quian Quiroga, and Timothy G. Constandinou. "Compact standalone platform for neural recording with real-time spike sorting and data logging." Journal of neural engineering 15, no. 4 (2018): 046014.

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